Section 3. System Board I/O Controllers

Keyboard/Mouse Controller

The keyboard/mouse controller uses an Intel 8042 microprocessor. The keyboard is connected to the left-most of the two controller connectors in the rear of the system unit. This connector is dedicated to the keyboard.

The keyboard controller receives the serial data, checks the parity, translates keyboard scan codes (see "Keyboard Controller Command and Status Bytes" on page 3-5), and presents the data to the system as a byte of data at I/O address hex 0060. The interface can interrupt the system when data is available or can wait for polling from the microprocessor.

I/O address hex 0064 is the command/status port. When the system reads I/O address hex 0064, it receives status information from the keyboard controller. When the system writes to the port, the keyboard controller interprets the byte as a command.

Keyboard Password Security

The keyboard controller provides for a password security mechanism. Three commands are available regarding password operation:

A4	**Test Password Installed**
A5	**Load Security**
A6	**Enable Security.**

The system microprocessor can issue a Test Password Installed command to determine if a password is currently installed. This feature allows the controlling program to decide whether or not to write over the existing password.

The system microprocessor can issue a Load Security command and set a password in the keyboard controller at any time. Any existing password is lost, and the new password becomes the active password. The password must be installed in scan code format.

The system microprocessor must issue the Enable Security command to set the keyboard controller into Secure mode. At this point the keyboard controller does not pass any information along to the system microprocessor. The keyboard controller intercepts the keyboard data stream, continuously comparing it to the installed password pattern. Until a match is encountered, no keyboard or

mouse data is passed to the system microprocessor. When a match occurs, the state of the keyboard controller is restored and data is allowed to pass to the system microprocessor.

The password can be changed as often as the user chooses. No command to verify the installed password is provided. No commands are accepted by the keyboard controller when keyboard security is active.

Keyboard Controller Command and Status Bytes

Keyboard Controller Command Byte (Hex 0064, Write)

Figure 3-1 and Figure 3-2 on page 3-6 show the keyboard controller command and status bytes:

Figure 3-1. Keyboard Controller Command Byte, Port Hex 0064 Write

Bit	Function		
7	Reserved = 0		
6	IBM Keyboard Translate Mode	1=	Translate incoming scan codes to Scan Code Set 1*
		0=	No translation
5	Disable Mouse	1=	Drive clock low, disabling mouse interface
		0=	Drive clock high, enabling mouse interface
4	Disable Keyboard	1=	Drive clock low, disabling keyboard interface
		0=	Drive clock high, enabling keyboard interface
3	Reserved = 0		
2	System Flag		Placed in the system flag bit of the keyboard controller status register
1	Enable Mouse Interrupt	1=	Keyboard controller generates an interrupt when mouse data is written to output buffer
0	Enable Keyboard Interrupt	1=	Keyboard controller generates an interrupt when keyboard data is written to output buffer

* Used on the IBM Personal Computer and the IBM Personal Computer XT.

Keyboard Controller Status Byte (Hex 0064, Read)

Figure 3-2 shows the keyboard controller status byte:

Figure 3-2. Keyboard Controller Status Byte, Port Hex 0064 Read

Bit	Function
7	Parity Error
6	General Time Out
5	Mouse Output Buffer Full
4	Inhibit Switch
3	Command/Data
2	System Flag
1	Input Buffer Full
0	Output Buffer Full

Input Buffer

The input buffer (hex 0060) is an 8-bit write-only register. When the input buffer is written, a flag is set that indicates a data write. Data written to the input buffer is sent to the keyboard unless the keyboard controller is expecting a data byte following a keyboard controller command. Data should be written to the keyboard controller input buffer only if Input Buffer Full (bit 1) in the status byte (hex 0064) is equal to 0.

Output Buffers

The output buffer (hex 0060) is an 8-bit read-only register. When the output buffer is read, the keyboard controller uses it to send information to the system microprocessor. The information can be scan codes from the keyboard, data from a mouse, or data bytes that result from a command from the system microprocessor.

Keyboard Controller Commands

A command is a byte written to the keyboard controller through I/O address hex 0064. The following are the recognized keyboard controller commands (hex values).

20-3F **Read Keyboard Controller RAM** — Bits D5-D0 specify the address.

20 **Read Keyboard Controller Command Byte** — The keyboard controller puts the command byte in its output buffer (hex 0060).

60-7F **Write Keyboard Controller RAM** – Bits D5-D0 specify the address.

60 **Write Keyboard Controller Command Byte** – The keyboard controller puts the next byte of data written to I/O address hex 0060 in its command byte.

A4 **Test Password Installed** – This command checks for a password installed in the keyboard controller. The result, hex FA (password installed) or hex F1 (password not installed), is placed in the output buffer (I/O address hex 0060 and IRQ01).

A5 **Load Security** – This command initiates the password load procedure. The keyboard controller inputs from the data port until it detects a 0, which terminates password entry.

A6 **Enable Security** – This command enables the keyboard controller security feature. This command is valid only when a password pattern is currently loaded into the keyboard controller.

A7 **Disable Mouse Interface** – This command sets bit 5 of the keyboard controller command byte to 1, driving the clock line low which disables the mouse interface. Data is not sent or received.

A8 **Enable Mouse Interface** – This command clears bit 5 of the keyboard controller command byte to 0, which enables the mouse interface.

A9 **Interface Test** – This command causes the keyboard controller to test the mouse clock and data lines. The result is placed in the output buffer (I/O address hex 0060 and IRQ01) as shown in Figure 3-3.

Figure 3-3. Command A9 Test Results

Test Result (hex)	Meaning
00	No error was detected.
01	Mouse clock line is stuck low.
02	Mouse clock line is stuck high.
03	Mouse data line is stuck low.
04	Mouse data line is stuck high.

AA **Self Test** – This command causes the keyboard controller to perform internal diagnostic tests. Hex 55 is placed in the output buffer (I/O address hex 0060) if no errors are detected.

AB **Interface Test** – This command causes the keyboard controller to test the keyboard clock and data lines. The result is placed in the output buffer (I/O address hex 0060 and IRQ01) as shown in Figure 3-4 on page 3-8.

Figure 3-4. Command AB Test Results

Test Result (hex)	Meaning
00	No error was detected.
01	Keyboard clock line is stuck low.
02	Keyboard clock line is stuck high.
03	Keyboard data line is stuck low.
04	Keyboard data line is stuck high.

AC **Reserved**

AD **Disable Keyboard Interface** – This command sets bit 4 of the keyboard controller command byte to 1, driving the clock line low which disables the keyboard interface. Data will not be sent or received.

AE **Enable Keyboard Interface** – This command clears bit 4 of the keyboard controller command byte to 0, which enables the keyboard interface.

C0 **Read Input Port** – This command causes the keyboard controller to read its input port and place the data in the output buffer (hex 0060). This command should only be used if the output buffer is empty.

C1 **Poll Input Port Low** – Port 1 bits 0-3, in status bits 4-7.

C2 **Poll Input Port High** – Port 1 bits 4-7, in status bits 4-7.

D0 **Read Output Port** – This command causes the keyboard controller to read its output port and place the data in the output buffer (hex 0060). This command should only be used if the output buffer is empty.

D1 **Write Output Port** – The next byte of data written to I/O address hex 0060 is placed in the keyboard controller output port.

Note: Bit 0 of the keyboard controller output port is connected to System Reset. This bit should not be written low.

Note: System Control Port A should be used to set Alternate Gate A20 instead of writing to the output port. See page 3-167.

D2 **Write Keyboard Output Buffer** — The next byte written to the input buffer (hex 0060), is written to the output buffer (hex 0060) as if initiated by a device. An interrupt occurs if the interrupt is enabled in the command byte.

D3 **Write Mouse Output Buffer** — The next byte written to the input buffer (hex 0060) is written to the output buffer (hex 0060) as if initiated by a device. An interrupt occurs if the interrupt is enabled in the command byte.

D4 **Write to Mouse** — The next byte written to the input buffer (hex 0060) is transmitted to the mouse.

E0 **Read Test Inputs** — This command causes the keyboard controller to read its T0 and T1 inputs. This data is placed in the output buffer. Data bit 0 represents T0 and data bit 1 represents T1.

F0-FF **Pulse Output Port** — Bits 0 through 3 of the keyboard controller output port can be pulsed low for approximately 6 microseconds. Bits 0 through 3 of this command indicate which bits are to be pulsed. A 0 indicates that the bit should be pulsed. A 1 indicates the bit should not be modified.

Note: Bit 0 of the keyboard controller output port is connected to System Reset. Pulsing of this bit resets the system microprocessor.

Keyboard/Mouse Programming Considerations

The following are some programming considerations for the keyboard/mouse controller.

- Status register (I/O address hex 0064) can be read at any time.
- Output buffer (I/O address hex 0060) should be read only when the Output Buffer Full (bit 0) in the status register is 1.
- The Mouse Output Buffer Full (bit 5) in the status register indicates that the data in the output buffer (hex 0060) came from the mouse. This bit is valid only when the Output Buffer Full (bit 0) is 1.
- The output buffer (hex 0060) and status register (hex 0064) should be written only when the Input Buffer Full (bit 1) and the Output Buffer Full (bit 0) are 0s.
- The devices connected to the keyboard controller should be disabled before initiating a command that generates output. If output is generated, any value in the output buffer is overwritten.

Mouse/System Timings

Data transmissions to and from the mouse connector consist of an 11-bit data stream sent serially over the data line. Figure 3-5 on page 3-10 shows the function of each bit.

Figure 3-5. Mouse Data Stream Bit Definitions

Bit	Function
11	Stop Bit (always 1)
10	Parity Bit (odd parity)
9	Data Bit 7 (most-significant)
8	Data Bit 6
7	Data Bit 5
6	Data Bit 4
5	Data Bit 3
4	Data Bit 2
3	Data Bit 1
2	Data Bit 0 (least-significant)
1	Start Bit (always 0)

System Receiving Data

The following describes the typical sequence of events that takes place when the system is receiving data from the mouse. Figure 3-6 on page 3-11 shows a graphic representation of the timing relationships.

1. The mouse checks the clock line. If the line is inactive, output from the mouse is not allowed.
2. The mouse checks the data line. If the line is inactive, the mouse receives data from the system.
3. The mouse checks the clock line at intervals not exceeding 100 microseconds during transmission. If the system is holding the clock line inactive, the transmission is terminated. The system can terminate transmission anytime during the first 10 clock cycles.
4. A final check for terminated transmission is performed at least 5 microseconds after the 10th clock.
5. The system can hold the clock line inactive to inhibit the next transmission.
6. The system can set the data line inactive when it has data to transmit to the mouse. The start bit (always 0) sets the data line inactive.
7. The system raises the clock line to allow the next transmission.

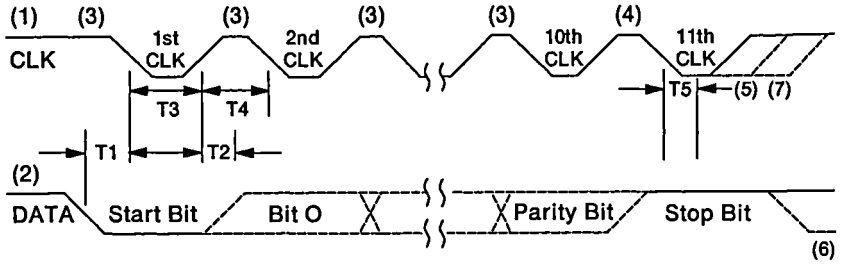


Figure 3-6. Receiving Data Timings

	Timing Parameter	Min/Max (microseconds)
T1	Time from DATA transition to falling edge of CLK	5 / 25
T2	Time from rising edge of CLK to DATA transition	5 / T4 - 5
T3	Duration of CLK inactive	30 / 50
T4	Duration of CLK active	30 / 50
T5	Time to mouse inhibit after clock 11 to ensure the mouse does not start another transmission	>0 / 50

System Sending Data

The following describes the typical sequence of events that takes place when the system is sending data to the mouse. Figure 3-7 on page 3-12 shows timing relationships.

1. The system checks for a mouse transmission in process. If a transmission is in process and beyond the 10th clock, the system must receive the data.
2. The mouse checks the clock line. If the line is inactive, an I/O operation is not allowed.
3. The mouse checks the data line. If the line is inactive, the system has data to transmit. The start bit (always 0) sets the data line inactive.
4. The mouse sets the clock line inactive. The system then places the first bit on the data line. Each time the mouse sets the clock line inactive, the system places the next bit on the data line until all bits are transmitted.
5. The mouse samples the data line for each bit while the clock line is active. Data must be stable within 1 microsecond after the rising edge of the clock line.
6. The mouse checks for a positive-level stop bit after the 10th clock. If the data line is inactive, the mouse continues to clock until the

data line becomes active, clocks the line-control bit, and at the next opportunity sends a Resend command to the system.

7. The mouse sets the data line inactive, producing the line-control bit.
8. The system can set the clock line inactive, inhibiting the mouse.

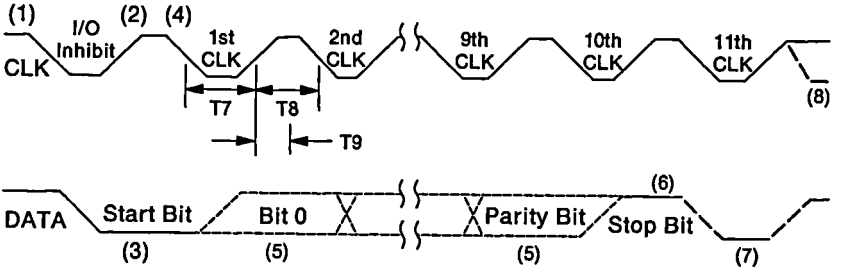


Figure 3-7. Sending Data Timings

	Timing Parameter	Min/Max (microseconds)
T7	Duration of CLK inactive	30 / 50
T8	Duration of CLK active	30 / 50
T9	Time from inactive to active CLK transition, used to time when the mouse samples DATA	5 / 25

Signals

The keyboard and mouse signals are driven by open-collector drivers pulled to 5 V dc through 4.7K ohm resistors. Figure 3-8 shows the characteristics of the signals.

Figure 3-8. Keyboard/Mouse Signals

Signal		
Sink Current	20 mA	Maximum
High-level Output Voltage	+5.0 V dc minus pullup	Minimum
Low-level Output Voltage	+0.5 V dc	Maximum
High-level Input Voltage	+2.0 V dc	Minimum
Low-level Input Voltage	+0.8 V dc	Maximum

Connector

The keyboard and the mouse connectors are 6-pin miniature DIN connectors. Figure 3-9 shows the voltages and signals assigned to the keyboard/mouse connectors.

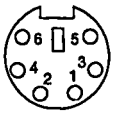


Figure 3-9. Keyboard/Mouse Connectors Voltage and Signal Assignments

Pin	I/O	Signal Name
1	I/O	Data
2	NA	Ground
3	NA	Ground
4	NA	+5 V dc
5	I/O	Clock
6	NA	Ground

Video Subsystem

The system video is generated by the IBM Video Graphics Array (VGA) and its associated circuitry. The associated circuitry consists of the video memory and a video digital-to-analog converter (DAC). The 256KB of video memory consists of four 64KB by 8 memory maps. The red, green, and blue (RGB) outputs from the video DAC drive analog displays with 31.5 KHz horizontal deflection.

All video modes available on the IBM Monochrome Display Adapter, IBM Color/Graphics Monitor Adapter, and IBM Enhanced Graphics Adapter are supported. All video modes supported by the video subsystem are available on all of the supported analog displays. Colors will be displayed as shades of gray when the monochrome analog display is used.

The modes available are:

- 640 by 480 graphics in both 2 and 16 colors
- 720 by 400 alphanumeric in both 16-color and monochrome
- 360 by 400 16-color alphanumeric
- 320 by 200 graphics with 256 colors.

In addition, all 200 line modes are double-scanned by the video subsystem and displayed as 400 lines on the display. This means that each 1-PEL-high horizontal scan line is displayed twice on the display.

The VGA interfaces with the system microprocessor and video memory. All data passes through the VGA when the system microprocessor writes to or reads from video memory. The VGA controls the arbitration for video memory between the system microprocessor and the cathode ray tube (CRT) controller function contained within the VGA. Programs do not need to wait for horizontal retrace to update the display buffer. The system microprocessor receives better performance when accessing the display buffer during non-active display times because there is less interference from the CRT controller.

Video memory addressing is controlled by the VGA. The starting address of the video memory is programmable to three different starting addresses for compatibility with previous video adapters. BIOS will program the VGA appropriately during a video mode set.

In alphanumeric modes, the system microprocessor writes ASCII character code and attribute data to the video memory maps 0 and 1, respectively. The character generator is stored in video map 2 and is loaded by BIOS during an alphanumeric video mode set. BIOS downloads the character generator data (character generator = font = character set) from system ROM. Three fonts are contained in ROM. Two fonts contain dot patterns identical to those provided by the IBM Monochrome Display Adapter, the IBM Color/Graphics Monitor Adapter, and the IBM Enhanced Graphics Adapter. The third font is an 8 x 16 character font. Up to eight 256-character fonts can be loaded into video memory map 2 at a time (the IBM Enhanced Graphics Adapter allows up to four fonts). A BIOS interface exists to load user-defined fonts. As on the IBM Enhanced Graphics Adapter, a register selects which font is actually used to form characters. Also, as on the IBM Enhanced Graphics Adapter, the intensity bit in the attribute byte may be redefined as a switch between two 256-character fonts. This allows 512 characters to be displayed on the screen at one time. See "Character Map Select Register" on page 3-61 and "RAM-Loadable Character Generator" on page 3-97.

The VGA formats the information stored in video memory into an 8-bit digital value that is sent to the video DAC. This 8-bit value allows access to a maximum of 256 registers inside the video DAC. For example, in the two-color graphics modes, only two different 8-bit values would be presented to the video DAC. In the 256-Color Graphics mode, 256 different 8-bit values would be presented to the video DAC. Each register inside the video DAC contains a color value that is selected from a choice of over 256,000 colors.

The video DAC outputs three analog color signals (red, green, and blue) that are sent to the display connector. The monochrome analog display uses only the green analog output. This output is used to determine the shade of gray that is displayed.

The video subsystem supports attachment of only 31.5 KHz direct-drive analog displays. Other IBM displays are not supported because they have digital interfaces, or have a different horizontal sweep frequency.

A BIOS call enables or disables the VGA. Disable means that the VGA will not respond to video memory or I/O reads or writes. The contents of registers and video memory are preserved with the values present when the disable is invoked. Because of this, the VGA continues to generate valid video output if it was doing so before it was disabled.

Compatibility with other hardware is best achieved by using the BIOS interface whenever possible. If an application is forced to write directly to the VGA, the following rules should be followed:

- To program address registers, all currently reserved bits should be set to 0 to maximize compatibility with other hardware.
- To program data registers, all currently reserved bits should be read out and written back unmodified to maximize compatibility with other hardware.

Previous video adapters required that the video mode used correspond to the display attached. For example, the IBM Enhanced Graphics Adapter required that the Enhanced Color Display be attached to run mode hex 3*, and required that the monochrome display be attached to run mode hex 7. All the modes supported by the VGA are supported by the IBM 31.5 KHz direct-drive analog displays. Colors are displayed as shades of gray when the monochrome analog display is connected. Circuitry on the system board detects which type of analog display is connected (color or monochrome). BIOS maps (sums) the colors into shades of gray.

Figure 3-10 on page 3-17 is a block diagram of the video subsystem on the system board.

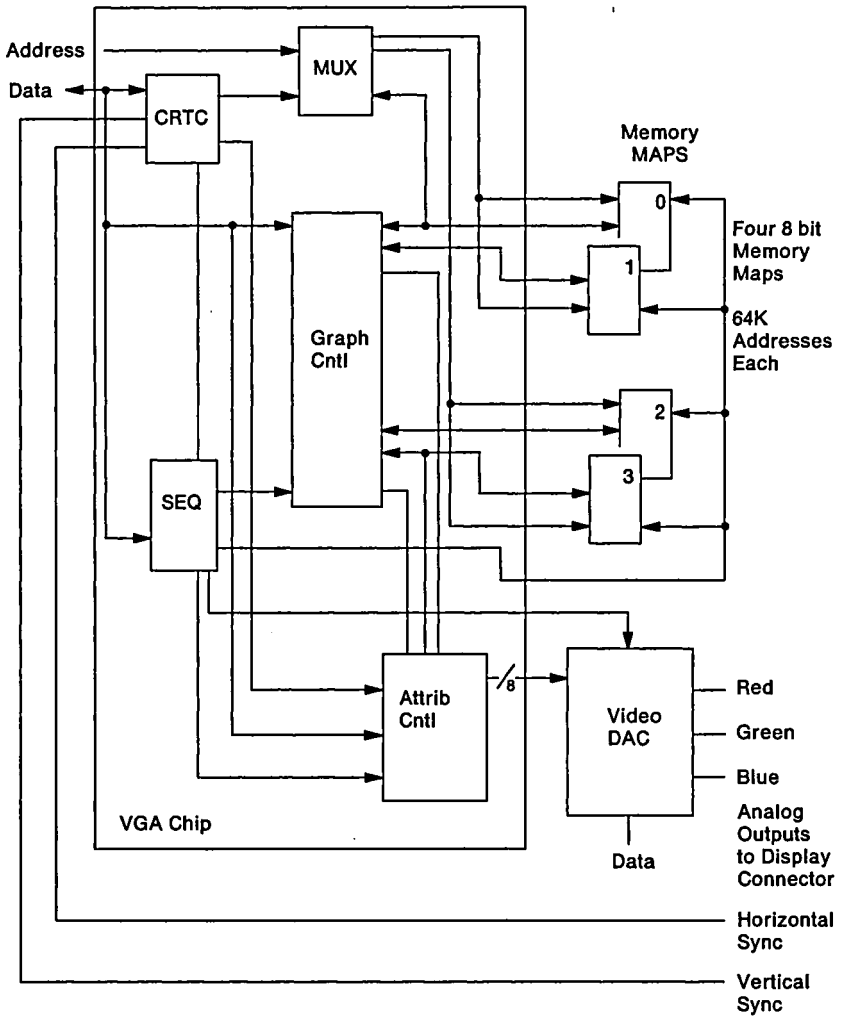


Figure 3-10. Video Subsystem Block Diagram

VGA Components

Most of the logic for the VGA is contained in one module. This module contains all the circuits necessary to generate the timing for the video memory and generates the video information that goes to the video DAC.

BIOS ROM

Software support is provided by video BIOS. Video BIOS is part of the system BIOS. BIOS is contained in the read-only memory (ROM) on the system board. This ROM BIOS contains the character generators and the control code to run the video subsystem.

Support Logic

Two clock sources (25.175 MHz and 28.322 MHz) provide the dot rate. The clock source is selected by setting a bit in a sequencer register. This is done by BIOS when a mode set is done.

The digital video output is sent to the video digital-to-analog converter (DAC), which contains a color look-up table. Three analog signals (red, green, blue) are output from the DAC and are sent to the display. (See "Attribute Controller" on page 3-21.) The sync signals to the monitor are TTL levels. The analog video signals are 0 to 0.7 volts.

The maximum number of colors displayed is 16 out of 256K, except mode hex 13, which can display 256 out of 256K. The maximum number of shades of gray is 16 out of 64, except mode hex 13, which can display 64 out of 64 shades of gray.

Video Graphics Array Major Components

The video graphics array has four major components:

- CRT controller
- Sequencer
- Graphics controller
- Attribute controller.

CRT Controller

The cathode ray tube (CRT) controller generates horizontal and vertical synchronous timings, addressing for the regenerative buffer, cursor and underline timings, and refresh addressing for the dynamic RAMs.

Sequencer

The sequencer generates basic memory timings for the dynamic RAMs and the character clock for controlling regenerative memory fetches. It allows the system microprocessor to access memory during active display intervals by inserting dedicated system microprocessor memory cycles periodically between the display memory cycles. Map Mask registers are available to protect entire memory maps from being changed.

The graphics controller is the interface between video memory and either the attribute controller during active display times or the system microprocessor during video memory reads or writes. During display times, memory data is latched and sent to the attribute controller. In all points addressable (APA) modes, the parallel memory data is converted to serial bit-plane data before being sent. In alphanumeric (A/N) modes, the parallel attribute data is sent directly. During a system microprocessor write or read to video memory, the graphics controller can perform logical operations on the memory data before it reaches video memory or the system microprocessor data bus, respectively. These operations include four logical write modes and two logical read modes. These features allow enhanced operations such as a color-compare read mode, individual bit masking during write modes, 32-bit writes in a single memory cycle, and writing to the display buffer on non-byte boundaries.

Figure 3-11 is a block diagram of the graphics controller.

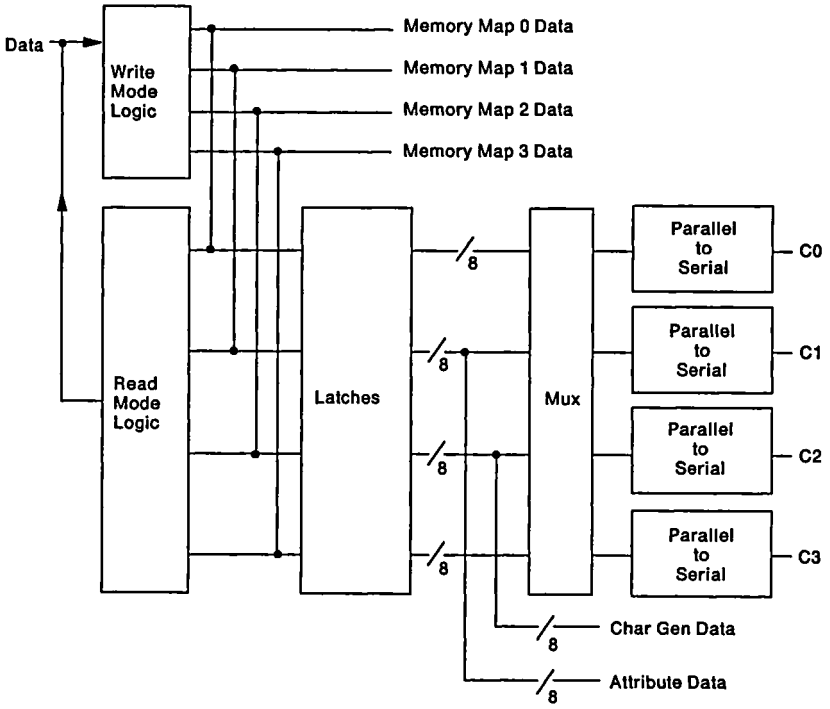


Figure 3-11. Graphics Controller Block Diagram

Attribute Controller

The attribute controller takes in data from video memory through the graphics controller and formats it for display. Incoming attribute data in A/N mode, and serialized bit-plane data in APA mode is converted to an 8-bit output digital color value. Each output color value is selected from an internal color palette of 64 possible colors (except in 256-Color mode). The output color value is sent to the integrated DAC, where it is used as an address into an 18-bit color register whose value is in turn converted to three analog color signals that drive the display. Blinking, underlining, cursor insertion, and PEL panning are also controlled by the attribute controller.

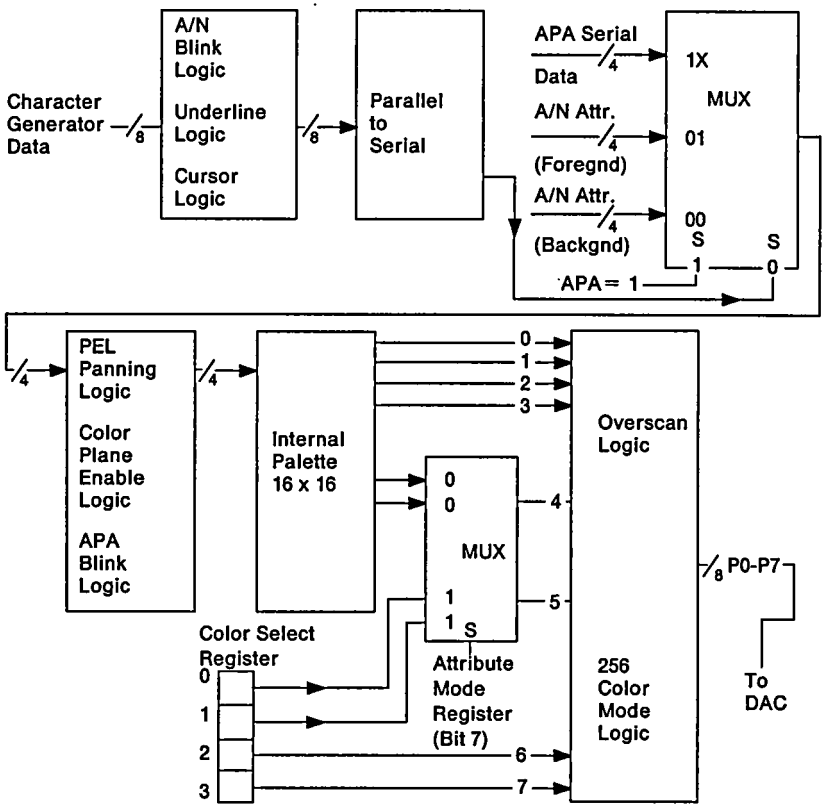


Figure 3-12. Attribute Controller Block Diagram

Modes of Operation

Figure 3-13 describes the modes supported by BIOS on IBM 31.5 KHz direct-drive analog color and monochrome displays.

Figure 3-13. BIOS Video Modes

Mode (hex)	Type	Alpha Format	Buffer Start	Box Size	Max Pgs.	Vert. Freq.	PELS	
	Colors							
0, 1	A/N	16/256K	40 x 25	B8000	8 x 8	8	70 Hz	320 x 200
2, 3	A/N	16/256K	80 x 25	B8000	8 x 8	8	70 Hz	640 x 200
0*, 1*	A/N	16/256K	40 x 25	B8000	8 x 14	8	70 Hz	320 x 3/0
2*, 3*	A/N	16/256K	80 x 25	B8000	8 x 14	8	70 Hz	640 x 350
0+, 1+	A/N	16/256K	40 x 25	B8000	9 x 16	8	70 Hz	360 x 400
2+, 3+	A/N	16/256K	80 x 25	B8000	9 x 16	8	70 Hz	720 x 400
4, 5	APA	4/256K	40 x 25	B8000	8 x 8	1	70 Hz	320 x 200
6	APA	2/256K	80 x 25	B8000	8 x 8	1	70 Hz	640 x 200
7	A/N	-	80 x 25	B0000	9 x 14	8	70 Hz	720 x 350
7+	A/N	-	80 x 25	B0000	9 x 16	8	70 Hz	720 x 400
D	APA	16/256K	40 x 25	A0000	8 x 8	8	70 Hz	320 x 200
E	APA	16/256K	80 x 25	A0000	8 x 8	4	70 Hz	640 x 200
F	APA	-	80 x 25	A0000	8 x 14	2	70 Hz	640 x 350
10	APA	16/256K	80 x 25	A0000	8 x 14	2	70 Hz	640 x 350
11	APA	2/256K	80 x 30	A0000	8 x 16	1	60 Hz	640 x 480
12	APA	16/256K	80 x 30	A0000	8 x 16	1	60 Hz	640 x 480
13	APA	256/256K	40 x 25	A0000	8 x 8	1	70 Hz	320 x 200

* Enhanced modes (EGA)
\+ Enhanced modes (VGA)

When the color display is used, each color is selected from a palette of over 256,000 colors.

When the monochrome display is used, the colors are displayed as shades of gray. Each shade of gray is selected from a palette of 64 shades.

Modes hex 0 through 6 emulate the support provided by the IBM Color/Graphics Monitor Adapter.

Modes hex 0, 2, and 4 are identical to modes hex 1, 3, and 5, respectively. On the IBM Color/Graphics Monitor Adapter there is a difference in these modes. In modes hex 0, 2, and 4, the color burst was turned off. Color burst is not provided by the video subsystem. Mode hex 3+ is the default mode with an analog color display attached to the system. Mode hex 7+ is the default mode with an analog monochrome display attached to the system.

Mode hex 7 emulates the support provided by the IBM Monochrome Display Adapter.

Modes hex 0*, 1*, 2*, 3*, D, E, F, and 10 emulate the support provided by the IBM Enhanced Graphics Adapter.

Double-scan means that each horizontal scan line is displayed twice. This is used for 200-line modes, which are displayed as 400 lines. Border support depends on the BIOS mode selected. Figure 3-14 shows double-scan and border support.

Figure 3-14. BIOS Double-Scan and Border Support

Mode (hex)	Double Scan	Border Support
0, 1	Yes	No
2, 3	Yes	Yes
0*, 1*	No	No
2*, 3*	No	Yes
0+, 1+	No	No
2+, 3+	No	Yes
4, 5	Yes	No
6	Yes	Yes
7	No	Yes
7+	No	Yes
D	Yes	No
E	Yes	Yes
F	No	Yes
10	No	Yes
11	No	Yes
12	No	Yes
13	Yes	Yes

* Enhanced modes (EGA)
\+ Enhanced modes (VGA)

Display Support

The video subsystem supports attachment of 31.5 KHz horizontal sweep frequency direct-drive analog displays. These displays have a vertical sweep frequency capability of 60 to 70 cycles per second, providing extended color and sharpness and reduced flicker in most modes. Other IBM displays are not supported because they have digital interfaces, or have a different horizontal and vertical sweep frequency. Figure 3-15 summarizes the analog display characteristics.

Figure 3-15. IBM 31.5 KHz Direct-Drive Analog Displays

Parameter	Color	Monochrome
Horizontal Scan Rate	31.5 KHz	31.5 KHz
Vertical Scan Rate	60 to 70 Hz	60 to 70 Hz
Video Bandwidth	28 MHz	28 MHz
Displayable Colors*	256/256K Maximum	64/64 Shades Gray
Maximum Horizontal Resolution	720 PELs	720 PELs
Maximum Vertical Resolution	480 PELs	480 PELs

* Controlled by Video Circuit.

Since both color and monochrome displays run at the same sweep rate, all modes work on either type. The vertical size of the display is controlled by the polarity of the vertical and horizontal sync pulses. This is done so that 350, 400, or 480 lines can be displayed without adjusting the display. (See "Display Connector Timing (SYNC Signals)" on page 3-105.)

Video Subsystem Programmable Option Select

The video subsystem supports Programmable Option Select (POS). When the POS sleep bit is set, the video subsystem does not respond to any memory or I/O reads or writes. Video is still generated if the video subsystem is programmed to do so. POS must be enabled for video subsystem operation.

The implementation of POS for the video subsystem is as follows:

- When in Setup mode (I/O address hex 0094, bit 5 equals 0), the VGA responds to a single option select byte at I/O address hex 0102 and treats the LSB (bit 0) of that byte as the VGA sleep bit. When the LSB is 0, the VGA does not respond to commands, addresses, or data on the data bus. When the LSB is 1, the VGA responds. If the VGA was set up and is generating video output when the LSB is set to 0, the output is still generated.
- The VGA responds only to address hex 0102 when in the Setup mode. No other addresses are valid at that time. Conversely, the VGA ignores address hex 0102 when in the Enabled mode (I/O address hex 0094, bit 5 equals 1), and decodes normal I/O and memory addresses.

Note: When VGA is disabled, accesses to the video DAC registers are disabled.

When the system is powered on, POST initializes and enables the video subsystem.

For information on BIOS calls to enable or disable the VGA, see *BIOS Interface Technical Reference for IBM PS/1™ Computer.*

Alphanumeric Modes

This section describes the alphanumeric modes supported by the video subsystem and BIOS. Note that the colors in this section are generated when the BIOS is used to set the mode. BIOS initializes the video subsystem and the video DAC palette to generate these colors. If the video DAC palette is changed, different colors are generated.

The alphanumeric modes are modes hex 0 - 3 and 7. The mode chart lists the variations of these modes. The data format for alphanumeric modes is the same as the data format on the IBM Color/Graphics Monitor Adapter, the IBM Monochrome Display Adapter, and the IBM Enhanced Graphics Adapter (EGA). As in the EGA, bit 3 of the attribute byte may be redefined by the Character Map Select register to act as a switch between character sets. This gives the programmer access to 512 characters at one time.

When an alphanumeric mode is selected, the BIOS transfers character patterns from the ROM to map 2. The system microprocessor stores the character data in map 0, and the attribute data in map 1. The programmer can view maps 0 and 1 as a single buffer in alphanumeric modes. The CRT controller generates sequential addresses, and fetches one character code byte and one attribute byte at a time. The character code and row scan count are combined to address map 2, which contains the character generators. The appropriate dot patterns are then sent to the palette in the attribute section, where color is assigned according to the attribute data.

Every display-character position in the alphanumeric mode is defined by 2 bytes in the display buffer. Figure 3-16 shows the 2-byte character/attribute format used in both the color/graphics and the monochrome emulation modes.

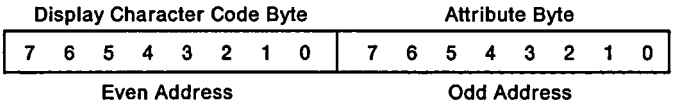


Figure 3-16. Character/Attribute Format

See Section 11, "Characters and Keystrokes" on page 11-1 for characters loaded during BIOS mode sets.

Figure 3-17 shows the functions of the attribute byte.

Figure 3-17. Attribute Byte Functions

Attribute Function	Attribute Byte 7 6 5 4 B/I R G B Background	Attribute Byte 3 2 1 0 I/CS R G B Foreground
Normal (White on Black)	B/I 0 0 0	I/CS 1 1 1
Reverse (Black on White)	B/I 1 1 1	I/CS 0 0 0
Nondisplay (Black)	B/I 0 0 0	I/CS 0 0 0
Nondisplay (White)	B/I 1 1 1	I/CS 1 1 1
Mono=Underline / Color=Blue	B/I 0 0 0	I/CS 0 0 1

I = Highlighted
B = Blinking Foreground (Character)
CS = Character select

The BIOS defaults on a mode set are blink for bit 7 (B/I) and intensity for bit 3 (I/CS).

Figure 3-18 shows the attribute byte definitions.

Figure 3-18. Attribute Byte Definitions

Bit	Color	Function
7	B/I	Blinking/Background Intensity
6	R	Red Background
5	G	Green Background
4	B	Blue Background
3	I/CS	Intensity/Character Select
2	R	Red Foreground
1	G	Green Foreground
0	B	Blue Foreground

See "Character Map Select Register" on page 3-61 and "Attribute Mode Control Register" on page 3-89.

Any other code combination produces white-on-white in the monochrome emulation mode and the following colors in the color emulation mode:

Figure 3-19. Attribute Byte Colors

I	R	G	B	Color
0	0	0	0	Black
0	0	0	1	Blue
0	0	1	0	Green
0	0	1	1	Cyan
0	1	0	0	Red
0	1	0	1	Magenta
0	1	1	0	Brown
0	1	1	1	White
1	0	0	0	Gray
1	0	0	1	Light Blue
1	0	1	0	Light Green
1	0	1	1	Light Cyan
1	1	0	0	Light Red
1	1	0	1	Light Magenta
1	1	1	0	Yellow
1	1	1	1	White (High Intensity)

Both 40-column and 80-column alphanumeric modes are supported. The 40-column alphanumeric modes (all variations of modes hex 0 and 1) have the following features:

- Display up to 25 rows of 40 characters each
- Require 2,000 bytes of read/write memory per page
- One character and one attribute for each character.

The 80-column alphanumeric modes (all variations of modes hex 2, 3, and 7) have the following features:

- Display up to 25 rows of 80 characters each
- Require 4,000 bytes of read/write memory per page
- One character and attribute for each character.

Graphics Modes

This section describes the graphics modes supported by the video subsystem and BIOS. Note that the colors in this section are generated when the BIOS is used to set the mode. BIOS initializes the video subsystem and the video DAC palette to generate these colors. If the video DAC palette is changed, different colors are generated.

320 x 200 Four-Color Graphics (Modes Hex 4 and 5)

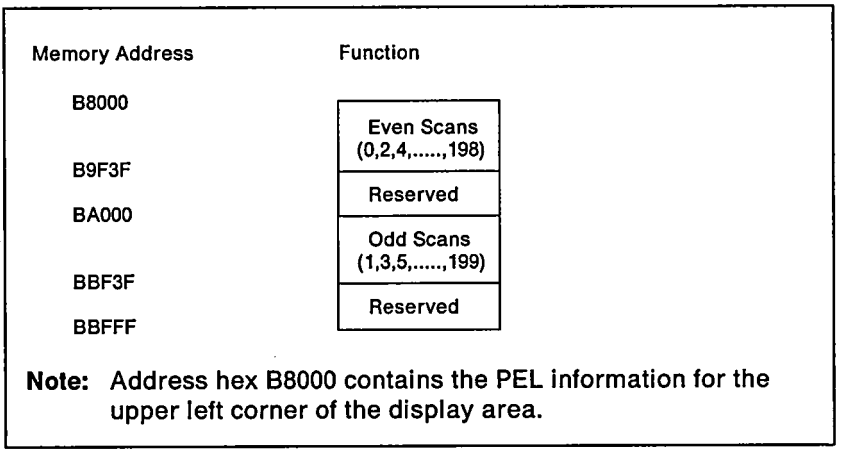
Addressing, mapping, and data format are the same as the 320-by-200-PEL mode of the IBM Color/Graphics Monitor Adapter. The display buffer is configured at hex B8000. Bit image data is stored in memory maps 0 and 1. The two bit planes (C0 and C1) are each formed from bits from both memory maps.

This mode has the following features:

- Contains a maximum of 200 rows of 320 PELs
- Selects one of four colors for each PEL
- Requires 16,000 bytes of read/write memory
- Uses memory-mapped graphics
- Double-scanned on display to 400 rows
- Formats four PELs-per-byte as shown in Figure 3-20.
- Organizes graphics memory in two banks of 8,000 bytes using the format as shown in Figure 3-21 on page 3-29.

Figure 3-20. PEL Format, Modes Hex 4 and 5

Bit	Function
7	C1 - First Display PEL
6	C0 - First Display PEL
5	C1 - Second Display PEL
4	C0 - Second Display PEL
3	C1 - Third Display PEL
2	C0 - Third Display PEL
1	C1 - Fourth Display PEL
0	C0 - Fourth Display PEL



Note: Address hex B8000 contains the PEL information for the upper left corner of the display area.

Figure 3-21. Video Memory Format

Color selection is determined as shown in Figure 3-22.

Figure 3-22. Color Selections, Modes Hex 4 and 5

C1	C0	Color Selected	
0	0	Black	
0	1	Light Cyan	* Green
1	0	Light Magenta	* Red
1	1	Intensified White	* Brown

* Selectable by a video BIOS call.

640 x 200 Two-Color Graphics (Mode Hex 6)

Addressing, mapping, and data format are the same as the 640-by-200-PEL black and white mode of the IBM Color/Graphics Monitor Adapter. The display buffer is configured at hex B8000. Bit image data is stored in memory map 0 and comprises a single bit plane (C0).

This mode has the following features:

- Contains a maximum of 200 rows of 640 PELs.
- Supports two colors only.
- Requires 16,000 bytes of read/write memory.
- Addressing and mapping procedures are the same as 320-by-200 two- and four-color graphics, but the data format is different. In this mode, each bit in memory is mapped to a PEL on the screen.
- Double-scanned on display to 400 rows.
- Formats 8 PELs per byte in the following manner:

Figure 3-23. PEL Format, Mode Hex 6

Bit	Function
7	First Display PEL
6	Second Display PEL
5	Third Display PEL
4	Fourth Display PEL
3	Fifth Display PEL
2	Sixth Display PEL
1	Seventh Display PEL
0	Eighth Display PEL

The bit definition for each PEL is 0 for Black and 1 for Intensified White.

640 x 480 Two-Color Graphics (Mode Hex 11)

This mode provides two-color graphics with the same data format as mode 6. Addressing and mapping is shown under "Video Memory Organization" on page 3-35.

The bit image data is stored in map 0 and comprises a single bit plane (C0). A sequential buffer starting at address hex A0000 is provided. Location hex A0000 contains the byte with information for the first 8 PELs; location hex A0001 contains information for the second 8 PELs, and so on. The bit definition for each PEL is 0 for Black and 1 for Intensified White.

640 x 350 Graphics (Mode Hex F)

This mode emulates the EGA graphics mode on the IBM Monochrome Display with the following attributes: black, white, blinking white, and intensified white. Resolution of 640-by-350 requires 56KB to support four attributes. Maps 0 and 2 are used in this mode. Map 0 is the video bit plane, and map 2 is the intensity bit plane. Both planes reside at address hex A0000.

Two bits, one from each bit plane, define one PEL on the screen. Figure 3-24 shows the PEL bit definitions. C0 is the video bit plane and C2 is the intensity bit plane.

Figure 3-24. PEL Bit Definitions

C2	C0	PEL Color
0	0	Black
0	1	White
1	0	Blinking White
1	1	Intensified White

The byte organization in memory is linear. The first 8 PELs on the screen are defined by the contents of memory in location hex A0000, the second 8 PELs by location hex A0001, and so on. The first PEL within any one byte is defined by bit 7 in the byte. The last PEL within the byte is defined by bit 0 in the byte.

Since both bit planes reside at address hex A0000, the user must select which plane or planes to update. This is accomplished by the Map Mask register of the sequencer. (See "Video Memory Organization" on page 3-35.)

16-Color Graphics (Modes Hex D, E, 10 and 12)

These modes support graphics in 16 colors. The bit image data is stored in all four memory maps in these modes. Each memory map contains the data for one bit plane. Each bit plane represents a color as shown below. The bit planes are denoted as C0, C1, C2, and C3, respectively.

C0 = Blue PELs
C1 = Green PELs
C2 = Red PELs
C3 = Intensified PELs

Four bits (one from each plane) define one PEL on the screen. Figure 3-25 shows the color combinations.

Figure 3-25. Palette Colors

C3	C2	C1	C0	Color
0	0	0	0	Black
0	0	0	1	Blue
0	0	1	0	Green
0	0	1	1	Cyan
0	1	0	0	Red
0	1	0	1	Magenta
0	1	1	0	Brown
0	1	1	1	White
1	0	0	0	Dark Gray
1	0	0	1	Light Blue
1	0	1	0	Light Green
1	0	1	1	Light Cyan
1	1	0	0	Light Red
1	1	0	1	Light Magenta
1	1	1	0	Yellow
1	1	1	1	Intensified White

The display buffer resides at address hex A0000. The Map Mask register is used to select any or all of the maps to be updated when a memory write to the display buffer is executed by the system microprocessor.

256-Color Graphics (Mode Hex 13)

This mode provides graphics with the capability to display 256 colors on the screen at one time.

The display buffer is linear, starting at address hex A0000, and is 64,000 bytes long. The first location contains the 8-bit color for the upper left PEL. The second byte contains the second PEL, and so on for 64,000 PELs (320-by-200). The bit image data is stored in all four memory maps and comprises four bit planes. The four bit planes are sampled twice to produce eight bit planes that address the video DAC.

The internal palette of the video subsystem is not used to select colors. It is set by BIOS and should not be changed. The external palette in the video DAC is programmed by the BIOS such that the first 16 locations contain colors that are compatible with colors of other modes (See Figure 3-26). The second 16 locations contain 16 evenly spaced gray shades. The remaining 216 locations are loaded, based on a hue-saturation-intensity model tuned to provide a usable, generic color set that covers a wide range of color values.
Figure 3-26 shows the colors that are compatible with colors of other modes.

Figure 3-26. Attribute Byte

Attribute Byte								Analog Output Color
C7	C6	C5	C4	C3	C2	C1	C0	
0	0	0	0	0	0	0	0	Black
0	0	0	0	0	0	0	1	Blue
0	0	0	0	0	0	1	0	Green
0	0	0	0	0	0	1	1	Cyan
0	0	0	0	0	1	0	0	Red
0	0	0	0	0	1	0	1	Magenta
0	0	0	0	0	1	1	0	Brown
0	0	0	0	0	1	1	1	White
0	0	0	0	1	0	0	0	Dark Gray
0	0	0	0	1	0	0	1	Light Blue
0	0	0	0	1	0	1	0	Light Green
0	0	0	0	1	0	1	1	Light Cyan
0	0	0	0	1	1	0	0	Light Red
0	0	0	0	1	1	0	1	Light Magenta
0	0	0	0	1	1	1	0	Yellow
0	0	0	0	1	1	1	1	Intensified White

The video DAC palette can be programmed from a selection of over 256,000 different colors.

This mode has the following features:

- Contains a maximum of 200 rows of 320 PELs
- Double-scanned on display to 400 rows
- Selects one of 256 colors for each PEL
- Requires 64,000 bytes of read/write memory
- Uses memory-mapped graphics
- Uses 1 byte of memory for each PEL.

Video Memory Organization

The video display buffer on the system board consists of 256KB of dynamic read/write memory configured as four 64KB video maps.

The address of the display buffer can be changed to remain compatible with other video adapters and application software. Four locations are provided. The buffer can be configured at segment address hex A0000 for a length of 128KB, at hex A0000 for a length of 64KB, at hex B0000 for a length of 32KB, or at hex B8000 for a length of 32KB.

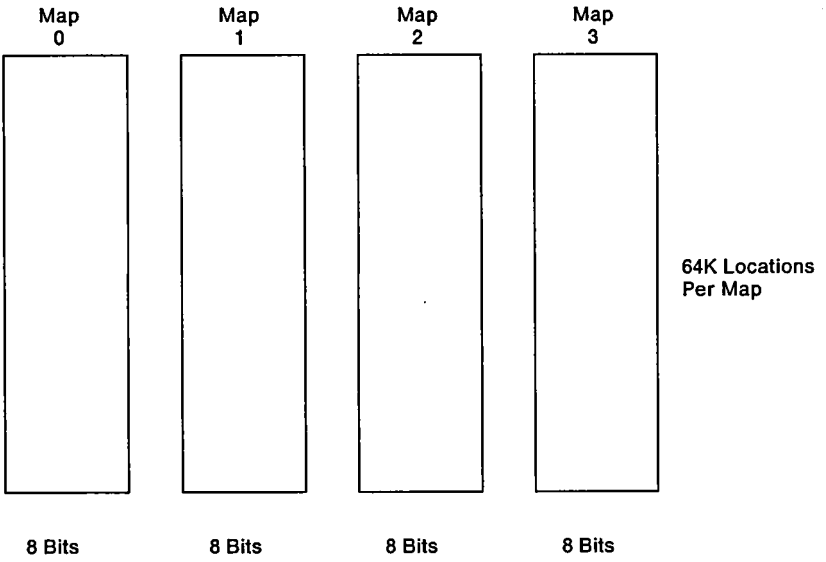


Figure 3-27. 256KB Video Memory Map

Maps 0 through 3 usually form bit planes 0 through 3:

Map 0 = Bit Plane 0

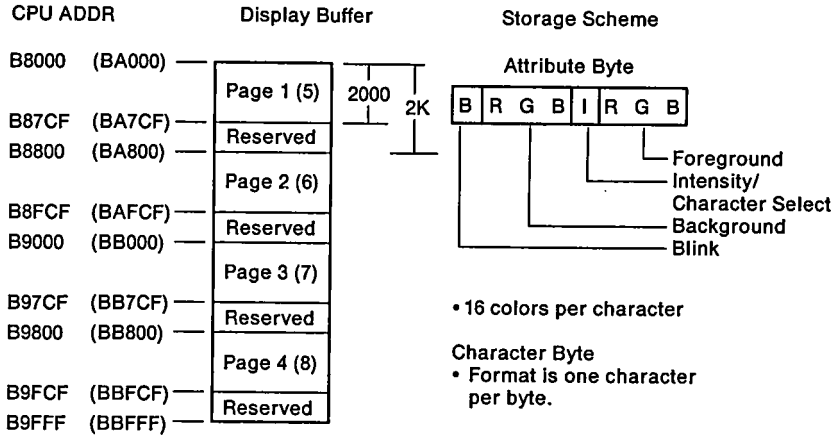
Map 1 = Bit Plane 1

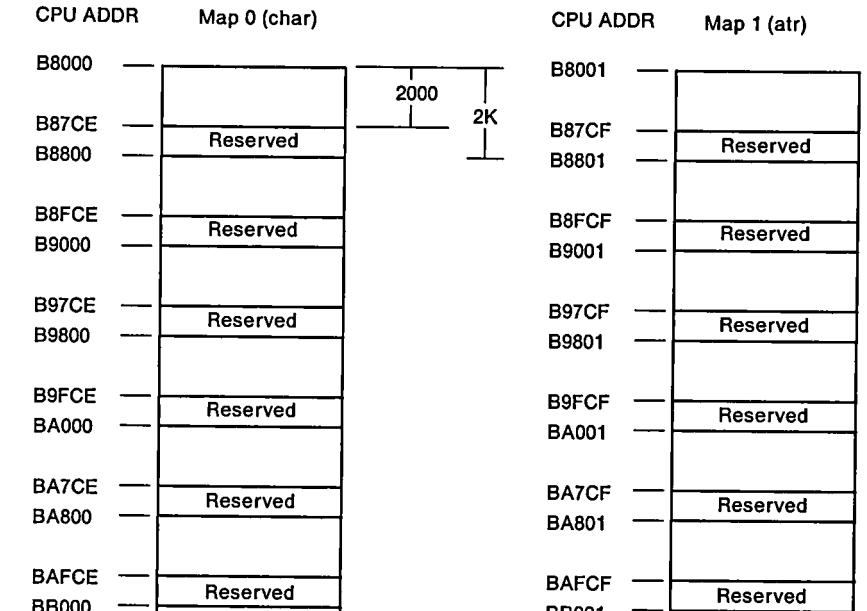
Map 2 = Bit Plane 2

Map 3 = Bit Plane 3

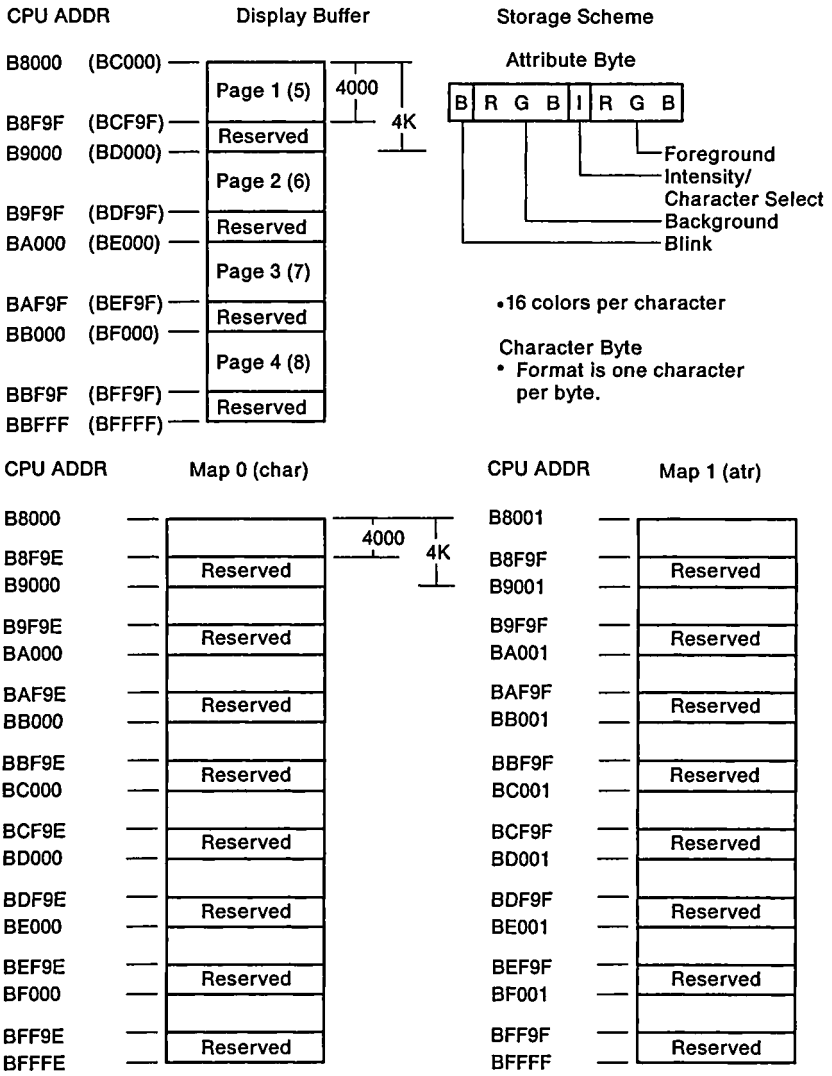
In mode hex 13, each of the four bit planes is formed with data from all four maps. The four bits are sampled twice internally to produce the eight bit values needed to select 256 colors.

Modes Hex 0, 1 (All Variations of Modes Hex 0 and 1)

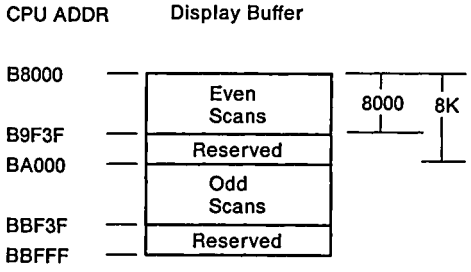


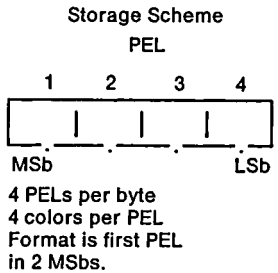


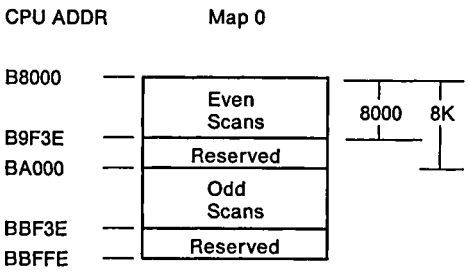
Modes Hex 2, 3 (All Variations of Modes Hex 2 and 3)

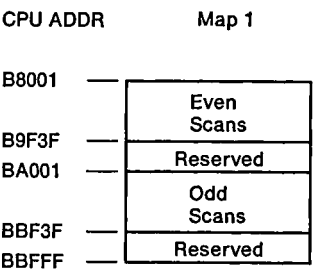


Modes Hex 4, 5

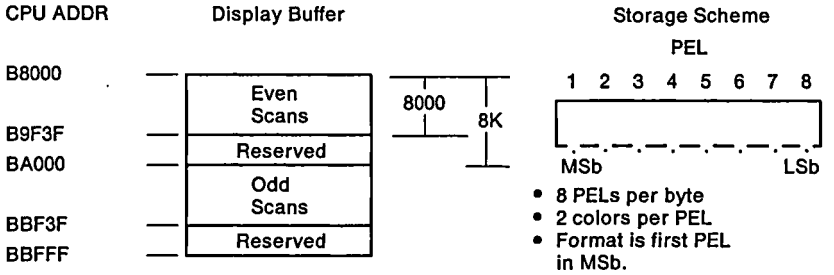

CPU ADDR
Display Buffer
B8000
B9F3F
BA000
BBF3F
BBFFF
Even Scans
Reserved
Odd Scans
Reserved
8000
8K

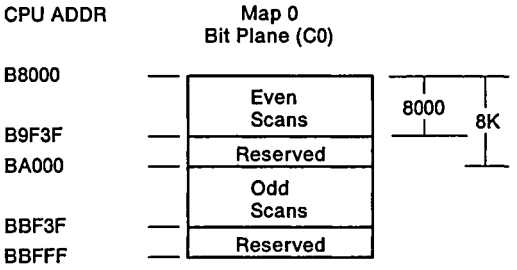

Storage Scheme
PEL
1
2
3
4
MSb
LSb
• 4 PELs per byte
• 4 colors per PEL
• Format is first PEL in 2 MSbs.


CPU ADDR
Map 0
B8000
B9F3E
BA000
BBF3E
BBFFE
Even Scans
Reserved
Odd Scans
Reserved
8000
8K

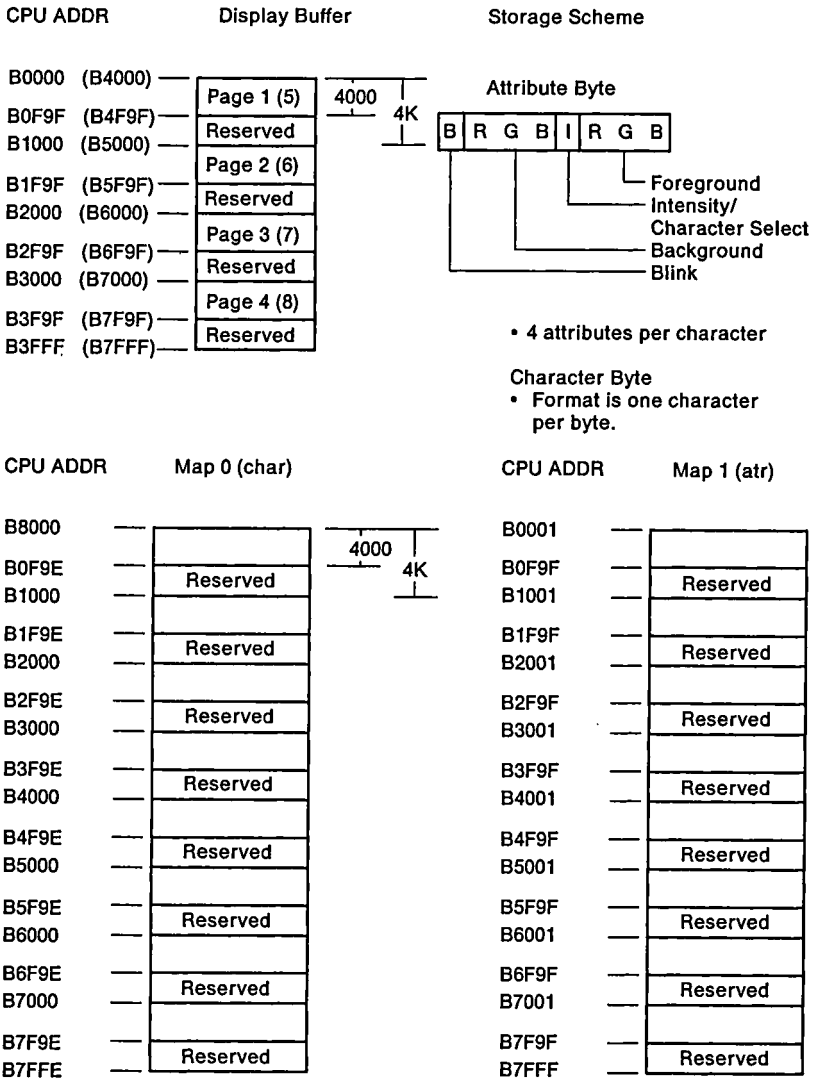

CPU ADDR
Map 1
B8001
B9F3F
BA001
BBF3F
BBFFF
Even Scans
Reserved
Odd Scans
Reserved

Mode Hex 6

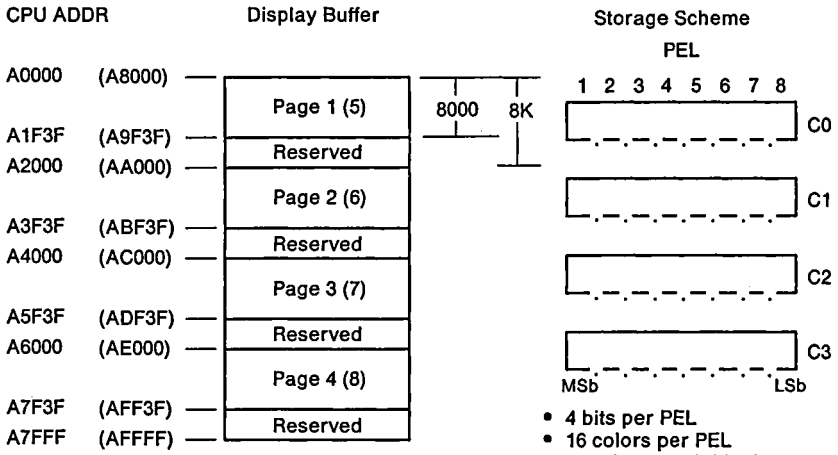

CPU ADDR
Display Buffer
Storage Scheme
PEL
1 2 3 4 5 6 7 8
B8000
Even Scans
B9F3F
Reserved
BA000
Odd Scans
BBF3F
Reserved
BBFFF
8000
8K
MSb
LSb
• 8 PELs per byte
• 2 colors per PEL
• Format is first PEL in MSb.


CPU ADDR
Map 0
Bit Plane (C0)
B8000
Even Scans
B9F3F
Reserved
BA000
Odd Scans
BBF3F
Reserved
BBFFF
8000
8K

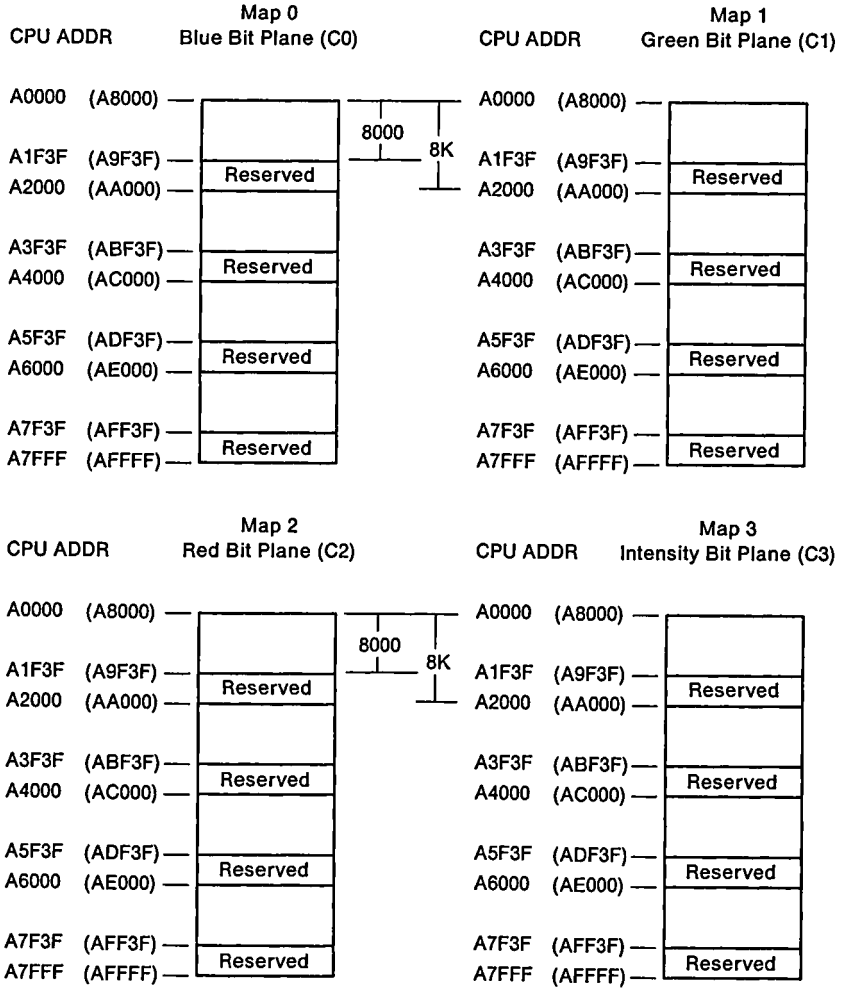
Mode Hex 7 (All Variations of Mode Hex 7)



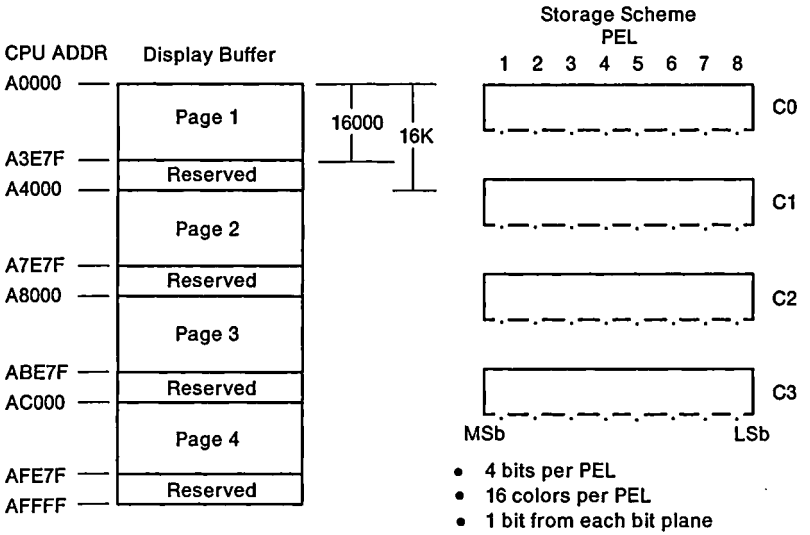
Mode Hex D



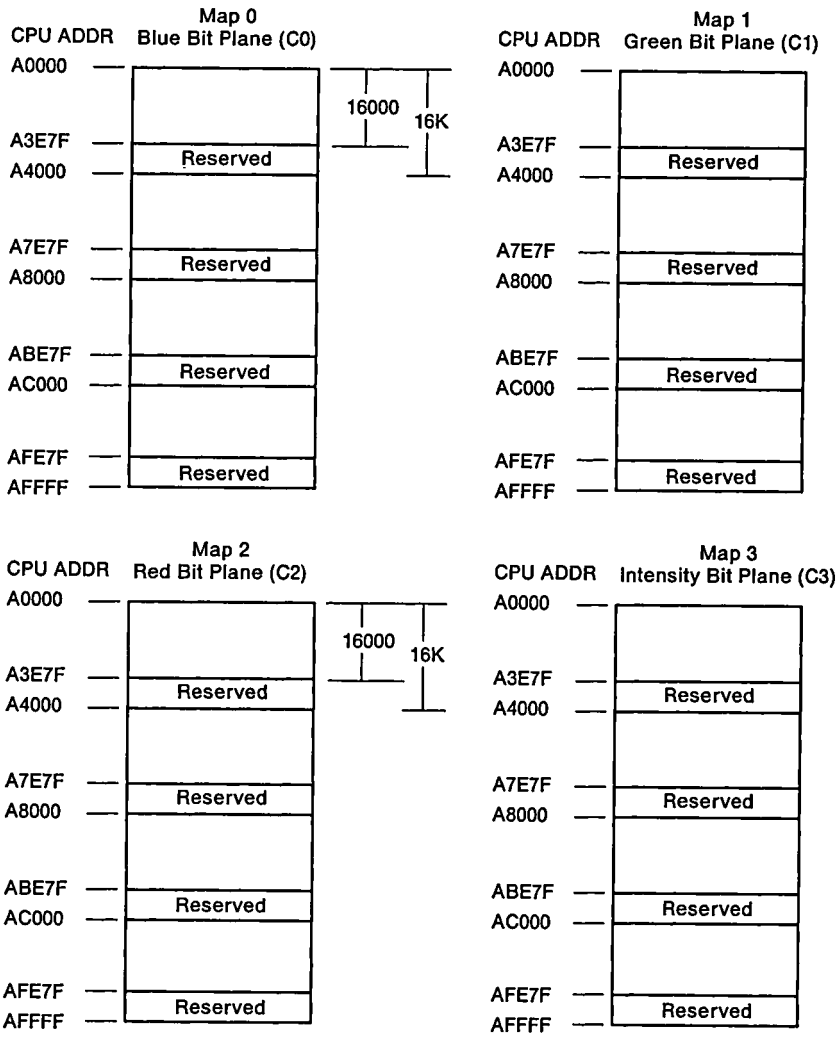
- 4 bits per PEL
- 16 colors per PEL
- 1 bit from each bit plane (C3,C2,C1,CO) per PEL
- Format is first PEL in MSb of all 4 bit planes.


Map 0
CPU ADDR
Blue Bit Plane (C0)
A0000 (A8000)
A1F3F (A9F3F)
A2000 (AA000)
A3F3F (ABF3F)
A4000 (AC000)
A5F3F (ADF3F)
A6000 (AE000)
A7F3F (AFF3F)
A7FFF (AFFFF)
Reserved
8000
8K
Map 1
CPU ADDR
Green Bit Plane (C1)
Map 2
CPU ADDR
Red Bit Plane (C2)
Map 3
CPU ADDR
Intensity Bit Plane (C3)

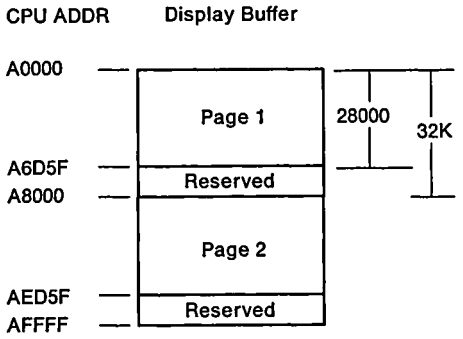
Mode Hex E

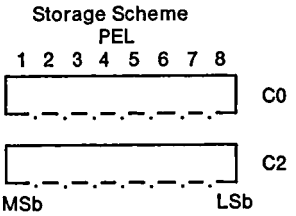


- 4 bits per PEL
- 16 colors per PEL
- 1 bit from each bit plane (C3,C2,C1,C0) per PEL
- Format is first PEL in MSb of all 4 bit planes.

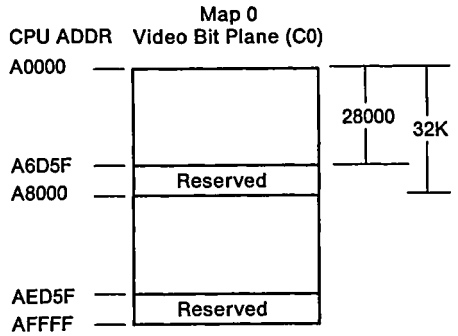

Map 0
CPU ADDR
Blue Bit Plane (C0)
A0000
A3E7F
A4000
A7E7F
A8000
ABE7F
AC000
AFE7F
AFFFF
Reserved
Reserved
Reserved
Reserved
16000
16K
Map 1
CPU ADDR
Green Bit Plane (C1)
A0000
A3E7F
A4000
A7E7F
A8000
ABE7F
AC000
AFE7F
AFFFF
Reserved
Reserved
Reserved
Reserved
Map 2
CPU ADDR
Red Bit Plane (C2)
A0000
A3E7F
A4000
A7E7F
A8000
ABE7F
AC000
AFE7F
AFFFF
Reserved
Reserved
Reserved
Reserved
16000
16K
Map 3
CPU ADDR
Intensity Bit Plane (C3)
A0000
A3E7F
A4000
A7E7F
A8000
ABE7F
AC000
AFE7F
AFFFF
Reserved
Reserved
Reserved
Reserved

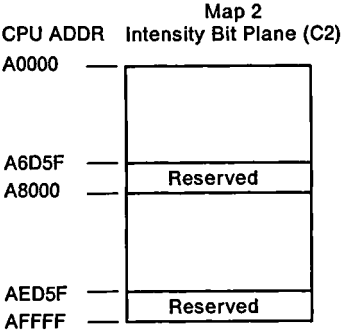
Mode Hex F



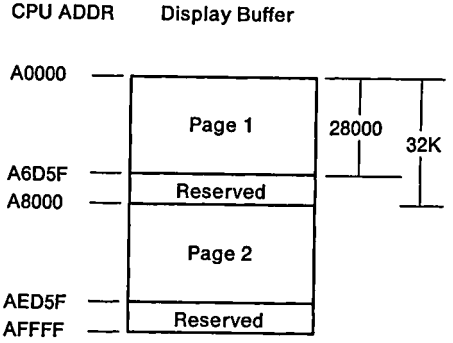


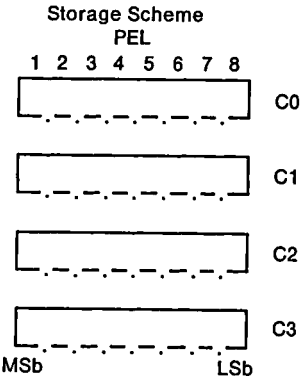
- 2 bits per PEL
- 4 attributes per PEL
- 1 bit from each bit plane (C2,C0)
- Format is first PEL in MSb of video and intensity bit planes.



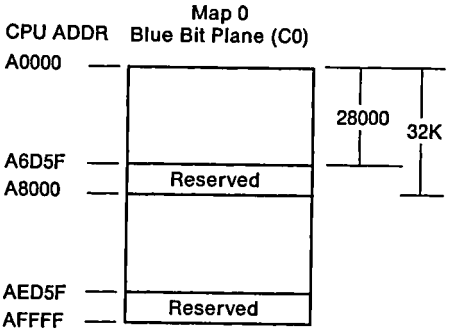


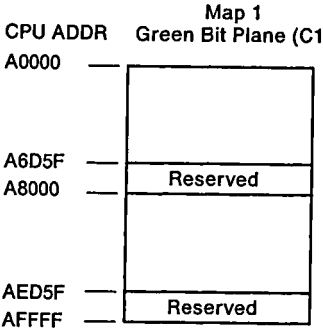
Mode Hex 10

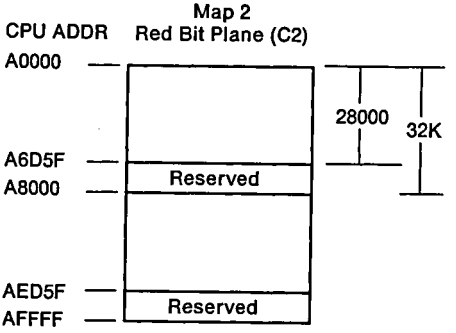


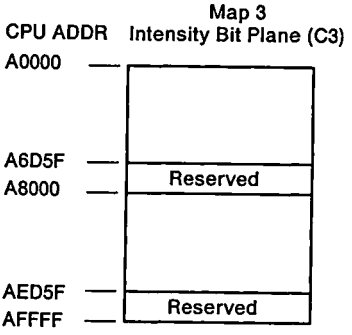


- 4 bits per PEL
- 16 colors per PEL
- 1 bit from each bit plane (C3,C2,C1,C0) per PEL
- Format is first PEL in MSb of all 4 bit planes.

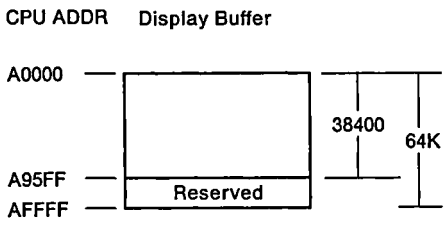




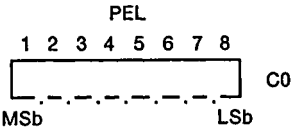




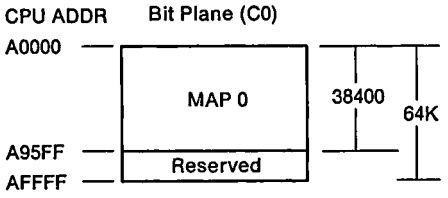
Mode Hex 11



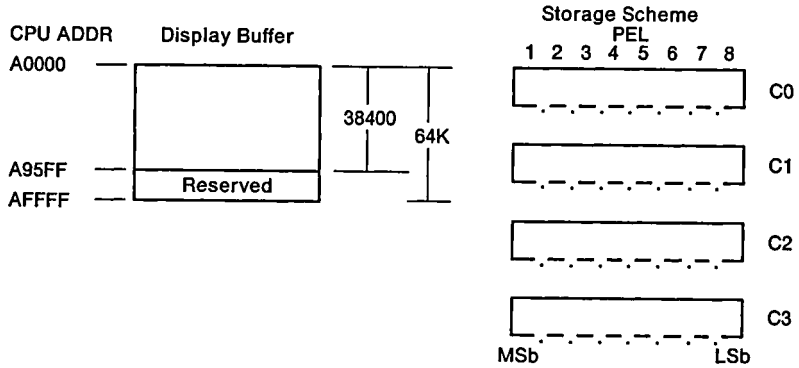
Storage Scheme



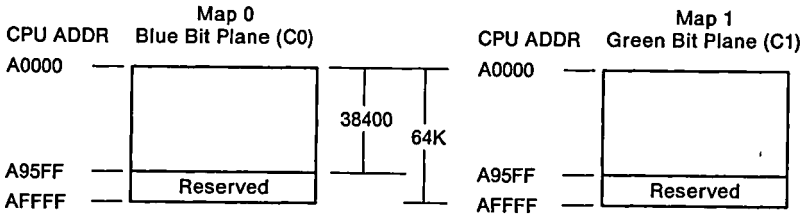
- 1 bit per PEL
- 2 attributes per PEL
- Format is first PEL in MSb position.

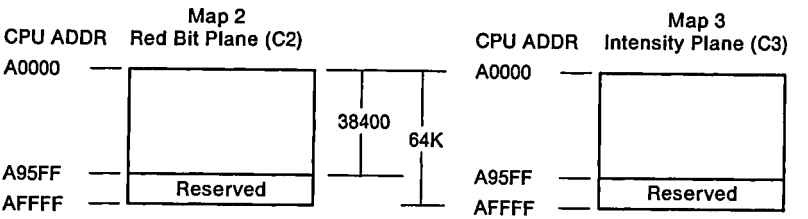


Mode Hex 12

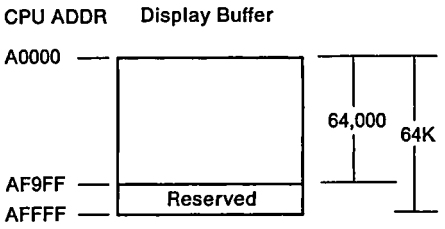


- 4 bits per PEL
- 16 colors per PEL
- 1 bit from each bit plane (C3,C2,C1,C0) per PEL
- Format is first PEL in MSb of all 4 bit planes.

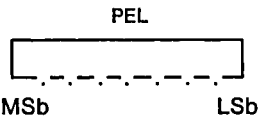




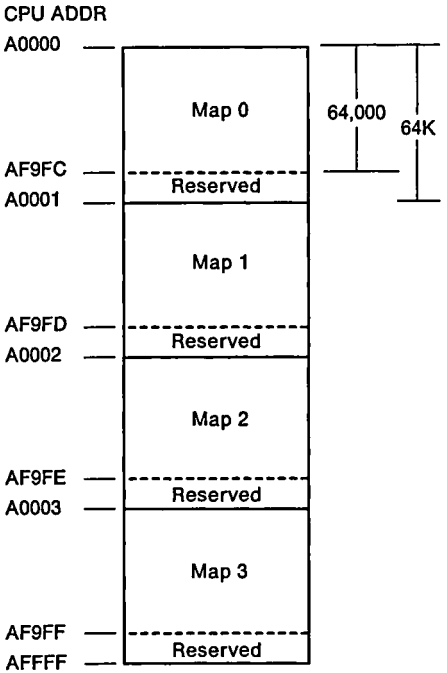
Mode Hex 13



Storage Scheme



- 8 bits per PEL
- 256 colors per PEL
- 1 PEL per byte
- Format is PEL 1 at address A0000.



Video Memory Read/Write Operations

Read Operations

There are two ways to do a video memory read. When read type 0 is selected using the Graphics Mode register, the system microprocessor video memory read returns the 8-bit value that is determined by the logical decode of the memory address, and the Read Map Select register if applicable. When read type 1 is selected using the Graphics Mode register, the 8-bit value returned is the result of the color compare operation controlled by the Color Compare and Color Don't Care registers. Figure 3-28 on page 3-51 shows the data flow for the color compare operations.

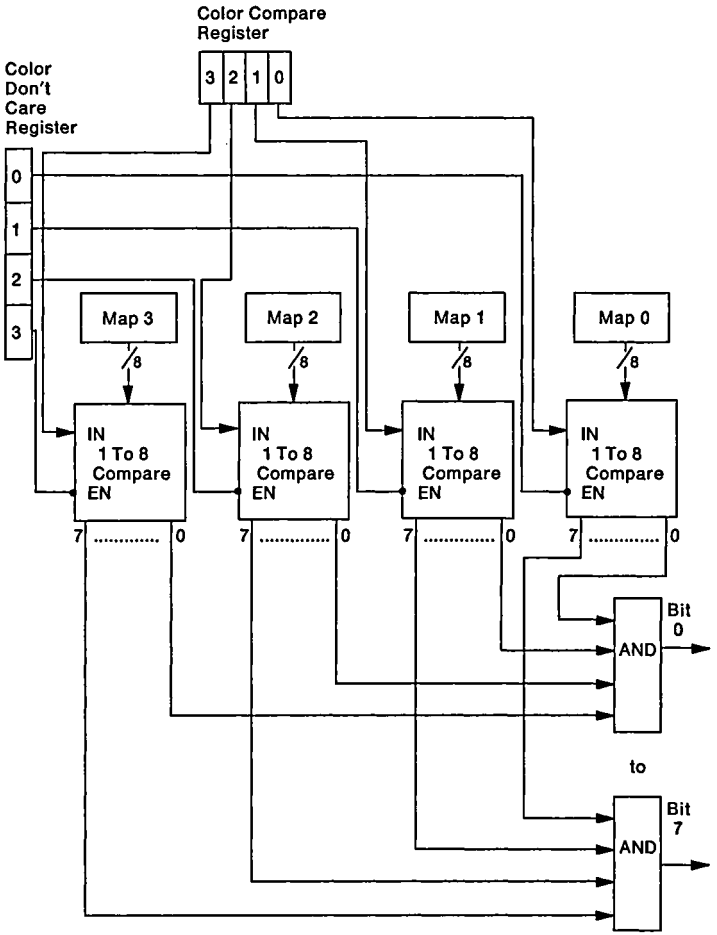


Figure 3-28. VGA Color Compare Operations

Write Operations

During system microprocessor video memory writes, the maps are enabled by the logical decode of the memory address and, depending on the video mode, of the Map Mask register. Figure 3-29 shows the data flow for a system microprocessor write operation.

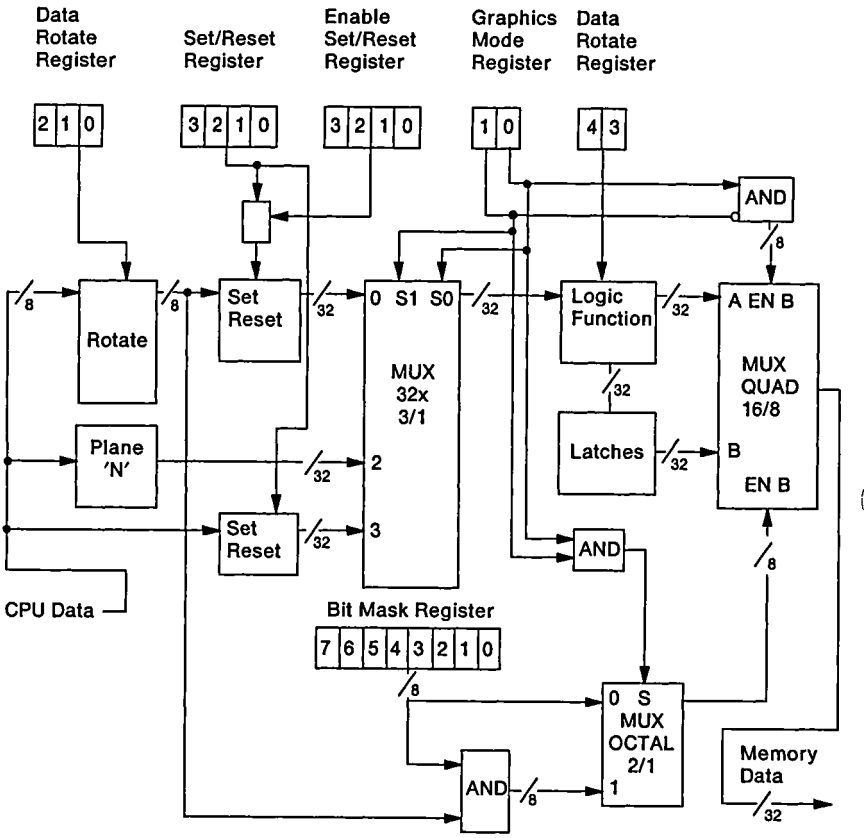


Figure 3-29. Data Flow for VGA Memory Write Operations

Note: Which maps are actually written with data is under control of the system microprocessor video memory address, which depends on the mode selected and the Map Mask register.

Registers

There are six sets of registers in the video subsystem as shown in Figure 3-30.

Figure 3-30. VGA Register Overview

	R/W	Monochrome Emulation	Color Emulation	Either
General Registers Addresses used 03BA or 03DA; 03C2; 03CA; and 03CC				
Miscellaneous Output Reg	W			03C2
	R			03CC
Input Status Register 0	RO			03C2
Input Status Register 1	RO	03BA	03DA	
Feature Control Register	W	03BA	03DA	
	R			03CA
VGA Enable Register	RW			03C3
Attribute Mode Control Registers Addresses used 03C0 - 03C1				
Address Register	RW			03C0
Other Attribute Registers	W			03C0
	R			03C1
CRT Controller Registers Addresses used 03D4 to 03D5 or 03B4 to 03B5				
Index Register	RW	03B4	03D4	
Other CRT Controller Regs.	RW	03B5	03D5	
Sequencer Registers Addresses used 03C4 to 03C5				
Address Register	RW			03C4
Other Sequencer Registers	RW			03C5
Graphics Controller Registers Addresses used 03CE to 03CF				
Address Register	RW			03CE
Other Graphics Registers	RW			03CF
Video DAC Registers Addresses used 03C6 to 03C9				
PEL Address Register	RW (Write Mode)			03C8
	WO (Read Mode)			03C7
DAC State Register	RO			03C7
PEL Data Register	RW			03C9
PEL Mask Register	RW			03C6

RO = Read-Only, RW = Read / Write, WO = Write-Only
Register addresses are in hex.

General Registers

This section contains descriptions of the following registers.

Figure 3-31. General Register Overview

Name	Read Port	Write Port	Index
Miscellaneous Output Register	03CC	03C2	-
Input Status Register 0	03C2	-	-
Input Status Register 1	03?A	-	-
Feature Control Register	03CA	03?A	-
VGA Enable Register	03C3	03C3	-

The (?) is controlled by bit 0 of the Miscellaneous Output register.

? = B in Monochrome Emulation Modes and

? = D in Color Emulation Modes

Register addresses are in hex.

Miscellaneous Output Register

This is a read/write register. A hardware reset causes all bits to be reset to 0. Read address = hex 03CC; write address = hex 03C2.

Figure 3-32. Miscellaneous Output Register

Bit	Function
7	Vertical Sync Polarity
6	Horizontal Sync Polarity
5	Page Bit For Odd/Even (Modes 0-5)
4	Reserved = 0
3	Clock Select 1
2	Clock Select 0
1	Enable RAM
0	I/O Address Select

Bit 7 When bit 7 is set to 1, negative vertical retrace is selected. When bit 7 is set to 0, positive vertical retrace is selected.

Bit 6 When bit 6 is set to 1, negative horizontal retrace is selected. When bit 6 is set to 0, positive horizontal retrace is selected.

Note: Bits 7 and 6 are selected based on the vertical size as shown in Figure 3-33.

Figure 3-33. Display, Vertical Size

Bit 7	Bit 6	Vertical Size
0	0	Reserved = 0
1	0	400 lines
0	1	350 lines
1	1	480 lines

Bit 5 Bit 5 selects between two 64K pages of memory when in the Odd/Even modes (0-5). When bit 5 is set to 1, the high page of memory is selected. When bit 5 is set to 0, the low page of memory is selected. This bit is provided for diagnostic use.

Bit 4 Reserved

Bits 3, 2 Bits 3 and 2 select the clock source according to Figure 3-34.

Figure 3-34. Clock Select 3 and 2 Bit Definitions

Bit 3	Bit 2	Function
0	0	Selects 25.175 MHz clock for 640 horizontal PELs
0	1	Selects 28.322 MHz clock for 720 horizontal PELs
1	0	Reserved
1	1	Reserved

Bit 1 When bit 1 is set to 1, Video RAM to the system microprocessor is enabled. When bit 1 is set to 0, Video RAM address decode from the system microprocessor is disabled.

Bit 0 This bit maps the CRT controller I/O addresses for IBM Monochrome or Color/Graphics Monitor Adapter emulation. When bit 0 is set to 1, the CRT controller address is set to hex 03DX and Input Status register 1 address is set to hex 03DA for IBM Color/Graphics Monitor Adapter emulation. When bit 0 is set to 0, the CRT controller address is set to hex 03BX and and Input Status register 1 address is set to hex 03BA for IBM Monochrome Adapter emulation.

Input Status Register 0

This is a read-only register. Read address = hex 03C2.

Figure 3-35. Input Status Register 0

Bit	Function
7	CRT Interrupt
6, 5	Reserved = 0
4	Switch Sense Bit
3 - 0	Reserved = 0

Bit 7 When bit 7 is set to 1, a vertical retrace interrupt is pending. When bit 7 is set to 0, the vertical retrace interrupt is cleared.

Bits 6, 5 Reserved

Bit 4 Bit 4 allows the system microprocessor to read the switch sense line and allows the power-on self-test to determine if a monochrome or color display is connected to the system.

Bits 3 - 0 Reserved

Input Status Register 1

This is a read-only register. Read address = hex 03?A.

Figure 3-36. Input Status Register 1

Bit	Function
7, 6	Reserved = 0
5	Diagnostic 0
4	Diagnostic 1
3	Vertical Retrace
2, 1	Reserved = 0
0	Display Enable

Bits 7, 6 Reserved.

Bits 5, 4 Diagnostic Usage - Bits 5 and 4 are selectively connected to two of the eight color outputs of the attribute controller. The Color Plane Enable register controls the multiplexer for the video wiring. Figure 3-37 shows the combinations available and the color output wiring.

Figure 3-37. Diagnostic Bits

Color Plane Enable Register		Input Status Register 1	
Bit 5	**Bit 4**	**Bit 5**	**Bit 4**
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

Bit 3 Vertical Retrace - When bit 3 is set to 1, a vertical retrace interval is occurring. When bit 3 is set to 0, video information is being displayed. Bit 3 can be programmed, through bits 5 and 4 of the Vertical Retrace End register, to interrupt the system microprocessor on interrupt level 2 at the start of the vertical retrace.

Bit 2, 1 Reserved.

Bit 0 Display Enable - When bit 0 is set to 1, a horizontal or vertical retrace interval is occurring. This bit is the real-time status of the inverted display enable signal. To avoid glitches on the display, some programs use this status bit to restrict screen updates to inactive display intervals. The video subsystem has been designed to eliminate this software requirement, so display screen updates may be made at any time.

Feature Control Register

This is a read/write register. Read address = hex 03CA; write address = hex 03?A.

All bits in this register are reserved and bit 3 must be 0.

VGA Enable Register

Figure 3-38. VGA Enable Register, Hex 03C3

Bit	Function
7 - 1	Reserved = 0
0	VGA Enable

Bits 7 - 1 Reserved

Bit 0 When bit 0 is set to 1, the video I/O and memory address decoding is enabled. When bit 0 is set to 0, the video I/O and memory address decoding is disabled.

Note: Accesses to the Video Subsystem Enable register are not affected by the VGA sleep bit (I/O port 102, bit 0), described in "Video Subsystem Programmable Option Select" on page 3-24.

Sequencer Registers

This section contains descriptions of the following registers.

Figure 3-39. Sequencer Register Overview

Name	Port (hex)	Index (hex)
Sequencer Address	03C4	-
Reset	03C5	00
Clocking Mode	03C5	01
Map Mask	03C5	02
Character Map Select	03C5	03
Memory Mode	03C5	04

Sequencer Address Register

The Sequencer Address register is a pointer register located at address hex 03C4. This register is loaded with a binary value that points to the Sequencer Data register where data is to be written. This value is referred to as *Index* in Figure 3-39.

Figure 3-40. Sequencer Address Register

Bit	Function
7 - 3	Reserved = 0
2 - 0	Sequencer Address Bits

Bits 7 - 3 Reserved

Bits 2 - 0 Bits 2 through 0 contain the binary value pointing to the register where data is to be written.

Reset Register

This is a read/write register pointed to when the value in the Sequencer Address register is hex 00. The port address for this register is hex 03C5.

Figure 3-41. Reset Register, Index Hex 00

Bit	Function
7 - 2	Reserved = 0
1	Synchronous Reset
0	Asynchronous Reset

Bits 7 - 2 Reserved.

Bit 1 Synchronous Reset - When bits 0 and 1 are both 1, the sequencer operates. When bit 1 is set to 0, the sequencer is synchronously cleared and stopped. Bit 1 must be set to 0 before changing either bit 3 or bit 0 of the Clocking Mode register (index 01), or bits 2 or 3 of the Miscellaneous Output register (hex 03C2).

Bit 0 Asynchronous Reset - When bits 0 and 1 are both 1, the sequencer operates. When bit 0 is set to 0, the sequencer is asynchronously cleared and stopped. Resetting the sequencer with this bit can cause data loss in the dynamic RAMs.

Clocking Mode Register

This is a read/write register pointed to when the value in the Sequencer Address register is hex 01. The port address for this register is hex 03C5.

Figure 3-42. Clocking Mode Register, Index Hex 01

Bit	Function
7, 6	Reserved = 0
5	Screen Off
4	Shift 4
3	Dot Clock
2	Shift Load
1	Reserved = 0
0	8/9 Dot Clocks

Bits 7, 6 Reserved.

Bit 5 Screen Off - When bit 5 is set to 1, the video screen is turned off and maximum memory bandwidth is assigned to the system microprocessor. When bit 5 is set to 0, normal screen operation is selected. The screen is blanked when this bit is set, and the sync pulses are maintained. Use this bit for rapid full-screen updates.

Bit 4 Shift 4 - When bit 4 is set to 1, the serializers are loaded every fourth character clock. This mode is useful when 32 bits are fetched per cycle and chained together in the shift registers. When bit 4 is set to 0, the video serializers are loaded every character clock.

Bit 3 Dot Clock - When bit 3 is set to 1, the master clock is divided by 2 to generate the dot clock. Dot clock divided by 2 is used for 320- and 360-horizontal-PEL modes. When bit 3 is set to 0, the dot clock is derived from the sequencer master clock input (normal). All the other timings are affected because they are derived from the dot clock.

Bit 2 Shift Load - When bit 2 is set to 1, the video serializers are reloaded every other character clock. This mode is useful when 16 bits are fetched per cycle and chained together in the shift registers. When bit 2 is set to 0, and bit 4 is set to 0, the video serializers are reloaded every character clock.

Bit 1 Reserved.

Bit 0 8/9 Dot Clocks - When bit 0 is set to 1, the sequencer generates character clocks 8 dots wide. When bit 0 is set to 0, the sequencer generates character clocks 9 dots wide. Alphanumeric modes hex 0+, 1+, 2+, 3+, 7 and 7+ are the only modes that use character clocks 9 dots wide. All other modes must use 8 dots per character clock. The 9-dot mode is for alphanumeric modes only. The ninth dot equals the eighth dot for ASCII codes hex C0 through DF. (See the enable line graphics character codes bit in "Attribute Mode Control Register" on page 3-89.)

Map Mask Register

This is a read/write register pointed to when the value in the Sequencer Address register is hex 02. The port address for this register is hex 03C5.

Figure 3-43. Map Mask Register, Index Hex 02

Bit	Function
7 - 4	Reserved = 0
3	Map 3 Enable
2	Map 2 Enable
1	Map 1 Enable
0	Map 0 Enable

A logical 1 in any of bits 3 through 0 enables the system microprocessor to write to the corresponding map. If this register is programmed with a value of 0FH, the system microprocessor can perform a 32-bit write operation with only one memory cycle. This substantially reduces the overhead on the system microprocessor during display update cycles in graphics modes. Data scrolling operations are also enhanced by setting this register to a value of 0FH and writing the display buffer address with the data stored in the system microprocessor data latches. This is a read-modify-write operation. When odd/even modes are selected, maps 0 and 1 and maps 2 and 3 should have the same map mask value. When chain 4 mode is selected, all maps should be enabled.

Character Map Select Register

This is a read/write register pointed to when the value in the Sequencer Address register is hex 03. The port address for this register is hex 03C5.

Figure 3-44. Character Map Select Register, Index Hex 03

Bit	Function
7, 6	Reserved = 0
5	Character Map Select High Bit A
4	Character Map Select High Bit B
3, 2	Character Map Select A
1, 0	Character Map Select B

Bits 3 and 2 select the portion of map 2 used to generate alphanumeric characters when attribute bit 3 is 1, according to Figure 3-45.

Figure 3-45. Character Map Select A

Bit 5 Value	Bit 3 Value	Bit 2 Value	Map Selected	Table Location
0	0	0	0	1st 8KB of Map 2
0	0	1	1	3rd 8KB of Map 2
0	1	0	2	5th 8KB of Map 2
0	1	1	3	7th 8KB of Map 2
1	0	0	4	2nd 8KB of Map 2
1	0	1	5	4th 8KB of Map 2
1	1	0	6	6th 8KB of Map 2
1	1	1	7	8th 8KB of Map 2

In alphanumeric modes, bit 3 of the attribute byte normally has the function of turning the foreground intensity on or off. This bit can be

redefined as a switch between character sets. For this feature to be enabled, the following must be true:

- Memory Mode register (index 04) bit 1 must be equal to 1
- The value of Character Map Select A does not equal the value of Character Map Select B.

If either condition is not met, the first 16KB of map 2 is used.

Bits 1 and 0 select the portion of map 2 used to generate alpha characters when attribute bit 3 is 0, according to Figure 3-46.

Figure 3-46. Character Map Select B

Bit 4 Value	Bit 1 Value	Bit 0 Value	Map Selected	Table Location
0	0	0	0	1st 8KB of Map 2
0	0	1	1	3rd 8KB of Map 2
0	1	0	2	5th 8KB of Map 2
0	1	1	3	7th 8KB of Map 2
1	0	0	4	2nd 8KB of Map 2
1	0	1	5	4th 8KB of Map 2
1	1	0	6	6th 8KB of Map 2
1	1	1	7	8th 8KB of Map 2

Memory Mode Register

This is a read/write register pointed to when the value in the Sequence Address register is hex 04. The output port address for this register is 03C5.

Figure 3-47. Memory Mode Register, Index Hex 04

Bit	Function
7 - 4	Reserved = 0
3	Chain 4
2	Odd/Even
1	Extended Memory
0	Reserved = 0

Bits 7 - 4 Reserved.

Bit 3 Chain 4 - When bit 3 is set to 1, the 2 low-order bits select the map that will be accessed as shown in Figure 3-48 on page 3-63. When bit 3 is set to 0, the system microprocessor sequentially addresses access data within a bit map using the Map Mask register.

Note: This bit controls the map selected in the graphics subsection during system microprocessor reads.

Figure 3-48. Memory Mode, Chain 4

A1	A0	Map Selected
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2 Odd/Even - When bit 2 is set to 1, the system microprocessor sequentially accesses data within a bit map. When bit 2 is set to 0, even addresses access maps 0 and 2 and odd addresses access maps 1 and 3. The maps are accessed according to the value in the Map Mask register (index 02).

Bit 1 Extended Memory - When bit 1 is set to 1, more than 64KB of video memory is present. This bit must be set to allow the VGA to use the 256KB of video memory on the system board, and to enable the character map selection on the previous page.

Bit 0 Reserved.

CRT Controller Registers

This section contains descriptions of the following registers:

Figure 3-49. CRT Controller Register Overview

Name	Port (hex)	Index (hex)
CRT Controller Address	03?4	-
Horizontal Total	03?5	00
Horizontal Display Enable End	03?5	01
Start Horizontal Blanking	03?5	02
End Horizontal Blanking	03?5	03
Start Horizontal Retrace Pulse	03?5	04
End Horizontal Retrace	03?5	05
Vertical Total	03?5	06
Overflow	03?5	07
Preset Row Scan	03?5	08
Maximum Scan Line	03?5	09
Cursor Start	03?5	0A
Cursor End	03?5	0B
Start Address High	03?5	0C
Start Address Low	03?5	0D
Cursor Location High	03?5	0E
Cursor Location Low	03?5	0F
Vertical Retrace Start	03?5	10
Vertical Retrace End	03?5	11
Vertical Display Enable End	03?5	12
Offset	03?5	13
Underline Location	03?5	14
Start Vertical Blank	03?5	15
End Vertical Blank	03?5	16
CRTC Mode Control	03?5	17
Line Compare	03?5	18

? = B in Monochrome Emulation Modes
? = D in Color Emulation Modes.
This is controlled by bit 0 of the Miscellaneous Output register.

CRT Controller Address Register

The CRT Controller Address register is a pointer register located at hex 03B4 or hex 03D4. Which address is used depends on bit 0 of the Miscellaneous Output register at address hex 03C2. The CRT Controller Address register is loaded with a binary value that points to the CRT Controller Data register where data is to be written. This value is referred to as *Index* in Figure 3-49 on page 3-64. All CRT controller registers are read/write registers.

Figure 3-50. CRT Controller Address Register

Bit	Function
7	Reserved = 0
6	Reserved = 0
5	Reserved = 0
4	CRTC Index
3	CRTC Index
2	CRTC Index
1	CRTC Index
0	CRTC Index

Bits 7, 6 Reserved.

Bit 5 Bit 5 is used for chip testing and must be 0.

Bits 4 - 0 Bits 4 through 0 contain the index value of the CRT Controller Data register where data is to be written.

Horizontal Total Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 00. The port address for this register is hex 03?5.

This register defines the total number of characters (minus 5) in the horizontal scan interval including the retrace time. The value directly controls the period of the horizontal retrace output signal. An internal horizontal character counter counts character clock inputs to the CRT controller, and all horizontal and vertical timings are based upon the Horizontal Total register. Comparators are used to compare register values with horizontal character values to provide horizontal timings.

Horizontal Display Enable End Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 01. The port address for this register is hex 03?5.

This register defines the length of the horizontal display enable signal. It determines the number of displayed character positions per horizontal line. The value in this register is the total number of displayed characters less 1.

Start Horizontal Blanking Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 02. The port address for this register is hex 03?5.

The horizontal blanking signal becomes active when the horizontal character counter reaches the value in this register.

End Horizontal Blanking Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 03. The port address for this register is hex 03?5.

Figure 3-51. End Horizontal Blanking Register, Index Hex 03

Bit	Function
7	Reserved = 1
6	Display Enable Skew Control
5	Display Enable Skew Control
4 - 0	End Horizontal Blanking

This register determines when the horizontal blanking output signal becomes inactive.

Bit 7 Bit 7 is used for chip testing and must be set to 1.

Bits 6, 5 Display Enable Skew Control - Bits 6 and 5 determine the amount of display enable skew. Display enable skew control is required to provide sufficient time for the CRT controller to access the display buffer to obtain a character and attribute code, access the character generator font, and then go through the Horizontal PEL Panning register in the attribute controller. Each access requires the display enable signal to be skewed one character clock unit so that the video output is in

synchronization with the horizontal retrace and vertical retrace signals. The bit values and amount of skew are shown in Figure 3-52 on page 3-67.

Figure 3-52. Bit Values and Amount of Skew

Bit 6	Bit 5	Skew
0	0	Zero-character Clock Skew
0	1	One-character Clock Skew
1	0	Two-character Clock Skew
1	1	Three-character Clock Skew

Bits 4 - 0 End Horizontal Blanking - A value equal to the 5 least-significant bits of the horizontal character counter value at which time the horizontal blanking signal becomes inactive (logical 0). To obtain a blanking signal of width W, the following algorithm is used: Value of Start Blanking register + width of blanking signal in character clock units = 6-bit result to be programmed into the End Horizontal Blanking register. Bit 5 is located in the End Horizontal Retrace register (index hex 05).

Start Horizontal Retrace Pulse Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 04. The port address for this register is hex 03?5.

This register is used to center the screen horizontally, and to specify the character position at which the horizontal retrace signal becomes active. The value programmed is a binary count of the character position at which the signal becomes active.

End Horizontal Retrace Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 05. The port address for this register is hex 03?5.

Figure 3-53. End Horizontal Retrace Register, Index Hex 05

Bit	Function
7	End Horizontal Blanking, Bit 5
6, 5	Horizontal Retrace Delay
4 - 0	End Horizontal Retrace

This register specifies the character position at which the horizontal retrace pulse becomes inactive (logical 0).

Bit 7 End Horizontal Blanking, MSB - The first 5 bits are located in the End Horizontal Blanking register (index hex 03).

Bits 6, 5 Bits 6 and 5 control the skew of the horizontal retrace signal. Binary 00 equals no horizontal retrace delay. For some modes, it is necessary to provide a horizontal retrace signal that takes up the entire blanking interval. Some internal timings are generated by the falling edge of the horizontal retrace signal. To guarantee the signals are latched properly, the retrace signal is started before the end of the display enable signal, and then skewed several character clock times to provide proper screen centering.

Bits 4 - 0 A value equal to the 5 least-significant bits of the horizontal character counter value at which the horizontal retrace signal becomes inactive (logical 0). To obtain a retrace signal of width W, the following algorithm is used: Value of Start Retrace register + width of the horizontal retrace signal in character clock units = 5-bit result to be programmed into the End Horizontal Retrace register.

Vertical Total Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 06. The port address for this register is hex 03?5.

This register contains the low-order 8 bits of a 10-bit register. The binary value represents the number of horizontal raster scans on the CRT minus 2, including vertical retrace. The value in this register determines the period of the vertical retrace signal.

Bit 8 of this register is contained in the CRT Controller Overflow register, index hex 07 bit 0.

Bit 9 of this register is contained in the CRT Controller Overflow register, index hex 07 bit 5.

CRT Controller Overflow Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 07. The port address for this register is hex 03?5.

Figure 3-54. CRT Controller Overflow Register, Index Hex 07

Bit	Function
7	Bit 9 of the Vertical Retrace Start (Index hex 10)
6	Bit 9 of the Vertical Display Enable End (Index hex 12)
5	Bit 9 of the Vertical Total (Index hex 6)
4	Bit 8 of the Line Compare (Index hex 18)
3	Bit 8 of the Start Vertical Blanking (Index hex 15)
2	Bit 8 of the Vertical Retrace Start (Index hex 10)
1	Bit 8 of the Vertical Display Enable End (Index hex 12)
0	Bit 8 of the Vertical Total (Index hex 6)

Preset Row Scan Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 08. The port address for this register is hex 03?5.

Figure 3-55. Preset Row Scan Register, Index Hex 08

Bit	Function
7	Reserved = 0
6	Byte Panning Control
5	Byte Panning Control
4 - 0	Starting Row Scan Count after a Vertical Retrace

This register is used for PEL scrolling.

Bit 7 Reserved.

Bits 6, 5 Bits 6 and 5 control byte panning in modes programmed as multiple shift modes. (Currently, no modes are programmed for multiple shift operation.) This is required for PEL panning operations. The PEL Panning register in the attribute section provides panning of up to 7 or 8 individual PELs. In single-byte shift modes, to pan to the next higher PEL (8 or 9), the CRT controller start address is incremented and attribute panning is reset to 0. In multiple shift modes, the byte pan bits are used as extensions to the attribute PEL Panning register. This allows panning across the width of the video output shift. For example, in the 32-bit shift mode, the byte pan and PEL panning bits provide up to 31 bits of panning capability. To pan from position 31 to 32, the CRT controller start address is incremented and PEL and byte panning is reset to 0. These bits should normally be set to 0.

Bits 4 - 0 Bits 4 through 0 specify the starting row scan count after a vertical retrace. The row scan counter increments each horizontal retrace time until a maximum row scan occurs. At maximum row scan compare time, the row scan is cleared (not preset).

Maximum Scan Line Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 09. The port address for this register is hex 03?5.

Figure 3-56. Maximum Scan Line Register, Index Hex 09

Bit	Function
7	200 --> 400 Line Conversion
6	Bit 9 of the Line Compare (Index hex 18)
5	Bit 9 of the Start Vertical Blanking (Index hex 15)
4 - 0	Maximum Scan Line

Bit 7 When bit 7 is set to 1, 200 to 400 line conversion is performed. The clock in the row scan counter is divided by 2. This allows the older 200-line modes to be displayed as 400 lines on the display (this is double scanning, in which each line is displayed twice). When bit 7 is set to 0, the clock to the row scan counter is equal to the horizontal scan rate. Double scan is not enabled.

Bit 6 Bit 9 of the Line Compare register (index hex 18).

Bit 5 Bit 9 of the Start Vertical Blank register (index hex 15).

Bits 4 - 0 Bits 4 through 0 specify the number of scan lines per character row. The number programmed is the maximum row scan number minus 1.

Cursor Start Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 0A. The port address for this register is hex 03?5.

Figure 3-57. Cursor Start Register, Index Hex 0A

Bit	Function
7, 6	Reserved = 0
5	Cursor Off
4 - 0	Row Scan Cursor begins

Bits 7, 6 Reserved.

Bit 5 When bit 5 is set to 1, the cursor is turned off. When bit 5 is set to 0, the cursor is turned on.

Bits 4 - 0 Bits 4 through 0 specify the row scan of a character line where the cursor is to begin. The number programmed is the starting cursor row scan minus 1.

When the Cursor Start register is programmed with a value greater than the Cursor End register, no cursor is generated.

Cursor End Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 0B. The port address for this register is hex 03?5.

Figure 3-58. Cursor End Register, Index Hex 0B

Bit	Function
7	Reserved = 0
6, 5	Cursor Skew Control
4 - 0	Row Scan Cursor ends

Bit 7 Reserved.

Bits 6, 5 Bits 6 and 5 control the skew of the cursor signal. Cursor skew delays the cursor by the selected number of clocks. For example, a skew of 1 moves the cursor right one position on the screen.

Figure 3-59. Cursor Skew

Bit 6	Bit 5	Function
0	0	Zero-character Clock Skew
0	1	One-character Clock Skew
1	0	Two-character Clock Skew
1	1	Three-character Clock Skew

Bits 4 - 0 Cursor End - Bits 4 through 0 specify the row scan of a character line where the cursor is to end.

Start Address High Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 0C. The port address for this register is hex 03?5.

This register contains the most-significant 8 bits of the start address. The 16-bit value, from the Start Address High and Low registers, is the first address after the vertical retrace on each screen refresh.

Start Address Low Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 0D. The port address for this register is hex 03?5.

This register contains the least-significant 8 bits of the start address.

Cursor Location High Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 0E. The port address for this register is hex 03?5.

This register contains the most-significant 8 bits of the cursor location.

Cursor Location Low Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 0F. The port address for this register is hex 03?5.

This register contains the least-significant 8 bits of the cursor location.

Vertical Retrace Start Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 10. The port address for this register is hex 03?5.

This register contains the least-significant 8 bits of the vertical retrace signal start position, programmed in horizontal scan lines. Bits 8 and 9 are in the CRT Controller Overflow register (index hex 07).

Vertical Retrace End Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 11. The port address for this register is hex 03?5.

Figure 3-60. Vertical Retrace End Register, Index Hex 11

Bit	Function
7	Protect R0-7
6	Select 5 Refresh Cycles
5	Enable Vertical Interrupt=0
4	Clear Vertical Interrupt=0
3 - 0	Vertical Retrace End

Bit 7 When bit 7 is set to 1, writing to CRT controller registers 0 through 7 is disabled. When bit 7 is set to 0, writing to CRT controller registers is enabled. Bit 4 in CRT Controller Overflow register, index hex 07, is not protected.

Bit 6 When bit 6 is set to 1, five DRAM refresh cycles are generated per horizontal line. Selecting five refresh cycles allows use of the VGA chip with slow sweep rate displays (15.75 KHz). When bit 6 is set to 0, three refresh cycles are selected. This bit is set to 0 by BIOS during a mode set, a reset, or power-on.

Bit 5 When bit 5 is set to 0, a vertical retrace interrupt is enabled. The vertical retrace interrupt is on IRQ2. This interrupt level can be shared so the Input Status register 0, bit 7, should be checked to find out if the VGA generated the interrupt. As with bit 4, do not change the value of the other bits in this register.

Bit 4 When bit 4 is set to 0, vertical retrace interrupt is cleared. At the end of the active vertical display time, a flip-flop is set in the VGA for vertical interrupt. The output of this flip-flop goes to the system board interrupt controller. An interrupt handler has to reset this flip-flop by writing a 0 to this bit, then setting the bit to 1 so that the flip-flop does not hold interrupts inactive. *Do not change* the other bits in this register. The register is readable, so a read can be done to determine what the other bit settings are before the flip-flop is reset.

Bits 3 - 0 Bits 3 through 0 determine the horizontal scan count value when the vertical retrace signal becomes inactive. The register is programmed in units of horizontal scan lines. To obtain a vertical retrace signal of width W, the following algorithm is used: Value of Start Vertical Retrace register + width of the vertical retrace signal in horizontal scan units = 4-bit result to be programmed into the End Horizontal Retrace register.

Vertical Display Enable End Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 12. The port address for this register is hex 03?5.

This register contains the least-significant 8 bits of a 10-bit value that defines the vertical display enable end position.

Bit 8 of this value is contained in the CRT Controller Overflow register, index hex 07, bit 1.

Bit 9 of this value is contained in the CRT Controller Overflow register, index hex 07, bit 6.

This value specifies which scan line ends the active video area of the screen. It is programmed with the total number of lines minus 1.

Offset Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 13. The port address for this register is hex 03?5.

This register specifies the logical line width of the screen. The starting memory address for the next character row is larger than the current character row by two or four times this amount. The Offset register is programmed with a word address. Depending on the method of clocking the CRT controller, this word address is either a word or doubleword address.

Underline Location Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 14. The port address for this register is hex 03?5.

Figure 3-61. Underline Location Register, Index Hex 14

Bit	Function
7	Reserved = 0
6	Doubleword Mode
5	Count by 4
4 - 0	Horizontal Row Scan where Underline will occur

Bit 7 Reserved.

Bit 6 When bit 6 is set to 1, memory addresses are doubleword addresses. (See "CRTC Mode Control Register" on page 3-76.)

Bit 5 When bit 5 is 1, the memory address counter is clocked with the character clock divided by 4. This bit is used when doubleword addresses are used.

Bits 4 - 0 Bits 4 through 0 specify the horizontal row scan of a character row on which an underline occurs. The value programmed is the scan line number desired minus 1.

Start Vertical Blanking Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 15. The port address for this register is hex 03?5.

This register contains the least-significant bits of a 10-bit value. Bit 8 is in the CRTC Overflow register (index hex 07). Bit 9 is in the Maximum Scan Line register (index hex 09).

The value in these 10 bits is one less than the horizontal scan line count at which the vertical blanking signal becomes active.

End Vertical Blanking Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 16. The port address for this register is hex 03?5.

This register specifies the horizontal scan count value when the vertical blanking signal becomes inactive. The register is programmed in units of horizontal scan lines.

To obtain a vertical blanking signal of width W, the following algorithm is used: (Value of Start Vertical Blanking register minus 1) + width of the vertical blanking signal in horizontal scan units = 8-bit result to be programmed into the End Vertical Blanking register.

CRTC Mode Control Register

This is a read/write register pointed to when the value in the CRTC Address register is hex 17. The port address for this register is hex 03?5.

Figure 3-62. CRTC Mode Control Register, Index Hex 17

Bit	Function
7	Hardware Reset
6	Word/Byte Mode
5	Address Wrap
4	Reserved = 0
3	Count By 2
2	Horizontal Retrace Select
1	Select Row Scan Counter
0	Compatibility Mode Support 0

Bit 7 When bit 7 is set to 1, horizontal and vertical retrace are enabled. When bit 7 is set to 0, horizontal and vertical retrace are cleared. This bit does not reset any other registers or outputs.

Bit 6 When bit 6 is set to 1, Byte Address mode is selected. When bit 6 is set to 0, the Word Address mode shifts all memory address counter bits down 1 bit, and the most-significant bit of the counter appears on the least-significant bit of the memory address outputs.

Bit 6 of the End Vertical Blanking register in the CRT controller also controls the addressing. When it is 0, bit 6 above has control. When it is 1, the addressing is shifted by 2 bits. (See Figure 3-63.)

Figure 3-63. Internal Memory Address Counter Wiring to the Output Multiplexer

Memory Address	Byte Address Mode	Word Address Mode	Doubleword Address Mode
MA 0/RFA 0	MA 0	MA 15 or MA 13	MA 12
MA 1/RFA 1	MA 1	MA 0	MA 13
MA 2/RFA 2	MA 2	MA 1	MA 0
MA 3/RFA 3	MA 3	MA 2	MA 1
MA 4/RFA 4	MA 4	MA 3	MA 2
MA 5/RFA 5	MA 5	MA 4	MA 3
MA 6/RFA 6	MA 6	MA 5	MA 4
MA 7/RFA 7	MA 7	MA 6	MA 5
MA 8/RFA 8	MA 8	MA 7	MA 6
MA 9	MA 9	MA 8	MA 7
MA 10	MA 10	MA 9	MA 8
MA 11	MA 11	MA 10	MA 9
MA 12	MA 12	MA 11	MA 10
MA 13	MA 13	MA 12	MA 11
MA 14	MA 14	MA 13	MA 12
MA 15	MA 15	MA 14	MA 13

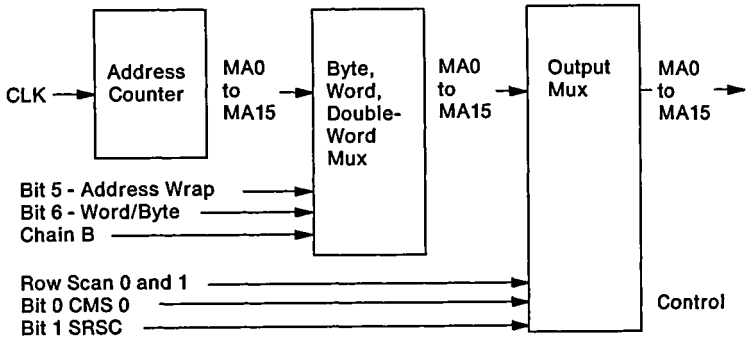


Figure 3-64. CRT Controller Memory Address Mapping

Bit 5 Address Wrap - Bit 5 selects memory address counter bit MA 13 or bit MA 15, and it appears on the MA 0 output pin in the Word Address mode. If the VGA is not in the Word Address mode, MA 0 counter output appears on the MA 0 output pin. When bit 5 is set to 1, MA 15 is selected. In odd/even mode, bit MA 15 should be selected since 256KB of video memory is installed on the system board. (Bit MA 13 is selected in applications where only 64KB memory is present. This function implements IBM Color/Graphics Monitor Adapter compatibility.)

Bit 4 Reserved.

Bit 3 Count By 2 - When bit 3 is set to 1, the memory address counter is clocked with the character clock input divided by 2. When bit 3 is set to 0, the memory address counter is clocked with the character clock input. This bit is used to create either a byte or word refresh address for the display buffer.

Bit 2 Horizontal Retrace Select - Bit 2 selects horizontal retrace or horizontal retrace divided by 2 as the clock that controls the vertical timing counter. This bit can be used to effectively double the vertical resolution capability of the CRT controller. The vertical counter has a maximum resolution of 1024 scan lines due to the 10-bit wide Vertical Total register. If the vertical counter is clocked with the horizontal retrace divided by 2, then the vertical resolution is doubled to 2048 horizontal scan lines. When bit 2 is set to 1, HRTC divided by 2 is selected. When bit 2 is set to 0, HRTC is selected.

Bit 1 Select Row Scan Counter - When bit 1 is set to 1, the MA 14 counter bit on the MA 14 output pin is selected. When bit 1 is set to 0, row scan counter bit 1 on the MA 14 output pin is selected.

Bit 0 Compatibility Mode Support - When bit 0 is set to 1, the MA 13 counter bit appears on the MA 13 output pin of the CRT controller. When bit 0 is set to 0, row scan address bit 0 is substituted for MA 13 during active display time. The CRT controller used on the IBM Color/Graphics Monitor Adapter is the 6845. The 6845 has 128 horizontal scan line address capability. To obtain 640 by 200 graphics resolution, the CRT controller is programmed for 100 horizontal scan lines with two row scan addresses per character row. Row scan address bit 0 becomes the most-significant address bit to the display buffer. Successive scan lines of the display image are displaced in memory by 8KB. This bit allows compatibility with the 6845 and color graphics APA modes of operation.

Line Compare Register

This is a read/write register pointed to when the value in the CRT Controller Address register is hex 18. The port address for this register is hex 03?5.

This register contains the least-significant 8 bits of the compare target. When the vertical counter reaches this value, the internal start of the line counter is cleared. As a result, an area of the screen is not affected by scrolling. Bit 8 of this value is in the CRT Controller Overflow register, index hex 07. Bit 9 is in the Maximum Scan Line register, index hex 09.

Graphics Controller Registers

This section contains descriptions of the following registers.

Figure 3-65. Graphics Controller Register Overview

Name	Port (hex)	Index (hex)
Graphics Address	03CE	-
Set/Reset	03CF	00
Enable Set/Reset	03CF	01
Color Compare	03CF	02
Data Rotate	03CF	03
Read Map Select	03CF	04
Graphics Mode	03CF	05
Miscellaneous	03CF	06
Color Don't Care	03CF	07
Bit Mask	03CF	08

Graphics Address Register

This is a read/write register and the port address for this register is hex 03CE.

Figure 3-66. Graphics Address Register

Bit	Function
7 - 4	Reserved = 0
3 - 0	Graphics Address

Bits 7 - 4 Reserved.

Bits 3 - 0 Bits 3 through 0 point to the other registers in the graphics section.

Set/Reset Register

This is a read/write register pointed to by the value in the Graphics Address register. This value must be hex 00 before writing can occur. The port address for this register is hex 03CF.

Figure 3-67. Set/Reset Register, Index Hex 00

Bit	Function
7 - 4	Reserved = 0
3	Set/Reset Map 3
2	Set/Reset Map 2
1	Set/Reset Map 1
0	Set/Reset Map 0

Bits 7 - 4 Reserved.

Bits 3 - 0 Bits 3 through 0 represent the value written to all 8 bits of the respective memory map when the system microprocessor does a memory write with write mode 0 selected and Set/Reset mode enabled. Set/Reset can be enabled on a map-by-map basis with separate OUT instructions to the Enable Set/Reset register, index hex 01.

Enable Set/Reset Register

This is a read/write register and is pointed to by the value in the Graphics Address register. This value must be hex 01 before writing can occur. The port address for this register is hex 03CF.

Figure 3-68. Enable Set/Reset Register, Index Hex 01

Bit	Function
7 - 4	Reserved = 0
3	Enable Set/Reset Map 3
2	Enable Set/Reset Map 2
1	Enable Set/Reset Map 1
0	Enable Set/Reset Map 0

Bits 7 - 4 Reserved.

Bits 3 - 0 Bits 3 through 0 enable the set/reset function. When enabled (bit = 1) and write mode is 0, the respective memory map is written with the value of the Set/Reset register. When write mode is 0 and Set/Reset is not enabled (bit = 0) on a map, that map is written with the value of the system microprocessor data.

Color Compare Register

This is a read/write register pointed to by the value in the Graphics Address register. This value must be hex 02 before writing can occur. The port address for this register is hex 03CF.

Figure 3-69. Color Compare Register, Index Hex 02

Bit	Function
7 - 4	Reserved = 0
3	Color Compare Map 3
2	Color Compare Map 2
1	Color Compare Map 1
0	Color Compare Map 0

Bits 7 - 4 Reserved.

Bits 3 - 0 Bits 3 through 0 represent a 4-bit color value to be compared. If the system microprocessor sets Read Type bit in the Graphics Mode register, index hex 05 and does a memory read, the data returned from the memory cycle will be a 1 in each bit position where the four maps equal the Color Compare register.

The color compare bit is the value that all bits of the corresponding map's byte are compared with. Each of the 8 bit positions of the selected byte are then compared across the four maps, and a 1 is returned in each bit position where the bits of all four maps equal their respective color compare values.

Data Rotate Register

This is a read/write register pointed to by the value in the Graphics Address register. This value must be hex 03 before writing can occur. The port address for this register is hex 03CF.

Figure 3-70. Data Rotate Register, Index Hex 03

Bit	Function
7 - 5	Reserved = 0
4	Function Select
3	Function Select
2	Rotate Count 2
1	Rotate Count 1
0	Rotate Count 0

Bits 7 - 5 Reserved.

Bits 4, 3 Data written to memory can operate logically with data already in the system microprocessor latches.

Data can be any of the choices selected by the Write Mode bits in the Graphics Mode register, index hex 05, except system microprocessor latches, which cannot be modified. If rotated data is selected, the rotate applies before the logical function. The bit functions are defined in Figure 3-71.

Figure 3-71. Function Select Bit Definitions

Bit 4	Bit 3	Function
0	0	Data unmodified.
0	1	Data ANDed with latched data.
1	0	Data ORed with latched data.
1	1	Data XORed with latched data.

Bits 2 - 0 Rotate Count - Bits 2 through 0 represent a binary encoded value of the number of positions to right-rotate the system microprocessor data bus during system microprocessor memory writes. This operation is done when the write mode is 0. To write non-rotated data, the system microprocessor must select a count of 0.

Read Map Select Register

This is a read/write register pointed to by the value in the Graphics Address register. This value must be hex 04 before writing can occur. The port address for this register is hex 03CF.

Figure 3-72. Read Map Select Register, Index Hex 04

Bit	Function
7 - 2	Reserved = 0
1	Map Select 1
0	Map Select 0

Bits 7 - 2 Reserved.

Bits 1, 0 Bits 1 and 0 represent a binary encoded value of the memory map from which the system microprocessor reads data. This register has no effect on the Color Compare Read mode. In odd/even modes the value may be 00 or 01 (10 or 11) for chained maps 0, 1 (2, 3).

Graphics Mode Register

This is a read/write register pointed to by the value in the Graphics Address register. This value must be hex 05 before writing can occur. The port address for this register is 03CF.

Figure 3-73. Graphics Mode Register, Index Hex 05

Bit	Function
7	Reserved = 0
6	256-Color Mode
5	Shift Register Mode
4	Odd/Even
3	Read Type
2	Reserved = 0
1, 0	Write Mode

Bit 7 Reserved.

Bit 6 When bit 6 is set to 1, the shift registers are loaded in a manner that supports the 256-Color mode. When bit 6 is set to 0, bit 5 is allowed to control the loading of the shift registers.

Bit 5 When bit 5 is set to 1, the shift registers in the graphics section format the serial data stream with even-numbered bits from both maps on the even-numbered maps and odd-numbered bits from both maps on the odd-numbered maps. This bit is used for modes 4 and 5.

Bit 4 Odd/Even - When bit 4 is set to 1, the odd/even addressing mode is selected, which is used for emulation of the IBM Color/Graphics Monitor Adapter compatible modes. Normally, this value follows the value of the Memory Mode register bit 2 (Odd/even) of the sequencer.

Bit 3 Read Type - When bit 3 is set to 1, the system microprocessor reads the results of the comparison of the four memory maps and the Color Compare register, index hex 02. When bit 3 is set to 0, the system microprocessor reads data from the memory map selected by the Read Map Select register, unless bit 3 (Chain 4) of the Memory Mode register equals 1. In this case, the Read Map Select register, index hex 04, has no effect.

Bit 2 Reserved.

Bits 1, 0 Write mode.

The bit functions are defined in Figure 3-74.

Figure 3-74. Write Mode Bit Definitions

Bit 1	Bit 0	Function
0	0	Each memory map is written with the system microprocessor data rotated by the number of counts in the Data Rotate register, unless Set/Reset is enabled for the map. Maps for which Set/Reset is enabled are written with 8 bits of the value contained in the Set/Reset register for that map.
0	1	Each memory map is written with the contents of the system microprocessor latches. These latches are loaded by a system microprocessor read operation.
1	0	Memory map *n* (0 through 3) is filled with 8 bits of the value of data bit *n*.
1	1	Each map is written with 8 bits of the value contained in the Set/Reset register for that map (the Enable Set/Reset register has no effect). Rotated system microprocessor data is ANDed with the Bit Mask register data to form an 8-bit value that performs the same function as the Bit Mask register does in write modes 0 and 2 (see "Bit Mask Register" on page 3-86).

The logic function specified by the Function Select bits in the Data Rotate register, index hex 03, is applied to data being written to memory following modes 0, 2, and 3 above.

Miscellaneous Register

This is a read/write register pointed to by the value in the Graphics Address register. This value must be hex 06 before writing can occur. The port address for this register is hex 03CF.

Figure 3-75. Miscellaneous Register, Index Hex 06

Bit	Function
7 - 4	Reserved = 0
3	Memory Map 1
2	Memory Map 0
1	Odd/Even
0	Graphics Mode

Bits 7 - 4 Reserved.

Bits 3, 2 Bits 3 and 2 control the mapping of the regenerative buffer into the system microprocessor address space. The bit functions are defined in Figure 3-76.

Figure 3-76. Memory Map Bit Definitions

Bit 3	Bit 2	Function
0	0	Hex A0000 for 128KB
0	1	Hex A0000 for 64KB
1	0	Hex B0000 for 32KB
1	1	Hex B8000 for 32KB

Bit 1 Odd/Even - When bit 1 is set to 1, the system microprocessor address bit 0 is replaced by a more-significant bit and odd/even maps to be selected with odd/even values of the system microprocessor A0 bit, respectively.

Bit 0 Graphics Mode - Bit 0 controls alphanumeric mode addressing. When bit 0 is set to 1, graphics mode is selected and the character generator address latches are disabled.

Color Don't Care Register

This is a read/write register and is pointed to by the value in the Graphics Address register. This value must be hex 07 before writing can occur. The port address for this register is hex 03CF.

Figure 3-77. Color Don't Care Register, Index Hex 07

Bit	Function
7 - 4	Reserved = 0
3	Map 3 = Don't Care
2	Map 2 = Don't Care
1	Map 1 = Don't Care
0	Map 0 = Don't Care

Bits 7 - 4 Reserved.

Bits 3 - 0 When any of bits 3 through 0 are set to 1, the associated map is included in the color compare cycle. When any of bits 3 through 0 are set to 0, the associated map is not included in the color compare cycle.

Bit Mask Register

This is a read/write register and is pointed to by the value in the Graphics Address register. This value must be hex 08 before writing can occur. The port address for this register is hex 03CF.

If any bit in this register is set to 1, writes are allowed to the corresponding bit in each map. When any bit is set to 0, the corresponding bit in each map will not change, provided that the location being written was the last location read by the system microprocessor.

The bit mask applies to write modes 0 and 2. To preserve bits using the bit mask, data must be latched internally by reading the location. When data is written to preserve the bits, the most current data in the latches is written in those positions. The bit mask applies to all maps simultaneously.

Attribute Controller Registers

This section contains descriptions of the following registers.

Figure 3-78. Attribute Controller Register Overview

Name	Port (hex)	Index (hex)
Address Register	03C0/1	-
Palette Registers	03C0/1	00-0F
Attribute Mode Control Register	03C0/1	10
Overscan Color Register	03C0/1	11
Color Plane Enable Register	03C0/1	12
Horizontal PEL Panning Register	03C0/1	13
Color Select Register	03C0/1	14

Each Attribute Data register is written at hex 03C0 as described below. Data is read from the registers at address hex 03C1.

Attribute Address Register

This is a read/write register. The port address is hex 03C0.

Figure 3-79. Attribute Address Register

Bit	Function
7, 6	Reserved = 0
5	Palette Address Source
4 - 0	Attribute Address

Bits 7, 6 Reserved.

Bit 5 Bit 5 must be set to 1 for normal operation of the attribute controller. This enables the video memory data to access the Palette registers. Bit 5 must be set to 0 when loading the Palette registers.

Bits 4 - 0 Bits 4 through 0 is a binary value that points to the Attribute Data register where data is to be written.

The Attribute Controller register does not have an address bit input to control selection of the address and data registers. An internal address latch controls selection of either the address or data registers. To initialize the latch, an IOR instruction is issued to the attribute controller at address hex 03BA or 03DA. This clears the latch, and selects the address register. After the address register has been loaded with an OUT to hex 03C0, the next OUT instruction to hex 03C0 loads the data register.

The latch toggles each time an OUT instruction is issued to the attribute controller. It does not toggle on IN instructions for a read to 03C1. (See "VGA Programming Considerations" on page 3-93.)

Palette Registers

These are read/write registers pointed to by the value in the Attribute Address register. This value must be hex 00 - 0F before writing can occur. The output port address for these registers is hex 03C0. The input port address is hex 03C1.

Figure 3-80. Palette Registers, Index Hex 00-0F

Bit	Function
7, 6	Reserved = 0
5	P5
4	P4
3	P3
2	P2
1	P1
0	P0

Bits 7, 6 Reserved.

Bits 5 - 0 Bits 5 through 0 allow a dynamic mapping between the text attribute or graphic color input value and the display color on the CRT. The value in these six bits selects the appropriate color.

The Palette registers should be modified only during the vertical retrace interval to avoid problems with the displayed image. These internal Palette register values are sent to the video DAC, where they in turn serve as addresses into the video DAC internal registers. (See "Attribute Controller" on page 3-21.)

Attribute Mode Control Register

This is a read/write register pointed to by the value in the Attribute Address register. This value must be hex 10 before writing can occur. The output port address for this register is hex 03C0. The input port address for this register is hex 03C1.

Figure 3-81. Attribute Mode Control Register, Index Hex 10

Bit	Function
7	P5, P4 Select
6	PEL Width
5	PEL Panning Compatibility
4	Reserved = 0
3	Select Background Intensity or Enable Blink
2	Enable Line Graphics Character Codes
1	Monochrome/Color Emulation
0	Graphics/Alphanumeric Mode

Bit 7 P5, P4 Select - When bit 7 is set to 1, P5 and P4 are bits 1 and 0 of the Color Select register. When bit 7 is set to 0, P5 and P4 are the outputs of the Palette registers. (See "Attribute Controller" on page 3-21 and "Video DAC Programming Considerations" on page 3-103.)

Bit 6 PEL Width - When bit 6 is set to 1, the video pipeline is sampled so that 8 bits are available to select a color in the 256-Color mode (hex 13). Bit 6 should be set to 0 in all other modes.

Bit 5 PEL Panning Compatibility - When bit 5 is set to 1, a successful line compare in the CRT controller forces the output of the Horizontal PEL Panning register to 0 until +VSYNC becomes active, at which time the output returns to its programmed value. This bit allows a selected portion of a screen to be panned. When bit 5 is set to 0, line compare has no effect on the output of the Horizontal PEL Panning register.

Bit 4 Reserved.

Bit 3 Enable Blink/Select Background Intensity - When bit 3 is set to 1, the blink attribute in alphanumeric modes is enabled. Bit 3 must also be set to 1 for blinking graphics modes. When bit 3 is set to 0, the background intensity of the attribute input is selected. This mode is also available on the IBM Monochrome and Color/Graphics Monitor adapters.

Bit 2 Enable Line Graphics Character Codes - When bit 2 is set to 1, the special line graphics character codes are enabled for the IBM Monochrome emulation mode. When bit 2 is set to 0, the ninth dot will be the same as the background.

When enabled, this bit forces the ninth dot of a line graphic character to be identical to the eighth dot of the character. The line graphics character codes for the Monochrome emulation mode are hex C0 through hex DF.

For character fonts that do not use the line graphics character codes in the range of hex C0 through hex DF, bit 2 should be a logical 0. Otherwise, unwanted video information is displayed on the CRT screen.

BIOS sets this bit, the correct dot clock, and other registers when a 9-dot alphanumeric mode is set.

Bit 1 Monochrome/Color Emulation - When bit 1 is set to 1, a monochrome emulation mode is set. When bit 1 is set to 0, a color emulation mode is set.

Bit 0 Graphics/Alphanumeric Mode - When bit 0 is set to 1, graphics mode is selected. When bit 0 is set to 0, alphanumeric mode is selected.

Overscan Color Register

This is a read/write register pointed to by the value in the Attribute Address register. This value must be hex 11 before writing can occur. The output port address for this register is hex 03C0. The input port address for this register is hex 03C1.

This register determines the overscan (border) color displayed on the CRT.

The border is a band of color around the perimeter of the display area. Its width is the same as one 80-column character. This border is not supported in the 40-column alphanumeric modes or the 320-PEL graphics modes, except for mode hex 13.

Color Plane Enable Register

This is a read/write register pointed to by the value in the Attribute Address register. This value must be hex 12 before writing can occur. The output port address for this register is 03C0. The input port address for this register is 03C1.

Figure 3-82. Color Plane Enable Register, Index Hex 12

Bit	Function
7, 6	Reserved = 0
5, 4	Video Status MUX
3 - 0	Enable Color Plane

Bits 7, 6 Reserved.

Bits 5, 4 Video Status MUX - Bits 5 and 4 select two of the eight color outputs to be available on the status port. Figure 3-83 shows the combinations available and the color output wiring.

Figure 3-83. Color Output Wiring

Color Plane Register		Input Status Register 1	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

Bits 3 - 0 Enable Color Plane - When any of bits 3 through 0 is a 1, the respective display memory color plane is enabled.

Horizontal PEL Panning Register

This is a read/write register pointed to by the value in the Attribute Address register. This value must be hex 13 before writing can occur. The output port address for this register is hex 03C0. The input port address for this register is hex 03C1.

Figure 3-84. Horizontal PEL Panning Register, Index Hex 13

Bit	Function
7 - 4	Reserved = 0
3 - 0	Horizontal PEL Panning

Bits 7 - 4 Reserved.

Bits 3 - 0 Bits 3 through 0 select the number of PELs to shift the video data horizontally to the left. PEL panning is available in both alphanumeric (A/N) and all points addressable (APA) modes. In modes 0+, 1+, 2+, 3+, 7, and 7+ the image can be shifted a maximum of 8 PELs. In 256-Color APA mode (mode 13), the image can be shifted a maximum of 3 PELs. Further panning may be accomplished by changing the start address in the CRT controller. In all other A/N and APA modes, the image can be shifted a maximum of 7 PELs. The sequence for shifting the image is shown in Figure 3-85.

Figure 3-85. Image Shifting

PEL Panning Register Value	Number of PELs Shifted to the Left		
	0+, 1+, 2+, 3+, 7, 7+	All Other Modes	Mode 13
0	1	0	0
1	2	1	-
2	3	2	1
3	4	3	-
4	5	4	2
5	6	5	-
6	7	6	3
7	8	7	-
8	0	-	-

Color Select Register

This is a read/write register pointed to by the value in the Attribute Address register. This value must be hex 14 before writing can occur. The port address for this register is hex 03C1 for input and hex 03C0 for output.

Figure 3-86. Color Select Register, Index Hex 14

Bit	Function
7 - 4	Reserved = 0
3	S_color 7
2	S_color 6
1	S_color 5
0	S_color 4

Bits 3, 2 Bits 3 and 2 are the 2 most-significant bits of the 8-bit digital color value in all modes except 256-Color Graphics mode. In 256-Color Graphics mode, the 8-bit attribute stored in video memory becomes the 8-bit digital color value sent to the Video DAC. (See "VGA Programming Considerations.")

Bits 1, 0 Bits 1 and 0 can be used in place of the P4, P5 outputs from the Palette registers to form the 8-bit digital color value sent to the Video DAC. (See "Attribute Mode Control Register" on page 3-89.) Bits 1 and 0 are also used to rapidly switch between sets of colors in the video DAC.

VGA Programming Considerations

The following are some programming considerations for the VGA.

- Certain internal timings must be guaranteed by the user to have the CRT controller perform properly. These timings can be guaranteed by ensuring that the rules listed below are followed when programming the CRT controller.
  - The Horizontal Total register (RO) must be greater than or equal to a value of 25 (decimal).
  - The minimum positive pulse width of the HSYNC signal must be four character clock units.
  - End Horizontal Retrace register must be programmed so that the HSYNC output goes to 0 at least one character clock time before the horizontal display enable signal goes to 1.

- Vertical Retrace Start register must be a minimum of one horizontal scan line greater than the Vertical Display Enable End register which defines where the vertical display enable signal ends.

All of the above rules are satisfied when the video mode is set by the BIOS.

- When bit 5 of the Attribute Mode Control register is 1, a successful line compare (see "Line Compare Register" on page 3-79) in the CRT controller forces the output of the Horizontal PEL Panning register to 0 until VSYNC occurs. When VSYNC occurs, the output returns to the programmed value. This allows the portion of the screen indicated by the Line Compare register to be operated on by the Horizontal PEL Panning register.
- A write to the Character Map Select register becomes valid on the next whole character line. No deformed characters are displayed by changing character generators in the middle of a character scan line.
- For 256-Color 320-by-200 Graphics mode (hex 13), the attribute controller is configured so that the 8-bit attribute stored in video memory for each PEL becomes the 8-bit address (P0 - P7) into the DAC. The user should not modify the contents of the internal Palette registers when using this mode.
- The following sequence should be followed when accessing any of the Attribute Data registers pointed to by the Attribute Address register:

  1. Disable interrupts
  2. Reset read/write latch
  3. Write to Attribute Address register
  4. Read from or write to a data register
  5. Enable interrupts.

- The Color Select register in the attribute controller section may be used to rapidly switch between sets of colors in the video DAC. When bit 7 of the Attribute Mode Control register is 0, the 8-bit color value presented to the video DAC is composed of 6 bits from the internal Palette registers and bits 2 and 3 from the Color Select register. When bit 7 of the Attribute Mode Control register is 1, the 8-bit color value presented to the video DAC is composed of the lower 4 bits from the internal Palette registers and the 4 bits in the Color Select register. By changing the value in the Color Select register, the software rapidly switches between sets of colors in the video DAC. Note that BIOS does not support multiple sets of colors in the video DAC. The user must load

these colors if this function is to be used. (See "Attribute Controller" on page 3-21.) Note that the above discussion applies to all modes except 256-Color Graphics mode. In this mode, the Color Select register is not used to switch between sets of colors.

- An application that saves the video state must store the 4 bytes of information contained in the system microprocessor latches in the graphics controller subsection. These latches are loaded with 32 bits from video memory (8 bits per map) each time the system microprocessor does a read from video memory. The application needs to:

  1. Use write mode 1 (Graphics Mode register) to write the values in the latches to a location in video memory that is not part of the display buffer. The last location in the address range is a good choice.
  2. Save the values of the latches by reading them back from video memory.

  Note: If in a chain 4 or odd/even mode (Memory Mode register), it will be necessary to reconfigure the memory organization as four sequential maps prior to performing the sequence above. BIOS provides support for completely saving and restoring video state. (See *BIOS Interface Technical Reference for IBM PS/1™ Computer.*)

- The description of the Horizontal PEL Panning register includes a figure showing the number of PELs shifted left for each valid value of the Horizontal PEL Panning register and each valid video mode. Further panning beyond that shown in the figure may be accomplished by changing the start address in the CRT Controller registers (Start Address High and Start Address Low). The sequence involved in further panning would be as follows:

  1. Use the Horizontal PEL Panning register to shift the maximum number of bits to the left. (See Figure 3-84 on page 3-92 for the appropriate values.)
  2. Increment the start address.
  3. If modes 0+, 1+, 2+, 3+,7, or 7+ are not used, set the Horizontal PEL Panning register to 0. If these modes are used, set the Horizontal PEL Panning register to 8. The screen will now be shifted 1 PEL left of the position it was in at the end of step 1. Step 1 through step 3 may be repeated as desired.

- The Line Compare register (CRT Controller register, index hex 18) should be programmed with even values in 200-line modes

when used in split screen applications that scroll a second screen on top of a first screen. This is a requirement imposed by the double scan logic in the CRT Controller.

- If the Cursor Start register (CRT Controller register, index hex 0A) is programmed with a value greater than that in the Cursor End register (CRT Controller register, index hex 0B), then no cursor is displayed. A split cursor is not possible.
- In 8-dot character modes, the underline attribute produces a solid line across adjacent characters, as in the IBM Color/Graphics Monitor Adapter, Monochrome Display Adapter and the Enhanced Graphics Adapter. In 9-dot modes, the underline across adjacent characters is dashed, as in the IBM 327X display terminals. In 9-dot modes, the line graphics characters (hex C0 - DF character codes) have solid underlines.

Programming the Registers

Each of the video subsections has an address register and a number of data registers. The address register serves as a pointer to the other registers on the device. These registers are loaded by the system microprocessor by executing an OUT instruction to its I/O address with the index of the selected data register.

The data registers in each subsection are accessed through a common I/O address. They are distinguished by the pointer (index) in the address register. To write to a data register, the address register is loaded with the index of the appropriate data register, then the selected data register is loaded by executing an OUT instruction to the common I/O address.

The general registers are not accessed through an address register; they are written directly.

See "Video DAC/System Microprocessor Interface" on page 3-102 for details on accessing the video DAC.

For compatibility with the IBM Enhanced Graphics Adapter (EGA), the internal VGA palette is programmed the same as the EGA. The video DAC is programmed by BIOS so that the compatible values in the internal VGA palette produce a color compatible with that produced by EGA. Mode hex 13 (256 colors) is programmed so that the first 16 locations in the DAC produce compatible colors.

The color palette is changed when BIOS is used to load the video DAC palette for a color mode, and a monochrome display is connected to the system unit. The colors are summed to produce shades of gray that allow color applications to produce a readable screen.

There are 4 bits that should not be modified (unless the sequencer is reset by setting bit 1 of the Reset register to 0). These bits are:

- Bit 3 or bit 0 of the Clocking Mode register
- Bit 3 or bit 2 of the Miscellaneous Output register.

RAM-Loadable Character Generator

The character generator is RAM-loadable and can support characters up to 32 scan lines high. Three character generators are stored within the BIOS, and one is automatically loaded into the RAM by the BIOS when an alphanumeric mode is selected. The Character Map Select register can be programmed to define the function of bit 3 of the attribute byte to be a character generator switch. This allows the user to select between any two character sets residing in map 2. This effectively gives the user access to 512 characters instead of 256. Character tables can be loaded offline. Up to eight tables can be loaded.

The structure of the character tables is described in Figure 3-87. The character generator is in map 2 and must be protected using the map mask function.

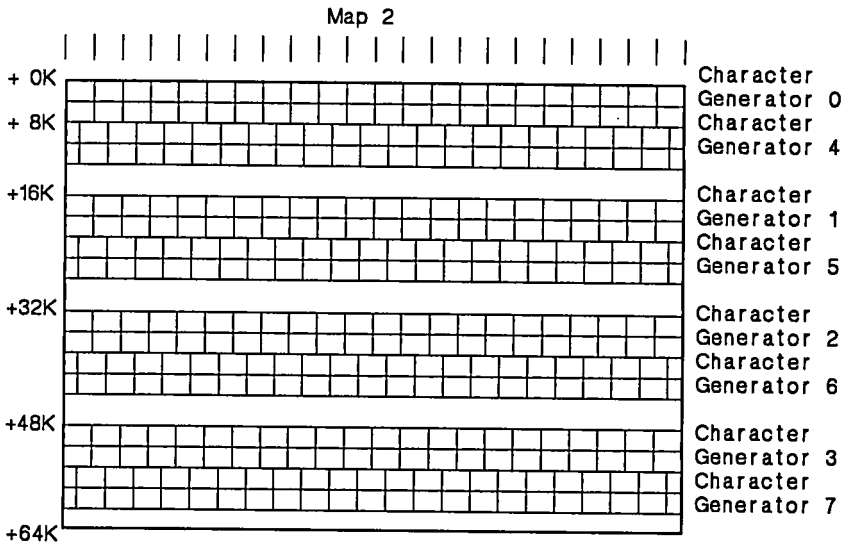


Figure 3-87. Character Table Structure

Figure 3-88 shows the structure of each character pattern. If the CRT controller is programmed to generate *n* row scans, then *n* bytes must be filled in for each character in the character generator. The example assumes eight row scans per character.

Address	Byte Image								Data
CC * 32 + 0				X	X				18H
1			X	X	X	X			3EH
2		X	X			X	X		66H
3		X	X			X	X		66H
4		X	X	X	X	X	X		7EH
5		X	X			X	X		66H
6		X	X			X	X		66H
7		X	X			X	X		66H

Figure 3-88. Character Pattern Example

Note: CC equals the value of the character code. For example, hex 41 is the character code for an ASCII A.

Creating a Split Screen

The VGA hardware supports a dual-screen display. The top portion of the screen is designated as screen A and the bottom portion of the screen is designated as screen B, as shown in Figure 3-89.

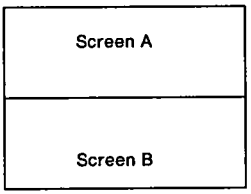


Figure 3-89. Dual-Screen Definition

Figure 3-90 shows the screen mapping for a system containing a 32KB alphanumeric storage buffer. Note that the VGA has a 32KB storage buffer in alphanumeric mode. Information displayed on screen A is defined by the Start Address High and Low registers (index hex 0CH and 0DH) of the CRT controller. Information displayed on screen B always begins at address hex 0000.

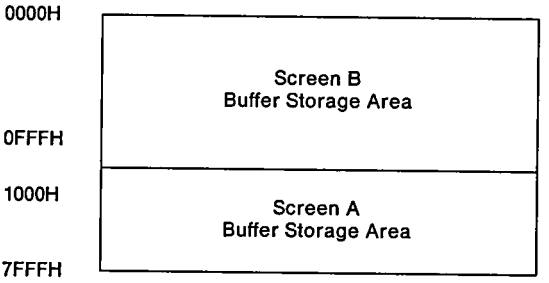


Figure 3-90. Screen Mapping within the Display Buffer Address Space

The Line Compare register (index hex 18H) of the CRT controller performs the split screen function. The CRT controller has an internal horizontal scan line counter. The CRT controller also has logic that compares the horizontal scan line counter value to the Line Compare register value and clears the memory address generator when a compare occurs. The linear address generator then sequentially addresses the display buffer starting at location 0, and each subsequent row address is determined by the 16-bit addition of the start of line latch and the Offset register.

Screen B can be smoothly scrolled onto the CRT by updating the Line Compare in synchronization with the vertical retrace signal. The information on screen B is not affected by scrolling operations that utilize the Start Address High and Low registers to scroll through the Screen A address map.

When bit 5 of the Attribute Mode Control register is 1, a successful line compare forces the output of the Horizontal PEL Panning register to 0 until vertical synchronization occurs. When VSYNC occurs, the output returns to its programmed value. This feature allows the information on screen B to remain unaffected by PEL panning operations on screen A.

Video Digital-to-Analog Converter (Video DAC)

The video DAC integrates the function of a color look-up table with three internal DACs for driving an analog display.

The size of the color look-up table is 256 by 18 bits to allow the display of 256 colors from a palette of over 256,000 possible colors. Each RGB analog output is driven by a 6-bit DAC. Each register in the color look-up table contains 6 bits each for the red, green, and blue DACs.

Figure 3-91. Video DAC I/O Address Usage
Video Digital-to-Analog Converter (DAC) Addresses in Hex

PEL Address (Write mode)	RW	03C8
PEL Address (Read mode)	WO	03C7
DAC State Register	RO	03C7
PEL Data Register	RW	03C9
PEL Mask *	RW	03C6

RO = Read-Only, RW = Read / Write, WO = Write-Only.

* This register must not be written to by application code, or destruction of the color look-up table may occur. (See "Video DAC Programming Considerations" on page 3-103.)

Video DAC Operation

The PEL address inputs (P0 - P7) and the blanking input are sampled on the rising edge of the PEL clock. After three further rising edges of the PEL clock, the analog outputs reflect the state of these inputs.

During normal operation, the PEL address inputs (P0 - P7) are used as a pointer to one of the 256 internal registers (color look-up table). The value in each register is then, in turn, converted to an analog signal for each of the three analog outputs (red, green, blue). The blanking input can also be used to force the analog outputs to 0 volts. The blanking operation is independent of the state of the PEL address inputs.

During system microprocessor accesses, the 8-bit PEL Address register acts as a pointer to the 256 internal registers. Each internal register is 18 bits wide; 6 bits each for red, green, and blue. The internal registers are accessible through the system microprocessor interface as described on the following page.

The system microprocessor interface is asynchronous with the video path. The timing of this interface is controlled by the write enable and read enable signals.

Video DAC/System Microprocessor Interface

The PEL Address register holds an 8-bit value that is used to address a location within the color look-up table. The PEL Address register may be written at two different addresses to establish a read or write mode, respectively. Once the PEL Address register has been written and an access has been made to a location in the color look-up table, the PEL Address register automatically increments and further accesses may occur to successive locations.

Each time the PEL Address register is written at address hex 03C8, it identifies that a write sequence will occur. A write sequence consists of three successive byte writes to the PEL Data register at address hex 03C9. The least-significant 6 bits of each byte are concatenated to form the value placed in the 18-bit Data register. The order is red byte first, then green, and finally blue. Once the third byte has been written, the value in the Data register is written to the location pointed to by the PEL Address register. The order of events for a write cycle is:

1. Write the PEL Address register at hex 03C8.
2. Three bytes are written to the PEL Data register at hex 03C9.
3. The contents of the PEL Data register are transferred to the location in the color look-up table pointed to by the PEL Address register.
4. The PEL Address register auto-increments by 1.
5. Go to step 2.

Each time the PEL Address register is written at address hex 03C7, it identifies that a read sequence will occur. A read sequence consists of three successive byte reads from the PEL Data register at address hex 03C9. The least-significant 6 bits of each byte taken from the PEL Data register contain the corresponding color value. The order is red byte first, then green, and finally blue. The order of events for a read cycle is:

1. Write the PEL Address register at hex 03C7.
2. The contents of the location in the color look-up table pointed to by the PEL Address register are transferred to the PEL Data register.

3. The PEL Address register auto-increments by one.
4. Three bytes are read back from the PEL Data register at hex 03C9.
5. Go to step 2.

If the PEL Address register is written during either a read or write cycle, a mode is initialized and the unfinished cycle is aborted. The effects of writing the PEL Data register during a read cycle or reading the PEL Data register during a write cycle are undefined and may change the look-up table contents.

A read from address hex 03C7 returns 0's in bit positions 0 and 1 if the video DAC is currently in a read mode. A read from address hex 03C7 returns 1's in bit positions 0 and 1 if the video DAC is currently in a write mode.

Reads from the PEL Address register at hex 03C8 or the DAC State register at hex 03C7 do not interfere with read or write cycles and may occur at any time.

Video DAC Programming Considerations

As explained above, the effects of writing the PEL Data register during a read cycle or reading the PEL Data register during a write cycle are undefined and may change the look-up table contents. Therefore, the following sequence must be followed to ensure the color look-up table integrity during accesses to it:

1. Write address to the PEL Address register.
2. Disable Interrupts.
3. Write or read three bytes of data.
4. Go to step 3. Repeat this step for the desired number of locations.
5. Enable interrupts.

Note: The above sequence assumes that any interrupting process will return the video DAC in the correct mode (write or read). If this is not the case, the sequence shown below should be followed:

1. Disable interrupts.
2. Write address to PEL Address register.
3. Write or read three bytes of data.
4. Go to step 2. Repeat this step for the desired number of locations.
5. Enable interrupts.

There is a timing requirement on the minimum amount of time that must separate the trailing edge of one Read or Write command to the video DAC and the leading edge of the next Read or Write command. The minimum separation is 240 nanoseconds. Software must ensure that the 240-nanosecond separation exists between two successive accesses to the video DAC. Assembly language programs can meet this requirement by placing a JMP $+2 instruction between successive accesses to the video DAC.

To prevent *snow* on the screen, an application reading or writing the Video DAC register should ensure that the blanking input to the video DAC is asserted. This can be accomplished either by restricting data transfers to retrace intervals (use Input Status register 1 to determine when retrace is occurring) or by using the screen off bit located in the Clocking Mode register of the sequencer subsection.

Note: BIOS provides read and write interfaces to the video DAC.

The PEL Mask register (hex 03C6) must not be written by application code, or destruction of the color look-up table may result. This register is correctly initialized to hex FF by BIOS during a video mode set.

Display Connector Timing (SYNC Signals)

BIOS sets the VGA registers to generate the video modes. The video modes are shown in Figure 3-13 on page 3-22. All of these modes are 70 Hz vertical retrace except for modes 11 and 12. These two modes are 60 Hz vertical retrace. The VGA generates timings that are within the specifications for the supported displays using these modes.

The analog displays operate from 60 to 70 Hz vertical retrace frequency. The following timing diagrams represent only the vertical frequencies set by BIOS.

Note: The vertical size of the display is encoded using the polarity of the SYNC signals as shown in Figure 3-92. (See "Miscellaneous Output Register" on page 3-54.) The polarity of the SYNC pulse refers to whether it is a positive pulse (with respect to ground) or a negative pulse (with respect to +5 V dc).

Figure 3-92. Display Vertical Size

VSYNC Polarity	HSYNC Polarity	Vertical Size
+	+	Reserved
-	+	350 lines
+	-	400 lines
-	-	480 lines

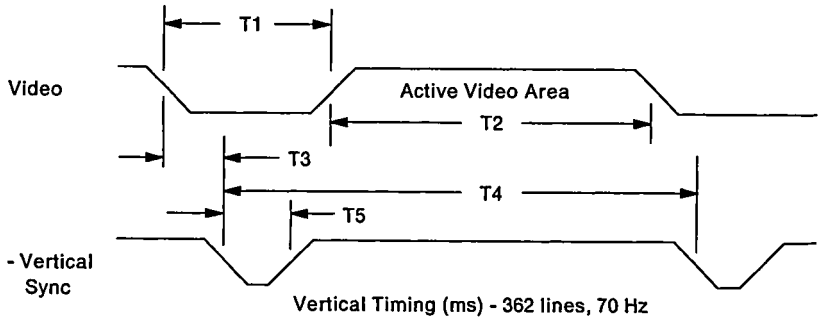


Figure 3-93. Display Vertical SYNC, 350 Lines

Signal	Time
T1	2.765 milliseconds
T2	11.504 milliseconds
T3	0.985 milliseconds
T4	14.268 milliseconds
T5	0.064 milliseconds

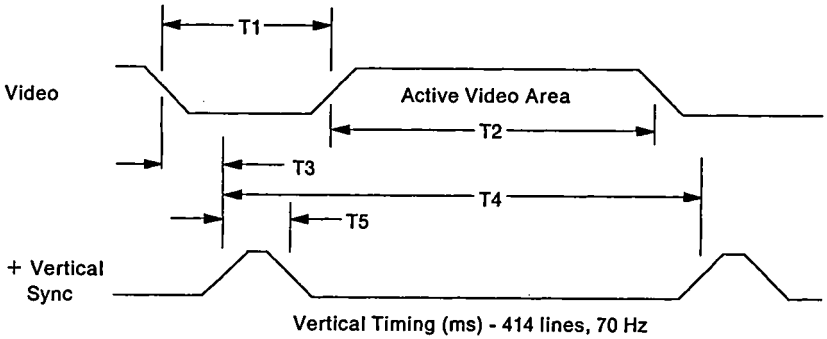


Figure 3-94. Display Vertical SYNC, 400 Lines

Signal	Time
T1	1.112 milliseconds
T2	13.156 milliseconds
T3	0.159 milliseconds
T4	14.268 milliseconds
T5	0.064 milliseconds

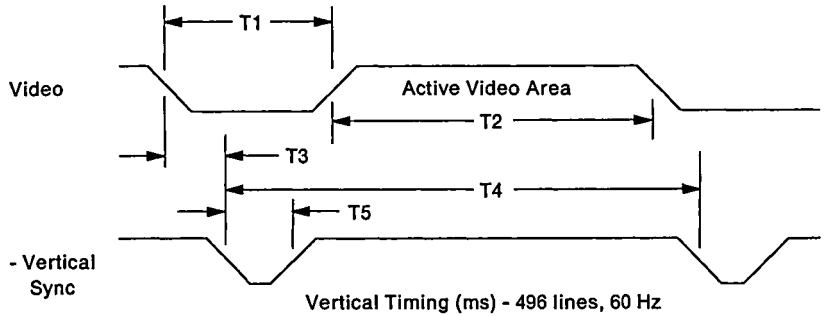
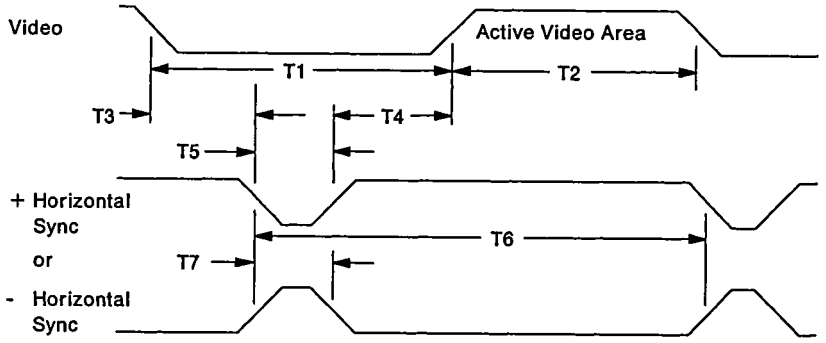


Figure 3-95. Display Vertical SYNC, 480 Lines

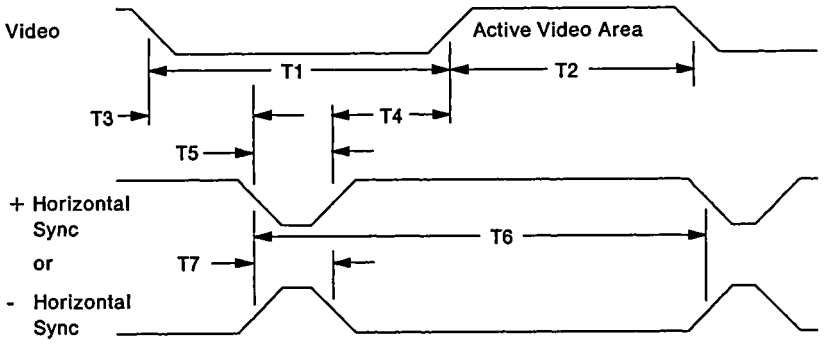
Signal	Time
T1	0.922 milliseconds
T2	15.762 milliseconds
T3	0.064 milliseconds
T4	16.683 milliseconds
T5	0.064 milliseconds



Horizontal Timing (μs) – 80 column with border

Figure 3-96. Display Horizontal Timing, 80 Column with Border

Signal	Time
T1	5.720 microseconds
T2	26.058 microseconds
T3	0.318 microseconds
T4	1.589 microseconds
T5	3.813 microseconds
T6	31.778 microseconds
T7	3.813 microseconds



Horizontal Timing (μs) – 40/80 column, no border

Figure 3-97. Display Horizontal Timing, 40/80 Column, no Border

Signal	Time
T1	6.356 microseconds
T2	25.422 microseconds
T3	0.636 microseconds
T4	1.907 microseconds
T5	3.813 microseconds
T6	31.778 microseconds
T7	3.813 microseconds

Display Connector

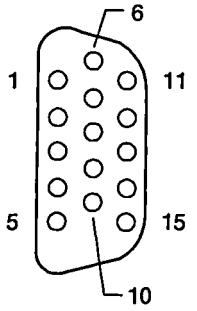


Figure 3-98. Display Connector Signals

Pin	Signal
1	Red Video
2	Green Video
3	Blue Video
4	NC
5	Ground
6	Ground (Analog)
7	Ground (Analog)
8	Ground (Analog)
9	NC
10	Ground
11	NC
12	NC
13	Horizontal SYNC
14	Vertical SYNC
15	NC

Diskette Drive Controller

The diskette drive controller and connector are on the system board.

Note: This section is included as a guide to compatibility for existing software. New software should access the diskette drive controller through BIOS.

The Intel 82077AA diskette controller interfaces with the diskette drives. The controller operates in the IBM PS/2® Model 30 compatibility mode. The following are supported by the system board:

- Two drives
- 1.44MB, 3.5-inch drive accepting either 1MB or 2MB unformatted media
- 360KB, 5.25-inch drive
- 1.2MB, 5.25-inch drive
  - using both 1.2MB and 360KB formats
  - operating at 500K bps at high density and 300K bps at low density.

Precompensation of 125 nanoseconds is provided for all cylinders.

The diskette drive controller reads and writes both high- and low-density media.

Warning: Sixteen-bit operations to the video subsystem can cause a diskette overrun in the 1.44MB mode because data width conversions may require more than 12 microseconds. If an overrun occurs, BIOS returns an error code and the operation should be retried.

Warning: The diskette controller does not check if the media supports the density selected. Low density media (360KB or 720KB) will not be reliably formatted to the high density (1.2MB or 1.44MB) and loss of data may result. High density media will not be reliably formatted to the low density and loss of data may result. The diskette should be formatted at the correct density.

PS/2 is a registered trademark of the International Business Machines Corporation.

Registers

Status Register A

This is a read-only register that shows the status of the corresponding signals. The input port address is hex 03F0.

Figure 3-99. Status Register A (Hex 03F0)

Bit	Function
7	IRQ6
6	DRQ2
5	Step (latched)
4	Track 0
3	-Head 1 Select
2	Index
1	Write Protect
0	-Direction

Status Register B

This is a read-only register that shows the status of signals between the diskette drive and the controller. The input port address is hex 03F1.

Figure 3-100. Status Register B (Hex 03F1)

Bit	Function
7	-Drive 2 Installed
6	-Drive Select 1
5	-Drive Select 0
4	Write Data (latched)
3	Read Data (latched)
2	Write Enable (latched)
1, 0	Reserved

Digital Output Register

This is a write-only register used to control drive motors, drive selection, and feature enable. All bits are cleared by a Reset. The output port address is hex 03F2.

Figure 3-101. Digital Output Register (Hex 03F2)

Bit	Function
7, 6	Reserved
5	Motor Enable 1
4	Motor Enable 0
3	DMA and Interrupt Enable
2	-Controller Reset
1, 0	Drive Select (0 or 1)*

* 00 = drive 0, 01 = drive 1

Digital Input Register

This is a read-only register used to sense the state of the diskette change signal and for diagnostic purposes. The input port address is hex 03F7.

Figure 3-102. Digital Input Register (Hex 03F7)

Bit	Function
7	-Diskette Change
6 - 4	Reserved
3	DMA enable
2	No Write Pre Comp
1, 0	Data Rate Select (0 or 1)*

* 00 = 500K bps, 10 = 250K bps, 01 = 300K bps

Configuration Control Register

This is a write-only register used to set the transfer rate. The output port address is hex 03F7.

Figure 3-103. Configuration Control Register (Hex 03F7)

Bit	Function
7 - 3	Reserved = 0
2	No write Pre Comp
1, 0	Data Rate Select (0 or 1)*

* 00 = 500K bps, 10 = 250K bps, 01 = 300K bps

Diskette Drive Controller Status Register

This is a read-only register used to facilitate the transfer of data between system microprocessor and the controller. The input port address is hex 03F4.

Figure 3-104. Diskette Drive Controller Status Register (Hex 03F4)

Bit	Function
7	Request for Master
6	Data Input/Output
5	Non-DMA Mode
4	Diskette Controller Busy
3	Reserved
2	Reserved
1	Drive 1 Busy
0	Drive 0 Busy

Bit 7 When bit 7 is set to 1, the Data register is ready for transfer with the system microprocessor.

Bit 6 When bit 6 is set to 1, the data transfer is from the diskette drive controller to the system microprocessor. When bit 6 is set to 0, the data transfer is from the system microprocessor to the diskette drive controller.

Bit 5 When bit 5 is set to 1, the diskette drive controller is in the non-DMA mode.

Bit 4 When bit 4 is set to 1, a Read or Write command is being executed.

Bit 3, 2 Reserved.

Bit 1 When bit 1 is set to 1, diskette drive 1 is in the seek mode.

Bit 0 When bit 0 is set to 1, diskette drive 0 is in the seek mode.

Data Registers, Hex 03F5

Address hex 03F5 is the address/data register for several registers in a stack with only one register presented to the data bus at a time. These registers store data, commands, and parameters, and provide diskette-drive status information. Data bytes are passed through the address/data register to program or obtain results after a command.

Diskette Drive Controller Programming Considerations

Each command is initiated by a multibyte transfer from the system microprocessor, and the result can also be a multibyte transfer back to the system microprocessor. Because of this multibyte interchange of information between the diskette drive controller and the microprocessor, each command is considered to consist of three phases:

Command Phase: The system microprocessor issues a series of writes to the diskette drive controller that direct it to perform a specific operation.

Execution Phase: The controller performs the specified operation.

Result Phase: After completion of the operation, status and other housekeeping information is made available from the system microprocessor through a sequence of Read commands.

The following is a summary of the commands that are issued to the diskette drive controller.

- Read Data command
- Read Deleted-Data command
- Read Track command
- Read ID command
- Write Data command
- Write Deleted-Data command
- Format Track command
- Recalibrate command
- Sense Interrupt Status command
- Specify command
- Sense Drive Status command
- Seek command.

Figure 3-105 shows the symbols used in the format of the individual commands. (See "Command Format" on page 3-118 for the individual commands.)

Figure 3-105 (Page 1 of 2). Command Symbols, Diskette Drive Controller

Symbol	Name	Description
C	Cylinder Number	C contains the current or selected cylinder number in binary notation.
D	Data	D contains the data pattern to be written to a sector.
D7-D0	Data Bus	An 8-bit data bus in which D7 is the most-significant bit and D0 is the least-significant bit.
DTL	Data Length	When N is 00, DTL is the data length to be read from or written to a sector.
EOT	End of Track	The final sector number on a cylinder.
GPL	Gap Length	The length of gap 3 (spacing between sectors excluding the voltage-controlled oscillator synchronous field).
H	Head Address	The head number, either 0 or 1, as specified in the ID field.
HD	Head	The selected head number, 0 or 1 (H=HD in all command words).
HLT	Head Load Time	The head load time in the selected drive (2 to 254 milliseconds in 2-millisecond increments).
HUT	Head Unload Time	The head unload time after a read or write operation (16 to 240 milliseconds in 16-millisecond increments).

Figure 3-105 (Page 2 of 2). Command Symbols, Diskette Drive Controller

Symbol	Name	Description
MF	FM or MFM Mode	A 0 selects FM mode and a 1 selects MFM.
MT	Multitrack	A 1 selects multitrack operation (both HD0 and HD1 will be read or written).
N	Number	The number of data bytes written in a sector.
NCN	New Cylinder Number	The new cylinder number for a seek operation.
ND	Non-Data Mode	This indicates an operation in the non-data mode.
PCN	Present Cylinder Number	The cylinder number at the completion of a Sense Interrupt Status command (present position of the head).
R	Record	The sector number to be read or written.
SC	Sector	The number of sectors per cylinder.
SK	Skip	This stands for skip deleted-data address mark.
SRT	Step Rate	The stepping rate for the diskette drive (1 to 16 milliseconds in 1-millisecond increments).
ST 0 - ST 3	Status 0-Status 3	Four registers that store status information after a command is executed.
STP	Scan Test	If STP is 1, the data in contiguous sectors is compared with the data sent by the system microprocessor during a scan operation. If STP is 2, then alternate sectors are read and compared.
US0 - US1	Unit Select	The selected drive number encoded the same as bits 0 and 1 of the Digital Output register.

Command Format

This section contains the format of the commands that are issued to the diskette drive controller.

The following abbreviations are used in the figures on the following pages. An X is used to indicate a *don't care* condition.

MT = Multitrack
MF = MFM mode
SK = Skip deleted-data address mark
HD = Head number
USX = Unit select
SRT = Diskette stepping rate
HUT = Head unload time
HLT = Head load time
ND = Non-data mode.

Read Data Command Format

Command Phase

Figure 3-106. Read Data Command

	7	6	5	4	3	2	1	0
Byte 0	MT	MF	SK	0	0	1	1	0
Byte 1	X	X	X	X	X	HD	US1	US0
Byte 2	Cylinder Number (C)							
Byte 3	Head Address (H)							
Byte 4	Sector Number (R)							
Byte 5	Number of Data Bytes in Sector (N)							
Byte 6	End of Track (EOT)							
Byte 7	Gap Length (GPL)							
Byte 8	Data Length (DTL)							

Result Phase

Figure 3-107. Read Data Result

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0 (ST 0)							
Byte 1	Status Register 1 (ST 1)							
Byte 2	Status Register 2 (ST 2)							
Byte 3	Cylinder Number (C)							
Byte 4	Head Address (H)							
Byte 5	Sector Number (R)							
Byte 6	Number of Data Bytes in Sector (N)							

Read Deleted-Data Command Format

Command Phase

Figure 3-108. Read Deleted-Data Command

	7	6	5	4	3	2	1	0
Byte 0	MT	MF	SK	0	1	1	0	0
Byte 1	X	X	X	X	X	HD	US1	US0
Byte 2	Cylinder Number (C)							
Byte 3	Head Address (H)							
Byte 4	Sector Number (R)							
Byte 5	Number of Data Bytes in Sector (N)							
Byte 6	End of Track (EOT)							
Byte 7	Gap Length (GPL)							
Byte 8	Data Length (DTL)							

Result Phase

Figure 3-109. Read Deleted-Data Result

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0 (ST 0)							
Byte 1	Status Register 1 (ST 1)							
Byte 2	Status Register 2 (ST 2)							
Byte 3	Cylinder Number (C)							
Byte 4	Head Address (H)							
Byte 5	Sector Number (R)							
Byte 6	Number of Data Bytes in Sector (N)							

Read a Track Command Format

Command Phase

Figure 3-110. Read a Track Command

	7	6	5	4	3	2	1	0
Byte 0	0	MF	0	0	0	0	1	0
Byte 1	X	X	X	X	X	HD	US1	US0
Byte 2	Cylinder Number (C)							
Byte 3	Head Address (H)							
Byte 4	Sector Number (R)							
Byte 5	Number of Data Bytes in Sector (N)							
Byte 6	End of Track (EOT)							
Byte 7	Gap Length (GPL)							
Byte 8	Data Length (DTL)							

Result Phase

Figure 3-111. Read a Track Result

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0 (ST 0)							
Byte 1	Status Register 1 (ST 1)							
Byte 2	Status Register 2 (ST 2)							
Byte 3	Cylinder Number (C)							
Byte 4	Head Address (H)							
Byte 5	Sector Number (R)							
Byte 6	Number of Data Bytes in Sector (N)							

Read ID Command Format

Command Phase

Figure 3-112. Read ID Command

	7	6	5	4	3	2	1	0
Byte 0	0	MF	0	0	1	0	1	0
Byte 1	X	X	X	X	X	HD	US1	US0

Result Phase

Figure 3-113. Read ID Result

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0 (ST 0)							
Byte 1	Status Register 1 (ST 1)							
Byte 2	Status Register 2 (ST 2)							
Byte 3	Cylinder Number (C)							
Byte 4	Head Address (H)							
Byte 5	Sector Number (R)							
Byte 6	Number of Data Bytes in Sector (N)							

Write Data Command Format

Command Phase

Figure 3-114. Write Data Command

	7	6	5	4	3	2	1	0
Byte 0	MT	MF	0	0	0	1	0	1
Byte 1	X	X	X	X	X	HD	US1	US0
Byte 2	Cylinder Number (C)							
Byte 3	Head Address (H)							
Byte 4	Sector Number (R)							
Byte 5	Number of Data Bytes in Sector (N)							
Byte 6	End of Track (EOT)							
Byte 7	Gap Length (GPL)							
Byte 8	Data Length (DTL)							

Result Phase

Figure 3-115. Write Data Result

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0 (ST 0)							
Byte 1	Status Register 1 (ST 1)							
Byte 2	Status Register 2 (ST 2)							
Byte 3	Cylinder Number (C)							
Byte 4	Head Address (H) Bits 7 - 0							
Byte 5	Sector Number (R)							
Byte 6	Number of Data Bytes in Sector (N)							

Write Deleted-Data Command Format

Command Phase

Figure 3-116. Write Deleted-Data Command

	7	6	5	4	3	2	1	0
Byte 0	MT	MF	0	0	1	0	0	1
Byte 1	X	X	X	X	X	HD	US1	US0
Byte 2	Cylinder Number (C)							
Byte 3	Head Address (H)							
Byte 4	Sector Number (R)							
Byte 5	Number of Data Bytes in Sector (N)							
Byte 6	End of Track (EOT)							
Byte 7	Gap Length (GPL)							
Byte 8	Data Length (DTL)							

Result Phase

Figure 3-117. Write Deleted-Data Result

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0 (ST 0)							
Byte 1	Status Register 1 (ST 1)							
Byte 2	Status Register 2 (ST 2)							
Byte 3	Cylinder Number (C)							
Byte 4	Head Address (H)							
Byte 5	Sector Number (R)							
Byte 6	Number of Data Bytes in Sector (N)							

Format a Track Command Format

Command Phase

Figure 3-118. Format a Track Command

	7	6	5	4	3	2	1	0
Byte 0	0	MF	0	0	1	1	0	1
Byte 1	X	X	X	X	X	HD	US1	US0
Byte 2	Number of Data Bytes in Sector (N)							
Byte 3	Sectors per Cylinder (SC)							
Byte 4	Gap Length (GPL)							
Byte 5	Data (D)							

Result Phase

Figure 3-119. Format a Track Result

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0 (ST 0)							
Byte 1	Status Register 1 (ST 1)							
Byte 2	Status Register 2 (ST 2)							
Byte 3	Reserved							
Byte 4	Reserved							
Byte 5	Reserved							
Byte 6	Reserved							

Recalibrate Command Format

Command Phase

Figure 3-120. Recalibrate Command

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	1	1
Byte 1	X	X	X	X	X	0	US1	US0

Result Phase: This command has no result phase.

Sense Interrupt Status Command Format

Command Phase

Figure 3-121. Sense Interrupt Status Command

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	0	0	0

Result Phase

Figure 3-122. Sense Interrupt Status Result

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0 (ST 0)							
Byte 1	Present Cylinder Number (PCN)							

Specify Command Format

Command Phase

Figure 3-123. Specify Command

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	0	1	1
Byte 1	SRT	SRT	SRT	SRT	HUT	HUT	HUT	HUT
Byte 2	HLT	HLT	HLT	HLT	HLT	HLT	HLT	ND

Result Phase: This command has no result phase.

Sense Drive Status Command Format

Command Phase

Figure 3-124. Sense Drive Status Command

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	0	0
Byte 1	X	X	X	X	X	HD	US1	US0

Result Phase

Figure 3-125. Sense Drive Status Result

	7	6	5	4	3	2	1	0
Byte 0	Status Register 3 (ST 3)							

Seek Command Format

Command Phase

Figure 3-126. Seek Command

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	1	1	1
Byte 1	X	X	X	X	X	HD	US1	US0
Byte 2	New Cylinder Number for Seek (NCN)							

Result Phase: This command has no result phase.

Invalid Command Format

Result Phase: The following status byte is returned to the system microprocessor when an invalid command has been received.

Figure 3-127. Invalid Command Result

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0 (ST 0)							

Command Status Registers

This section contains definitions of status registers ST 0 through ST 3.

Status Register 0

Figure 3-128 shows the bit definitions of status register ST 0.

Figure 3-128. Status Register 0 (ST 0)

Bit	Function
7, 6	Interrupt Code (IC) 00 = Normal Termination of Command (NT) - The command was completed and properly executed. 01 = Abrupt Termination of Command (AT) - The execution of the command was started but not successfully completed. 10 = Invalid Command Issue (IC) - The issued command was never started. 11 = Reserved (Abnormal Termination)
5	Seek End (SE) - Set to 1 when the diskette drive completes the Seek command.
4	Equipment Check (EC) - Set to 1 if the -track 0 signal fails to occur after 80 step pulses (Recalibrate command).
3	Set to 0.
2	Head Address (HD) - Indicates the state of the head at interrupt.
1	Unit select 1 (US 1) - Indicates drive 1 is at interrupt.
0	Unit select 0 (US 0) - Indicates drive 0 is at interrupt.

Status Register 1

Figure 3-129 shows the bit definitions of status register ST 1.

Figure 3-129. Status Register 1 (ST 1)

Bit	Function
7	End of Cylinder (EN) - Set to 1 when the controller tries to gain access to a sector beyond the final sector of a cylinder.
6	Reserved - This bit is always set to 0.
5	Data Error (DE) - Set to 1 when the controller detects a CRC error in either the ID field or the data field.
4	Overrun (OR) - Set to 1 if the controller is not serviced by the main system within a certain time limit during data transfers.
3	Reserved - This bit is always set to 0.
2	No Data (ND) - Set to 1 if the controller cannot find the sector specified in the ID register during the execution of a Read Data or Read Deleted-Data command. This flag is also set to 1 if the controller cannot read the ID field without an error during the execution of a Read ID command or if the starting sector cannot be found during the execution of a Read a Track command.
1	Not Writable (NW) - Set to 1 if the controller detects a write-protect signal from the diskette drive during execution of a Write Data, Write Deleted-Data, or Format a Track command.
0	Missing Address Mark (MA) - Set to 1 if the controller cannot detect the ID address mark. At the same time, the MD of Status register 2 is set to 1.

Status Register 2

Figure 3-130 shows the bit definitions of status register ST 2.

Figure 3-130. Status Register 2 (ST 2)

Bit	Function
7	Reserved - This bit is always set to 0.
6	Control Mark (CM) - This flag is set to 1 if the controller encounters a sector that has a deleted-data address mark during execution of a Read Data command.
5	Data Error in Data Field (DD) - Set to 1 if the controller detects an error in the data.
4	Wrong Cylinder (WC) - This flag is related to ND (no data) bit. When the contents of C on the medium are different from that stored in the ID register, this flag is set.
3	Set to 0.
2	Set to 0.
1	Bad Cylinder (BC) - Related to ND; when the contents of C on the medium are different from that stored in the ID register, and the contents of C is hex FF, this flag is set to 1.
0	Missing Address Mark in Data Field (MD) - Set to 1 if the controller cannot find a data address mark or a deleted-data address mark when data is read from the medium.

Status Register 3

Figure 3-131 shows the bit definitions of status register ST 3.

Figure 3-131. Status Register 3 (ST 3)

Bit	Function
7	Reserved.
6	Write Protect (WP) - Status of the -write-protect signal from the diskette drive.
5	Reserved.
4	Track 0 (T0) - Status of the -track 0 signal from the diskette drive.
3	Reserved.
2	Head Address (HD) - Status of the -head 1 select signal to the diskette drive.
1, 0	Status of DS1, DS0 pins.

Signal Descriptions

The diskette drive controller interface signal sequences and timings are compatible with the industry standard 5.25-inch diskette interface. All interface signals are TTL compatible at the driver/receiver, both in the rise and fall times as well as the interface levels.

The following paragraphs describe the interface to the diskette drive.

Output Signals

All output signals to the diskette drive operate between 5V dc and ground and must meet the following specifications at the input to the drives:

- The inactive level is +2.0V dc minimum.
- The active level is +0.8V dc maximum.

The following are descriptions of the diskette drive controller output signals:

-High Density Select: Signal is active low when a drive's high density mode is selected. The polarity of this signal is consistent with 1.44MB, 3.5-inch drives. Signal is low for 2MB mode (diskettes are formatted for 1.44MB capacity). Signal is high for 1MB mode (diskettes are formatted for 720KB capacity).

On 5.25-inch drives, the drive requires a high for enabling the 1.2MB mode; a low, for the low density 360KB mode. The signal needs to be inverted when interfacing with 5.25-inch drives.

-Drive Select 0 - 1: The drive select signals enable or disable all drive interface signals except -motor enable. When a drive select signal is active, the drive is enabled. When it is inactive, all controlled inputs are ignored, and all drive outputs are disabled.

-Motor Enable 0 - 1: When this signal is activated, along with the proper drive select signals, the spindle starts to turn. There must be a 500-millisecond delay after -motor enable 0 or -motor enable 1 becomes active before a read, write, or seek operation. When inactive, this signal causes the spindle motor to decelerate and stop.

-Direction: When this signal is active, -step moves the heads toward the drive spindle. When this signal is inactive, -step moves the heads away from the drive spindle. This signal is stable for 1 microsecond before and 1 microsecond after the trailing edge of the step pulse.

Note: After a direction change, a 15-millisecond delay is required before the next step pulse.

-Step: A 1-microsecond active pulse of this signal causes the read/write heads to move one track. The state of -direction at the trailing edge of -step determines the direction of motion.

Note: Before a read or write operation, a 15-millisecond seek settle time must be allowed.

-Write Data: A 250-nanosecond (minimum) pulse of this signal causes a bit to be written if -write enable is active. Data written on the diskette will have 125-nanosecond write precompensation.

-Write Enable: When active, this signal enables the write current circuits, and -write data controls the writing of information. Motor start and head settle times must be observed before this line becomes active.

-Head 1 Select: Making this signal active selects the upper head; otherwise, the lower head is selected.

Input Signals

All inputs from the drive can sink 4.0 mA at the active (low) level and must meet the following specifications at the drive output:

- The inactive level is +3.7V dc minimum.
- The active level is +0.4V dc maximum.

Note: The controller interfaces directly with the outputs of 3.5-inch drives with tri-state, totem pole outputs. The IBM PS/1 computer 5.25-inch diskette drive unit contains buffer circuits to isolate the 5.25-inch interface from the 3.5-inch interface.

-Index: When the drive senses the index, it generates an active pulse of at least 1 millisecond on this line. This signal is gated to the interface only when the drive is selected.

-Track 0: This signal is active when the read/write head is on track 0. Track 0 is determined by a sensor, not a track counter.

The 3.5-inch drive is able to seek to track 0 under control of the system even if there is no diskette inserted at the time. This is required so the system software can determine how many drives are attached to the system.

Software selects each drive and attempts to recalibrate that drive to track 0. The track 0 signal is used to determine whether or not each drive is installed in the system.

-Write Protect: When active, this signal indicates that a diskette is write-protected.

-Read Data: Each bit detected provides a 250-nanosecond active pulse on this line for the 250,000-bit rate or a 125-nanosecond pulse for the 500,000-bit rate.

-Drive Type 1: When signal is low and drive is selected, a 1.44MB drive is assumed. If high when selected, either a 5.25-inch drive is present or no drive is installed.

-Diskette Change: This signal is active at power-on and latched inactive when a diskette is present, the drive is selected, and a step pulse occurs. This signal is activated when the diskette is removed from the drive. The presence of a diskette is determined by a media sensor.

The signal is used in detection of the drive type. If "drive type 1" signal is not active (not a 3.5-inch drive), then a 1.2MB 5.25-inch drive is assumed if the diskette change signal is active at power-on. Otherwise, a 360KB, 5.25-inch drive is assumed if Track 0 is active after a recalibration.

-Drive 2 Installed: This signal determines the presence of a second drive in the system. The signal is derived by the cable configuration which has the signal open to drive A and connected to drive B. If drive B is present, the signal is grounded. If high (wire open), BIOS assumes that no drive is present in position B. The signal is connected to the Intel 82077AA controller.

Power Sequencing

The write gate signal is turned off and kept off before power is turned on or off. The read/write heads return to track 0 when the system power is turned on.

Connector

The system board has a single 2-by-17-pin connector for the attachment of one or two diskette drives. Signals and data are transmitted to and from the drives through a 34-wire cable.

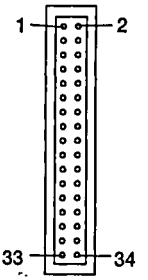


Figure 3-132 shows the voltages and signals assigned to the diskette drive connector.

Figure 3-132. Diskette Drive Controller Connector Voltage and Signal Assignments

Pin No.	I/O	Signal Name	Pin No.	I/O	Signal Name
1	I	-Drive 2 Installed	2	O	-High Density Select
3	NA	+5V dc	4	I	-Drive Type 1
5	NA	Signal Ground	6	NA	+12V dc
7	NA	Signal Ground	8	I	-Index
9	I	Reserved	10	O	-Motor Enable 1
11	NA	Signal Ground	12	O	-Drive Select 0
13	NA	Signal Ground	14	O	-Drive Select 1
15	NA	Signal Ground	16	O	-Motor Enable 0
17	NA	Signal Ground	18	O	-Direction
19	NA	Signal Ground	20	O	-Step
21	NA	Signal Ground	22	O	-Write Data
23	NA	Signal Ground	24	O	-Write Enable
25	NA	Signal Ground	26	I	-Track 0
27	NA	Signal Ground	28	I	-Write Protect
29	NA	Signal Ground	30	I	-Read Data
31	NA	Signal Ground	32	O	-Head 1 Select
33	NA	Signal Ground	34	I	-Diskette Change

Serial Port Controller

The serial port is controlled by a VL16C451A serial communications controller. The controller provides a TTL level interface which connects to a 2400 bps internal modem card or to a RS-232C interface card. It is programmable and supports asynchronous communications. The controller automatically adds and removes start, stop, and parity bits. A programmable baud-rate generator allows operation from 50 baud to 19,200 baud. The port supports 5-, 6-, 7- and 8-bit characters with 1, 1.5, or 2 stop bits. A prioritized interrupt system controls transmit, receive, error, and line status as well as data-set interrupts.

The VL16C451A controller is functionally compatible to the NS16450 controller. To programs, the VL16C451A appears to be identical to the serial portion of the IBM Personal Computer AT Serial/Parallel Adapter.

The serial port controller provides the following functions:

- Full double buffering in the character mode, eliminating the need for precise synchronization
- False-start bit detection
- Line-break generation and detection
- Modem control functions:
  - Clear to send (CTS)
  - Request to send (RTS)
  - Data set ready (DSR)
  - Data terminal ready (DTR)
  - Ring indicator (RI)
  - Data carrier detect (DCD).

Figure 3-133 on page 3-136 is a block diagram of the serial port controller.

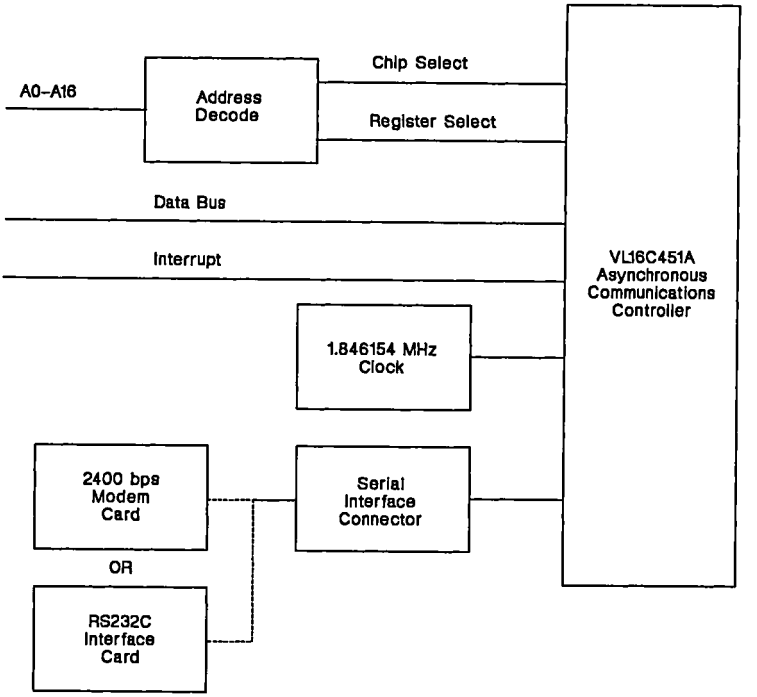


Figure 3-133. Serial Port Block Diagram

Communications Application

The serial output port is addressed as serial output port 1 (Serial 1) and interrupts as level 4 (IRQ4). To allow the controller to send interrupts to the interrupt controller, bit 3 of the Modem Control register must be set to 1. At this point, any interrupts allowed by the Interrupt Enable register will cause an interrupt.

Figure 3-134 shows the serial port data format.

Mark-ing	Start Bit	D0	D1	D2	D3	D4	D5	D6	D7	Parity Bit	Stop Bit

Figure 3-134. Serial Port, Data Format

Data bit 0 is the first bit to be sent or received. The controller automatically inserts the start bit, the correct parity bit (if programmed to do so), and the stop bits (1, 1.5, or 2, depending on the command in the Line Control register).

Programmable Baud-Rate Generator

The controller has a programmable baud-rate generator that can divide the clock input (1.846154 MHz) by any divisor from 1 to 65,535. The output frequency of the baud-rate generator is the baud rate multiplied by 16. Two 8-bit latches store the divisor in a 16-bit binary format. These divisor latches must be loaded during setup to ensure desired operation of the baud-rate generator. When either of the divisor latches is loaded, a 16-bit baud counter is immediately loaded. This procedure prevents long counts on the first load.

Registers

The controller has a number of accessible registers. The system programmer may gain access to or control any of the controller registers through the system microprocessor. These registers are used to control the controller operations and to transmit and receive data.

This section contains descriptions of the following registers:

Figure 3-135. Serial Port Register Addresses

DLAB State *	Port Address (hex)	R/W	Register
0	03F8	W	Transmitter Holding Register
0	03F8	R	Receiver Buffer Register
1	03F8	R/W	Divisor Latch, LSB
1	03F9	R/W	Divisor Latch, MSB
0	03F9	R/W	Interrupt Enable Register
X	03FA	R	Interrupt Identification Register
X	03FB	R/W	Line Control Register
X	03FC	R/W	Modem Control Register
X	03FD	R	Line Status Register
X	03FE	R	Modem Status Register
X	03FF	R/W	Scratch Register

* The DLAB state is controlled by bit 7 of the Line Control register.

Transmitter Holding Register

This register contains the character to be sent. Bit 0 is the least-significant bit and the first bit sent serially.

Receiver Buffer Register

This register contains the received character. Bit 0 is the least-significant bit and the first bit received serially.

Divisor Latch Register (LSB and MSB)

The Divisor Latch registers are used to program the baud rate generator. The values in these two registers form the divisor of the clock input (1.846154 MHz), which establishes the desired baud rate.

Figure 3-136 shows the use of the baud-rate generator with a frequency of (1.846154 MHz), For baud rates of 19,200 and below, the error obtained is minimal.

Note: In no case should the baud rate be greater than 19,200 baud with the RS-232C interface card or greater than 2,400 baud with the 2400 bps modem card.

Figure 3-136. Baud Rates at 1.846154 MHz

Desired Baud Rate	Standard Divisor Used to Generate 16x Clock (Decimal)	(Hex)	Percent of Error Difference Between Desired and Actual
50	2304	0900	0.160
75	1536	0600	0.160
110	1047	0417	0.186
134.5	857	0359	0.102
150	768	0300	0.160
300	384	0180	0.160
600	192	00C0	0.160
1200	96	0060	0.160
1800	64	0040	0.160
2000	58	003A	-0.531
2400	48	0030	0.160
3600	32	0020	0.160
4800	24	0018	0.160
7200	16	0010	0.160
9600	12	000C	0.160
19200	6	0006	0.160

Interrupt Enable Register (IER)

This 8-bit register allows the four types of controller interrupts to separately activate the chip-interrupt output signal. The interrupt system can be totally disabled by clearing bits 0 through 3 of the Interrupt Enable register. Similarly, by setting the appropriate bits of this register to 1, selected interrupts can be enabled. Disabling the interrupts inhibits the chip-interrupt output signal from the controller. All other system functions operate normally, including the setting of the Line Status and Modem Status registers.

Figure 3-137. Interrupt Enable Register (Hex 3F9)

Bit	Function
7 - 4	Reserved = 0
3	Modem Status Interrupt
2	Receiver Line Status Interrupt
1	Transmitter Holding Register Empty Interrupt
0	Received Data Available Interrupt

Bits 7 - 4 Reserved. Bits 7 through 4 are always cleared to 0.

Bit 3 When bit 3 is set to 1, the modem status interrupt is enabled.

Bit 2 When bit 2 is set to 1, the receiver line status interrupt is enabled.

Bit 1 When bit 1 is set to 1, the transmitter holding register empty interrupt is enabled.

Bit 0 When bit 0 is set to 1, the received data available interrupt is enabled.

Interrupt Identification Register

In order to minimize programming overhead during data character transfers, the controller prioritizes interrupts into four levels:

- Priority 1 - Receiver line status
- Priority 2 - Received data available
- Priority 3 - Transmitter holding register empty
- Priority 4 - Modem status.

The Interrupt Identification register stores information about a pending interrupt. When this register is addressed, the pending interrupt with the highest priority is held and no other interrupts are acknowledged until the system microprocessor services that interrupt.

Figure 3-138. Interrupt Identification Register (Hex 3FA)

Bit	Function
7 - 3	Reserved = 0
2	Interrupt ID, Bit 1
1	Interrupt ID, Bit 0
0	Interrupt Pending = 0

Bits 7 - 3 Reserved. Bits 7 through 3 are always set to 0.

Bits 2, 1 Bits 2 and 1 identify the pending interrupt with the highest priority, as shown in Figure 3-139.

Bit 0 When bit 0 is set to 1, no interrupt is pending, and polling (if used) continues. When bit 0 is set to 0, an interrupt is pending, and the contents of this register can be used as a pointer to the appropriate interrupt service routine.

Bit 0 can be used in either hard-wired, prioritized, or polled conditions to indicate that an interrupt is pending.

Bits 2 - 0 select interrupt control functions as shown in Figure 3-139.

Figure 3-139. Interrupt Control Functions

Bits 2 1 0	Priority	Type	Cause	Interrupt Reset Control
0 0 1	-	None	None	-
1 1 0	Highest	Receiver Line Status	Overrun, Parity, or Framing Error or Break Interrupt	Read the Line Status Register
1 0 0	Second	Received Data Available	Data in Receiver Buffer	Read the Receiver Buffer Register
0 1 0	Third	Transmitter Holding Register Empty	Transmitter Holding Register is Empty	Read Interrupt Identification Register or Write to Transmitter Holding Register
0 0 0	Fourth	Modem Status	Change in Signal Status from modem	Read the Modem Status Register

Line Control Register

This register programs the format of asynchronous communications.

Figure 3-140. Line Control Register (Hex 3FB)

Bit	Function
7	Divisor Latch Access Bit
6	Set Break
5	Stick Parity
4	Even Parity Select
3	Parity Enable
2	Number of Stop Bits
1	Word Length Select, Bit 1
0	Word Length Select, Bit 0

Bit 7 When bit 7 is set to 1, access is gained to the divisor latches of the baud-rate generator during a read or write operation. When bit 7 is set to 0, access is gained to the Receiver Buffer, Transmitter Holding, or Interrupt Enable registers.

Bit 6 When bit 6 is set to 1, set break is enabled, serial output is forced to the spacing state and remains there regardless of other transmitter activity. When bit 6 is set to 0, set break is disabled.

Bit 5 When bits 5 through 3 are set to 1's, the parity bit is sent and checked as a logical 0. When bits 5 and 3 are both set to 1's, and bit 4 is set to 0, the parity bit is sent and checked as a logical 1.

Bit 4 When bits 4 and 3 are set to 1's, an even number of logical 1's are transmitted and checked in the data word bits and parity bit. When bit 4 is set to 0, and bit 3 is set to 1, an odd number of logical 1's are transmitted and checked in the data word bits and parity bit.

Bit 3 When bit 3 is set to 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit. (The parity bit is used to produce an even or odd number of 1's when the data word bits and the parity bit are summed.)

Bit 2 Bits 2 through 0 specify the number of stop bits in each serial character that is sent or received as shown in Figure 3-141.

Figure 3-141. Stop Bits

Bit 2	Word Length *	Number of Stop Bits
0	N/A	1
1	5 Bits	1-1/2
1	6 Bits	2
1	7 Bits	2
1	8 Bits	2

* Word length is specified by bits 1 and 0 in this register.

Bits 1, 0 Bits 1 and 0 specify the number of bits in each serial character that is sent or received. Word length is selected as shown in Figure 3-142.

Figure 3-142. Word Length

Bits 1 0	Word Length
0 0	5 Bits
0 1	6 Bits
1 0	7 Bits
1 1	8 Bits

Modem Control Register

This register controls the data exchange with the modem, data set, or peripheral device emulating a modem.

Figure 3-143. Modem Control Register (Hex 3FC)

Bit	Function
7 - 5	Reserved = 0
4	Loop Test
3	Out 2
2	Out 1
1	Request to Send (RTS)
0	Data Terminal Ready (DTR)

Bits 7 - 5 Reserved. Bits 7 through 5 are always set to 0.

Bit 4 Bit 4 provides a loopback feature for diagnostic testing of the serial port. When bit 4 is set to 1:

- Transmitter serial output is set to the marking state.
- Receiver serial input is disconnected.
- Output of the Transmitter Shift register is *looped back* to the Receiver Shift register input.

  Note: The Transmitter and Receiver Shift registers are not accessible VL16C451 registers.

- The modem control inputs (CTS, DSR, DCD, and RI) are disconnected.
- The modem control outputs (DTR, RTS, OUT 1, and OUT 2) are internally connected to the four modem control inputs.
- The modem control output pins are forced inactive.

When the serial port is in the diagnostic mode, transmitted data is immediately received. This feature allows the system microprocessor to verify the transmit-data and receive-data paths of the serial port.

When the serial port is in the diagnostic mode, the receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but their sources are the lower 4 bits of the Modem Control register instead of the four modem control input signals. The interrupts are still controlled by the Interrupt Enable register.

Bit 3 Bit 3 controls the OUT 2 signal which is an auxiliary user-programmed interrupt enable signal. OUT 2 is used to control the interrupt signal to the channel. When bit 3 is set to 1, the interrupt is enabled. When bit 3 is set to 0, the interrupt is disabled.

Bit 2 Bit 2 controls the OUT 1 signal which is an auxiliary user-programmed output signal. When bit 2 is set to 1, OUT 1 is forced active. When bit 2 is set to 0, OUT 1 is forced inactive.

Bit 1 Bit 1 controls the RTS modem control output signal. When bit 1 is set to 1, RTS is forced active. When bit 1 is set to 0, RTS is forced inactive.

Bit 0 Bit 0 controls the DTR modem control output signal. When bit 0 is set to 1, DTR is forced active. When bit 0 is set to 0, DTR is forced inactive.

Line Status Register

This register provides the system microprocessor with status information about the data transfer.

Figure 3-144. Line Status Register (Hex 3FD)

Bit	Function
7	Reserved = 0
6	Transmitter Shift Register Empty (TSRE)
5	Transmitter Holding Register Empty (THRE)
4	Break Interrupt (BI)
3	Framing Error (FE)
2	Parity Error (PE)
1	Overrun Error (OR)
0	Data Ready (DR)

Bit 7 Reserved. Bit 7 is always set to 0.

Bit 6 Bit 6 is set to 1 when both the Transmitter Holding register and the Transmitter Shift register are empty. Bit 6 is set to 0 when either the Transmitter Holding register or the Transmitter Shift register contains a data character.

Bit 5 Bit 5 indicates that the serial port controller is ready to accept a new character for transmission. Bit 5 is set to 1 when a character is transferred from the Transmitter Holding register into the Transmitter Shift register. Bit 5 is set to 0 when the system microprocessor loads the Transmitter Holding register.

Bit 5 also causes the controller to issue an interrupt to the system microprocessor when bit 1 in the Interrupt Enable register is set to 1.

Bit 4 Bit 4 is set to 1 when the received data input is held in the spacing state for longer than a full word transmission time (that is, the total time of start bit + data bits + parity + stop bits).

Note: Bits 1 through 4 are the error conditions that produce a receiver line status interrupt whenever any of the corresponding conditions are detected.

Bit 3 Bit 3 is set to 1 when the stop bit, following the last data bit or parity bit, is at a spacing level. This indicates that the received character did not have a valid stop bit.

Bit 2 Bit 2 is set to 1 when a parity error is detected (the received character does not have the correct even or odd parity, as selected by the even-parity-select bit in the Line Control register). Bit 2 is set to 0 when the system microprocessor reads the contents of the Line Status register.

Bit 1 When bit 1 is set to 1, it indicates that data in the Receiver Buffer register was not read by the system microprocessor before the next character was transferred into the Receiver Buffer register, destroying the previous character. Bit 1 is set to 0 when the system microprocessor reads the contents of the Line Status register.

Bit 0 Bit 0 is set to 1 when a complete incoming character has been received and transferred into the Receiver Buffer register. Bit 0 is set to 0 when the system microprocessor reads the Receiver Buffer register.

Modem Status Register

This register provides the current state of the control lines from the modem (or external device) to the system microprocessor. In addition, bits 3 through 0 of this register provide change information. These 4 bits are set to 1 whenever a control input from the modem changes state. They are set to 0 whenever the system microprocessor reads this register.

Figure 3-145. Modem Status Register (Hex 3FE)

Bit	Function
7	Data Carrier Detect
6	Ring Indicate
5	Data Set Ready
4	Clear to Send
3	Delta Data Carrier Detect
2	Trailing Edge Ring Indicate
1	Delta Data Set Ready
0	Delta Clear to Send

Bit 7 Bit 7 is the inverted DTR modem control input signal. If bit 4 of the Modem Control register is set to 1, this bit is equivalent to bit 3 in the Modem Control register.

Bit 6 Bit 6 is the inverted RI modem control input signal. If bit 4 of the Modem Control register is set to 1, this bit is equivalent to bit 2 in the Modem Control register.

Bit 5 Bit 5 is the inverted DSR modem control input signal. If bit 4 of the Modem Control register is set to 1, this bit is equivalent to bit 0 in the Modem Control register.

Bit 4 Bit 4 is the inverted CTS modem control input signal. If bit 4 of the Modem Control register is set to 1, this bit is equivalent to bit 1 in the Modem Control register.

Bit 3 When bit 3 is set to 1, it indicates that DTR has changed state since the last time it was read by the system microprocessor.

Note: Whenever bit 0, 1, 2, or 3 is set to 1, a modem status interrupt is generated.

Bit 2 When bit 2 is set to 1, it indicates that RI has changed from an active condition to an inactive condition.

Bit 1 When bit 1 is set to 1, it indicates that DSR has changed state since the last time it was read by the system microprocessor.

Bit 0 When bit 0 is set to 1, it indicates that CTS has changed state since the last time it was read by the system microprocessor.

Scratch Register

This register does not control the serial port in any way. It can be used by the system microprocessor to temporarily hold data.

Serial Port Controller Programming Considerations

The serial port uses the VL16C451A serial communications controller. The VL16C451A is functionally compatible with the NS16450 and appears identical to software as the IBM Personal Computer AT serial port on the serial/parallel adapter. See "Hardware Interrupts" on page 12-6 for additional programming considerations.

The serial port must be configured as Serial 1 (COM1:) using the system configuration utilities.

Signal Descriptions

Modem Control Input Signals

The following are system board input signals from the modem or RS-232C interface card to the controller. Bits 7 through 4 in the Modem Status register indicate the condition of these signals. Bits 3 through 0 in the Modem Status register monitor these signals to indicate when the modem changes state.

Clear to Send (CTS): When active, this signal indicates that the modem is ready for the serial port to transmit data.

Data Set Ready (DSR): When active, this signal indicates that the modem or data set is ready to establish the communications link and transfer data with the controller.

Ring Indicate (RI): When active, this signal indicates that the modem or data set detected a telephone ringing signal.

Received Level Signal Detect (RLSD): When active, this signal indicates that the modem or data set detected a data carrier.

Modem Control Output Signals

The following are controller output signals. They are all set inactive upon a master reset operation. These signals are controlled by bits 3 through 0 in the Modem Control register.

Data Terminal Ready (DTR): When active, this signal informs the modem or data set that the controller is ready to communicate.

Request to Send (RTS): When active, this signal informs the modem or data set that the controller is ready to send data.

Output 1 (OUT 1): This signal is pulled high.

Output 2 (OUT 2): User-programmed output. This signal controls interrupts to the system.

System Board Voltage Interchange

The system board provides a serial interface connector with TTL level signals for connection to either a 2400 bps modem card or to a RS-232C interface card. Included for the connector are +5V dc, +12V dc, and −12V dc.

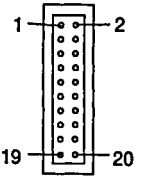


Figure 3-146. Serial Interface Connector

See Connector J2 on page 9-5 for signal definition.

Parallel Port Controller

The parallel port allows the attachment of devices that transfer 8 bits of parallel data at standard TTL levels. It has a 25-pin, D-shell connector. This port may be addressed as parallel port 1, 2, or 3.

The parallel port is compatible with previous IBM Personal Computer parallel port implementations. The primary function of the parallel port is to attach a printer with a parallel interface to the system. The parallel port has an Extended mode that allows support of bidirectional input and output. The port also supports edge-triggered interrupts and a readable interrupt-pending status. The interrupt level is common with the Audio Card.

Figure 3-147 is a block diagram of the parallel port controller.

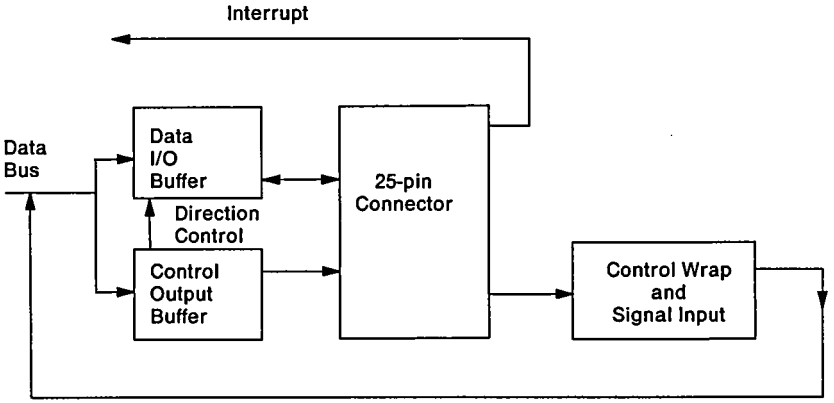


Figure 3-147. Parallel Port Controller Block Diagram

Parallel Port Programmable Option Select

The parallel port can be configured to three different address spaces previously used in IBM Personal Computer products. These addresses are selected by placing the system board in Setup; clear bit 7 of port hex 94. Perform an I/O write to port hex 0102. Bits 6 and 5 in port hex 0102 are used to select the address spaces shown in Figure 3-148.

When setup is complete, be sure to set bit 7 of port hex 94.

Figure 3-148. Parallel Port Configuration

Bit 6	Bit 5	Function
0	0	Parallel 1 LPT1:
0	1	Parallel 2 LPT2:
1	0	Parallel 3 LPT3:

The address assignments for each configuration are shown in Figure 3-149.

Figure 3-149. Parallel Port Address Assignments

Port	Data Address (hex)	Status Address (hex)	Parallel Control Address (hex)
Parallel 1	03BC	03BD	03BE
Parallel 2	0378	0379	037A
Parallel 3	0278	0279	027A

Parallel Port Extended Mode

The Extended mode option of the parallel port is selected through Programmable Option Select. With the system board in Setup, the Extended mode is selected by writing a 0 to bit 7 of I/O address hex 0102. The Extended mode makes the parallel port an 8-bit parallel and bidirectional interface. Figure 3-150 shows the possible configurations for the parallel port in the Extended mode.

Figure 3-150. Parallel Port Extended Mode Configurations

Port Mode	Port Direction	POS Mode Bit	Parallel Control Direction Bit	System Reset
Extended	Write	0	0	1
Extended	Write	0	0	0
Extended	Read	0	1	0
Compatible	Write	1	NA	0

Parallel Port Controller Programming Considerations

The following are some considerations for programming the parallel port controller.

The interface responds to five I/O instructions: two output and three input. In the Compatible mode, the output instructions transfer data into two latches whose outputs are presented on the pins of the D-shell connector. In the Extended mode, the 8-bit data latch output to the D-shell connector is controlled by bit 5 in the Parallel Control port.

In the Compatible mode, two of the three input instructions allow the processor to read back the contents of the two latches. In the Extended mode, the read-back of the 8-bit data in the Data Address is controlled by bit 5 in the Parallel Control port. The third input instruction allows the system microprocessor to read the real-time status of a group of pins on the connector.

The Extended mode can be used by externally attached equipment.

During POST, the parallel port is configured as an output port. POST status information is written to this port during the power-on initialization as well as initialization after a reset from the keyboard (Ctrl, Alt, Delete).

The following is a detailed description of each interface port instruction. For specific signal timing parameters, refer to the specifications for the equipment connected to the parallel port connector.

Data Address Port

The Data Address port is the 8-bit data port for both the Compatible and Extended modes. For the Compatible mode, a write operation to this port immediately presents data to the connector pins. A read operation from this port in the Compatible mode produces the data that was last written to it.

In the Extended mode, a write operation to this port latches the data but it is only presented to the connector pins if the direction bit was set to write in the Parallel Control port. A read operation in the Extended mode produces either:

- The data previously written if the direction bit in the Parallel Control port is set to write.

- The data on the connector pins from another device if the direction bit is set to read.

Status Port

The Status port is a read-only port in either mode. A read operation to this port presents the system microprocessor with the interrupt pending status of the interface as well as the real-time status of the connector pins as shown in Figure 3-151. An interrupt is pending when the interrupt status bit is set to 0.

Figure 3-151. Status Port

Port Bit	Port Data
7	-Busy
6	-Acknowledge (-ACK)
5	Paper End (PE)
4	Select (SLCT)
3	-Error
2	-IRQ Status
1, 0	Reserved

Bit 7 Bit 7 represents the state of the -BUSY signal. When this signal is active, the printer is busy and cannot accept data.

Bit 6 Bit 6 represents the current state of the printer -ACK signal. When bit 6 is set to 0, the printer has received a character and is ready to accept another.

Bit 5 Bit 5 represents the current state of the printer PE signal. When bit 5 is set to 1, the printer has detected the end of the paper.

Bit 4 Bit 4 represents the current state of the SLCT signal. When bit 4 is set to 1, the printer has been selected.

Bit 3 Bit 3 represents the current state of the printer -ERROR signal. When bit 3 is set to 0, the printer has encountered an error condition.

Bit 2 When bit 2 is set to 0, the printer has acknowledged the previous transfer using the -ACK signal.

Bits 1, 0 Reserved.

Parallel Control Port

The Parallel Control port is a read/write port. A write operation to this port latches the 6 least-significant data bits of the bus. The sixth bit corresponds to the direction control bit and is only applicable in the Extended mode. The remaining 5 bits are compatible with previous implementations as shown in Figure 3-152. A read operation to the Parallel Control port sends the system microprocessor the data that was last written to it, with the exception of the write-only direction bit.

Figure 3-152. Parallel Control Port

Port Bit	Port Data
7, 6	Reserved
5	Direction
4	IRQ EN
3	Pin 17 (SLCT IN)
2	Pin 16 (-INIT)
1	Pin 14 (AUTO FD XT)
0	Pin 1 (STROBE)

Bits 7, 6 Reserved.

Bit 5 Bit 5 controls the direction of the data port. For more information on the use of this bit, see Figure 3-150 on page 3-150. This is a write-only bit.

Bit 4 When bit 4 is set to 1, an interrupt occurs when the -ACK signal changes from active to inactive. This bit enables the parallel port interrupt.

Bit 3 Bit 3 controls the SLCT IN signal. When bit 3 is set to 1, the printer is selected.

Bit 2 Bit 2 controls the -INIT printer signal. When bit 2 is set to 0, the printer starts.

Bit 1 Bit 1 controls the AUTO FD XT signal. When bit 1 is set to 1, the printer will automatically line feed after each line is printed.

Bit 0 Bit 0 controls the STROBE signal to the printer. When bit 0 is set to 1, data is clocked into the printer.

Parallel Port Timing

The timing for the parallel port depends on the timing of the devices connected to the port. Figure 3-153 shows the sequence for typical parallel port signal timing.

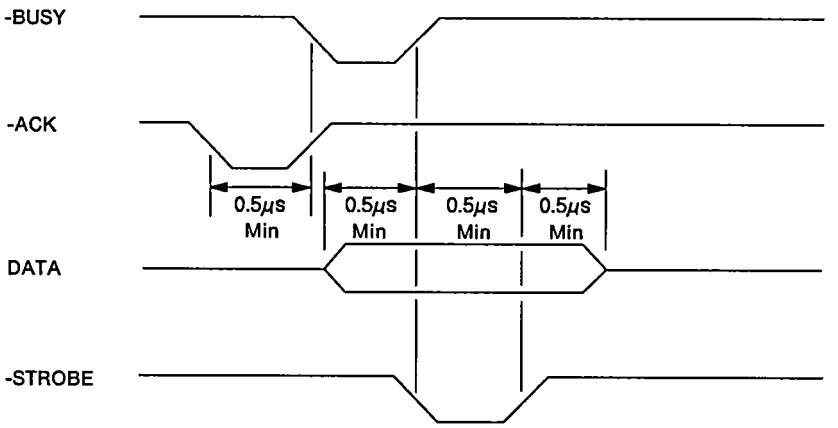


Figure 3-153. Parallel Port Timing Sequence

Signal Descriptions

Figure 3-154 and Figure 3-155 list characteristics of the data, interrupt, and control signals.

Figure 3-154. Data and Interrupt Signals		
Sink Current	12 mA	Maximum
Source Current	2 mA	Maximum
High-level Output Voltage	2.4V dc	Minimum
Low-level Output Voltage	0.5V dc	Maximum

Pins 1, 14, 16, and 17 are driven by open collector drivers pulled to 5 V dc through 4.7 K ohm resistors.

Figure 3-155. Control Signals		
Sink Current	10 mA	Maximum
Source Current	0.2 mA	Maximum
High-level Output Voltage	5.0V dc minus pullup	Minimum
Low-level Output Voltage	0.5V dc	Maximum

Connector

The parallel port connector is a standard 25-pin D-shell connector. The D0 - D7 lines on the connector are driven by drivers capable of sourcing 2 mA and sinking 12 mA.

Figure 3-156 show the voltages and signals assigned to the parallel port connector.

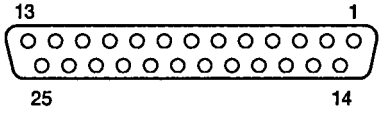


Figure 3-156. Parallel Port Connector Signal and Voltage Assignments

Pin No.	I/O	Signal Name	Pin No.	I/O	Signal Name
1	I/O	-STROBE	14	O	-AUTO FD XT
2	I/O	Data Bit 0	15	I	-ERROR
3	I/O	Data Bit 1	16	O	-INIT
4	I/O	Data Bit 2	17	O	-SLCT IN
5	I/O	Data Bit 3	18	NA	Ground
6	I/O	Data Bit 4	19	NA	Ground
7	I/O	Data Bit 5	20	NA	Ground
8	I/O	Data Bit 6	21	NA	Ground
9	I/O	Data Bit 7	22	NA	Ground
10	I	-ACK	23	NA	Ground
11	I	BUSY	24	NA	Ground
12	I	PE	25	NA	Ground
13	I	SLCT			

Memory

The system has the following types of memory:

- Read-Only Memory (ROM)
- Random Access Memory (RAM)
- Complementary Metal Oxide Semiconductor RAM (CMOS RAM).

Read-Only Memory (ROM)

The system board ROM subsystem consists of either two 128K-by-8-bit modules or four 128K-by-8-bit modules arranged in 16 bit words. 512KB of ROM are addressed from F80000 to FFFFFF. Addresses FE0000 to FFFFFF are also addressed as 0E0000 to 0FFFFF.

Random Access Memory (RAM)

The system board RAM starts at address hex 000000 of the 16MB address space. 512KB of RAM are soldered on the system board. An additional 512KB may be added by installing a memory card into connector on the system board. The RAM operates with one wait state. The system board memory is not parity checked. Memory-refresh requests occur once every 15 microseconds.

RAM can be disabled in 128KB blocks, from 0KB to 640KB (five blocks). If I/O memory exists in any block, the RAM will be automatically disabled by the POST.

The 512KB memory card connects to a 2-by-20 card edge connector on the system board.

Figure 3-157 shows the pin definitions for the RAM module connectors.

Figure 3-157. Memory Option Connector Pin Assignments

Pin	I/O	Signal	Pin	I/O	Signal
1	I/O	Data Bit 0	2	I/O	Data Bit 1
3	I/O	Data Bit 2	4	I/O	Data Bit 3
5	N/A	Ground	6	I/O	Data Bit 4
7	I/O	Data Bit 5	8	I/O	Data Bit 6
9	I/O	Data Bit 7	10	N/A	Ground
11	I/O	Data Bit 8	12	I/O	Data Bit 9
13	I/O	Data Bit 10	14	I/O	Data Bit 11
15	N/A	Ground	16	I/O	Data Bit 12
17	I/O	Data Bit 13	18	I/O	Data Bit 14
19	I/O	Data Bit 15	20	N/A	Ground
21	N/A	+5V dc	22	I	-Second Bank
23	I	1Mb Chip Detect	24	O	-Row Address Strobe 1
25	O	-Row Address Strobe 0	26	O	-Write Strobe
27	O	-Column Address Strobe High	28	O	-Column Address Strobe Low
29	N/A	Ground	30	O	Address Bit 9
31	O	Address Bit 8	32	O	Address Bit 7
33	O	Address Bit 6	34	O	Address Bit 5
35	N/A	Ground	36	O	Address Bit 4
37	O	Address Bit 3	38	O	Address Bit 2
39	O	Address Bit 1	40	O	Address Bit 0

Figure 3-158 shows the mapping for the memory locations on the system board.

Figure 3-158. System Board Memory Map

Hex Range	Function
000000 to 09FFFF	640KB System Board RAM *
0A0000 to 0BFFFF	Video RAM
0C0000 to 0DFFFF	128KB I/O Expansion Adapters
0E0000 to 0FFFFF	128KB System Board ROM (also mapped in hex FE0000 to FFFFFF)
100000 to 15FFFF	384KB System Board RAM with 512KB RAM option
160000 to F7FFFF	I/O Channel Expansion Memory Addresses
F80000 to FFFFFF	512KB System Board ROM

* A 256-byte portion of this RAM is reserved as a BIOS data area. A 1K portion of this RAM is reserved as an extended BIOS data area. See *BIOS Interface Technical Reference for IBM PS/1™ Computer* for details.

Note: With the system board in setup, the system board memory can be disabled by writing port address hex 104 as shown in the following figure.

Figure 3-159. System Board Memory Enable

Bits	Function	Hex Range
7 - 5	Reserved	
4	Enable Fifth 128KB Bank	080000 - 09FFFF
3	Enable Fourth 128KB Bank	060000 - 07FFFF
2	Enable Third 128KB Bank	040000 - 05FFFF
1	Enable Second 128KB Bank	020000 - 03FFFF
0	Enable First 128KB Bank	000000 - 01FFFF

Complementary Metal Oxide Semiconductor RAM

The real-time clock and 64 bytes of nonvolatile RAM are contained on the real-time clock/complementary metal oxide semiconductor (RTC/CMOS) RAM chip. The internal clock circuitry uses 14 bytes of this memory, and the rest is allocated to configuration and system status information.

Figure 3-160 shows the RTC/CMOS RAM bytes and their addresses.

Figure 3-160. RTC/CMOS RAM Address Map

Address (hex)	Function
000 - 00D	Real-Time Clock Information
00E	Diagnostic Status Byte
00F	Shut Down Status Byte
010	Diskette Drive Byte
011	Fixed Disk Type Byte
012 - 014	Reserved
015 - 016	Low and High Base Memory Bytes
017 - 018	Low and High Memory Expansion Bytes
019 - 031	Reserved
032 - 033	Configuration CRC Bytes
034 - 036	Reserved
037	Date Century Byte
038 - 03F	Reserved

RTC/CMOS RAM I/O Operations

When performing I/O operations to the RTC/CMOS RAM addresses (see Figure 3-160 on page 3-158 and the following pages), interrupts should be inhibited to avoid having interrupt routines change the CMOS address register before data is read or written. Port hex 0070 should be left to point to status register D of the RTC/CMOS.

I/O operations to the RTC/CMOS RAM addresses require the following sequence:

1. OUT to port hex 0070 with the RTC/CMOS address to be written.

   Note: The NMI mask bit resides in port hex 0070. (See "Non-Maskable Interrupt" on page 2-28.)

2. JMP $+2 for I/O delay.
3. OUT to port hex 0071 with the data to be written.

Reading the RTC/CMOS RAM requires the following sequence:

1. OUT to port hex 0070 with the CMOS address to be read.
2. IN from port hex 0071, and the data read is returned in the AL register.

Warning: When writing port hex 0070, a read or write to port hex 0071 must be accessed immediately. Failure to do this can cause intermittent failures and unreliable operation of the RTC/CMOS RAM.

Real-Time Clock

Figure 3-161 shows bit definitions for the real-time clock bytes (addresses hex 000 - 00D).

Figure 3-161. Real-Time Clock (Addresses Hex 000 - 00D)

Address (hex)	Function	Byte Number
000	Seconds	0
001	Second Alarm	1
002	Minutes	2
003	Minute Alarm	3
004	Hours	4
005	Hour Alarm	5
006	Day Of Week	6
007	Date Of Month	7
008	Month	8
009	Year	9
00A	Status Register A	10
00B	Status Register B	11
00C	Status Register C	12
00D	Status Register D	13

Note: INT hex 1A is the BIOS call to read and set the time and date. It initializes registers A, B, C, and D.

Status Register A

Bit 7 Update in Progress (UIP)— When bit 7 is set to 1, it indicates that the time update cycle is in progress. When bit 7 is set to 0, it indicates that the current date and time are available to read. Reading the date or time when this bit is set to 1 may result in incorrect values.

Bits 6 - 4 22-Stage Divider (DV2 through DV0)— These three divider-selection bits identify which time-base frequency is being used. The system initializes the stage divider to 010, which selects a 32.768 KHz time base. This is the only stage divider supported by the system microprocessor for proper timekeeping.

Bits 3 - 0 Rate Selection Bits (RS3 through RS0)— These bits allow the selection of a divider output frequency. The system initializes the rate selection bits to 0110, which selects a 1.024 KHz square-wave output frequency and a 976.562 microsecond periodic interrupt rate.

Status Register B

Bit 7 Set— When bit 7 is set to 1, any update cycle in progress is aborted and the program can initialize the 14 time-bytes without any further updates occurring until a 0 is written to this bit. When bit 7 is set to 0, the cycle is updated normally by advancing the counts at one per second.

Bit 6 Periodic Interrupt Enable (PIE)— When bit 6 is set to 1, it enables the interrupt to occur at a rate specified by the rate and divider bits in register A. When bit 6 is set to 0, the interrupt is disabled. Bit 6 is a read/write bit that the system initializes to a 0.

Bit 5 Alarm Interrupt Enable (AIE)— When bit 5 is set to 1, the alarm interrupt is enabled. When bit 5 is set to 0, the alarm interrupt is disabled. The system initializes this bit to 0.

Bit 4 Update-Ended Interrupt Enabled (UIE)— When bit 4 is set to 1, the update-ended interrupt is enabled. When bit 4 is set to 0, the update-ended interrupt is disabled. The system initializes this bit to 0.

Bit 3 Square Wave Enabled (SQWE)— When bit 3 is set to 1, the square-wave frequency, as set by the rate selection bits in Status register A, is enabled. When bit 3 is set to 0, square wave is disabled. The system initializes this bit to 0.

Bit 2 Date Mode (DM)— When bit 2 is set to 1, the time and date are updated using a binary format. When bit 2 is set to 0, the time and date are updated using a binary-coded-decimal (BCD) format. The system initializes this bit to 0.

Bit 1 24/12— When bit 1 is set to 1, the hours byte is in 24-hour mode. When bit 1 is set to 0, the hours byte is in 12-hour mode. The system initializes this bit to 1.

Bit 0 Daylight Savings Enabled (DSE)— When bit 0 is set to 1, daylight savings time is enabled. When bit 0 is set to 0, daylight savings time is disabled (reverts to standard time). The system initializes this bit to 0.

Status Register C

Bits 7 - 4 IRQF, PF, AF, UF— These read-only flag bits are affected when the PIE, AIE, and UIE interrupts (bits 6 - 4) are enabled with Status Register B.

Bits 3 - 0 Reserved.

Status Register D

Bit 7 Valid RAM Bit (VRB)— This bit is read-only and indicates the condition of the contents of the CMOS RAM through the power sense pin. A low state of the power sense pin indicates the real-time clock has lost its power. When bit 7 is set to 1, there is power on the real-time clock. When bit 7 is set to 0, the real-time clock has lost power.

Bits 6 - 0 Reserved.

CMOS RAM Configuration

The following shows the bit definitions for the CMOS configuration bytes (addresses hex 00E - 03F).

Diagnostic Status Byte (Hex 00E)

Bit 7 Real-Time Clock Power— When bit 7 is set to 1, the real-time clock chip has lost power. When bit 7 is set to 0, the real-time clock chip has not lost power.

Bit 6 Configuration Record and Checksum Status— When bit 6 is set to 1, the checksum is incorrect. When bit 6 is set to 0, the checksum is correct. The checksum is used to verify the bytes from hex 10 to hex 33.

Bit 5 Incorrect Configuration— This is a check, at power-on time, of the equipment byte of the configuration record. When bit 5 is set to 1, the configuration information is incorrect. Power-on checks require at least one diskette drive installed (bit 0 of the equipment byte set to 1). When bit 5 is set to 0, the configuration information is correct.

Bit 4 Memory Size Miscompare— When bit 4 is set to 1, the power-on check determines that the memory size is different from the memory size in the configuration record. When bit 4 is set to 0, the memory size is the same.

Bit 3 Reserved

Bit 2 Time Status Indicator (POST validity check)— When bit 2 is set to 1, the time is invalid. When bit 2 is set to 0, the time is valid.

Bit 1 Reserved.

Bit 0 Reserved.

Shut Down Status Byte (Hex 00F)

The bits in this byte are defined by the power-on diagnostics.

Diskette Drive Type Byte (Hex 010)

Bits 7 - 4 Type of first diskette drive:

0000 = No drive present
0001 = Reserved
0010 = Reserved
0011 = Reserved
0100 = High-density diskette drive (1.44MB).

Note: 0101 through 1111 are reserved.

Bits 3 - 0 Type of second diskette drive installed:

0000 = No drive present
0001 = 360KB 5.25-inch diskette drive
0010 = 1.2MB 5.25-inch diskette drive
0011 = Reserved
0100 = High-density diskette drive (1.44MB).

Note: 0101 through 1111 are reserved.

Fixed Disk Type Byte (Hex 011)

This byte defines the type of fixed disk drive (drive C) installed. Hex 00 indicates a fixed disk drive is not present.

Reserved (Hex 012 to 014)

Base Memory Bytes (Hex 015 and 016)

These bytes define the amount of memory installed below the 640KB address space.

The hex value from these bytes represents the number of 1KB blocks of base memory. For example, hex 0280 is equal to 640KB. Byte hex 015 is the least-significant byte of the base memory size. Byte hex 016 is the most-significant byte of the base memory size.

Memory Expansion Bytes (Hex 017 and 018)

These bytes define the amount of memory installed above the 1MB address space.

The hex value from these bytes represents the number of 1KB blocks of expansion memory. For example, hex 0800 is equal to 2048KB. Byte hex 017 is the least-significant byte of the expansion memory size. Byte hex 018 is the most-significant byte of the expansion memory size.

Reserved (Hex 019 through 031)

Configuration CRC Bytes (Hex 032 and 033)

These bytes contain the cyclic-redundancy-check (CRC) data for bytes hex 010 through hex 031 of the 64-byte CMOS. Byte hex 032 is the most-significant byte of the configuration CRC. Byte hex 033 is the least-significant byte of the configuration CRC.

Reserved (Hex 034 through 036)

Date Century Byte (Hex 037)

This byte contains the BCD value for the century (BIOS interface to read and set).

Reserved (Hex 038 through 03F)

Miscellaneous System Ports

Ports hex 0061, 0070, and 0092 contain information that is used for system control.

System Control Port B (Hex 0061)

Port B is accessed by I/O read or write operations to I/O address hex 0061. Figure 3-162 shows the bit definitions.

Figure 3-162. System Control Port B, Write Operations

Bit	Function
7 - 4	Reserved
3	-Enable Channel Check
2	-Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-163. System Control Port B, Read Operations

Bit	Function
7	Parity Check
6	Channel Check
5	Timer 2 Output
4	Toggles with each Refresh Request
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Bit 7 When bit 7 is set to 1, a parity check has occurred on a read operation.

Note: System board RAM does not support parity.

Bit 6 When bit 6 is set to 1, a channel check has occurred on a read operation.

Bit 5 Bit 5 returns the condition of timer/counter 2 output signal on a read operation.

Bit 4 Bit 4 toggles for each refresh request on a read operation.

Bit 3 When bit 3 is set to 0, channel check is enabled on a write. The result of the last write operation to this bit is returned on a read operation. The system initializes this bit to 1 during a power-on reset.

Bit 2 When bit 2 is set to 0, parity check is enabled on a write. The result of the last write operation to this bit is returned on a read operation. The system initializes this bit to 1 during a power-on reset.

Note: System board RAM does not support parity.

Bit 1 When bit 1 is set to 1, speaker data is enabled on a write. The result of the last write operation to this bit is returned on a read operation. The system initializes this bit to 0 during a power-on reset.

Bit 0 When bit 0 is set to 1, timer 2 gate is enabled on a write. The result of the last write operation to this bit is returned on a read operation. When bit 0 is set to 0, the gate is disabled on a write.

RTC/CMOS and NMI Mask (Hex 0070)

Figure 3-164. RTC/CMOS and NMI Mask

Bit	Function
7	Non-maskable Interrupt (NMI)
6	Reserved
5 - 0	RTC/CMOS RAM

Bit 7 When bit 7 is cleared to 0, NMI is enabled. When bit 7 is set to 1, NMI is masked off. This bit is set to 1 during a power-on reset. This bit is write-only. See "Interrupts" on page 2-28 for more information about the NMI.

Bit 6 Reserved.

Bits 5 - 0 See "RTC/CMOS RAM I/O Operations" on page 3-159.

Note: Port hex 0071 is used with port hex 0070 to read and write to the CMOS RAM and the NMI Mask register.

System Control Port A (Hex 0092)

Port hex 0092 supports alternate system microprocessor reset, PASS A20, and CMOS security lock. Figure 3-165 shows the bit definitions for port hex 0092.

Figure 3-165. System Control Port A

Bit	Function
7 - 4	Reserved
3	Security Lock Latch
2	Reserved = 0
1	Alternate Gate A20
0	Reserved

Bits 7 - 4 Reserved.

Bit 3 When bit 3 is set to 1, the 8-byte password is electrically locked in the secured area of CMOS. This read/write bit is set by POST, and it can only be cleared by turning the system power off and then turning the power on.

Note: System board and POST do not support password.

Bit 2 Reserved.

Bit 1 When bit 1 is set to 1, the A20 address bit is active when the microprocessor is in Real Address mode. When bit 1 is set to 0, A20 is inactive in Real Address mode. This read/write bit is set to 0 during a system reset.

Bit 0 Reserved.