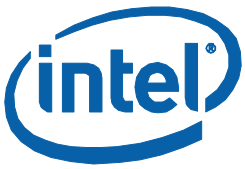


CPU Monitoring With DTS/PECI

White Paper
Michael Berktold
Thermal/Mechanical Engineer
Tian Tian
Technical Marketing Engineer
Intel Corporation

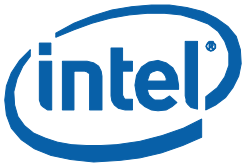
September 2010

322683

Executive Summary

This document describes various methodologies to access processor temperature data reported by the on-die DTS (Digital Temperature Sensor). It also discusses PECI (Platform Environmental Control Interface) and its role in CPU thermal management. Another focus is the 45 nm processor as the DTS and PECI technology is refined every generation.

This document provides a detailed guidance on DTS and PECI usage. Two of the latest Intel® architecture processors families are used as examples, the Intel® Xeon® Processor 5200 and 5500 Series. The document explains DTS capabilities and describes how to correctly interpret the results. Several third party software such as Real Temp* and Core Temp* are evaluated and the accuracy of the test results is discussed. The article describes the methodology of using direct MSR access for CPU thermal status and it also touches on the usage of PECI.



Contents

Introduction

Digital Thermal Sensors (DTS) have been introduced to Intel® architecture CPU families since Intel® Pentium® M processors. The data reported in DTS reflects the delta between the current temperature and the maximum junction temperature of the die (Tj). The data can be obtained by Model Specific Register (MSR) access or Platform Environment Control Interface (PECI) and used by the system for fan speed control or used by customers to develop advanced power management and thermal control schemes.

PECI is the bridge between applications and CPUs to get to DTS and other information. There is a variety of information available on PECI in multiple documents such as CPU datasheets and BIOS specifications. This document was created to help users obtain a complete and consistent picture of how to take advantage of PECI to monitor the processor temperature. Other PECI information will not be discussed in this document.

There are quite a few third-party software utilities available for both Windows and Linux operating systems to read the DTS. However the developers for these tools do not have visibilities on certain information of DTS and they have to make some assumptions. Users of these tools need to be aware of the limitations of these tools.

Thermal Mechanisms Overview

Two of the newer generations of Intel® architecture CPUs: Intel® Xeon® Processor 5200 and 5500 Series are used as examples in this document. Both processor families support TM1 (Thermal Monitor 1), TM2 (Thermal Monitor 2), per-core DTS as well as sideband access to CPU thermal data via the PECI.

Hardware Thermal Mechanisms

Intel® architecture CPUs provide the capability of shutdown when processor core temperature rises above a factory-set limit. THERMTRIP# will be asserted to indicate the processor junction temperature has reached a point beyond which permanent silicon damage may occur. The response to THERMTRIP# is that the processor will shut off its internal clocks to reduce the processor junction temperature. Then core voltage VCC will be removed. THERMTRIP# remains asserted only until PWRGOOD is de-asserted.

Two automatic thermal monitoring mechanisms (TM1 and TM2) can force the processor to reduce its power consumption. TM1, introduced with Intel® Pentium® 4, controls the processor core temperature by modulating the duty cycle of processor clock. TM1 is enabled by setting IA32_MISC_ENABLE bit 3. Software does not have native access to the native thermal condition of the processor. It cannot alter the trigger conditions. TM1 is factory calibrated to trip when the core temperature crosses a certain level.

TM2 is an additional thermal protection mechanism, was introduced with Intel® Pentium® M. TM2 controls temperature by reducing the operating frequency and voltage of the processor. After the second temperature sensor has been tripped, the thermal monitor (TM1/TM2) will remain engaged for a minimum time period (on the order of 1 ms). The thermal monitor will remain engaged until the processor core temperature drops below the preset trip temperature of the temperature sensor. While the processor is in a stop-clock state, interrupts will be blocked from interrupting the processor. This holding off of interrupts increases the interrupt latency, but does not cause interrupts to be lost. Outstanding interrupts remain pending until clock modulation is complete.

Intel® Xeon® 5500 processors also introduce Turbo Mode (may not be available for some SKUs) that can opportunistically increase processor performance using the available thermal and power headroom. This operation is transparent to most application software. BIOS and OS can disengage it when it requires more predicable processor operations.

Software Capabilities

Software can take advantages of thermal headroom to opportunistically increase performance. On the other hand, applications that are more concerned about power consumption can use thermal information to implement intelligent power management schemes to reduce consumption.

BIOS can enable or disable TM1 and TM2, although the recommendation is to enable both TM1 and TM2. TM1 is enabled by BIOS setting bit 3 of IA32_MISC_ENABLE. OS and application software must not disable operation of these mechanisms. TM2 is enabled by BIOS setting bit 13 of IA32_MISC_ENABLE.

The thermal monitor can be programmed to generate an interrupt to the processor when the thermal sensor is tripped. The delivery mode, mask and vector for this interrupt can be programmed through the thermal entry in the local APIC's LVT (Local Vector Table). The low-temperature interrupt enable and high temperature interrupt enable flags in the IA32_THERM_INTERRUPT MSR control when the interrupt is generated; that is, on a transition from a temperature below the trip point to above and/or vice-versa.

Software access to DTS reading is achieved by MSR access. Users can use PECI to read out temperature. Software also has capability to adjust CPU P state and T state to change power/performance position. Discussions on P/T state control is covered in a separate document that is coming out soon.

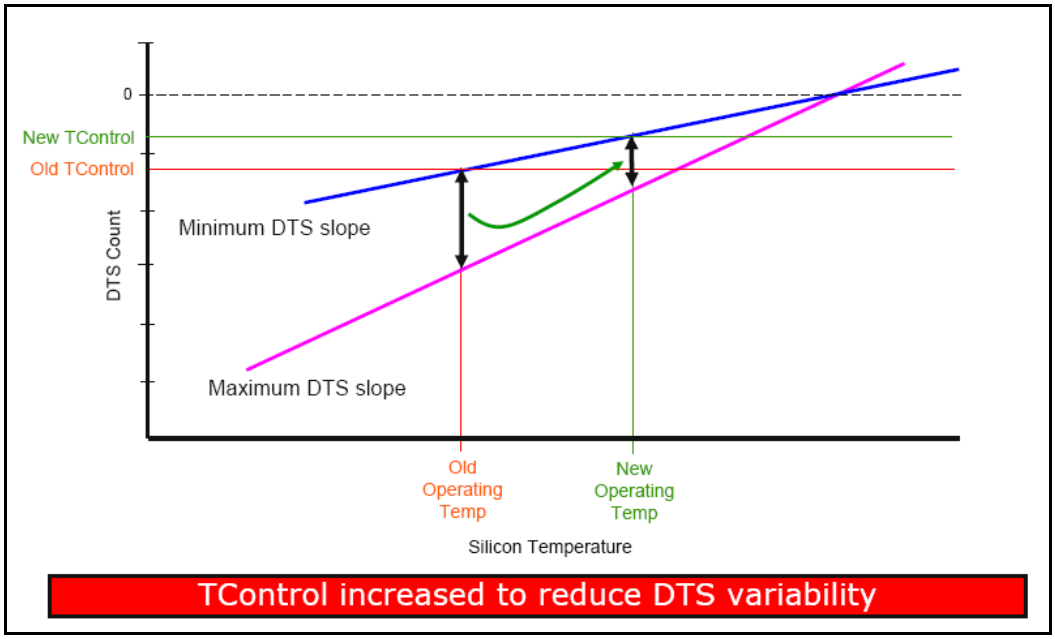
DTS Accuracy and Range

The DTS accuracy and range varies from generation to generation. It is important to understand the limits of each generation when using the DTS or PECI. The important thing to note is that PECI is accurate enough for fan speed control and Thermal Control Circuit (TCC) activation warning.

DTS in Intel® Xeon® 5200 and 5400 Processor Series

The characteristics of the Digital Thermal Sensor (DTS) vary from die to die and each processor DTS is factory calibrated. As a result, given the same $T_{CONTROL}$ setting, not all processors will be at the same silicon temperature when at $T_{CONTROL}$. Acoustic performance will vary from part to part as a result of this DTS variability. This variability also impacts the number of DTS values that could be reported below $T_{CONTROL}$. Because of the magnitude of the variation the $T_{CONTROL}$ value was increased. Increasing $T_{CONTROL}$ reduces the range of DTS variability and results in better acoustics. The DTS value is referred to as a DTS Count since one count does not necessarily equal one degree.

Figure 1. $T_{CONTROL}$ Increased to Reduce DTS Variability



When the DTS reaches its minimum reportable temperature, the value reported via the PECI bus stops decreasing. At this point, DTS readings will remain fixed until the temperature increases above the minimum reportable limit. For Intel® Xeon® 5200 and 5400 Processor Series, Intel guarantees the minimum reportable limit to be at least 10 DTS counts below $T_{CONTROL}$.

DTS in Intel® Xeon® 5500

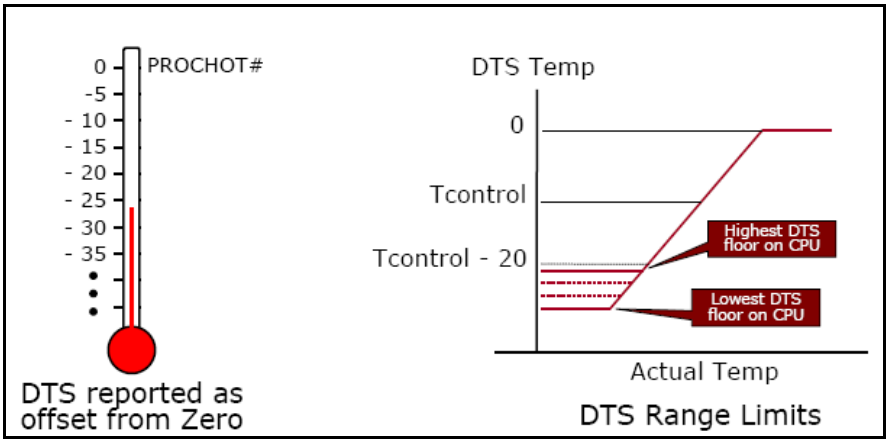
Intel® Xeon® 5500 Processor Series are very similar to previous generations. A few minor updates were made for this series.

The DTS converts an analog signal into a digital value and reports temperatures as a relative offset to zero. When the DTS reads zero, PROCHOT# is activated and the processor begins to throttle. Data is stored in an internal register and PECI averaging register. Internal registers are software visible and PECI is bi-directional single pin interface to processor registers.

There are multiple DTS sensors per processor die. Software only has access to the core temperature registers. PECI monitors all sensors and reports the highest temperature. Dual die quad-core processors have two PECI domains so fan speed control must use the PECI to access DTS on both die and the hottest die is used to determine fan speed. A monolithic quad-core processor has only one PECI domain.

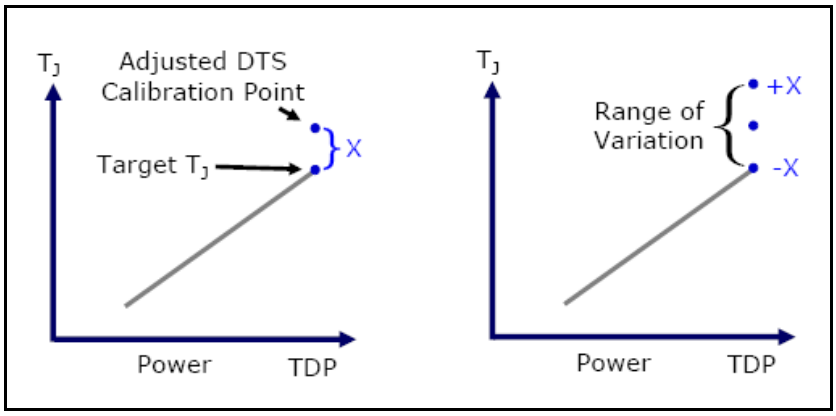
The DTS circuit is designed to read over a reasonable operating range but it may 'bottom out' when temperatures are ~20 C below $T_{CONTROL}$ (depends on characteristics of each DTS).

Figure 2. DTS Range Limits



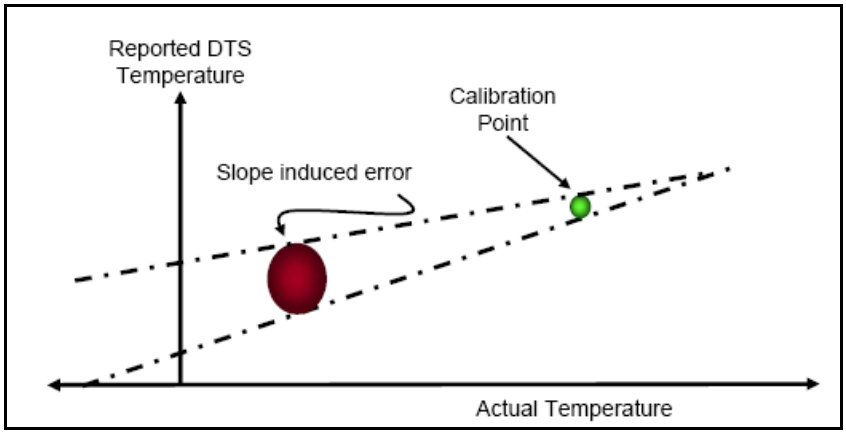
Each DTS is individually calibrated but normal factory variation influences the accuracy and PROCHOT# trip temperature will vary from part to part. The DTS calibration point is adjusted higher than target $T_{JUNCTION}$ to minimize the potential for PROCHOT# activation below $T_{CASEMAX}$. Since all the adjustment and variation is pushed to the high side the DTS is not a good tool to estimate T_{CASE}.

Figure 3. DTS Calibration and Variation



The DTS may also have some slope error which means 1°C may not be equal to one DTS count. This slope error overshadows calibration error at low temperatures which is another reason why the DTS is not a good tool to estimate T_{CASE}. At higher temperatures the accuracy is good enough for fan speed control and to detect a thermal solution failure at PROCHOT#.

Figure 4. DTS Slope Error



The Intel® Xeon® 5500 processor generation has improved the DTS circuit to expand the temperature range, improve calibration accuracy and reduce slope error.

PECI Overview

The Platform Environmental Control Interface (PECI) is an Intel® proprietary interface that provides a communication channel between Intel® processors and chipset components to external thermal monitoring devices. The Intel® Xeon® 5500 processor contains a Digital Thermal Sensor (DTS) that reports a relative die temperature as an offset from Thermal Control Circuit (TCC) activation temperature. Temperature sensors located throughout the die are implemented as analog-to-digital converters calibrated at the factory. PECI provides an interface for external devices to read processor temperature, perform processor manageability functions, and manage processor interface tuning and diagnostics. Generic PECI specification details can be found in *RS – Platform Environment Control Interface (PECI) Specification*.

The EMTS and datasheets document more specifics on PECI Client Capabilities, Client Command Suites, Multi-Domain Commands, Client Responses, Originator Responses, Temperature Data, and Client Management.

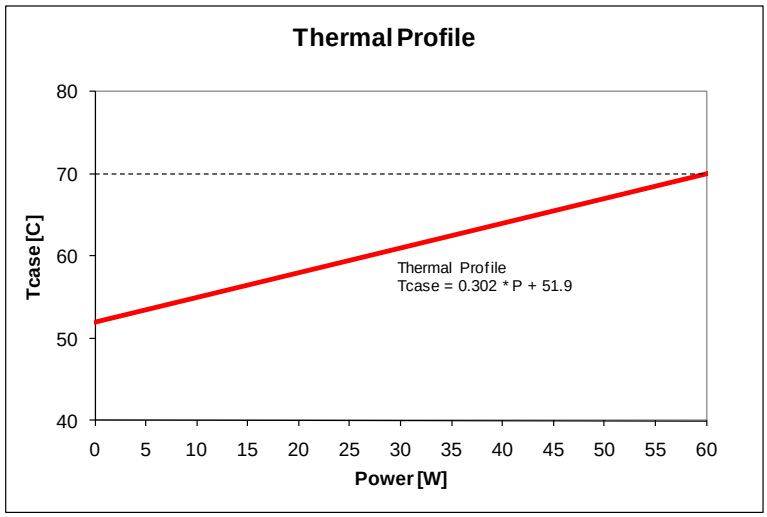
Note: Contact your Intel field representative for access to the Platform Environment Control Interface Specification or the Intel® Xeon® 5500 processor EMTS.

PECI Overview

Thermal solutions should be designed to meet the thermal specification which for Desktop and Server processors is a Thermal Profile. After a solution has been designed, the fan speed can be controlled through the PECI in actual use.

Thermal profiles can look like Figure 5:

Figure 5. Sample Thermal Profile



At low temperatures, PECI will read a large gap to PROCHOT#. As the processor heats up the gap will decrease until $T_{CONTROL}$ is reached. $T_{CONTROL}$ is fused into each processor and can be read at any time. When the processor is cooler than $T_{CONTROL}$, the fan speed can be reduced to help acoustics and save power. Once $T_{CONTROL}$ is reached, the system fans should be running at their full design speed. As the temperature increases past $T_{CONTROL}$ because of rising ambient temperatures or increase processor power the PECI value will approach zero. At a PECI value of zero the processor will reach PROCHOT# and the processor will gradually throttle back its power to keep its temperature below PROCHOT#. If a catastrophic system fan failure or run away local ambient temperature continues to push the processor temperature well beyond PROCHOT# even at its reduced power levels it will eventually reach THERMTRIP# and shut down.

Differences Between PECI 1.0 and PECI 2.0

There are no changes to electrical or timing definitions between PECI 1.0 and 2.0. PECI 2.0 is fully backwards compatible with existing PECI 1.1 hosts and associated firmware. Key differences are captured in Table 1:

Table 1. Differences Between PECI 1.0 and PECI 2.0

Categories	PECI 1.1	PECI 2.0
BIOS	BIOS discovery of client required, including #Domains	No BIOS discovery required
C-States	Unavailable during some deeper C-states	Available under all C-states and S0/S1
DTS	Instantaneous DTS temperature readings	Thermal Smoothing capabilities (Fractional data reported along with averaged samples, down to 1/64°C)
Capabilities	Capabilities limited to Ping() and GetTemp()	Interface to RAS data, DRAM throttling and IBIST controls Completion codes used for host response management 'Assured Write' capability for write data protection
MISC		No software or sideband initialization required

NOTES: All Intel® Xeon® 5200 and 5400 Processor Series support PECI.

PECI Vendors

The PECI specification is required only if the customer or vendor will be designing PECI device hardware or firmware. This requires special licensing which Intel can help with if needed by your customer.

Contact your Intel field representative to gain access to the EMTS, which should suffice for PECI system development. For PECI 2.0, here is the current list of third-party vendor companies that Intel has enabled:

1. ServerEngines*
2. ASpeed Technology*
3. Nuvoton* (Winbond* subsidiary)
4. Renesas*
5. SMSC* (Standard Microsystems Corporation)
6. ITE Tech

The following vendors have (had) PECI 1.1 parts:

1. On Semi* (purchased PECI business from ADI*)
2. Maxim*

Third Party DTS Tools

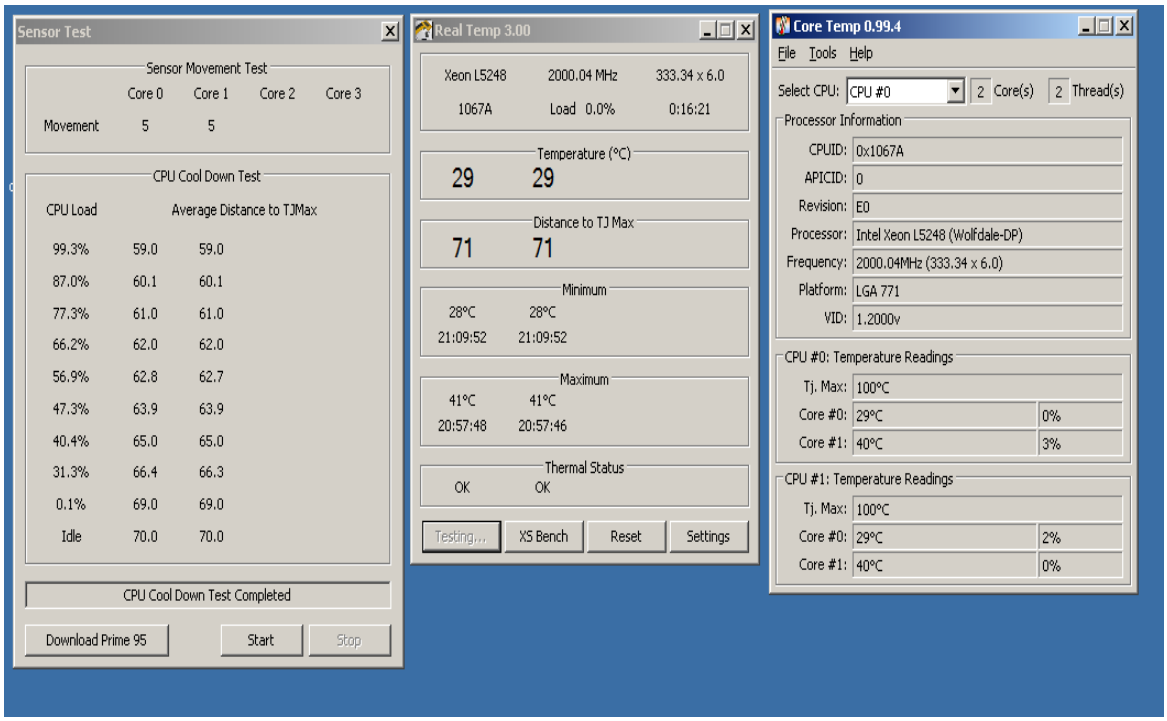
Real Temp* and Core Temp*

There are quite a few third-party software utilities to read out DTS data, such as Real Temp* and Core Temp*. These tools provide a convenient way to see the temperature variation reported by the sensor. However, since developers of these tools do not have knowledge of what the actual junction temperature is, they make some assumptions (for example, by assuming a value of 100 or 105 degrees), which may not be true for some processors.

The next section is an example of DTS reading by both Real Temp* and Core Temp*, in this case they all assume Tj = 100 degrees.

Running Windows Tools on Intel® Xeon® 5200 Processor Series Cores

Figure 6. Intel® Xeon® Processor Series DTS Data as Reported by Real Temp* and Core Temp*



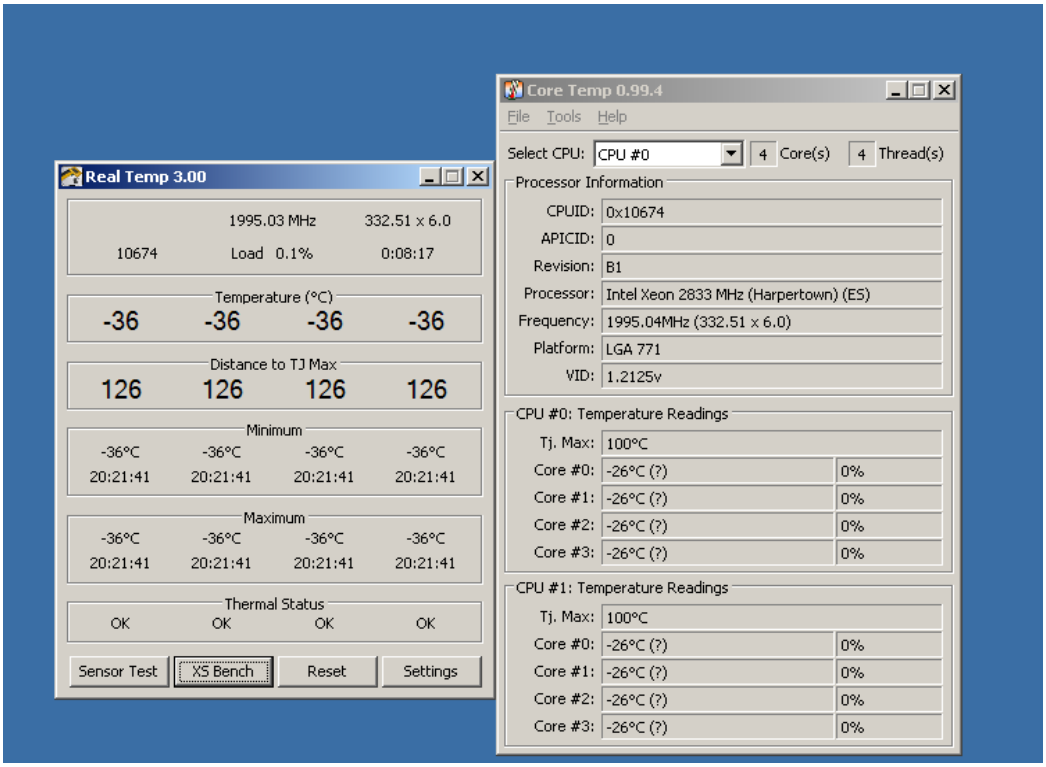
Performance tests and ratings are measured using specific computer systems and/or components and reflect the approximate performance of Intel products as measured by those tests. Any difference in system hardware or software design or configuration may affect actual performance. Buyers should consult other sources of information to evaluate the performance of systems or components they are considering purchasing. For more

information on performance tests and on the performance of Intel products, visit Intel Performance Benchmark Limitations

There are several issues with these tools. First the assumed value for Tj may not be correct and thus impact the accuracy of actual temperature reporting. Secondly the DTS is only accurate when in the adjacency of Tj. Not knowing the intention and effective range of DTS, the tools try to compensate with the inaccuracy of low temperature reading, which may not be a correct interpretation.

Another issue with third-party software is that sometimes they report DTS data when the reading is invalid. There is a bit in thermal status MSR that indicates if the current DTS data is valid. When the data is marked as invalid, software should simply ignore the data. Here is an example where software read out invalid DTS data and generated unrealistic results:

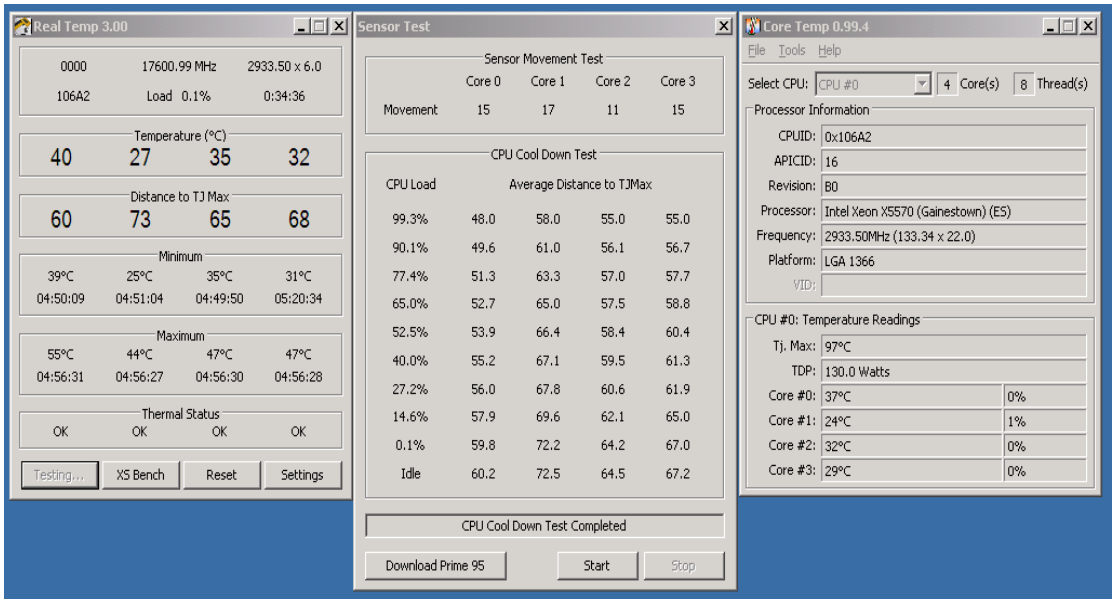
Figure 7. Invalid DTS Reading Output Examples by Real Temp* and Core Temp*



Running Windows* Tools on Intel® Xeon® 5500 Cores

The results of running Real Temp* and Core Temp* on Intel® Xeon® 5500 processors are captured in Figure 8:

Figure 8. Intel® Xeon® 5500 DTS reading by Real Temp* and Core Temp*

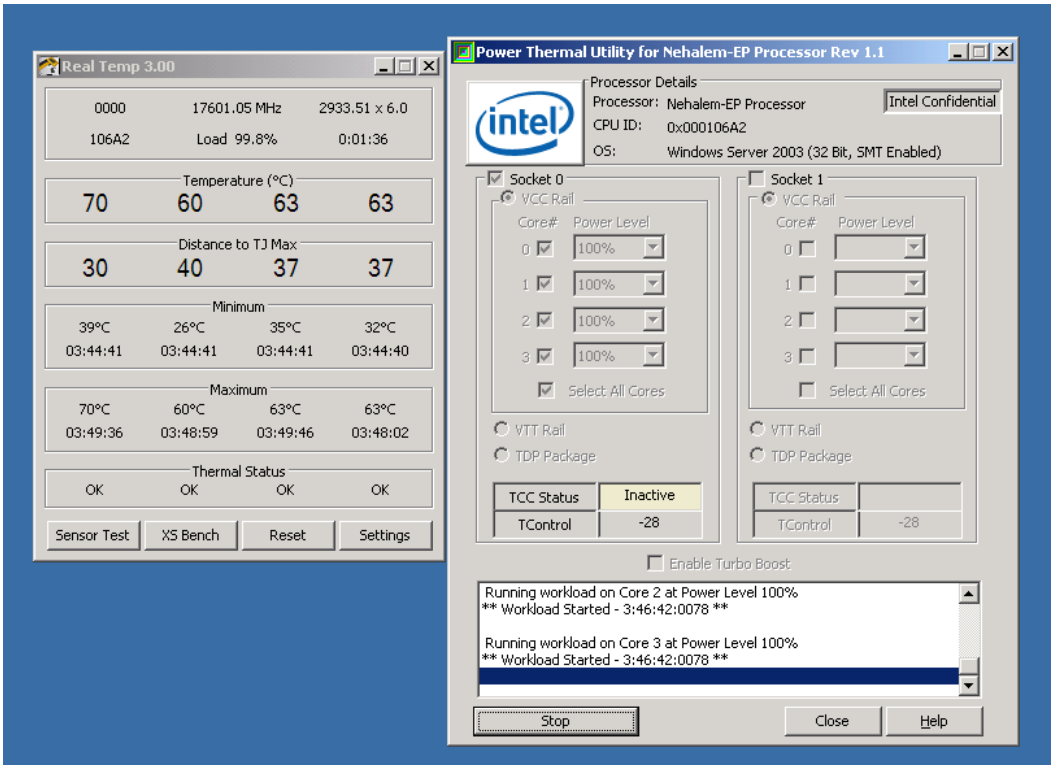


Running the Power Thermal Utility on Intel® Xeon® 5500 Processor Series

Figure 9 shows the effect of running the Power Thermal Utility (PTU) at 100% power level on DTS reading. The highest temperature the cores can reach by running the PTU software program is ~70°C.

To gain access to the PTU for the Intel® Xeon® 5500 processor as well as PTUs for other processors, contact your Intel field representative.

Figure 9. Intel® Xeon® 5500 DTS Reading With maxPower Test Running



Linux* Core Temp

Core Temp is a Linux* kernel module. It has been maintained relatively well and has included support for the Intel® Xeon® 5200 and 5400 Processor series. Our tests are done on Fedora* 10, which has kernel version of 2.6.25.

The main piece of Core Temp is msr read and write, as shown below:

```
#include <asm/msr.h>
static inline int wrmsr eio(u32 reg, u32 eax, u32 edx)
{
        int err;
        err = wrmsr safe(reg, eax, edx);
        if (err)
                err = -EIO;
        return err;
}

static inline int rdmsr_eio(u32 reg, u32 * eax, u32 * edx)
```

```
{
        int err;
        err = rdmsr safe(reg, eax, edx);
        if (err)
                err = -EIO;
        return err;
}
```

Eventually, Core Temp sends the temperature data to sysfs and can be read by users.

The following command will read out core 0 DTS:

```
> cat /sys/devices/platform/coretemp.0/temp1_input
```

On WDP system the sample data we received is:

```
> 70000 (Which means 70°C)
```

Tjmax used by Core Temp:

```
> cat /sys/devices/platform/coretemp.0/temp1_crit
> 100000 (Which means 100°C)
```

On Intel® Xeon® 5500 system the sample data we received is:

```
> 40000 (which means 40°C)
```

Direct MSR Access

The Mode Specific Registers (MSRs) for both Intel® Xeon® 5200 and 5500 processor families are similar to these of Pentium M. For more information regarding to MSRs, please refer to the *IA-32 Intel® Architecture Software Developer's Manual*, Volume 3B. Contact your Intel field representative for access to the latest version.

All MSRs can be read with the RDMSR and written with the WRMSR instructions. The software utilities described above all ultimately reply on these instructions to obtain MSR content.

Key Thermal-related MSRs

Some information as released in Intel® Architecture Software Developers' Manuals:

Table 2. IA32_THERM_INTERRUPT

ADDR	Name and Bits	Description
19BH	IA32_THERM_INTERRUPT	Thermal INT control Modulation Control (R/W)
	0	High-Temperature INT enable
	1	Low-Temperature INT enable
	2	PROCHOT# INT enable
	3	FORCEPR# INT Enable
	4	Critical Temperature Enable
	7:5	Reserved
	14:8	Threshold #1 Value
	15	Threshold #1 INT Enable
	22:16	Threshold #2 Value
	23	Threshold #2 INT Enable
	24:63	Reserved

Table 3. IA32_TEMPERATURE_TARGET

ADDR	Name and Bits	Description
1A2H	IA32_TEMPERATURE_TARGET	Processor Junction Temperation Tj
	23:16	Temperature Target: the minimum temperature at which PROCHOT# will be asserted. The value is degree C
	63:24	Reserved

RDMSR and WRMSR instructions

Intel® architecture provides two system instructions that are used to read and write MSRs.

"RDMSR" instruction reads the contents of a 64-bit model specific register (MSR) specified in the ECX register into registers EDX:EAX. The EDX register is loaded with the high-order 32 bits of the MSR and the EAX register is loaded with the low-order 32 bits.

"WRMSR" writes the contents of registers EDX:EAX into the 64-bit model specific register (MSR) specified in the ECX register. The contents of the EDX register are copied to high-order 32 bits of the selected MSR and the contents of the EAX register are copied to low-order 32 bits of the MSR. (On processors that support the Intel® 64 architecture, the high-order 32 bits of each of RAX and RDX are ignored.)

Both "RDMSR" and "WRMSR" instructions must be executed at privilege level 0 or in real-address mode; otherwise, a general protection exception #GP(0) will be generated.

MSR Tools

There are many tools in Windows and Linux available to read out MSR data. These tools eventually use WRMSR/RDMSR instructions provided by Intel® architecture. Users can also develop their own MSR probing scripts.

In Windows, a tool called CrystalCPUID* (version 4.5 or newer) is one of many tools that can be used to capture MSR data. It provides a simple MSR walker and a MSR writer that serve the purpose of MSR read/write.

Discussions

Multi-core Implications

PROCHOT is package level and bi-directional signal. In a CMP implementation, only a single PROCHOT# pin will exist at a package level. When either core's thermal sensor trips, PROCHOT# will be driven by the processor package. It is important to note that in this scenario, PROCHOT# will be asserted though only one core may be throttling. When PROCHOT# is driven by an external agent, both processor cores will throttle. Bi-directional PROCHOT# is a new feature from the Intel® Pentium® M processor.

The IA32_THERM_STATUS MSR is associated with a processor core and is not shared between the two cores on the package (it is shared between logical processors on a HT technology processor). Similarly, the IA32_THERM_INTERRUPT MSR for controlling the thermal interrupts on "hot-to-not" and "not-to-hot" transitions are unique for each logical processor.

The thermal control circuitry that enables processor clock modulation can be enabled in software by writing to the IA32_THERM_CONTROL Model Specific Register which is replicated for each logical processor. In a CMP processor, each processor core will modulate the clock independently.

How to Convert PECI/DTS Values to An Absolute Temperature

For legacy system level fan speed control that requires an absolute temperature value for the processor, an absolute temperature value can be approximated.

Note: PECI is most accurate near the maximum temperature (PROCHOT#) and it is accurate enough for fan speed control in the $T_{CONTROL}$ range but it can be very inaccurate at low temperatures.

In order to send an absolute temperature to the system level fan speed control some work will have to be done upstream. The first step is to note the TCC activation target temperature. For Intel® Xeon® 5500 generations this is visible in the IA32_Temperature_Target MSR but for Intel® Xeon® 5200 processors our best guidance is in Table 7 below but it is important to note that these values are only guidance and not specification. The second step is to read the individual DTS values or the temperature monitor over PECI directly. The PECI bus will report the highest temperature value as the smallest temperature delta to TCC. The last step is to subtract the temperature offset from the TCC activation target to approximate an absolute temperature.

When using absolute temperature for fan speed control it is important to follow the intent of the standard PECI-based recommended method. Fans should be at full fan speed once the processor has reached $T_{CONTROL}$. To determine the absolute $T_{CONTROL}$ temperature for fan speed control logic, subtract the $T_{CONTROL}$ offset from the TCC activation target.

Table 4. TCC Activation T_J Targets

Process	Processor	TCC Activation T_J Target
45nm	Intel® Xeon® Processors 5400 Quad-Core:	
	X5492, X5482, X5472, X5470, X5460, X5450	85 °C
	E5472, E5462, E5450/40/30/20/10/05	85 °C
	L5408	95 °C
	L5430, L5420, L5410	70 °C
45nm	Intel® Xeon® Processors 5200 Dual-Core	
	X5282, X5272, X5270, X5260	90 °C
	E5240, E5220, E5205	90 °C
	E5205, E5220	70 °C
	L5240	70 °C
	L5238, L5215	95 °C
65nm	Intel® Xeon® Processors 5000 Quad-Core	
	Intel Xeon processors X5000	90-95 °C
	Intel Xeon processors E5000	80 °C
	Intel Xeon processors L5000	70 °C
	L5318	95 °C
65nm	Intel® Xeon® Processors 5000 Dual-Core	
	5080, 5063, 5060, 5050, 5030	80 90 °C
	5160, 5150, 5148, 5140, 5130, 5120, 5110	80 °C
	L5138	100 °C

The Differences Between Reading the PECI Bus and Reading the DTS Through An MSR

Each DTS needs to be read individually but they can be read without extra PECI hard ware. The DTS gives an instantaneous value at a resolution of 1 degree and may be subjective to noise.

PECI reports the average temperature of the hottest core but usually needs extra logic such as a BMC chip. PECI reads at a higher resolution and also uses an averaging function to remove the affect of noise.

Conclusion

You should now have a better understanding for how to use DTS/PECI to monitor processor temperature. The DTS can be used to monitor silicon junction temperature. PECI is used to focus on the hottest DTS value. Third party hardware and software are used to read PECI.

Thermal mechanisms are controlled by the same DTS values that are read over PECI so monitoring these temperature values will give some warning for thermal events like throttling. The DTS has accuracy and range limits that have changed over the last few processor generations. PECI hardware and software is available from a variety of vendors. MSR values can be read directly or third party DTS tools can be used to monitor temperature.

The Intel® Embedded Design Center provides qualified developers with web-based access to technical resources. Access Intel Confidential design materials, step-by step guidance, application reference solutions, training, Intel's tool loaner program, and connect with an e-help desk and the embedded community. Design Fast. Design Smart. Get started today. http://intel.com/embedded/edc.

Related Documents

Table 5. List of Related Documents

Document Title	Document #
Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B: System Programming Guide	253669
Dual-Core Intel® Xeon® Processor 5200 Series [Wolfdale-DP] Thermal/Mechanical Design Guidelines, Revision 2.0	352031
Intel® Xeon® Processor 5200 Series Thermal/Mechanical Design Guidelines	318675
Intel® Xeon® Processor 5200 Series Processor in Embedded Applications Thermal/Mechanical Design Guidelines	319012
Quad-Core Intel® Xeon® Processor 5400 Series [Harpertown] Thermal/Mechanical Design Guidelines, Revision 2.0	373191
Intel® Xeon® Processor 5400 Series Thermal/Mechanical Design Guidelines	318611
Intel® Xeon® Processor L5408 Series in Embedded Applications Thermal/Mechanical Design Guidelines	319133
Dual-Core Intel® Xeon® Processor 5200 Series [Wolfdale-DP] – Electrical, Mechanical, and Thermal Specification (EMTS) – Rev. 2.2	352033
Intel® Xeon® Processor 5200 Series Datasheet	318590
Quad-Core Intel® Xeon® Processor 5400 Series [Harpertown] – Electrical, Mechanical, and Thermal Specification (EMTS) – Rev. 2.2	352007
Intel® Xeon® Processor 5400 Series Datasheet	318589
Intel® Xeon® Processor 5500 Series (Nehalem-EP) Processor Electrical, Mechanical, and Thermal Specifications (EMTS) - Revision 2.0	362033
Intel® Xeon® Processor 5500 Series Datasheet, Volume 1	321321-001
Intel® Xeon® Processor 5500 Series Datasheet, Volume 2	321322-001
Intel® Xeon® Processor 5500 Series Thermal/Mechanical Design Guide	321323
PECI 2.0 Feature Set Overview	357014
Nehalem-EP Processor Power Thermal Utility Rev 1.1	387761
Nehalem-EP Processor Power Thermal Utility - Linux Version, Rev 1.4	414105
NOTES: For access to Intel Confidential and Intel Restricted Secret documents, contact your Intel field representative.	

Authors

Michael Berktold is a Sr. Thermal/Mechanical Engineer with Embedded and Communications Group at Intel Corporation.

Tian Tian is a Technical Marketing Engineer with Embedded and Communications Group at Intel Corporation.

Acronyms

CMP	Chip Multi-Processing, a single physical package that utilizes multiple cores for multi-processing capabilities.
PECI	Platform Environmental Control Interface. The temperature reported over PECI is always a negative value and represents a delta below the onset of thermal control circuit (TCC) activation, as indicated by PROCHOT#.
PROCHOT#	PECI value = 0. (Processor Hot) will go active when the processor's temperature monitoring sensor detects that the processor has reached its maximum safe operating Temperature. This indicates that the Thermal Control Circuit (TCC) has been activated, if enabled. The TCC will remain active until shortly after the processor deasserts PROCHOT#.
PWRGOOD	The signal used during power-on reset to indicate that power is good and applied to the processor. The power-on reset causes all MSRs and general purpose registers within the processor to be initialized to their default value. During the power-on reset, PWRGOOD signal is de-asserted.
TCC	Thermal Control Circuit, a feature of the processor that is used to cool the processor should the processor temperature exceed a predetermined activation temperature.
THERMTRIP#	PECI reads 0 still or error. Assertion of THERMTRIP# (Thermal Trip) indicates the processor junction temperature has reached a temperature beyond which permanent silicon damage may occur.
(TM1 & TM2)	Thermal Monitor. A feature on the processor that can keep the processor's die temperature within factory specifications under normal operating conditions.
$T_{CONTROL}$	PECI value processor specific. If the value reported via PECI is less than TCONTROL, then the case temperature is permitted to exceed the Thermal Profile. If the value reported via PECI is greater than or equal to TCONTROL, then the processor case temperature must remain at or below the temperature as specified by the thermal specification.