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List of Symbols

Symbol	Description	Unit
A	Amplitude	1
ΔA	Amplitude deviation	1
A/D	Analog-to-Digital	
$A_{foldback}$	Ratio between amplifier bandwidth and system bandwidth	1
A_b	Amplitude of square wave	1
A_c	Amplitude of sine wave	1
A_d	Attenuation component: index d	1
A_e	Amplitude of error signal	1
A_f	Amplitude of fundamental	1
A_j	Amplitude level: index j	1
A_l	Limiter constant	1
A_{rms}	Root Mean Square amplitude value	1
A_s	Amplitude of sine wave	1
$A_{stopband}$	Stopband attenuation	dB
ATE	Automatic Test Equipment	
A_{pp}	Peak-to-peak amplitude	1
A_n	Operational Amplifier: index n	1
A_0	Output value of 1-bit quantizer	1
$A_{openloop}$	Open-loop amplification	1
B	Full-Scale Value	1
B_{in}	Input number of bits	1
B_0	Most Significant Bit Value	1
B_m	m_{th} Bit Value	1
B_{n-1}	Least Significant Bit Value	1
B_{out}	Output number of bits	1

BER	Bit Error Rate	1
C	Constant	1
C_{bc}	Base-Collector capacitance	F
C_{be}	Base-Emitter capacitance	F
C_{bex}	Extra Base-Emitter capacitance	F
C_d	Diode capacitance	F
C_g	Comparator gain index: g	F
$C_{H(old)}$	Hold capacitor	F
C_{in}	Input capacitance	F
CML	Current Mode Logic	
C_n	Capacitor: index n	F
$CMOS$	Complementary Metal Oxide Semiconductor	
C_m	Digital code: index m	F
C_n	Capacitor: index n	F
D/A	Digital-to-Analog	
DC	Direct Current	A
D_n	Diode: index n	
DNL	Differential Non-Linearity	1
D_{out}	Digital output data	1
$E(.)$	Statistical expectation	1
ECL	Emitter Coupled Logic	
$ENOB$	Effective Number of Bits	1
EPS	Errors Per Second	1
ERB	Effective Resolution Bandwidth	Hz
$EXOR$	Exclusive OR function	
E_{glitch}	Glitch error	Vs
E_{LSB}	LSB energy	Vs
E_{noise}	Quantization noise voltage	V
E_{total}	Total noise voltage	V
E_{qns}	Quantization noise voltage	V
$E^2_{qns}(f)$	Quantization noise density	V^2/Hz
f	Frequency	Hz
f_b	-3 dB bandwidth	Hz
f_c	Clock frequency	Hz
f_{comp}	Comparator -3 dB bandwidth	Hz
f_{in}	Input signal frequency	Hz

f_{osc}	Oscillation frequency	Hz
f_{qns}	Quantization noise bandwidth	Hz
f_s	Sample frequency	Hz
f_{sig}	Signal bandwidth	Hz
f_{UGB}	Unity Gain Bandwidth	Hz
FSR	Full-Scale Range	1
G_A	Amplifier gain	1
$G(z)$	Transfer function	1
g_m	Mutual transconductance	A/V
$H(z)$	Transfer function	1
$H(\omega)$	System transfer function	1
$HS3$	High-speed bipolar oxide isolated process	
f_1	Unity gain bandwidth	Hz
f_t	Transition frequency	Hz
I	Current	A
ΔI	Current deviation	A
i	As index	1
IC	Integrated Circuit	
I_{comp}	Compensation current	A
$I_{leakage}$	Leakage current	A
I_{out}	Output current	A
I_{Ref}	Reference current	A
$IEEE$	Institute of Electrical and Electronic Engineers	
INL	Integral Non-Linearity	1
i_0	Base-Emitter reverse current	A
I_0	Bias current index: 0	A
I^2S	Inter IC Signal Standard	
I_T	Temperature-dependent current	A/degree C
I_{in}	Input current	A
$J-FET$	Junction Field Effect Transistor	
$J(z)$	Transfer function	1
k	Boltzmann's constant 1.38×10^{-23} J/K As index	1
$K(z)$	Transfer function	1
LSB	Least Significant Bit	
m	As index	1
	Mean value	1

Δ_m	Error of m^{th} bit 1	
MN	N-MOS transistor	
MP	P-MOS transistor	
MSB	Most Significant Bit	
M_n	Meta stable condition index: n	1
N	As variable: Sample rate reduction ratio	1
$N_{digital}$	Number of counts	1
N_{fold}	Number of folds	1
n	As index: number of bits	1
	As exponent in temp. relation $\approx 1.4 - 1.8$	
Δn	Error of n_{th} bit	1
n_r	Number of pulses index: r	1
OA	Operational Amplifier	
p	Ratio between emitter areas	1
P	Reference level	1
$PSSR$	Power Supply Rejection Ratio	1
$P(x)$	Probability distribution function	1
ppm	Parts per million	10^{-6}
p_{signal}	Signal power	W
p_{total}	Total noise power	W
q	Electron charge	1.6×10^{-19} C
Q	Reference level	1
q_e	Quantization error	1
$Q(k)$	Probability function (large k)	1
q_s	Quantization level	1
q_{nd}	Quantization noise plus distortion	W
q_{qns}	Quantization noise power	W
Q_n	Transistor index: n	
Q_{ref}	Reference charge	C
RC	First-order time constant	s
R_L	Load resistor	Ohm
R_n	Resistor index: n	Ohm
R_{out}	Output resistance	Ohm
RAM	Random Access Memory	
ROM	Read Only Memory	
R_{ref}	Reference source value	1

$SINAD$	Signal-to-noise and distortion ratio	dB
$SFDR$	Spurious Free Dynamic Range	1
S/N	Signal-to-noise ratio	dB
$S/N(f)$	Signal-to-noise density ratio	dB $\sqrt{Hz}$
S/N_{system}	Signal-to-noise ratio of a system	dB
$S/N_{quantizer}$	Signal-to-noise ratio of quantizer	dB
S_n	Switch index: n	
S	Step size	1
S_{tcor}	Correction factor	1
S_{tout}	Output step size	1
SW_n	Switch index: n	
ΔS_{tout}	Output step size deviation	1
T	Absolute temperature	K
ΔT	Absolute temperature variation	K
THD	Total Harmonic Distortion	
$T_{conversion}$	Conversion time	s
T_0	Reference temperature	K
T_p	Time period index: p	s
T_n	Transistor index: n	
TTL	Transistor Transistor Logic	
t	Time	s
Δt	Time deviation	s
t_{max}	Maximum time deviation	s
t_d	Delay time	s
δt_{td}	Delay time difference	s
t_{dif}	Time difference	s
t_h	Hold time	s
$U(t)$	Unity step function	1
V	Potential	V
ΔV	Potential deviation	V
V_a	Analog voltage	V
V_B	Battery voltage	V
V_{be}	AC Base-emitter voltage	V
V_{BE}	DC Base-emitter voltage	V
V_D	Diode voltage	V
$V_{difference}$	Difference voltage	V

V_{droop}	Droop voltage	V
V_{fs}	Full-scale voltage value	V
V_g	Bandgap voltage of silicon	1.208 V
V_{id}	Idle noise voltage	V
V_{in}	Input voltage	V
V_{lr}	Linear voltage range	V
V_{max}	Maximum voltage	V
V_n	Voltage at node index: n	V
V_{out}	Output voltage	V
V_p	Peak voltage	V
V_{ref}	Accurate reference voltage	V
V_{rn}	Reference voltage at node index: n	V
V_{tap}	Reference tap voltage	V
V_{th}	Threshold voltage	V
z	Complex frequency for discrete signals	
β	Transistor current gain	1
β_{square}	Unit area MOS gain factor	$\mu A/V^2\mu$
ϵ	Amplitude deviation	1
ϵ_m	Error index: m	1
Δ	Matching deviation	1
π	Angular constant	3.14159
λ_n	Integration constant index: n	1
λ	Global transfer	1
λ_b	Global transfer of square wave	1
λ_l	Global transfer of limiter	1
λ_m	Maximum value of λ	1
λ_s	Global transfer of sine wave	1
Λ	Real value	1
$\sigma(P)$	Standard deviation of P	1
τ_d	Delay time	s
Θ_n	Complex phase	rad
ω	Angular frequency	rad/s
Φ	Phase angle	rad

Preface

In this introduction an overview of the contents of this book will be given. Analog-to-digital (A/D) and digital-to-analog (D/A) converters provide the link between the analog world of transducers and the digital world of signal processing, computing, and other digital data collection or data processing systems. Numerous types of converters have been designed that use the best technology available at the time a design is made. High-performance sub-micron CMOS technologies result in high-resolution or high-speed A/D and D/A converters that can be applied in digital audio, digital video, instrumentation and signal processing systems. Furthermore, sub-micron CMOS technologies show an increase in conversion speed into the Giga Hertz range. Applications in these areas are, for example, in high-definition digital television, digital receiver applications, Local Area Networks, cable modem chips and digital oscilloscopes. The availability of high-speed memory chips results in so-called "one-shot" memory applications in these oscilloscopes. In this book different techniques to improve the accuracy in high-resolution A/D and D/A converters will be discussed. Also, special techniques to reduce the number of elements in high-speed A/D converters by a repetitive use of comparators will be described.

In chapter one the application of converters in systems will be discussed. If analog-to-digital and digital-to-analog converters are applied in discrete-time systems it is important to perform these operations on frequency-band-limited signals. In most cases filters are needed to limit the input and output spectrum of the analog signals. If no band limitation is performed, then aliasing of the analog signals into the signal band of interest can occur. General criteria that determine the overall system performance in the case of ideal converters are introduced and defined. Combinations of analog and digital filtering operations result in linear phase filtering over the band of interest. Such a linear phase filtering is very important in digital audio systems.

Performance definitions of converters are defined in chapter two. The performance definitions must be unique for a specific parameter. Good parameter definitions of converters are very important in determining the final performance of a discrete-time system. Furthermore, these definitions can be used to compare the performance of different brands of converters. In particular, a good definition of the dynamic parameters of converters is needed. The application of converters in digital audio, digital video systems and digitization of carrier signals, for example, requires these dynamic specifications. Many converters that originally were designed for high-accuracy measurement system applications are not optimized for dynamic operations. In digital audio, for example, many specifications, that are important in instrumentation (such as offset, full-scale accuracy, temperature drift) are of minor value. The specific dynamic parameters must therefore be defined and related to important design parameters. Glitches in D/A converters introduce distortion in digital audio systems, while in video display systems fuzzy images are obtained. Definitions like Effective Number of Bits (ENOB), Spurious Free Dynamic Range (SFDR), jitter of the sampling clock and interconnect wire delay will be correlated to Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) specifications. Furthermore quantization spectra and the influence on the linearity specification will be derived.

In general it can be said that the number of systems and circuits that can perform analog-to-digital conversion is much larger than the number of structures and basic solutions to digital-to-analog conversion. In chapter three examples of high-speed analog-to-digital converters are discussed. Up until now the full-flash converter was considered the fastest converter type that can be designed. This, however, is only partly true. Due to the use of a large amount of components for example, in an 8-bit converter 255 comparators are needed to detect every code level the size of such a converter becomes large with respect to the time a signal needs to travel over the interconnection lines on a chip. In high-speed converters the time difference for signals traveling at the top of the converter structure with respect to signals traveling in the middle of the structure may become in the order of pico seconds. At high-input frequencies these time differences in signal transfer introduce distortion. Depending on input frequency and resolution of a converter, timing differences may not exceed pico second values. When taking into account that the transmission speed over the interconnection lines in sub-micron CMOS integrated circuit is about one-third of the speed of light, then 1 psec equals about 100 microns of interconnect. When the

size of an analog-to-digital converter chip without sample-and-hold amplifier increases, it is practically impossible to match clock- and signal-line delays within the required timing accuracy. Therefore, improved converter systems with a reduced chip size using a continuous input-signal folding architecture overcome these problems. In a final system implementation of such a system, only zero crossings of the analog signal are important for the converter accuracy. To reduce the number of input amplifier-comparator stages in such a system, an interpolation of zero crossings is used. This system results in a compact very high-performance analog-to-digital converter structure. In an MOS technology switches and capacitors are the main design elements. The input signal can be stored on multiple capacitors and then a comparison is made to perform an A/D conversion. Subranging or two-step system solutions can be easily implemented. These systems show a very good performance close to the ideal converter at reasonable high sampling rates. Finally pipeline converters will be discussed. These systems can use a 1.5 bit per stage or multi-bit per stage conversion units. The multi-bit per stage can suffer from linearity problems in the first stages depending on the resolution of the converter. Calibration of these stages can overcome these problems.

High-speed digital-to-analog converters discussed in chapter four show good performance at sampling frequencies up to 1 GSample/s. These converters can use binary weighted capacitor arrays. In modern technologies capacitor matching is good enough to obtain a full linearity specification up to 12-bit resolution without trimming. However, most high-speed digital-to-analog converters use segmented current source structures in combination with binary weighting of current sources. The segmentation improves linearity and guarantees monotonicity, while furthermore it is more easy to obtain a low glitch energy under dynamic operation of the converter. Especially the performance at high output signal frequencies is discussed in a couple of designs. Timing is the most important issue after obtaining the linearity specification.

In high-accuracy analog-to-digital and digital-to-analog converters the accuracy with which the binary weighting of the bit weights is performed is an important design criterion. In chapters five and six generally applicable methods to obtain high-accuracy converters will be introduced. These methods will mainly use a combination of accuracy introduced by matched elements and a dynamic method to improve the limited passive accuracy. Resistor or capacitor matching in integrated circuits limits the resolution of converters based on these elements to about twelve bits. Trimming methods

can be used to overcome this problem. These trimming methods, however, are expensive, while in addition changes of the trimmed elements due to time or temperature variations destroy the accurate trimming of the converter. In MOS technologies accuracy is obtained by matching binary weighted capacitor banks. Accuracies of ten to twelve bits are possible without trimming.

When monotonicity of a converter is the most important design criterion then special system configurations are possible. Solutions based on current swapping or voltage division will be described. These systems are inherently monotonic while overall linearity is limited.

When the absolute accuracy in a converter is required, then special systems are needed. Systems which convert the digital value into an accurate time need a limited amount of accurate elements. However, speed is limited, while systems with higher sampling rates suffer from extremely high clock frequencies which result in high-frequency signal radiation.

To overcome these problems a combination of passive and active matching of components will be used. The first method combines accurate passive division with a time interchanging concept to obtain a very high weighting accuracy without using accurate elements. Furthermore, this method is independent of element aging and remains accurate over a large temperature range. Examples of digital-to-analog and analog-to-digital converters will be given that use this special method. In an MOS technology calibration of current sources can be used to obtain a segmented converter structure. Such a structure is less sensitive to element matching, while the calibration of the individual current sources makes the system independent of element aging and less temperature-sensitive. The gate capacitance of an MOS device is used to store the error signal information that is needed to calibrate the bit current sources.

In high-speed, high-accuracy analog-to-digital converters the analog input signal must be sampled and kept constant during the time the conversion takes place. High-resolution, high-speed and high-accuracy sample-and-hold amplifiers are a key element for analog-to-digital conversion in, for example, digital video, digital audio or carrier signal conversion. In chapter seven sample-and-hold amplifiers are discussed. A high-performance sample-and-hold amplifier in front of a parallel-type A/D converter can for example improve at high frequencies the dynamic performance of such a converter. The sampling of the analog signal in this way is performed by the sample-

and-hold amplifier. Distortion introduced by timing uncertainties at high frequencies in the flash converter can be avoided in this way. Only a single switch in the sample-and-hold amplifier determines the timing accuracy.

Different examples of sample-and-hold amplifiers are shown. Furthermore in sub-micron technology the sampling switches may become a problem. Therefore clock bootstrapping techniques will be shown that improve the performance of the sampling switches.
In chapters eight and nine examples of noise-shaping techniques to improve the dynamic range of a system are described. Such techniques are very useful when speed can be exchanged with accuracy or with the word length used in a system.

An ultimate of the noise-shaping techniques are the well-known sigma-delta A/D and D/A converters which basically use a noise-shaping filter in cooperation with a quantizer and a 1-bit D/A or A/D converter stage. Such a 1-bit converter is extremely linear, which results in a very good differential linearity of such a converter. The most important design criteria and limitations will be given. At the moment the dynamic range of a system must be increased but the maximum clock speed in the system cannot be enlarged, then a multi-bit D/A converter can be used in the feedback loop. At that moment, however, the linearity of the D/A converter determines the overall linearity of the converter. Therefore, dynamic element matching in the form of Data Weighted Averaging or other error randomizing techniques can be used.
The root locus method can be used successfully to determine the stability of noise-shaping coders. However, modeling a quantizer simply with a variable gain is not sufficient to predict the stability at small signals of the converter. Therefore a modified model using a variable gain and a phase uncertainty is introduced. This model predicts the small signal stability of the converters pretty well. Especially when a higher-order noise-shaping filter is used, the stability analysis gives an insight in the operation of the system when small input signals are applied. A noise-shaping coder is said to be stable when an idle pattern at half the sampling frequency is present under nearly all input signal conditions. Different architectures will be described which introduce a high-order noise-shaping filter architecture without running into a stability problem. A special system that uses a signal-level-dependent filtering order implements a kind of feed-forward coupling in the filtering function. At low-level input signals a high-order filtering function is present, but at the moment the signal in the loop increases in amplitude, the filter order is

reduced. In this way a very good optimum between filter order and stability of operation is obtained. Examples of designed 16- to 20-bit D/A converters using 1-bit or multi-bit D/A converters will be described.
The MASH structure that uses a cascade of first or second order noise-shaping stages prevents the problem of instability while at the same time a higher order noise-shaping filtering operation is performed.
Bandpass sigma-delta modulators are added to complete the overview. A specific design using a continuous time noise-shaping filter shows already very good performance for applications in digital radio systems.
Finally an example of a 5-digit digital voltmeter system that completes chapter eight will be given.

Low-noise high-stability reference sources are a basic element in converters. Different methods to obtain accurate and temperature insensitive reference sources will be given in chapter ten. The temperature dependence of the bandgap voltage (about 1.2 V) reference sources is small and in CMOS the parasitic substrate bipolar PNP devices are used for this purpose. The noise analysis of these systems is performed. In signal processing applications the absolute value of the reference source is not always important. System noise might be dominant and therefore reference sources must be designed for minimum noise performance. In low-voltage systems (1 V) the bandgap designs are difficult and mostly higher voltages are used to solve this problem.

In high-speed analog-to-digital converters that are based on the full-flash or folding principles, the question about the relation between maximum analog input frequency and the bandwidth of the comparator-amplifier stages arises. In chapter eleven an analysis that determines the relation between the maximum analog input frequency and the bandwidth of the comparator-amplifier stages is performed. Furthermore it will be shown from this analysis that a limited analog bandwidth of the system results in third-order signal distortion. This distortion can fold signals back into the baseband of the converter and results in a reduction of the signal-to-noise ratio of the system. The maximum analog input frequency will be defined as that input frequency for which the signal-to-noise ratio is reduced by a value equal to half the least significant bit. The number of effective bits as a function of input frequency will be used as an accurate measure for the performance of high-speed analog-to-digital converters. A second analysis about the decision failure of comparators in flash-type converters is performed. This analysis gives insight in the relation between the bit error rate (BER) of a comparator as a function of the gain-bandwidth product of a technology.

Comparator stages can be optimized for a minimum error.

In chapter twelve attention is paid to sub-micron CMOS technologies. Especially matching of components is a very important requirement. Most systems used today have a differential signal operation to reduce cross talk from other (mostly digital) system parts. Results and design issues are given in this chapter.
Components in an integrated circuit are best matched when they are placed close to each other. Furthermore, these devices must be placed on chip using an isothermal boundary. When more devices such as transistors or resistors must have a very good matching, care must be taken that neighboring, not active elements are placed at the edges of the layout of such a system. In this way an improvement in matching between the individual elements of the array is obtained.
After defining the important specifications of converters, good measurement set-ups and definitions are needed. In chapter thirteen attention is paid to measuring the static and dynamic performance of converters. Usually DC parameters can be measured with automatic test equipment and are well defined. Much attention has been paid to obtaining measurements and measurement set-ups which give the required parameter in a fairly simple way and use a well-defined test condition. One of the most important parameters to be determined in this way is the dynamic performance of a system. The dynamic range is determined by measuring the signal-to-noise ratio of a converter over half the sampling frequency. This signal-to-noise ratio must, in the case of a well-designed converter, be close to the theoretical value, which is defined over a bandwidth equal to half the sampling frequency. When large discrepancies are found, then this converter is not designed to operate under dynamic conditions. Sometimes it is possible to overcome some of the problems by adding external circuitry, which, for example, can be a deglitcher circuit to reduce the glitch of the converter or by adding data latches which perform the switching of the bit weights in a digital-to-analog converter at the same time moment.

During the writing of this book an attempt has been made to discuss the most important parameters and design criteria and giving worked-out examples of practical circuits and systems. On the other hand, no attempt has been made to be complete and cover all subjects in detail. By including practically worked-out examples, what in a number of cases are products supplied by semiconductor manufacturers, the reader gets familiar with design problems and practical system implementations under real conditions.

For the most part, these implementations differ quite a lot from the basic system solution.
Furthermore this book is not written to be complete. Always it can be improved and system or circuit solutions that are more optimal to perform a function will be available or will soon be. An attempt has been made to include important design examples from literature to give the reader an insight on what can be obtained in CMOS technology. Furthermore circuits or systems are mostly briefly discussed. The size of the book would increase too much in case all circuits should have been discussed more detailed. Therefore the limited description has been used. The reader can copy the publication from IEEE in case he is interested in more detailed analysis and study the specific system.

Chapter 1

The converter as a black box

1.1 Introduction

A/D and D/A converters are the link between the analog world of transducers and the digital world of signal processing and data handling. In an analog system bandwidth is limited by device and element performance and by the parasitics introduced. Thermal noise generated in active and passive components limits the dynamic range of an analog system. The ratio between the maximum allowable analog signal and the noise determines the dynamic range of the system. The signal-to-noise (S/N) ratio is a measure of the maximum dynamic range.

In a digital system the amplitude is quantized into discrete steps, and at the same time the signal is sampled at discrete time intervals. When the sampling time moments at quantization differ from the sampling time moments at the time the signal is reconstructed into an analog signal again, a signal distortion is introduced. This phenomenon is very important in discrete-time systems and finds its origin in "time jitter" or time uncertainty of the sampling clock. In particular, input signals at the high-frequency end of the signal band show a great sensitivity to a sampling time uncertainty. Furthermore, the sampling operation of analog signals introduces a repetition of input signal spectra at the sampling frequency and multiples of the sampling frequency. If the input signal bandwidth is larger than half the sampling frequency, aliasing of spectra occurs. In that case frequencies around the sampling frequencies and its multiples are folded back into the baseband of the system. Usually this is an unwanted phenomenon. To avoid aliasing of the signal, the input bandwidth must be limited to not more than half

the sampling frequency (Nyquist criterion see [7]). This filtering must be performed by continuous-time filters. Different solutions of filtering will be discussed. The preferable filtering type in high-resolution converters is obtained by a combination of digital filtering and linear phase analog filtering.

The quantization of analog signals into a number of amplitude-discrete levels places limitations on the accuracy with which signals can be reproduced. This quantization error is often called "quantization noise" to indicate that the errors have a random amplitude distribution and in this way have a noise-like frequency spectrum. This random character, however, implies that under no circumstances should the analog input signal and the sampling clock have any correlation [8]. If a correlation exists then the quantization errors appear at well-defined points in the frequency spectrum which are generally multiples of the signal frequency. Quantization of signals results in quantization errors. These quantization errors show an infinite bandwidth and after sampling, components above half the sampling frequency are folded back into the baseband. An analysis concerning the distortion of a signal due to quantization and the inter modulation between signals due to quantization will be shown. The ratio between the input signal frequency and the sampling frequency should preferably be an irrational number to avoid this correlation. In this case the quantization of a signal is performed at different amplitude levels of the quantizer and shows therefore a more randomized noise like character. The dynamic range of a digital system is determined by the number of quantization levels as will be shown in this chapter. By definition the noise is measured over a bandwidth equal to half the sampling frequency of the system.

In this chapter the different criteria mentioned will be described in more detail. The converter will be treated as an ideal black box. Specifications for input and output circuitry connected to the ideal converter will be derived under the condition that the overall system performance must be close to the ideal converter performance.

1.2 Basic D/A and A/D converter function

In Figure 1.1 a block diagram of a D/A converter is shown. Digital signals are applied to the converter as parallel signals. Suppose we have a binary-weighted converter, then the digital input value is converted into an analog

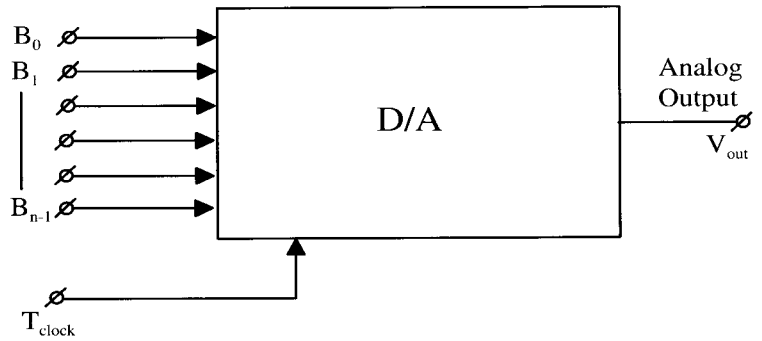


Figure 1.1: Block diagram of a D/A converter

value using the following equation:

$$V_{out} = \sum_{m=0}^{n-1} B_m 2^m R_{ref}. \tag{1.1}$$

In this equation V_{out} represents the analog output value and R_{ref} is a reference value. (R_{ref} may be a reference voltage, current or charge).

A reference current source or a reference voltage source are mostly used in practical implementations.

Note that equation 1.1 represents an n-bit binary weighted converter. B_{n-1} represents the Most Significant Bit (MSB) and B_0 is the Least Significant Bit (LSB) of the converter. The factor 2^m indicates the binary weighting of the bit values as a function of the variable m. $B_m = 1$ in case the value of bit m is added to the output signal and $B_m = 0$ when this bit is NOT added top the output.

The analog output value according to equation 1.1 can only change with a minimum step size equal to R_{ref} because of the quantization process. As *quantization step* $q_s = R_{ref}$ will be introduced. To simplify calculations q_s will be set at 1.

At the moment the Most Significant Bit is coupled with the reference R_{ref} then equation 1.1 changes into:

$$V_{out} = \sum_{m=0}^{n-1} B_m 2^{-m} R_{ref}. \tag{1.2}$$

By using the definition given in 1.2 the quantization step size q_s becomes:

$$q_s = 2^{-n+1} R_{ref}. \tag{1.3}$$

In the succeeding part of the book only the definition according to 1.1 will be used.

A block diagram of an A/D converter is shown in Figure 1.2. A sample-

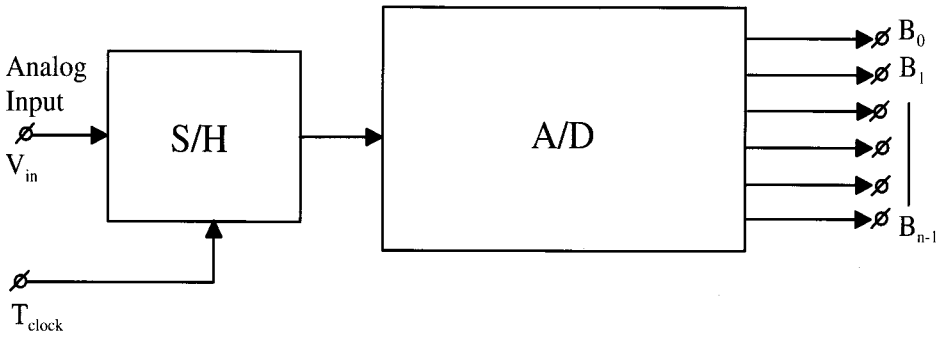


Figure 1.2: Block diagram of an A/D converter

and-hold amplifier is added to sample the input signal and hold the signal information at the sampled value during the time in which the conversion into a digital number is performed. In an A/D converter the equation 1.1 changes into:

$$\frac{V_a}{R_{ref}} = D_{out} + q_e = \sum_{m=0}^{n-1} B_m 2^m + q_e. \tag{1.4}$$

This can be partly rewritten as:

$$D_{out} = \sum_{m=0}^{n-1} B_m 2^m. \tag{1.5}$$

In this equation D_{out} represents the digitized value of the analog input signal V_a and q_e represents the quantization error. The quantization error represents the difference between the analog input signal V_a divided by R_{ref} and the quantized digital signal D_{out} when a finite number of quantization levels n is used.

1.3 Classification of signals

1.3.1 Different signal conditions

In an analog-to-digital and a digital-to-analog converter different signal conditions will be found. In Fig. 1.3 these different signal conditions are shown. To convert an analog signal into a digital signal two steps must be taken:

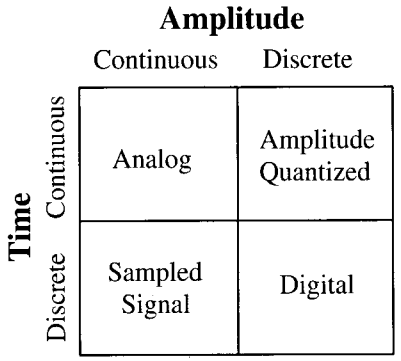


Figure 1.3: Different signal conditions

- Amplitude Quantization
- Sampling

These two operations must always be performed in a converter, but it does not matter which of the two is done first. What the effect of these two operations on a signal is and what kind of measures have to be taken to obtain a minimum signal distortion will be discussed now.

1.3.2 Analog signals

Analog signals are continuous-time and continuous-amplitude signals. Basically, there is no limitation in bandwidth and amplitude. When analog signals are processed by systems, however, frequency limitations are introduced and noise generated by active or passive components is added.

The dynamic range of a system is determined by the signal-to-noise ratio (S/N) of that system. An ideal test signal is supposed to be applied to that system for the determination of the signal-to-noise ratio. Maximum signal is determined by the distortion components generated in the system. A 10

% distortion level is adopted, for example, in power amplifiers to define the maximum signal level.

1.3.3 Discrete-time signals

Discrete-time signals are generated by sampling an analog signal at discrete time intervals without quantizing the amplitude of this signal. In most systems equal time intervals are used as the sampling clock. The sampling operation, however, introduces replica of the input frequency spectrum around the sampling frequency and multiples of the sampling frequency. To avoid aliasing of frequency spectra, the input signal bandwidth must be limited to half the sampling frequency as implied by the Nyquist criterion [7]. When an analog signal has to be limited in bandwidth, then a continuous-time filter instead of a switched capacitor filter is needed to avoid a repetition of frequency spectra in this filter. Such filters, however, can introduce phase distortion, which may be audible in high-performance digital audio systems.

One example of a discrete-time system is a sample-and-hold amplifier. In such an amplifier analog signals are sampled and stored on a capacitor during the hold time. Samples are taken at well-defined discrete time intervals without quantizing the signal amplitude.

1.3.4 Amplitude-discrete signals

In a continuous-time system the amplitude can be quantized into discrete amplitude levels, resulting in an amplitude-discrete signal. This operation can be performed to maintain well-defined amplitude levels when signals pass through several processing stages. This amplitude quantization introduces quantization errors that limit the accuracy and dynamic range of a system. To obtain step-like output signals of the quantizer, a high gain and a large comparator bandwidth are needed.

1.3.5 Digital signals

Digital signals are obtained if a signal is sampled at discrete time intervals and the amplitude is quantized in discrete amplitude levels. The amplitude quantization introduces quantization errors which limit the accuracy of the system. Sampling at discrete equal time intervals, requires a limited input spectrum to avoid aliasing. Variations in sampling time moments of fast-changing analog signals result in amplitude quantization errors, compared with signals sampled at equal well-defined time intervals. To avoid such

errors, the sampling time uncertainty must be small. Especially at the high end of the input frequency spectrum these errors are significant.

Digital values represent well-defined levels. In a binary coded system a "0" or ZERO represents an "off" or "false" state, while a "1" or ONE represents an "on" or "true" state. These well-defined levels are called logic levels which may be TTL, ECL, or CMOS levels in a binary-coded system.

A/D and D/A converters perform digitization or reconstruction of analog signals. The performance of such a system can be measured by measuring the signal-to-noise ratio over a well-defined system bandwidth. To simplify comparison of converters a measuring bandwidth equal to half the sampling frequency is used. In the following paragraphs these definitions will be explained in more detail.

1.4 Quantization errors

The quantization process in an ideal converter introduces an irreversible error (see [9] [10]). Furthermore the sampling time is fixed and constant and does not introduce an extra error. All errors discussed in this section are referred to the quantization error, so we will start analyzing the influence on the performance of the converter. Therefore we want to calculate the relation between the quantization step q_s and the input signal V_{in}. The quantization step is determined by the number of steps a signal is quantized into. This number of quantization steps is expressed in a number of (binary-weighted) bits n. In Figure 1.4 the quantization of a signal at the amplitude level A_j is shown. A signal $A_j + \varepsilon$ is ideally quantized into level A_j as long as the value of ε is between $-\frac{q_s}{2} < \varepsilon \leq \frac{q_s}{2}$. From this example it can be seen that the quantization error basically never exceeds an amplitude level equal to $\pm\frac{q_s}{2}$. Signals that are somewhat larger than $A_j + \frac{q_s}{2}$ are quantized to the next quantization level A_{j+1}.
In the lower part of Fig. 1.4 the probability density of the error over the quantization interval $-\frac{q_s}{2}$ to $\frac{q_s}{2}$ is shown. The uniform probability error function shows that there is no correlation between the signal frequency and the sampling frequency.
The mean-square-error due to quantization can now be calculated. We assume that over a long period of time all levels of uncertainty within the quantizing region $A_j \pm \frac{q_s}{2}$ appear the same number of times. A uniform probability density function over the interval $-\frac{q_s}{2}$ to $+\frac{q_s}{2}$ is defined in this

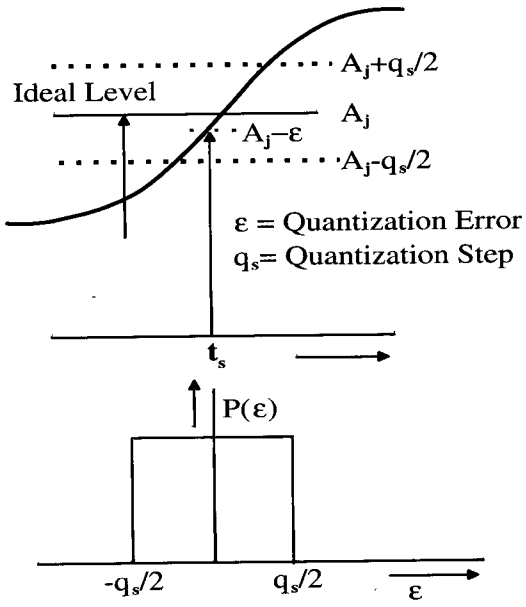


Figure 1.4: Quantization Error and Error Probability Density

way. On this assumption the mean-squared value of ε will then be:

$$E(\varepsilon^2) = \frac{1}{q_s}\int_{-\frac{q_s}{2}}^{\frac{q_s}{2}} \varepsilon^2 d\varepsilon. \tag{1.6}$$

The symbol $E(.)$ represents the statistical expectation. The average value of the error is zero with the assumptions made.

Solving the integral, the quantization error can be expressed as a quantization error voltage e^2_{qns}. The rms quantization error voltage $e^2_{qns} = E(\varepsilon^2)$ can be represented by:

$$e^2_{qns} = \frac{1}{12}q_s^2. \tag{1.7}$$

In an amplitude quantized system using n binary weighted bits the number of quantization levels (decision levels) equals $2^n - 1$. The maximum peak-to-peak amplitude in this system equals $2^n q_s$ before the next quantization level is reached. However, this maximum peak-to-peak level cannot always be obtained. As a result, the maximum peak-to-peak *sinewave* signal amplitude is between:

$$(2^n - 1)q_s \leq A_{pp} \leq 2^n q_s. \tag{1.8}$$

Here A_{pp} is the peak-to-peak amplitude of the input or output signal used in the system.

In case a converter with a large number of bits is used, then the peak-to-peak signal amplitude can be approximated by:

$$A_{pp} = 2^n q_s. \tag{1.9}$$

The rms signal value A_{rms} of sine wave signal with amplitude A_{pp} can be calculated as:

$$A_{rms} = \frac{2^n q_s}{2\sqrt{2}}. \tag{1.10}$$

The signal-to-noise ratio (S/N) corresponding to the dynamic range of a converter can be calculated using equation 1.10 divided by the square root of equation 1.7, resulting in:

$$S/N = 2^n\sqrt{1.5}. \tag{1.11}$$

Converting equation 1.11 into decibels results in:

$$S/N = n\ 6.02 + 1.76\ \text{dB}. \tag{1.12}$$

It must be noted that converters with resolutions between 1 and 4 bits show a deviation concerning the dynamic range with respect to formula 1.12. A more accurate analysis of the dynamic range of such converters will be performed in one of the following sections.

Formula 1.12 shows that the dynamic range of a system increases by 6 dB when an extra bit is added.

By definition: The dynamic range of a system is equal to the signal-to-noise ratio of that system measured over a bandwidth equal to half the sampling frequency.

The dynamic range of a 16-bit digital audio system can be found by inserting $n = 16$ into formula 1.12. We obtain S/N = 98.1 dB.

The quantization error in a non-correlated sampled system can be modeled by a random process like noise. Many times quantization errors are called quantization noise, but always keep in mind that it is an error signal!

It is therefore very useful to express formula 1.7 as a noise density per unit bandwidth ($e^2_{qns}(f)$):

$$e^2_{qns}(f) = \frac{q_s^2}{12 f_{qns}} = \frac{q_s^2}{6 f_s}. \tag{1.13}$$

Here f_{qns} is the quantization noise bandwidth and f_s is the sample frequency.

Because the signal-to-noise ratio in a system is calculated over a bandwidth equal to half the sampling frequency, the following relation is used: $f_{qns} = \frac{1}{2} f_s$.

The signal-to-noise ratio as density derived from 1.11 becomes:

$$S/N(f) = 2^{n-1}\sqrt{3 f_s}. \tag{1.14}$$

The signal-to-noise ratio of a system with a bandwidth equal to f_{sig} is found by dividing equation 1.14 by $\sqrt{f_{sig}}$. The result becomes:

$$S/N_{system} = 2^{n-1}\sqrt{3\frac{f_s}{f_{sig}}}. \tag{1.15}$$

It is very advantageous to use formula 1.15 for dynamic range calculations of systems that do not use Nyquist sampling.

1.5 Oversampling of converters

When in a system the sampling frequency is made much higher than the maximum signal frequency, this operation is called "oversampling." The quantization error in this case is randomized over a larger frequency band. As a result the quantization noise density is reduced and the effective resolution of the system increases when the system bandwidth is kept equal to the bandwidth of a Nyquist sampled system using the lower sampling frequency.

Using formula 1.15 we have an expression for the signal-to-noise ratio of the oversampled system:

$$S/N_{system} = 2^{n-1}\sqrt{3}\sqrt{\frac{f_s}{f_{sig}}}, \tag{1.16}$$

or in decibels we get

$$S/N = n \times 6.02 - 1.25 + 10 \log \frac{f_s}{f_{sig}} \text{ dB}. \tag{1.17}$$

As an example the dynamic range of a four times oversampled system will be calculated. By inserting $\frac{f_s}{f_{sig}} = 8$ into formula 1.17, the result becomes:

$$S/N = (n+1) \times 6.02 + 1.76 \text{ dB}. \tag{1.18}$$

Comparing this result with formula 1.12, it can be seen that the dynamic range increases by 6 dB or 1 bit. In Figure 1.5 a graphical approach to

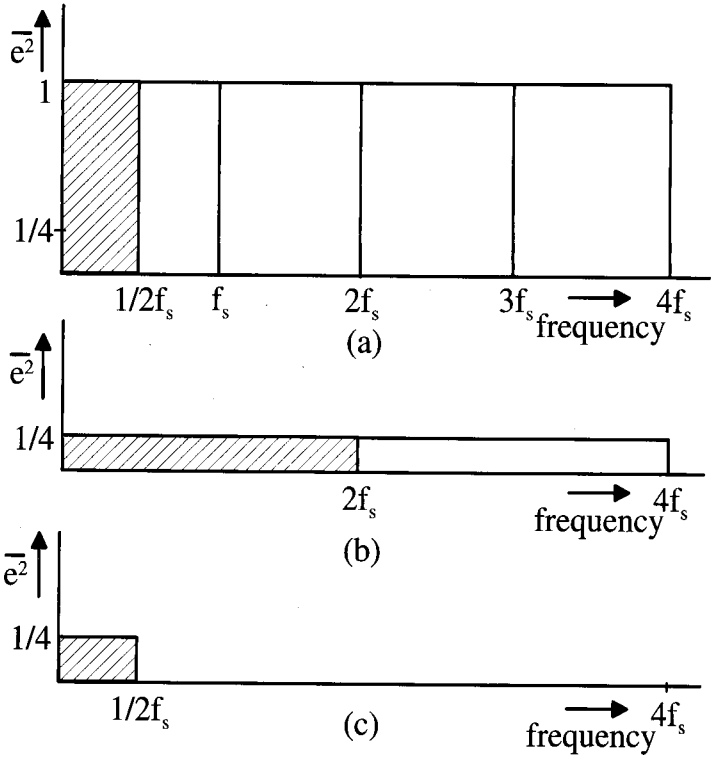


Figure 1.5: (a) Quantization error of a Nyquist sampled converter system (b) Quantization error of a four times oversampled converter system (c)Quantization error resulting after bandwidth limitation

the oversampling of converters is shown. Note the reduction in quantization noise density of the oversampled system. The total quantization error shown as shaded areas is equal for both systems because the same number of bits is used. In the dashed areas signals appear that are introduced by the sampling process. For simplicity only the frequency range from zero to f_s or $4f_s$ is shown in the figure. The sampling operation introduces replica of the frequency spectra at multiples of the sampling frequency, too. Usually these

replica do not add additional information to the picture and are therefore omitted. This omission is introduced in the following figures as well. When the signal bandwidth is kept at $\frac{1}{2}f_s$, the total quantization error is reduced with a factor four in figure (c), and the increase in resolution with 1 bit is obtained.
It must be noted, however, that the improvement in resolution is only obtained as long as the linearity of the converter is at least equal to the dynamic range obtained by oversampling. In case the linearity of the converter is limited, then the improvement in signal-to-quantization error is obtained, but distortion components will NOT be reduced due to oversampling!
Furthermore, distortion in an oversampled system using the same signal bandwidth can still be smaller compared to a Nyquist sampled system. This can be explained by supposing that a signal frequency close to half the sampling frequency of the Nyquist system is applied. In the Nyquist sampled system large quantization steps of nearly full scale occur. Such large steps result in, for example, slewing of the output amplifier in a D/A converter system or slewing of the sample-and-hold amplifier in an A/D converter system. This slewing results in a nonlinear operation of a part of the circuit giving distortion. When a large oversampling is used, then the quantization steps are reduced with a factor nearly equal to the oversampling ratio. In this case slewing of amplifiers can be avoided and a lower distortion in the system is obtained.

1.6 Quantization error spectra

Up until now quantization has been seen as an error power that reduces the dynamic range of a converter system. To obtain information about quantization error frequency components that might have an influence on harmonic distortion and inter modulation distortion in case more signals are applied, the following analysis will be used. Suppose an analog ramp signal is quantized as shown in Fig. 1.6, then the error signal can be determined as a sawtooth with amplitude q_s and 2^n repetitions as shown in Fig. 1.7.
Note that at this moment ONLY AMPLITUDE QUANTIZATION is used. SAMPLING of the signal will be performed at a later stage. This means that there exists NO Nyquist bandwidth limitation during this analysis.
By shifting the DC value of the signal as shown in Fig. 1.7 then a Fourier analysis of that signal gives only odd harmonics described as:

$$q_{error} = y(x) + \sum_{m=1}^{\infty} \frac{1}{m\pi} \sin 2m\pi x. \tag{1.19}$$

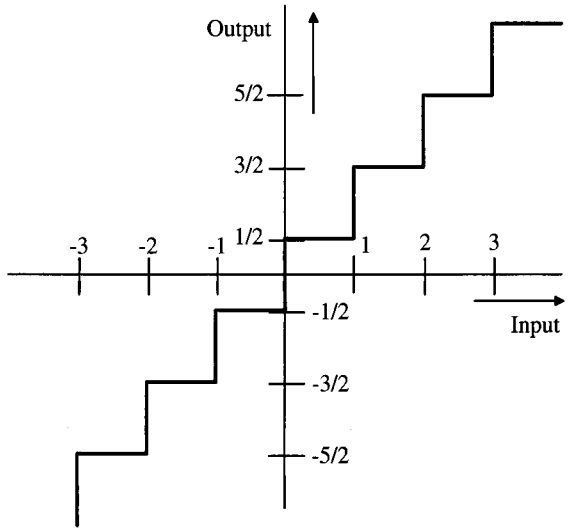


Figure 1.6: Quantized "Ramp" Signal

In case a sine wave is applied then the output spectrum becomes more

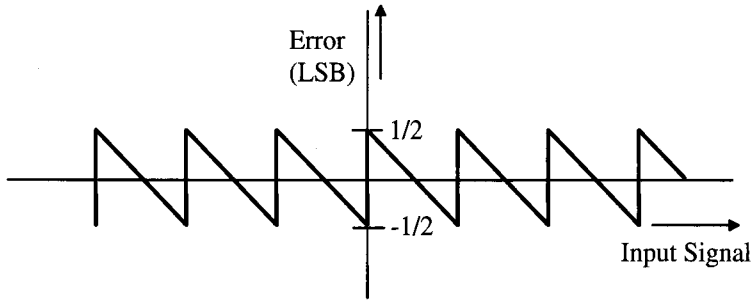


Figure 1.7: Sawtooth Error Signal

complex. The error signal will get a kind of frequency modulation. From [110] we obtain:

$$y = A \sin \Phi + Im \left(\sum_{m=1}^{\infty} \sum_{p=-\infty}^{\infty} \frac{1}{m\pi} J_p(2m\pi A) e^{jp\Phi} \right) \tag{1.20}$$

Simplifying this equation we get:

$$y = \sum_{p=1}^{\infty} A_p \sin p\Phi. \tag{1.21}$$

With A_p defined by:

$$A_p = \delta_{p1} A + \sum_{m=1}^{\infty} \frac{2}{m\pi} J_p(2m\pi A) \quad \text{p = odd} \tag{1.22}$$

$$A_p = 0 \quad \text{p = even,} \tag{1.23}$$

$$\delta_{p1} = 1 \quad \text{p = 1,} \tag{1.24}$$

$$\delta_{p1} = 0 \quad \text{p} \neq 1. \tag{1.25}$$

The amplitude of the harmonic with index p is given by A_p from equation 1.22.
In an n-bit converter the sine wave amplitude using a unit step size becomes:

$$A = \frac{2^n - 1}{2} \approx 2^{n-1}. \tag{1.26}$$

Inserting this amplitude into equation 1.22 then the amplitude of the frequency component A_p becomes:

$$A_p = \delta_{p1} 2^{n-1} + \sum_{m=1}^{\infty} \frac{2}{m\pi} J_p(2m\pi 2^{n-1}) \quad \text{p = odd} \tag{1.27}$$

The quantization error spectra can be plotted using 1.27. In Fig. 1.8 a spectrum with up to 30.000 odd components of a 10-bit quantizer is shown. The spectrum slowly decreases with increasing number of harmonics and has a length of infinity. The spectrum shows furthermore peaks that can mathematically be determined to occur at the $2^n\pi = 3217^{th}$ harmonic of the input signal. A more detailed part of the frequency spectrum of the same quantizer of Fig. 1.8 is shown in Fig. 1.9. Lower order odd harmonic amplitudes can be estimated from this figure. Third harmonic is about 90 dB down with respect to full scale. The ratio between for example the third harmonic component and the fundamental sine wave for an n-bit converter becomes:

$$A_{3,1} = \frac{\sum_{m=1}^{\infty} \frac{2}{m\pi} J_3(2m\pi 2^{n-1})}{2^{n-1} + \sum_{m=1}^{\infty} \frac{2}{m\pi} J_1(2m\pi 2^{n-1})}. \tag{1.28}$$

This result for the third order distortion can be simplified as:

$$A_{3,1} = 2^{-n\frac{3}{2}} \quad (n \geq 1). \tag{1.29}$$

As a result a 10-bit converter has a third order distortion component 90 dB down with respect to full scale. Increasing the resolution of the converter with 1-bit, then the distortion component reduces with $2^{\frac{3}{2}} = 9$ dB.

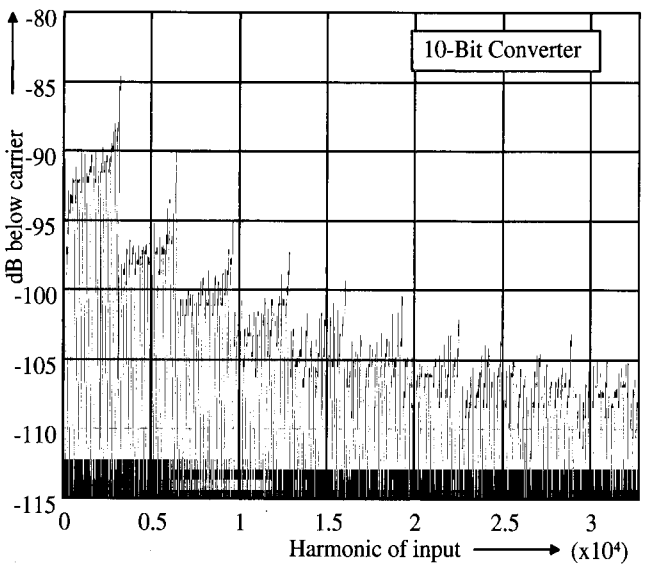


Figure 1.8: 10-bit quantizer spectrum with 30.000 components

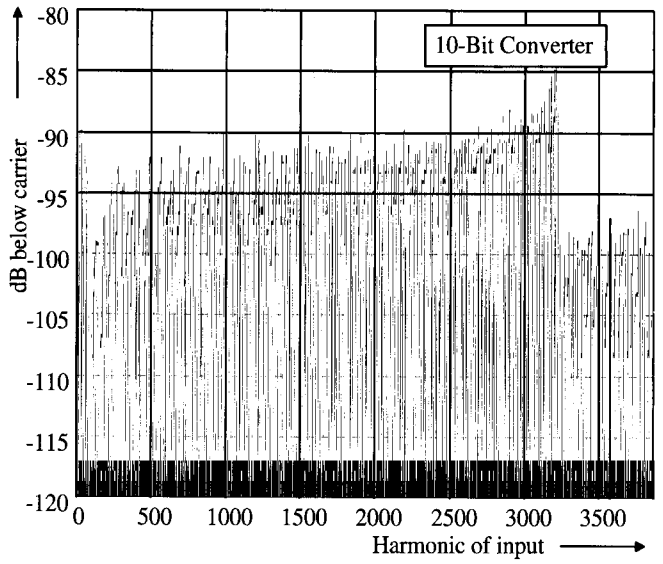


Figure 1.9: 10-bit quantizer spectrum with 3500 components

1.7 Amplitude dependence of quantization components

So far the calculation of the quantization spectra has been performed for signals exactly fitting within the quantization levels. In case a signal varies within a quantization level then the total spectrum changes. Suppose that the amplitude varies as ΔA [0 1], then equation 1.27 is modified into:

$$A_p = \sum_{m=1}^{\infty} \frac{2}{m\pi} J_p(m\pi(2^n - \Delta A)) \quad \text{odd } p \neq 1. \tag{1.30}$$

Taking as an example p=3 and p=31 then the result for a 6-bit converter is shown in Fig. 1.10. This figure (1.10) shows that depending on the signal

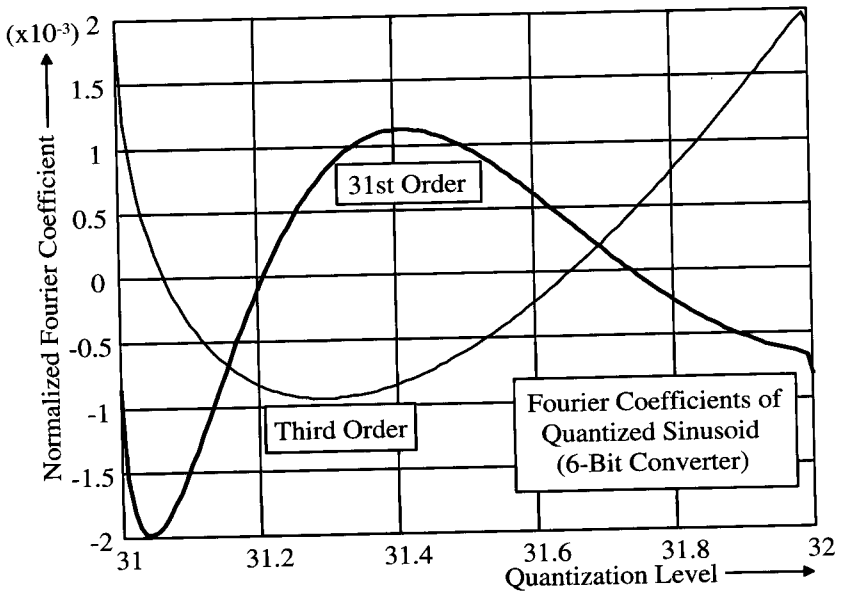


Figure 1.10: Distortion variation within a quantization step

amplitude distortion components can be reduced to zero. Maximum third order distortion is found roughly at the quantization levels.

1.8 Multiple signal distortion

At the moment two or more signals are quantized, then it is important to know what the so called cross-modulation or inter modulation products (IM3) will be. A formula for two input signals will be given.
Suppose we apply the following signals

$$x(t) = A(t)\sin\Phi(t) + a(t)\sin\phi(t). \tag{1.31}$$

Using the previously described analysis and using some mathematical manipulations we get for the cross-modulation:

$$y = \sum_{p+q=odd>0}^{\infty} A_{pq}\sin(p\Phi + q\phi) \tag{1.32}$$

$$A_{pq} = \delta_{p1}\delta_{q0}A + \delta_{p0}\delta_{q1}a + \sum_{n=1}^{\infty}\frac{2}{n\pi}J_p(2n\pi A)J_q(2n\pi a). \tag{1.33}$$

With

$$A = \frac{2^n - 1}{4} \approx 2^{n-2} \quad \text{and} \quad a = \frac{2^n - 1}{4} \approx 2^{n-2} \tag{1.34}$$

the inter modulation product as a function of the number of bits in a converter becomes:

$$A_{pq} = \sum_{n=1}^{\infty}\frac{2}{n\pi}J_p(2n\pi 2^{n-2})J_q(2n\pi 2^{n-2}). \tag{1.35}$$

In Fig. 1.11 the full error spectrum of an 8-bit quantizer with a two-tone input signal is shown. From this figure it is seen that the spectrum is more flat compared to a single tone spectrum. A detailed part of Fig. 1.11 shows that more spectral components are generated with repetitions equal to the difference in signal frequency (in this special case a frequency difference of 0.0625). A smaller amplitude per component is obtained. The inter modulation distortion can be determined referred to the amplitude of one signal component. We obtain:

$$A_{21,1} = \frac{\sum_{n=1}^{\infty}\frac{2}{n\pi}J_2(2n\pi 2^{n-2})J_1(2n\pi 2^{n-2})}{2^{n-2} + \sum_{n=1}^{\infty}\frac{2}{n\pi}J_1(2n\pi 2^{n-2})J_0(2n\pi 2^{n-2})}. \tag{1.36}$$

Again this complex equation can be simplified into:

$$A_{21,1} = 2^{-2n}(\text{n} \geq 1). \tag{1.37}$$

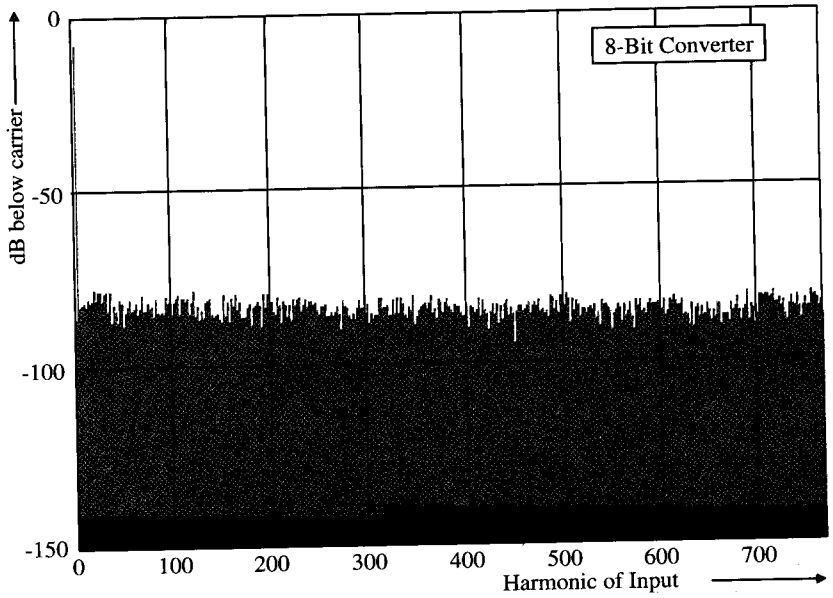


Figure 1.11: Two-tone 8-bit quantization error spectrum

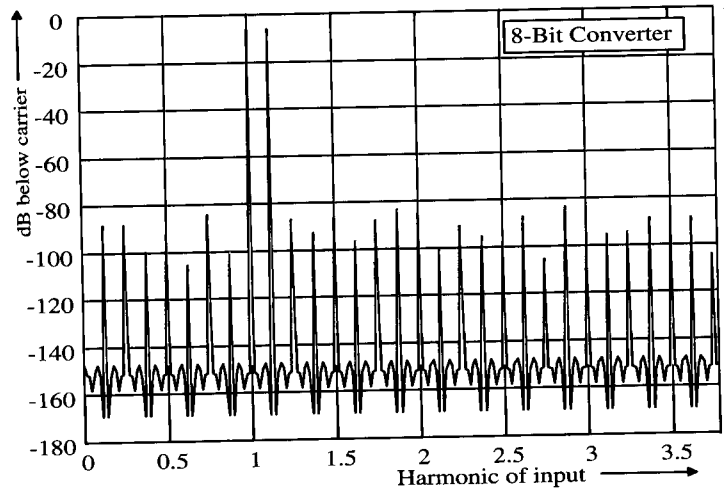


Figure 1.12: Detail of two-tone 8-bit quantization error spectrum

With A_{21} the frequency component $2p - q$ is denoted.
This means that with an increase in resolution of 1-bit, the inter modulation product will decrease with 12 dB.
Quantization of analog signals results in errors that are correlated with the signal mostly as odd harmonics of the signal. The analyzed spectra show basically an infinite number of spectral components. In Fig. 1.13 signal to quantization error, signal to third order distortion and the signal to inter modulation component (IM3) as a function of the number of bits are shown. From Fig. 1.13 it can be seen that ideal converters with resolutions above

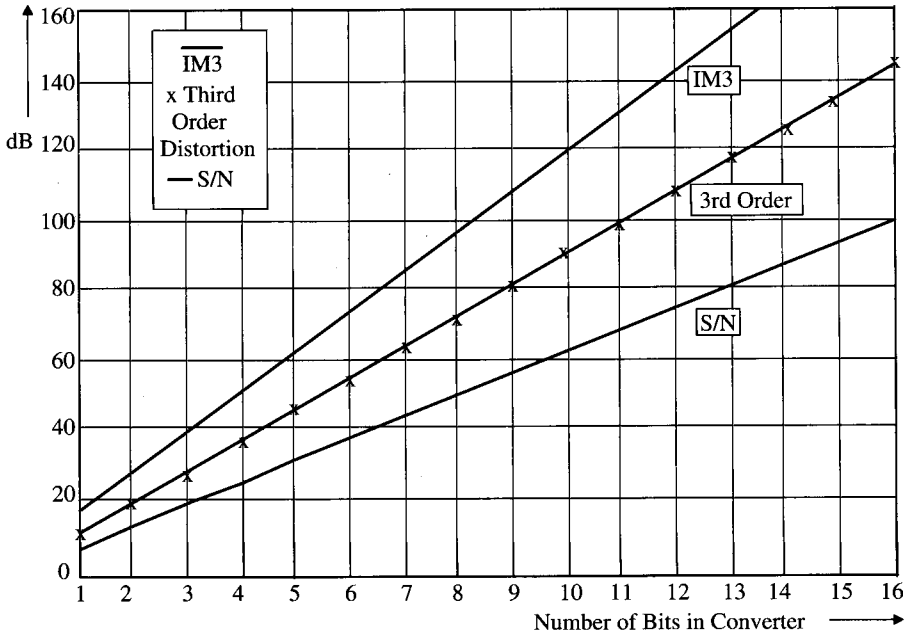


Figure 1.13: S/N, Third order distortion and IM3 of Quantizers

10-bit show distortion and inter modulation components due to quantization that practically can be ignored.

1.9 Accurate dynamic range calculation

As mentioned before, the calculation of the dynamic range of converters with a resolution between 1 to 4 bits deviates from the general formula:

$$S/N = n\ 6.02 + 1.76 \ \text{dB}. \tag{1.38}$$

A special case of a 1-bit converter can be simply calculated.
Suppose a single bit digital-to-analog converter reproduces an analog signal. The output signal has no DC component. This results in an amplitude of the D/A converter of $\frac{1}{2}$. The power of the D/A converter now equals:

$$P_{DA} = \frac{1}{4} \tag{1.39}$$

The amplitude of the reproduced fundamental signal using a Fourier series equals $\frac{2}{\pi}$. The rms signal power of the fundamental becomes:

$$P_{signal} = \frac{2}{\pi^2} \tag{1.40}$$

As a result the quantization error power becomes:

$$P_{quantization} = P_{DA} - P_{signal} = \frac{1}{4} - \frac{2}{\pi^2} \tag{1.41}$$

The signal-to-noise ratio of the single bit converter becomes:

$$S/N_{1-bit} = \sqrt{\frac{P_{signal}}{P_{quantization}}} = \frac{1}{\sqrt{\frac{\pi^2}{8} - 1}}. \tag{1.42}$$

So $S/N_{1-bit} = 6.31$ dB.
Using S/N = n 6.02 + 1.76 dB we obtain $S/N_{1-bit} = 7.78$ dB for the converter.
Because the amplitudes of the quantization error components are known from the previous analysis, it is possible to derive a general formula that describes accurately the dynamic range of an n-bit converter.
The fundamental signal amplitude for an n-bit converter (p=1) is:

$$A_1 = 2^{n-1} + \sum_{m=1}^{\infty} \frac{2}{m\pi} J_1(2m\pi 2^{n-1}). \tag{1.43}$$

Then the total quantization error can be calculated as the sum of the power of all odd harmonics. The odd harmonics are obtained when p is replaced by p = 2q + 1 with q = 1 to infinity.

$$A_{quantization} = \sqrt{\sum_{q=1}^{\infty} (\sum_{m=1}^{\infty} \frac{2}{m\pi} J_{2q+1}(2m\pi 2^{n-1}))^2} \tag{1.44}$$

number of bits n	S/N Accurate dB	S/N n 6.02 + 1.76 dB
1	6.31	7.78
2	13.30	13.80
3	19.52	19.82
4	25.59	25.84
5	31.65	31.86
6	37.70	37.88
7	43.76	43.90
8	49.82	49.92
9	55.87	55.94
10	61.93	61.96

Table 1.1: S/N as a function of the number of bits n

The signal-to-noise of an n-bit converter is accurately modeled with:

$$S/N(n) = \frac{A_1}{A_{quantization}} = \frac{2^{n-1} + \sum_{m=1}^{\infty} \frac{2}{m\pi} J_1(2m\pi 2^{n-1})}{\sqrt{\sum_{q=1}^{\infty} (\sum_{m=1}^{\infty} \frac{2}{m\pi} J_{2q+1}(2m\pi 2^{n-1}))^2}} \tag{1.45}$$

To evaluate equation 1.45 a lot of computing power is needed. The final results of this analysis compared to the simplified formula of S/N = n 6.02 + 1.76 dB is shown in table 1.1. From this table it can be seen that for converters with resolutions of 1 and 2 bits a significant difference exists between the accurate calculation and the "general" accepted formula.

1.10 Sampling time uncertainty

Sampling time uncertainty introduces additional errors when analog signals are sampled at equal time intervals and reconstructed at time intervals that show a timing uncertainty or vice versa. Sampling clocks show short term and long term time jitter. Especially the short term time jitter has influence on the performance of a converter. The slope of the signals applied to a converter system convert the sampling clock jitter into a noise like error that reduces the dynamic range or introduces distortion. To obtain quantitative insight into the problem of sampling time uncertainty, suppose that a sine wave close to half the sampling frequency is applied to an A/D converter. The maximum slope of the input signal occurs at the zero crossing of the

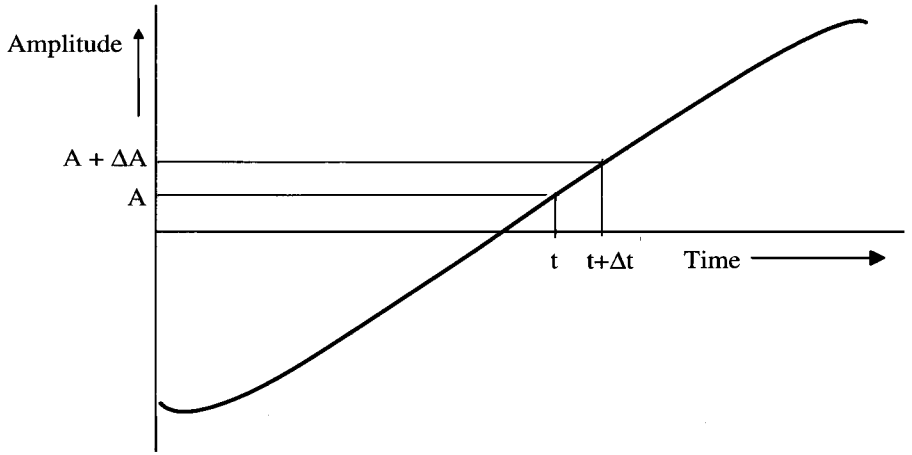


Figure 1.14: Sampling time uncertainty calculation model

signal as shown in Figure 1.14. If the sampling time moment varies between t and $t + \Delta t$, then an amplitude variation between A and $A + \Delta A$ is obtained. The peak-to-peak amplitude variation ΔA must be at maximum equal to the quantization step q_s of the converter to avoid a significant loss in quantization resolution of the converter. Note that the quantization step q_s is equal to the Least Significant Bit (LSB) value of the converter.

Suppose furthermore that the converter has a binary weighting with n bits, then the number of quantization levels is equal to $2^n - 1$. When $n \gg 1$, the number of levels can be approximated by 2^n.

The sampling time uncertainty Δt must be so small that the LSB amplitude level is not exceeded for signals with a bandwidth equal to half the sampling frequency .

With a sine wave input of $V_{in} = A \sin \omega t$ we obtain for the sampling time uncertainty:

$$\Delta t = \frac{\Delta A}{A\omega \cos \omega t}, \tag{1.46}$$

and with

$$\Delta A = \frac{2A}{2^n}, \tag{1.47}$$

the result becomes:

$$\Delta t = \frac{2^{-n}}{\pi f_{in} \cos 2\pi f_{in} t}. \tag{1.48}$$

Here $2A$ = peak-to-peak amplitude of the signal, $\omega = 2\pi f_{in}$ and f_{in} is the input signal frequency.

Formula 1.48 shows that the sampling time uncertainty depends on the moment the input signal is sampled (t is still in the equation!). The tightest specification for the sampling time uncertainty is obtained when $t = 0$.

Inserting $t = 0$ into formula 1.48 results in:

$$\Delta t_{max} = \frac{2^{-n}}{\pi f_{in}}. \tag{1.49}$$

As an example the sampling time uncertainty is calculated for a 16-bit digital audio system with an input frequency f_{in} of 20 kHz. Inserting these values into equation 1.49 gives a time uncertainty (Δt) of less than $\frac{1}{4}$ nsec. With f_{in} = 5 MHz and n = 10 bit, the peak-to-peak clock uncertainty must be below 65 psec.

1.10.1 Reduction of ENOB by sampling clock jitter

However, we want to know the influence of the RMS clock jitter on the Effective Number Of Bits (ENOB's) of a converter. With ENOB defined as:

$$ENOB = \frac{SNDR_{effective} - 1.76}{6.02} \tag{1.50}$$

Here $SNDR_{effective}$ is the "measured" effective resolution of a converter in dB and includes all the non-ideality effects of a practical converter.
The error power due to jitter equals:

$$\Delta A^2 = q_s^2 2^{2n} f_{sig}^2 \pi^2 \cos^2(2\pi f_{sig} t) \Delta t^2. \tag{1.51}$$

In this power equation the slope of the signal determines the sensitivity of the converter to clock jitter. We can average this slope over the signal period and get:

$$\frac{1}{\pi} \int_0^{\pi} \cos^2 \phi d\phi = \frac{1}{2}. \tag{1.52}$$

Inserting 1.52 into 1.51 gives:

$$\Delta A^2 = q_s^2 2^{2n-1} f_{sig}^2 \pi^2 \Delta t^2 = q_s^2 2^{2n-1} \pi^2 \frac{\Delta t^2}{T_{sig}^2}. \tag{1.53}$$

With $f_{sig} = \frac{1}{T_{sig}}$.
The total error power due to quantization and jitter becomes:

$$q^2_{total} = \frac{q_s^2}{12} + \Delta A^2 = \frac{q_s^2}{12}(1 + k_j^2). \tag{1.54}$$

Where k_j defined as:

$$k_j^2 = \frac{\Delta A^2}{\frac{q_s^2}{12}} \tag{1.55}$$

Using equation 1.54 we can rearrange equation 1.55 and obtain for k_j:

$$k_j = 2^n \pi \sqrt{6} \frac{\Delta t}{T_{sig}}. \tag{1.56}$$

We will call $\Delta t = T_{jitter}$ the sample clock phase noise (rms).
The dynamic range of the converter due to clock jitter noise power N_j

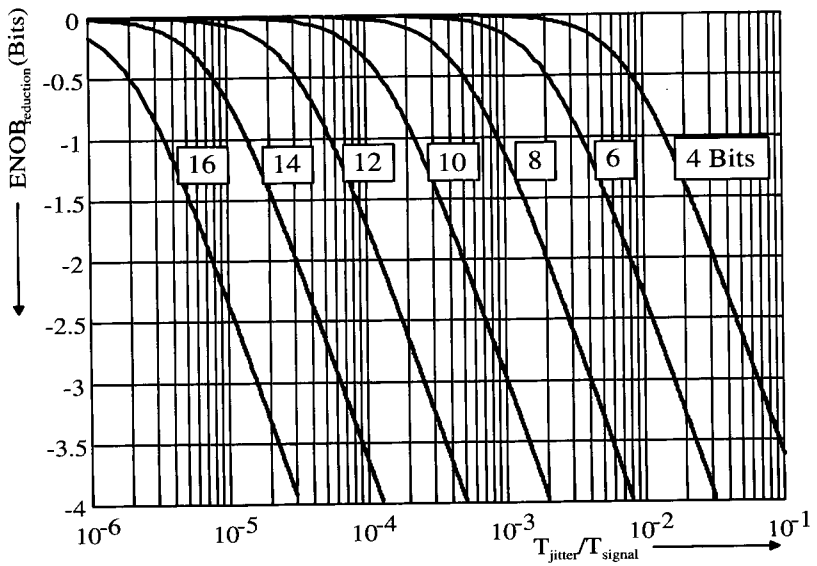


Figure 1.15: Reduction in ENOB's versus $\frac{T_{jitter}}{T_{sig}}$

changes according to:

$$\frac{S}{N + N_j} = \frac{S}{N} \cdot \frac{N}{N + N_j} = \sqrt{1.5}\, 2^n\, 2^{-\frac{\log(1+k_j^2)}{2\log 2}} \tag{1.57}$$

The reduction in ENOB's as a result of jitter then equals:

$$n_{reduction} = \frac{\log(1 + k_j^2)}{2\log 2}. \tag{1.58}$$

If $k_j = 1$ then the ENOB's reduce with $\frac{1}{2}$ bit or 3 dB. The timing accuracy with an ENOB reduction of $\frac{1}{2}$ bit or 3 dB becomes:

$$\Delta t = T_{jitter} = \frac{2^{-n}}{\pi\sqrt{6}} T_{sig} \text{ with } k_j = 1 \text{ (rms)}. \tag{1.59}$$

The ratio between the clock jitter and the signal frequency can be calculated as a function of the number of bits in the converter. In Fig. 1.15 the decrease in ENOB's as a function of $\frac{T_{jitter}}{T_{sig}}$ is shown for converters having a resolution between 4 and 16 bits.

1.11 Sampling clock time uncertainty

It is difficult to obtain information about the time uncertainty of clock generators. In this section a simple model will be introduced to obtain an estimation of the pulse-to-pulse time uncertainty of a sampling clock generator. In general it can be said that a sine wave that is generated by a highly frequency selective element shows a high stability. Suppose now that a nearly ideal sine wave $V_{cl} = A \sin \omega t$ is generated. When a highly frequency selective element is used then the (white) noise generation added to the sine wave is very small. Mostly a square wave is required as a clock signal in sampled data system. This square wave generation is obtained by applying the sine wave signal V_{cl} to a squaring circuit. Such a squaring circuit, however, generates white noise with a bandwidth equal to the squaring amplifier bandwidth f_b. The addition of the wide-band noise results in a pulse-to-pulse time uncertainty which is determined by the noise amplitude and the slope of the sine wave input signal. In Figure 1.16 the simplified calculation model is shown. In Figure 1.16 e_n represents the (rms) white noise generated by the squaring system. Mostly e_n is thermal noise and can be expressed as:

$$e_n^2 = 4kTR_n\Delta f. \tag{1.60}$$

R_n represents the equivalent noise resistance of the squaring circuit.

The time uncertainty can be calculated. Differentiating V_{cl} we obtain for the time uncertainty:

$$\Delta t = \frac{e_n}{2\pi f_{cl} A \cos 2\pi f_{cl} t}. \tag{1.61}$$

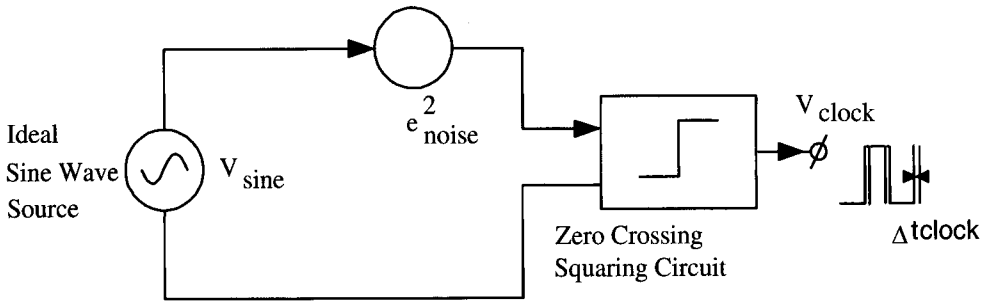


Figure 1.16: Clock time uncertainty model

The maximum sensitivity of the squaring circuit is found at the zero crossing of the sine wave which corresponds to $\cos 2\pi f_{cl} t = 1$. Furthermore, noise equation 1.60 gives the rms value corresponding to 1σ. To obtain the total 1σ time uncertainty the result of equation 1.61 must be doubled. We obtain for the clock time uncertainty $\Delta\, t_{cl}$:

$$\Delta t_{cl} = \frac{e_n}{\pi f_{cl} A}. \tag{1.62}$$

Equation 1.62 shows that with a constant value of noise e_n the time uncertainty will decrease with increasing clock frequency f_{cl}. When we suppose that the squaring circuit has a single time constant with a bandwidth f_b then 1.60 can be inserted in 1.62, resulting in:

$$\Delta t_{cl} = \frac{\sqrt{2\pi k T R_n f_b}}{\pi f_{cl} A}. \tag{1.63}$$

Note that the noise-bandwidth of a first order system is equal to:

$$f_{noise} = \frac{\pi}{2} f_b. \tag{1.64}$$

In 1.64 f_{noise} is the noise bandwidth of the system.

Furthermore, in amplifier systems a general relation exists between the rise time t_r of the output pulse and the bandwidth f_b:

$$f_b \times t_r \approx 0.35. \tag{1.65}$$

Inserting 1.65 into 1.63 results in:

$$\Delta t_{cl} = \frac{\sqrt{0.7 k T R_n}}{f_{cl} A \sqrt{\pi t_r}}. \tag{1.66}$$

Suppose we have an ideal 50 Ohm system and we want to generate a clock signal with a rise time of 250 psec and a repetition rate of 10 MHz. With a sine wave amplitude of 0.5 V an rms clock time uncertainty of 2.7 psec is obtained.

1.12 Conversion systems

When an analog-to-digital or digital-to-analog converter is applied in a complete system using digital signal processing then extra components must be added. In Fig. 1.17(a) an A/D converter system is shown while Fig. (b) shows a D/A system. The filters at the input of the analog-to-digital con-

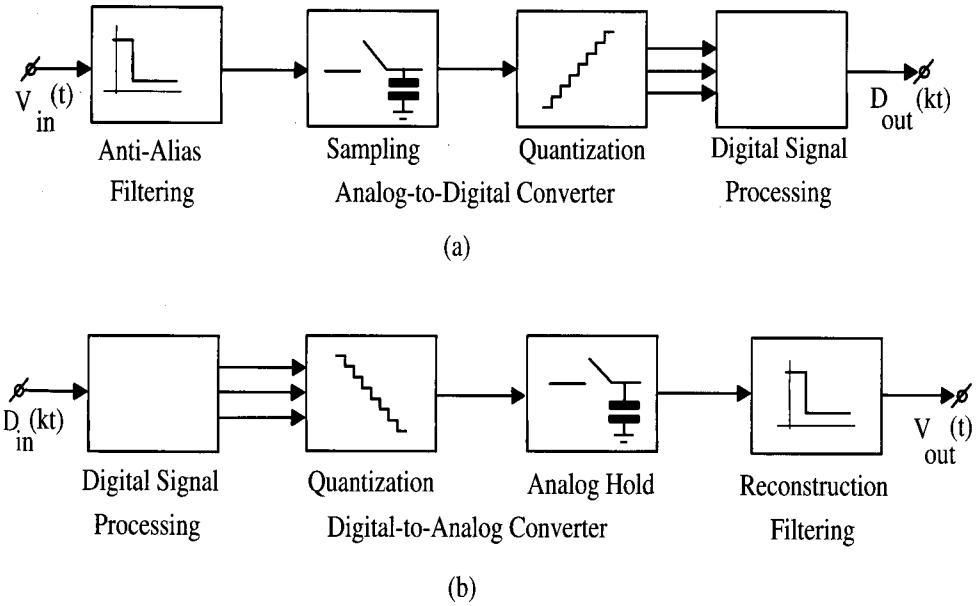


Figure 1.17: A/D converter system (a) and D/A converter system (b)

verter limit the input signal band. In many case this signal band is a low-pass band, but bandpass applications are possible too. In the bandpass case the high frequency band is converted into a low-pass frequency band and then converted into a digital value. Such an operation is called sub sampling. When the sample-and-hold amplifier shows a good high frequency performance then the sub sampling operation is performed with low distortion. Bandpass signals can be converted into low-pass signals. Such applications occur mostly in radio receivers.

In Fig. 1.17(b) the reconstruction of a signal takes place. To eliminate the high-frequency sampled signals a low-pass filter is applied. The stopband attenuation of such a filter depends on the required performance and on the system to which the output terminal is connected. Again a bandpass filter can be used to filter out at the required carrier frequency the band of interest. As will be discussed in the next sections, the performance of the filters in A/D and D/A converter systems have a strong influence on the total performance of such a system. First aliasing will be discussed.

1.12.1 Sampling with no-aliasing

In case a signal with a bandwidth smaller than the Nyquist bandwidth $\leq \frac{f_s}{2}$ is sampled with a sampling frequency f_s then no aliasing will occur. In Fig. 1.18 this operation is shown. Analyzing Fig. 1.18(a) we see, that outside

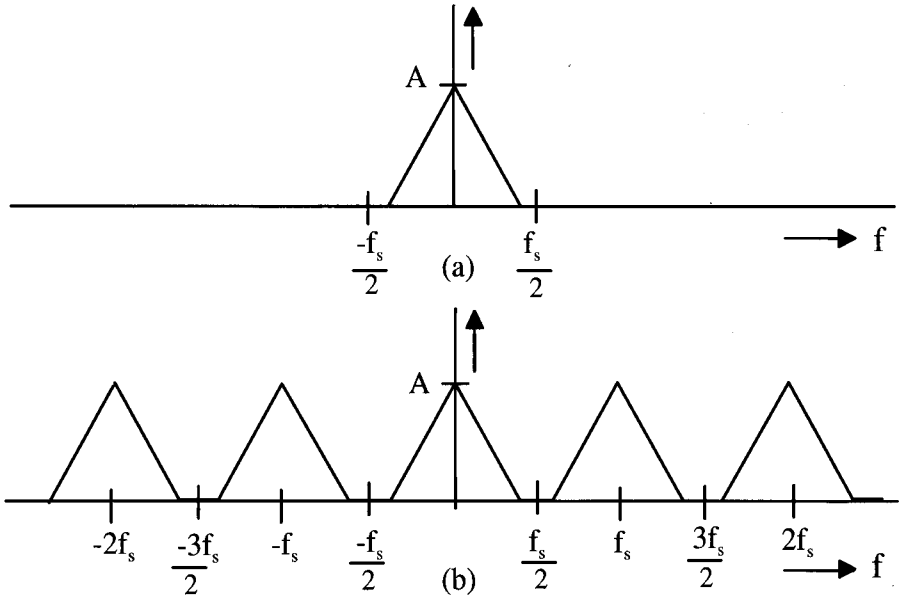


Figure 1.18: Input signal band (a) and sampled signal spectrum (b)

the band $-\frac{f_s}{2}$ to $\frac{f_s}{2}$ no signal is present. When this signal is sampled with f_s then the repetitions of the signal band around multiples of the sampling frequency appear. It can be expected that filtering out only the signal band of interest and having no disturbance outside this band is a difficult and might be a costly operation. Sharp filters are needed with large stopband attenuation. What is happening in case aliasing occurs will now be shown.

1.12.2 Sampling with aliasing

In case the sampling frequency is not chosen high enough or in case the filtering functions have a limited stop band attenuation, then aliasing occurs. In Fig. 1.19 this operation is shown. From Fig. 1.19(b) it is seen that in

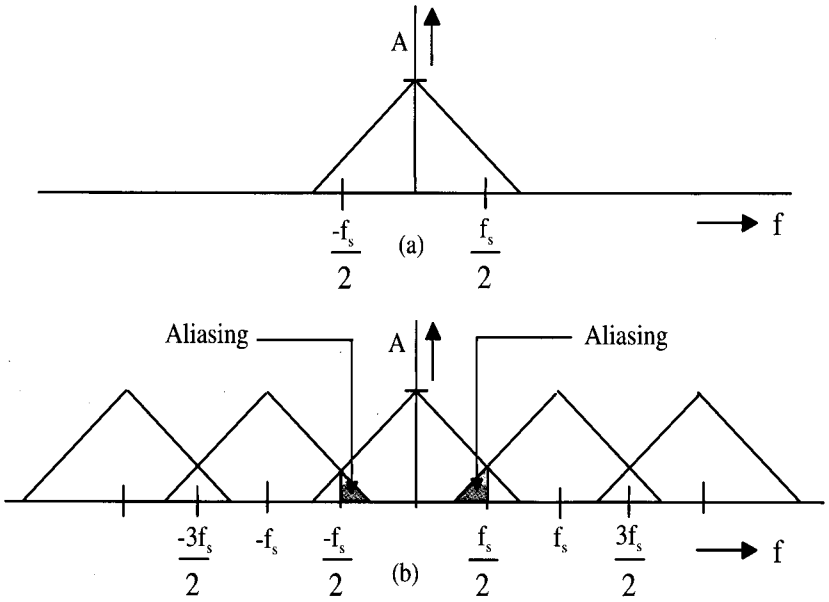


Figure 1.19: Input signal band (a) and sampled signal spectrum (b)

case a frequency band larger than half the sampling frequency is sampled, the signal part above $\frac{f_s}{2}$ is aliased in the base band. This aliasing is a process that never can be reversed. In this case distortion occurs that is not allowed. Therefore a higher sampling frequency or a smaller signal band need to be applied to the converter system. In some cases there is no manner that the aliasing can be avoided. This occurs in the case of the wide-band quantization error spectrum in an analog-to-digital or digital-to-analog converter. All spectrum components above half the sampling frequency will be aliased into the baseband. Such an operation shows a large amount of spectral components having a noise like behavior.

1.12.3 Sampling of quantization errors

The sampling of quantization errors occurs always in an analog-to-digital or digital-to-analog converter. In Fig. 1.20 the sampling of the quantization

error spectrum is shown. From this figure it can be seen that all error

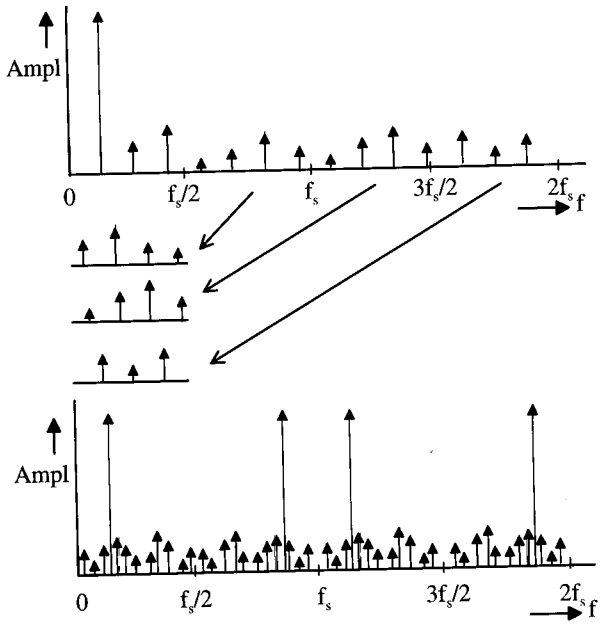


Figure 1.20: Sampling of a quantized signal

components above half the sampling frequency are folded back into the base band. To get a good understanding of this operation the frequency band must be extended from $f_s = -\infty \; to \; \infty$. In the figure only half this frequency range is shown, but in that case the signal band between multiples of $\frac{f_s}{2}$ and f_s must be mirrored and then added to the base band. This results in a very large amount of components in the base band and the noise like behavior is found. Furthermore the figure shows, that when a correlation between the signal frequency and the sampling frequency exists, the quantization error components fold back at the multiples of the signal frequency and then add or subtract to give the final quantization error. In the correlated case no components will appear in between the multiples of the signal frequency existing in the base band. However, in this case the total quantization error power in the base band will still be equal to $\frac{q_s^2}{12}$.

1.13 Nyquist filtering in A/D converter systems

In some cases the sampling frequency and the maximum applicable signal frequency are very close to Nyquist. In this case a "brick"wall filtering of the input signal is required to avoid aliasing of high frequency components that do not belong to the signal band. A basic solution to this filtering problem is shown in Fig. 1.21 The shaded area (Figure 1.21(b)) shows the

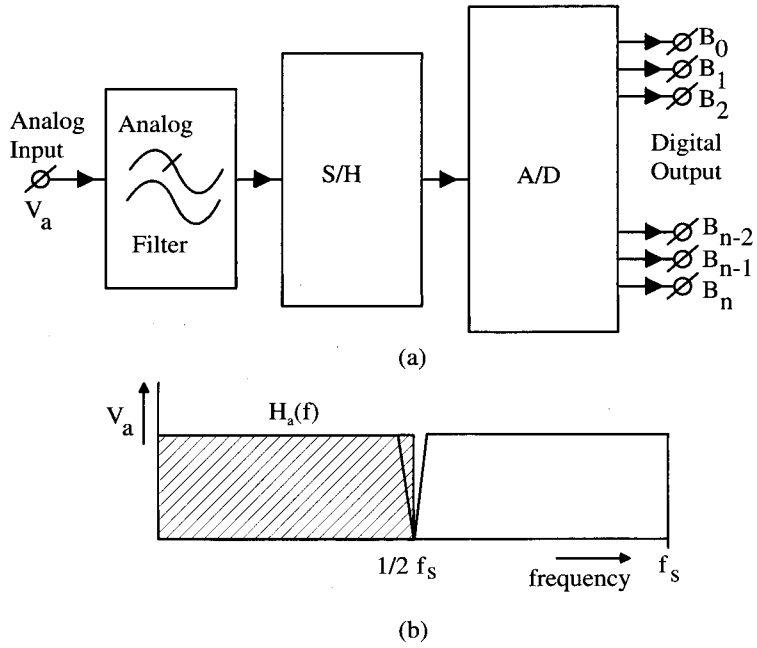


Figure 1.21: (a) A/D converter with "brick"wall filtering (b) Filter response

frequency response $H_a(f)$ of an ideal low-pass filter. The drawn line close to half the sampling frequency shows the transition band of a more practical analog filter. The dashed area indicates the passband region of the input filter. The frequency response of such an ideal low-pass filter is equal to:

$$H_a(f) = 1 \text{ for } |f| < \frac{f_s}{2} \tag{1.67}$$

$$= 0 \text{ for } |f| > \frac{f_s}{2}. \tag{1.68}$$

In systems with a minimum sampling rate f_s compared to the analog bandwidth, a zero transition band of the filter is required. Analog filters with such a steep characteristic mostly have a nonlinear phase characteristic. Higher

order filter structures that are needed to obtain the system performance will be sensitive to component accuracy and are therefore costly and difficult to design. Furthermore, the stop band rejection must be related to the number of bits in the system. Aliasing of these stop band signals should result in errors which are below the quantization noise level.

1.14 Combined analog and digital filter

A combination that overcomes a number of the limitation of Nyquist analog filtering is shown in Fig. 1.22. This system uses a combination of an analog pre-filtering, a digital post-filtering and decimation. This architecture is shown in Figure 1.22. In this system a four times oversampled A/D converter allows the use of a simpler analog nearly linear-phase pre filter to reject the signal band around the high sampling frequency $4f_s$. This simple analog filter is followed by a sample-and-hold amplifier, an analog-to-digital converter and a linear-phase digital filter performing the steep filtering characteristic. In Figure 1.23(a) the frequency characteristic of the analog filter

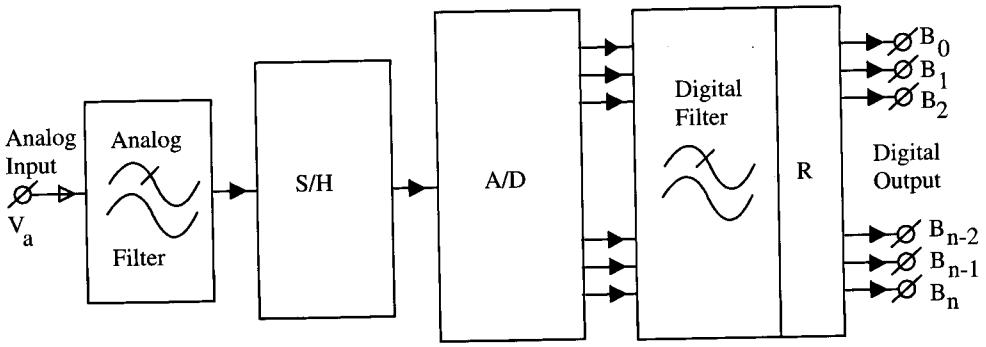


Figure 1.22: (a) A/D converter with combined analog and digital filtering

is shown. The signal after sampling by the analog-to-digital converter is shown in Fig. 1.23(b). As can be seen the sampling operation aliases the high-frequency signal part into the base band. Frequencies between $\frac{f_s}{2}$ and $3.5f_s$ show a large amplitude and must be filtered out. The digital filter performs this steep filtering 1.23(c). Input signals present in the frequency range between $3\frac{1}{2}f_s$ and $4\frac{1}{2}f_s$ are filtered by the analog pre filter. The attenuation of the analog input filter in this frequency band must be so large, that the amplitude of the aliased components is well below the quantization level of the analog-to-digital conversion system. This means that the

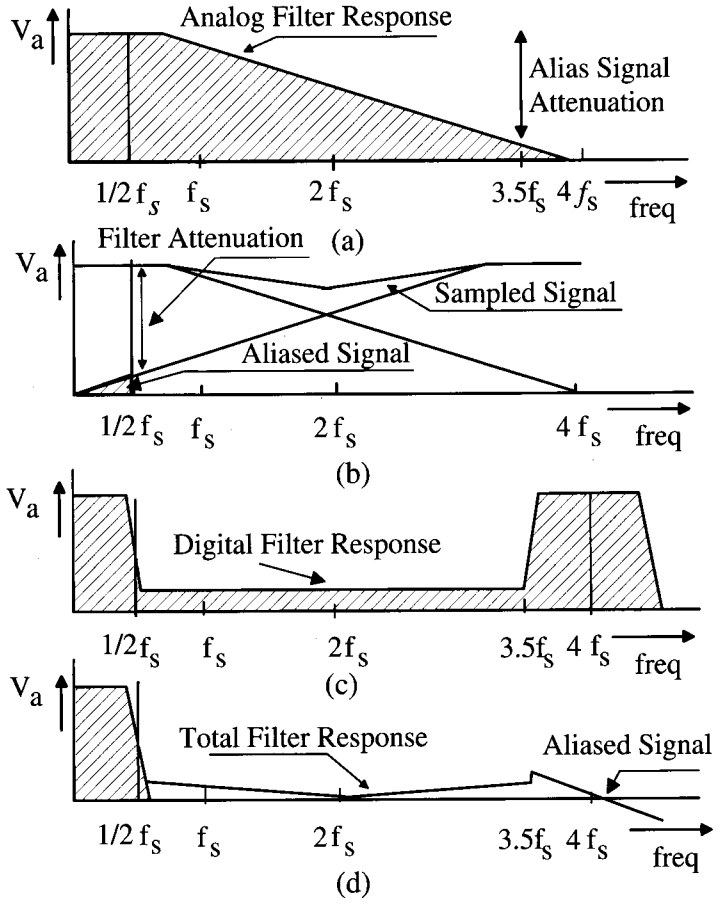


Figure 1.23: (a) Analog (b) Sampled Signal (c) digital (d) total filter frequency response

filter attenuation must be at least equal to the dynamic range of the system to have a minimum influence of aliased spectra on the total system performance. The digital post filter then performs the required steep filtering in between $\frac{f_s}{2}$ and $2f_s$. The final result of the analog pre filtering and digital post filtering operation is shown in Figure 1.23(d). The stop band rejection of the combined analog and digital filter must be made so high that sub sampling can be applied without aliasing the stop band signal components into the baseband. In that case digital output words at the lower sampling rate f_s can be supplied to the following digital signal processing circuitry. In some cases it can be advantageous to apply oversampling and decimation to increase the resolution of a system. (For example, distortion products at the high-frequency band edge are removed by the digital filter.) In Figure 1.22 the sub sampling or decimation operation with a factor R = 4 is shown as the box called R. The final result of this whole operation is an accurate filtering with an almost linear phase characteristic.

1.15 Output filtering in D/A converter systems

In D/A converter systems low-pass filtering is needed to reject the repeated spectra around the sampling frequency and multiples of the sampling frequency. Only the baseband is of interest, while the high-frequency components of the output signal of the D/A converter can, for example, overload the power post amplifier which drives the loudspeaker in a digital audio system. This reconstruction filter interpolates between the quantization steps from the output signal and transforms it into a smooth signal. In Figure 1.24 an ideal D/A converter system is shown. In this ideal system the sample-and-hold (S/H) amplifier transmits very short output pulses to the reconstruction filter. In this way no significant amplitude distortion at output frequencies close to half the sampling frequency is introduced.
However, there is one big difference. At the moment the length of the output pulses of the sample-and-hold amplifier increase to about the sampling time, an amplitude distortion is found. D/A converters act as a sample-and-hold function when during reproduction of the digital signal into an analog value the output signal is maintained. This "zero-order" hold operation introduces the amplitude distortion. A circuit block called sample-and-hold (S/H) is added for this purpose in Figure 1.24 to make this clear, while Figure 1.25 shows the operation of a zero-order hold. During the hold time t_h of the D/A converter the analog output signal remains constant. The low-pass filter "averages" this signal resulting in the dashed output signal shown in

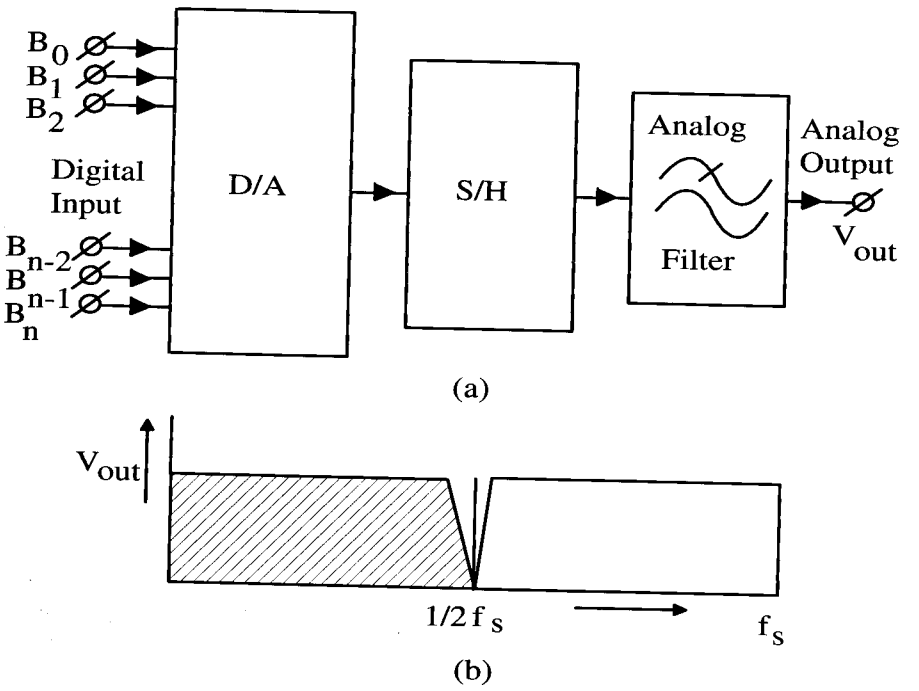


Figure 1.24: (a) D/A converter system (b) Ideal amplitude characteristic of the total system

the figure. The frequency response of the zero-order hold can be calculated.

Suppose t_h is the time during that the circuit is in the hold mode, then the frequency response becomes:

$$H(j\omega) = \frac{1 - e^{-j\omega t_h}}{j\omega}. \tag{1.69}$$

After rearranging we obtain for the amplitude characteristic of the system:

$$\mid H(\omega) \mid = t_h \frac{\sin \omega \frac{t_h}{2}}{\omega \frac{t_h}{2}}. \tag{1.70}$$

This is a well-known amplitude reduction called $\frac{\sin x}{x}$ distortion. In a normal D/A converter as shown in Figure 1.24, the hold time is equal to the sampling time so: $t_h = \frac{1}{f_s}$. Every clock cycle the input data can change and remains constant over that clock cycle. With $\omega = 2\,\pi f_{in}$ formula 1.70

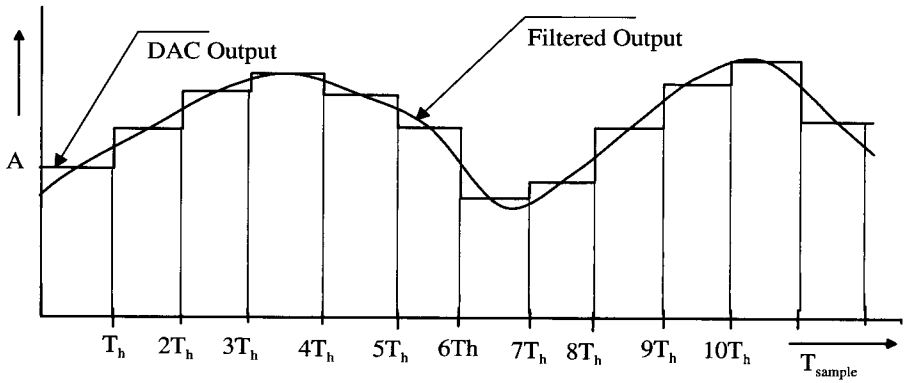


Figure 1.25: Zero-order hold operation

can be rewritten into:

$$| H(2\pi f_{in}) |= \frac{1}{f_s} \frac{\sin \frac{\pi f_{in}}{f_s}}{\pi \frac{f_{in}}{f_s}}. \tag{1.71}$$

In a D/A converter system that is sampled at the Nyquist rate, the maximum input frequency is almost equal to half the sampling frequency. Inserting f_{in} $= \frac{1}{2} f_s$ into equation 1.71 results in an amplitude reduction of $\frac{2}{\pi}$ or 3.92 dB. The amplitude response of the $\frac{\sin x}{x}$ operation is shown in Figure 1.26 for a system using Nyquist sampling. On the other hand, the zero-order hold

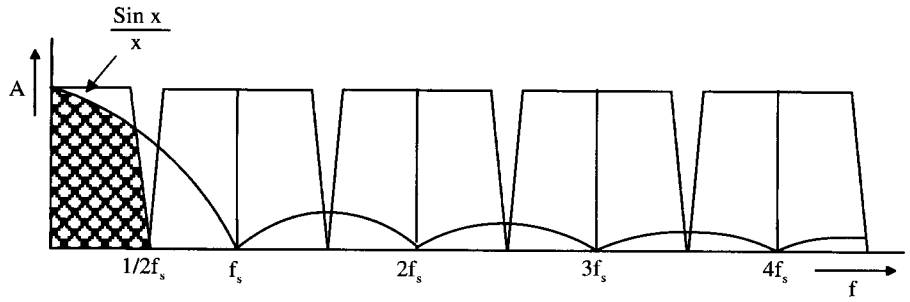


Figure 1.26: Zero-order hold amplitude reduction

operation can be used as a simple low-pass filter. When narrow band signals with respect to the sampling frequency are reproduced, then the $\frac{\sin x}{x}$ filtering operation can already introduce sufficient suppression of the repeated signals. In Figure 1.26 the dashed area shows the narrow-band signal in

comparison with the sampling frequency. At f_s the sampled signals are significantly reduced in amplitude compared to the base-band.

In some cases it is possible to design an analog low-pass output filter in such a way that the $\frac{\sin x}{x}$ amplitude reduction is compensated for by an increase in the amplitude characteristic of this filter at the high-frequency band edge.

A second possibility to overcome this problem is obtained by a decrease of the hold time t_h. The hold-time reduction at a constant sampling frequency f_s can be obtained by introducing a switch at the output of the digital-to-analog converter. During the hold time t_h the output signal of the digital-to-analog converter is applied to the low-pass output filter and during the time $t_s - t_h$ a zero output signal is applied to the low-pass output filter. In Fig. 1.27 this operation is shown. In this figure, the hold time t_h is sampling in between of the sampling time t_s to avoid glitches introduced during switching from one output code to the next code. Furthermore the requirement on the timing of the deglitcher pulse is very high. A small time jitter is required to avoid the introduction of extra timing errors, although this "retiming" can be used to eliminate timing errors introduced during the reproduction of the analog signal.

(Note: $t_s = \frac{1}{f_s}$.)

Suppose that t_h is a fraction k of t_s, so $t_h = kt_s$; then equation 1.71 can be rewritten as:

$$| H(2\pi f_{in}) |= \frac{k}{f_s} \frac{\sin k\pi \frac{f_{in}}{f_s}}{k\pi \frac{f_{in}}{f_s}}. \tag{1.72}$$

Note that $0 \leq$ k ≤ 1.

A decrease of the hold time t_h, for example, by a factor equal to four reduces the amplitude reduction from 3.92 dB to 0.22 dB at $f_{in} = \frac{1}{2} f_s$.

At the moment that k is close to 0, then the limit of the value of $\frac{\sin x}{x}$ is nearly one. No amplitude reduction over a large bandwidth is obtained at the cost of an overall output signal reduction. The disadvantage of this operation is the necessity to use an output amplifier to compensate for the amplitude reduction. At a certain moment the output amplitude can be so small that the noise of the output amplifier is larger than the quantization noise of the digital-to-analog converter. A second problem in practice is

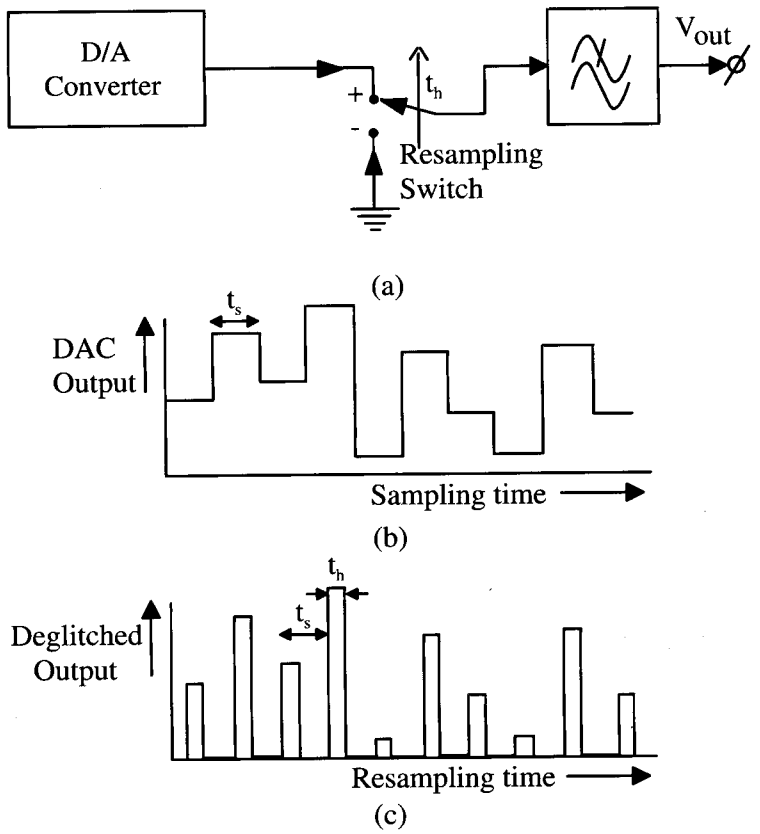


Figure 1.27: (a) D/A Converter with deglitcher switch (b) D/A Converter output signal (c) Deglitched output signal

found in the accuracy with which the switching of the signal must be performed. Furthermore, large signal pulses are applied to the output filter. When an active solution for such a filter is used, then slew rate errors can be introduced, resulting in distortion of the output signal.

A third possibility to avoid the amplitude reduction is obtained by increasing the sampling frequency of the converter. With the same input frequency f_{in} the ratio $\frac{f_{in}}{f_s}$ decreases, giving the desired result. Such an operation can be performed by an oversampling D/A converter. In Figure 1.28 a D/A converter that combines a digital oversampling annex low-pass filtering function is shown. With the box called R the oversampling is introduced. In this specific example a four times oversampling is used. In reference [13]

a detailed description of such a system is given. The frequency response

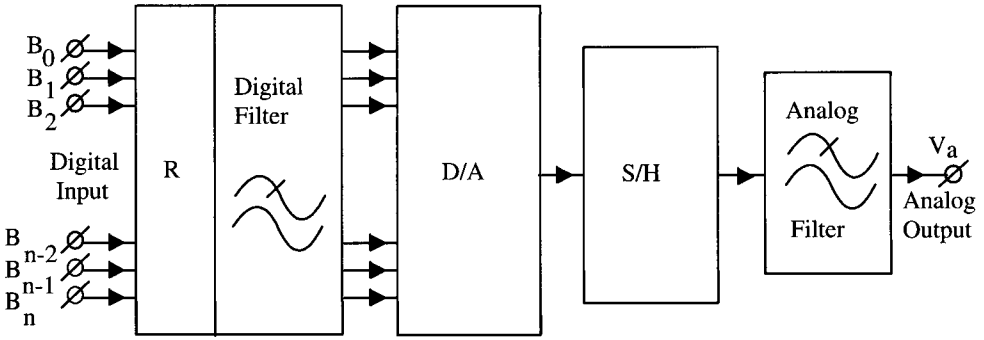


Figure 1.28: D/A converter system using combined digital-analog low-pass filter

curves of the different filters are shown in Fig. 1.29. The digital filtering performs the steep filtering around $\frac{f_s}{2}$. The analog post filter takes care of the signal bands around $4f_s$ and multiples of $4f_s$. This is shown in Figure 1.29(b). The total filter response is shown in Fig. 1.29(c). This figure has only been drawn up to a frequency of $4f_s$, because above this frequency the attenuation of the repeated signal spectra will be reduced so much that no contribution to the dynamic range of the system is obtained. The analog filter can furthermore be designed having a nearly linear phase characteristic. Such a filter has a so called Bessel algorithm to be designed. As a result, the amplitude decrease due to the $\frac{\sin x}{x}$ signal reduction is reduced to 0.22 dB, which can be compensated for in the analog or digital filter. Although the total filter exhibits a narrow transition band, a nearly linear overall phase characteristic is obtained.

Nowadays oversampling ratios of 8 or 16 in 16-bit digital audio D/A converter systems is not unusual. Dynamic range of these systems increases in this way to above 98 dB, which is more than the coding used with the compact disk. The increase in resolution of the converter can be successfully applied when a digital processing algorithm increases the number of significant bits. An example of such a processing can be tone control. In such an application a 12 dB bass or treble boost increases the dynamic range needed in the converter to 18 bits. Furthermore, the somewhat larger dynamic range can improve the linearity around zero when small input signals have to be reconstructed. Special noise-shaping techniques can be used to increase the dynamic range of a system. In Chapters 8 and 9 these systems

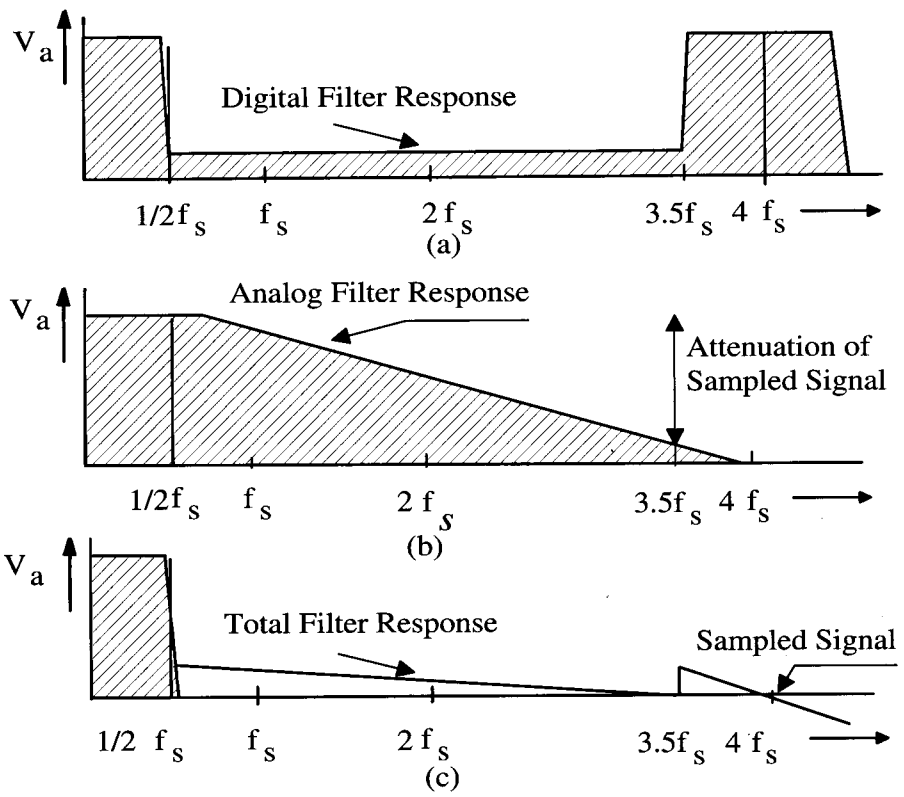


Figure 1.29: (a) Amplitude characteristic of the digital filter (b) Amplitude characteristic of the analog post filter (c) Amplitude characteristic of the total system

will be described.
Note the following:

Although an A/D converter is mostly preceded by a sample-and-hold amplifier, the transfer function of this sample-and-hold unit does not introduce the well-known $\frac{\sin x}{x}$ amplitude reduction. A sample-and-hold amplifier tracks the input signal during the sampling mode. At the moment the amplifier is switched from the sample into the hold mode, the momentary signal is applied to the hold amplifier. This means that at the sample moments the exact signal value is sampled and converted into a digital value. No holding or averaging operation is performed on the signal. The extra hold time introduced by the hold amplifier is only needed to allow the A/D converter

to perform the conversion from an analog discrete-time signal into a digital output signal.

1.16 Dynamic range and alias filter order

In the previous section we have seen that the filtering operation has a strong influence on the dynamic range of an analog-to-digital or digital-to-analog converter system. Especially when the input signals are not well determined,

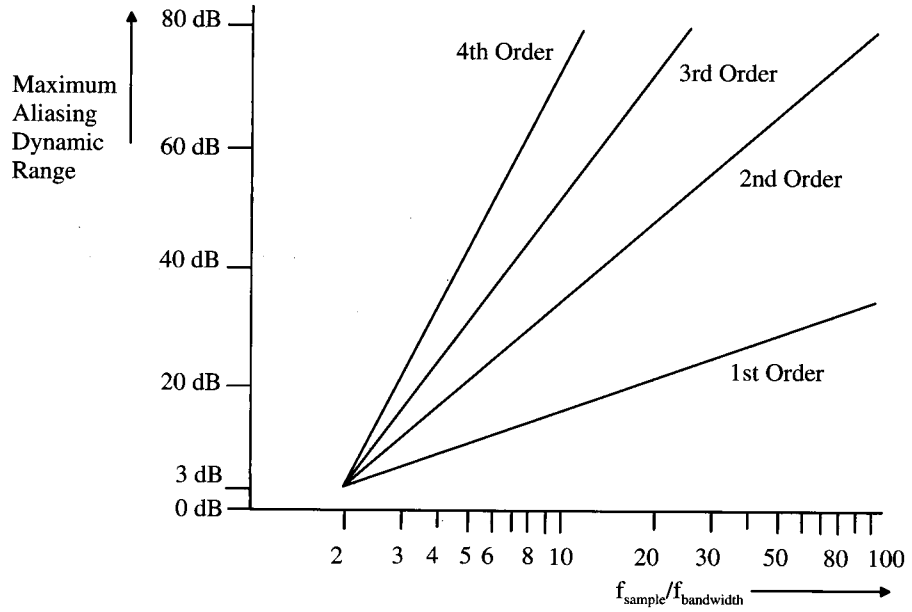


Figure 1.30: Relation between filter order, oversampling ratio and dynamic range

a more stringent filtering is required. In case we suppose that the largest alias component determines the dynamic range of a system, then an estimate of the filter order versus dynamic range can be made. In Fig. 1.30 the relation between dynamic range, filter order and oversampling factor is shown. This curve lets the user quickly determine what filter order and oversampling ratio are needed in case a converter system has to be designed. In case a high-order analog filter above order 4 or 5 has to be used, then problems in designing such a filter because of accuracy of components will occur. In a high-resolution system the attenuation of this filter must be large, while the transition band is usually small. Steep filters are needed

because of the narrow transition band. These filters might be of the elliptical type. Such analog filters have a serious phase distortion. In digital audio systems, for example, this phase distortion can be audible. In stereo systems phase distortion affects the directional information of the sound. Therefore oversampling with a limited filter order gives the most reliable solution to a converter system.

1.17 Analog filter designs

In this section practical filter designs will be discussed and the influence of such a design on the system performance will be discussed. The first design uses the Butterworth criterion having a maximally flat pass band. Phase distortion in this filter is small compared to Chebychev or elliptic filter structures.

1.17.1 Fourth order Butterworth filter

A Butterworth design of a fourth order low-pass active analog filter is shown in Fig. 1.31 The frequency response curves of this filter are shown in Fig.

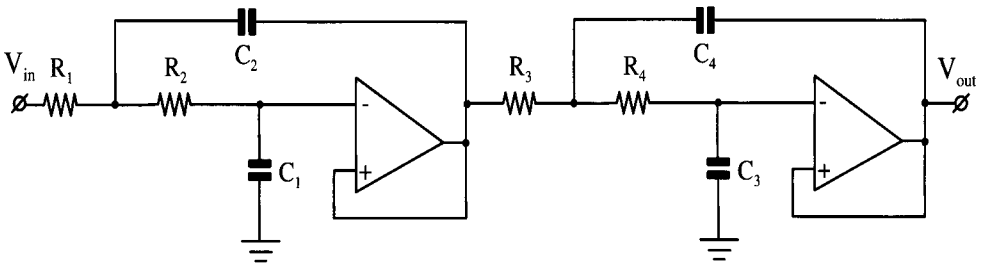


Figure 1.31: Fourth order Butterworth LP filter

1.32(a). The noise density as a function of frequency is shown in Fig. 1.32(b). In this active filter the total noise as a function of the signal bandwidth has been plotted in Fig. 1.32(c). This curve shows that with increasing bandwidth, the total noise still increases. Such a filter as an input filter for an analog-to-digital converter can have a strong influence on the dynamic range because the wide-band noise of the operational amplifier used is sampled and folded back into the baseband. Not only the noise in the passband, but the out of band noise and signal attenuation are important. Out of band signals may be caused by low level oscillations of the filter

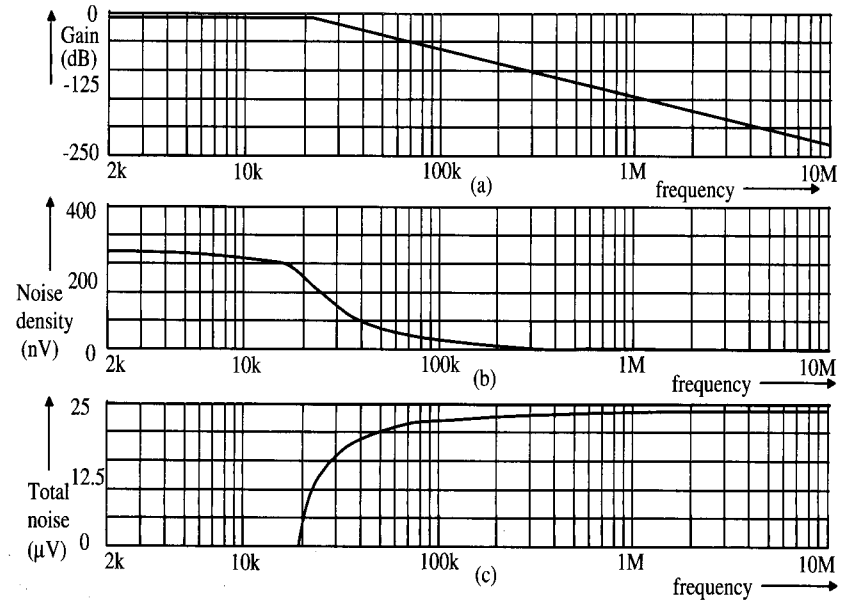


Figure 1.32: Frequency response and noise of fourth order LP filter

structures or that the stopband attenuation decreases at high frequencies. Mostly attention is paid to the passband, but in analog-to-digital conversion systems the stopband characteristic has a strong influence on the overall performance.

1.17.2 Fifth order Butterworth filter

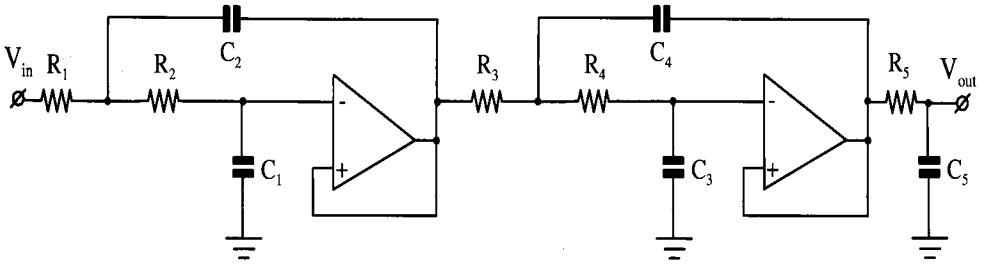


Figure 1.33: Fifth order Butterworth LP filter

To increase the stopband attenuation and obtain a reduction in oversampling ratio the order of the filter is increased with one. This filter is shown in

Fig. 1.33. The extra time constant is added at the output of the filter. Care must be taken in this case that the loading of the filter does not influence the last time constant. The input capacitance must be small and the resistive impedance large compared to the added RC time constant. In CMOS technology mostly this requirement can be easily fulfilled. Furthermore signal levels at the moment sampling takes place by eg. the sample-and-hold amplifier must be as large as possible to minimize the aliased wide-band noise. In case amplification before sampling takes place, then this amplification can be performed with a limited bandwidth. Only the signal band is important in this case. The frequency response of this filter is shown in Fig. 1.34. The

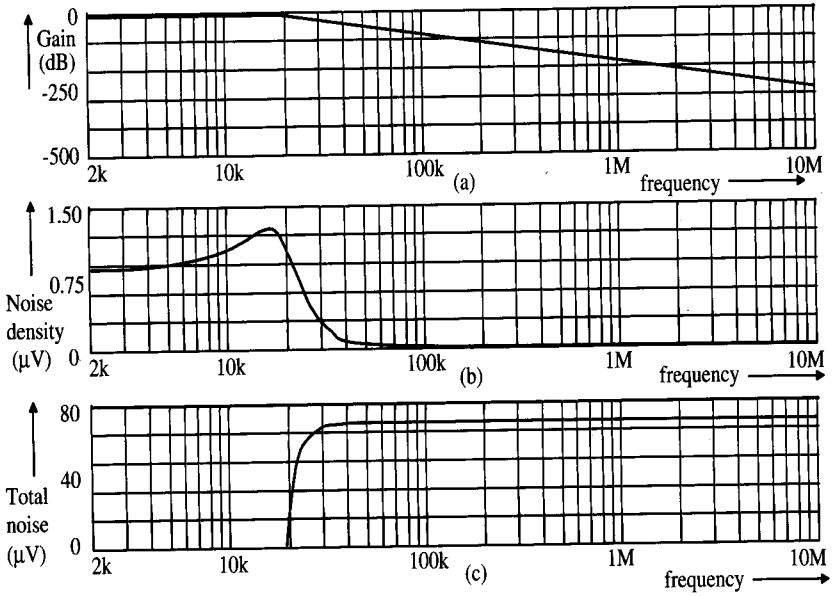


Figure 1.34: Frequency response and noise of fifth order LP filter

noise performance of this filter shows an important result. The extra RC filter at the output of the system limits the wide-band output noise. Above about 100 kHz the total noise is nearly constant. Wide-band noise from the operational amplifiers used in the active filter is therefore limited. As a result the dynamic range of this converter system is only slightly influenced by the performance of the operational amplifiers.
When constructing $L-C$-type low-pass filters for measuring purpose, care must be taken in choosing the components used. Some type of practical capacitors show a nonlinear signal behavior resulting in distortion. High-

performance capacitors are needed in low-distortion systems to avoid this problem. Furthermore, the size of the pot cores used to construct the inductors must be large to avoid nonlinear effects due to magnetic saturation in these cores. An additional problem may exist by mounting the pot cores too close to each other. In that way the magnetic fields generated by the coils are transferred through the filter. This results in a limited stop band attenuation. By using adequate elements, low-pass measuring filters can be designed for digital audio systems up to a dynamic range of 20-bits.

1.17.3 Digital filter design

A transversal digital filter with a linear phase characteristic can be designed using the appropriate software.The passband ripple of this filter is 0.05 dB. What will be shown here is the frequency response of a digital oversampling filter that can be applied to digital audio digital-to-analog converter systems. In such a system the maximum attenuation of the digital filter can be limited to about 70 dB. This amount of filtering is sufficient to avoid distortion and inter modulation effects because a low-performance cassette recorder is used to make a private copy of a CD. The frequency response of the designed filter using the Remez algorithm is shown in Fig. 1.35.

1.18 Minimum required stop band attenuation

Suppose the analog low-pass filter in the A/D converter system as shown in Figure 1.21 has a limited stop band rejection. Suppose, furthermore, that the analog bandwidth of the input amplifier, the sample-and-hold amplifier, or the comparator in the A/D converter is limited to f_{comp}. In analog-to-digital converter systems which use, for example, a successive approximation conversion algorithm (see Chapter 5) the comparator bandwidth must be at least N times larger than the sampling frequency. In such a system during the sampling time N trials are made to make the digital-to-analog converter output equal to the analog input signal. Moreover, to obtain an accurate settling of the comparator subtracter system even a larger bandwidth in the comparator is needed. At which point the aliasing occurs depends on the architecture of the analog-to-digital converter and the point in the system where the sampling is performed. Due to the sampling of the input signal all input frequencies that are in the aliasing signal bands are folded back into the baseband of the system. The number of aliasing signal bands that are folded back into the baseband are limited by the extra filtering intro-

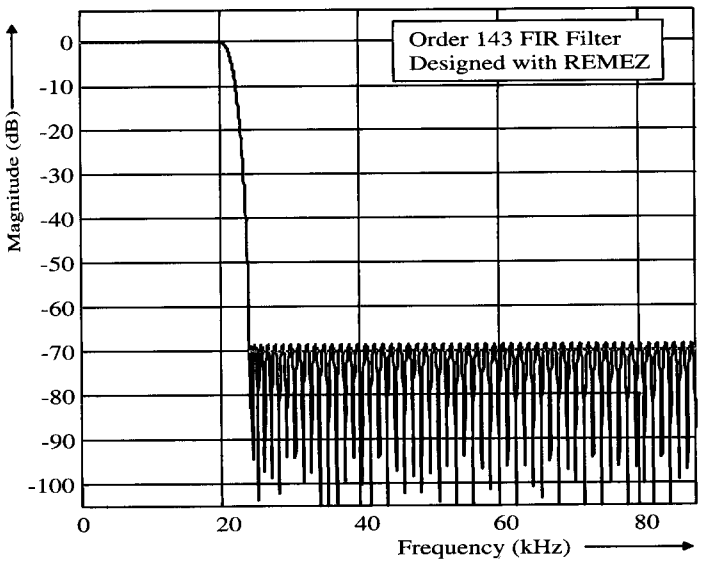


Figure 1.35: Frequency response of a digital LP filter

duced by the input signal amplifier, the sample-and-hold amplifier, or the bandwidth of the comparator in the A/D converter. In Figure 1.36 the attenuated signal at the output of the amplifier-comparator stage is shown as a function of frequency. In this configuration the sampling is performed by the comparator stage as is the case in, for example, a flash-type analog-to-digital converter (See Chapter 3).

Note that the bandwidth f_{comp} of the input amplifier or comparator in this example is about $3f_s$. When white noise or frequency components attenuated by the input anti-aliasing filter in the frequency range between $f = \frac{f_s}{2}$ and $f \gg 3f_s$ are input into the system, then the number of bands that are folding back noise or unwanted signal components into the baseband of the system is equal to:

$$N_{fold} = \frac{f_{comp} - \frac{f_s}{2}}{\frac{f_s}{2}}. \tag{1.73}$$

The fold-back noise and the unwanted signal components add to the quantization error and thus reduce the signal-to-noise ratio of the system. The

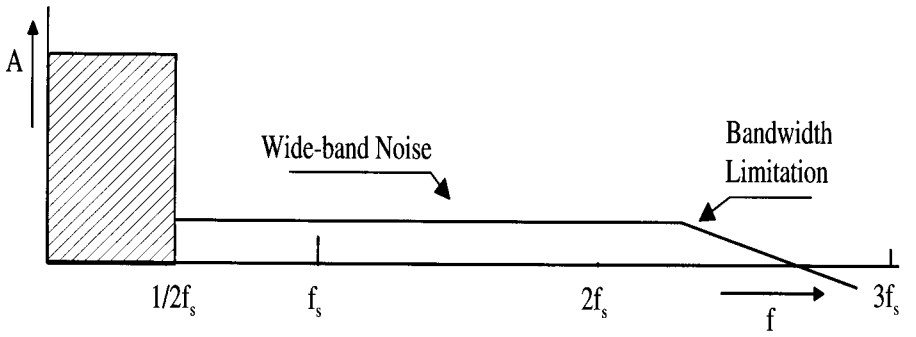


Figure 1.36: Output signal of the amplifier-comparator stage in an A/D converter system

"noise" in the baseband now increases to

$$\sqrt{N_{fold} + 1} = \sqrt{2 \times \frac{f_{comp}}{f_s}}. \tag{1.74}$$

If we want to have a condition in which the total fold-back noise in the base-band is equal to the quantization "noise" in the system when a signal is applied in the baseband, then the stop-band rejection of the low-pass filter must be increased by a factor equal to: $\sqrt{N_{fold}}$.

This increase in stop-band rejection ($A_{foldback}$) is equal to:

$$A_{foldback} = \sqrt{N_{fold}} = 10 \log N_{fold}\, dB. \tag{1.75}$$

This means that in a system with n bits the minimum stop-band rejection of the input filter must be:

$$A_{stopmin} = n \times 6.02 + 1.76 + 10 \log N_{fold}. \tag{1.76}$$

Formula 1.76 gives a minimum anti-aliasing filter stop-band attenuation requirement under the condition that the total amount of fold-back noise is equal to the quantization noise.

Inserting formula 1.74 into formula 1.76 results in an expression for the minimum required stop-band rejection $A_{stopmin}$:

$$A_{stopmin} = n \times 6.02 + 1.76 + 10 \log(2 \times \frac{f_{comp}}{f_s})\, dB. \tag{1.77}$$

When a low-pass filter with a minimum stop-band rejection equal to formula 1.77 is used, then the dynamic range (S/N ratio) of the system is reduced by 3 dB.

If a smaller reduction is required, then the stop-band attenuation must be increased.

As an example, the minimum stop-band rejection of an input filter for an audio A/D converter will be calculated. This calculation involves the worst-case condition of signals outside the signal band. Suppose the bandwidth of the comparator is equal to 8.8 MHz, then with a sampling frequency of 44 kHz we obtain for the minimum stop-band rejection using formula 1.77 $A_{stopband} = 98 + 26 = 124$ dB. In practical situations, however, the noise and signals outside the baseband usually do not have the maximum amplitude equal to the signal amplitude. Furthermore, the basic A/D converter itself must have a signal-to-noise ratio measured over the signal band close to the theoretical value of 98.1 dB. The noise level of the analog filter must be well below the quantization noise of the system to avoid a reduction of dynamic range.

1.19 Conclusion

In this chapter the dynamic range of A/D and D/A converters is defined. Requirements for input and output filters are introduced. Different methods to implement anti-alias or reconstruction filters are shown. If a linear phase characteristic is required in a system, a combined analog-digital filtering solution gives the best results. Examples of practical analog and digital filter functions have been shown. Attention has been paid to the stop band noise of analog filters and the required construction of such a filter.

Quantization errors have been analyzed. Especially attention has been paid to the spectrum of quantization errors and the influence of quantization on inter modulation distortion has been shown. Using this analysis an accurate analysis of the dynamic range of low resolution converters has been derived. Aliasing of the quantization errors results in a noise like behavior of the quantization error. There exists no possibility to use filtering in between quantization and sampling to reduce the aliasing effect.

A general relation defining the sampling time uncertainty in relation to the

resolution of the converter and the maximum input signal frequency is derived. This relation determines the stability of the sampling clock required over a short period of time. The relation between sampling time uncertainty and the reduction in Effective Number of Bits (ENOB's) has been derived too. This relation is very useful in determining the dynamic range of a converter system with respect to maximum required input frequency and sampling clock short term stability.

A simple sampling clock time uncertainty calculation model is introduced, giving an understanding of the pulse-to-pulse time jitter of high stability sampling clock systems applied to converters.

An analysis of the amplitude reduction as a function of sample time for D/A converters is given. Oversampling or a reduction of the output sample time decreases this reduction to within acceptable values.

Chapter 2

Specifications of converters

2.1 Introduction

To obtain insight into the design criteria for converters it is important to arrive at a unanimous definition of specifications. These specifications must include the application of converters in conversion systems (see references [14, 15]). Dynamic specifications of converters are needed to obtain insight in the applicability of a certain converter in a digital signal processing system: for example, digital audio or digital video. In a conversion system the complete conversion from analog into digital or digital into analog information is performed. Such systems include input or output amplification and anti-alias filtering.

Unanimous specifications for DC performance are well known in literature. Specifications for converters in signal-processing systems are more difficult to standardize. One of the reasons for this limitation in specification can be that in the early days of conversion the application of converters was in the area of digital voltmeters and control systems. These systems need the high dc performance at low signal speeds.

Digital audio in comparison with voltmeters, for example, applies for high-performance dynamic system specifications. The performance of converters in digital audio or digital video systems is at the limit of the possibilities of today's technology. In this chapter the most important specifications will be defined and discussed in more detail.

2.2 Digital data coding

Information in digital form appears at the input of a D/A converter or at the output of an A/D converter. This code can appear in parallel form or serially on a single line.

In the digital world several logic systems are used. Today's CMOS logic is overtaking the widely used Transistor Transistor Logic (TTL) in which a "1," ONE or "true" represents a minimum level of +2.4 V and "0," ZERO or "false" corresponds to a maximum level of +0.4 V. CMOS logic swings are determined by the applied supply voltage, which for today's logic blocks is 5 V but will in the future reduce to 3.3 V. In high-speed systems Emitter Coupled Logic (ECL) is used with levels of - 0.9 V for a logic "1" and - 1.8 V for a logic "0." The small logic swing of 0.9 V allows for high-speed applications. The advantage of ECL circuits is the possibility of a full differential system operation. This differential operation prevents large current spikes from flowing in the supply lines during switching. Thus a low interference between the analog signal path and the digital signal path can be obtained.

In systems with a serial digital data stream, a conversion from a serial stream into a parallel word must be performed. A shift register that performs serial to parallel conversion is added for this purpose. Furthermore, data latches are added which at the end of the serial-to-parallel conversion get the data word latched on the command of the latch clock. These data latches directly drive the current or voltage switches for example in a D/A converter. Analog data appear at the output of the converter after new data are latched in. The data latches together with the bit switches are optimized to obtain a minimal output glitch during switching of the converter. This is very important in a D/A converter system. Such a system can be operated without a so-called deglitcher when the glitch energy is small compared to the LSB energy. A "glitch" is a large output signal change (larger than the amplitude of an LSB step) appearing during a code transition of a converter. In Figure 2.1 an example of a serial-to-parallel conversion in a D/A converter is shown. The advantage of this circuit configuration is that the data latches together with the bit switches can be optimized for the best switching performance. Usually this means the smallest glitch error. D/A converters with parallel digital inputs often do not have data latches on board. Applying these converters requires an accurate board layout to match the delays between the output signals of the data latches and the switches. Users are not always aware of this problem and therefore end up with a low overall performance

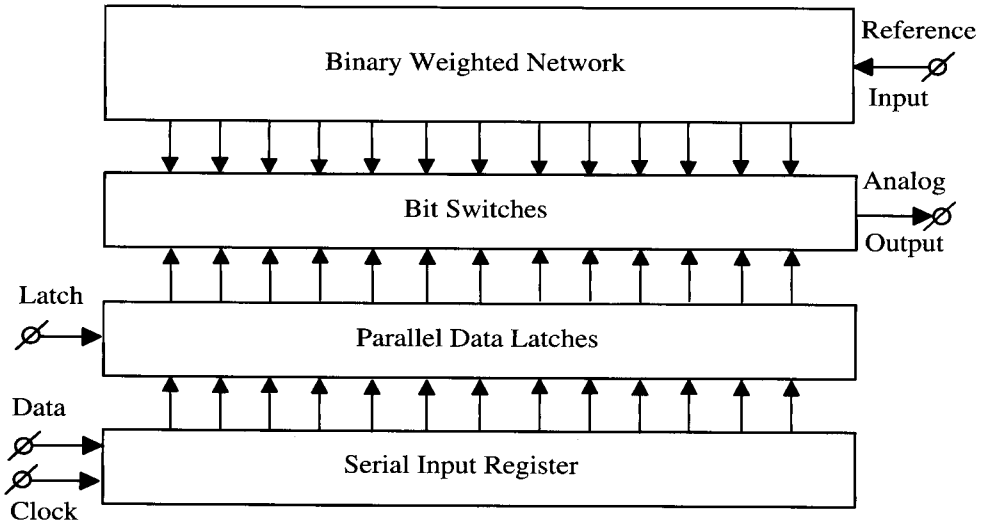


Figure 2.1: Serial-to-parallel conversion in a D/A converter

of the converter system. Large "glitches" may appear at the output of the converter because of the non-equal switching time of bit switches during code transitions.

2.3 Digital coding schemes

As a digital code the natural binary code (base 2) is used. Without additional measures it is difficult to obtain bipolar signals. Therefore, an offset binary code is introduced. This code is "offset" by turning on the MSB bit for an analog value of zero. In most cases an additional current is added to subtract the MSB bit current from the input or output current value to obtain analog zero. The principal drawback of the offset binary code is that a major carry transition occurs if a small bipolar signal is generated or converted around zero. Such a transition requires the highest linearity around zero and immediately gives rise to glitch problems. These problems are worst for D/A converters. In A/D converters the noise that is part of the offset current is added to the input signal and may result in a reduction of the dynamic range of the system. Furthermore, this offset must be stable with temperature, and variations in supply voltage should not change the zero setting of the A/D converter.

A sign-magnitude code seems to be the most straightforward approach to the glitch and noise problem. The sign-magnitude coding introduces an inverter into the system operating on the command of the sign bit of the signal. This inverter, however, introduces an accuracy problem which is even more difficult to solve in high-resolution converters than the dc "offsetting" of the converter in the offset binary mode.

In Figure 2.2 a basic inverter implementation is shown. At the output of

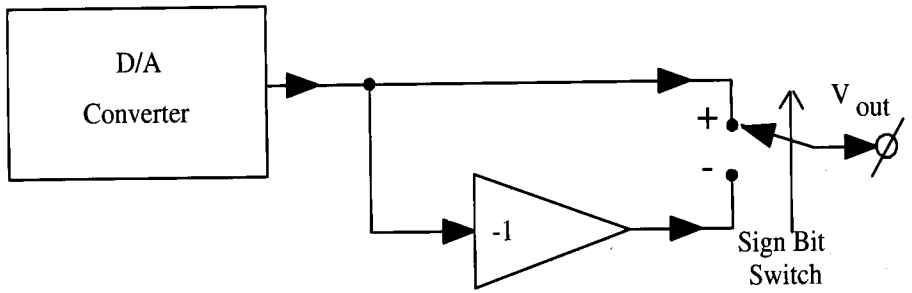


Figure 2.2: Basic sign-magnitude inverter implementation

the digital-to-analog converter an analog inverting operational amplifier and a switch (S) controlled by the sign-bit is added to the system. During the positive output signal generation the output signal of the digital-to-analog converter is directly applied to the output terminal. During the negative signal generation the output signal of the digital-to-analog converter coming from the analog inverter is applied to the output terminal. The accuracy with which the signal is inverted determines the total accuracy of the system. In practical implementation an accuracy between 1% and 0.1% can be obtained. Other codes can also be used. When computational operations are needed the twos complement code is very useful. In Table 2.1 the different codes that can be used in converters are shown. From the table it can be seen that with the ones complement and the sign-magnitude code two code possibilities for zero are found. A computation has to be performed to avoid this double zero coding.

The preferred code implementation concerning noise and glitches is the sign-magnitude code. However, this code suffers from linearity problems around zero. As a result the offset binary code is the most commonly used code implementation in converter applications.

Number	Sign + Magnitude	Twos Complement	Offset Binary	Ones Complement
+7	0 1 1 1	0 1 1 1	1 1 1 1	0 1 1 1
+6	0 1 1 0	0 1 1 0	1 1 1 0	0 1 1 0
+5	0 1 0 1	0 1 0 1	1 1 0 1	0 1 0 1
+4	0 1 0 0	0 1 0 0	1 1 0 0	0 1 0 0
+3	0 0 1 1	0 0 1 1	1 0 1 1	0 0 1 1
+2	0 0 1 0	0 0 1 0	1 0 1 0	0 0 1 0
+1	0 0 0 1	0 0 0 1	1 0 0 1	0 0 0 1
+0	0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0
−0	1 0 0 0	(0 0 0 0)	(1 0 0 0)	1 1 1 1
−1	1 0 0 1	1 1 1 1	0 1 1 1	1 1 1 0
−2	1 0 1 0	1 1 1 0	0 1 1 0	1 1 0 1
−3	1 0 1 1	1 1 0 1	0 1 0 1	1 1 0 0
−4	1 1 0 0	1 1 0 0	0 1 0 0	1 0 1 1
−5	1 1 0 1	1 0 1 1	0 0 1 1	1 0 1 0
−6	1 1 1 0	1 0 1 0	0 0 1 0	1 0 0 1
−7	1 1 1 1	1 0 0 1	0 0 0 1	1 0 0 0
−8		1 0 0 0	0 0 0 0	

Table 2.1: Different digital coding schemes

2.4 Ideal and Non-ideal converters

A converter basically consists of an amplitude quantizer followed by a sampler. In general the sequence of quantizer and sampler can be changed without having any influence on the performance or the operation of the system. An ideal converter is shown in Fig. 2.3 The specifications of an ideal converter do not show any errors due to non-ideal components or clock jitter and are therefore only theoretical of importance. In practical converters, electronic elements used to construct the converter show finite matching. Resistors and capacitors show when carefully layed out a .1% or better matching. Active elements like bipolar and CMOS devices show offsets when used in differential pairs. These offsets will be characterized in a separate chapter. Noise in active and passive elements reduces the maximum dynamic range of a system. Especially with low supply voltages the limiting effects of noise will occur in wide-band or high-resolution converters. To simplify and have the possibility of modeling non-ideal effects in converters

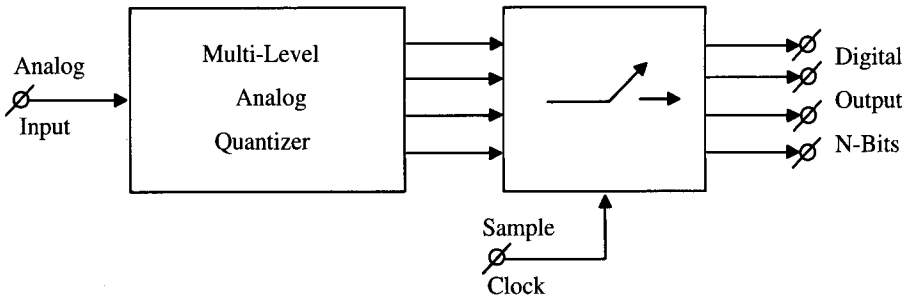


Figure 2.3: Ideal converter

all mismatch and/or offsets will be incorporated in the reference ladder or reference elements. In Fig. 2.4 this model is shown. The non-idealities in-

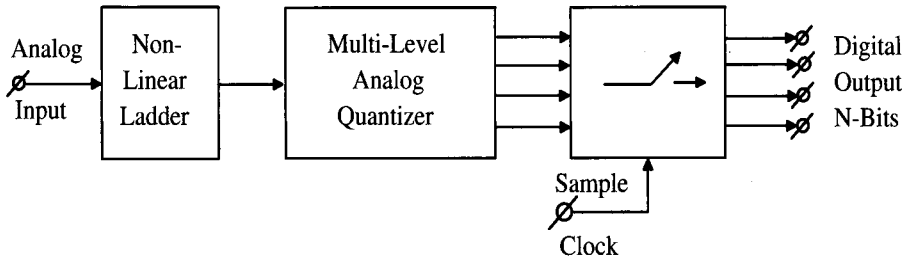


Figure 2.4: Non-ideal converter

troduced by component mismatch introduces errors in the operation of the converter. In general a designed converter meets a linearity specification set at about $\pm \frac{1}{2}$ LSB as will be defined in the following sections. Such a specification will introduce errors that are far more significant than errors introduced by quantization. It is therefore important to refer these errors to the quantization error. The non-ideality then results in a decrease of performance in Effective Number of Bits (ENOBs) compared to the ideal converter.
Note that these specifications are for the converter only.

2.5 DC specifications

2.5.1 Absolute accuracy

Accuracy of converters should not be confused with linearity and resolution. It includes the errors of quantization, nonlinearities, short-term drift, offset, and noise.

The *absolute accuracy* of a converter is the actual full-scale input or output (analog-to-digital or digital-to-analog converter) signal (voltage, current, or charge) referred to the absolute standard of the National Bureau of Standards. This absolute accuracy is mostly related to the reference source used in the converter. Sometimes this reference source consists of a special temperature-compensated zener diode. In integrated circuits this zener diode is replaced by an integrable source which in modern systems is based on the band-gap voltage of silicon. This reference source should have a low-noise with respect to the resolution of the converter. Temperature coefficients in the ideal case should be so small that the accuracy of the reference over the specified temperature range stays within the resolution of the converter ($\frac{1}{2}$ LSB over the full temperature range).

2.5.2 Relative accuracy

The *relative accuracy* is the deviation of the output signal or output code of a converter from a straight line drawn through zero and full scale. Output signals or output codes must be corrected from a possible zero offset.
This relative accuracy is called: *Integral Non Linearity* (INL) or sometimes *linearity*. Throughout this book the Integral Non Linearity will be used. In Figure 2.5 a graphical example is shown of the integral nonlinearity definition for a digital-to-analog converter.
In the figure the boundaries for which the nonlinearity deviates not more than $\pm \frac{1}{2}$ LSB of a straight line through zero and full scale are shown.

The $\pm \frac{1}{2}$ LSB integral nonlinearity definition implies a *monotonic* behavior of this converter.

Monotonicity of a converter means that the output of, for example, a D/A converter never decreases with an increasing digital input code. A minimum increase of *zero* is allowed for a 1 LSB increase in input signal in a D/A converter. In Figure 2.5 the transfer curve of a monotonic converter is shown.

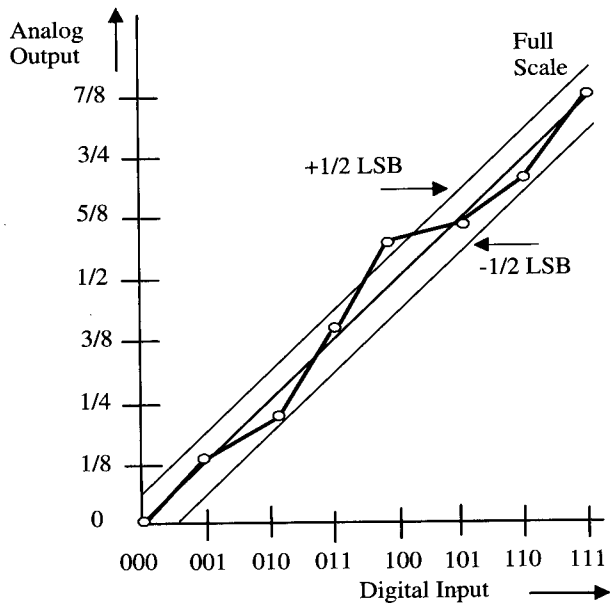


Figure 2.5: Definition of the Integral Non-Linearity of a D/A converter

In an analog-to-digital converter *monotonicity* means that *no missing codes* can occur. It must be noted at this point that converters can be designed which are *guaranteed monotonic* but do not have the half LSB linearity specification. These converters are based on non-binary weighting of the bit currents. As an example of such a converter a tapped resistor with switches performs a monotonic digital-to-analog conversion without requiring an integral nonlinearity specification.

Examples of converters which are monotonic by design are presented in references [21, 22, 31].

Note that the *monotonicity* specification does NOT automatically include that a converter has a $\pm \frac{1}{2}$ LSB integral nonlinearity error!

2.5.3 Nonlinearity calculation

A simple calculation can be performed to show that the nonlinearity specification of $\pm \frac{1}{2}$ LSB is sufficient to prove *monotonicity* of a binary-weighted converter. During this calculation all signals or codes are corrected for zero offset in advance simplifying the analysis.

Suppose we have an n-bit binary-weighted converter, then with ε_m corresponding to the error of the m^{th} bit, the non-ideal weighting of this bit can be written as:

$$b_m = 2^m + \varepsilon_m. \tag{2.1}$$

Note that a unity LSB bit weight is used in this equation. This unity bit weight does not influence the nonlinearity calculations.

The nonlinearity will now be calculated as the total deviation from a straight line between zero and full-scale. The full-scale value B of an n-bit converter can be expressed as:

$$B = \sum_{m=0}^{n-1} (2^m + \varepsilon_m). \tag{2.2}$$

With

$$\sum_{m=0}^{n-1} 2^m = 2^n - 1, \tag{2.3}$$

this can be simplified into:

$$B = 2^n - 1 + \sum_{m=0}^{n-1} \varepsilon_m. \tag{2.4}$$

Note that the total number of quantization steps is given by equation 2.3. The "ideal" step size S of the converter can be calculated using the full-scale value of the converter and the number of quantization steps, resulting in:

$$S = \frac{B}{2^n - 1} = 1 + \frac{\sum_{m=0}^{n-1} \varepsilon_m}{2^n - 1}. \tag{2.5}$$

The linearity error Δ_k of the k^{th} bit compared with a value obtained from the ideal straight line through zero and full scale becomes:

$$\Delta_k = 2^k.(1 + \frac{\sum_{m=o}^{n-1} \varepsilon_m}{2^n - 1}) - (2^k + \varepsilon_k). \tag{2.6}$$

In general errors will have positive and negative signs. Adding all errors together must result in a total error of zero, because the sum of all non-ideal bit weights is used as the full scale value. The following calculation proves this statement. Summing Δ_k results in:

$$\sum_{k=0}^{n-1} \Delta_k = \sum_{k=0}^{n-1} \frac{2^k}{2^n - 1} \cdot \sum_{m=0}^{n-1} \varepsilon_m - \sum_{k=0}^{n-1} \varepsilon_k. \tag{2.7}$$

Inserting again:

$$\sum_{k=o}^{n-1} 2^k = 2^n - 1, \tag{2.8}$$

this equation can be simplified into:

$$\sum_{k=o}^{n-1} \Delta_k = \sum_{m=0}^{n-1} \varepsilon_m - \sum_{k=0}^{n-1} \varepsilon_k = 0. \tag{2.9}$$

As a result of this calculation the absolute values of the sum of all positive errors Δ_k must be equal to the sum of all negative errors Δ_k. The integral non linearity of a converter (INL) is now specified as the total error of the positive or negative errors or:

$$INL = \sum_{k=0}^{n-1} Positive\Delta_k = -\sum_{k=0}^{n-1} Negative\Delta_k \leq \frac{1}{2}\, LSB. \tag{2.10}$$

To prove *monotonicity* of a binary-weighted converter, suppose that as a first step only the MSB bit value is too small. This means that the sum of the remaining bit errors must be equal to the MSB bit error but with the opposite sign. The nonlinearity error Δ_{n-1} of the MSB bit can be expressed as (2.6):

$$\Delta_{n-1} = 2^{n-1}.(1 + \frac{\sum_{m=0}^{n-1} \varepsilon_m}{2^n - 1}) - (2^{n-1} + \varepsilon_{n-1}), \tag{2.11}$$

or:

$$\Delta_{n-1} = (\frac{2^{n-1}}{2^n - 1} \cdot \sum_{m=0}^{n-1} \varepsilon_m) - \varepsilon_{n-1}. \tag{2.12}$$

As defined in equation 2.10 the MSB-bit error given by equation 2.12 is equal to the integral non linearity (INL) of the converter. Thus:

$$INL = \Delta_{n-1}. \tag{2.13}$$

In Figure 2.6, the minimum condition for *monotonicity* is shown. The dashed slanted lines indicate the $\pm \frac{1}{2}$ LSB boundaries determined by the integral nonlinearity specification. As is shown, this converter has a $\pm \frac{1}{2}$ LSB nonlinearity specification.

When the MSB-bit is smaller than the sum of the other bits, the converter becomes $non - monotonic$ as is indicated by the dashed curve in the figure. The major carry transition from all bits except MSB switched on (011) compared to only MSB switched on (100) is shown. Furthermore, it is assumed

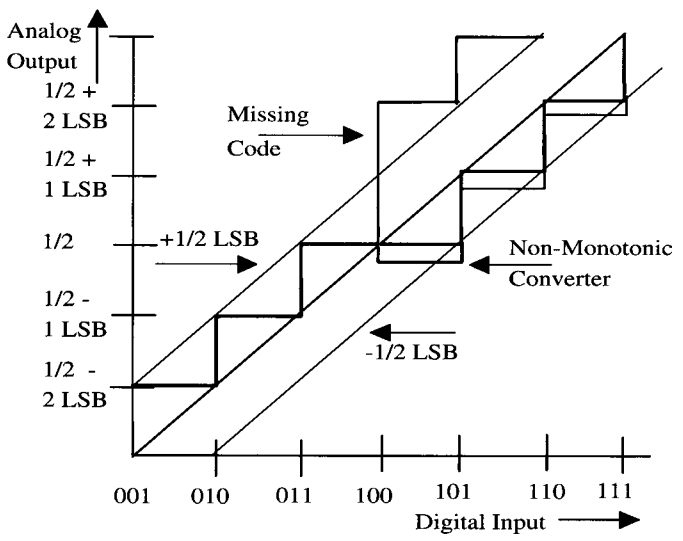


Figure 2.6: MSB major carry transition

that the MSB bit value is too small compared to the rest of all bits.

The linearity error given by equation 2.10 is a measure for *monotonicity* of the converter. When in a D/A converter the digital input code is increased by a value of 1 LSB, the minimum requirement for *monotonicity* is no increase in analog output value as shown in Figure 2.6. This means that twice the error given by equation 2.12 must be less or equal to 1 LSB or:

$$\Delta_{n-1} = \frac{2^{n-1}}{2^n - 1} \cdot \sum_{m=0}^{n-1} \varepsilon_m - \varepsilon_{n-1} \leq \frac{1}{2} LSB, \tag{2.14}$$

or:

$$INL \leq \frac{1}{2} LSB. \tag{2.15}$$

In an analog-to-digital converter an INL definition including the quantization levels equal to 2.15 is valid.
In case the MSB bit value is 2 LSB values larger than the sum of all the smaller bits, then a missing code appears in the converter. An analog value is skipped. This is the top line shown in Fig. 2.6.
In general it can be said that the errors of the individual bit weights must be added according to the definition given in equation 2.10. To guarantee *monotonicity* of the converter, the sum of the errors must never exceed $\frac{1}{2}$ LSB value. An identical calculation can be performed for other bit weights

in the converter. In this way the generalized *monotonicity* definition can be proven. Performing such calculations, it will be found that the error at the MSB transition shows the most stringent linearity requirement.

In Figure 2.7 the errors of the individual bit weights of a binary weighted converter are shown. The errors for full-scale and zero are calibrated to be zero. In this way a straight line between zero and full-scale is obtained. Starting from the left side of the figure, the errors start from the MSB-error and go down to the LSB-error. Finally the total of the positive and the negative errors are plotted at the most right side. This converter can be specified as having a $\pm \frac{1}{2}$ LSB integral nonlinearity error. In a converter

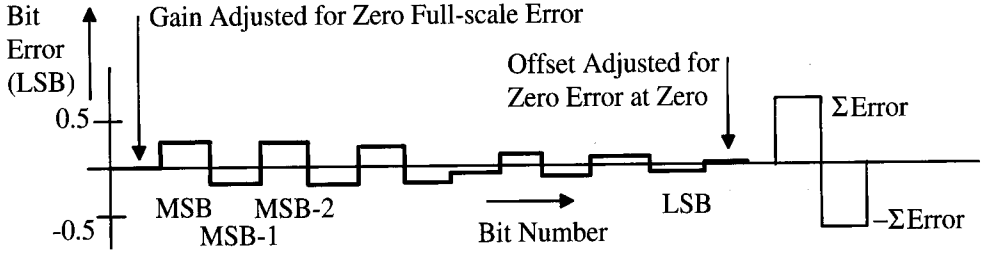


Figure 2.7: Bit-weight error of a binary-weighted converter

it is always possible to generate a code that coincides with this worst-case error. Furthermore, a converter might be *monotonic* having a linearity error of more than $\frac{1}{2}$ LSB. In that case an increase in analog output larger than 2 LSBs is possible. A "missing" code value is introduced in this converter.

Conclusion: A converter is always *monotonic* when the integral nonlinearity specification (INL) is less than or equal to $\pm \frac{1}{2}$ LSB.

However, when a converter is specified to be always *monotonic*, then this specification does not automatically imply an integral nonlinearity error of less than or equal to $\pm \frac{1}{2}$ LSB.

2.5.4 Differential nonlinearity

Differential nonlinearity (DNL) error describes the difference between two adjacent analog signal values compared to the step size (LSB weight) of a converter generated by transitions between adjacent pairs of digital code numbers over the full range of the converter.

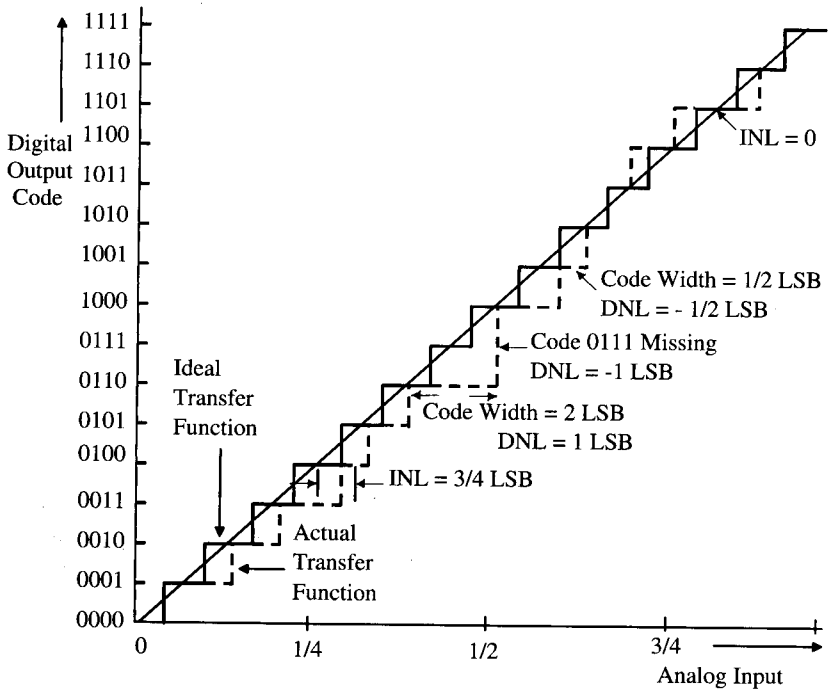


Figure 2.8: Transfer curve of a 4-bit A/D converter

The differential nonlinearity is zero if every transition to its neighbors equals 1 LSB. In a *monotonic binary − weighted* converter an increase of the digital code value by 1 LSB can result in an increase in analog signal between 0 and 2 LSBs. The maximum differential nonlinearity in this case is $\pm$ 1 LSB.

Writing down the differential nonlinearity for a digital-to-analog converter in a formula gives:

$$DNL = S_{out}(C_{m+1}) - S_{out}(C_m) - 1LSB. \tag{2.16}$$

C_{m+1} and C_m are two adjacent digital input codes. $S_{out}(C_n)$ is the output signal of the converter with an input code C_n.
The value of 1 LSB corresponds to the "ideal" step from the previous section. In case of an analog-to-digital converter the DNL can be written as:

$$DNL = A_{input}(Q_{m+1}) - A_{input}(Q_m) - 1LSB. \tag{2.17}$$

Q_{m+1} and Q_m are two adjacent quantization levels. $A_{input}(Q_n)$ is the analog input voltage corresponding to the quantization level Q_n.

In Figure 2.8 the transfer curve of a 4-bit A/D converter is shown. The drawn line shows the ideal transfer characteristic, while a dashed line indicates the measured transfer curve of a practical converter. Integral nonlinearity (INL), differential nonlinearity (DNL), and full-scale range (FSR) are shown partly as a function of the LSB error between drawn line and actual measured dashed lines. Furthermore, an example of a missing code is given in the picture. In a visualized way the nonlinearity errors are shown to improve understanding.

2.5.5 Offset

Input amplifiers, output amplifiers, and comparators in practical circuits inherently have a built-in offset voltage and offset current. This offset is caused by the finite matching of components. The offset results in a non-zero input- or output voltage, current or digital code although a zero signal is applied to the converter.

Offset is very important in dc systems. Temperature dependence of the offset must be small. Trimming or auto zero procedures can remove the offset in a system. Furthermore, care must be taken during the layout of the circuit to avoid thermal coupling and thermal gradients over an integrated circuit. If such a coupling exists, then the output code or output signal show slow changing components depending on the applied input signal or input code. Such signal components are unwanted.

2.5.6 Temperature dependence

Monotonicity and linearity must be maintained over a large temperature range to keep distortion and signal-to-noise ratio within the specified range. Mostly this requires a very good thermal tracking of components. In an n-bit system with a relative accuracy of $\pm \frac{1}{4}$ LSB this linearity may change maximally by $\pm \frac{1}{4}$ LSB over the full temperature range to maintain monotonicity of the system. A $\pm \frac{1}{2}$ LSB linearity over the full temperature range is obtained in this way, while in binary weighted systems this linearity specification automatically includes *monotonicity* of the converter over the full temperature range.

If we have a variation in temperature of ΔT, then the difference in thermal

tracking for components must not exceed a value of

$$\frac{2^{-n}}{4\Delta T} \quad \text{per degree C.} \tag{2.18}$$

The error introduced by the thermal mismatch in this case amounts to $\frac{1}{4}$ LSB over a temperature range of ΔT.

Because the most significant bits in a converter must have a high accuracy, the thermal tracking of these bits must be very good. The estimate given in 2.18 is only needed for most significant bit matching. In a 16-bit system subjected to a temperature change of 105^0 C this means that the temperature tracking of components should not exceed 0.04 ppm per degree C. In this analysis it is supposed that the linear (first-order) temperature coefficient is much larger than the second-order term. Sometimes the first order temperature coefficient is reduced by a clever design. At that moment the second order coefficient takes over.
All specifications are performed at a specified temperature (usually 25^oC) and over the full temperature range: -20^oC to $+85^oC$ for consumer and -55^oC to $+125^oC$ for military applications are commonly used temperature ranges.

2.5.7 Supply voltage

Specifications of converters are given at nominal supply voltages. Variations in supply voltages usually may not exceed a $\pm 5\%$ tolerance. To include these minimum and maximum supply voltage boundaries, a specification about the supply voltage dependence of a parameter is given, allowing the user to determine the error budget.

Additional specifications about power dissipation, input bias currents, reference impedance, clock input, output loading, and fan-in and fan-out of the logic system are needed.

2.6 Dynamic specifications

2.6.1 Signal-to-Noise Ratio

The most important dynamic specification of a converter is the signal-to-noise ratio. This signal-to-noise ratio depends on the resolution of the converter and automatically includes specifications of linearity, distortion, sampling time uncertainty, glitches, noise, and settling time. Over half the

sampling frequency, this signal-to-noise ratio must be specified and should ideally follow the theoretical formula: $S/N_{max} = 6.02\ \mathrm{n} + 1.76\ \mathrm{dB}$.

This S/N ratio is calculated for a sine wave input with a maximum amplitude. The ratio between the frequency of the sine wave and the sampling frequency should be irrational. In case input signals with a smaller amplitude are applied, then the S/N ratio decreases in accordance to the input signal decrease.

Specifications must be given as a function of the signal frequency with various amplitudes and as a function of amplitude with a constant signal frequency. An even more stringent dynamic performance definition is obtained if the total harmonic distortion (THD) of the converter is added to the quantization error. Even in this case the maximum signal-to-noise ratio of a high-performance converter must be close to the above given formula. In Figure 2.9 the signal-to-noise ratio of a converter as a function of frequency from full scale to -30 dB in steps of -10 dB is shown. The sampling frequency of the 16-bit converter is 176.4 kHz and the measuring bandwidth is 20 kHz. Note that at lower output amplitudes the signal-to-noise ratio in the frequency range from 10 kHz to 20 kHz is at maximum. Distortion products of signals above 10 kHz are rejected by the output reconstruction filter.

In Figure 2.10 the signal-to-noise ratio as a function of amplitude is shown. The signal frequency is 1 kHz, while in this situation a sampling frequency of 44.1 kHz is used. At full-scale output a larger deviation from the theoretical 16-bits line in observed. Measuring bandwidth is 20 kHz.

2.6.2 Spurious Free Dynamic Range

When converters are used with large oversampling ratios or the spectral purity of the converter is important, an additional specification determining the ratio between the maximum signal component and the largest distortion component can be obtained. This ratio is called Spurious Free Dynamic Range (SFDR). In Figure 2.11 an amplitude spectrum of a converter is shown. From the figure it is seen that the SFDR ratio is obtained at the moment a maximum signal is applied to the converter. The ratio between the amplitude of the signal and the largest distortion component is defined as maximum distortion-free dynamic range of the converter.

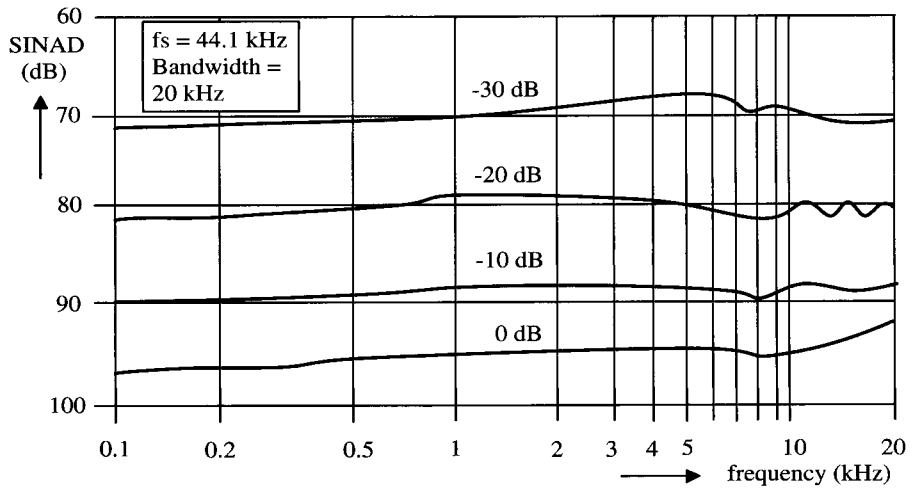


Figure 2.9: Signal-to-(noise plus distortion) ratio as a function of frequency with various amplitude values

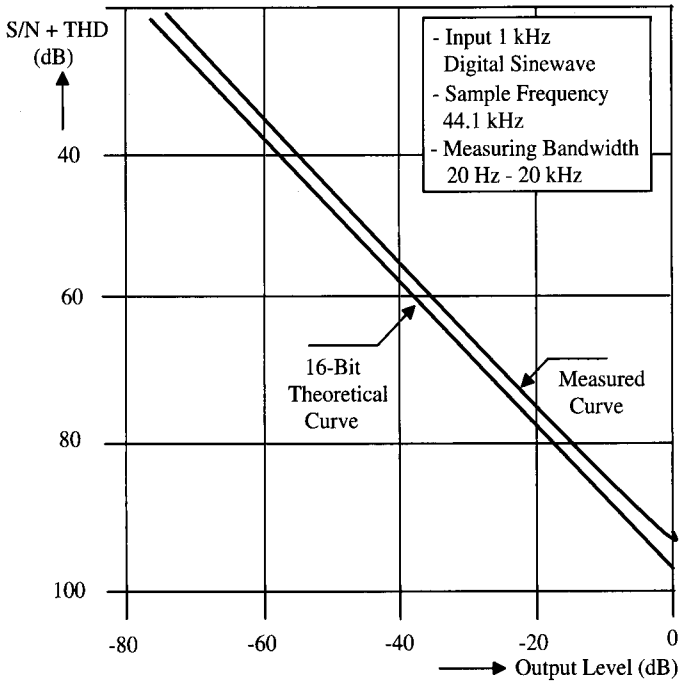


Figure 2.10: Signal-to-(noise plus distortion) ratio as a function of amplitude

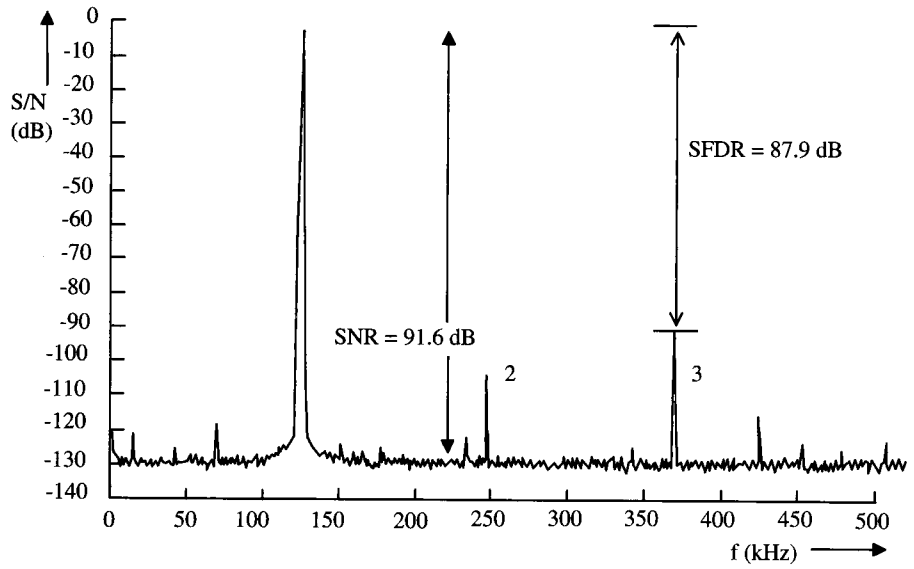


Figure 2.11: Definition of Spurious free Dynamic Range

Note that in Figure 2.11 the measuring bandwidth of the spectrum analyzer is much smaller than the total bandwidth (in this case 250 kHz) over which the signal-to-noise ratio is determined. Using such a small bandwidth results in an accurate determination of the different distortion products of a converter.

Converters with a good integral linearity usually give an SFDR that is larger than the signal-to-noise ratio of the system. To prove this statement, suppose a converter with n_d distortion components is analyzed. Furthermore, it is adopted that the n_d distortion components have equal amplitude and are a factor a_d attenuated with respect to the total noise of the system. Then we obtain for the total noise plus distortion (q_{nd}) in the system:

$$q_{nd} = q_n \sqrt{1 + \frac{n_d}{a_d^2}}. \tag{2.19}$$

The signal-to-noise ratio in this system will be reduced by the distortion of the converter. In the following table the influence of the distortion on the total performance of the converter is shown with $a_d = 3.162$ (10 dB) and n_d varies from 1 to 4. In practical converters mostly second and third harmonic distortion is found. In that case $n_d = 2$ and from Table 2.2 a loss of 0.8 dB

n_d	q_{nd}/q_n
1	1.05
2	1.10
3	1.14
4	1.18

Table 2.2: Signal-to-noise reduction ratio as a function of distortion products

in signal-to-noise ratio compared to an ideal converter gives a SFDR that is 10 dB larger than the signal-to-noise ratio.

Equation 2.19 shows that a large SFDR requires a converter with a signal-to-noise ratio as close as possible to the theoretical attainable value.

2.6.3 Effective Number Of Bits (ENOB's)

To get a comparison method for converters the Effective Number of Bits (ENOB's) is measured under Nyquist conditions. The dynamic range of the converter measured includes quantization errors, clock jitter errors, distortion errors and circuit noise. Then the ENOB's are defined as:

$$ENOB = \frac{SNDR_{measured} - 1.76}{6.02} \tag{2.20}$$

Using this definition it is very easy to compare analog-to-digital or digital-to-analog converters with the same number of bits, but due to different circuit designs having different performance.

2.6.4 Dynamic range versus converter linearity

At the moment the signal-to-noise plus distortion (SINAD) of a converter is measured as a function of the converter construction, the results shown in Figure 2.12 can be obtained. The dynamic range of an ideal 16-bit converter is a straight line. At the moment a converter uses an algorithm to obtain monotonicity without guaranteeing the integral nonlinearity specification of $\frac{1}{2}$ LSB then the curve called segmented D/A converter is obtained. The distortion in the system reduces the maximum dynamic range. At the moment a non-monotonic design is measured, then the third curve called basic D/A converter is obtained. Because of the non-monotonicity of the converter the distortion starts at about -40 dB from the maximum output

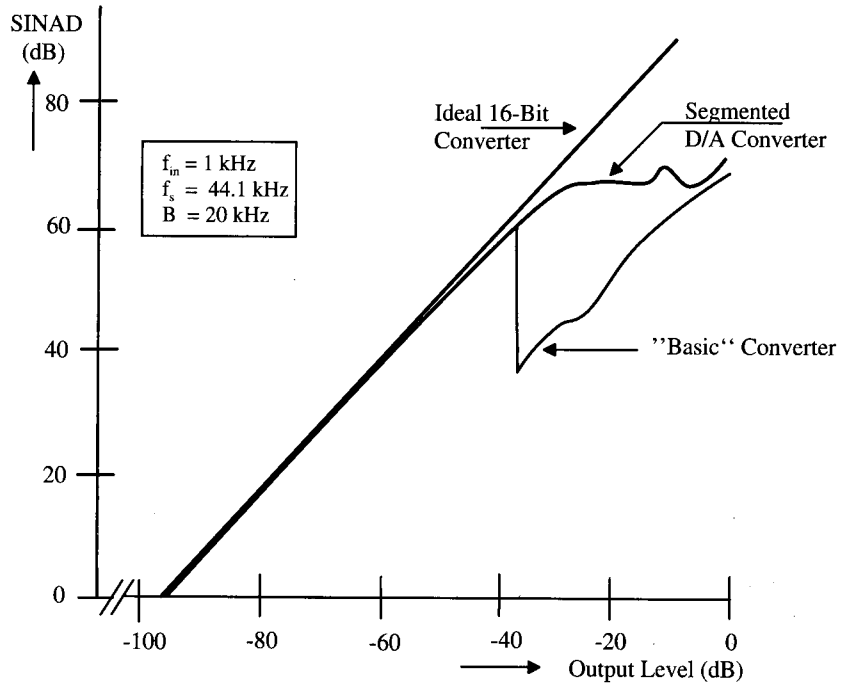


Figure 2.12: SINAD as a function of converter construction

level. This distortion reduces the dynamic range with about 20 dB when non-monotonicity is observed. The amount of dynamic range reduction by entering the non-monotonic relation between input and output signal of the converter depends on the matching of the components. Practical matching properties are about 0.1 % resulting in a monotonic range of about 60 dB. This result is obtained in Figure 2.12.

2.6.5 Required accuracy of converter elements

When designing converters with resolutions from 8 to 16 bits the following question arises:

How accurate do I need to design the unit currents or resistors to obtain a certain INL and/or DNL?

To answer this question a Matlab program has been used to obtain information about the INL and ENOB and INL and SFDR performance of converters. The converters have been modeled using unit current sources or

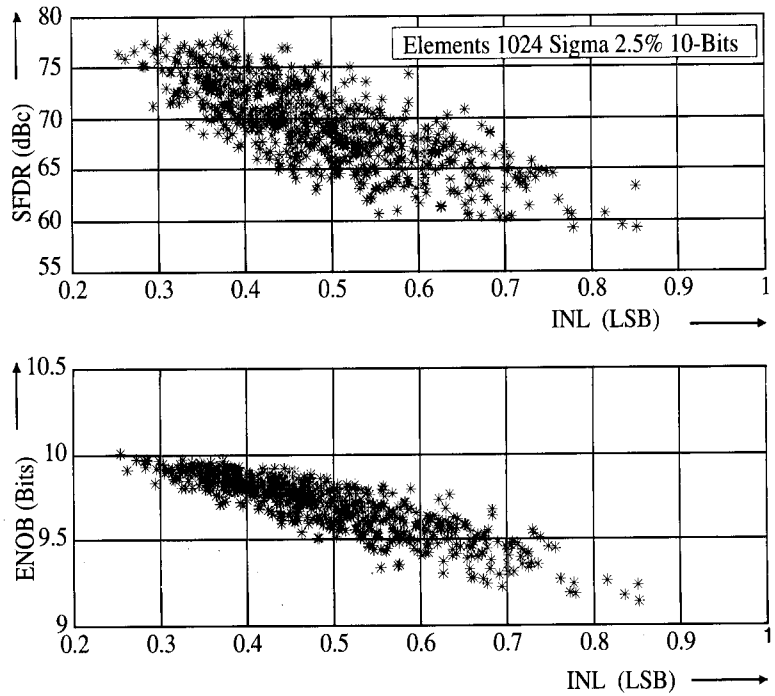


Figure 2.13: SFDR and ENOB of a 10-bit converter versus INL

unit resistors to determine every quantization level. This means that in a 10-bit converter 1024 elements are used. In Fig. 2.13 the simulation results for a 10-bit converter are shown. A total number of 1000 "converters" have been analyzed using this program. At the same time the ratio between the largest distortion component and the signal component defined as Spurious Free Dynamic Range (SFDR) is shown too. The matching of the unit resistor elements has a σ of 2.5 % in this simulation. In Fig. 2.14 a histogram of SFDR and ENOB of the converters is shown. This histogram shows that 1σ of the converters reaches $\pm\frac{1}{2}$ LSB INL and 3σ are within 1 LSB INL.

2.6.6 Element matching versus INL of 8 to 14 bit converters

In the range of 8 to 14 bits of resolution of a converter simulations have been performed. As a result of these simulations Fig. 2.15 shows the relation between the required unit element matching and the linearity (INL) of a 8-bit converter. In Fig. 2.16 the results of a simulation of a 10-bit converter

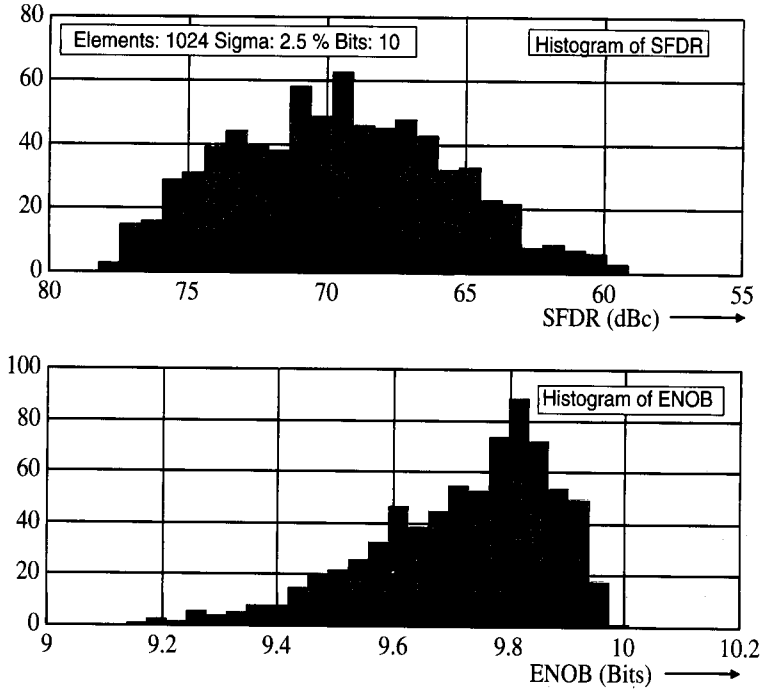


Figure 2.14: Histogram of SFDR and ENOB of 1000 10-bit converters

are shown. To increase the amount of data simulations for 12 and 14 bit converters will be shown too. In Fig. 2.18 the results of a simulation of a 14-bit converter are shown. From these simulation results it can be seen that with a linearity better than .5 LSB the σ of the resistor matching must be below the value indicated by the arrow. Although above the indicated value still a good linearity can be obtained, a yield problem is introduced. The indicated limits give about 99 % yield to obtain .5 LSB linearity or 1 LSB linearity. In tabular form the results of resistor matching versus the converter accuracy for different converter resolutions can be organized as shown in Table 2.3.

It must be noted, that in case a segmented or binary weighting in a converter is used, then the matching accuracy between the segmented elements or the binary weighted elements increases according to the value or the amount of elements used to obtain the required weight. In practice mostly a number of elements is put in parallel to increase the unit value. As a result the

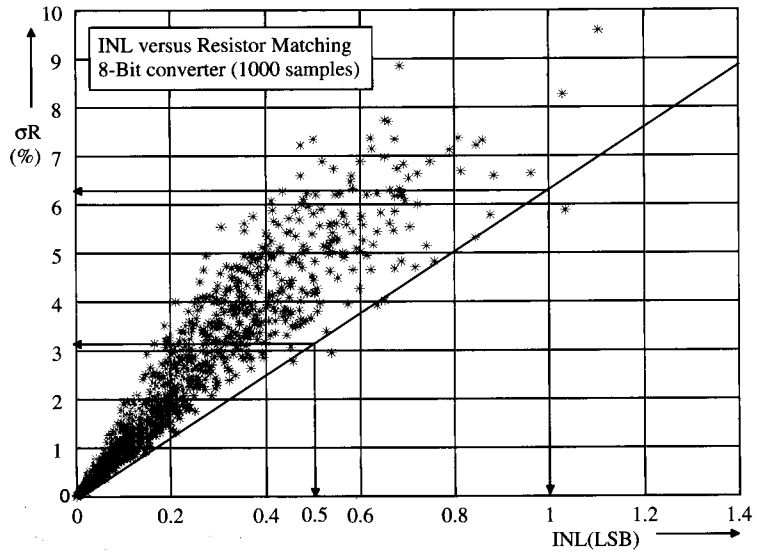


Figure 2.15: Relation between INL and unit element matching (8-bit)

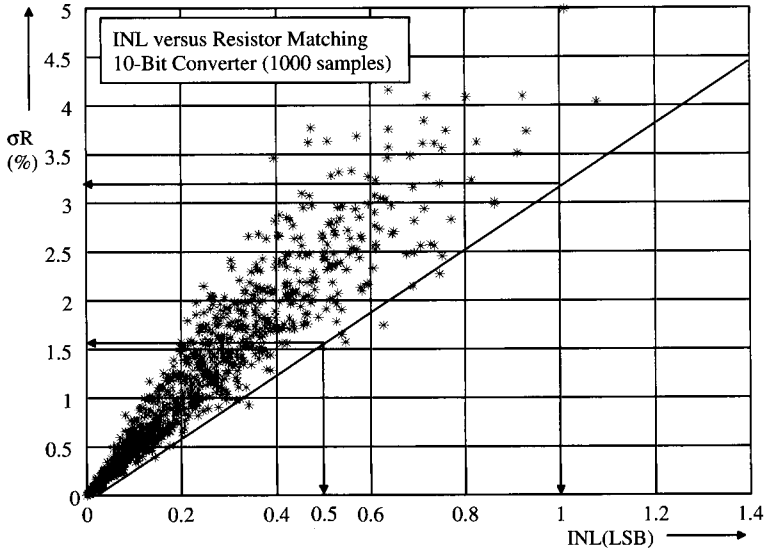


Figure 2.16: Relation between INL and unit element matching (10-bit)

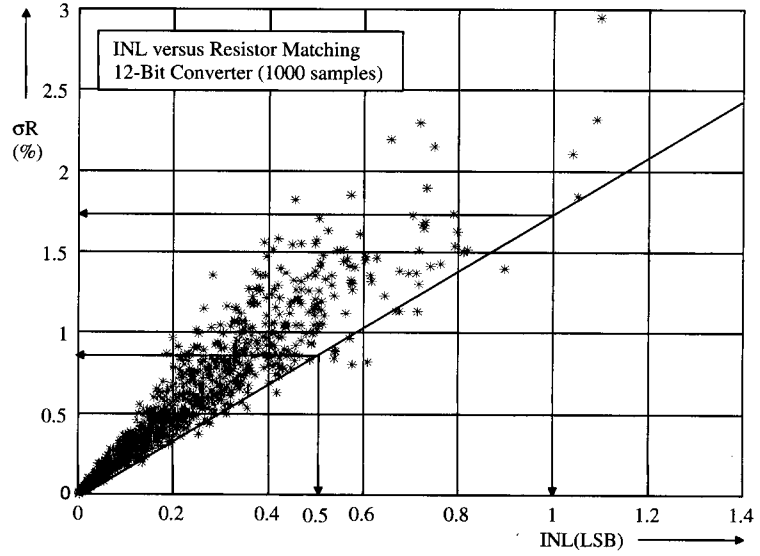


Figure 2.17: Relation between INL and unit element matching (12-bit)

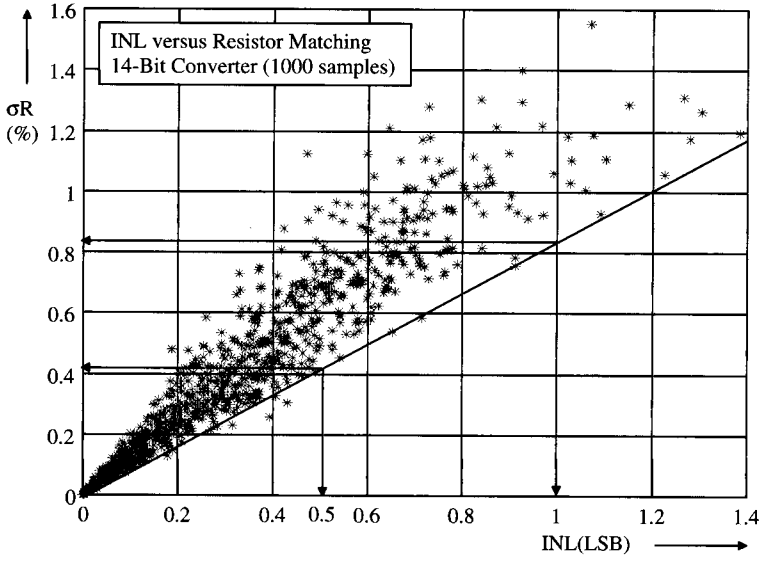


Figure 2.18: Relation between INL and unit element matching (14-bit)

Number of Bits	INL $\approx \frac{1}{2}$ LSB	INL $\approx$ 1 LSB
8-bit	3.1 %	6.2 %
10-bit	1.6 %	3.1 %
12-bit	0.9 %	1.7 %
14-bit	0.4 %	0.85 %

Table 2.3: Resistor matching versus converter accuracy data

accuracy increases with $\sqrt{N}$.

2.6.7 ENOB and SFDR versus INL converter model

The finite matching of components in a converter results in a limited linearity of such a converter. A very useful relation between INL and reduction in ENOB of a converter will be introduced. Furthermore an estimate for the SFDR of the converter will be derived too.
The transfer function of a converter in an ideal case equals 1. However, due to non-linearity in the converter a deviation from the transfer function is obtained. The INL of the converter introduces this error. Suppose the transfer function is equal to:

$$V_{out} = V_{in}(1 + INL(LSB)). \tag{2.21}$$

Furthermore when an input signal with frequency f_{sig} is applied at this converter, then the Fourier components of the INL function result in harmonic distortion. A good model for the INL function need to be introduced at this point. The following can be said about the INL of a converter:

Converters in sub-micron CMOS technology use mostly differential structures. This means that even distortion components will be rejected. The INL function in such an application shows a mirror symmetrical function. As a result the following INL modeling will be used:

$$INL(LSB) = a_2 \cos(2\omega t) + a_4 \cos(4\omega t) + a_6 \cos(6\omega t) + ... \tag{2.22}$$

The cosine function is introduced here to obtain the mirror symmetrical function around the midtap of the converter. With an input $a_{sig} \sin(\omega t)$ applied to this system the output becomes using only three coefficients:

$$V_{out} = a_{sig} \sin(\omega t)(1 + a_2 \cos(2\omega t) + a_4 \cos(4\omega t) + a_6 \cos(6\omega t)). \tag{2.23}$$

The result of the equation gives only odd harmonics of the input signal:

$$V_{out} = a_{sig}(1+\frac{1}{2}a_2)\sin(\omega t) + \quad (2.24)$$

$$\frac{1}{2}a_{sig}(a_2+a_4)\sin(3\omega t) + \quad (2.25)$$

$$\frac{1}{2}a_{sig}(a_4+a_6)\sin(5\omega t) + \quad (2.26)$$

$$\frac{1}{2}a_{sig}a_6\sin(7\omega t). \quad (2.27)$$

When an input signal is applied, then this signal with frequency ω modulates the INL function with the same frequency and harmonics are found. As is shown here, the output distortion frequency shifts with the signal frequency to both sides of the distortion component. Suppose now that the

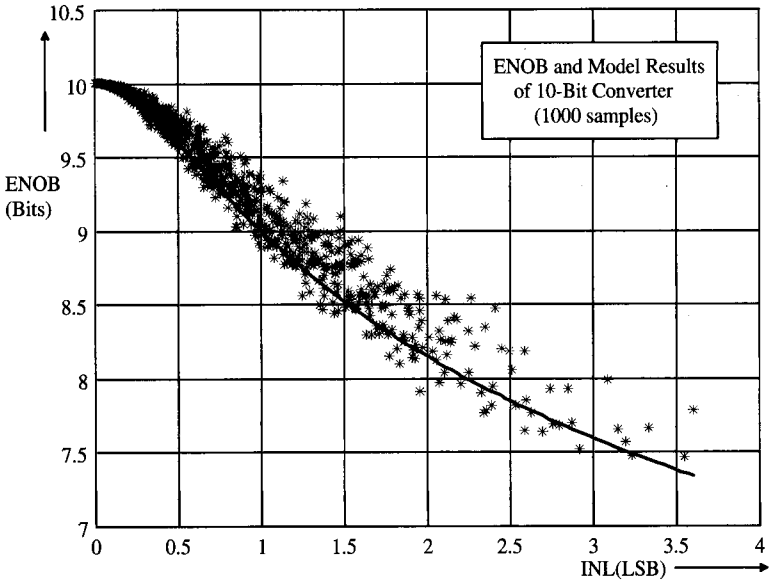


Figure 2.19: INL versus ENOB reduction model

INL error function is described by a_4 only, then a third and fifth harmonic will appear at the output of the converter. The amplitude of these distortion components are equal and the power can be calculated. The error power becomes:

$$P_{distortion} = 2.(\frac{1}{2\sqrt{2}}a_4)^2 = \frac{a_4^2}{4}. \quad (2.28)$$

This distortion power adds to the quantization error power to obtain the effective number of bits (ENOB's) of the converter. Furthermore when only one distortion component is present then the value of a_4 is equal to $\mid INL \mid$, with INL expressed in LSB's (q_s).
The total quantization plus distortion power becomes:

$$P_{total} = N + N_{INL} = \frac{q_s^2}{12} + \frac{a_4^2}{4} = \frac{q_s^2}{12}(1+3 \mid INL \mid^2). \quad (2.29)$$

In this equation a_4 is defined as:

$$a_4 = \mid INL \mid q_s. \quad (2.30)$$

The ENOB's can be obtained from:

$$ENOB = \frac{S}{N+N_{INL}} = \frac{S}{N}.\frac{N}{N+N_{INL}} = \sqrt{1.5}\ 2^n\ 2^{-\frac{\log(1+3*|INL|^2)}{2\log 2}} \quad (2.31)$$

This analysis has been given for one distortion component. In a practical converter a number of distortion components will appear. However, depending on the construction of a converter it is possible that a certain INL mask appears. This mask will introduce steady distortion parts resulting in a reduction of the effective number of bits. To verify this simple model an analysis has been performed on 1000 random designs of 10-bit converters. In Fig. 2.19 the simulation results of the random converters and the simple model equation are given.
Here $2|INL|$ is the peak to peak systematic signal distortion component due to finite converter accuracy. This value gives the worst case condition, because it is not known how the INL curve as a function of the signal value behaves. A Fourier analysis would give exactly the value of the different distortion components and in that way a better estimation of the total distortion can be obtained. The figure shows that in general equation 2.31 gives a good practical estimate for the ENOB's of a converter. This equation shows furthermore that the reduction in effective number of bits is independent of the resolution of the converter. Therefore the following will be introduced to define the reduction in bits:

$$n_{reduction} = \frac{\log(1+3*|INL|^2)}{2\log 2}. \quad (2.32)$$

In Fig. 2.20 the worse case reduction in ENOB's of a converter as a function of the INL is shown. This graph is very useful to get quick information about the converter resolution and the linearity. It must be noted, however, that

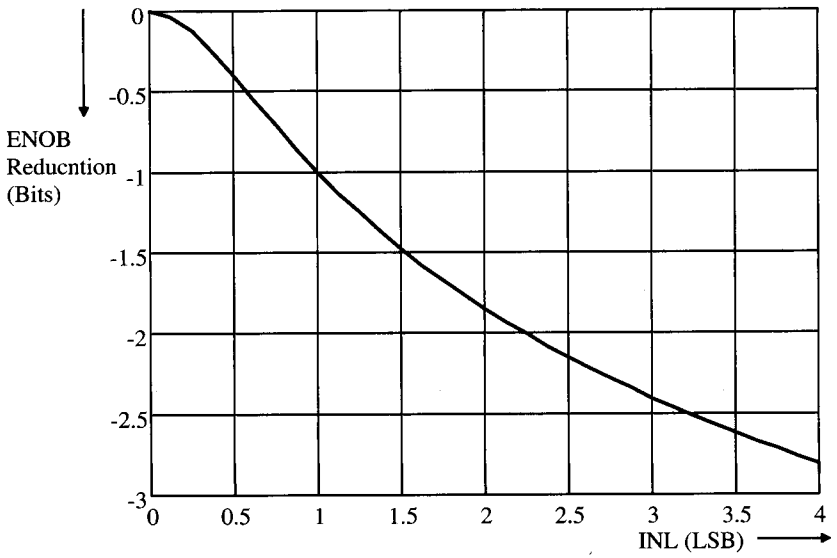


Figure 2.20: ENOB Reduction vs INL of a Converter

in the given analysis the converter reference has been constructed using the same amount of reference elements as the resolution of the converter (2^n). In many applications, however, the amount of elements is much smaller than the amount of steps defined by the converter. In that case the accuracy of the elements calculated before must be increased with a factor equal to the square root out of the ratio between the effective used elements and the resolution of the converter.
As an example, suppose that 64 elements are used to define the "coarse" levels of a 10 bit converter, then the accuracy of the element matching must be increased with a factor M:

$$M = \sqrt{\frac{1024}{64}} = 4. \tag{2.33}$$

As a result the matching between the 64 elements in the converter must be better than 1.6%/4 = .4%. The ENOB is reduced with .5 LSB.

SFDR calculation

The spurious free dynamic range SFDR of a converter can be modeled in the same way. The distortion component a_4 will be used again. The distor-

tion components are equal and therefore only the amplitude of one of the harmonics is sufficient to obtain the SFDR, We obtain for this component:

$$a_{distort} = \frac{1}{2}a_4 = \frac{1}{2} \mid INL \mid q_s. \tag{2.34}$$

Note that this is the peak amplitude of the distortion and that $(2^N - 1)q_s$ is the peak-to-peak input signal amplitude.
One problem occurs at the moment an ideal converter is analyzed. In that case the largest quantization distortion component determines the SFDR. From an earlier analysis it is known that the amplitude of the quantization distortion component varies with the resolution of a converter as:

$$a_{quantization} = 2^{-1.5N_{bits}} q_s. \tag{2.35}$$

This means that the largest amplitude determines the SFDR as a function of INL. The SFDR of a converter becomes:

$$SFDR = \frac{1}{\mid INL \mid 2^{-Nbits} + 2^{-1.5N_{bits}}}. \tag{2.36}$$

Expressed in decibels the SFDR becomes:

$$SFDR(dB) = -20\log(\mid INL \mid 2^{-N_{bits}} + 2^{-1.5N_{bits}}). \tag{2.37}$$

Again simulations have been performed to verify the validity of this equation using 1000 random generated 10-bit converters. The result of the SFDR analysis and the model are shown in Fig. 2.21. This analysis shows that the model describes sufficiently accurate the SFDR of practical converters.

2.6.8 Intermodulation modeling

The intermodulation of a converter is obtained with two input frequencies ω_1 and ω_2 applied to the converter. The signals must half less than half full scale amplitude to avoid overload of the converter. The frequency difference between the two frequencies is mostly small (In AM radio channels 9 kHz for example). The intermodulation of a converter can be modeled using the same relation for the INL of a converter but then for the two input frequencies:

$$INL(LSB) = a_2\cos(2\omega_1 t) + a_2\cos(2\omega_2 t) + a_4\cos(4\omega_1 t) + a_4\cos(4\omega_2 t) + ... \tag{2.38}$$

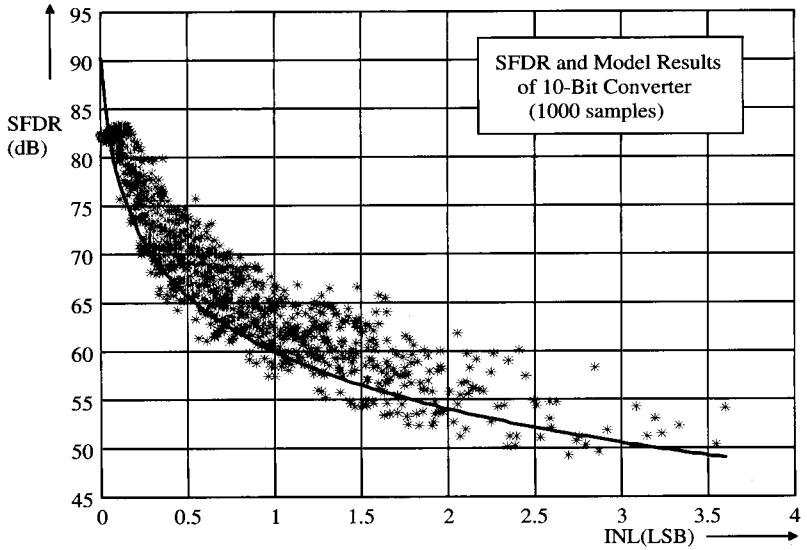


Figure 2.21: SFDR and model results versus INL of a Converter

The cosine function is introduced again to obtain the mirror symmetrical function around the mid tap of the converter. With an input signal equal to:

$$\frac{1}{2}a_{sig1}\sin(\omega_1 t) + \frac{1}{2}a_{sig2}\sin(\omega_2 t) \tag{2.39}$$

applied to this system the output signal becomes using only coefficient a_2:

$$V_{out} = (\frac{1}{2}a_{sig1}\sin(\omega_1 t) + \frac{1}{2}a_{sig2}\sin(\omega_2 t))(1 + a_2\cos(2\omega_1 t) + a_2\cos(2\omega_2 t)). \tag{2.40}$$

The intermodulation terms become after rearranging the equation:

$$int_1 = \frac{1}{4}a_{sig1}a_2\sin((2\omega_1 - \omega_2)t) \tag{2.41}$$

$$int_2 = \frac{1}{4}a_{sig2}a_2\sin((2\omega_2 - \omega_1)t). \tag{2.42}$$

$$\tag{2.43}$$

Note that **only** the intermodulation frequencies have been calculated resulting in two output signals. The signal (S) to intermodulation ($int_{1,2}$) ratio

becomes referred to a single input signal:

$$\frac{S}{int_{1,2}} = \frac{2}{a_2}. \tag{2.44}$$

Supposing that the term a_2 is the only nonlinearity of the converter, then this term can be again related to the INL of the converter resulting in:

$$a_2 = \mid INL \mid q_s. \tag{2.45}$$

The intermodulation component is referred to an input signal amplitude of half full scale. Furthermore a_2 is a peak amplitude while the full scale range of the converter is a peak-to-peak amplitude. Thus a_2 becomes:

$$a_2 = \mid INL \mid q_s = \mid INL \mid 2^{-N_{bits}+1}. \tag{2.46}$$

With full scale value equals 1.
However, when the converter has an ideal linearity, then still due to quantization intermodulation products appear. These components depend on the number of bits as:

$$int_{quantization} = 2^{-2N_{bits}}. \tag{2.47}$$

The final result for the intermodulation including quantization components gives:

$$\frac{S}{int_{1,2,total}} = \frac{1}{\mid INL \mid 2^{-N_bits} + 2^{-2N_{bits}}}. \tag{2.48}$$

Furthermore it is known that:

$$SFDR = \frac{1}{\mid INL \mid 2^{-Nbits} + 2^{-1.5N_{bits}}}. \tag{2.49}$$

This means that in case a final nonlinearity exists, the intermodulation can be approximated by:

$$\frac{S}{int_{1,2,total}} \approx SFDR \approx \frac{1}{\mid INL \mid 2^{-Nbits} + 2^{-1.5N_{bits}}}. \tag{2.50}$$

This equation is valid for those converters that have an INL distortion component mostly depending on a_2. When other components are dominant then the intermodulation distortion components appear at higher signal frequencies. However, in digital radio receivers a number of channels may be present for conversion. As a result of more than two channels present, these channels can cause intermodulation distortion that appears in the wanted channel. In Fig. 2.22 the calculated intermodulation distortion and the model given by equation 2.50 are shown. This plot shows a reasonable fit with the simple model.

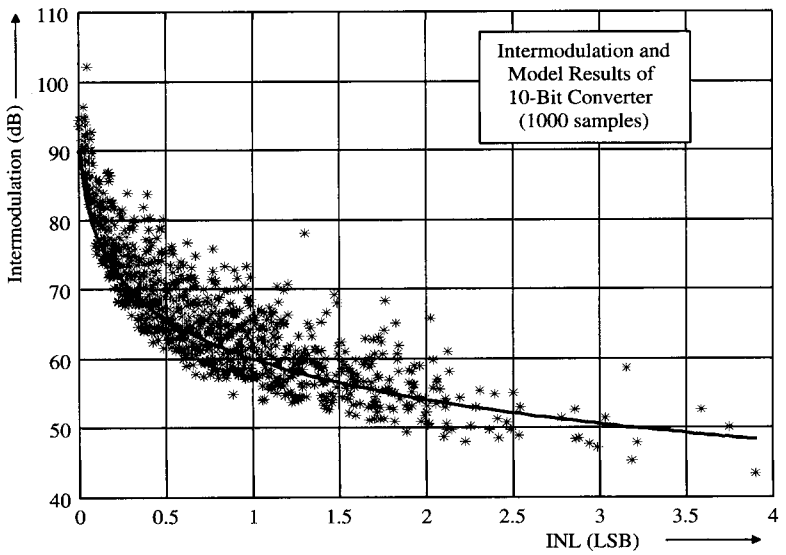


Figure 2.22: Intermodulation and model results versus INL of a Converter

2.6.9 Glitches

Glitches are usually important for the performance specification of D/A converters. A glitch is generated when during a major carry code transition the new code signal value appears before or after the signal value of the former code disappears. The largest glitch is mostly generated by a major carry transition around the MSB level. In Figure 2.23 a glitch at the major carry transition is shown. The glitch obtained at the output of the D/A converter is generated by a slow switching on of the MSB bit value. As a result the output signal jumps from the value given by 01111 through 00000 to 10000. A sharp glitch is generated at the output which results in distortion giving a decrease is signal-to-noise ratio.To perform worst case calculations on the influence of timing on the glitch size a styled square glitch is used. In Figure 2.24 this styled glitch is shown. Suppose the full-scale (peak-to-peak) amplitude of the converter equals $2A$, then the MSB value is close to A. Furthermore, the difference in switching time is defined as t_{dif}. The glitch-area error is then equal to:

$$E_{glitch} = At_{dif} \quad Vsec. \tag{2.51}$$

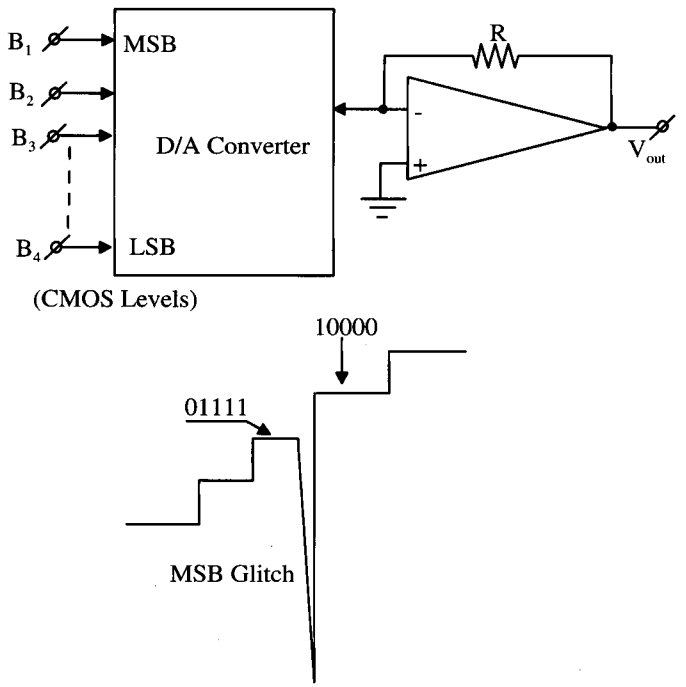


Figure 2.23: Major carry glitch

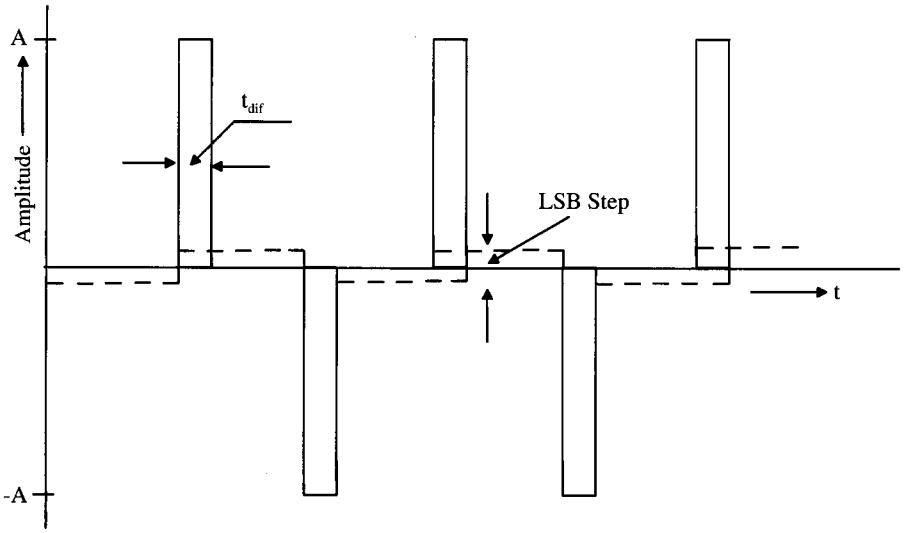


Figure 2.24: Styled glitch of a converter

As an example, the glitch error of a 16-bit D/A converter will be calculated compared to the LSB bit value.

Suppose the switching time difference $t_{dif} = 1$ nsec and the full-scale value of the converter is 1 V, then the glitch error becomes: $E_{glitch} = 500$ pVsec.

The LSB area now equals:

$$E_{LSB} = 2^{-n+1} A t_s \quad Vsec. \tag{2.52}$$

With a sample time t_s of 20 μ sec for the converter and $n = 16$ we obtain:

$E_{LSB} = 300$ pVsec.

The glitch error in this example is about one and a half times larger than the LSB area. To qualify this converter as "good," the glitch error must be at least reduced by a factor three.

From equations 2.51 and 2.52 the time difference t_{dif} can be expressed as:

$$t_{dif} = g 2^{-n+1} t_s \tag{2.53}$$

with:

$$g = \frac{E_{glitch}}{E_{LSB}}. \tag{2.54}$$

A solution to reduce the glitch error is the addition of a so-called "deglitcher" circuit at the output of a D/A converter. However, such a deglitcher circuit uses an analog storage element to hold the output signal during the code transition. Such a deglitcher circuit with a distortion level below the LSB level is difficult to design. In practical solutions it is simpler to optimize data latch and bit-switch for minimum glitch energy. Mostly in the latter case a better performance is obtained. Glitches exhibit in the output signal of a D/A converter as distortion, thus reducing the signal-to-noise ratio compared to the maximum theoretical value. When oversampling of a converter is used to obtain a larger dynamic range (S/N ratio), the distortion products introduced by the glitches counteract the increase in dynamic range, including distortion.

An example of a measured MSB-glitch of a 14-bit D/A converter is shown in Figure 2.25. The output signal is measured across a 25 ohm load resistor. Full-scale value under this measuring condition is 50 mV. The signal

is directly applied to a 1 Ghz bandwidth oscilloscope without using an operational amplifier to convert the D/A current signal into a voltage. The

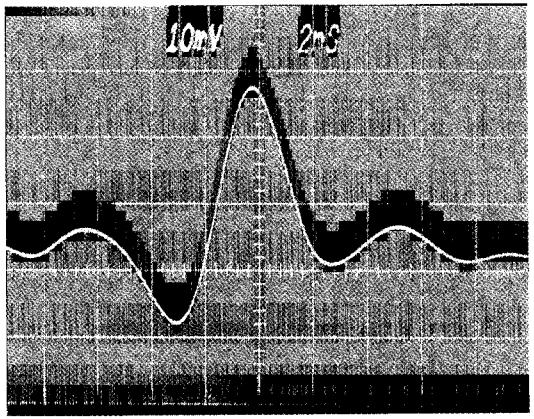


Figure 2.25: Measured MSB-glitch error

glitch energy becomes even more important in systems that use a large oversampling ratio together with a noise-shaping technique. In such systems an *averaging* of signals occurs. This means that the number of MSB transitions that generate a glitch are increased to more than the minimum number required in generating, for example, a sine wave. At that moment the amount of glitch energy adds to the output signal. As a result the dynamic range and the distortion of the system do not decrease as much as expected by the theoretical analysis of the system.

2.6.10 Noise

Thermal noise (white noise) of bit-currents, amplifiers, resistors, and so on, adds to the quantization noise. This thermal noise exhibits itself as a deviation from the theoretical maximum signal-to-noise ratio that an ideal converter can have. When the thermal noise specification is given for a converter, this figure is not a measure for the (dynamic) signal-to-noise ratio of the system. However, the noise of the individual bit currents must be much lower than the quantization "noise" of the system.

A simple calculation demonstrates the decrease in signal-to-noise ratio of a system compared to the signal-to-noise ratio of the basic converter in that system. Define the noise power of the quantizer as $N_{quantizer}$ and the thermal noise power of the system as $N_{thermal}$. When there exists no correlation

between the noise sources, then the total noise in the system (N_{system}) will be:

$$N_{system} = \sqrt{N_{quantizer}^2 + N_{thermal}^2}. \tag{2.55}$$

In rewriting equation 2.55 to the quantizer noise, the result becomes:

$$N_{system} = N_{quantizer}\sqrt{1 + \frac{N_{thermal}^2}{N_{quantizer}^2}}. \tag{2.56}$$

The ratio $\frac{N_{thermal}^2}{N_{quantizer}^2}$ can be expressed as a ratio between the signal-to-noise ratios of the individual parts of the system. Then equation 2.56 changes into:

$$N_{system} = N_{quantizer}\sqrt{1 + \frac{(S/N_{quantizer})^2}{(S/N_{thermal})^2}}. \tag{2.57}$$

Suppose further that the ratio between the signal-to-noise ratios of the thermal part and the quantizer part is equal to k or:

$$k = \frac{S/N_{quantizer}}{S/N_{thermal}}. \tag{2.58}$$

Inserting equation 2.58 into equation 2.57 and normalizing this equation into the signal-to-noise ratio of the total system, we obtain:

$$S/N_{system} = S/N_{quantizer} \times \frac{1}{\sqrt{1+k^2}}. \tag{2.59}$$

This calculation is only valid if there exists no correlation between the quantization noise (error) and the thermal (white) noise.

With $k^2 \ll 1$ this can be rewritten as:

$$\frac{1}{\sqrt{1+k^2}} \simeq (1 - \frac{1}{2}k^2). \tag{2.60}$$

Thus:

$$S/N_{system} = S/N_{quantizer}(1 - \frac{1}{2}k^2). \tag{2.61}$$

Inserting for $k = \frac{1}{3}$, then:

$$S/N_{system} = 0.95 S/N_{quantizer}. \tag{2.62}$$

This means that in a 16-bit D/A converter system with a theoretical signal-to-noise ratio of 98.1 dB, the thermal signal-to-noise ratio must be at least

108 dB (k = $\frac{1}{3}$ $\approx$ −9.5 dB) to get an overall signal-to-noise ratio loss in a system of not more than 0.5 dB.

In flash-type analog-to-digital converters a large comparator bandwidth is required to quantize an input signal with low distortion. In Chapter 11 the ratio between maximum analog input frequency and comparator bandwidth will be determined. As a result of the large comparator bandwidth it is difficult to keep the (thermal) noise in the system low enough not to deteriorate the dynamic range of the system. In A/D converters using a successive approximation conversion method, an identical phenomenon concerning noise is found.

The noise generated in the input circuits causes a "dithering" of the comparator at the transition levels between the successive quantization levels. We also have to add the aliasing noise. In Figure 2.26 a Gaussian distribution curve of noise is assumed. Here σ is the rms value of the noise. The

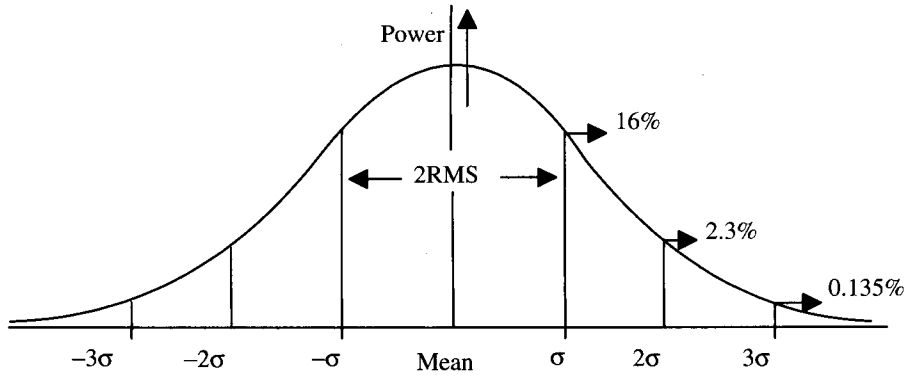


Figure 2.26: Gaussian distribution curve of noise

effect of noise on the signal-to-noise ratio of an A/D converter is estimated using two dc biasing conditions for the converter.

The first estimate on the influence of noise on the maximum signal-to-noise ratio of an A/D converter is performed when this converter is operated at an input dc voltage equal to decision level A_j. In Figure 2.27 this situation is shown. In Figure 2.27 A_{j-n} represents the decision levels of a converter while Q_{j-n} are the corresponding quantization codes. Note that at a code level Q_{j-n} an input signal variation equal to $\pm\frac{1}{2}$ LSB does not change the output code of the converter. The condition given in Figure 2.27 is such that

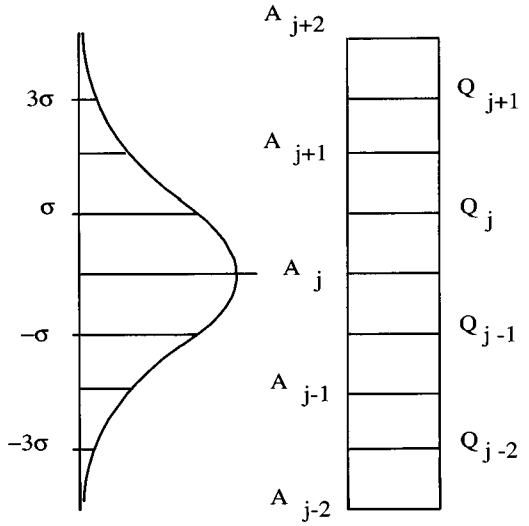


Figure 2.27: A/D input noise dc biased at decision level A_j

a comparator is always tripped resulting in a 1 LSB peak-to-peak output signal generation.

The next change in output code occurs when the levels A_{j+1} and A_{j-1} are tripped. This results in a peak-to-peak output code of 3 LSB. The following tripping levels result in a 5 LSB peak-to-peak output signal generation.

From Figure 2.27 it is found that the 2σ noise level is equal to 1 LSB or $e_{noise} = \sigma = \frac{1}{2}$ LSB. Looking at the distribution curve we can say that during 95 percent of the time the peak-to-peak quantization error is equal to 1 LSB. During the next 4.6 percent of the time the peak-to-peak error increases to 3 LSBs. The next 0.006 percent of the time the peak-to-peak error increases to 5 LSBs. The input noise trips the different quantization levels with steps equal to 1 LSB.

The output noise of the converter can now be estimated with respect to the noise level of a quantization step which is equal to 1 LSB. Adding the quantization noise powers, we obtain:

$$P_{total} = .954 \times q^2_{qnsLSB} + .046 \times q^2_{qns3LSB} + .00006 \times q^2_{qns5LSB}. \quad (2.63)$$

In this equation q^2_{qnsLSB} represents the quantization noise power of the LSB bit. The quantization error of the 3LSB level is 3 times larger (peak-to-

peak value) than the quantization error of the LSB bit. Furthermore the quantization error of the 5LSB level is 5 times larger (peak-to-peak value) than the LSB bit. If the next quantization level is tripped by noise, then the peak-to-peak value increases with 2 LSB. Inserting values into formula 2.63 gives:

$$P_{total} = q^2_{qnsLSB} \times 1.37. \quad (2.64)$$

This total power can be converted into a voltage across the same load resistance. This results in:

$$e_{total} = q_{qnsLSB} \times 1.16. \quad (2.65)$$

When no input signal is applied to the analog-to-digital converter, then an output noise equal to 1.16 times the noise of an LSB bit is generated.

At the moment the dc biasing of the converter is changed with a value of $\frac{1}{2}$ LSB, a dead zone is found equal to $\pm \frac{1}{2}$ LSB.

In Figure 2.28 this situation is shown. The first term in formula 2.63 disap-

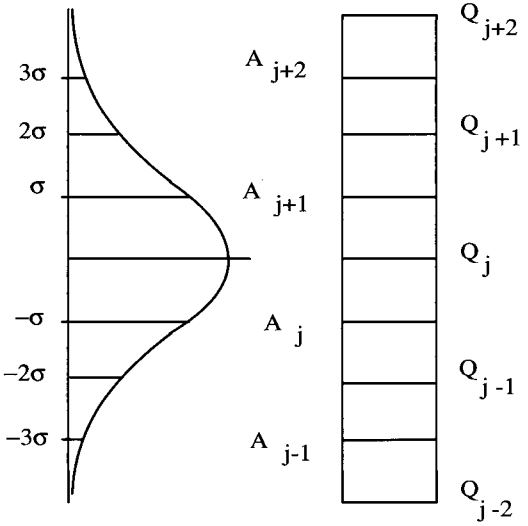


Figure 2.28: A/D noise level dc biased $\frac{1}{2}$ LSB above quantization level

pears. No output code appears because of the dead zone in the quantizer. An output code with a peak-to-peak value of 2 LSB appears at the output when the decision levels A_j and A_{j+1} are tripped.

As a result formula 2.63 now changes into:

$$P_{total} = .317 \times q^2_{qns2LSB} + .0027 \times q^2_{qns4LSB}. \quad (2.66)$$

Inserting values for the two quantization errors as defined above results in:

$$P_{total} = q^2_{qnsLSB} \times 1.31; \quad (2.67)$$

or, converted into a voltage, this value becomes:

$$e_{total} = q_{qnsLSB} \times 1.14. \quad (2.68)$$

So this analysis shows that the output noise nearly changes with changing input dc signal.
As already stated the rms value of the applied input noise equals $\frac{1}{2}$LSB = q_s. The noise power becomes:

$$P_{noise} = \frac{q_s^2}{4} \quad (2.69)$$

The quantization power equals:

$$P_{quantization} = \frac{q_s^2}{12} \quad (2.70)$$

The total power then becomes:

$$P_{total} = P_{noise} + P_{quantization} = \frac{q_s^2}{12}(1+3) \quad (2.71)$$

As a result the quantization error increases with $\sqrt{4} = 2$. This means that the dynamic range of the system decreases with 1 bit or 6 dB.
Using equations 2.64 and 2.67 the noise power can again be calculated. In this situation, however, the signal is a symmetrical square wave around zero with amplitude $\frac{1}{2}q_s$. So the power becomes:

$$P_{squarewave} = 1.3 \times \frac{q_s^2}{4} \quad (2.72)$$

The quantization power is again

$$P_{quantization} = \frac{q_s^2}{12} \quad (2.73)$$

The total power in this example results in:

$$P_{total} = P_{squarewave} + P_{quantization} = \frac{q_s^2}{12}(1+3.9) \quad (2.74)$$

In this case the dynamic range of the system reduces with $\sqrt{4.9} = 2.2$. So then the dynamic range of the system reduces with 1.15 bit or 6.9 dB.
In a good approximation generally it can be said that the dynamic range of a converter system reduces due to input noise in the system with a factor related to the quantization power and the extra (white) noise power. Total error power is the sum of quantization power plus noise power.
At the moment the noise level of the input amplifier and comparator of an analog-to-digital converter is reduced with respect to the example given above, then the noise at the output of the converter in terms of LSB values shows larger variations when the input dc signal changes with respect to the quantization levels. This can be seen from the following example. At the moment the output noise of the input condition given by equation 2.65 tends to approach the quantization error q_{qnsLSB}, the noise given by equation 2.68 tends to approach zero because of the dead-band introduced at quantization level Q_j. In this manner a very simple test of an A/D converter can be performed by simply changing the input bias condition and analyzing the output signal. A small input referred noise of a converter is found when during the bias condition variations zero output codes follow 1 LSB output codes. The input noise level is well below $\frac{1}{2}$ LSB.

In this calculation it is supposed that the noise applied at the input of the A/D converter has a bandwidth that does not exceed half the sampling bandwidth. If the noise bandwidth is much larger than half the sampling frequency, the noise increases by a factor $\sqrt{2\frac{f_b}{f_s}}$. Here f_b is the bandwidth of the input amplifier-comparator stage. The results of formulas 2.65 and 2.67 must be multiplied by this factor.

Designers of high-resolution A/D converters must be aware of this noise phenomenon.

2.6.11 Minimum reference step size

In parallel type analog-to-digital converters a number of reference voltages for each comparator level are mostly generated by a resistor network. At the moment the input signal is smaller than the reference voltage the comparator gives a "0," while with a larger input voltage the comparator gives a "1." Although this sounds very simple, every comparator generates its own non-correlated thermal noise. These noise sources can result in inaccurate decisions, although compared to the reference voltage the input signal can be smaller for a certain comparator, because of noise a wrong decision may

occur. The minimum step size needed in the reference network can be calculated referred to the noise generated in every comparator. For simplicity the $\frac{1}{f}$ noise component is neglected to simplify the calculations. In bipolar technologies this simplification is mostly allowed.

Suppose the noise shows a Gaussian distribution with probability density:

$$P(x) = \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{(x-m)^2}{2\sigma^2}}. \tag{2.75}$$

In equation 2.75 σ is the standard deviation and can be put equal to the rms value of the signal (noise). m is the mean value and is zero in the case of noise.

Integration of equation 2.75 gives the probability that the amplitude of a signal is within a predetermined range.
At the moment large values for σ are considered, an approximation can be used for the integral of the probability density. The one-sided (one tail) result of this approximation is given in 2.76.

$$Q(k) = \frac{1}{\sqrt{2\pi}k} e^{-\frac{k^2}{2}}. \tag{2.76}$$

This approximation is only valid for k$\gg$ 1.

Furthermore, k gives the number of times a signal is larger than σ.
The possibility that the noise amplitude is larger than kσ is determined by 2Q(k), or

$$2Q(k) = \sqrt{\frac{2}{\pi}} \frac{1}{k} e^{-\frac{k^2}{2}}. \tag{2.77}$$

In Table 2.4 the probability as a function of k is given. From the Table it can be seen that the minimum reference voltage step size in a parallel type of converter must be at least between 6 to 7 times the rms noise voltage of a comparator. In that case the probability of a decision error due to noise tripping of a quantization level is below 10^{-9} with $V_{refstep} = 6\ e_{noise}$. Here e_{noise} is the input referred noise voltage of a comparator plus additional noise of the resistive reference divider.

2.6.12 Bit Error Rate (BER)

In analog-to-digital converters many decisions during a conversion process are performed. Especially in high-speed parallel-type converters this phenomenon is found [12]. At the moment a wrong decision has been taken, the

k	2Q(k)
3	$2.9\ 10^{-3}$
4	$6.7\ 10^{-5}$
5	$5.9\ 10^{-7}$
6	$2.0\ 10^{-9}$
7	$2.6\ 10^{-12}$
8	$1.3\ 10^{-15}$

Table 2.4: Amplitude probability as a function of k rms value

internal code is converted into a wrong output code. Sometimes the internal code can be a meta stable condition of a comparator. A meta stable code of a comparator is an output code level that does not confirm the logical levels for "1" or "0." In such a case the conversion process from the internal code into the output code results in erroneous output codes. To obtain information about the error process the Bit Error Rate (BER) is defined. This figure defines the number of decision errors a converter makes. A high-quality analog-to-digital converter, for example, has BER numbers between 10^{-10} and 10^{-15}. In the design process of comparators this BER factor must be taken into account. In Chapter 11 an analysis of this phenomenon is presented.

2.6.13 Maximum sampling rate

The maximum sampling rate of a converter is a difficult to define number. In some cases the reduction in dynamic range (S/N ratio) can be used to define the maximum sampling rate. A definition can be:

The maximum sampling frequency of the converter for which the dynamic range measured over the Nyquist bandwidth is reduced with 3 dB or 0.5 bit.

This definition gives a rough indication about the maximum sampling frequency.

In systems which will use storage or digital signal processing it is better to relate the maximum sampling frequency with the bit error rate. In this case the definition of maximum sampling frequency can be related to the number

of errors per second (EPS). We obtain:

$$EPS = BER.f_{sample} \tag{2.78}$$

In Chapter 11 is shown that the BER is related to the sampling frequency as:

$$BER = e^{-\frac{C_b}{f_{sample}}} \tag{2.79}$$

with C_b is a constant determined by the system. Equation 2.78 changes into:

$$EPS = f_{sample}.e^{-\frac{C_b}{f_{sample}}}. \tag{2.80}$$

Solving equation 2.80 for f_{sample}, the maximum sampling frequency can be found from:

$$f_{sample\ max} = \frac{EPS}{BER}. \tag{2.81}$$

Assume that for one error per minute a BER of 10^{-10} is obtained as a solution from equation 2.80, then the maximum sampling rate of a converter equals: $f_{sample\ max} = 160$ MHz.

Using this definition a more accurate number for the maximum sampling rate is obtained.

2.6.14 Digital signal feed-through

Digital signals in most of the converters are TTL- or CMOS compatible. The disadvantage of the TTL levels in, for example, high-resolution D/A converters is the feed-through of the TTL logic levels into the analog output (current) signal. This feed-through reduces the dynamic range of the converter and introduces harmonic distortion. These distortion phenomena can be explained by supposing that at the output of the D/A converter a sine wave is generated. In a system with offset binary coding the MSB bit changes with the sign of the sine wave. Feed-through in this case adds to the fundamental frequency, which can result in amplitude changes. The MSB -1 bit, however, changes twice as fast as the output sine wave. Feed-through in this case adds signals to the output, which results in harmonic distortion. To avoid this problem a serial coding of the input signal must be used. This serial coding reduces the number of input pins with TTL levels. Furthermore, the frequency spectrum of the input digital signal is far above the signal bandwidth of the converter, and therefore this spectrum will be removed by the reconstruction low-pass output filter.

2.6.15 Distortion

In a sampled system the signal band of interest is not only present as a baseband signal but is also reproduced around multiples of the sampling frequency f_s, $2f_s$, $3f_s$, and so on. If such a signal is applied to a linear

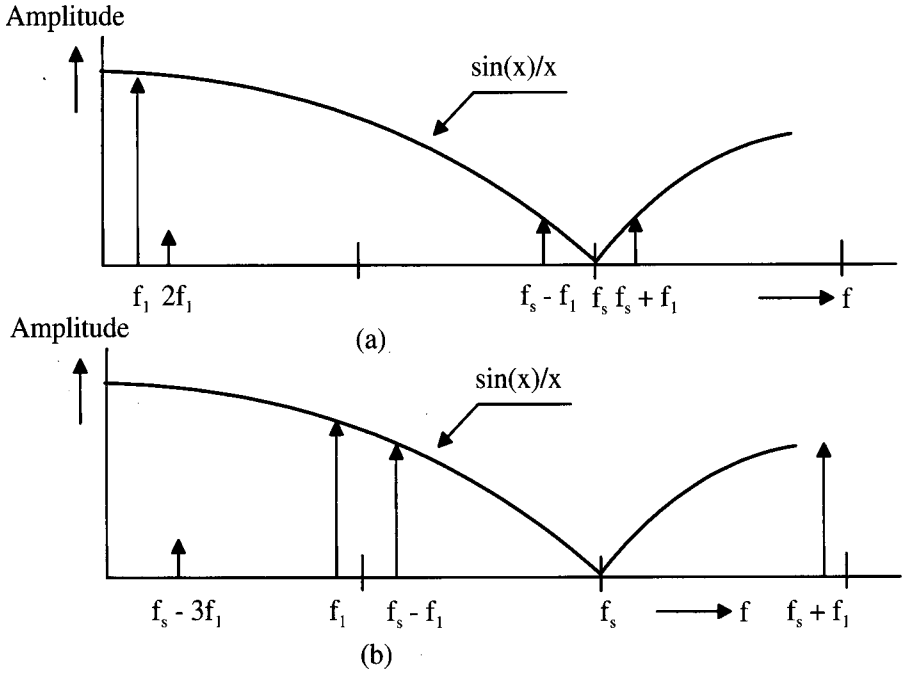


Figure 2.29: D/A converter distortion model

amplifier, then, due to the finite linearity of such a system, inter modulation products can be generated. Apart from the harmonic distortion components introduced by the finite linearity of a converter, two dominating inter modulation products for an input signal with a frequency f_{in} can easily be found by mixing the lower band frequency f_s - f_{in} with the upper band frequency f_s + f_{in}, resulting in a harmonic distortion $2f_{in}$. When the second harmonic $2(f_s$ - $f_{in})$ of the lower band mixes with the upper band f_s + f_{in}, a non-harmonic product | f_s - $3f_{in}$ | is obtained. As long as the frequency f_s - $3f_{in} \geq f_b$ only the harmonic distortion $2f_{in}$ is found. Here f_b is the system bandwidth. The minimum sampling frequency at which only harmonic distortion products are found can be calculated. With $f_{in} = f_b$ we obtain $f_s = 4f_b$. In a digital audio system with $f_b = 20$ kHz the lowest sampling frequency to obtain only harmonic products must be at least $f_s = 80$ kHz.

However, a lower sampling frequency (f_s = 44 kHz) is normally used, so harmonic and non-harmonic products must be encountered. In Figure 2.29 a graphic approach to the distortion problem in a D/A converter is shown. From Figure 2.29(b) it can be seen that signals close to half the sampling frequency have a large amplitude "mirrored" signal component (f_s - f_{in}). These signals require extreme linearity of the post-amplifier system to avoid mixing, resulting in non-harmonic distortion products appearing in the base-band. When, for example, the "hold" time of the converter is reduced, then the $\frac{\sin x}{x}$ amplitude distortion is reduced. At that moment the amplitude of the high-frequency signal components increases, the linearity requirements of the post amplifier system must be even more increased. Note that an identical result is obtained for a sample-and-hold amplifier.

2.6.16 Power supply rejection ratio

The power supply rejection ratio (PSRR) of a system as a function of frequency gives important data about the sensitivity of the system for noise induced on the power rails from, for example, the logic circuitry. Especially at high frequencies a good power supply rejection ratio is important to make the circuit immune from spikes introduced by fast logic circuits (CMOS logic).

2.6.17 Settling time

The settling time of a system is defined as the time needed from the start of a transition until the time the output reaches the new value within the specified accuracy. The settling time specification of the full step of a digital-to-analog converter is important for applications of such a converter in a successive approximation analog-to-digital converter configuration.

2.6.18 Acquisition time

The acquisition time of a system is the time difference between the moment a command is given and the moment the system responds to this command. At the moment the system responds to the input signal, the error between the input signal and the output signal of the system must be within a specified number usually given in the data sheet. This time is important in, for example, sample-and-hold amplifiers. In Figure 2.30 the definition of the acquisition time is shown applied to a sample-and-hold amplifier. The acquisition time is defined in this system as the time difference from giving the

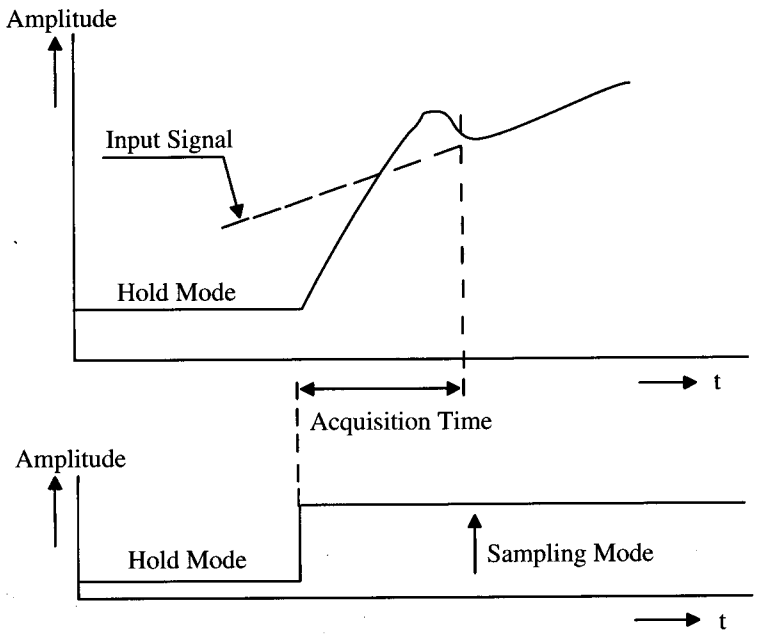


Figure 2.30: Definition of the acquisition time of a S/H amplifier

"track" command until the output signal tracks the input signal. The moment of "tracking" is the time for which the output signal "tracks" the input signal with a well-specified accuracy. The acquisition time is also a measure of the maximum applicable sampling frequency of a sample-and-hold amplifier. After the acquisition time is elapsed, the system (sample-and-hold amplifier, for example) can be switched into the hold mode.

2.6.19 Aperture time

The aperture time of a sample-and-hold amplifier is specified as the time difference between the "hold" command and the moment the real sample is taken. In a sample-and-hold amplifier and flash-type A/D converters this specification is very important. Differences in aperture time, usually called *aperture time uncertainty*, determine one of the major errors in sampled systems (see, for example, Chapter 1, "Time Jitter").
In sample-and-hold amplifiers the aperture time determines the minimum time required to elapse before the "start conversion" command can be given. Usually an extra time called *hold mode settling time* is needed to be able to specify the exact moment at which the hold output signal is within the spec-

ified accuracy. In a flash-type A/D converter the aperture time determines the difference between the sample command and the actual time the analog input signal is sampled and converted into a digital signal. In Figure 2.31 the definition of the aperture time is shown. A variation of the time differ-

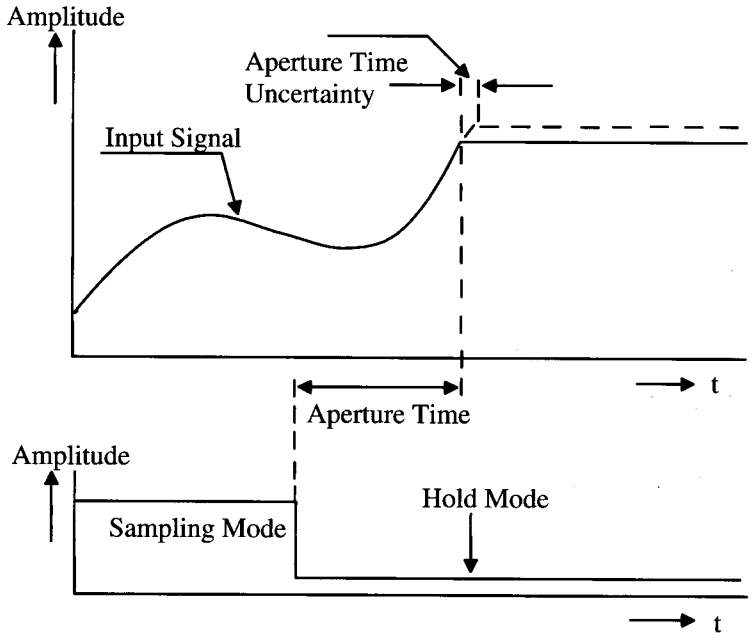


Figure 2.31: Definition of aperture time

ence between the "hold" command and the "start conversion" command in an A/D conversion system can result in fractional changes of the signal-to-noise ratio. Depending on the type of A/D converter, the start conversion command can be given before the final settling of the hold amplifier. As a result, a fractional change in maximum accuracy of the sample-and-hold amplifier is found. This accuracy variation gives rise to small changes in the maximum signal-to-noise ratio of a system. An optimum signal-to-noise ratio is mostly obtained when the time difference between the sample command and the start conversion command is more than the minimum time required according to the specification sheet. The hold mode settling time must be added.

2.6.20 Sample-to-hold step

The sample-to-hold step is a change of the analog output signal in a sample-and-hold amplifier at the moment the circuit changes state from the sample to the hold mode. Due to the charge feed-through in the switch an extra amount of charge which is not a measure of the analog input signal is added to the hold signal. This *hold* step introduces an error. In Figure 2.32 the sample-to-hold step of a sample-and-hold amplifier is shown. When the *hold* step is independent of the signal level, no nonlinear distortion is introduced and the hold step can be seen as an extra dc offset. Sometimes a control signal can be applied to the sample-and-hold amplifier to zero the hold step. Basically, designs can be made which minimize the sample-to-hold step and make this step independent of the input signal level. (See chapter 7 for a detailed description of sample-and-hold amplifiers.)

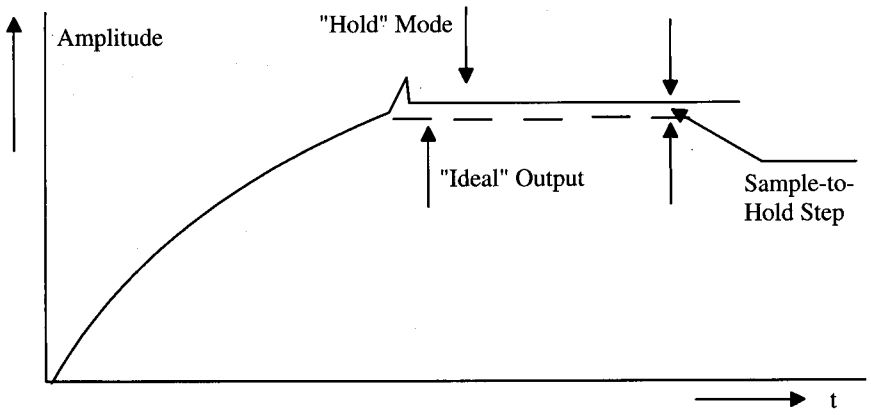


Figure 2.32: Sample-to-hold step

2.6.21 Droop rate

At the moment a sample-and-hold amplifier is in the hold mode, the output signal is stored on the hold capacitor. The voltage across the hold capacitor is sensed with an amplifier with a small input bias current. This input bias current, together with possible switch leakage currents, discharges the hold capacitor, resulting in a droop of the voltage across this capacitor. The rate with which the capacitor is discharged must be small. Then the total droop during the conversion time of a converter can be kept small, usually under 1 LSB. In this way variations in the conversion time do not change the

accuracy of the system. Mostly the droop rate is specified in mV/μsec. In some cases when the droop rate cannot be made small enough with respect to a 1 LSB value, then a fixed conversion time is used at which the final decision is taken. The droop can be measured and added to the output result of the analog-to-digital converter. In this way a reasonable accuracy of the total system is obtained. An estimation between the total leakage current $I_{leakage}$, the conversion time of an analog-to-digital converter $T_{conversion}$ and the droop rate of the system is found from:

$$V_{droop} = \frac{I_{leakage}}{C_{hold}} T_{conversion}. \tag{2.82}$$

When the droop rate is too high, a larger hold capacitor can be used to keep the droop rate within a 1 LSB specification.

2.6.22 Signal feed-through during hold mode

When the sample-and-hold amplifier is in the hold mode, then the input signal must be disconnected from the stored signal on the hold capacitor. In a practical system the sampling switch shows a finite impedance at the moment it is in the "off" mode. Especially at high signal frequencies the capacitive coupling over the sample switch results in a finite feed-through of the input signal onto the signal of the hold capacitor. The architecture of a sample-and-hold amplifier must be configured in such a way that a maximum attenuation between input signal and signal across the hold capacitor is obtained. The attenuation must be larger than the dynamic range of the analog-to-digital converter that is used for the conversion of the analog input signal into a digital output value. As an example, a feed-through attenuation between 70 to 80 dB is required for high-speed 8- to 10-bit analog-to-digital converter systems.

2.6.23 Noise in sample-and-hold amplifiers

In sample-and-hold amplifiers the noise introduced will be tracked as accurately as possible. As a result the output signal at the moment the system is switched from track into hold mode contains the momentary noise value present at the sampling moment. Usually it is not possible to introduce a noise filtering operation in such a system because at that moment the high frequency signal components are not accurately sampled. It is impossible to avoid the sampling of noise. Therefore, it is necessary to design circuits in such a way that the peak value of the noise generated over the applicable

signal bandwidth of the system is below an LSB value of the succeeding analog-to-digital converter.

2.6.24 Overview of sample-and-hold specifications

To obtain a quick overview about the various specifications of a sample-and-hold amplifier these different parameters are shown in Figure 2.33. The top of the figure shows the input signal as it is applied to the sample-and-hold system. The middle part shows the control signal as a function of time as it is applied to this system. In the bottom part of figure 2.33 the output signal as a function of time is shown. Note that during large signal transients the

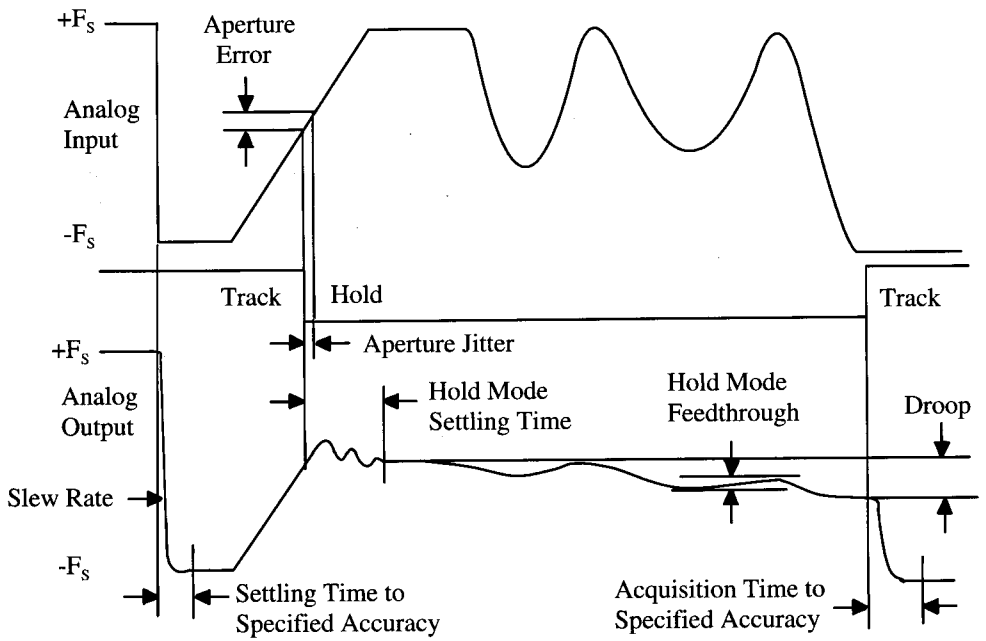


Figure 2.33: Overview of sample-and-hold parameters

analog output slews until it reaches the final value. Furthermore, during the hold mode the feed-through of the analog output signal is shown. The slow decrease of the output signal as a function of time shows the droop. The ringing shown in the figure when the system is switched from sample to hold mode increases the aperture time. In some designs the output voltage of the sample-and-hold can show an overshoot at the moment the slew operation in the amplifiers is finished and the signal level comes within the linear operation range. This overshoot can be caused by a limited overall system

stability introduced by a maximization of the bandwidth. Note furthermore that the input settling is a different specification than the aperture time. This settling time is responsible for signal transients during track mode. In the same way hold mode settling corresponds to the time needed for the system to settle within a specified accuracy during the final "off" switching into hold mode.

2.6.25 Analog system bandwidth

In high-speed A/D converter systems the analog bandwidth with a full-scale input signal must be defined. In ideal converter systems the maximum analog bandwidth is equal to half the sampling bandwidth. In practice, however, there are various reasons why this theoretical value is not obtained. In Chapter 3 a number of reasons will be given and explained. Therefore, it is necessary to give a good specification for the analog signal bandwidth of a converter.

A very precise specification of this analog bandwidth is found by specifying the maximum analog frequency for which the signal-to-noise ratio of the system decreases by 3 dB or $\frac{1}{2}$ LSB with respect to the theoretical value of the system defined over a bandwidth equal to half the sampling frequency [52].

By definition the bandwidth obtained in this way is called Effective Resolution Bandwidth (ERB).
The effective measured dynamic range can be converted into the Effective Number Of Bits (ENOB's) of the converter.

During the determination of the effective resolution bandwidth of a system a fixed sampling frequency is used. This sampling frequency is usually more than two times the analog effective bandwidth.
In Figure 2.34 the results of resolution bandwidth measurements are shown. The 3 dB decrease in signal-to-noise ratio of the system is used to define the (full-scale) analog signal bandwidth of the system. The effective resolution bandwidth must be measured at full scale to include time jitter, noise, and linear and nonlinear distortion products.

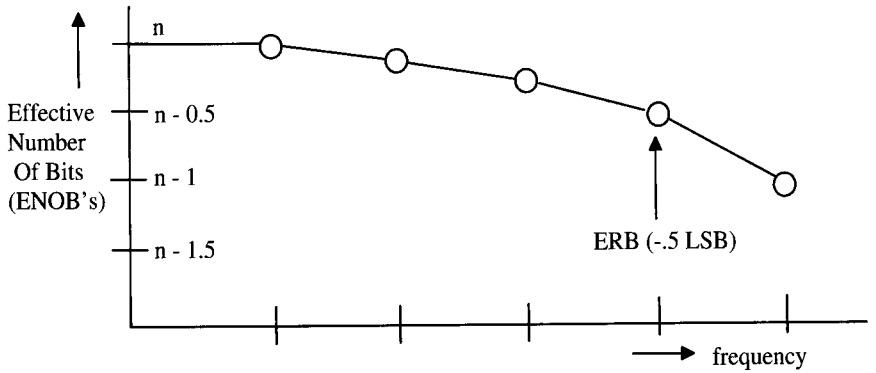


Figure 2.34: Effective resolution bandwidth of a converter

2.6.26 Differential gain and differential phase

In the beginning phase of digital video systems, the analog specification of differential gain and differential phase using a stepped well-defined series of color sub-carrier bursts between zero and full scale of a converter has been used to specify the linearity of the converter at high frequencies. A typical specification is: 1% gain variation and 0.5 degree phase variation at color sub-carrier frequency.

2.7 Figure of Merit

As a comparison between different architectures and performance of a converter the Figure Of Merit (FOM) has been defined. This index compares converters with respect to power consumption, ENOB's and maximum input signal frequency. The Figure of Merit is defined as:

$$FOM = \frac{Power}{2f_{in}2^{ENOB}} \tag{2.83}$$

In this equation $2f_{in}$ can be defined as the Nyquist frequency, however, in case the resolution is determined by the effective number of bits (ENOB) the input frequency can be different from the sampling frequency and in such a case will be smaller than the Nyquist frequency. An aggressive value for the FOM = 1 pJ. A resolution/input frequency plot for analog-to-digital converters can be drawn. (see Fig. 2.35). With improved technology and advanced converter architectures the FOM drops about a factor 10 in 10

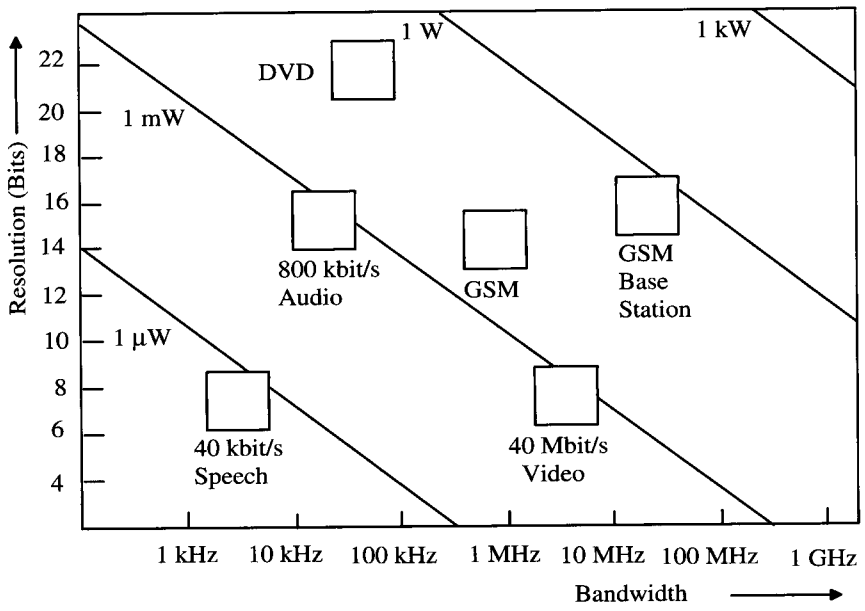


Figure 2.35: Resolution vs Input Frequency FOM plot

years. From the plot in Fig. 2.35 a power estimation is obtained for a certain converter resolution at a required maximum input frequency.

2.8 Conclusion

In this chapter the basic requirements for A/D and D/A converters are defined. These definitions lead to basic circuit design constraints which must be fulfilled to obtain high-performance converters. In a binary-weighted converter the $\pm \frac{1}{2}$ LSB linearity specification is the only necessary specification to guarantee *monotonicity*.
In high-resolution binary-weighted converters the linearity requirement implies a very high accuracy of the most significant bit weights to obtain a monotonic converter. Signal-to-noise and signal-to-(noise plus distortion) specifications give a quick and reliable qualification of a converter. It includes noise, glitch error, sampling time uncertainty, and distortion. These dynamic specifications are very important in digital-signal-processing systems such as, for example, digital audio and digital video systems.
The Effective Number of Bits (ENOB) specification allows a quick comparison between converters with identical resolution but different dynamic specifications. The Spurious Free Dynamic Range (SFDR) gives a quick overview of the largest distortion components of a converter while this specification gives furthermore some indications about intermodulation distortion in case the converter is applied in a digital receiver system.

Quantization spectra have been derived. These spectra give a good insight in the distortion introduced by quantization and how with a sampling operation these spectra are folded back into the base-band of the converter.

Relations between clock time jitter and the reduction in resolution of the converter are given in this chapter. Furthermore an analysis has been made about the accuracy with which elements are needed to match to obtain a linearity specification of $\frac{1}{2}$ LSB. Furthermore models have been derived that determine the reduction in resolution as a function of the linearity of a converter. Identical relations have been derived for the SFDR specification. The glitch energy is an important measure for the application of a D/A converter in an oversampled and noise-shaped system. Due to the increase in sampling frequency the number of *zero crossings* in an offset binary-coded converter increases, especially when a noise-shaping operation is included in the filter section. As a result, the distortion increases, and the gain and dynamic range is not in accordance with the theoretically expected values. A low glitch design is needed in this case. In Chapter 8 the noise-shaping techniques will be explained.
The Bit-Error-Rate specification is an important specification for high-frequency analog-to-digital converters. It determines the accuracy and repeatability of high-speed comparators. Apart from the Effective Resolution and the Effective Resolution Bandwidth of a converter, the BER specification determines the errors made by the converter during a longer period of time. Applications in oscilloscopes are requiring a low BER to allow error free measurements over a long period of time (1 hour, 1 day).

Chapter 3

High-speed A/D converters

3.1 Introduction

The best-known architecture for a high-speed analog-to-digital converter is the flash converter structure. In this structure an array of comparators compares the input voltage with a set of increasing reference voltages. The comparator outputs represent the input signal in a digital (thermometer) code which can be easily converted into a Gray or binary weighted output code. The flash architecture shows a good speed performance and can easily be implemented in an integrated circuit as a repetition of simple comparator blocks and a (ROM) decoder structure. However, this architecture requires 2^N-1 comparators to achieve an N-bit resolution. The parallel structure makes it difficult to obtain a high-resolution while maintaining at the same time a large bandwidth, a low power consumption, and a small die size.
Interpolation between reference levels reduces the number of reference taps and input amplifiers resulting in a lower power consumption. The influence of offset voltages in the input amplifiers can be reduced by using averaging between active amplifier stages. At the same time, signal-to-noise ratio is improved without using more power. An alternative to the full-flash architecture is the multi-step A/D conversion or sub ranging principle. In high-speed converters the two-step architecture is the most popular because of the ease of implementation. However, a two-step architecture must be preceded by a sample-and-hold amplifier which performs the sampling of the analog input signal. In the two-step architecture a coarse and fine quantization takes place. These succeeding conversion steps need time. The sample-and-hold operation on the signal keeps the sampled signal constant. During this "hold" time the conversion takes place, making it virtually "timeless." Af-

ter the coarse quantization is performed, the digital signal is applied to a D/A converter to reconstruct the analog signal. This reconstructed signal is subtracted from the analog input signal which is held by the sample-and-hold amplifier. After subtraction has taken place the residue signal can be amplified and is then applied to the fine quantizer which performs the conversion into a digital value. The coarse plus fine output code with, in many cases, an error correction operation results in the final digital output word. A good balance between circuit complexity, power consumption, and die size is obtained in this type of converter. The final dynamic performance, however, depends substantially on the quality and dynamic performance of the sample-and-hold amplifier.

In MOS technology circuits can be operated in a continuous-time mode or in a discrete-time mode. Most architectures in MOS use a discrete-time mode of operation. In such a solution the sample-and-hold operation is combined with the system function. Mostly the discrete-time operation includes an automatic offset cancelation technique in the comparator stages. In a full-flash system, 2^N-1 small sample-and-hold amplifier-comparators are therefore used to perform the conversion function. Because of the small value of the hold capacitor, offsets induced by switching transients and channel charges of the switching devices limit the resolution of the total system.

In MOS using a discrete-time circuit solution a two-step system implementation can be easily obtained by using a set of coarse sampled data comparator-amplifiers stages and a set of identical fine stages. The coarse conversion is performed by comparing the input signal with the coarse tap voltages on the input ladder. After the coarse value is determined, a block of fine reference voltages is switched on. These reference voltages are in-between the two already determined coarse ladder taps. Again a comparison is performed and the final output code is obtained. In this system the ladder is used for coarse and fine quantization without needing an extra D/A subtracter circuit to drive the fine converter stage.
Pipeline converter architectures are very popular in CMOS technology. This architecture consists of a cascade of simple modular converter blocks performing between 1 and 5 bit conversions each. Each block consists of an A/D converter, a D/A converter for the reconstruction of the analog signal, a subtracter to determine the signal residue after the quantization and a gain stage. A sample-and-hold function is part of the converter block. Analog data is delayed by the sample-and-hold amplifier stage during the conversion resulting in an output code latency equal to the number of cascaded stages.

A high resolution at a high sampling frequency is possible using the pipeline architecture. Sharing of amplifiers in a pipeline converter is possible. This reduces power consumption and reduces die size.

To overcome some problems of the sample-and-hold amplifier, design alternatives have been worked out that have the advantage of the digital sampling used in the full-flash converter and the die size of the two-step system but do not require a sample-and-hold amplifier. This architecture is called a *folding architecture*, which is capable of achieving a large analog bandwidth and high resolution without incurring the power and area penalties associated with the flash architectures (see references [49, 50, 51, 52, 5]).

By using folding techniques, an A/D converter can be designed in which each comparator detects the zero crossings of the input signal through a number of quantization levels, thus reducing the number of comparators required for a given resolution. The number of comparators is reduced by the number of times that the input signal is folded by the folding stages. However, each reference level requires a folding stage generating the folding signal. This folding signal is a combination of output signals from folding stages. By combining a number of output signals from folding stages, a repetitive folded signal is applied to the decision-making comparators. The folding factor, which determines the number of signals to be combined reduces at the same time the number of comparators. This reduction in comparators, however, is offset by the number of folding stages that are needed to obtain the resolution of the converter. The number of folding stages can be further reduced by interpolating between outputs of folding stages to generate additional folding signals without the need for more folding stages. The interpolation stage in this way reduces the number of folding stages by the interpolation factor. The folding architecture results in a compact, low-power system with small signal and clock delays over the interconnection lines. Therefore, a larger analog input bandwidth can be obtained than would be possible with a standard flash converter. However, the folding operation increases the internal signal frequencies with the folding factor.

Different system implementations will be described using CMOS technologies.

Up until now no accurate model has existed that describes the frequency limitations of flash-type converter structures. A high-level model has been developed that describes the nonlinear behavior of amplifier stages. This

behavior results in a signal-dependent delay giving third-order distortion. Keeping in mind the clock timing accuracies needed in accordance with the converter speed, the third-order distortion term is thought to impose a basic speed limitation on flash converters. This model is used to optimize the analog bandwidth of the converter with respect to the technology used.

Time interleaving of converters increases the sampling rate into the multi-Gigahertz range. Applications of these architectures are mostly in digital oscilloscopes.

3.2 Design problems in high-speed converters

There are two main problems that impair the dynamic performance of high-speed A/D converters: *timing* and *distortion*. [43, 5].

3.2.1 Timing errors

In most A/D converters there are four main sources of timing errors:

1. Sampling clock jitter.
2. Limited rise and/or fall time of the sampling clock.
3. Skew of the clock and input signal at different places on the chip.
4. Signal-dependent delay.

The sampling clock jitter can originate both inside and outside the A/D converter. The outside sampling clock must be designed to have a very small (short-term) jitter. Internally, a small rise or fall time of the sampling clock avoids additional jitter caused by (white) noise of the clock amplifier circuits. Furthermore, crosstalk from other circuits must be minimized to avoid modulation of the sampling clock. The skew between the clock and the analog signal introduces timing errors between the same signal at different places on the die. The clock signal at the top comparator stage, for example, may be slightly out of phase with the clock signal at the middle comparator. This difference in time causes a quantization error that results in nonlinear distortion. As an example, in about 12 ps a signal can travel only 3.6 mm over an interconnection line at the speed of light. On a die the transmission speed is lower because of the high dielectric constant of the oxide layers and the finite conduction of the epitaxial layer or the substrate material. In practice a speed between half and one-third of the speed

of light is obtained on the die. This means that 1 ps equals a distance of 100 μm to 200 μm between elements in an integrated circuit. Therefore, the sampling clock lines and the signal lines in the converter must be laid out very carefully. If the paths of clock and signal lines include different processing circuits, the delays of these processing elements have to match within a fraction of the required timing accuracy. It implies, furthermore, that a small total die size is best for minimum timing performance errors.

Finally, many circuits introduce a signal-dependent delay. For example, each amplitude-limiting circuit followed by a bandwidth-limiting circuit introduces a delay that is slope-dependent. These circuits are invariably found in input and comparator stages of high-speed A/D converters. A behavior model is developed that can be used for optimization of the analog bandwidth of A/D converters. A relation between the maximum analog input frequency and the small signal bandwidth of the input amplifier-comparator stage is determined with this model. The signal-dependent delay of a signal exhibits itself as a third-order distortion of the quantized signal.

3.2.2 Distortion

The distortion of a quantized signal can be caused by five main reasons:

1. Sampling comparators aperture time.
2. Distortion in the input buffer or input signal amplifier.
3. Offset in input amplifiers and comparators.
4. Changes in the reference voltage values.
5. Delays of analog signal and clock signal.

A large comparator aperture time may be caused by the architecture of the comparator or by a large rise or fall time of the sampling clock. Such a large aperture time results in high-frequency sampling errors and causes an averaging effect in the time domain. This phenomenon exhibits itself as a third-order distortion. An enhanced small signal bandwidth of the comparator stages reduces this effect.

Non-linear distortion in the input buffer amplifier introduces harmonics and mixing products of the input signal. These harmonics may give aliasing

products in the baseband due to mixing of these components with the sample frequency.

Matching in CMOS technology is limited resulting in substantial influence of amplifier offset voltages on the linearity of a converter. Comparator offset voltages must be small with respect to the reference voltage steps to obtain a nonlinearity which is only dependent on the accuracy of the resistive divider. Scaling of input devices results in a reduction of the offset voltage at the cost of die size and (non-linear) input capacitance of the converter. Input buffer amplifiers are difficult to design and require a lot of power.

Most high-speed A/D converters require a large number of reference voltages that are normally generated by a resistive divider and a reference source. Errors in these reference voltages introduce a nonlinear distortion equivalent to a nonlinear distortion in the input amplifier. An additional problem, especially in converters with a large bandwidth, is the kickback from the comparator stages (clock feed-through) on the reference voltages. During sampling of the input signal, the reference voltage temporarily deviates from the nominal value, resulting in additional quantization errors. Timing and distortion problems are common to all high-speed A/D converter architectures.

3.3 Internal converter coding schemes

In converters different internal coding schemes are used before the final (binary weighted) code is generated at the output of the system. These different coding schemes will be described here.

3.3.1 Thermometer code

In full-flash systems an internal code called *thermometer code* is mostly used. Every time a reference level has been tripped by the input signal an output "1" is added to the output code of the comparators. In Table 3.1 the output binary code and the (internal) thermometer code are shown for a value up to 8. From the table it is easy to see why this code is called *thermometer code*. With an increasing binary number the number of "1"s is increasing. By using a simple gate function or a ROM the binary output code can be obtained in an easy manner. Looking at the table, for the binary code 0010, for example, we only need to encode in an *and* gate the values of $b.\bar{c}$. When the output value is true, then a true is applied to the

BINARY CODE d c b a	THERMOMETER CODE h g f e d c b a
0 0 0 0	0 0 0 0 0 0 0 0
0 0 0 1	0 0 0 0 0 0 0 1
0 0 1 0	0 0 0 0 0 0 1 1
0 0 1 1	0 0 0 0 0 1 1 1
0 1 0 0	0 0 0 0 1 1 1 1
0 1 0 1	0 0 0 1 1 1 1 1
0 1 1 0	0 0 1 1 1 1 1 1
0 1 1 1	0 1 1 1 1 1 1 1
1 0 0 0	1 1 1 1 1 1 1 1

Table 3.1: Binary-thermometer code implementation

ROM function and the binary output code 0010 is obtained. This operation is performed for every binary output signal using other combinations of the thermometer code.

3.3.2 Gray encoder

At the moment a special analog encoding is used at the input of the comparators then the *Gray* shows to be an efficient code for implementation. In Table 3.2 the binary-Gray code implementation is shown. The specific characteristic of the Gray code is that from one code to the next code *only one bit* changes. This is shown in Table 3.2. As a result, the value for a in the Gray code is obtained by combining the levels 1, 3, 5, 7, 9, 11, 13, and 15. For b in the Gray code a combination of levels 2, 6, 10, and 14 is used. In the same way for c a Gray code combination of levels 4 and 12 is used.

When in a system a Gray code is generated, then a binary output code is obtained by using an exclusive OR function between a and b. The output of the exclusive OR function is put in an AND function with the $\bar{c}$ of the Gray code to obtain the binary a output code. An identical operation is needed for binary b using Gray b, c, and d. Binary c is obtained from d Gray code directly.

A circuit implementation of a Gray code analog-to-digital converter will be shown in one of the following sections.

INPUT LEVELS	BINARY CODE d c b a	GRAY CODE d c b a
0	0 0 0 0	0 0 0 0
1	0 0 0 1	0 0 0 1
2	0 0 1 0	0 0 1 1
3	0 0 1 1	0 0 1 0
4	0 1 0 0	0 1 1 0
5	0 1 0 1	0 1 1 1
6	0 1 1 0	0 1 0 1
7	0 1 1 1	0 1 0 0
8	1 0 0 0	1 1 0 0
9	1 0 0 1	1 1 0 1
10	1 0 1 0	1 1 1 1
11	1 0 1 1	1 1 1 0
12	1 1 0 0	1 0 1 0
13	1 1 0 1	1 0 1 1
14	1 1 1 0	1 0 0 1
15	1 1 1 1	1 0 0 0

Table 3.2: Binary-Gray code implementation

3.3.3 Circular code

At the moment signals are repeating in a converter implementation, then a circular code is mostly generated. In table 3.3 the binary code and a corresponding circular code are shown. The Table shows that with an increasing binary number in the circular code the number of "1"s is increasing until the row is completely filled with "1"s at code 1111. Then the "1"s are moving out until finally the code 1000 appears at the end of the scale. When the code is increased with one step, the starting code 0000 appears again. Because of this phenomenon this code is called circular code. The conversion of the circular code into a binary one is performed by using an exclusive OR function ($a.\bar{b} + \bar{a}.b$) and a ROM encoder. The output of the exclusive OR results in a true state at two code transitions. The MSB determined by c in the binary code is equal to d in the circular code. The remaining three bit codes are determined by a, b and c. The result of this operation is that with only four comparators a three bit binary output code can be determined.

In one of the following sections attention will be paid to circuit implementations for circular codes. Such a code appears in "folding" analog-to-digital converters, too.

BINARY CODE c b a	CIRCULAR CODE d c b a
0 0 0	0 0 0 0
0 0 1	0 0 0 1
0 1 0	0 0 1 1
0 1 1	0 1 1 1
1 0 0	1 1 1 1
1 0 1	1 1 1 0
1 1 0	1 1 0 0
1 1 1	1 0 0 0

Table 3.3: Binary-circular code implementation

3.4 Full-flash converters

In an N-bit flash A/D converter, $2^N - 1$ reference voltages and comparator stages are used to convert the analog input signal into a thermometer-like digital output code (see Figure 3.1). This code is converted into a binary output code using a ROM structure. In today's technologies, 8-bit converters having a reasonable die size and consuming moderate power are available. Increasing the resolution to 10 bits increases the die size and power dissipation roughly four times. In practice, however, there is a limit to the power dissipation that can be handled in IC packages. Therefore, the power per comparator stage must be drastically reduced to keep the overall power dissipation at the same level as the 8-bit unit. As a result, the bandwidth of the comparators has to be reduced, resulting in a much lower effective analog bandwidth for the converter. The bandwidth of a system is mostly related to biasing current, which in turn results in power dissipation. Because of the increase in size, it is more difficult to distribute clock and input signal lines without introducing delay-induced errors exceeding $\pm \frac{1}{2}$ LSB, and to match the properties of all these comparators within the same specification. The input capacitance of the system increases linearly with the number of comparators, making it impractical to incorporate an input signal buffer on the chip. Even external buffers are difficult to design and need a large power-driving capability at high frequencies. The large number of compara-

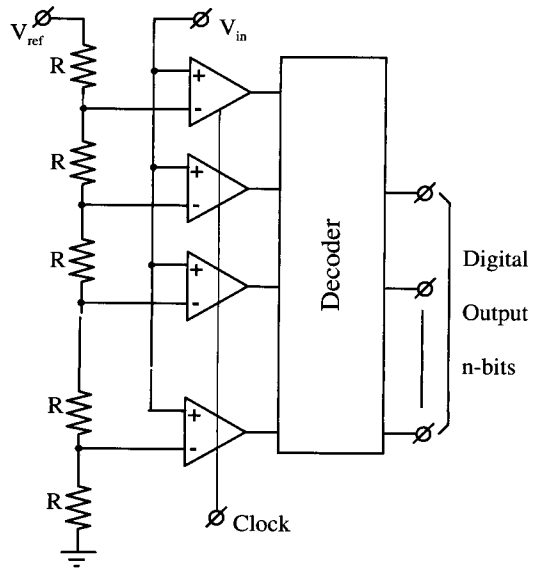


Figure 3.1: Full-flash A/D converter structure

tors results in a heavy loading of the clock driving circuits. Small rise and fall times of the clock signals are difficult to obtain and therefore external clock drivers are often required.

3.4.1 Comparator input amplifier

The continues time comparator input amplifier circuit diagram is shown in Figure 3.2. The circuit consists of a differential amplifier M_1, M_2 which compares the analog input signal with the reference voltage generated across a tapped resistor. The input signal is amplified and appears across the drain resistors R. Because of finite matching properties of MOS devices it is important to know the offset voltage of the input amplifier. This offset voltage is defined as the difference in gate voltage required to give a zero differential output voltage as shown in Figure 3.2. As will be shown in a separate chapter offset voltage of CMOS transistors depends on the technology used. Furthermore the designer has the ability to change the size of devices M_1 and M_2 to tailor the offset voltage. In practice this can be done only over a limited range. Having a reference voltage of 1 V and needing an 8-bit resolution, the reference step size becomes $\frac{1}{2^N} \approx 4$ mV. Suppose we use a 0.5 μm technology, then the *unit* offset voltage (a_{vth}) is about 10 mV. To

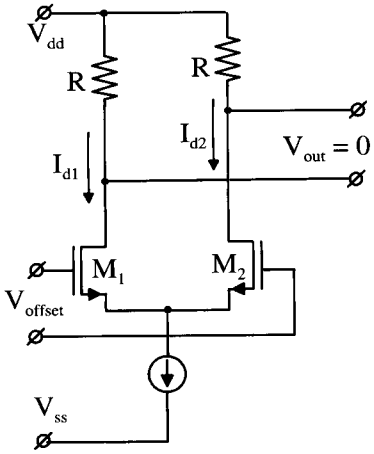


Figure 3.2: Comparator Input Amplifier

get a 1 σ offset of 1 mV we have to increase the device size according to:

$$V_{offset} = \frac{a_{vth}}{\sqrt{WL}}. \tag{3.1}$$

Using equation 3.1 we obtain for WL = 100. This means with W = 100 μm and L = 1 μm this requirement is fulfilled. Such a big size device has a large input capacitance. With C_{unit} = 2 fF ($1\mu^2$) we obtain per differential pair an input capacitance of:

$$C_{inputpair} = \frac{1}{2}WL.2fF = 100fF. \tag{3.2}$$

In an 8-bit full flash converter we have about $2^N = 256$ comparator input amplifiers so the total input capacitance of the 8-bit converter becomes:

$$256.100fF \approx 26pf. \tag{3.3}$$

This input capacitance is non-linear because always a limited number of input pairs are only active and contributing to the decision signals. To drive such a large input capacitance a buffer amplifier is needed. Such a buffer amplifier is difficult to design and consumes a lot of power. It is therefore important to reduce the number of input amplifier pairs and at the same time to reduce the offset voltage. Two useful techniques will be described now.

3.5 Interpolation

The output signals from the input amplifiers have with time a finite slope. Furthermore the difference between the signals is limited. As a result it is possible to accurately interpolate between two reference levels and get an accurate zero crossing of the differential output signal. The number of input amplifiers can be reduced depending on the number of times an interpolation takes place. In Fig. 3.3 an accurate interpolation using equal interpolation resistors R is shown. As can be seen from this figure, the signal $V_{outnInt}$ is interpolated between V_{outn} and V_{outn+1}. An extra zero crossing is obtained in this way without needing an input amplifier. To avoid interaction between

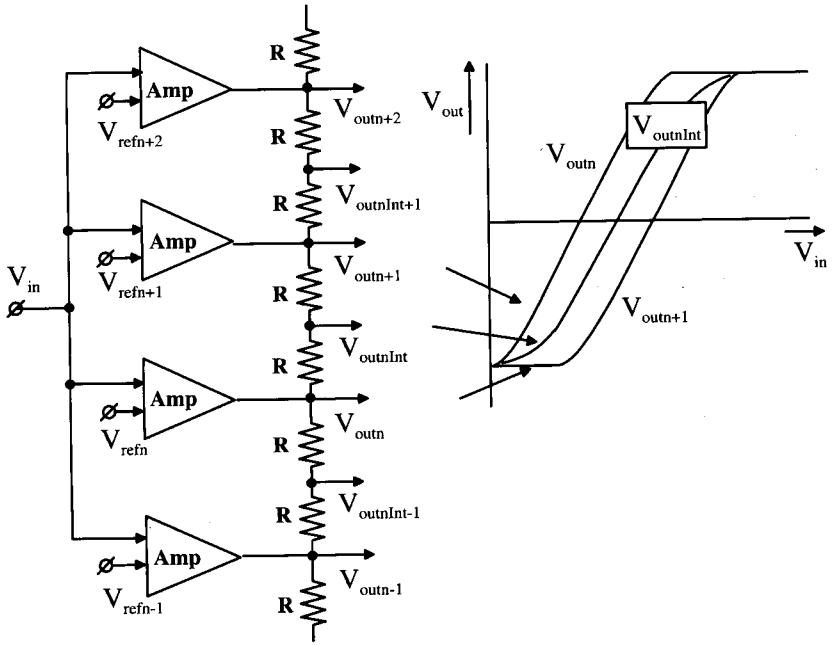


Figure 3.3: Resistive Interpolation

the amplifier stages an output buffer is added to the amplifiers called Amp. This amplifier is shown in Figure 3.4. In case the output impedance of the amplifiers is small compared to the interpolation resistor R, then no interaction between the stages occurs. Increasing the output impedance of the amplifier results in interaction between the interpolating stages. This interaction results, as will be discussed in one of the following sections, in *averaging* of zero crossing signals.

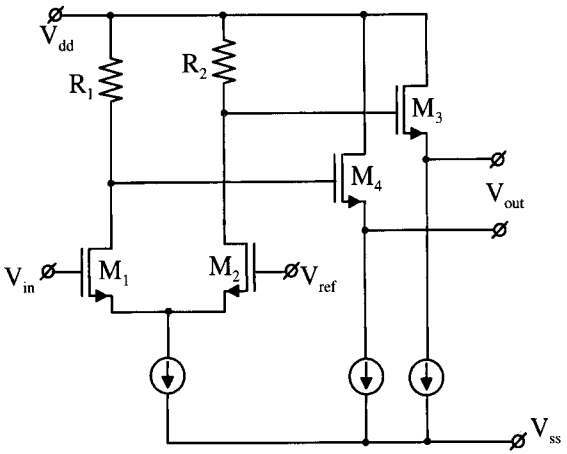


Figure 3.4: Input Amplifier with Buffer

3.5.1 DNL Improvement by interpolation

Interpolation has a positive effect on the differential non-linearity (DNL) of a converter. In Figure 3.5 the interpolation of 3 signals and the effect on DNL is shown. In the figure, the ladder reference levels are shown and so

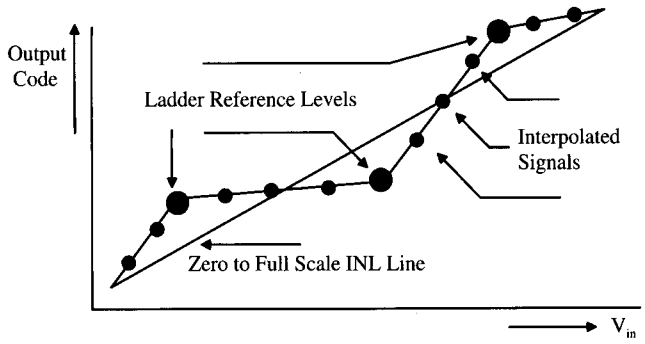


Figure 3.5: DNL Improvement by Interpolation

are the three interpolated signals. Using matched resistors, the interpolated signals are on a straight line between the ladder reference levels. The good matching of resistors results in a high-accuracy of the interpolated signals. This means that the step size of the interpolated signals is very accurate resulting in a small DNL error. In this simple explanation it is supposed that the offsets of succeeding amplifiers have no influence on the interpo-

lated signals. In practice some influence will be found.

3.5.2 Multiple interpolation

The number of interpolated signals can be rather easily increased as shown in Figure 3.6. The circuit diagram shows a method to obtain seven interpolated signals in between of two reference levels. In this case the values of the interpolation resistors must be chosen in such a way, that the output impedance for the in the middle generated signal with the capacitive loading of the succeeding stage does not introduce an extra delay. This results usually in a low value for the interpolation resistor R_{intpol}. As a result more power is needed to drive the interpolation resistor chain. An optimum has to be obtained between the number of times interpolation is used, the number of cascaded amplifier stages in the converter and the extra power needed for driving the interpolation stage. Mostly an interpolation between 1 and 3 is used and a cascade of such stages increases the amount of zero crossings obtained in this manner.

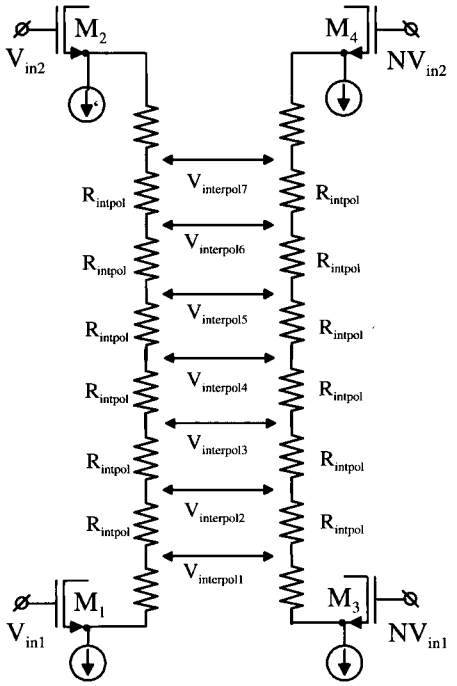


Figure 3.6: Multiple Interpolation Scheme

3.5.3 Multiple interpolation error

Although resistor matching is very good, interpolation causes some nonlinearity. This error needs to be calculated. Starting with the amplifier

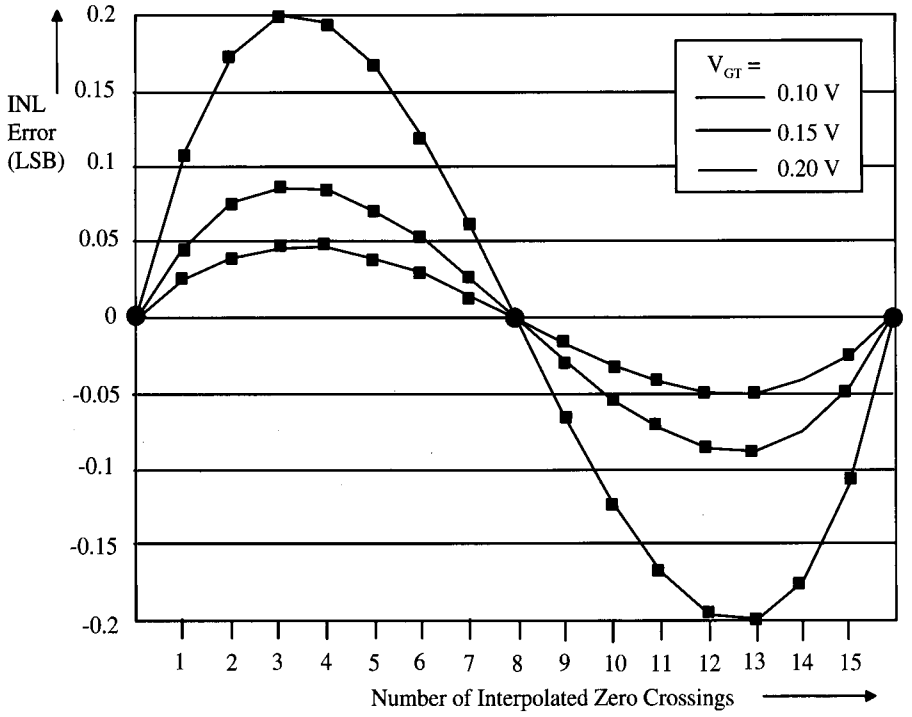


Figure 3.7: Interpolation error

stage shown in Fig. 3.2, the output voltage of this stage can be represented by:

$$V_{out} = \frac{A}{2V_{GT}}(V_{in} - V_{ref})\sqrt{4V_{GT}^2 - (V_{in} - V_{ref})^2}. \tag{3.4}$$

The gain A is expressed as:

$$A = g_m R, \tag{3.5}$$

with g_m as the transconductance of transistors M_1 and M_2 and

$$V_{GT} = V_{GS} - V_T = \frac{I_s}{g_m}. \tag{3.6}$$

I_s is the tail current of the differential pair. Now we will consider two adjacent reference levels eg. $V_{ref1} = 0$ and $V_{ref2} = V_{range}/16$. In this system

16 input levels are used and via interpolation a final resolution of 8-bits is obtained. The difference between an ideally interpolated signal and the resistive interpolation will be analyzed. It can be derived that the integral non-linearity error (INL error) due to the resistive linear interpolation yields:

$$\delta_{INL} = V_{in}\left(1 - \frac{16V_{in}}{V_{range}}\right)\left(\sqrt{1-\left(\frac{V_{in}}{2V_{GT}}\right)^2} - \sqrt{1-\left(\frac{V_{in}-\frac{V_{range}}{16}}{2V_{GT}}\right)^2}\right). \tag{3.7}$$

With linear interpolation, the zero crossings between two interpolated reference levels are located at:

$$V_{in} = i\frac{V_{range}}{2_N}, \quad \text{with} \quad \text{i} = 1, 2, ...\text{N}_{\text{interpol}} \tag{3.8}$$

In Fig. 3.7 the error has been plotted for $N = 8$ bit and $N_{interpol} = 15$. From Fig. 3.7 it can be seen that for an interpolation error smaller than 0.1 LSB V_{GT} of about 0.2 V is needed. Furthermore this figure shows that with a one times interpolation (middle of the figure) no error is introduced. This means that in cascaded amplifier stages a one times interpolation is preferred.

3.5.4 Active interpolation

An alternative to resistive interpolation is active interpolation. In this system amplifier transistors are split up into two equal devices as shown in Fig. 3.8. As shown in the figure, all transistors have equal size. In this picture a size of 0.5 is given related to the already used input amplifier pairs. At the gates of transistors M_1 and M_2 the output signal from amplifier A is applied, while at the gates of transistors M_3 and M_4 the output signal of amplifier B is introduced. These signals show a delay in time as can be seen from figure 3.8. The drain currents of M_1 and M_3 are added as has been done for M_2 and M_4 too and these combined drain currents flow through the load resistors R_1 and R_2. The output signal of this stage interpolates now between the output signal of amplifier A and the output signal of amplifier B. As long as offset voltages and mismatches are small compared to the required interpolation accuracy, this interpolation method does not show any interaction between the stages and performs well even at high signal frequencies.

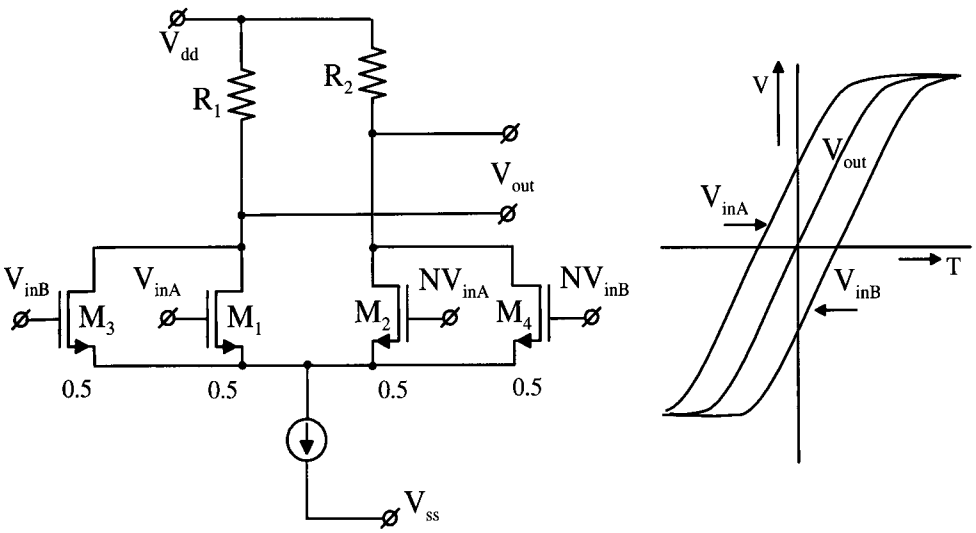


Figure 3.8: Active Interpolation Scheme

3.5.5 Capacitive interpolation

In time discrete systems sampled data is used. In such a system it is possible to use a capacitive interpolation to minimize the amount of ladder reference tabs. An example of capacitive interpolation is shown in Fig. 3.9. The operation of the circuit considers two phases of the clock signal:

- Reset Phase: Switches R are closed
- Compare Phase: Switches C are closed

During the reset phase switches R are closed and the reference levels V_{refn} and V_{refn+1} are charged on capacitors C and 2C respectively. It must be noted, that common mode levels of the differential amplifiers are set to a fixed value. This can be obtained by using a differential pair with a resistive load and connecting the reset switches between the drain and gate terminals of the transistors. After charging the capacitors C during the reset phase, the reference voltage of the interpolation amplifier is exactly in between of the reference levels V_{refn} and V_{refn+1}. Capacitors show a good matching so an accurate interpolation takes place. After the reset phase, switches R are opened and the compare phase starts by closing switches C. During this phase the input signal is applied to the differential amplifiers and amplified. This amplified signal can be applied to the comparators to determine the digital value of the input signal. As can be seen from Fig. 3.9 offset voltages

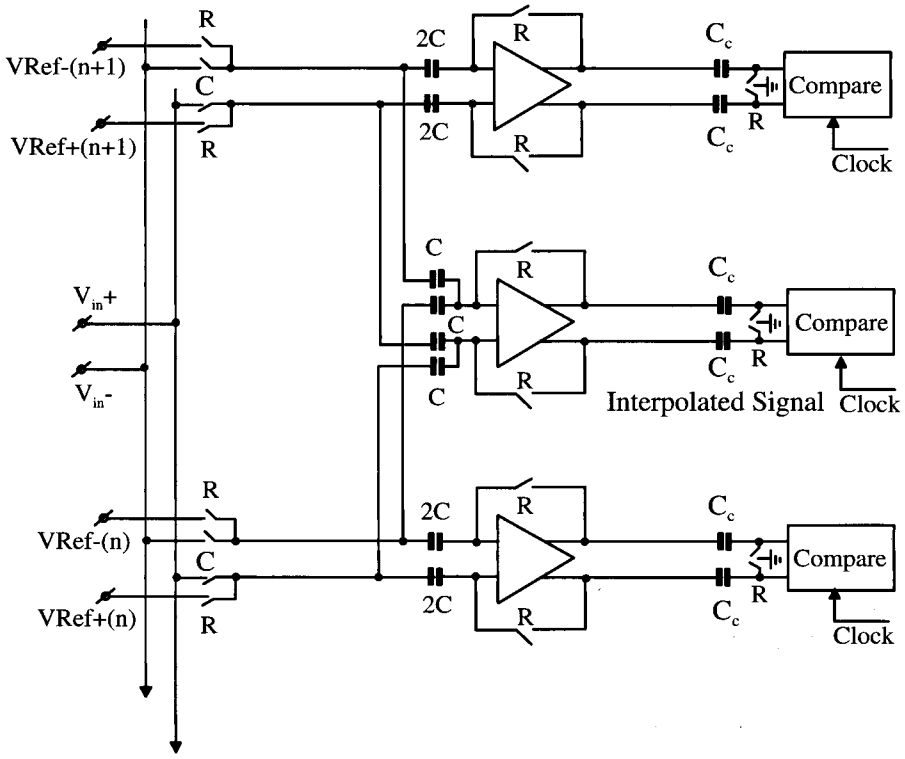


Figure 3.9: Capacitive Interpolation Scheme

of the amplifiers are stored on capacitors C_c. The amplified signals are then applied to the comparators to obtain the digital values. A substantial reduction of the offset voltages is obtained using this amplifier scheme.

3.6 Averaging

In continuous time systems offsets of amplifiers are the main limitation to increase the converter resolution above 6 bits. However, it has been shown already that sizing the input devices results in a reduction of offset voltage. This transistor sizing, however, is limited and introduces disadvantages like large input capacitance, large die size and high power dissipation. To partially overcome this problem an *Averaging* scheme will be introduced. This averaging scheme uses the outputs of more active input pairs to increase the effective gate area and in this way reduce the offset voltages. In Fig. 3.10 a system using resistive averaging is shown. The figure shows three

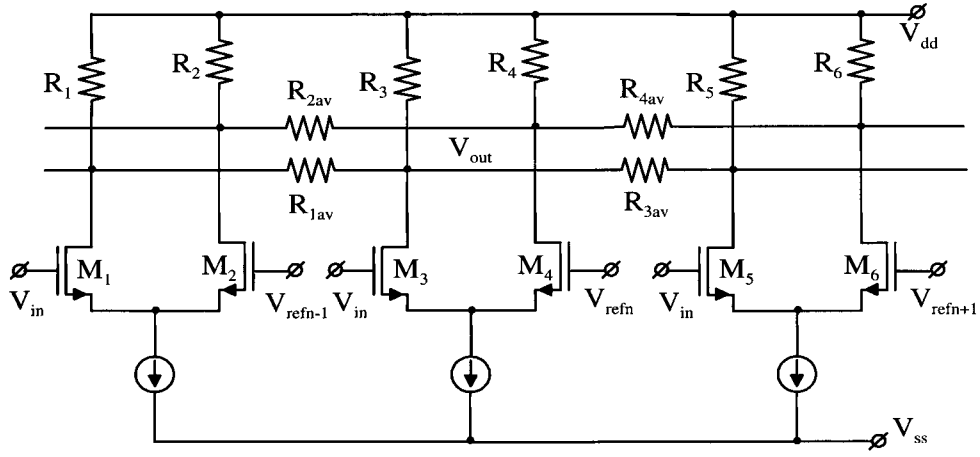


Figure 3.10: Resistive averaging Scheme [129]

differential amplifiers with load resistors R_1, R_2, . . R_6 as part of the input amplifier chain used in a flash analog-to-digital converter. Averaging is obtained by coupling the outputs of the differential amplifiers via averaging resistors R_{1av}, R_{2av}, R_{3av}, R_{4av}. This average resistor chain continues to couple more input stages. As long as the input amplifiers are active and operate in the linear signal range, then the output signals of these active amplifiers contribute via the averaging resistors to the signal of a differential amplifier operating around the "zero crossing" level. Here amplifier M_3, M_4 is supposed to be the zero crossing amplifier. The output signals from the "left" neighbors of the zero crossing amplifier influence the zero crossing. The same effect is obtained from the "right" neighbors. As long as the neighboring amplifiers are in the linear region it looks like that the zero crossing amplifier consists of a much bigger device with a size equal to the sum of the areas of the active linear amplifiers. As a result a very rough estimate of the reduction in offset voltage compared to a non-coupled single differential amplifier equal to $\sqrt{N_{active}}$ is obtained. Here N_{active} are the number of linear active amplifier stages contributing to the output signal of the zero crossing stage. Furthermore the signal amplitude increases with a value equal to about N_{active} while the noise increases with $\sqrt{N_{active}}$. As a result of this operation the signal-to-noise ratio (S/N) improves with $\sqrt{N_{active}}$, while the offset voltage reduces with the same amount. The described effect of offset averaging is shown in Fig. 3.11. The dots in the figure show the offset voltage in case NO averaging is used. At the moment the averaging resistors are included, then the reference levels move to the

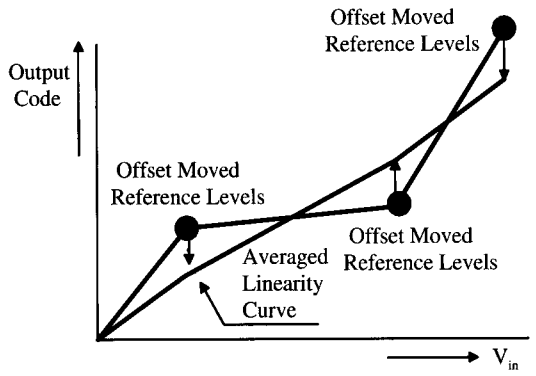


Figure 3.11: Effect of averaging on INL

averaged level. In the figure it is shown that the result of this operation is an improved integral non-linearity (INL).

3.6.1 Averaging non-linearity error

Although the averaging over amplifier stages shows a positive effect for offset voltage and dynamic range, at the edges of the system a non-linearity is found. This error is caused by the not equal amount of averaging amplifiers that contribute to the zero crossing of the "end point" amplifiers. In Fig. 3.12 an amplifier chain with averaging resistors is shown. From this figure it can be seen that the middle amplifier has the same amount of averaging stages at the left and right side. The top and bottom amplifiers show a large difference in averaging amplifiers. The amplifier connected to V_{rn-3} has at the right side the whole chain of linear stages to average the output signal while at the left side no amplifier to average the output signal is present. The same occurs for the amplifier connected to V_{rn+3}, but then at the right side no averaging amplifiers are present. As a result of this inequality a non-linearity of the converter transfer function is obtained. This is shown in the lower figure. In practice a usable input range of about 70% of the reference voltage range can be used. To overcome the linearity problem, the number of amplifiers can be increased and more stages are added at the top and the bottom part of the signal range. This causes an inefficiency of the system.

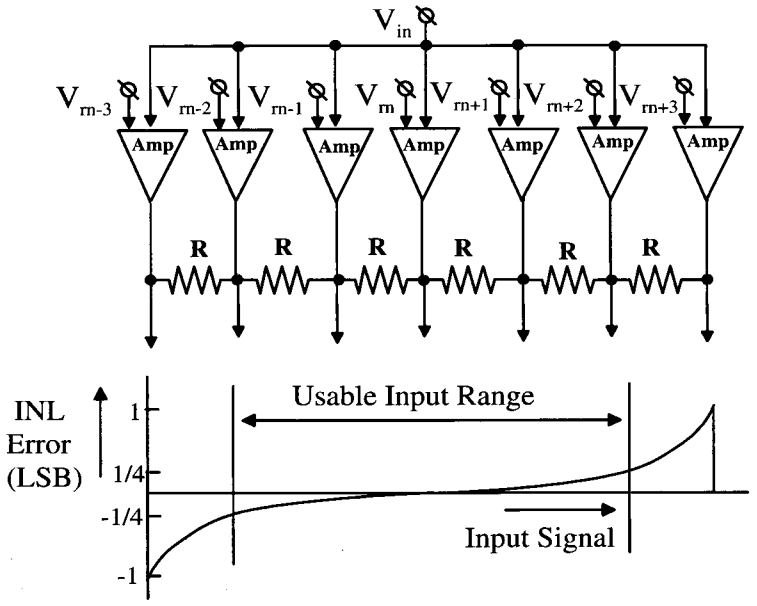


Figure 3.12: Effect of averaging on INL

3.6.2 Averaging non-linearity compensation

To overcome the problem with input non-linearity a compensation method can be used. This method uses only one extra amplifier at the top of the reference source and one at the bottom of the reference source. In Fig. 3.13 this compensation scheme is shown. The extra amplifiers at the top and the bottom of the reference ladder have a different averaging resistor. This resistor is called R_{comp}. A proper adjustment of this resistor is possible. Depending on the design of the input amplifier the value for R_{comp} can be determined. The usable input range increases from 70% to 95%.
In [113] the value for the compensation resistors has been derived using input pairs with a resistive load R_L and averaging resistor R. The compensation resistor becomes:

$$R_{comp} = R - R_L \tag{3.9}$$

From this equation it can be seen that no compensation is possible in case the averaging resistor $R \leq R_L$.

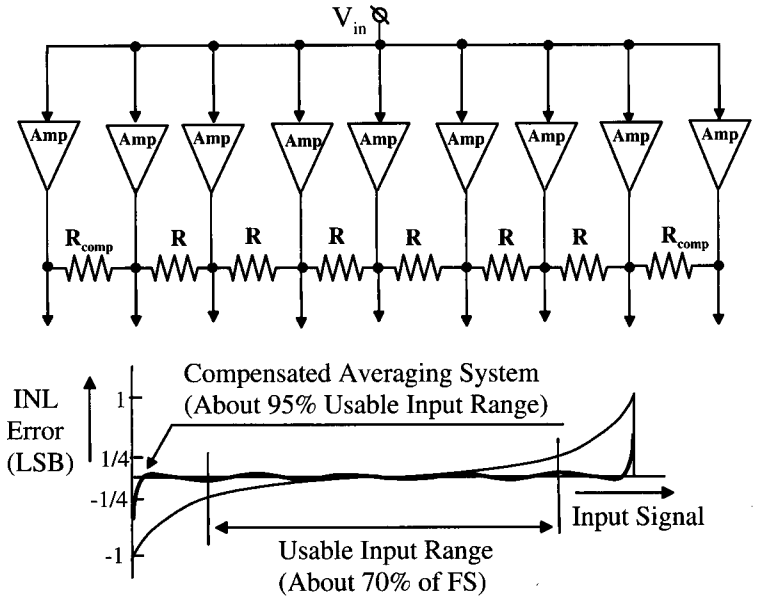


Figure 3.13: INL averaging compensation [113]

3.6.3 Moebius band averaging compensation

Because nearly all input amplifier are of the differential construction it is possible to obtain a non-linearity compensation using the Moebius band construction. The circuit diagram is shown in Fig. 3.14. In this compensation system the end signal of the averaging resistor string is connected to the inverted input side of the resistor string. This results in a continues ring of resistors. However, because the signals are not identical a misalignment occurs. In case the compensation resistor is adjusted, then an improvement in overall linearity is obtained. In this system extra amplifiers at the beginning and end of the reference ladder can be added to improve overall linearity. Spice simulations are required to obtain an optimum between linearity, extra amplifier pairs and signal range. An analytical result is too complicated to obtain.

3.6.4 Active averaging system

To avoid non-linearity caused by averaging a fixed amount of amplifiers can be determined that contribute to the averaging operation. In Fig. 3.15 the circuit diagram of such a system is shown. Again an averaging construction

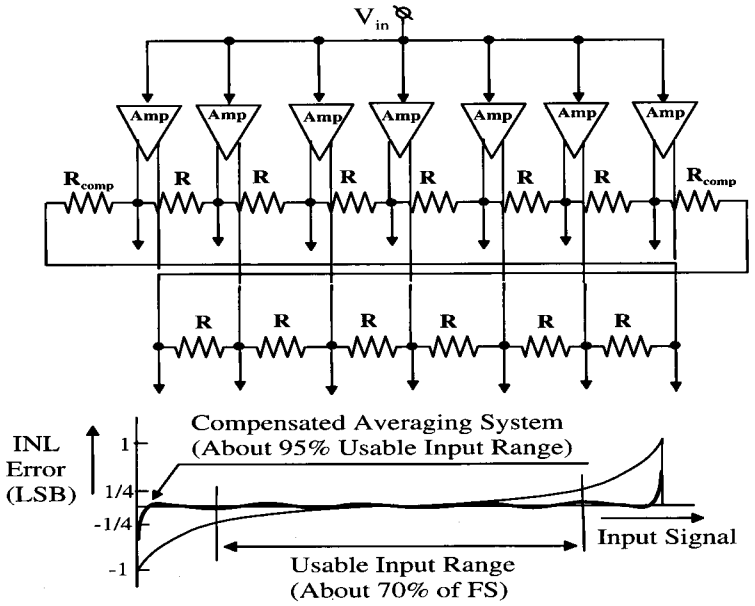


Figure 3.14: Moebius band averaging compensation

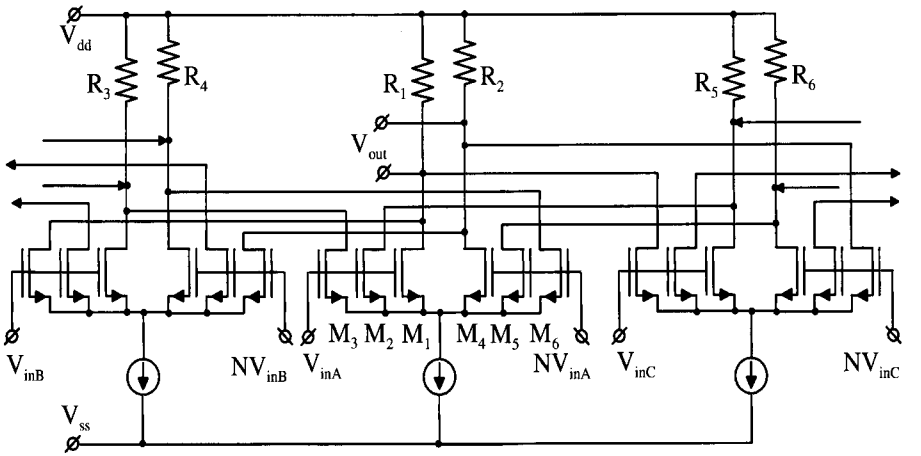


Figure 3.15: Active averaging system

is shown using three differential pairs. The input pairs in this system are split up into three parts. An equal split up is one of the possibilities that can easily be implemented. Starting with the middle pair consisting of M_1 to M_6, the output current of M_2 and M_5 go directly to the load resistors R_1 and R_2. From the left pair a split up current is added, while from the right part of the system again a current is added to the output current flowing through resistors R_1 and R_2. The output signal is obtained as the sum of the three neighboring differential pairs. Averaging occurs here over only three pairs. Therefore it is easy to determine the non-linearity of this system. Only one extra pair at the lower end and one extra pair at the higher end of the reference ladder are required to get an ideal linearity compensation. A drawback of this system is that more accurate elements, like the splitting up of transistors influence the offset and the linearity of the input system.

3.7 6-bit converter implementation

An application of the interpolation and averaging system is shown in [114]. The architecture of this flash converter is shown in Fig. 3.16 The input

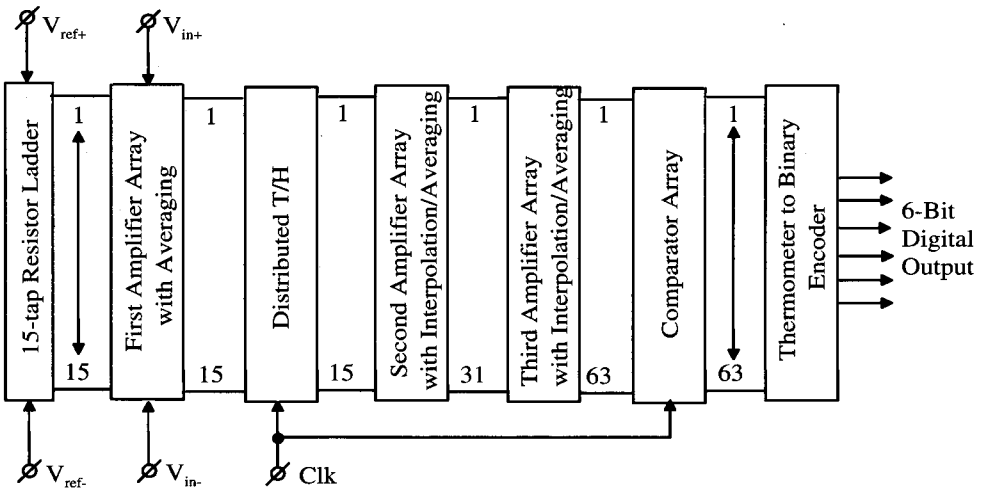


Figure 3.16: 6-bit converter architecture [114]

system consists of 15 differential stages that compare a differential input signal with a single reference voltage chain. After the input differential stages a distributed track-and-hold amplifier stage is used to sample the quantized input signal. In the second amplifier array consisting again out

of 15 stages a combination of averaging and interpolation is used. The number of output signals increase here to 31. The third amplifier stage uses again averaging and interpolation. At the output 63 amplified zero crossing signals appear that are applied to the comparator stages. The thermometer output code of the comparators is then converted into a binary weighted output code. Clock signals are only applied to the distributed track-and-hold amplifiers and the comparators.

3.7.1 Differential input amplifier system

The differential input amplifier system is shown in Fig.3.17. An optimum construction concerning linearity and accuracy for a differential input amplifier system uses two differential amplifiers and a single reference ladder. The output signals of transistors M_1 and M_3 are added and generate an output signal across load resistor R_1. The same is done for transistors M_2

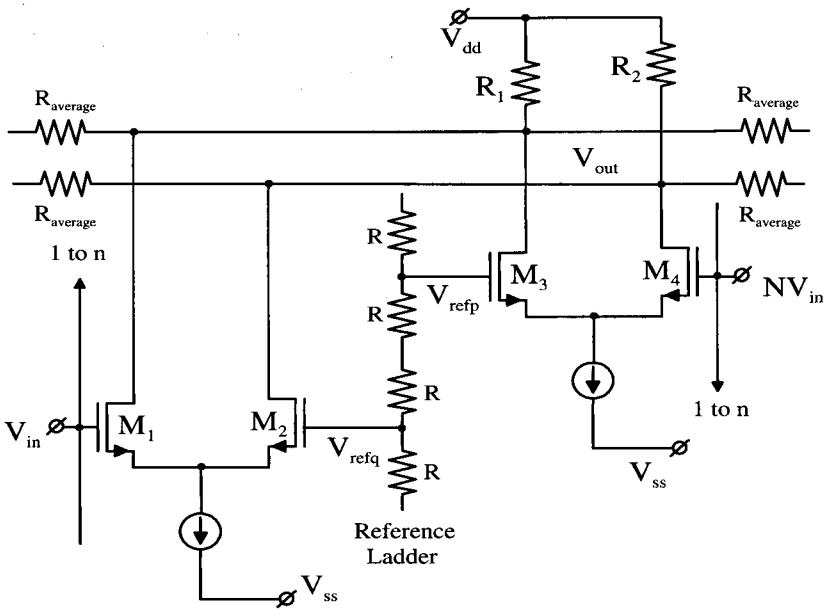


Figure 3.17: Differential input amplifier system

and M_4 using the load resistor R_2. At the gate of M_1 the input signal is applied, while at the gate of M_4 the inverted input signal is applied. In this way a differential input signal construction is obtained. Common mode signals applied at the input terminals are rejected depending on the matching between the input pairs M_1, M_2 and M_3, M_4 and the load resistors R_1

and R_2. When a positive common mode input signal is applied, then the current through M_1 increases. At the same time the current through M_3 decreases. The sum of the output currents of these two transistors is in a first approximation zero. The same occurs for the common mode signal applied to M_4 and M_2. Again these two currents must compensate at the output to reject the common mode signal. The described operation holds as long as the input devices are in the linear region. This means that only a limited amount of common mode voltage can be applied to this input system. It must be noted furthermore that the connections to the reference ladder per coupled differential pair are at the opposite terminal with respect to the zero reference in the middle of the ladder. At this middle point both differential pairs are connected to the same reference ladder terminal. A further disadvantage of this differential system can be the increase in offset voltage (with $\sqrt{2}$) and the increase in noise (with 3 dB). This is true at the moment an equal DC voltage across the load resistors is applied for a single differential stage and this circuit. Furthermore in this input system averaging is used to improve linearity caused by transistor offsets. This averaging is shown by the addition of the averaging resistors $R_{average}$.

3.7.2 Second and third amplifier stages

The circuit diagram of the second and third amplifier stages using averaging and interpolation are shown in Fig. 3.18. Here single differential amplifier stages with resistive loads are used. By splitting up the average resistors in two equal parts, the interpolation takes place. In this system a combination of averaging and interpolation is obtained. It must be noted with this system, that the output impedance of the interpolated signals is larger than the output impedance at the amplifier output terminals. Together with the load capacitance of the succeeding stage a position dependent bandwidth could be found. A careful choice of average resistor value, load resistor value and size of succeeding amplifier stage is needed.

3.7.3 ENOB measurement of 6-bit converter

At this point only the ENOB measurement of the practical implemented system will be given (see Fig. 3.19). For further details the reader is referred to study the article [114].

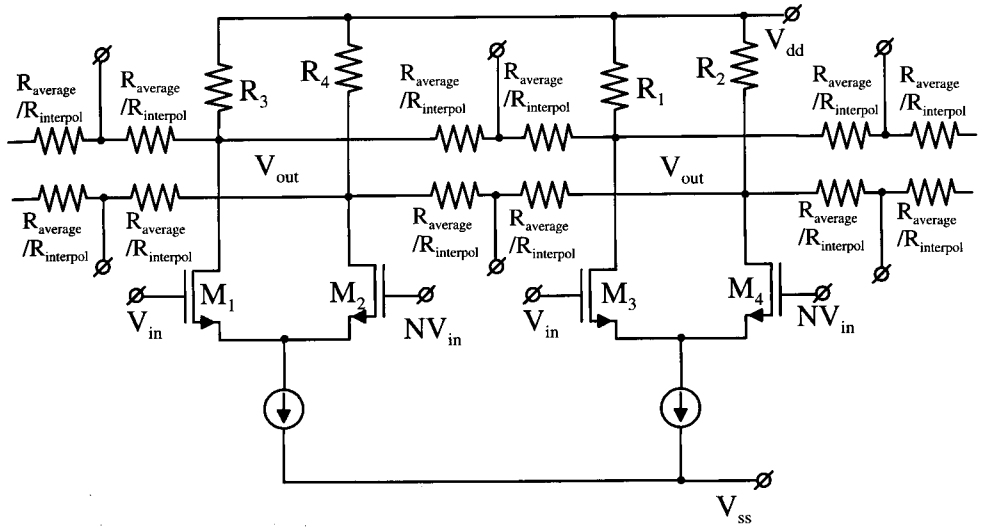


Figure 3.18: Combined averaging and interpolation amplifier system [114]

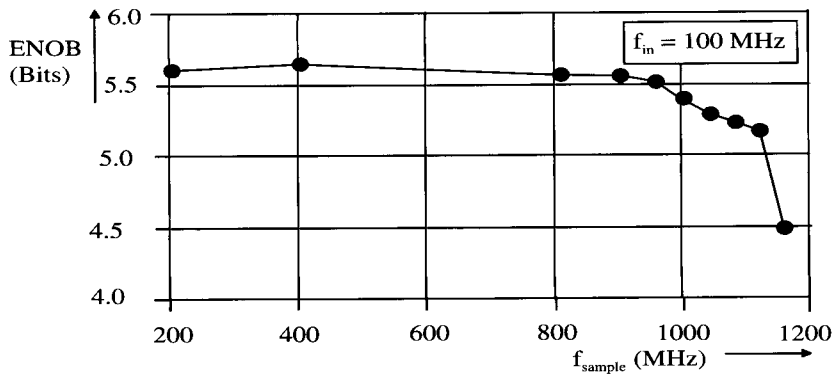


Figure 3.19: ENOB measurement [114]

3.7.4 Specification of 6-bit converter

In table 3.4 the specifications of the practical 6-bit converter are shown. The specification of the energy required to perform a conversion step is a

Technology	0.35 μ Standard CMOS Single Poly, Five Metal
Resolution	6 Bit
Effective Number of Bits	5.6 Bit
Resolution Bandwidth	450 MHz
Maximum Clock Frequency	1.1 GHz
Active Chip Area	0.3 mm^2
Supply Voltage	3.3 V
Power Dissipation	300 mW(ADC)
Analog Input Range	1.5 V (differential)
Integral Non-Linearity (INL)	1.5 LSB
Differential Non-Linearity (DNL)	0.7 LSB
Energy/Conversion Step	7 pJ

Table 3.4: 6-bit converter specification [114]

measure for the performance of the converter. This measure should be as small as possible.

3.8 Discrete time flash converter

The architecture of a 6-bit discrete time analog-to-digital converter is shown in Fig. 3.20 [115]. The converter consists of 32 input amplifiers, followed by an active interpolation stage using 64 amplifiers that drive the comparators. In this converter a bubble correction is used to avoid problems with the encoding in case more than one comparator stage in the thermometer code indicates a possible zero transition. In the input and second amplifier stage an auto zero operation is included to make the system less dependent on component matching. Furthermore the input stage is fully differential and needs only one reference ladder. The offset and reference information will be sampled on input capacitors and then during the next part of the sampling clock the comparison with the input signal takes place. The input amplifier circuit diagram is shown in Fig. 3.21. There are two modes of operation used in a discrete time input amplifier:

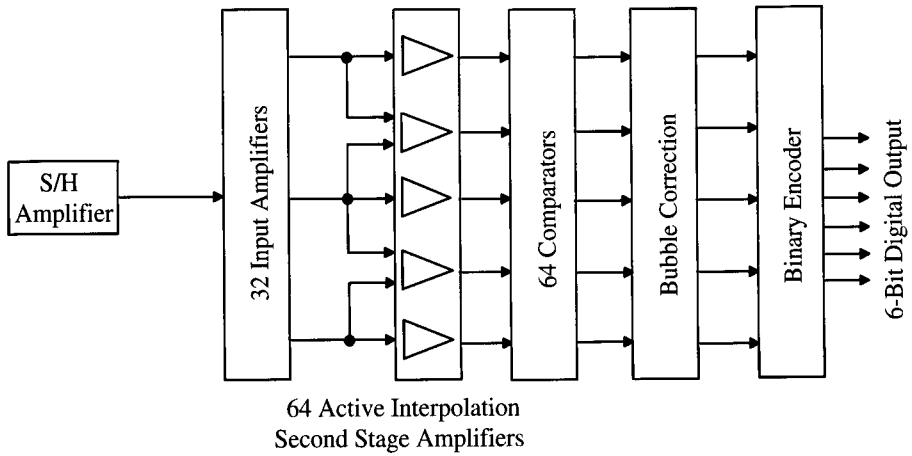


Figure 3.20: 6-bit converter architecture [115]

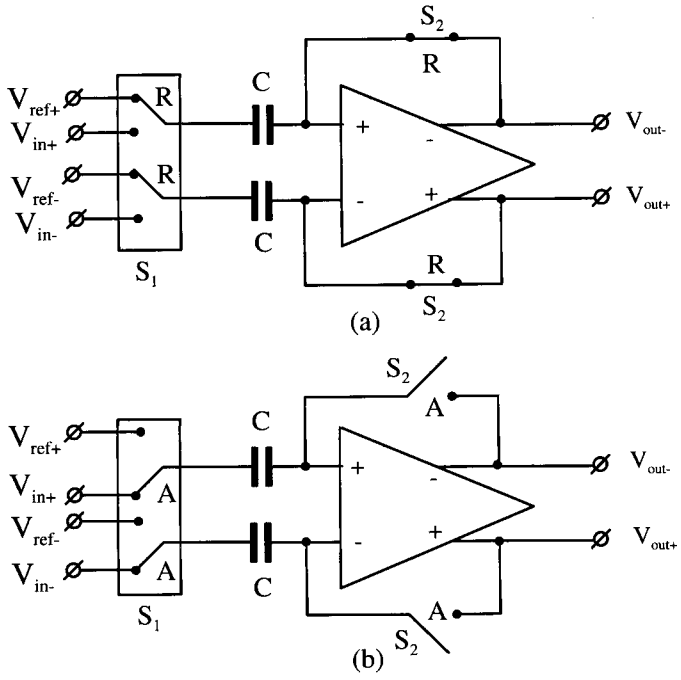


Figure 3.21: Discrete time input amplifier

- Reset mode (a)
- Amplify mode (b)

The reset mode is shown in Fig. 3.21(a). Switches S_1 are in the reset mode R and connect the reference voltage to the input capacitors C. Switches S_2 are closed. The differential amplifier in this mode acts as a low impedance and the reference voltages R_{ref+} and V_{ref-} are charged into the capacitors C. The amplify mode is shown in Fig. 3.21(b). Switches S_1 are in the amplify mode A and switches S_2 are open. The input signal is applied to the capacitors. The stored reference voltage on the capacitors is subtracted from the input signal and this difference signal is applied to the amplifier to be amplified. The output signals of these amplifiers can be applied to comparators to determine the zero crossing of the input signal. A thermometer code is obtained and with a decoder circuit this code can be converted into a binary weighted output code. In principle in this system a sample-and-hold amplifier is not required. A conversion takes place at the moment the comparators are activated to determine the zero crossing of the signal. However, it might be difficult to obtain a very small time skew between the sampling clock signal to the comparators. Therefore in the preferred application an input sample-and-hold amplifier is used. A very interesting detail is found in the design of the differential amplifier circuit used in this architecture. A circuit diagram of the amplifier is shown in Fig. 3.22. The input dif-

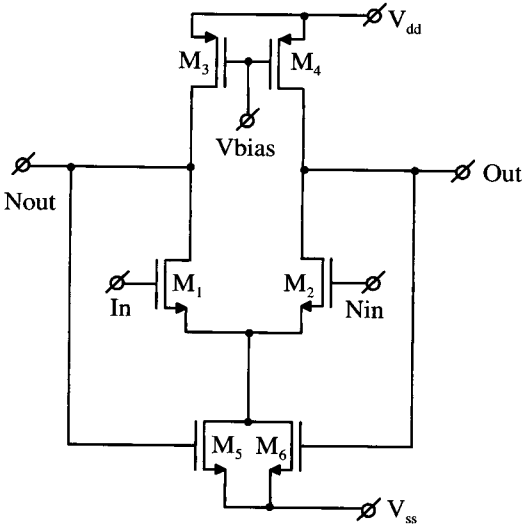


Figure 3.22: Differential amplifier circuit diagram [115]

ferential amplifier M_1, M_2 is loaded with current sources M_3, M_4 that are biased with V_{bias}. As a result of this construction, the tail current source consisting of transistors M_5, and M_6 must be controlled to obtain a good match between the drain currents of the input transistors M_1, M_2 and the load current sources. This current control is obtained by connecting the gates of M_5 and M_6 to the output terminals. This means that for common mode (bias) currents transistors M_5 and M_6 act as MOS diodes. The applied current from the current sources M_3 and M_4 will flow through the input transistors M_1 and M_2. The mismatch between the current sources adds to the offset of the input pair. The common mode level of the output stage is determined by the gate-source voltage of the biasing current sources M_5 and M_6. This means that a limited signal swing at the output can be obtained. In case a differential output signal is generated, then the gate-source voltages of M_5 and M_6 will have an opposite direction and with equal transconductance for these devices, no output signal variation will be found in the sum of the drain currents, being the tail current of the input differential pair. This operation is valid as long as the tail current pair is not over driven by the output signal of the differential input pair. This means that M_5 and M_6 must have a large linear signal range. A proper sizing of these devices is important for a good operation of the system. However, it can be noted that only around the zero crossing of this amplifier a linear operation is required. When over driven, the output signal in that case will be positive or negative and large enough to obtain an accurate comparison with the succeeding comparator.

3.8.1 Second amplifier stage

In the second amplifier stage active interpolation with an auto zero operation is used. The circuit diagram of the second stage is shown in Fig.3.23. This amplifier stage consists of two coupled differential stages using a controlled tail current source identical to the circuit from Fig. 3.22. The output load current sources M_9 and M_{10} have controllable current sources in parallel to add or subtract currents needed to obtain the auto zero operation. These current sources formed by the differential pair M_{11} and M_{12} is biased by the current source M_{13} to supply the extra control current. A current source biasing is needed here to obtain the required output common mode voltage set by the gate source voltage of transistors M_5, M_6 and M_7, M_8. During the auto zero clock phase, the inputs of differential pairs M_1, M_2 and M_3, M_4 are short circuited and at the same time the switches "auto zero" are closed. The required differential current to adjust the output offset is applied

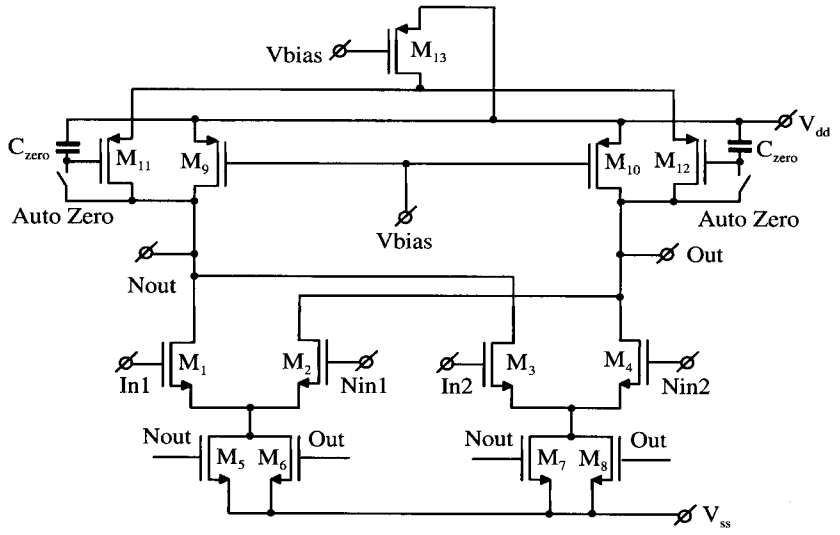


Figure 3.23: Second amplifier circuit diagram [115]

to the circuit and the difference is stored on the capacitors C_{zero}. During the amplify mode of the circuit the offset is held on the capacitors and the difference current is supplied to the output load. In this way an accurate interpolation depending on the transconductance of the input differential stages is obtained.

3.9 Gray code full flash converters

To reduce the number of comparators an analog encoding of the comparator input signals is used [53, 50]. A low device count implementation is obtained with a Gray coding of the signal. The advantage of the Gray code is that with a linear increasing input signal only one comparator may change state. In Table 3.5 the Gray code and the offset binary code are repeated for ease of understanding the total circuit implementation. Note from the table that in the Gray encoding there exists a mirroring of the code and that with every one bit increase only one bit changes state. The most significant bit can be encoded using a comparator at reference level 8.
The MSB-1 code is obtained by combining the comparator with input reference level 4 with the comparator with input level 12. To obtain the right information a cross-coupling of comparators must be used. This cross-coupling will be explained later.

DECIMAL VALUE	BINARY CODE	GRAY CODE
0	0 0 0 0	0 0 0 0
1	0 0 0 1	0 0 0 1
2	0 0 1 0	0 0 1 1
3	0 0 1 1	0 0 1 0
4	0 1 0 0	0 1 1 0
5	0 1 0 1	0 1 1 1
6	0 1 1 0	0 1 0 1
7	0 1 1 1	0 1 0 0
8	1 0 0 0	1 1 0 0
9	1 0 0 1	1 1 0 1
10	1 0 1 0	1 1 1 1
11	1 0 1 1	1 1 1 0
12	1 1 0 0	1 0 1 0
13	1 1 0 1	1 0 1 1
14	1 1 1 0	1 0 0 1
15	1 1 1 1	1 0 0 0

Table 3.5: Gray code table

The MSB - 2 code is obtained by combining the comparators with reference level 2, the comparator with reference level 6, the comparator with reference level 10, and the comparator with reference level 14. Again a cross-coupling of the stages is required to obtain the right encoding.
Finally, comparators with input levels of 1, 3, 5, 7, 9, 11, 13, and 15 are cross-coupled to obtain the LSB code information.
Note that an even number of encoding stages is needed except for the MSB. In Figure 3.24 an example of the encoding stages for the MSB, MSB-1, and MSB-2 codes are shown. The analog encoding of the comparator signals is performed by differential pairs. From Figure 3.24 it can be understood that every time a differential amplifier changes state, the output comparator which is connected between the output load resistors (e.g., R_1, R_2 . . R_6) must sense this difference voltage. The cross-coupling between the stages is needed to perform the 0 to 1 and 1 to 0 transition every time a level is detected. Because of the even amount of comparators, a middle level is not detectable. An odd number of stages is needed to perform a zero crossing in the system. Therefore, an extra current with a value I_0 must be connected to the output load resistor to obtain an accurate code transition detection.

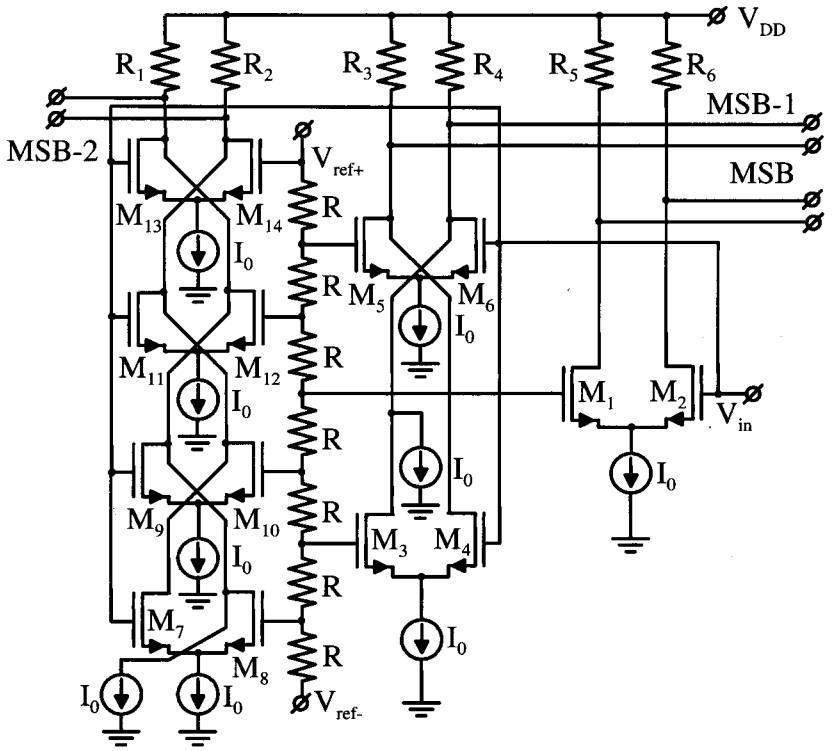


Figure 3.24: Analog Gray encoding for MSB, MSB-1, and MSB-2

The output code then changes state as shown in Figure 3.25. Note that only

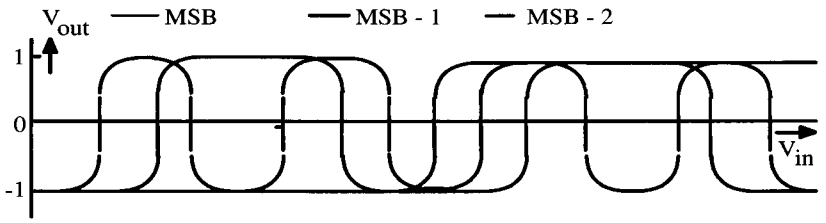


Figure 3.25: Output signal of the analog encoder

the MSB requires a single comparator stage giving an odd number of stages. Differential pair M_1, M_2 performs the MSB detection. The cross-coupled differential pairs M_3, M_4 and M_5, M_6 perform the MSB-1 detection. Note that the extra current source I_0 is connected to R_4 to obtain the zero crossing in case differential pair M_3, M_4 or M_5, M_6 are at equilibrium. The same current I_0 will flow through the load resistors R_3 and R_4 and the differential output current of the equilibrium pair will determine the zero crossing. Furthermore it is seen that always through the load resistors in this MSB-1 comparison stage a DC bias of I_0 will flow as a common mode signal. This might reduce the signal swing at the output. The encoding of MSB-2 is determined by the cross coupling of four differential stages (M_7, M_8, M_9, M_{10}, M_{11}, M_{12} and M_{13}, M_{14}). Again an extra current source I_0 is added to the system to obtain an accurate zero crossing. Because of the increasing number of encoding stages that are loading the output load resistors R_1, R_2 . . R_6 the bandwidth of the system is reduced, therefore decreasing the accuracy with which a high-frequency signal can be encoded. To overcome this problem a two-step encoding using two clocked comparators for the LSB must be used. The final LSB is then obtained by a logical combination of the two output codes.

The advantage of this system is the small amount of clocked comparators needed for the conversion, resulting in a small die size and a low power consumption. The disadvantage of the system is the difference in comparator delay of the different encoding stages, resulting in coding errors and distortion. With a sample-and-hold function in front of the system this problem can be overcome.

3.10 Circular code flash converters

To obtain equal comparator loading, an implementation of a circular code can be used [5]. Table 3.6 shows again the circular code implementation. To make the understanding easier of the encoding, a decimal code is added. Using Table 3.6 the MSB of the circular code is equal to the MSB of the

DECIMAL VALUE	BINARY CODE	CIRCULAR CODE
0	0 0 0	0 0 0 0
1	0 0 1	0 0 0 1
2	0 1 0	0 0 1 1
3	0 1 1	0 1 1 1
4	1 0 0	1 1 1 1
5	1 0 1	1 1 1 0
6	1 1 0	1 1 0 0
7	1 1 1	1 0 0 0

Table 3.6: Circular code table

binary code. All other circular codes shown in this simple example have only two transitions. These transitions are implemented by using two cross-coupled differential amplifiers as shown in Figure 3.26. The MSB-1 is obtained by cross-coupling differential amplifiers at decimal level 3 with the amplifier at level 6. MSB-2 is obtained by cross-coupling amplifier at level 2 with the amplifier at level 5. In case of the LSB code, the amplifier at decimal level 1 is cross-coupled with the amplifier at level 4. At the output of the cross-coupled amplifiers a comparator is added to obtain at the clock transitions a digital output code. With an EXOR function the code transitions are determined and converted into a binary code using a ROM structure. The advantage of the circular code implementation is a reduction in the amount of required comparators of at least a factor two. The loading of the "folding" (cross-coupled amplifier stages) is identical for all output "bits" except the MSB bit which only needs one amplifier-comparator stage. Up until a much higher input frequency a more equal delay in the system is obtained. Similar circuits will be used in "folding" analog-to-digital converters described in one of the following sections.

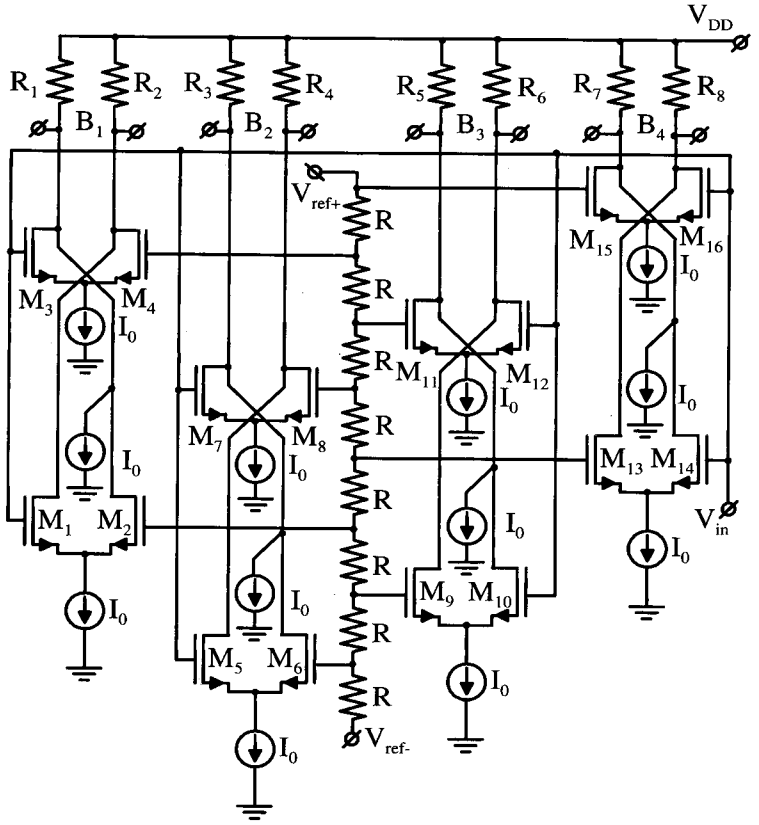


Figure 3.26: Circular code circuit implementation

3.11 Two-step flash converters

To avoid some of the problems encountered with a full-flash converter the two-step architecture was developed. This two-step method uses a coarse and fine quantization to increase the resolution of the converter (see Figure 3.27). Examples of converters using the two-step architecture are given in these references: [39, 54, 55, 57, 58, 80, 83]. Consider, for example, an 8-bit

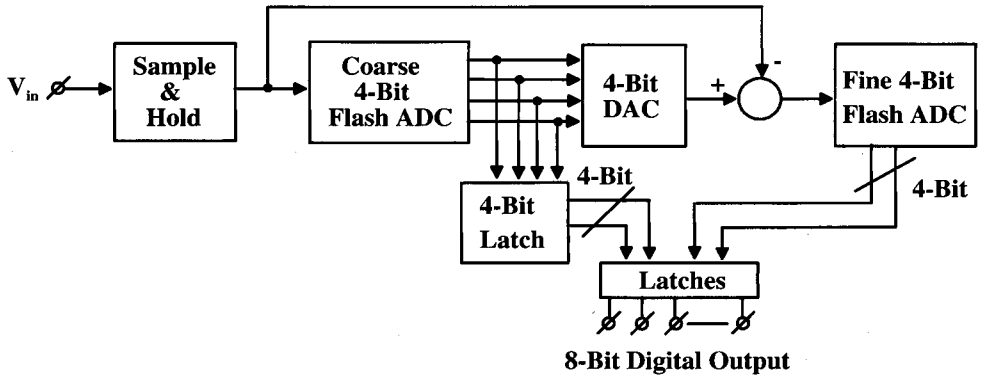


Figure 3.27: Two-step A/D converter structure

system that uses a 4-bit coarse quantization. After the coarse quantization has been performed, the 4-bit digital data are converted into an analog value again using a 4-bit D/A converter. This analog value is subtracted from the input signal and the difference is applied to a 4-bit fine converter which generates the fine code.

In this system an ideal coarse-fine signal level matching is expected. In practical applications, however, timing and accuracy limitations can result in conversion problems resulting in "missing" codes. To avoid such a problem, the full-scale range of the fine converter is increased with respect to the LSB step size of the coarse system. In this way a compensation for errors between coarse and fine conversion is obtained.

In this system only 40 comparators are needed to achieve 8-bit resolution. The (4-bit) D/A converter in these applications, however, needs to have an 8-bit accuracy and linearity to obtain the full 8-bit overall linearity. Furthermore, a sample-and-hold amplifier is needed to compensate for the time delay in the coarse quantization/reconstruction step. In this way the dynamic performance of the A/D converter is mostly determined by the performance of the sample-and-hold amplifier. In pipe-lined architectures a second sample-and-hold amplifier is used to store the analog remainder of the input

signal for fine quantization. In the meantime a new input sample is coarse-quantized. This architecture results in a higher throughput rate for the total system. Higher resolutions can easily be obtained without a drastic increase in hardware and power dissipation. The applicability of this converter type depends on the availability of high-performance sample-and-hold amplifiers.

3.11.1 Two-step A/D converter implementation

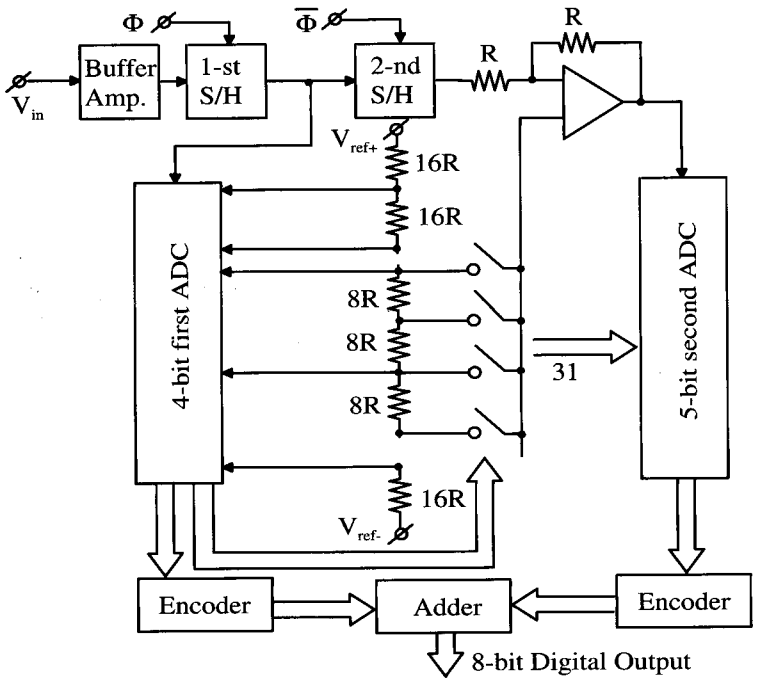


Figure 3.28: Two-step A/D converter implementation

In Figure 3.28 a two-step converter implementation is shown. The system is built-up using a first 4-bit coarse quantizer with built-in D/A converter function and a second 5-bit fine quantizer. The first sample-and-hold amplifier samples the analog input signal. This signal is converted into a digital value using the first 4-bit flash A/D converter. The information of the first quantizer is stored and the D/A converter segment is switched on. The D/A converter consists of a string of resistors having a double function. The first function is the generation of the reference voltages for the 4-bit coarse flash converter. When a coarse quantization has been performed, then the output data are stored, and the thermometer encoding in the flash converter allows

an easy control of the reconstruction D/A converter. This is the second function of the resistor string. From the figure it can be seen that in the D/A converter a double amount of taps is used. The subtracter circuit has a gain of two for signals applied at the non-inverting terminal. The D/A voltage is applied at this side and therefore the step sizes of the D/A must be reduced to half the step sizes of the 4-bit coarse quantizer. The extra tap voltages are generated over the resistors $8r$. After completion of the coarse quantization, the input signal is transferred into the second sample-and-hold amplifier. Then the D/A output signal is subtracted from the analog input signal and the remainder is applied to the 5-bit fine quantizer. Next, fine quantization takes place and the data are stored in latches. A 5-bit quantization is used to allow corrections for overflow and offset errors from the second sample-and-hold amplifiers and gain errors in the subtraction circuit. Finally, the two digital signals of the coarse and the fine quantizer are added to obtain a corrected 8-bit output signal.
In Figure 3.29 a more detailed circuit implementation of the sample-and-hold amplifiers and the subtracter circuit is shown. The sample-and-hold

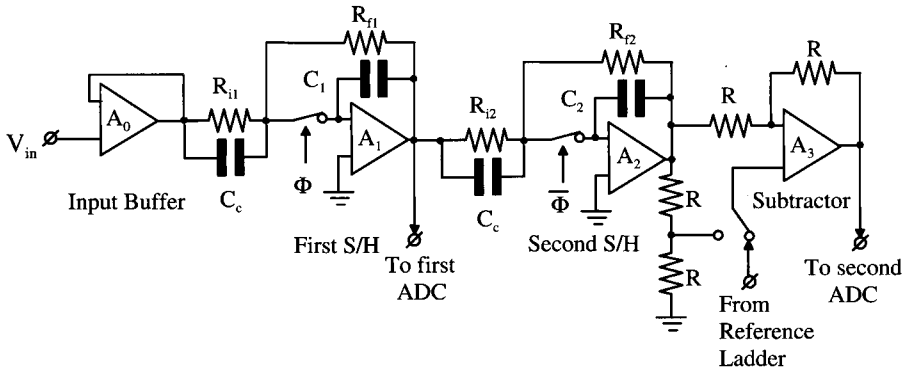


Figure 3.29: Detailed circuit diagram of the S/H and Subtracter circuit

amplifiers are, as discussed above, of the inverting type. The connection of the hold capacitor in parallel with the feedback resistor R_F introduces a frequency limitation that is not allowed. Therefore, across the input resistor R_I a compensation capacitor C_C is connected. With equal time constants the signal bandwidth of the sample-and-hold amplifiers is only dependent on the bandwidth of the amplifiers. However, with a limited accuracy in compensation a not exact pole-zero cancelation is introduced. This pole-zero error results is slow settling components in the output signal.

3.11.2 Two-step capacitive MDAC A/D converter

By incorporating a binary-weighted capacitor D/A converter into a sample-and-hold amplifier system, a two-step recycling A/D converter has been designed. In Figure 3.30 the basic system is shown [85]. From Figure 3.30

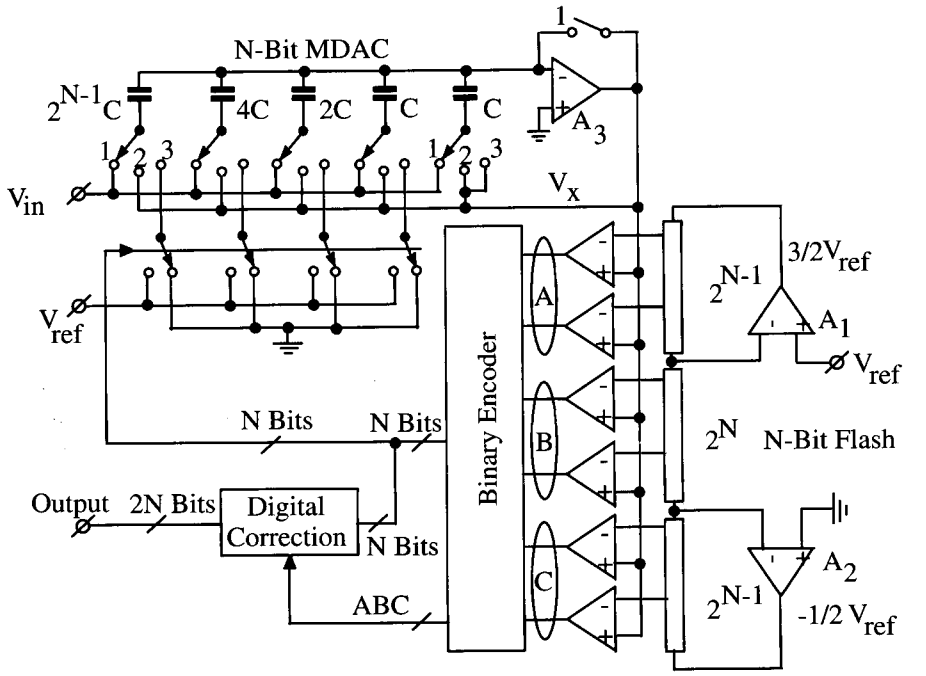


Figure 3.30: Two-step recycling A/D converter system [85]

the multiplying binary-weighted capacitor D/A converter can be seen. This D/A converter with the switched buffer amplifier A_3 operates as a sample-and-hold amplifier, a residue amplifier, and D/A amplifier. The output signal of the sample-and-hold amplifier is applied to the quantizer, consisting of a parallel A/D converter with overflow. To simplify the understanding of the operation of the system, the three different phases of the quantization are shown in Figure 3.31. In the top figure the input signal sampling is shown. The input signal is sampled on the binary-weighted capacitor D/A converter array.
The middle figure shows the hold phase of the system. The capacitor D/A converter array is switched between the input and the output of the buffer amplifier. During the hold mode the coarse quantization is performed using the parallel quantizer. The coarse data are stored, and the D/A operation

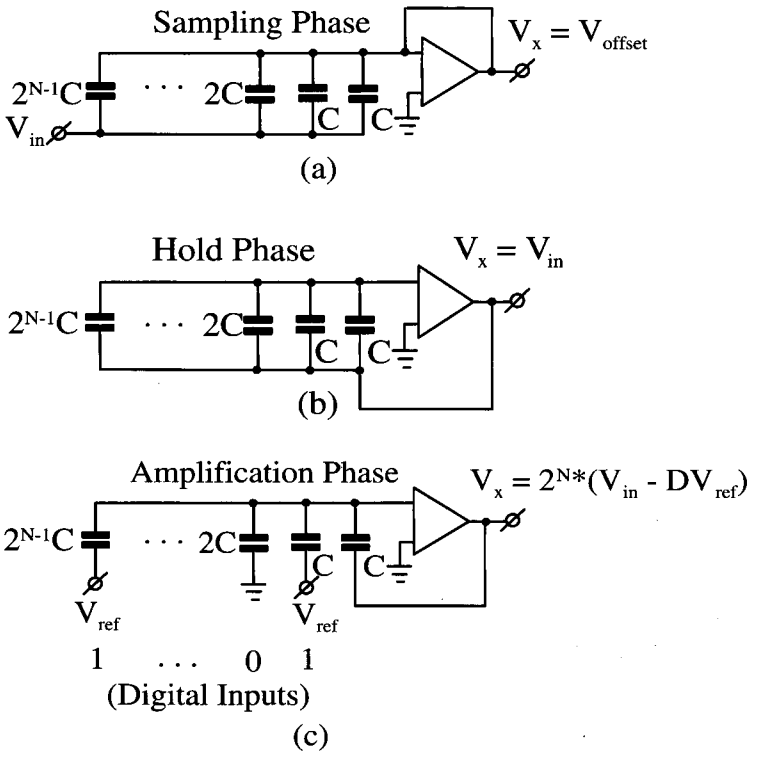


Figure 3.31: Three operation phases of the two-step A/D converter [85]

is performed which subtracts the coarse quantized signal from the analog input sample. In the bottom part of the figure this operation is shown. The residue signal is amplified by connecting a capacitor C between the input and the output of the buffer amplifier. An amplification with 2^N of the residue signal is obtained. Then the residue is quantized again to obtain the fine output code. The total output code is obtained by combining the fine and the coarse data.
Accuracy and linearity of this system are basically only determined by the accuracy of the binary-weighted capacitor array.

3.12 Sub ranging converter architecture

The sub ranging converter architecture is basically a two-step architecture. However, in the sub ranging system no gain stage between the first converter stage and the second converter stage is used. Matching problems between

gain stages and reference voltage of the second or subrange converter stage are avoided in this way. In Fig. 3.32 a basic subrange system is shown. An

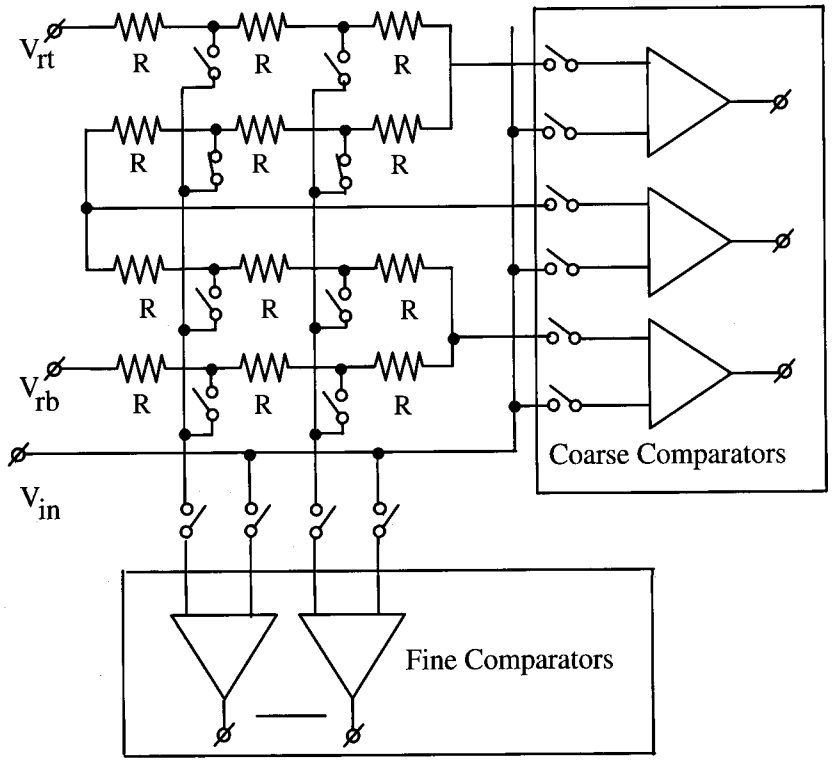


Figure 3.32: Sub ranging converter architecture

ideal 8-bit Sub ranging converter consists of a 4-bit coarse quantizer using 16 coarse comparators and a 4-bit fine quantizer using 15 fine comparators. Furthermore a reference ladder with $2^N - 1$ ladder taps is used. The coarse comparators are connected to 16 coarse ladder taps as shown in Fig. 3.32. These ladder taps have 15 fine taps in between of every coarse tap. When the coarse information is obtained, then the fine ladder taps in between of the coarse signal are addressed and the fine conversion can take place. It must be clear that at the input a sample-and-hold amplifier is needed to sample the analog input information. During the hold mode the coarse and fine conversion take place. In general the coarse comparators do have less gain than the fine comparators. Furthermore in a practical system an over and under range is required for the fine converter to correct for small errors encountered in the coarse quantization. Linearity of this system

is determined by the input sample-and-hold amplifier, the linearity of the reference ladder and the offset voltage of the fine comparators.

3.12.1 8-bit Sub ranging converter implementation

The architecture of an 8-bit Sub ranging converter is shown in Fig. 3.33 [57]. This converter consists of 16 coarse comparators connected to 16 coarse lev-

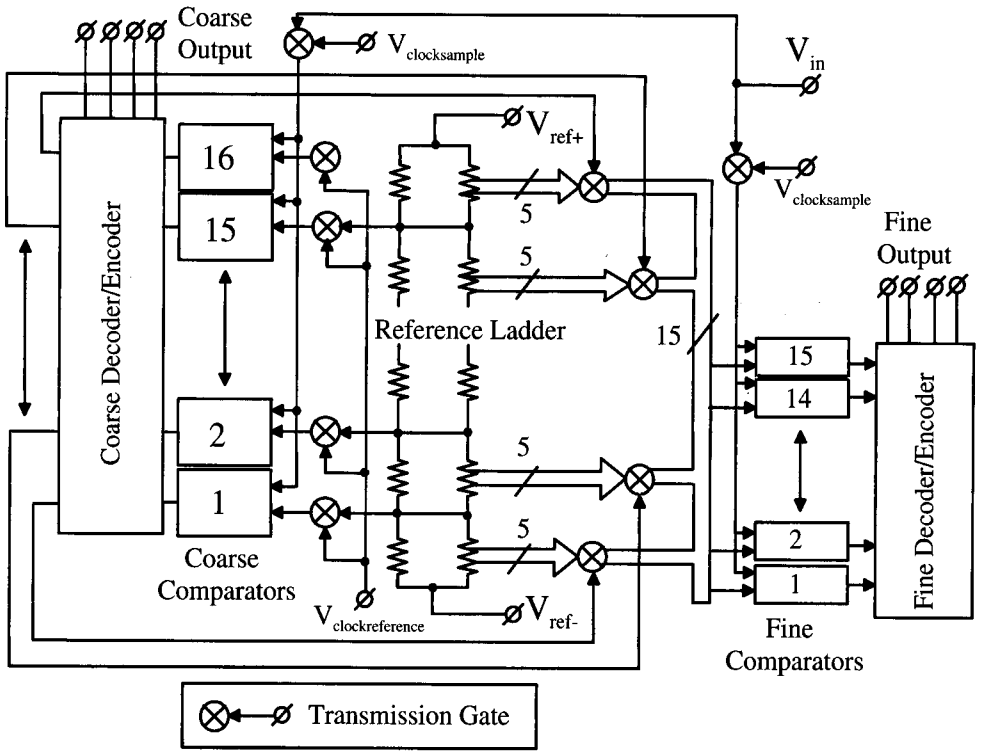


Figure 3.33: 8-bit Sub ranging converter architecture [57]

els of the reference voltage and 15 fine comparators connected to subranges of the reference ladder. The coarse converter determines the subrange ladder section that is applied to the fine converter to obtain the fine conversion. In this system no over range is used in the fine converter. In the following sections the coarse comparator, fine comparator and the reference ladder structure will be discussed.

3.12.2 Coarse comparator

The circuit diagram of the coarse comparator used in the 8-bit converter is shown in Fig. 3.34. The coarse comparator consists of switches, a storage

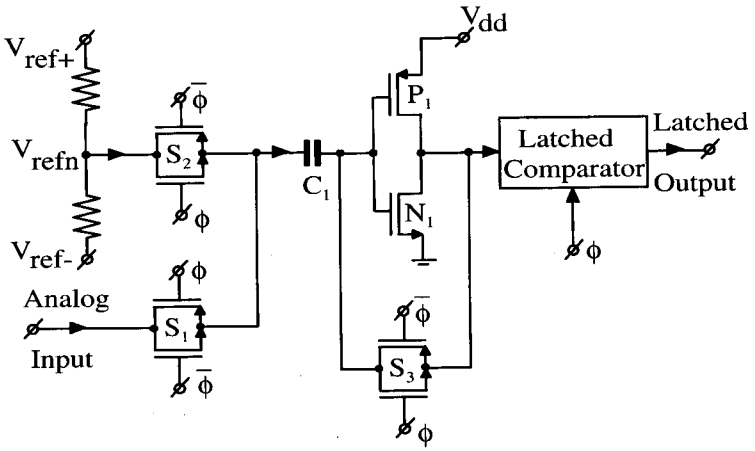


Figure 3.34: Coarse comparator circuit diagram

capacitor and an CMOS inverter followed by a latched comparator stage. The switches S_1, S_2 and S_3 consist of transmission gates to obtain a low impedance during closing of the switch. The transmission gate gives over a large signal level range a reasonable low on resistance. The operation of the circuit is as follows. Suppose switches S_2 and S_3 are closed, then the inverter stage consisting of transistors N_1 and P_1 is biased around half the supply voltage. The maximum bias current will flow through the inverter at this condition, while the impedance of the short circuited inverter is at its lowest value. This impedance can be estimated at:

$$R_{in} = \frac{1}{g_{mN} + g_{mP}} \approx \frac{1}{2g_{mN}}. \tag{3.10}$$

With switch S_2 closed, the reference voltage V_{refn} is charged on capacitor C_1. When switch S_1 is closed and the other switches are opened, then the input signal minus the reference voltage is applied to the gates of the inverter stage. This inverter shows maximum signal gain because of the previous bias condition. The difference signal is amplified and applied to a latched comparator to determine a digital output signal.

3.12.3 Fine comparator

The circuit diagram of the fine comparator is shown in Fig. 3.35 In the fine

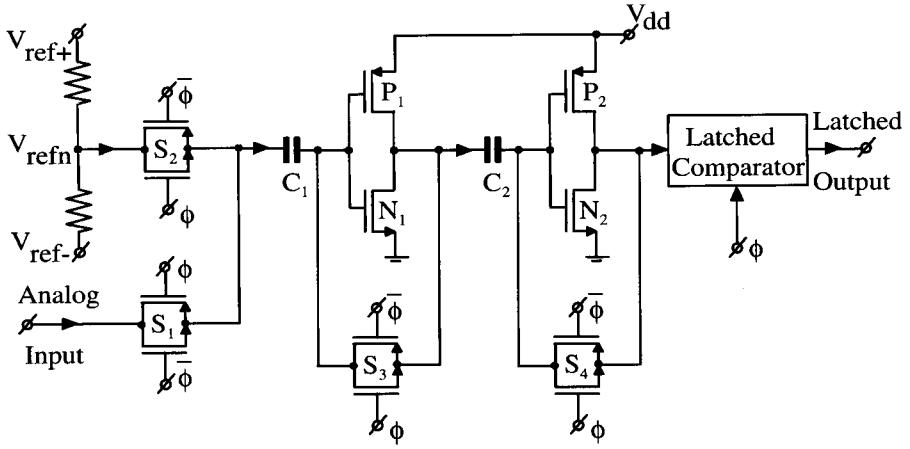


Figure 3.35: Fine comparator circuit diagram

comparator more gain is required to perform a reliable conversion of the analog signal into a digital output. Therefore an extra gain stage is added. This gain stage consists of an inverter N_2, P_2 with a storage capacitor C_2 and the transmission gate switch S_4. During the reference sampling mode switches S_2, S_3 and S_4 are closed and the reference voltage is charged on capacitor C_1. Capacitor C_2 stores the difference in gate-source voltages between the first and the second inverter stage. These inverter stages are during the sampling mode biased around half the supply voltage. When switch S_1 is closed, all other switches are open and the difference between input signal and reference voltage is applied to the gates of N_1 and P_1. This difference is amplified by the two inverter stages and then applied to a latched comparator to obtain a digital output signal. More gain is obtained in this system while offsets are canceled because of the two sampling conditions used.

3.12.4 Reference ladder construction

The reference ladder used in the 8-bit converter shows a specific implementation depicted in Fig. 3.36. The coarse taps of the reference ladder are built up using low value resistors R_{coarse}. This means that a good linearity and a small influence during reference sampling mode is obtained. The

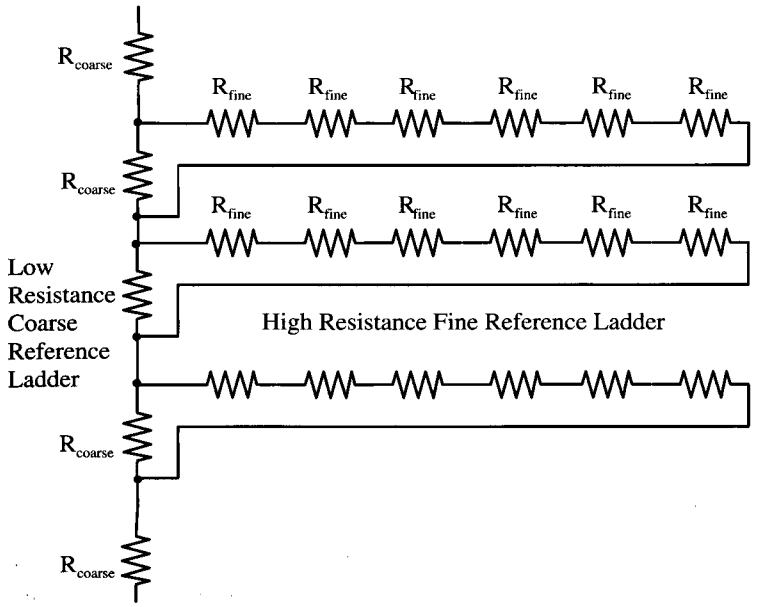


Figure 3.36: Reference ladder construction [57]

fine ladder taps are connected between the coarse taps each and use high resistor values R_{fine}. 15 resistors are used to obtain the fine levels needed in the 8-bit converter. The low impedance coarse ladder results in a small variation of the fine ladder impedance with respect to the fine comparators. Ladder linearity is determined by the coarse ladder while the fine ladder interpolates in between the coarse steps. Smaller size resistors can be used without influencing the overall accuracy.

3.12.5 Interleaved comparator flash converter

A doubling of the sampling speed is obtained by multiplexing the input comparator part. In Figure 3.37 a simplified circuit diagram of the comparator system is shown. The circuit consists of two comparator circuits as shown in Figure 3.35 in parallel. Two extra CMOS inverter stages are added to increase the comparator gain. The output signal of the comparators is applied to the output latch circuit via multiplexer S_7, S_8. The operation of the circuit is as follows. At the moment the input comparator part marked A_1 and A_2 is in the sampling mode by closing switches S_1, S_5 and S_8, the comparator part marked B_1 and B_2 is in the decision phase. Switches S_3 and S_8 are closed and the decision information is applied to the output latch. At

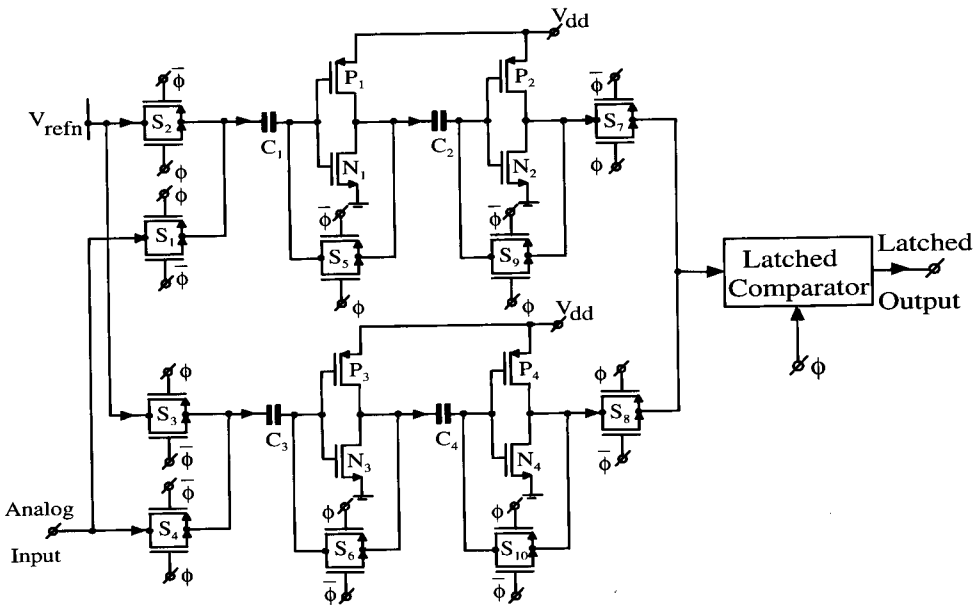


Figure 3.37: Interleaved comparator A/D converter

the next clock phase the function of comparator A_i and B_i is interchanged and the decision information from A_2 is applied to the latch via switch S_7. Using the dual input system, effectively a doubling of the sampling clock frequency is possible without loosing converter performance. However, sampling occurs on the rising *and* falling edge of the clock requiring an accurate square wave clock with small jitter on both edges.

3.12.6 Interleaved comparator two-step A/D converter

To increase the conversion speed of an A/D converter with comparators running at maximum speed, the number of coarse and fine quantizer blocks must be increased. An interesting optimum between the number of components and the maximum conversion speed is obtained by using one 4-bits coarse quantizer and two time interleaved 4-bits fine quantizers. In Figure 3.38 the system implementation of this converter is shown. The operation of the converter with the time interleaving of the fine comparators is as follows. During the sampling and coarse quantization of the input signal the coarse quantizer and the fine quantizer (A) are connected to the input terminal. After the input signal has been sampled, the coarse quantization is performed. Then the information from the coarse quantizer is used to generate

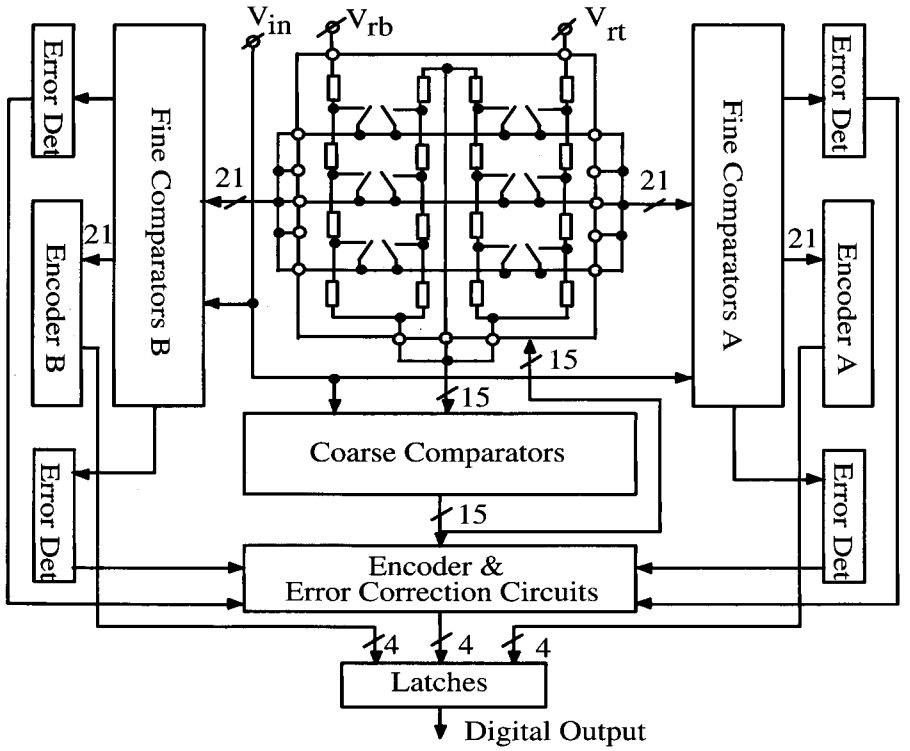


Figure 3.38: Interleaved comparator two-step A/D converter system

the fine reference levels to perform the fine quantization. Fine quantization is performed during a period equal to the time it takes to sample the input signal and perform a coarse quantization. The interleaving now occurs by taking the second input sample using the coarse quantizer and the second fine quantizer (B). At the moment the fine comparison of the first input sample is finished, the second fine converter (B) can start processing the second sample. During this processing the third input sample is taken using the coarse quantizer and the fine quantizer (A). This procedure repeats and the conversion speed can be increased to about two times the speed of the system from Figure 3.35. During the switching of the comparators an extra averaging period is used to increase speed and obtain a more accurate decision. In Figure 3.39 the operation of the fine quantizer is shown. At the

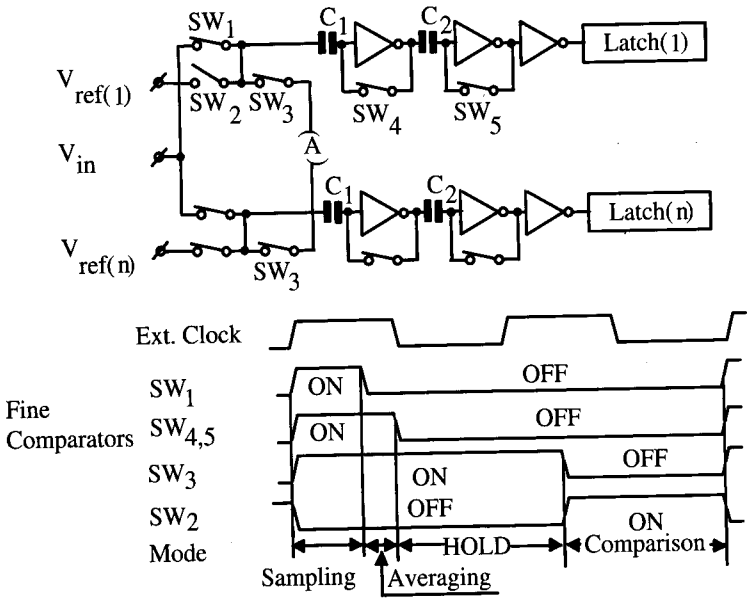


Figure 3.39: Fine quantizer circuit configuration and timing diagram

moment the sampling switch SW_1 is switched off, then the comparators still remain during a short period of time into the short circuited sampling mode. The switches SW_3 remain closed which results in an averaging of the channel charge and feed-through charge of the sampling switches SW_1. These charges are sampled on the capacitors C_1. Then switches SW_4 and SW_5 are switched off. A short time later switches SW_3 are opened and switches SW_2 are closed to perform the comparison. By this circuit implementation

a more accurate comparison of signals is possible. The averaging operation divides capacitive crosstalk and channel charge equally over all the sampling comparators resulting.

3.12.7 10-bit subrange converter

The architecture of a 10-bit subrange converter is shown in Fig. 3.40 [116]. The system consists of a 5-bit coarse converter using 31 comparators and a 5-

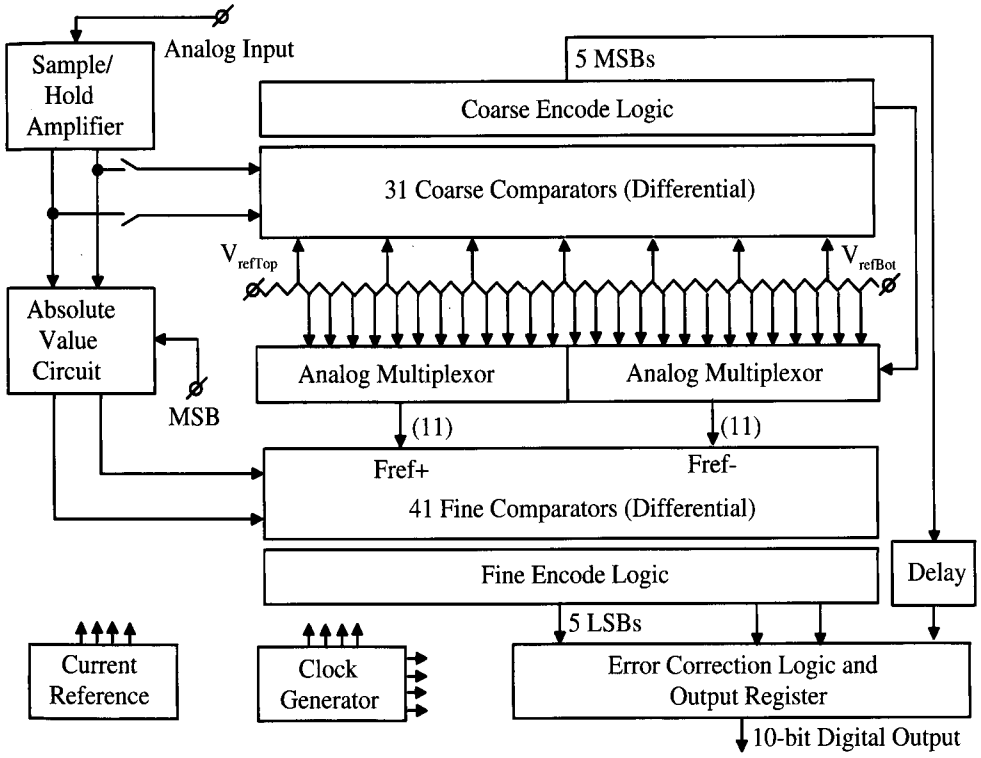


Figure 3.40: 10-bit Sub ranging architecture [116]

bit fine converter with over range using 41 comparators. At the low-end and high-end of the fine converter range 5 extra comparators are added to correct conversion errors of the coarse converter. Errors can be introduced by offsets between coarse and fine converters, timing errors, droop in the sample-and-hold amplifier and errors caused by charge freed through in switches. The output signal of the coarse converter addresses an analog multiplexer that applies the fine reference signals to the fine converter for further processing. Between the coarse and the fine sampled analog signal an absolute value

detector consisting of a set of switches is applied. With this configuration half the amount of switches is needed for the fine converter multiplexer. The whole internal system of the converter is differential so the absolute value system is easy to implement. A single reference ladder is used, requiring special amplifiers for the coarse and fine converter stages. Furthermore these amplifier stages use interpolation to minimize the loading of the sample-and-hold amplifier and the reference ladder. A single ended signal can be applied to the system. This single ended signal is converted into a differential sampled analog signal by the sample-and-hold amplifier. This sample-and-hold amplifier uses the full clock cycle to hold the information. Sampling is performed on the input capacitor and then the signal is transferred to the hold function. During hold the signal is once again transfered into a second hold capacitor to obtain the sampled information for the fine converter. This sample-and-hold amplifier will be described in a separate chapter about this subject.

3.12.8 Coarse converter stage

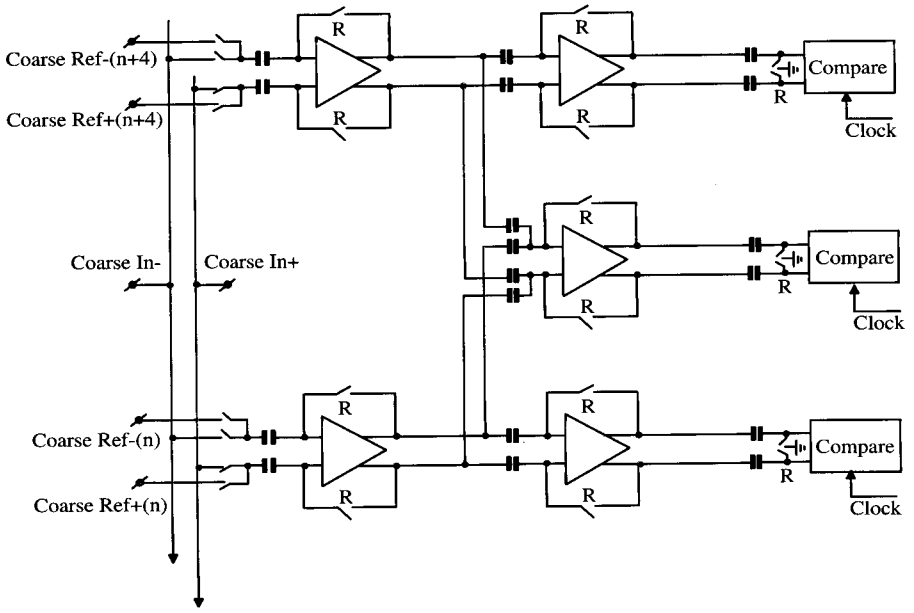


Figure 3.41: Coarse converter stage [116]

The circuit diagram of the coarse converter stage is shown in Fig. 3.41. The system uses a cascade of two differential amplifier stages in front of the

comparators. A single capacitive interpolation is used to reduce the number of coarse amplifiers loading the input sample-and-hold amplifier and the reference ladder. First the switches called R are closed. At this moment the reference voltage is loaded into the input capacitors, while in the second stage the capacitors hold the offset voltage between first and second stage. At the input of the comparators again the offset of the second stage is held. Then the switches R are opened and the input signal from the sample-and-hold amplifier is amplified and the comparators convert this signal into the digital coarse code. This code is used to address the analog multiplexer that applies the reference signal to the fine converter stage.

3.12.9 Fine converter stage

The fine converter stag is shown in Fig. 3.42. This circuit diagram is except from the extra capacitive interpolation used after the second stage identical to the circuit of Fig. 3.41. The interpolation introduced after the second

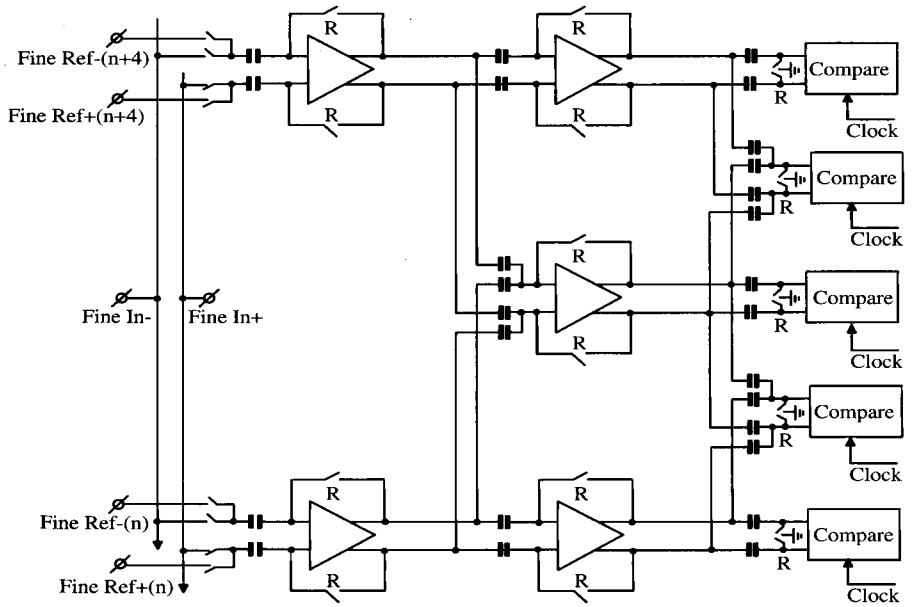


Figure 3.42: Fine converter stage [116]

amplifier stage increases the number of comparator levels without increasing the number of reference taps. The 41 comparators in the second stage use 10 taps on the ladder. Furthermore the multiplexer function is reduced in this way resulting in a smaller capacitive loading of the reference ladder. An

improved performance is obtained at a lower power consumption.

3.12.10 10-bit converter data

The 10-bit converter data are shown in table 3.7. This table shows that a very good ENOB performance for this converter is obtained. Linearity depends on the matching performance of the resistor ladder and the offset of the fine converter stage. A good offset compensation is obtained. The sample-and-hold amplifier at the input shows furthermore an excellent performance. Performance of this system will increase at the moment a more advanced technology will be used.

Technology	0.5 μ Standard CMOS
Resolution	10 Bit
Sample Frequency	30 MHz
Supply Voltage	5 V Analog
Power Dissipation	120 mW
Analog Input Range	1.75 Vpp
SNDR	60 dB
SNR	60 dB
THD	-74 DB
ENOB (f_{in} = 1 MHz)	9.7
SFDR (f_{in} = 1 MHz)	77 dB
Integral Non-Linearity (INL)	$\pm$0.4 LSB
Differential Non-Linearity (DNL)	$\pm$0.45 LSB

Table 3.7: 10-bit converter specification [116]

3.13 Pipeline converter architecture

The general architecture of a pipeline converter is shown in Fig. 3.43. A pipeline converter consists of a cascade of identical stages that are separated by a sample-and-hold amplifier. This sample-and-hold amplifier is part of the sub-converter stage. Mostly the converter is preceeded by a sample-and-hold amplifier. As can be seen from Fig. 3.43 in the lower part a converter stage consists of the already mentioned sample-and-hold amplifier followed by a p-bit analog-to-digital sub converter. This A/D converter drives directly a p-bit digital-to-analog converter to reconstruct the quantized analog

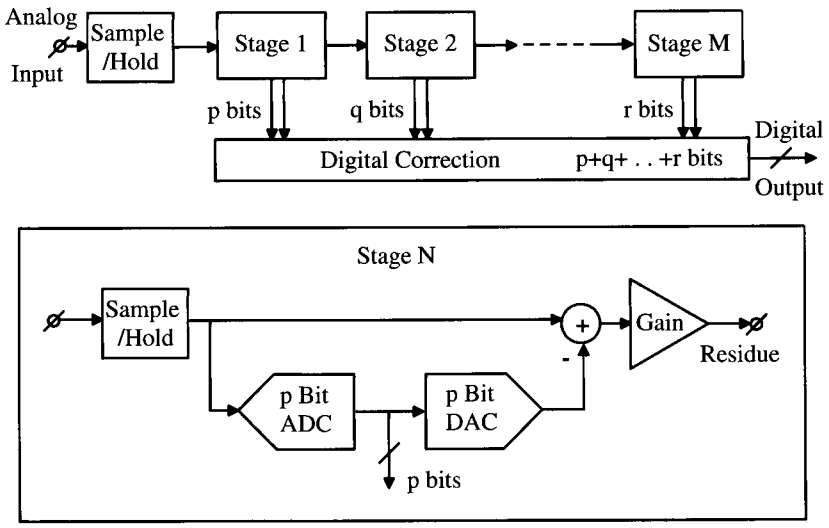


Figure 3.43: Pipeline converter architecture

signal. This quantized analog signal is subtracted from the sampled analog input signal of the stage. After subtraction of the quantized signal from the analog input signal this residue is amplified by the gain stage and then applied to the following sub-converter stage. By pipelining in the converter an optimization can be obtained between maximum sampling clock and the speed of the circuits used. In the first stage the maximum accuracy is required. This accuracy depends on the resolution the converter is designed for. After the first stage a reduced accuracy can be applied without influencing the overall converter accuracy too much. What architecture and what resolution is used per stage depends on the overall resolution that is required and what a designer thinks he can achieve. In this chapter different architectures will be discussed. Numerous pipeline designs are known in literature.

3.13.1 Single bit per stage sub-converter architecture

Starting with a single bit per stage architecture, the problems with this system will be described. In Fig. 3.44 the implementation of a sub-system is shown. In case a 1-bit implementation is used, then the analog-to-digital converter reduces into a zero crossing comparator. This comparator drives a switch that connects $+V_R$, or $-V_R$ to the switched capacitor subtracter/sample-and-hold amplifier. During the sampling mode of the in-

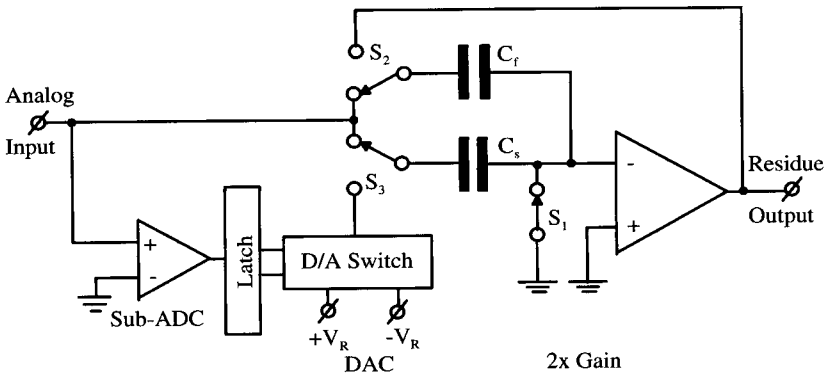


Figure 3.44: Single bit sub-system implementation

put information, switch S_1 is closed and switches S_2 and S_3 connect the analog input signal to the sample/hold capacitors C_s and C_f. The analog input information is stored on these capacitors. Then during the subtraction mode, switch S_1 is opened and switch S_2 connects the capacitor C_2 between the input and the output of the amplifier. Switch S_3 is connected to the digital-to-analog converter consisting of a switch connecting $+V_R$ or $-V_R$ to the capacitor C_s. During this operation the reference voltage V_R is subtracted or added to the analog input signal. At the output the residue is calculated and held in the capacitor C_f for further action. Because the input signal is already sampled on the capacitor C_f during sampling mode, the output signal becomes:

$$V_{residue} = (1 + \frac{C_s}{C_f})V_{input} + D * V_R \tag{3.11}$$

Here D is the decision of the single bit A/D converter and has a value ± 1. In case we choose $C_s = C_f$ then a gain of 2 is obtained. The matching accuracy between the two capacitors determines the gain accuracy, but because the input signal is already sampled on the feedback capacitor C_f with a 1 % capacitor matching a gain accuracy of 0.5 % is already obtained. The residue as a function of the analog input signal V_{in} is shown in Fig. 3.45. This figure shows that with ideal elements and an ideal gain of 2, no problem exists during the operation of the pipeline converter. However, in case offset is present or the gain is larger than 2, the following stages at that moment can not convert this signal and correct for the error. Therefore an over range in the system is needed as has been shown already during the description of the sub ranging converters. The number of bits in the sub-system is increased to

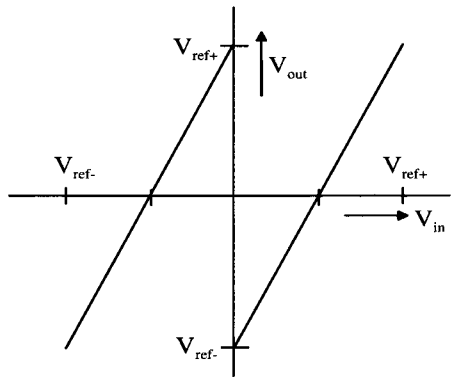


Figure 3.45: 1-bit residue signal

be able to compensate for errors due to offset and gain. The implementation of this sub-system is shown in Fig. 3.46. This system uses a 2 level analog-

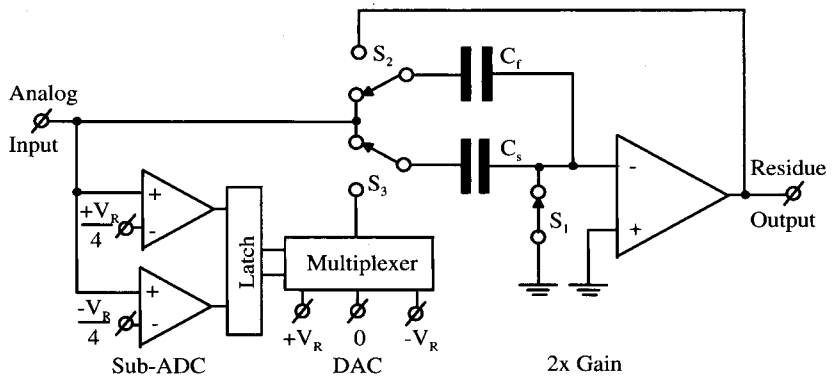


Figure 3.46: 1.5-bit sub-system implementation [119]

to-digital converter with reference levels $+\frac{V_r}{4}$ and $-\frac{V_R}{4}$. The digital-to-analog converter consists of a three level multiplexer with reference voltages $+V_R$ 0 and $-V_R$. During the signal sampling mode switch S_1 is closed and switches S_2 and S_3 sample the input signal on the capacitors C_s and C_f. Depending on the data from the analog-to-digital converter the following operation is performed by this sub-circuit:

$$v_{residue} = \begin{cases} (1 + \frac{C_s}{C_f})V_{input} - V_R, & if\ V_{input} > \frac{V_R}{4} \\ (1 + \frac{C_s}{C_f})V_{input}, & if\ -\frac{V_R}{4} < V_{input} < \frac{V_R}{4} \end{cases} \tag{3.12}$$

$$(1 + \frac{C_s}{C_f})V_{input} + V_R, \quad if\ V_{input} > -\frac{V_R}{4}.$$

During the subtraction/amplify mode the switch S_1 is opened and the capacitor C_f is connected as a feedback element over the amplifier, while capacitor C_s is connected to the digital-to-analog converter that performs the earlier described reference operation. The capacitors C_s and C_f are again equal giving the maximum accuracy for the 2x gain stage. It must be noted furthermore, that during the subtraction/amplify mode of a sub-system, the directly following sub-system is in the sampling mode. This means that during sampling the amplifier is not used. Some systems multiplex the amplifier to reduce die size and power consumption. The residue output signal in this system as a function of the input voltage is shown in Fig. 3.47. The 2-level

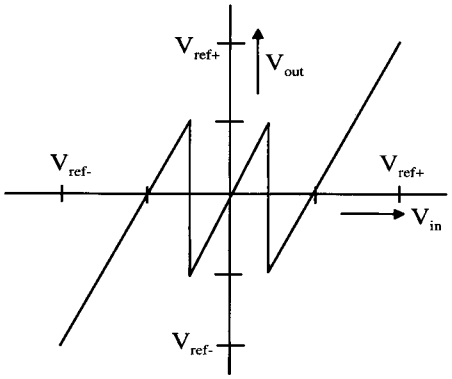


Figure 3.47: 1.5-bit residue signal

analog-to-digital converter in this system enables correction of signal errors due to not exact gain setting, offset and switch charge transfer. A system implementation is shown in [119]. The performance of this system is given in the following table. The converter in [119] is an interesting example as a pipeline converter implementation using 1.5 bit per stage.

3.13.2 Multi-bit pipeline converter

Converters with resolution of 12-bits and more use mostly at the first subsystem stage a multi-bit quantizer with multi-bit digital-to-analog converter. Then the system is completed using 1.5 bit per stage sub-systems. The operation of the multi-bit sub-system is shown in Fig. 3.48. This subsystem is shown in the sampling mode 3.48(a) and the amplification mode 3.48(b) to ease the explanation. The multi-bit digital-to-analog converter

Technology	0.6 μ Standard CMOS
Resolution	10 Bit
Sample Frequency	14.3 MHz
Supply Voltage	1.5 V Analog
Power Dissipation	36 mW
Analog Input Range	± 800 mV differential
SNDR	58.5 dB
Integral Non-Linearity (INL)	±0.7 LSB
Differential Non-Linearity (DNL)	±0.5 LSB

Table 3.8: 10-bit pipeline converter specification [119]

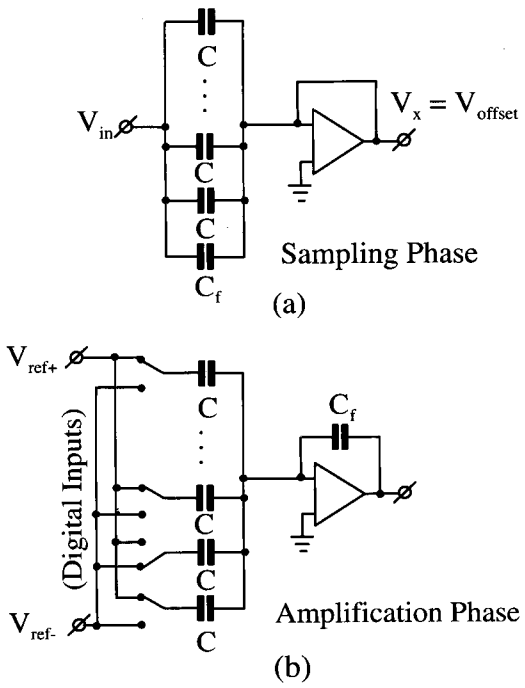


Figure 3.48: Multi-bit system operation [120]

consists of equal capacitors C to obtain the maximum accuracy in the system The feedback capacitor C_f is made equal to the DAC capacitor to maximize the gain accuracy of this system. During the sampling mode the input signal is stored on all capacitors C of the DAC and the feedback capacitor C_f. During the subtraction/amplification mode the residue is calculated using the input information to the DAC from the multilevel analog-to-digital converter. Depending on the value of the bits a subtraction or addition with V_{ref} or with -V_{ref} is performed. The residue signal of this multi-bit operation is shown in Fig. 3.49. The multi-bit operation allows correction of errors

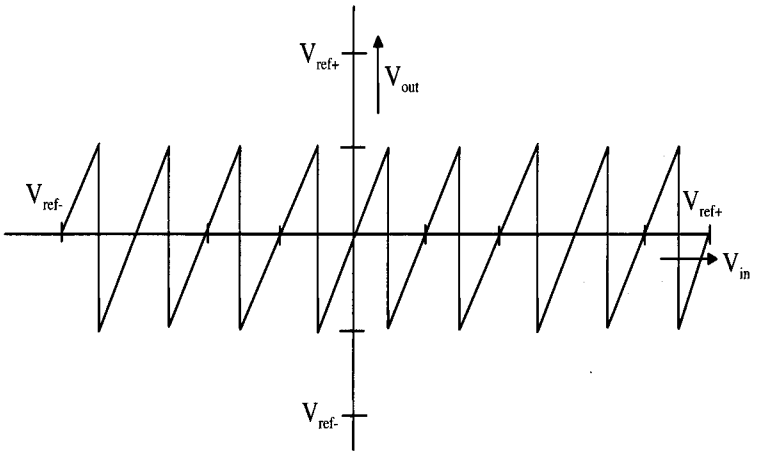


Figure 3.49: Multi-bit residue signal

caused by gain mismatches, offset and switch charge feed through. Multi-bit systems mostly use a 4-bit or 5-bit resolution. After this multi-bit operation the standard 1.5-bit per stage cascaded pipeline converter is used. Trimming of gain might be needed. An example of a multi-bit pipeline converter is shown in [120].

3.13.3 Sharing amplifiers in pipeline converters

To reduce power and die size the amplifiers in a pipelined converter can be shared between two succeeding stages. Because a sample phase is working independent of a comparison/residue subtraction cycle the amplifiers can be shared. During the sampling phase no amplifier is used in the system. In Fig. 3.50 the system architecture of the sharing of amplifiers is shown [122]. Amplifier sharing is obtained by introducing multiplexer switches in the system architecture. Switches indicated with (1) are used during the

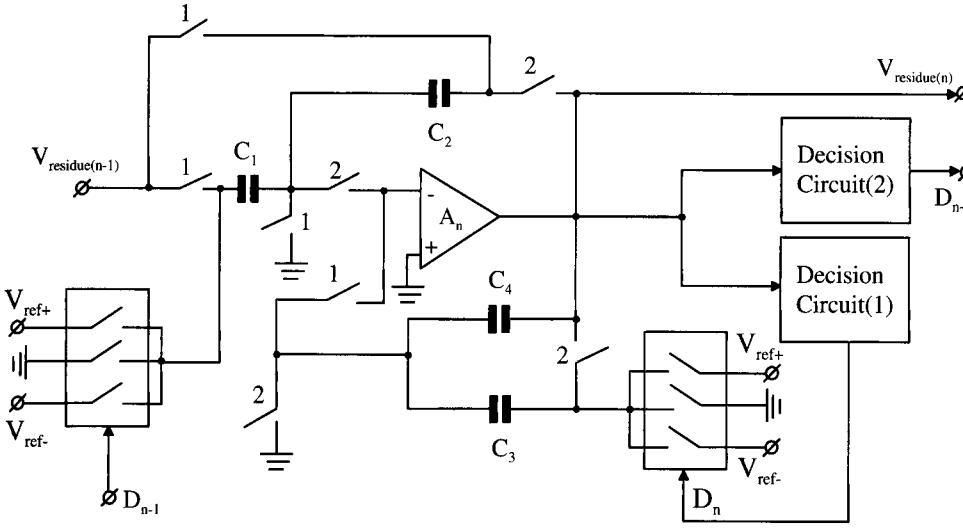


Figure 3.50: Sharing of amplifiers in pipeline converters [122]

sampling of the residue from the previous amplifier in the stage. At the same time the residue is calculated using the amplifier and the result is applied to decision circuit (2). During phase (2) the residue is calculated using the same amplifier and the result is applied to decision circuit (1). The details of the two operations are shown in Fig.3.51 and Fig. 3.52. The residue from the previous stage is sampled on capacitors C_1 and C_2. At the same time the residue is calculated using capacitors C_3 and C_4. The result of the previous decision stored in the decision circuit (1) is used to perform a reference signal operation (addition, subtraction or multiplication). The output signal of this reference operation is applied to decision circuit (2) to perform the next operation in the pipeline conversion architecture. During the second operation with the amplifier, the input residue sampled on capacitor C_1 and C_2 is combined with a reference signal operation. The required reference signal operation is determined by the previous decision D_{n-1} during the previous clock cycle. The residue is now sampled on the capacitors C_3 and C_4 and this information will be used during the next clock cycle. The advantage of sharing amplifiers results in a reduction of power consumption. A good performance with a small die size can be obtained using this architecture.

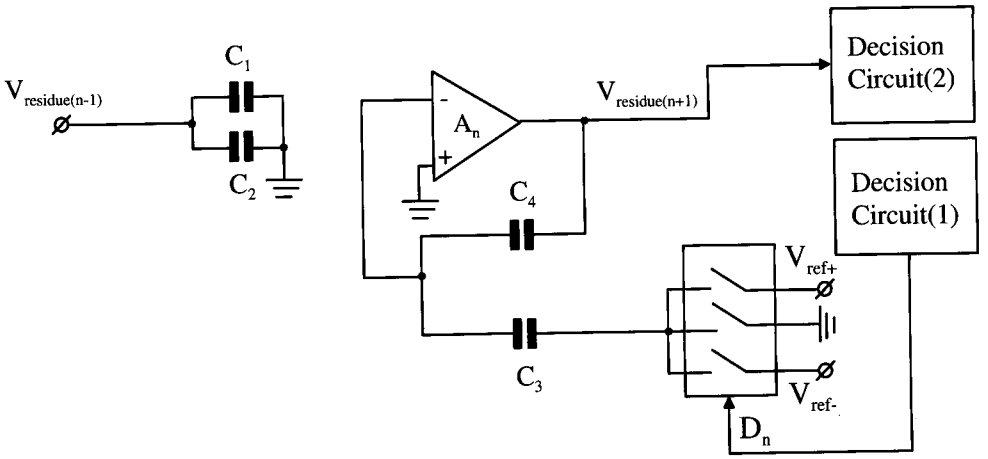


Figure 3.51: Sampling and residue calculation in pipeline converter [122]

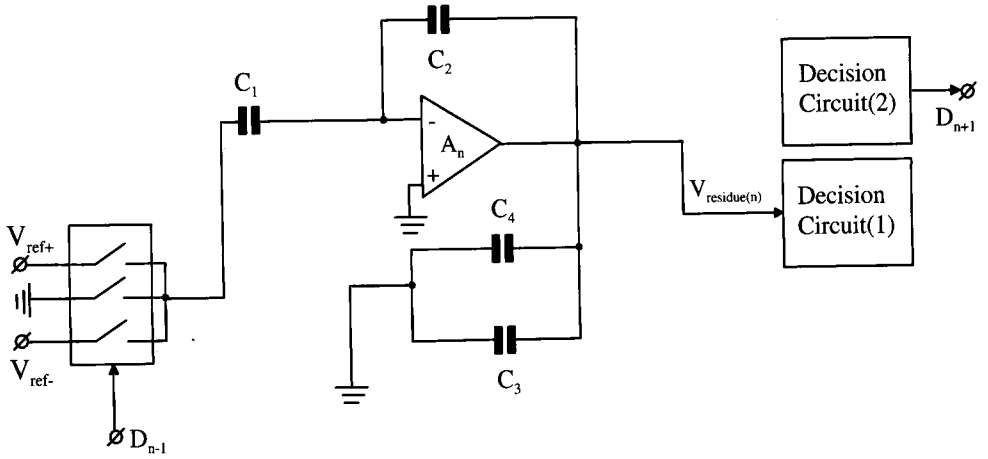


Figure 3.52: Reference signal operation [122]

3.14 Folding converter system

The architecture of a folding analog-to-digital converter system is shown in Fig. 3.53. In a folding analog-to-digital converter the advantages of the

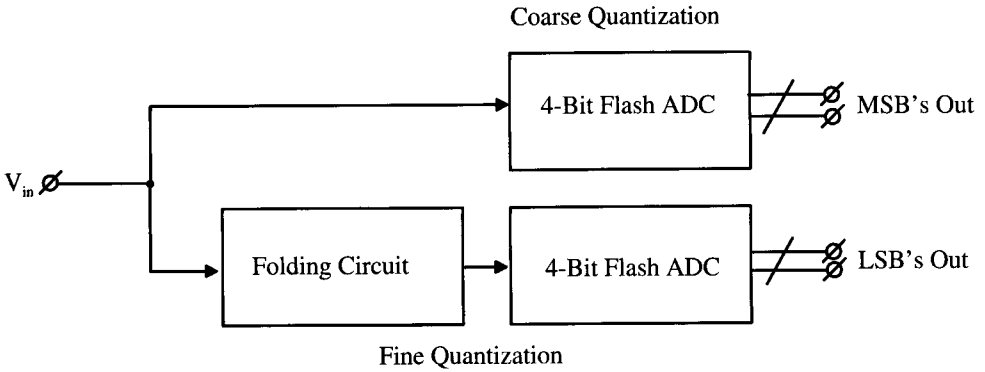


Figure 3.53: Folding converter system

digital sampling of signals used in a full-flash system are combined with the component savings architecture of the two-step system. No sample-and-hold is required in this system [49, 51, 52]. The architecture uses analog preprocessing to transform the input signal into a repetitive output signal to be applied to the fine converter (see Figure 3.53). In this system the most significant bits are determined by the coarse quantizer, which determines the number of times a signal is folded. The fine bits are determined by the fine quantizer which converts the preprocessed "folded" signal into the fine code. In this way it is possible to obtain an 8-bit resolution with only 30 comparators (4-bit coarse plus 4-bit fine). Sampling of the analog signal at the same clock edge does not require the need for a sample-and-hold amplifier. The low component count results in a small die area, while more power can be spent into the system to extend the bandwidth of the comparator and folding stages resulting in a higher sampling speed and a larger analog input bandwidth. On the other hand a reduction in power can be obtained when sampling rate and analog input bandwidth are fixed. One drawback, however, is the higher repetition rate of the folded input signals that can result in rounding-off the tips of the folded signal. This rounding problem can result in a loss of resolution at the high-frequency end of the input spectrum when amplitude quantization is used in the conversion process. The moment a sample-and-hold amplifier is added to the system, the rounding problem is eliminated and the only speed limitation is the settling time of

the system.

3.14.1 Current-folding A/D converter system

A simple example of a circuit implementation of a 4-level (2-bit) folding circuit is shown in Figure 3.54. The most important parts are the reference

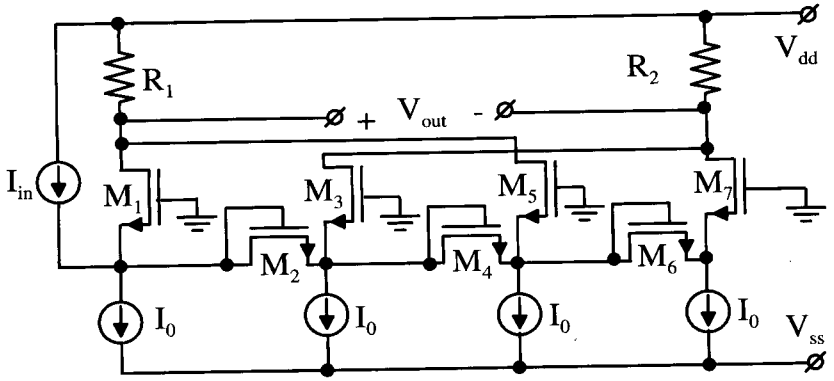


Figure 3.54: Current-folding 2-bit A/D converter structure

current sources I_0, the common-gate transistor stages M_1, M_3, M_5, and M_7, and the MOS diodes M_2, M_4, and M_6. The input signal current I_{in} is compared with the four reference currents I_0. The drains of the odd-numbered transistors of the common-gate stages M_1 and M_5 are connected and so are the drains of the other transistors M_3 and M_7. If the input current I_{in} is equal to zero, then through all common-gate transistors a current I_0 will flow. This results in a current $2I_0$ flowing through each of the load resistors R_1 and R_2. With equal-valued resistors ($R_1 = R_2 = R$), the differential output voltage V_{out} will be zero. If an input signal current I_{in} is applied, for example, $1\frac{1}{2}I_0$, then this current is subtracted from the reference current flowing through M_1. The difference in current, being $\frac{1}{2}I_0$, will forward-bias the diode M_2 and will be subtracted from the reference current I_0 flowing through M_3. As a result, the current through R_1 is reduced to I_0 and the current through R_2 is reduced to $1\frac{1}{2}I_0$. In Figure 3.55(a) the input signal changing from 0 to $4I$ and the corresponding output signal of the folding stage (3.55(b)) as a function of time are shown, respectively. The result of the operation is an output signal with a frequency that is a multiple of the input frequency. In this particular case with a full-scale input signal the output frequency is four times higher than the input frequency. Moreover, the output amplitude is reduced from $4I_0$ into a four

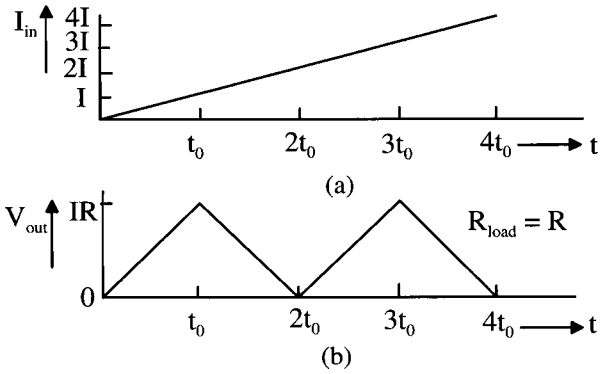


Figure 3.55: Input and output signal as a function of time

times repetition of I_0. The output signal of the circuit can be applied to a following quantizer which may consist of a flash A/D converter. The digital output signals of the coarse quantizer are determined by the conduction or non-conduction of the coupling diodes M_2, M_4, or M_6. The voltage excursion at the input of the circuit is equal to the voltage across the number of conducting diodes. In the example given in Figure 3.54 the maximum voltage excursion will be between zero and $3V_D$. With V_D being the voltage across a single MOS diode. When for an increasing resolution of this system the number of reference sources is increased, the voltage excursion at the input increases and may exceed the maximum gate-source voltage of the process used. The diode switching quantizes the input signal with a very high accuracy. The overall conversion accuracy is thus determined by the accuracy of the reference current sources I_0.

3.14.2 7-bit current folding implementation

The architecture of a 7-bit current folding converter is shown in Fig. 3.56. In this architecture a 3-bit current folding stage is used that determines the most significant bits (MSB's) of the converter. The folded signal is applied to a differential flash converter that determines the least significant bits (LSB's). In this fine converter a Gray encoding is used to minimize the amount of hardware.

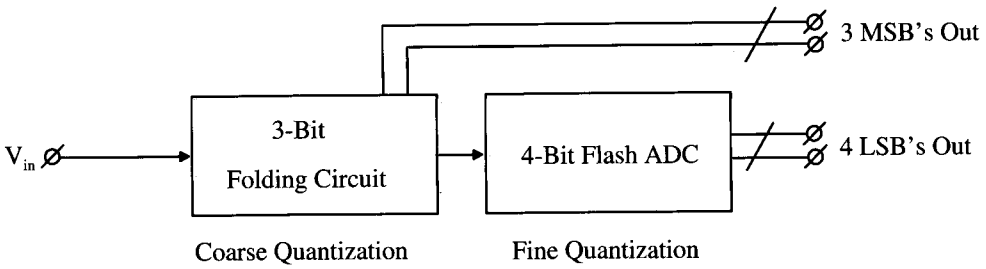


Figure 3.56: 7-bit current folding architecture

3.14.3 Improved current folding system

The improved current folding system that uses MOS diodes with small on voltages is shown in Fig. 3.57 The MOS diodes M_2, M_4 and M_6 have a

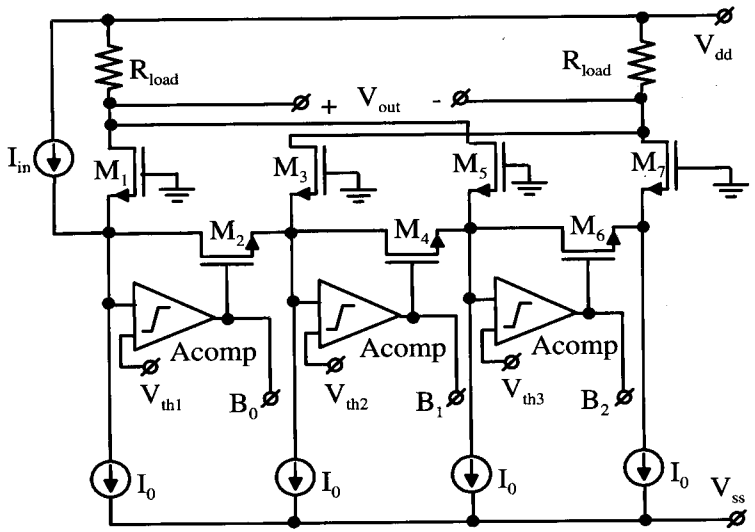


Figure 3.57: Improved current folding system

reduced ON voltage. The amplifiers A_{comp} reduce this ON voltage into the mV range with respect to the applied threshold voltages V_{th1}, V_{th2} and V_{th3}. The amplifiers A_{comp} switch on transistors M_2, M_4 and M_6. These transistors are operating in the linear range and therefore show a low resistance. The voltage drop across these diodes is small compared to the MOS diode voltage. More stages can be cascaded in this way. In the 3-bit coarse system 8 reference sources are used to obtain the required resolution including some

over range. The threshold voltages applied to the amplifiers are needed to avoid switching on due to some mismatch between the common gate transistors. A hysteresis is obtained. The output signals of the amplifiers A_{comp} give directly the coarse information data to be latched into the output buffer stages.

3.14.4 Fine converter system

The circuit diagram of the fine converter system is shown in Fig. 3.58. This fine converter stage has a differential input. The reference voltage is

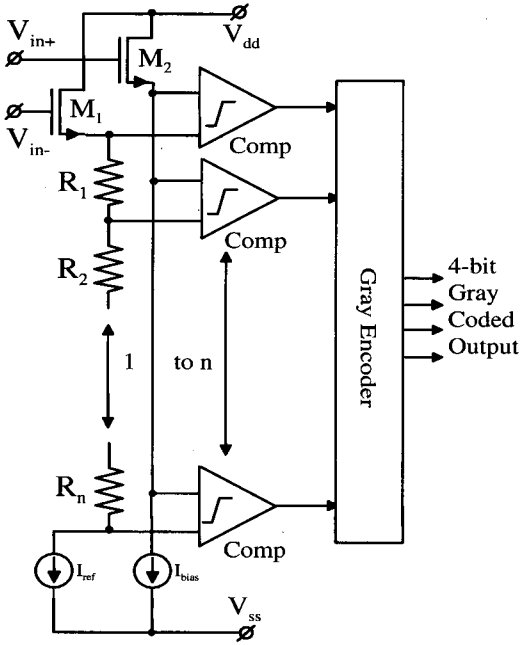


Figure 3.58: Fine converter system

generated with the reference current source I_{ref} across the ladder resistors $R_1, \ldots R_n$. The output of the comparators uses the Gray code. This means that in the encoder comparator signals are combined and then latched to give the fine output code (see Gray code converter in this chapter). It might be clear, that the reference ladder can be split-up into two equal parts loading transistor M_1 and transistor M_2. In this manner a better high-frequency operation is obtained. The bias current source I_{bias} must be replaced by an appropriate reference current source.

3.14.5 High-frequency rounding problem

The folding circuit from Fig. 3.57 applies at low frequencies a triangular wave signal to the fine converter. When frequencies increase, the output capacitance of the circuit together with the load resistor R_{load} limits the bandwidth of this stage. That means that at high frequencies a rounding of the output signal occurs. In Fig. 3.59 this rounding effect is shown. As can be seen from this figure, at low frequencies the complete triangular

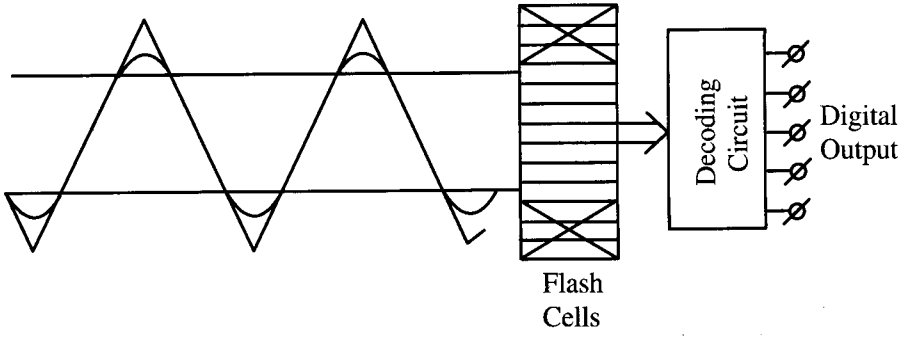


Figure 3.59: High-frequency rounding problem

wave is coded into the digital fine output signal. At high input frequencies, the rounding due to limited signal bandwidth is found and a sine wave like output signal is generated. This signal does not trip the comparators close to the bottom part and top part of the fine converter. As a result missing codes are found resulting in distortion.

3.14.6 Double folding system

To overcome the problem with high-frequency rounding a double folding system can be designed. In Fig. 3.60 a circuit diagram of a double folding system is shown. This system consists of two sets of cross-coupled differential pairs that are connected to a reference ladder. The reference taps for the section with output terminals $FineAD_1$ are in between of the reference ladder connection of the second section $FinAD_2$. As a result with a linear increasing input signal, the folded output signals at the output terminals seem to have a phase shift of 90^0. This virtual phase shift results from the time difference between which the different reference levels are tripped. In Fig. 3.61 the output signals of this double folding stage are shown. The idea behind this solution is, that the input amplifiers are only used during the linear part of the transfer function. At the moment the differential pair

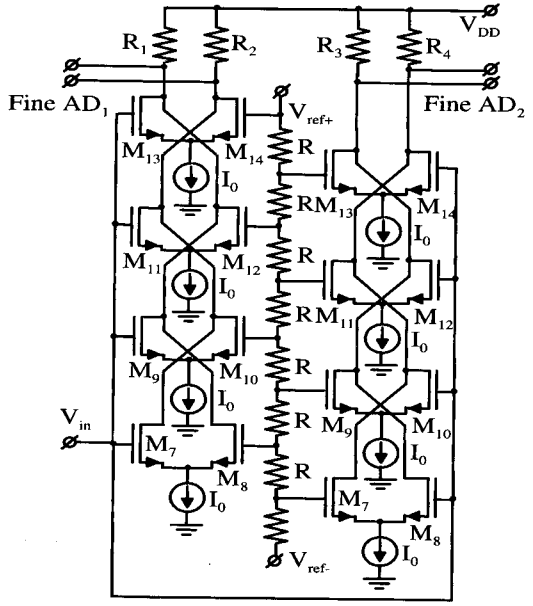


Figure 3.60: Double folding system

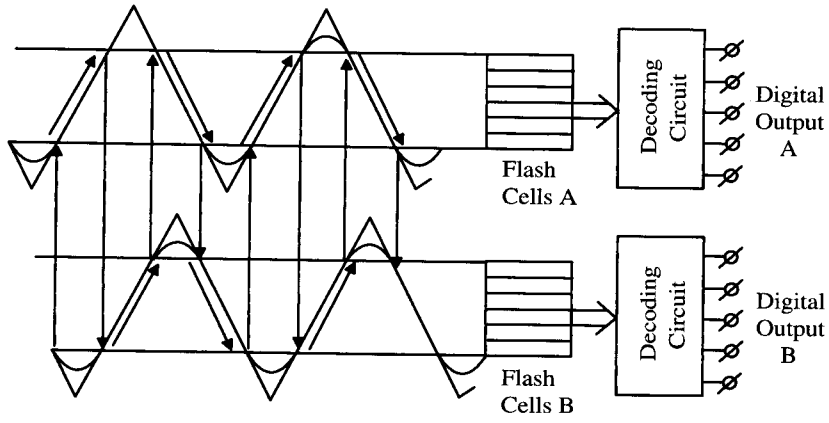


Figure 3.61: Double folding output signals

starts to deviate from the linear transfer, the signal switches from input pair A to input pair B. This is shown in Fig. 3.61. The arrows indicate that the fine system switches between flash A and flash B. During the linear transfer part the fine conversion takes place. The full resolution is obtained, although a rounding might occur at high frequencies. Furthermore no more comparators are needed than in the case of an ideal system.

3.14.7 8-bit folding and interpolation converter

The architecture of a 8-bit folding and interpolation converter is shown in Fig. 3.62. The input system consists of a parallel connection of 4 folding

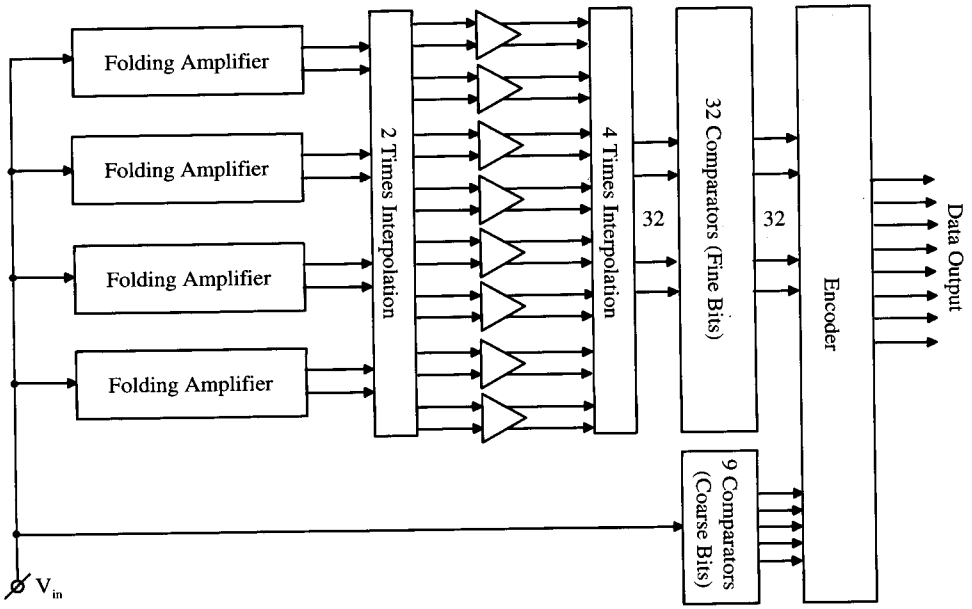


Figure 3.62: 8-bit folding and interpolation architecture [128]

amplifiers consisting of 8 cross-coupled differential pairs. These input stages are followed by a 2 times interpolation stage with an amplifier stage. After this amplifier stage a 4 times interpolation is applied so finally 32 comparators form the fine conversion stage. From the input reference ladder 9 comparators are used to determine the most significant bits (MSB's), so a digital output of 8-bits is obtained. The construction of the input folding amplifiers is shown in Fig. 3.63. In the folding amplifiers 8 cross-coupled differential amplifiers with tail current sources I_1 . . I_8 are used. Because of the cross-coupling in the differential amplifiers about 4 tail currents are

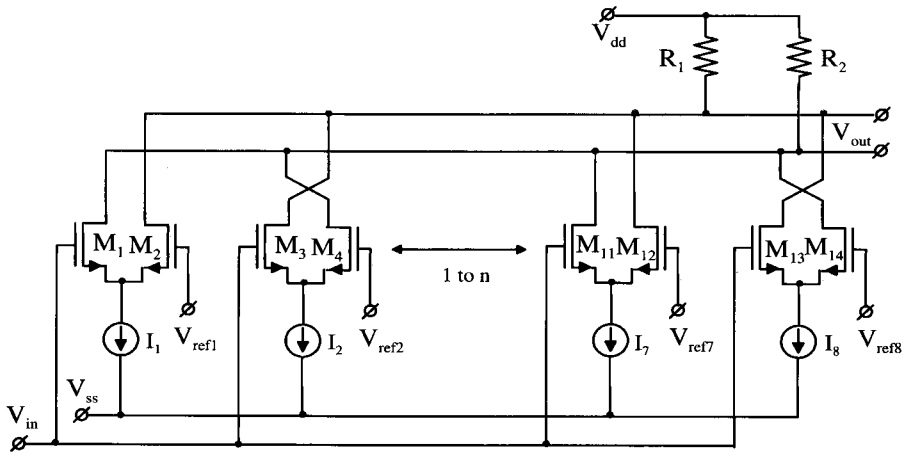


Figure 3.63: Input folding amplifier system

switched to the load resistor R_1 and the other 4 are switched to R_2. This means that depending on the input signal level with respect to the reference level the currents switched to the load resistors change. In case these resistors do not match very well, then except from the signal information from the input an extra error is introduced due to the variation of the tail currents. This variation causes a non-linearity. A current value of $4I_{tail}$ ($I_{tail} = I_1, ..I_8$) can be seen as common mode current and the signal current of one differential pair performing reference comparison is the real signal current. In case an even number of stages is used, then an extra current must be added to load resistor R_1 or an extra differential pair can be added to obtain the odd number of stages needed for a good folding operation. Mostly an extra differential pair is used. At high-frequencies a bandwidth problem occurs due to the large output capacitance of the devices. In the practical solution an input transistor size of 100 $\mu/1\mu$ is used.

3.14.8 Transimpedance amplifier

To overcome the frequency limitation problem a transimpedance amplifier is used. This system is shown in Fig. 3.64. The output time constant with the load resistor R becomes:

$$\tau = RC_{parasitic}. \tag{3.13}$$

This time constant is too large in high-frequency applications. Therefore an extra amplifier is used. This amplifier has the load resistor R in the

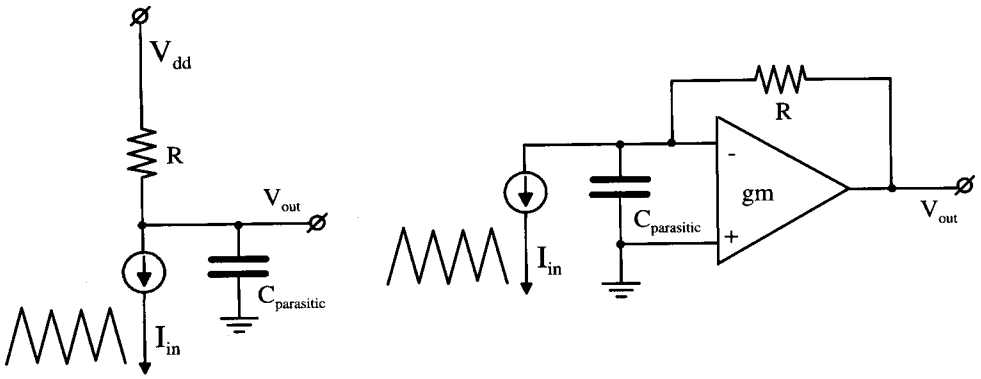


Figure 3.64: Transimpedance folding amplifier system [128]

feedback loop. As a result of this amplifier, the voltage across the parasitic capacitance is reduced, resulting in a much larger bandwidth. In this case the time constant becomes:

$$\tau = \frac{C_{parasitic}}{g_m}. \tag{3.14}$$

In this application we have:

$$\frac{1}{g_m} \ll R. \tag{3.15}$$

This means that the bandwidth of the system increases a lot.

3.14.9 Transimpedance amplifier circuit diagram

The circuit diagram of the transimpedance amplifier is shown in Fig. 3.65. In this amplifier a differential pair is used. The load resistors R_1 and R_2 are used as feedback between the drain and the gate of transistors M_1 and M_2. The gain of the system is determined by the transconductance of these transistors. A proper choice must be made to make g_m large compared to $\frac{1}{R}$. The differential signal flows through the transimpedance resistors and transistors M_1 and M_2 as shown by the arrows. A large transconductance gives a small input gate difference signal resulting in a large system bandwidth. The differential output impedance of this system in a first approximation is:

$$R_{out-differential} = \frac{2}{g_m}. \tag{3.16}$$

This means that when interpolation is used, a certain averaging of signals can be obtained as long as the interpolation resistor is in the range of the output impedance of the amplifiers.

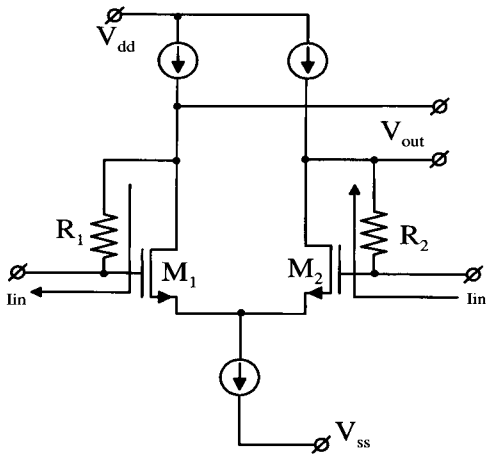


Figure 3.65: Transimpedance amplifier circuit diagram

3.14.10 Resistive interpolation

The used resistive interpolation scheme is shown in Fig. 3.66. At the moment the value of the interpolation resistor R_{int} is a number of times larger than $\frac{1}{g_m}$, then with interpolation averaging is combined. This means that offsets are automatically averaged over the 4 input amplifier folding blocks.

3.14.11 Comparator circuit

The circuit diagram of the comparator used with this converter is shown in Fig. 3.67. The comparator consists of an input differential pair M_1, M_2 loaded with current sources M_3 and M_5. A folded cascode consisting of M_4 and M_6 couples the input information to the comparator stage. This comparator stage consists of a cross-coupled pair M_7 and M_8. Transistor M_9 determines the moment a decision will be taken. At the moment M_9 is shorted, then the comparator stage is in Reset mode. The currents from the folded cascode stage bias transistors M_7 and M_8 so the maximum gain can be achieved. At the moment switch M_9 is opened, then this maximum gain is used to get a decision depending on the input information. At the output of the comparator a slave flip-flop is added to hold the digital output information. Diode connected MOS devices M_{11} and M_{12} limit the maximum output swing of the comparator stage. The following flip-flop stage converts this information into CMOS logic levels. In case a supply voltage of 2.5 V is used, then the diodes limit the output swing preventing the folded cascode

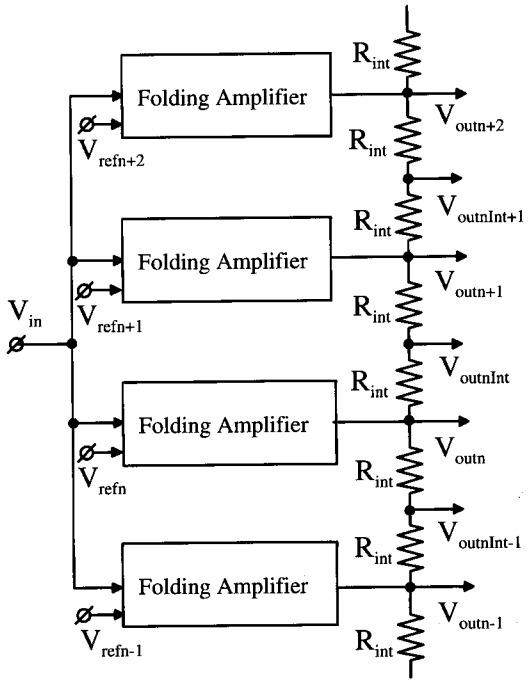


Figure 3.66: Resistive interpolation scheme

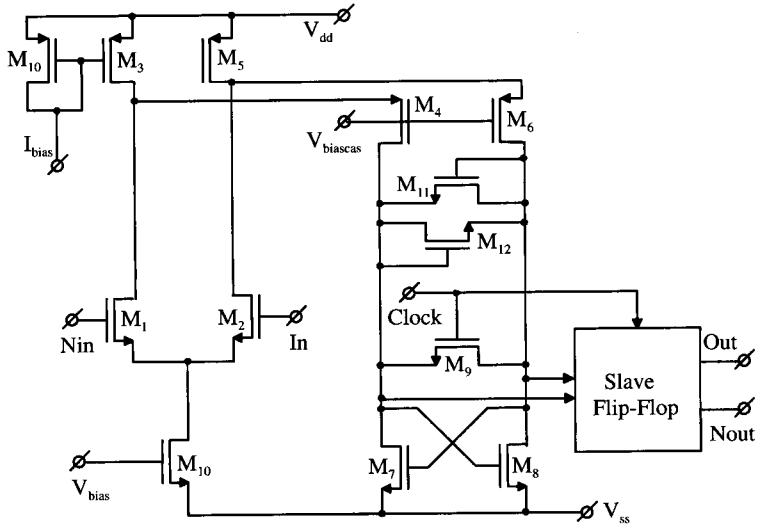


Figure 3.67: Comparator circuit diagram [128]

stage from becoming inactive resulting in a large kickback effect to the input of the comparator stage.

3.14.12 Converter specifications

The specifications of the implemented converter are shown in the following table.

Technology	0.8 μ Standard CMOS Single Poly, Double Metal
Resolution	8 Bit
Effective Number of Bits	7.6 Bit
Resolution Bandwidth	5 MHz
Maximum Clock Frequency	70 MHz
Active Chip Area	0.7 mm^2
Supply Voltage	5 V
Power Dissipation	110 mW
Analog Input Range	2.0 Vpp
Input Capacitance	1 pf
Integral Non-Linearity (INL)	0.5 LSB
Differential Non-Linearity (DNL)	0.2 LSB

Table 3.9: 8-bit converter specification [128]

3.14.13 Distributed S/H folding and interpolation converter

To improve the high-frequency performance of the folding analog-to-digital converter a sample-and-hold amplifier can be put in front of the converter. The architecture then modifies into Fig. 3.68. At the moment the sample-and-hold amplifier is put in front of the converter, then a high-performance system is required. To reduce the requirements of the sample-and-hold amplifier the architecture of the converter system can be modified using a distributed sample-and-hold function. This architecture is shown in Fig. 3.69. After the input preprocessing amplifiers a simple distributed track-and-hold function is implemented. After the preprocessing operation the signals are limited in signal swing, while furthermore the required accuracy is reduced because a number of bits have been already determined and only the fine conversion process needs to be done. In Fig. 3.69 folding signals are combined to obtain the coarse information, while after interpolation the fine conversion

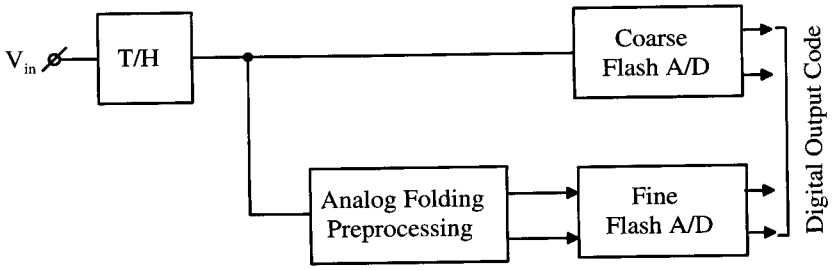


Figure 3.68: Folding converter with T/H input

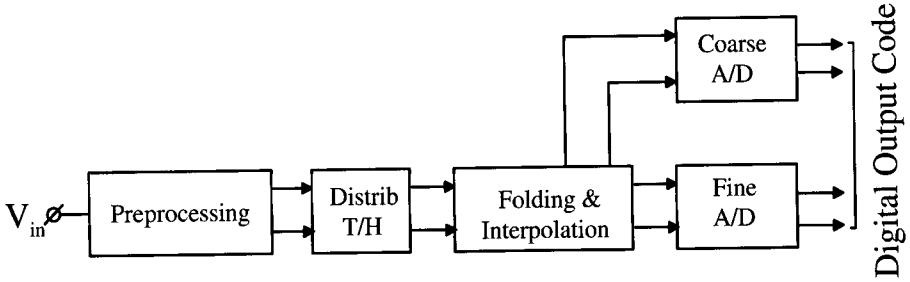


Figure 3.69: Folding converter with distributed T/H function

takes place. In Fig. 3.70 the comparison between an input sample-and-hold amplifier and a distributed track-and-hold function is shown. From Fig.

	Basic T/H:	Distributed T/H:
Linear Region	Entire Input Range	1/16 Input Range
Settling	8-Bit Accuracy	8-Bit Divided by Gain of Input Stage
Power	High-Linearity Buffer	No Additional
Clock Switch	Single	Multiple

= Advantageous

Figure 3.70: Comparison between input S/H and distributed T/H function

3.70 the following information is obtained. With an input sample-and-hold amplifier the full linearity is needed while settling needs to be for the full resolution of the converter. The hold stage needs a high-linearity buffer that drives the converter. Timing uncertainty, however, is determined by only 1 switch. This timing can be good controlled. The distributed track-and-hold amplifiers in the implemented converter have only $\frac{1}{16}$ of the input range when 16 input preprocessing amplifiers are used. This means that the accuracy and the settling requirement are reduced to about 5-bit resolution. Furthermore the distributed T/H function can be easily implemented in the design as will be shown. A disadvantage of the distributed T/H function is that multiple sampling switches must be controlled that can result in timing problems.

3.14.14 Distributed T/H folding and interpolation converter architecture

The architecture of a folding converter using distributed T/H amplifiers is shown in Fig. 3.71. The system consists of input amplifiers with resistive loads followed by simple distributed T/H functions. Coarse preprocessing is performed on the sampled signals by combining the appropriate signals from

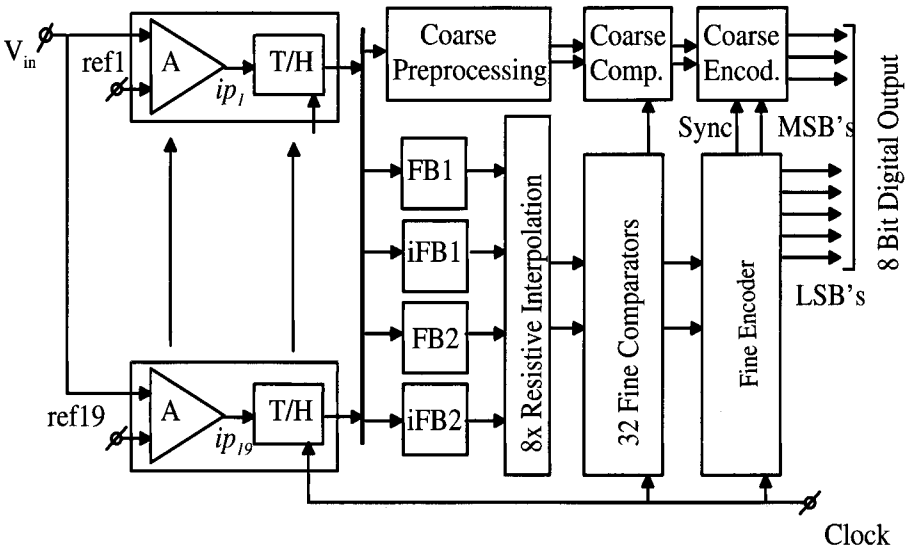


Figure 3.71: Distributed T/H folding converter architecture

the preamplifiers. After comparison the signals are decoded to obtain the coarse information. To prevent timing problems, the coarse information is corrected using the information from the fine converter. The coarse information determines the range of the signal, while the fine converter determines exactly the coarse information. The output signals of the T/H function are applied to the folding blocks. The implementation of these folding blocks uses a cascade of folding triplets that perform a 9 times folding. Via an active interpolation scheme additional folding signals are generated so 4 folding output signals are obtained from the fine folding blocks. These 4 signals are 8 times interpolated to obtain 32 repeating zero crossings. The comparators determine the digital output signal and after fine decoding the full 8-bit output signal is obtained. The timing of the distributed T/H stages is very important to obtain a good high-frequency performance of the converter. Different circuit implementation will be discussed.

3.14.15 Track-and-hold circuit implementation

The circuit implementation of the distributed track-and-hold function is shown in Fig. 3.72. This system consists of the input amplifier M_1 and M_2 that performs the comparison between a reference level V_{ref} and the input

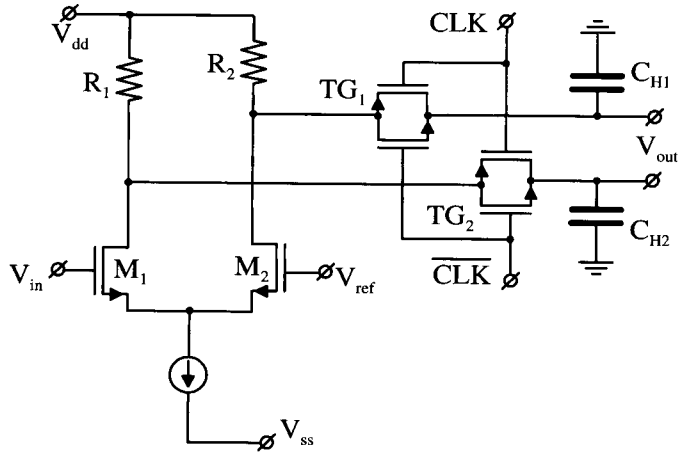


Figure 3.72: Distributed T/H circuit diagram

signal and amplifies this signal across the load resistors R_1 and R_2. Then a set of transmission gates (TG_1 and TG_2) act as sampling switches. The amplified input signal (V_{in} - V_{ref}) is then sampled on the hold capacitors C_{H1} and C_{H2}. The output of the T/H is loaded with the gate impedances of the folding stages. The signal swing at the output of the input amplifier is limited by the tail current source and the load resistors R_1 and R_2. Furthermore around the zero crossing of the amplified signals the levels for all the distributed T/H amplifiers are practically equal. This means that sampling occurs always at the same time moment. With a full input S/H amplifier this is one of the more difficult design issues. Using the distributed function the timing depends only on the layout of the T/H switches. This can be solved well in most cases.

3.14.16 Cascaded folding block architecture

The architecture of the cascaded folding function is shown in Fig. 3.73. In this system 17 input amplifiers are used to obtain 2 sets of 9 times folded output signals. To make the system less dependent on tail current and load resistor matching accuracy a two-step folding operation is used. In the first step three input signals are combined into a single folded output signal. Then three output signals of three input folders are combined to give a single output signal. 4 of these cascaded folding blocks are used to get 4 nine times folded output signals. Furthermore extra input amplifiers at the top and bottom of the reference ladder are added to obtain over

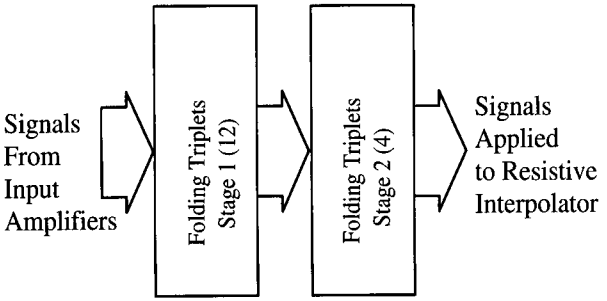


Figure 3.73: Cascaded folding block architecture

and under range information. The operation of the first triple folding block is shown in Fig. 3.74. From this figure we see that signals SR_1, SR_7

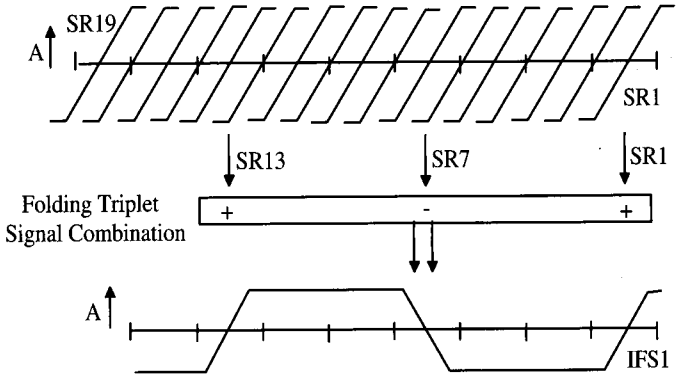


Figure 3.74: First folding block signal diagram

and SR_{13} are combined to give the intermediate 3 times folding output signal. All operations in the folding block are differential so differential output signals are obtained. The operation of the complete folding block is shown in Fig. 3.75. The parallel connection of three triple folding blocks from the first stage into the second folding block stage results in the 9 times folding operation. Signal frequencies in this system increase with a factor 9. This means that the folding stages must have enough bandwidth to settle to the required accuracy. In the practical solution the triple folding block uses an active interpolation to reduce the amount of input amplifiers and the amount of reference ladder taps.

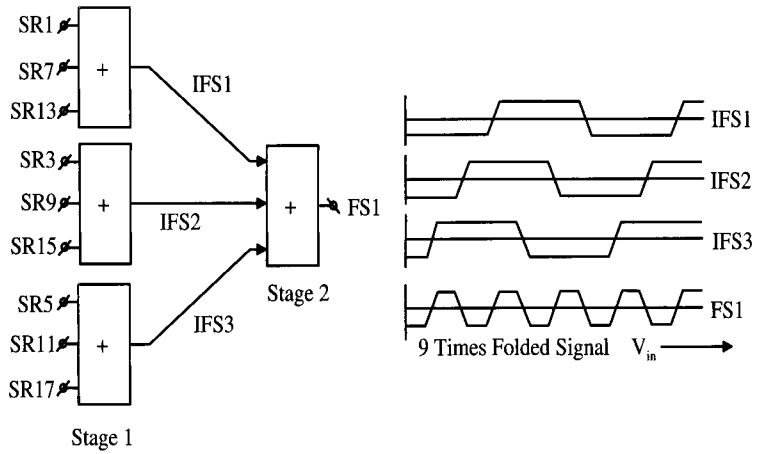


Figure 3.75: Cascaded folding block signal diagram

3.14.17 Triple folding block circuit diagram

The circuit diagram of the triple folding block with active interpolation is shown in Fig. 3.76. The circuit uses three cross-coupled differential stages

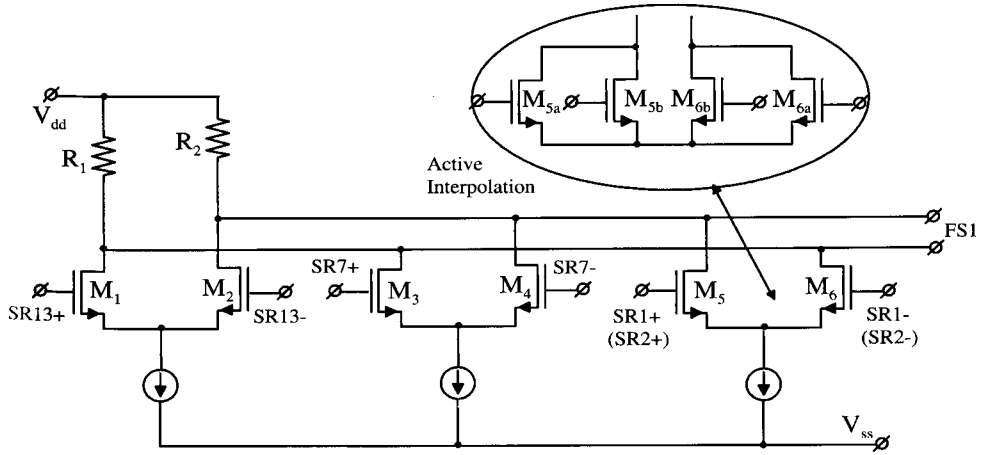


Figure 3.76: Triple block signal diagram

connected to the load resistors R_1 and R_2. However, differential pair M_5 and M_6 consists of two split-up pairs M_{5a}, M_{5b} and M_{6a}, M_{6b}. The gates of these transistors are connected to a reference level and one reference level higher. In this way interpolation between the two reference levels is obtained

and the number of reference levels can be reduced.

3.14.18 Coarse code generation

The block diagram showing the coarse code generation is shown in Fig. 3.77. From this figure it is seen that the most significant bit (MSB) is

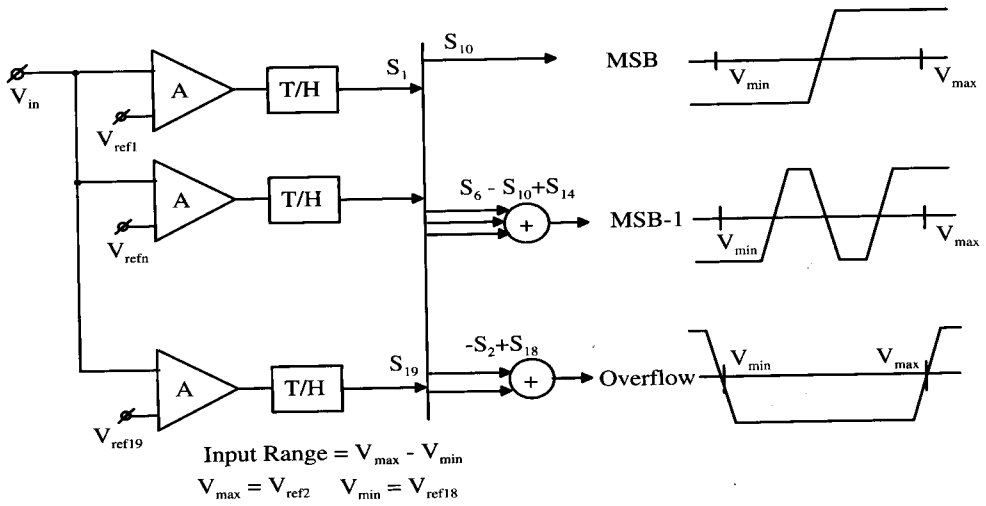


Figure 3.77: Coarse code generation

directly obtained from input amplifier S_{10}. The MSB-1 code is obtained by combining code S_6 with S_{10} and S_{14} in a triplet folding stage. Over and underflow use code S_2 and S_{18}.

3.14.19 Measurements

In Fig. 3.78 the measurements of the DNL and INL at a clock frequency of 80 MHz are shown. The signal-to-noise ratio and the ENOB measurement are shown in Fig. 3.79. The signal-to-noise ratio at 70 MHz is still 44 dB as is shown in the measurement, however, due to the increase in distortion the ENOB is limited to about 12 MHz.

3.14.20 8-bit distributed T/H folding and interpolation converter specifications

The specifications of the implemented folding converter with distributed T/H amplifiers is given in Table 3.10.

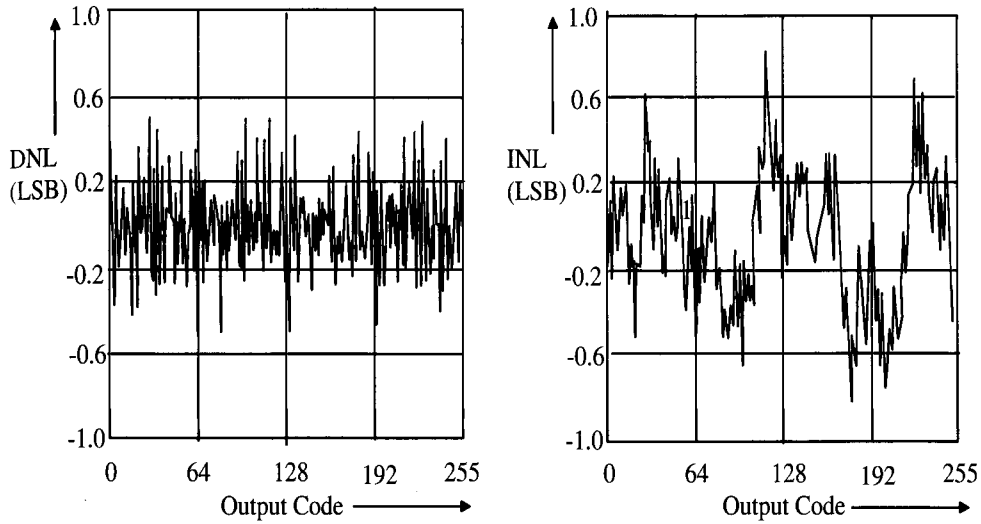


Figure 3.78: DNL and INL measurements

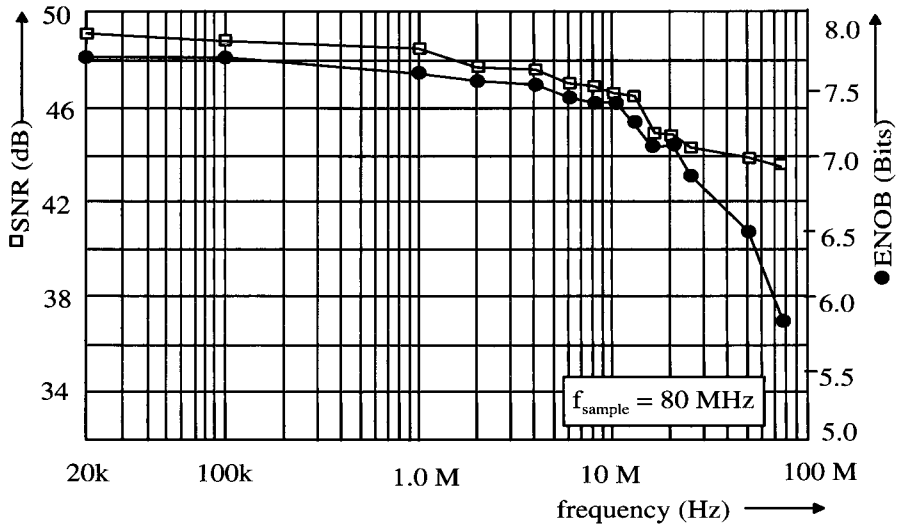


Figure 3.79: SNR and ENOB measurements

Technology	0.5 μ Standard CMOS Single Poly, Triple Metal
Resolution	8 Bit
Effective Number of Bits	7.5 Bit
Resolution Bandwidth	12 MHz
Maximum Clock Frequency	80 MHz
Active Chip Area	0.3 mm^2
Supply Voltage	3.3 V
Power Dissipation	80 mW
Analog Input Range	1.6 Vpp
Input Capacitance	2 pf
Bit Error Rate (BER)	10^{-12}
Integral Non-Linearity (INL)	0.8 LSB
Differential Non-Linearity (DNL)	0.45 LSB

Table 3.10: 8-bit distributed T/H converter specification

3.14.21 10-bit folding and averaging converter

The architecture of a 10-bit folding with averaging and interpolation converter is shown in Fig. 3.80 [126]. The system consists of an input sample-and-hold amplifier with differential inputs, a single reference ladder, input amplifiers with averaging and a 3 times folding followed again by the second amplifier stage with averaging and again 3 times folding, finally the third amplifier stage just uses averaging followed by 128 comparators to determine the fine output code. Parallel to the fine converter stage a coarse converter is used to determine the coarse bits. The output of the architecture is a 10-bit binary weighted digital code. In this architecture an improved averaging is used.

3.14.22 Improved averaging

The circuit diagram of the improved averaging scheme is shown in Fig. 3.34. The differential input stages that compare the analog sampled input signal from the sample-and-hold amplifier with the reference ladder are differential stages with a current source load. This load automatically adjusts for the DC biasing of the input stage. To obtain a strong coupling between the different input stages the current source loading is used. Resistors R_{nav} determine the coupling of stage n with the neighboring stage $n-1$. As long

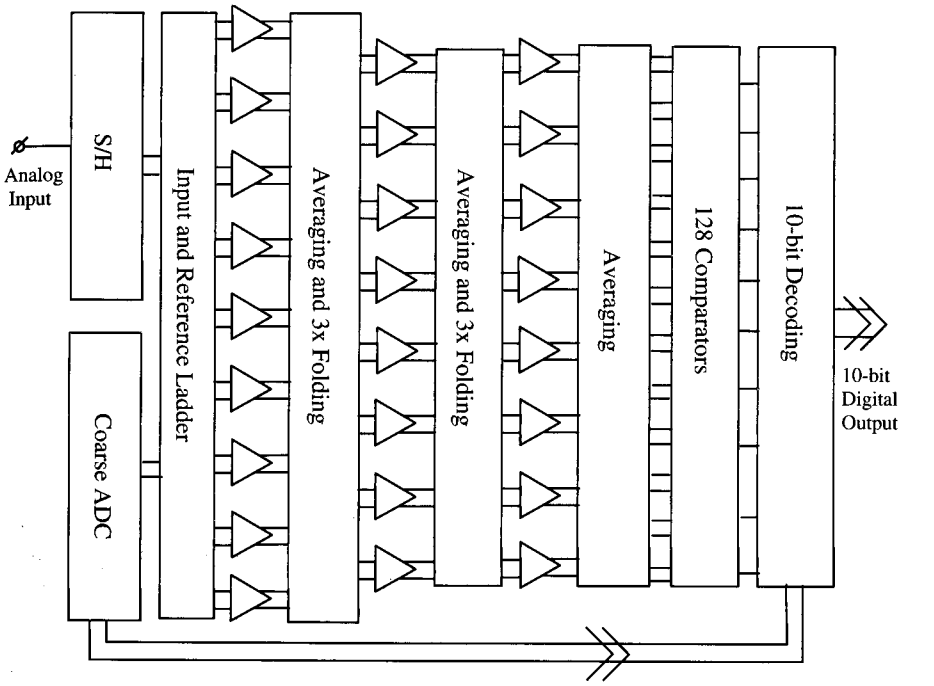


Figure 3.80: 10-bit folding and averaging architecture [126]

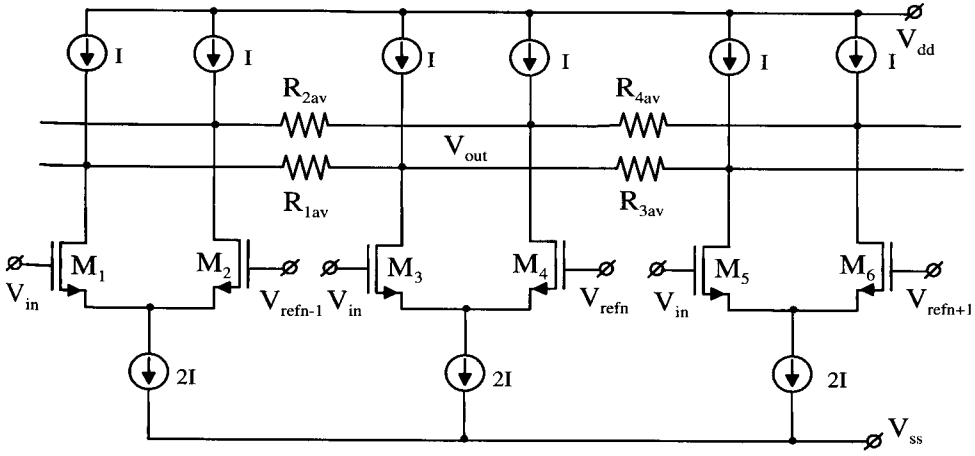


Figure 3.81: improved averaging scheme [126]

as the input stages are in the linear range, then this stage has a positive effect on the zero crossing of the total input amplifier system. The strong coupling between the stages reduces the offset. Furthermore triple folding stages are used to increase the number of repeating zero crossings in the system. An important part of the design is the circuit implementation of the load current sources.

3.14.23 Drain load current sources

The circuit diagram of the current sources loading the input amplifier stages is shown in Fig. 3.82. The current source consists of two cross-coupled

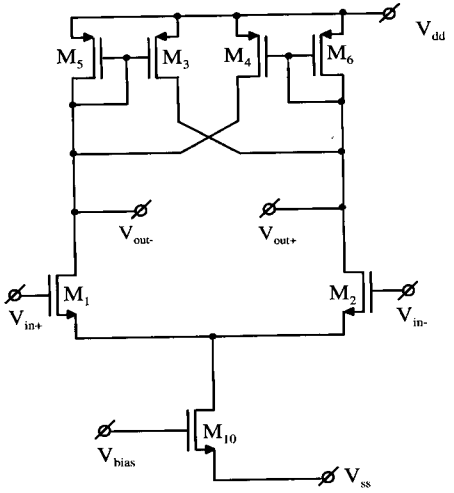


Figure 3.82: Current source circuit diagram [126]

current mirrors M_5, M_3 and M_6, M_4. The loading of the input stage M_1 and M_2 is basically performed by the MOS diodes M_5 and M_6. To increase the impedance of the diodes transistors M_3 and M_4 are added as a current mirror. The drains of these transistors are cross-coupled with respect to the differential output signals. All devices are identical, this means that, when a signal current flows through diode M_5 this current is mirrored by M_3 and then applied to the opposite output of the differential pair. The same occurs for diode M_6 with M_4 as current mirror. The cross coupling basically compensates for the current flowing through the diodes. As a result a high differential output impedance is obtained. In case common mode signals are applied, then the current mirrors act as being all in parallel, reducing the

output load impedance to:

$$R_{out-CM} \approx \frac{1}{2g_m}. \tag{3.17}$$

This can be seen as follows. If a common mode current flows through the diodes, then the same current flows through the mirror transistor. As a result half the input current flows through the diode and the other half flows through the mirror transistor. This results in half the voltage signal is generated across the diode resulting in the lower output impedance for common mode.

3.14.24 Differential converter input system

The construction of the differential input system for the analog-to-digital converter is shown in Fig. 3.83. The system consists of coupled differential

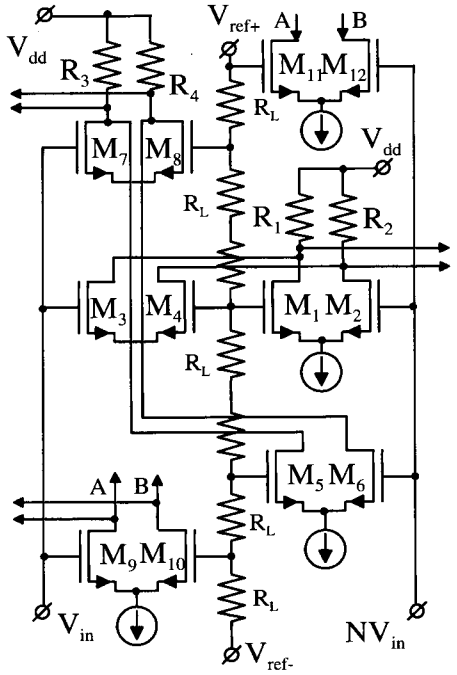


Figure 3.83: Differential converter input stage

stages with a single reference ladder. The differential stages of opposite reference levels are coupled to obtain the required amplified output signal. Differential input signals are normally amplified. However, common mode

signals are amplified too. The amplifiers in this way act as single ended input stages with respect to the reference ladder. Signals with opposite polarity are added so a cancelation of the common mode currents is obtained. This means that the input differential pairs need equal transconductances. This means a good matching of the input devices together with a matching of the tail current sources. Furthermore the common mode signal must be so small that the differential pairs do not operate outside the linear signal range.

3.14.25 Comparator circuit diagram

The circuit diagram of the comparator used in this converter is shown in Fig. 3.84. The comparator consists of the input differential pair M_1, M_2 loaded

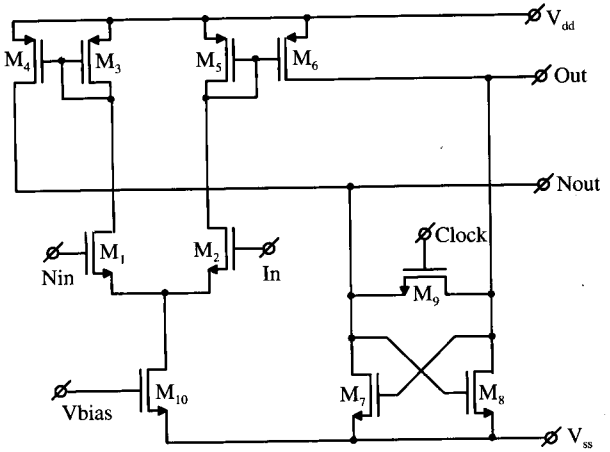


Figure 3.84: Comparator circuit diagram [126]

with current mirrors M_3, M_4 and M_5, M_6. The output current of the current mirrors is applied to the basic comparator stage consisting of the cross-coupled transistors M_7 and M_8. Transistor M_9 driven by the clock signal resets the system when this transistor is switched ON. With nearly equal input voltage to the comparator input stage, equal currents will flow through the drains of the input pair and these currents are mirrored to the output biasing the cross-coupled pair with this current. The maximum gain is obtained in this situation. At the moment transistor M_9 is switched off (open connection) then the cross-coupled stage immediately starts comparing the two input currents. A CMOS digital output level can be obtained with this stage. Because current mirrors are used, switching off transistor M_4 or M_6 does not give a kick-back effect to the input of the comparator stage.

Especially at low supply voltages this circuit configuration is operating very well.

3.14.26 Measurements

The measurement results of the SNDR and the Effective Number of Bits of this converter are shown in Fig. 3.85. At a sample frequency of 32 MHz the

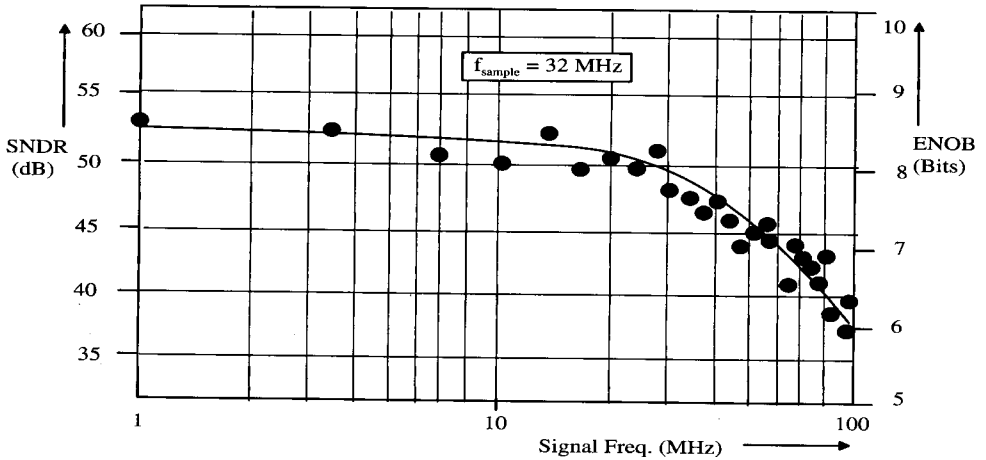


Figure 3.85: SNR and ENOB measurements [126]

low-frequency ENOB is 8.7 bits.

3.14.27 10-bit converter specifications

The specifications of the 10-bit averaging and interpolation converter are given in table 3.11.

3.15 Time interleaved high-speed converters

At the moment very high sampling rates in converters are needed, then it is not possible anymore to obtain these high sampling speeds in a single system architecture. These applications are found in digital oscilloscopes with analog bandwidths between 2 to 6 GHz and sampling rates up to 20 Gs/s. To be able to perform such an operation a multiple of analog-to-digital converters are used in a time interleaved mode. In Fig. 3.86 an architecture using four time interleaved converters is shown [168]. The type of basic converter architecture that has to be used is not important. Time interleaving can be

Technology	0.5 μ Standard CMOS Single Poly, Triple Metal
Resolution	10 Bit
Effective Number of Bits	8.7 Bit
Resolution Bandwidth	32 MHz
Maximum Clock Frequency	150 MHz
Active Chip Area	1.0 mm^2
Supply Voltage	5 V
Power Dissipation	170 mW (ADC) 240 mW (ADC + S/H)
Analog Input Range	2.0 V (differential)
Input Capacitance	4.5 pf (ADC) 1.0 pf (S/H)
Integral Non-Linearity (INL)	1.1 LSB
Differential Non-Linearity (DNL)	0.6 LSB

Table 3.11: 10-bit folding and averaging converter specification [126]

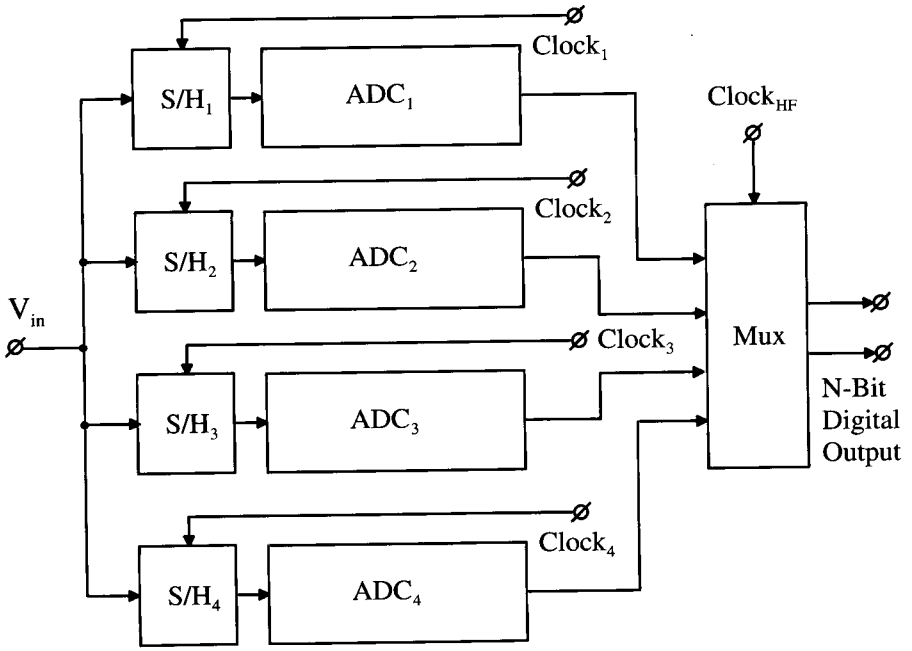


Figure 3.86: Time interleaved A/D converter architecture

applied to all converter architectures described in this chapter. As can be seen from the figure, the architecture contains four converters connected in parallel. These converters have each a sample-and-hold amplifier that has to handle the high performance analog input signals. The sample-and-hold amplifier determines the analog bandwidth of the total system. After sampling the input signal, then during the hold mode this signal is converted by the succeeding analog-to-digital converter into a digital output signal. Each converter uses in this specific example a four times lower sampling frequency then the output digital sample clock of the system. Furthermore the lower speed of each converter in the system improves the performance of the individual converter. Especially the BER of the converters can be improved considerably. With increasing sampling frequency of the individual converter the required BER can not be obtained anymore. By interleaving converters, the clock speed is reduced and more time is available to obtain a good BER specification. The digital output multiplexer increases the sampling frequency of the system with a factor four to obtain the required high sampling rate. In Fig. 3.87 the timing diagram of the High Frequency clock and the individual clocks of the four converters is shown. This figure shows

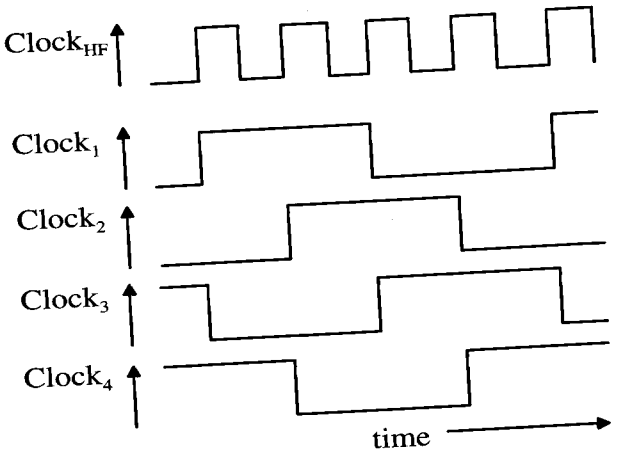


Figure 3.87: Timing diagram of interleaved A/D converter

that every clock to start conversion is delayed 1 HF cycle. In this way a time interleaving is obtained. It seems to be a very good alternative to increase sampling speed by a parallel connection of even more converters. However, problems occur because in a practical solution not all converters show the same offset voltage. By time interleaving (in this example of 4 converters) the different offset voltages of the four converters appears in the signal band

at a quarter of the HF sampling clock. This is not always allowed and therefore offset trimming is required. Furthermore the gain per converter must be equal. This gain must be trimmed too, while bandwidth limitations might introduce a very difficult to trim problem for the total system. Every converter used in the time interleaved architecture shows a different INL and DNL specification. This difference introduces distortion components that appear as signal frequency dependent distortion components in the signal band of interest. However, a careful design shows very good performance for high-frequency oscilloscope applications.

3.16 Minimum supply voltage calculation

In time continuous designs of analog-to-digital converters, the minimum required supply voltage can be calculated. In Fig. 3.88 an input amplifier system with a detail of a single amplifier stage are shown. The detailed

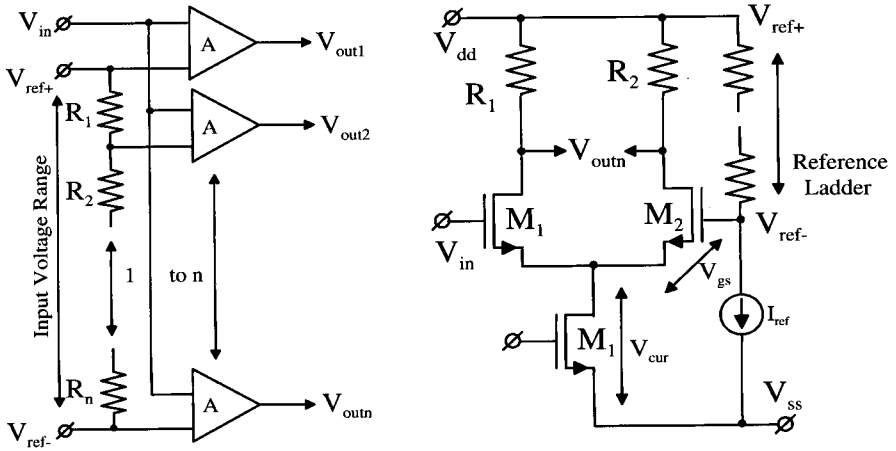


Figure 3.88: Minimum supply voltage calculation model

figure shows a differential amplifier pair M_1, M_2 with resistive loads R_1, R_2 and the reference ladder. Suppose that the reference ladder is connected to the positive supply voltage V_{dd} then with a reference voltage V_{ref} generated across the ladder, the gate voltage of M_2 becomes:

$$V_{gateM1} = V_{dd} - V_{ref} \tag{3.18}$$

The minimum supply voltage that is required to have a working system is now determined by:

$$V_{supply} = V_{dd} - V_{ss} = V_{ref} + V_{gs} + V_{dssaturation}. \tag{3.19}$$

Inserting values for $Vref$ = 1.2 V, V_{gs} + .7 V and $Vdssaturation$ = .2 V, the minimum required supply voltage becomes: V_{supply} = 2.1 V. This means that a system using 2.5 V typical with a 10 % margin giving $V_{supplymin}$ = 2.25 V can be designed.

3.17 Reference ladder signal feedthrough

The reference ladder of an analog-to-digital converter is always loaded with amplifier input stages. In case of a continuous time system the maximum ladder impedance can be calculated. The calculation model is shown in Fig. 3.89. The input amplifier differential pairs that are operating in the

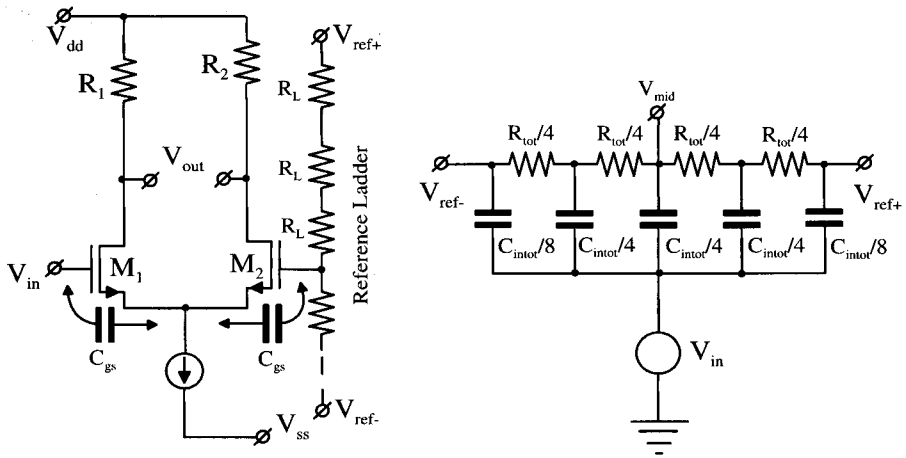


Figure 3.89: Maximum ladder impedance calculation model

linear range have an input capacitance that couples the input signal source with the ladder. The capacitance between the input and the ladder is equal to $\frac{1}{2}C_{gs}$. This capacitance is calculated for a single differential pair. With n-active stages in parallel the input capacitance loading the ladder becomes:

$$C_{intot} = n\frac{1}{2}C_{gs}. \tag{3.20}$$

A distributed model can be set-up to calculate at the middle of the ladder the amount of input signal that is modulating the reference voltage source.

In this model it is supposed that the bottom and top part of the reference ladder are fully decoupled to ground. A good estimate about the maximum value of the ladder resistance can be already obtained by using 4 sections. Working out the equations we obtain:

$$R_{laddermax} = \frac{4\frac{V_{mid}}{V_{in}}}{\pi f_{in} C_{intot}} = \frac{4\Phi}{\pi 2^n f_{in} C_{intot}}. \quad (3.21)$$

With Φ determining the amount of input signal feedthrough in LSB's and F_{in} the maximum input signal frequency. With $C_{intot} = 1$ pF, 1 LSB feedthrough and $f_{in} = 10$ MHz the maximum ladder resistance becomes 500 Ω. It must be noted that the calculated value is a worst case condition.

3.18 Bubble correction

The encoding from thermometer code into a binary weighted output code can in the simplest way performed by a simple AND gate. In Fig. 3.90

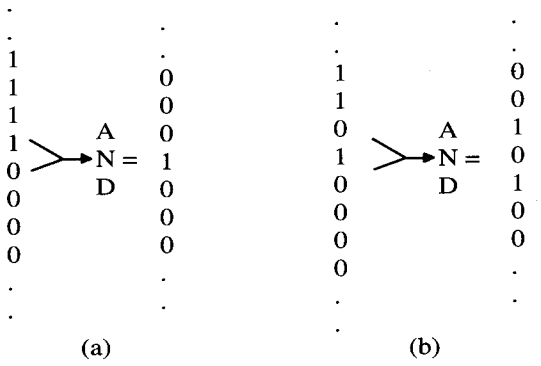


Figure 3.90: (a) Correct and (b) Incorrect encoding

a correct and incorrect encoding concerning the transition of the zero/one code is shown. At the moment a correct thermometer code is obtained, then a simple AND gate can encode a single 1/0 transfer. However, it is possible that due to offsets, noise or other high-frequency effects not a continuous row of 1's is followed by a continuous row of 0's, as shown in Fig. 3.90(b), then two output codes are generated. Normally the single "high" code is applied to a ROM encoder that performs the binary output encoding. In this case a wrong encoding is obtained. Such a wrong encoding can introduce large "digital" glitches that are not allowed. To overcome this problem a more

sophisticated encoding is needed. A simple bubble encoder uses three input AND gates. Then a simple correction of a floating one or a floating zero in the thermometer code can be corrected. More sophisticated correction codes are possible to overcome this problem. In case a folding converter architecture is used, then an EXOR gate determines the single 1 zero transition. In the circular code the 1/0 transition or the 0/1 transition determines the output code for the binary ROM encoder. However, a designer has to design comparators with a low BER. This overcomes part of the problem already.

3.19 Delay over interconnect lines

At the moment a technology scales down, the interconnect lines are reduced in size so the resistance per unit length increases. Furthermore the oxide thickness between the different interconnect layers or substrate is reduced, resulting in an increase of parasitic capacitance per unit area. With a scaled down technology the delay over an interconnect line increases. This delay can introduce clock timing errors that are not tolerable in a high speed analog-to-digital converter. In Fig. 3.91 the delay over interconnect lines with a minimum size as a function of length for different technologies is shown. From this figure it is seen that delay over interconnect lines can

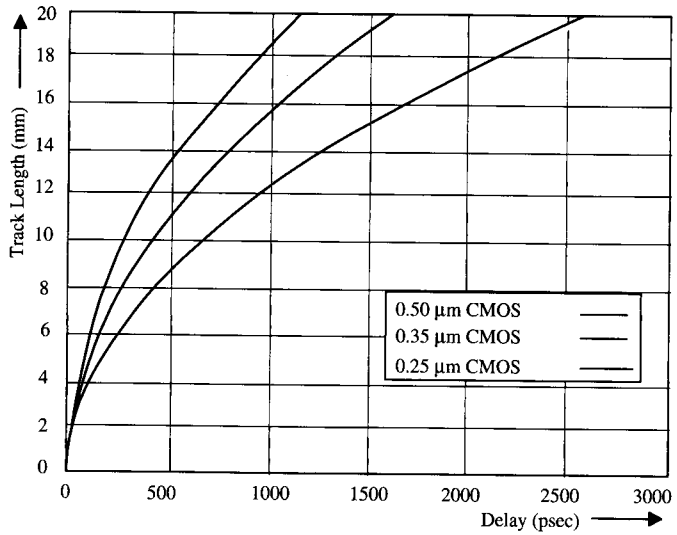


Figure 3.91: Wire delay for different technologies

not be neglected. A delay of 1 psec is equivalent to a wire length of about

100 μm. Such a delay can be already too large. Therefore in the layout of a high-speed analog-to-digital converter special attention has to be paid to clock and signal lines. In Fig. 3.92 an layout example is shown. In

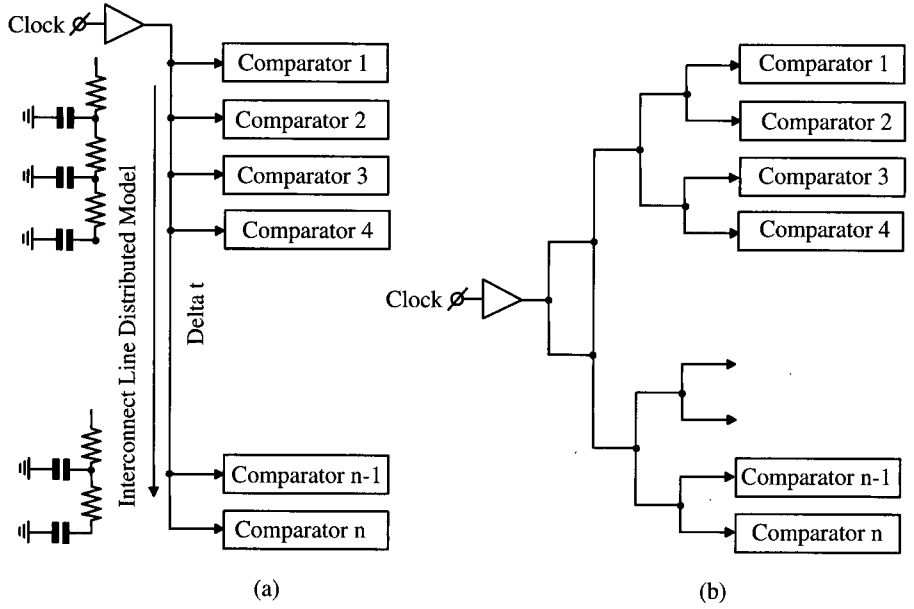


Figure 3.92: Clock layout structures

Fig. 3.92(a) the layout of the clock line in a full flash converter is shown. The clock signal is applied at one side of the chip layout. The interconnect line is modeled as a distributed RC network. As a result of this network comparator n is clocked with a delay δt later than the first comparator. In a full flash converter this results in distortion (usually third order distortion is introduced). To overcome the problem with the wire delay a tree type clock line structure is needed. This is shown in Fig. 3.92(b). The tree structure makes the wire line lengths to every comparator identical. This means that compared to the input clock a fixed delay is introduced at the clock inputs to the comparator. It must be noted, however, that it is required that all comparators have the same device size for the clock inputs, otherwise still an extra delay is introduced due to a larger or a smaller capacitance value at those terminals. The same attention has to be paid to the signal lines connecting the input signal to the different comparator input terminals. Solution form Fig. 3.92(a) could be used in case clock and input signals have the same delay. This must be verified with simulations. Otherwise it

is preferred to use a tree type structure for the input signal too.

3.20 Conclusion

In this chapter different architectures for high speed analog-to-digital conversion have been introduced. Starting with full flash converters, interpolation and averaging has been shown as a method to decrease the amount of hardware and power. At the same time in time-continuous solutions averaging techniques reduce the effect of mismatches between MOS devices. A two-step architecture needs a high-performance sample-and-hold amplifier to sample the analog input signal and hold this signal during the two phases of the conversion process. The sub ranging architecture is a two-step conversion process but is avoiding the accurate gain matching in the second step. Offsets in this architecture are critical. As a result time-discrete solutions automatically compensate for offsets, while these techniques furthermore can operate with lower supply voltages. The pipeline architecture is a cascade of practically identical stages requiring an accurate gain determined mostly by capacitor matching data. Sharing of amplifiers in pipe line converters is possible resulting in a reduced power consumption and smaller die size. Finally folding architectures are introduced that show a combination of a full flash architecture together with a two-step solution. The fine conversion step automatically fits within the coarse conversion range. Different practical solutions of all of the mentioned converter architectures are shortly described. Time interleaving of analog-to-digital converters increases the sampling rate considerably. Applications with multi Gigahertz sampling rates are available.

Chapter 4

High-speed D/A converters

4.1 Introduction

High-speed digital-to-analog converters are used to reconstruct analog signals from digitally generated arbitrary wave form generators. Furthermore these converters are used in telecom applications to generate the modulation signals in mobile phones. Other applications are Ethernet communication sets. Numerous applications are in the area instrumentation systems needing an accurate reconstruction of analog signals from digitally generated signals. The purity of the reconstruction is a measure of the quality of the converter. Especially problems arise at the high frequency end of the output signal spectrum. The spurious free dynamic range is a very good measure for the linearity of the converter at high output signal frequencies. Therefore special designs are needed that perform this function. In many cases the resolution is limited to 10 to 12 bits, although extension into the 14 to 16 bit range will come up soon.
With matched components (resistors, capacitors, or transistors) it is possible to directly convert a digital number into an analog quantized signal. However, the limited accuracy with which components can be matched maximizes the resolution to about 10 to 12 bits. In that case a converter still fulfills the linearity specification.

4.2 High-speed D/A converter architectures

In high-speed digital-to-analog converters with a high fidelity in the reconstruction of analog signals special architectures have to be used. Especially at the high frequency part of the signal spectrum all kinds of timing errors

might occur. These errors have to be minimized and the architecture must be adapted to get an optimum system performance.

4.2.1 Binary weighted converter coding

In a binary weighted architecture the overall accuracy (INL) and the differential linearity (DNL) must be fulfilled. Therefore the matching of the components generating the most significant bits needs most of the attention. Although the die size of a binary weighted converter might be relative small, dynamic performance is another specification that needs a lot of attention. Because bipolar signals (sine waves) are reconstructed, the converter operates with an offset binary coding. This means that around half full scale with a small signal the most significant bit value must be switched very accurately compared to the rest of the bits. This is true when a signal with 1 LSB amplitude is reconstructed. Glitches are mostly a problem due to some mismatch in switching between the MSB bit and all smaller bits. As a conclusion it can be said that binary weighting is not suited for high-speed digital-to-analog conversion.

4.2.2 Fully segmented converter architecture

To obtain a good dynamic performance a full segmentation of a converter can be used. This means that every level in the converter has a switch with a reference current or voltage level connected to this switch. Glitches in this way can be eliminated rather easy, although always attention has to be paid to the overall timing accuracy required to obtain a large dynamic range in accordance to the resolution of the converter. A problem with full segmentation, however, is found in the fact that for example in a 12 bit converter $2^{12} = 4096$ switches have to be addressed and switched at an accurate time moment. Jitter or time skews must be avoided in this architecture to minimize distortion at high frequencies. Die size will increase in the fully segmented converter architecture. This might be not always necessary so a solution is a combination of segmentation for the most significant bits with binary weighting for the least significant bits.

4.2.3 Partially segmentation combined with binary weighting converter architecture

Partially segmentation in the most significant bits combined with a binary weighting for the less significant bits seems to be a good compromise between

die size, power dissipation, accuracy and dynamic performance. With segmentation in the most significant bits the accuracy for the binary weighting can be less stringent. As long as the LSB's fit well within a segment of the MSB's, no monotonicity will arise. Furthermore the MSB levels always are increased by adding a current or voltage value, monotonicity is no problem at this point. How the split-up between number of segments MSB and LSB bits is a decision that depends on the requirements, the resolution of the converter and the matching accuracy of the technology used. In Fig. 4.1 a chart is shown that depicts die area versus segmentation. An optimum can be determined using such a plot for the design that has to be done. From

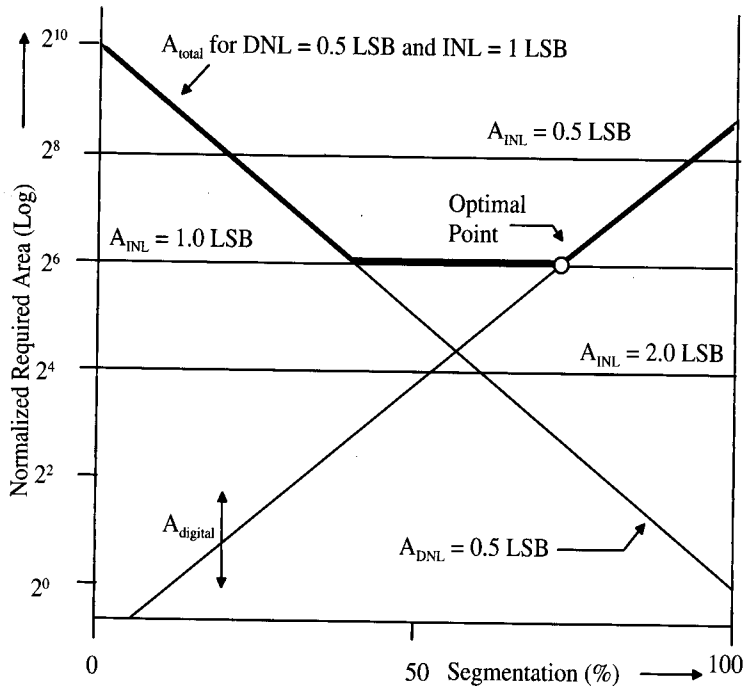


Figure 4.1: Segmentation versus die area plot [133]

this figure it can be seen that when no segmentation is used, extra die size must be incorporated to obtain the required accuracy and get a good linearity. The number of bits and the matching performance of the technology determines part of this curve. The amount of digital circuitry in a binary weighted converter is small. Mostly a number of latches to store the digital input data and control the switches is only required.
When a full segmentation is used, then the die size of the analog bit gen-

eration can be slightly reduced. Monotonicity is always guaranteed, while the DNL specification will be excellent. INL depends again on the process matching specs. However, the digital part of the system increases nearly exponentially as can be seen from the chart.
A combination of segmentation with binary weighting gives an optimum as shown. This optimum is obtained for an INL specification of 1 LSB and a DNL specification of 0.5 LSB.

4.3 Voltage weighting based architecture

An example of a fully segmented voltage based converter will be described here.

4.3.1 Dual-ladder 10-bit D/A converter

A dual-ladder resistor string is used to implement a 10-bit high-speed linear CMOS D/A converter [112]. In Figure 4.2 the basic dual-ladder implementation is shown. The coarse ladder consists of two rows, each built-up from

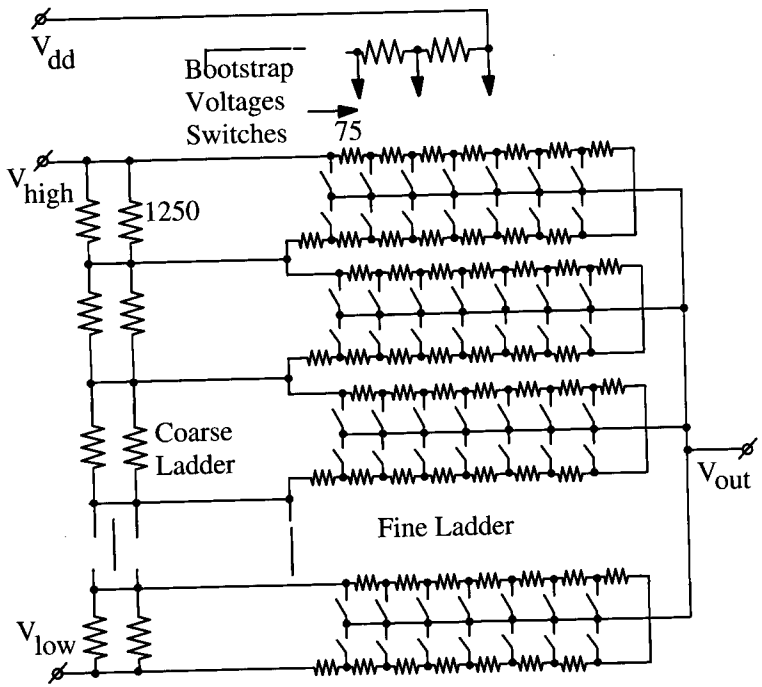


Figure 4.2: Basic dual-ladder system [112]

large size 250 Ω resistors which are connected anti-parallel to eliminate the first-order gradient.

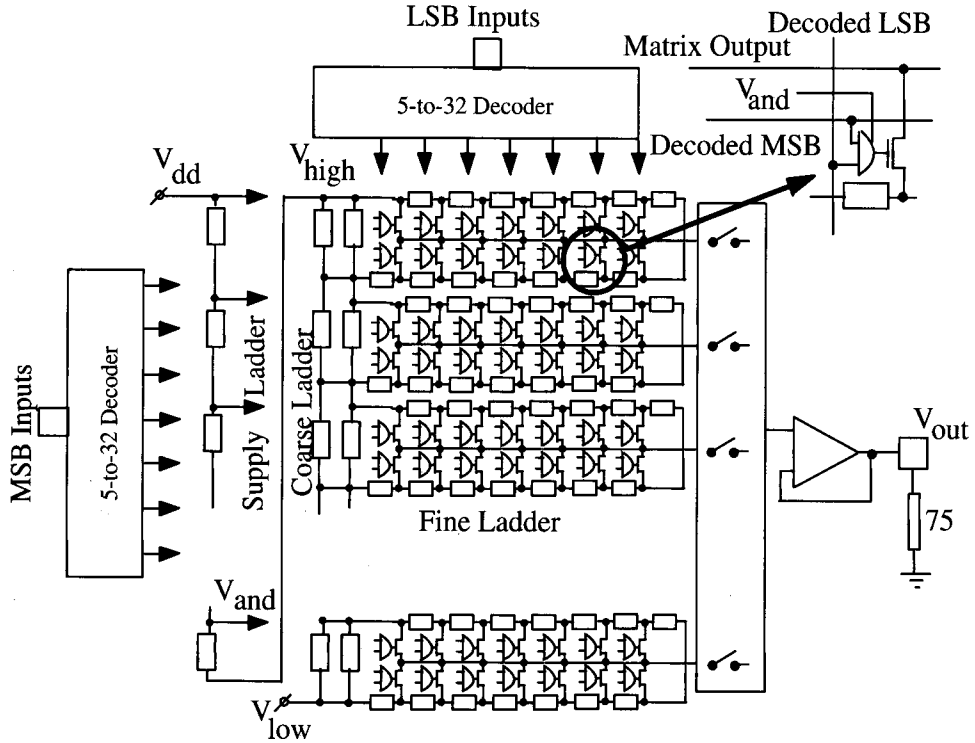


Figure 4.3: Block diagram of 10-bit D/A converter [112]

The coarse ladder in this way determines 16 accurate tap voltages and is responsible for the integral nonlinearity of the converter. A 1024-resistor fine ladder is arranged in a 32-by-32 matrix. Every 64th tap of this fine ladder is connected to the coarse ladder taps. As a result of this configuration the resistivity of a fine ladder resistor can be chosen at 75 Ω. By closing one of the 1024 switches an analog output voltage is obtained at the output. From Figure 4.2 it is easily seen that the output impedance varies as a function of the closed switch position in the network. To compensate for a variable output of the system compensation resistors are inserted. The insert of Figure 4.2 shows how these compensation resistors are added, depending on the switch position. In the insert two fine rows are shown together with the output resistor row shown on the top. As a result of this operation, the output impedance at every position in the fine ladder network is made

constant. No extra distortion or position dependent delay is found by this construction.

However, the ON resistance of MOS switches depends on the "drive" voltage that is applied to the device. As a result, the ON resistance of an MOS switch at the bottom part of the ladder is different from one at the top of the ladder. To overcome this problem an extra ladder is included in the system. This ladder voltage is used to bootstrap the drive voltage of the MOS switching devices. In this way equal drive voltages are applied to nearly all switching devices resulting in equal ON resistances. The coarse ladder can be designed with poly silicon or diffused resistor types, while in the fine ladder poly silicon resistors are preferred because of the low parasitic capacitance of these resistors.

In Figure 4.3 the block diagram of the 10-bit D/A converter is shown. The input digital data is split-up into two five bit parts which are applied to a 5-to-32 decoder. The 5-to-32 decoding is performed in two steps: a pre decoder converts into 10 lines that control 32 three-input NOR gates of which one gate is activated. The two decoders are placed on two sides of the system. To minimize the glitches, the two sets of decoded signal lines are latched by the main clock before running horizontally and vertically over the matrix. In this matrix, the 1024 AND gates perform the final decoding and drive the addressed switch. This switch connects the ladder tap to the output line. In the output line a multiplexer is used, connecting only one output rail to the output terminal, while keeping the other rails at the corresponding middle tap voltage. This scheme reduces the load capacitance and minimizes the (dis)charging of the matrix output rails. At the output terminal an output buffer amplifier is connected to drive a 75 Ω output terminal. In Figure 4.4 a circuit diagram of this output buffer is shown. The amplifier consists of a folded cascode followed by a Miller compensated common source PMOS. Miller compensation is used to stabilize this unity gain buffer stage. An extra 75 Ω on chip resistor is used to prevent shorting of the output amplifier by the bond-pad capacitor at high frequencies. The 75 Ω resistor can be controlled within about ±10 % so the gain variation is for video applications within acceptable values. In Table 4.1 the D/A converter data are shown. The dual ladder system results in a high-performance D/A converter with an excellent differential nonlinearity and a good glitch specification.

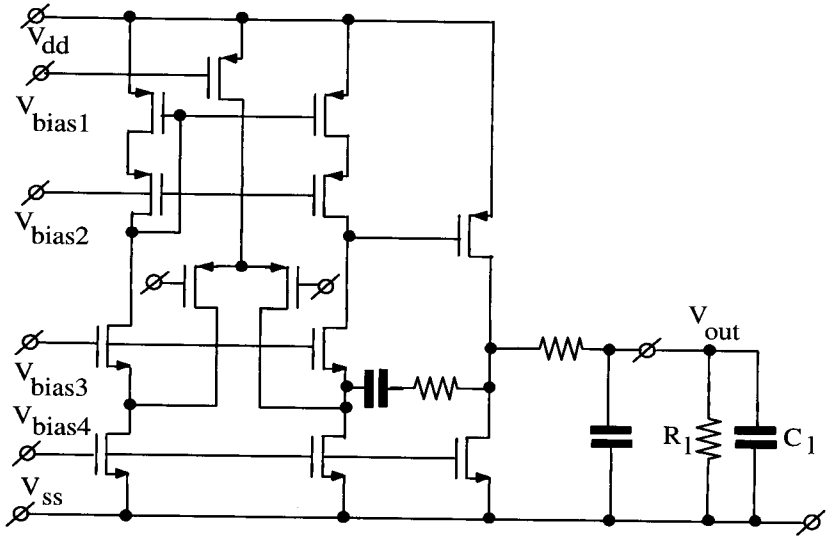


Figure 4.4: Output buffer amplifier [112]

Process	1.6 μm CMOS
DC resolution	10 bit
Differential non-linearity	< 0.1 LSB
Integral non-linearity	$\pm$ 0.35 LSB
Glitch energy	100 pVs
Rise/Fall time (10% – 90%)	6 ns
Signal bandwidth (−1 dB)	19 Mhz
Nominal supply voltage	5 V
Output voltage over 75 Ω	1 V
Power (50 MHz, 75 Ω)	65 mW
Die size	2.5 mm^2

Table 4.1: 10-bit D/A converter data [112]

4.3.2 Equal currents output ladder network

In Figure 4.5 an example of a system using equal currents and an R-$2R$ resistor output network giving the binary weighting is shown. The basic

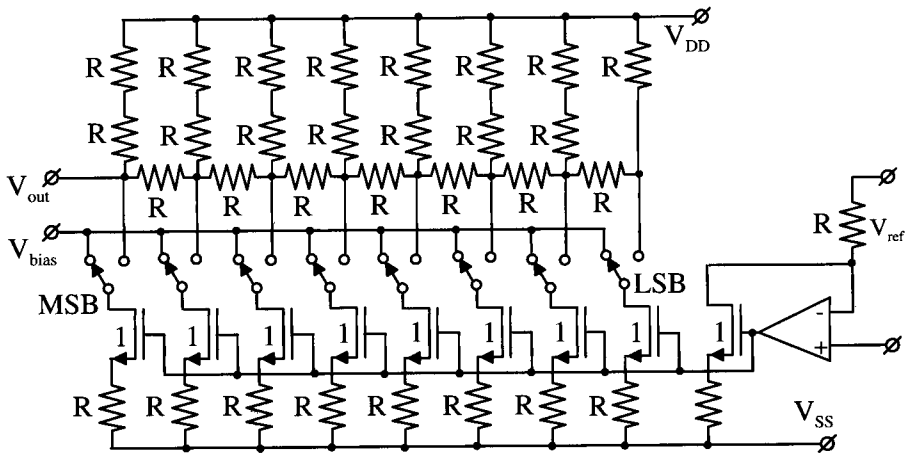


Figure 4.5: High-speed equal current binary weighted resistor network

idea behind this system is that for every technology there exists a transistor size and current density for which an optimum switching performance is obtained. Therefore equal currents are accurately generated in the lower part of the circuit shown in Figure 4.5 using MOS devices with equal source degeneration resistors R. However, degeneration resistors need a certain voltage drop (between 0.5 and 1 V) to be effective in matching accuracy of the output currents. Mostly no resistors are used in MOS technology but a cascoding of the current sources is required to make the output current independent of the output signal and reduce the distortion of the converter. Furthermore the equal current values need only equal sized transistors. The output capacitance of this network is small and equal to a single transistor capacitance. To accurately couple the reference source V_{ref} with the current value I an extra current source is added in a feedback loop with an operational amplifier. This operational amplifier adjusts the gate voltages of the current source transistors in such a way that the current I is equal to:

$$I = \frac{V_{ref}}{R}. \tag{4.1}$$

In high-speed converter systems the switching speed is an important parameter. Therefore a network with equal currents is used in combination with

an output R-$2R$ resistor network to obtain the binary weighting. Mostly the impedance of the R-$2R$ network is designed for 75 Ohm or 50 Ohm, depending on the characteristic impedance of the system the converter has to work with. The digital input information sets the switches in the required position. The current I is applied to an R-$2R$ network to obtain a binary voltage weighting depending on the weight of every input bit. With a low value for R e.g., R= 75 Ohm, the delay through the total R-$2R$ network is low so that a small acquisition time of the total system is obtained. A disadvantage of this system is that the number of accurately matched elements is increased. This has an influence on the yield of these systems, especially when the resolution of the system is increased to 12 to 14 bits. At the very high signal frequency range however, the parasitic capacitance of the switches and the current sources loading the R-$2R$ network introduce a small delay that influences the timing moment at which all analog data appears at the output terminals. As a results of this (although very small) delay an increase in distortion is found. Therefore this system is not for all conditions a good solution.

4.3.3 Data interleaved D/A converter

In very high-speed D/A converter applications the speed of the bit switches and the D/A converter system shown in Figure 4.6 is not the limiting factor [23, 24, 25, 26]. Input data latches and decoding circuitry limit the maximum throughput rate of the converter. Especially in low-glitch designs the three to five most significant bits are encoded into a thermometer code, using equal currents in a part of the circuit. This segment encoding improves monotonicity of a design by increasing the output values with equal steps. Furthermore, such a code minimizes in offset binary-coded converters the glitch energy when small (video) signals are decoded. In this case not the MSB but a much smaller current value is switched, resulting in smaller glitches. The improvement in glitch reduction depends on the number of currents used in the segmentation.

Note that for the generation of the lower bits again a system with equal currents and a binary weighted output ladder network is used. Depending on the technology used for the implementation of the circuit, an optimum between three to five segmented bits with five to seven weighted bits is found for an overall resolution between 8 to 12 bits. To increase the speed of the digital system a multiplexing of the input data channel is used. In Figure 4.6 an example of such a system is shown. As shown, the input

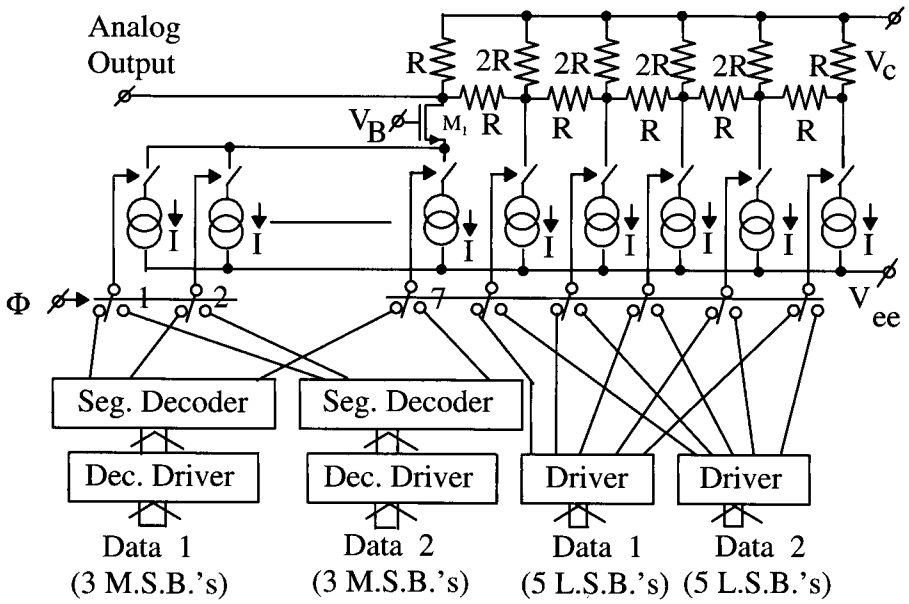


Figure 4.6: Input data interleaved D/A converter

data latches and the decoding circuitry are doubled to allow more time for decoding. A multiplexer switches the latched digital input to the bit switches. An increase in throughput rate of the D/A converter is obtained. Furthermore, the data of the latches remain fixed during the conversion. A clean control voltage is applied to the switches in contrary with data coming from a master-slave flip-flop. Clock speeds up to 1GHz are possible while the multiplexing of the input data stream reduces the amount of very high frequency clock and data feedthrough.

4.4 High-speed segmented converter architecture

In very high-speed digital-to-analog converters mostly a segmented architecture in combination with a binary weighting is used. In Fig. 4.7 this architecture as a combination of a 3-bit segmented current network with a 6-bit binary weighted current network is shown. In the segmented current network part all transistors are equal. This has been denoted with (1), however, the size of these transistors concerning the current weighting must be

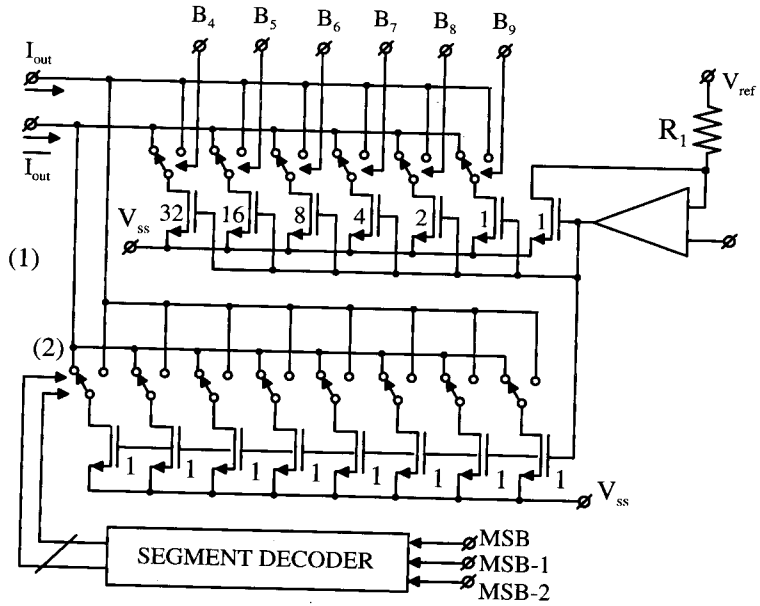


Figure 4.7: Segmented D/A converter architecture

equal to 64I. With

$$I = \frac{V_{ref}}{R_1}. \tag{4.2}$$

The current I in this systems is generated from a reference voltage V_{ref} and a resistor R_1. With the aid of an extra matched transistor and an operational amplifier in a feedback loop the gate source voltage for the whole current network is generated. Depending on the absolute full scale accuracy that is required, the extra reference transistor can be coupled to the binary weighted network or to the segmented network. The coupling to the segmented current sources increases the full scale accuracy at the cost of a larger dissipation.

In high-speed digital-to-analog converters the number of binary weighted bits is mostly much lower than the number of segmented bits. Segmentation improves the linearity, reduces the glitch energy but increases the amount of digital hardware. Binary weighting reduces the amount of digital hardware at the cost of increasing the glitch energy and requiring more analog weighting accuracy by increasing the device sizes. The optimum between segmentation and binary weighting depends on the converter resolution, the matching parameters of the technology used and the layout of the circuit.

4.4.1 10-bit 500 Msamples/sec digital-to-analog converter

The architecture of a 10-bit 500 Msamples/sec digital-to-analog converter is shown in Fig. 4.8 [133]. In this converter 8-bit segmentation is used

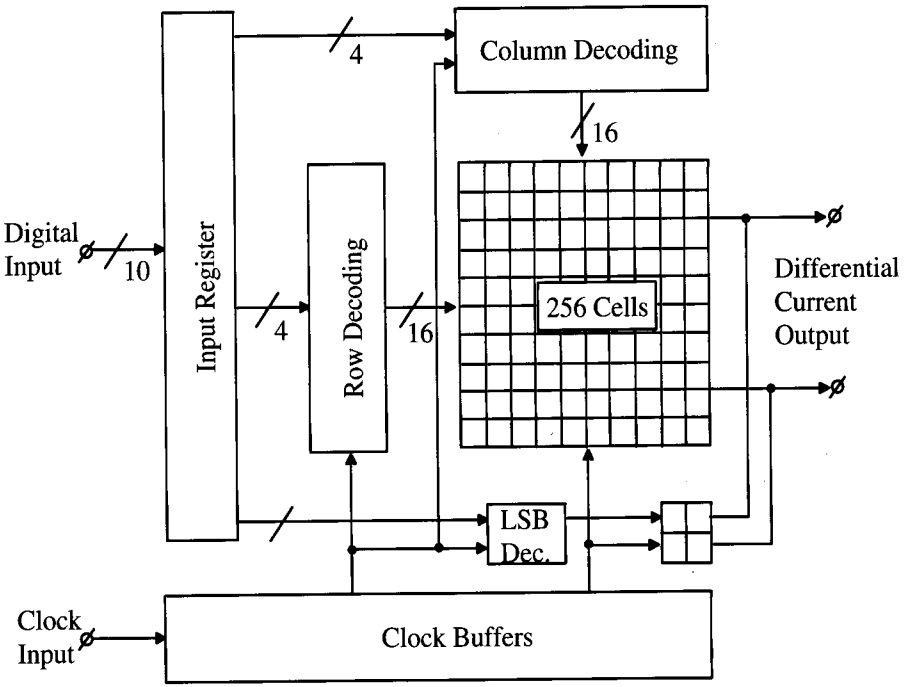


Figure 4.8: 10-bit 500 Msamples/s D/A converter architecture [133]

resulting in 256 equal sized current sources. A 2-bit binary weighted section completes the 10-bit current network. The large amount of segmentation here is used to minimize the glitches and obtain a high accuracy resulting in a good integral non-linearity (INL) and a small differential non-linearity (DNL). The decoding to drive the 256 current network consists of a 4-bit (16 elements) row decoder combined with a 4-bit (16 elements again) column decoder. The 2 least significant bits use an extra decoder to compensate for time delays. At the output a differential output current is obtained. This current flows through the output load resistors to generated the output signal voltage. A clock buffer is included on the chip to obtain a good timing accuracy for the different clock signals used in the converter. Especially the clock moment that drives the bit current switches is very important. Time skews in these clock edges will result in distortion at high output signal frequencies of the digital-to-analog converter. How the segmented network

has been constructed is shown in Fig. 4.9. In the left part of Fig. 4.9 the

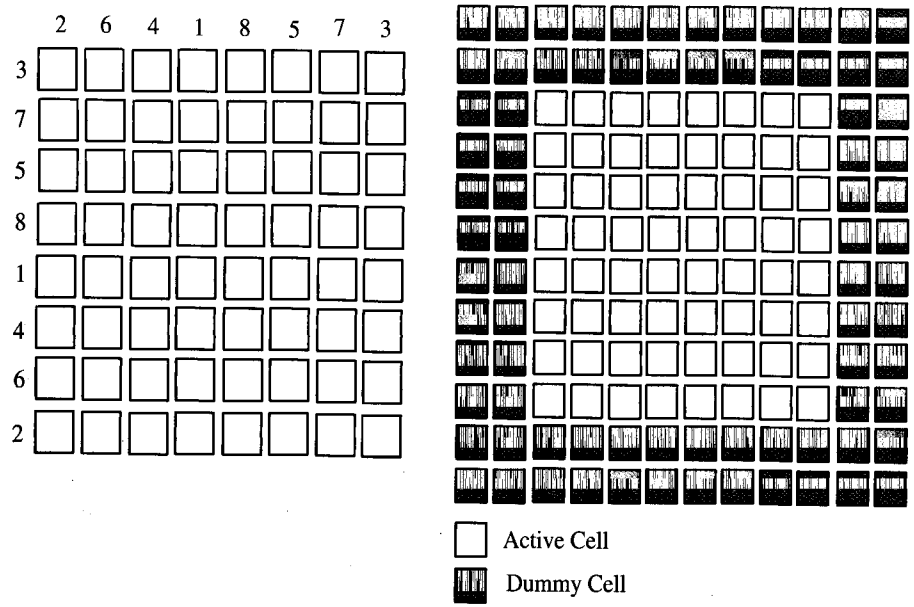


Figure 4.9: Segmented current network layout [133]

layout of one quarter of the 256 current cells as an 8 by 8 matrix is shown. These cells will be later on put into a four quadrant complete system layout as will be shown. Let us first concentrate on the 8 by 8 segmented current cell matrix. In case only such a current cell is used, then measurements will show that not the optimum in accuracy is obtained with this system. The cells that are at the edges always lack a neigbouring cell at one side. This lacking of neighbours results in a less accurate current division. To overcome such a problem dummy cells are applied. These dummies are equal to the active cells but are not used in the current division network. This is shown in the right part of Fig. 4.9. To obtain the best division accuracy two rows of dummy cells are used. Increasing the amount of dummy cells only results in a large die size without significantly contributing to the division accuracy. Note furthermore that in the matrix layout the current cells are randomly placed over the whole area. The numbers at the edges of the matrix determine the addressing of the current cells used in the converter. This improves INL of the converter.
The circuit diagram of the segmented current cells in shown in Fig. 4.10. The current cell consists of a digital and an analog part. The digital part

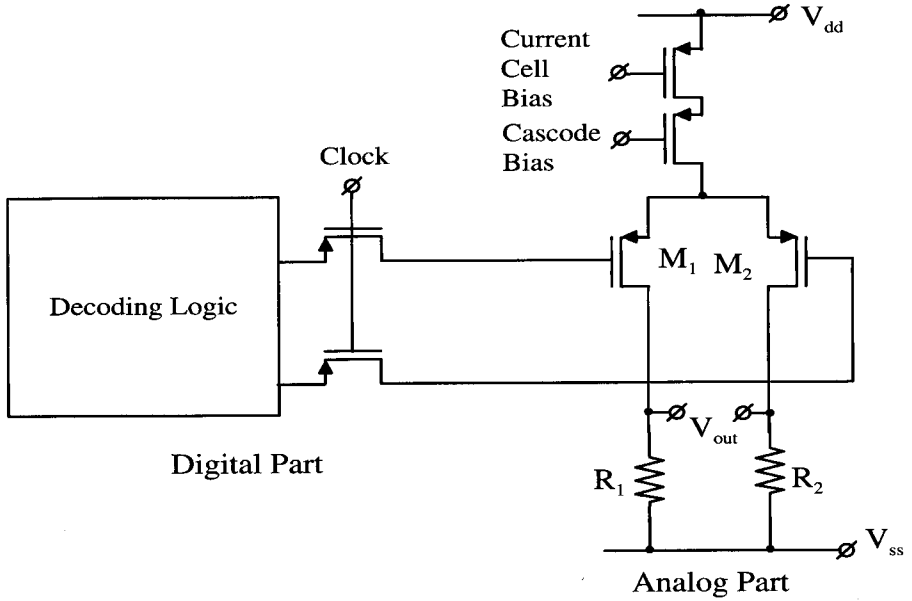


Figure 4.10: Current cell circuit diagram [133]

consists of the decoding logic with the clocked pass transistors to control the switches and an analog part consisting of the cascoded current sources with the differential switch pair M_1 and M_2. The digital part is layed out outside the matrix while the analog part is one of the many cells of the matrix. The output currents of all cells are summed and the total current will be supplied to the load resistors R_1 and R_2 converting the bit currents into the output voltage. A current cell transistor is used with equal gate-source bias voltage for all the cells to generated the segmented reference currents. To avoid the output signal of the converter to modulate the division accuracy due to channel length modulation, a cascode transistor is used. When the switching differential pairs are operated in the saturated mode, then an extra "cascode" is introduced. In this way the drain voltage of the cascode transistor remains already at a fixed voltage level. The final biasing and layout of the total 256 current network matrix is shown in Fig. 4.11. The 8 by 8 matrix current cells are put together in a four quadrant layout to obtain the 256 current network. A global biasing as shown in Fig. 4.11 is applied outside the four quadrant layout to bias the local biasing cells that are added to the current cells. A randomization of part of the circuitry is used to reduce the effect of gradients on the chip. Part of the local biasing is

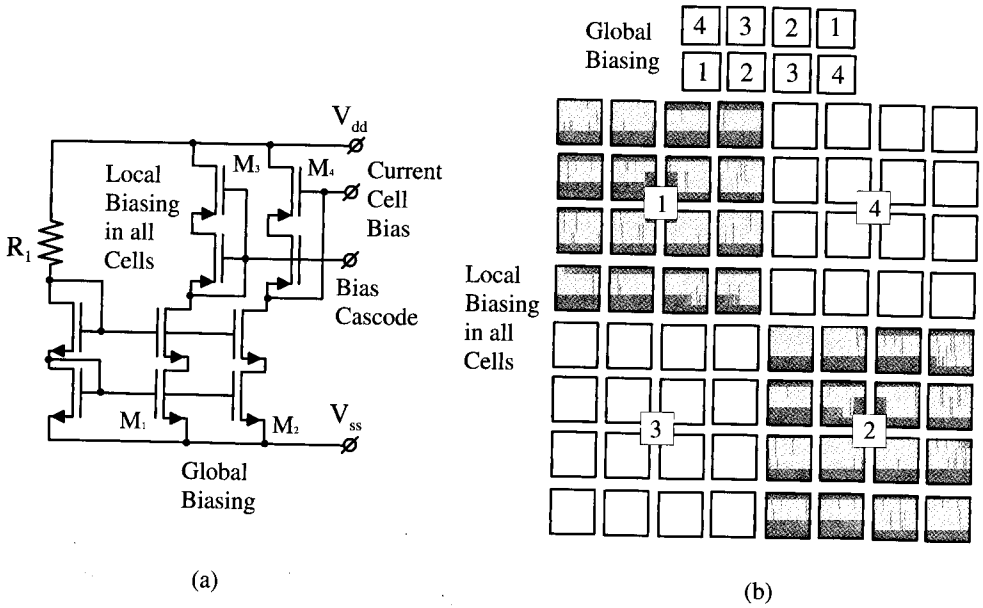


Figure 4.11: Complete 256 current matrix layout [133]

performed to obtain an accurate matching of the currents while furthermore a bias voltage for the cascode transistors is generated. Using global and local biasing avoids problems with voltage drops across the different interconnects used in the matrix. Always care must be taken that the voltage drops across the interconnect lines is not too large with respect to the (voltage) matching accuracy between the devices. This converter has been implemented in a 0.35 μ digital CMOS technology.

4.4.2 Measurement results of 500 Msamples/s 10-bit converter

The following table gives the most important specifications. In very high-speed digital-to-analog converters the high-frequency distortion measurements are of utmost importance. The results of the high-frequency sine wave performance summary are given in fig. 4.12. From Fig. 4.12 it is shown that with a sampling frequency of 500 MHz the spurious free dynamic range (SFDR) at 240 MHz is better than 51 dB. This is a very impressive result obtained by a careful layout and a proper choice of architecture.

Process	0.35 μm digital CMOS Single Poly 4 Metal
DC resolution	10 bit
Differential non-linearity	< 0.1 LSB
Integral non-linearity	$\pm$ 0.2 LSB
SFDR	73 dB
Nominal supply voltage	3.3 V
Output voltage over 75 Ω	2 V_{pp}
Power (f_s = 500 MHz, 75 Ω)	18 mA (analog) 20 mA (digital)
Die size	0.6 mm^2

Table 4.2: 10-bit 500 Msamples/s D/A converter data [133]

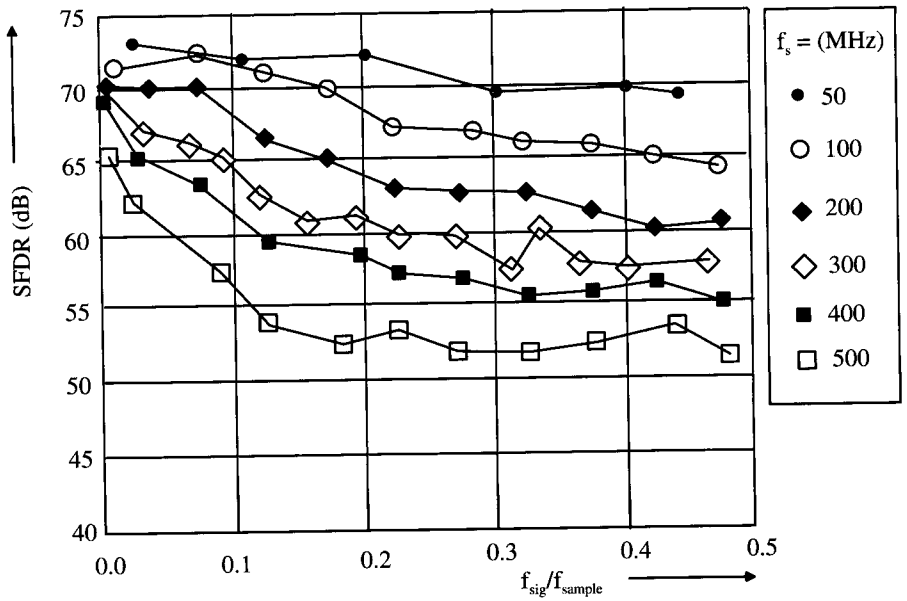


Figure 4.12: Sine wave performance summary [133]

4.4.3 A 10-bit 1-Gsample/s Nyquist digital-to-analog converter

The architecture of a 10-bit 1-Gsample/s Nyquist digital-to-analog converter is shown if Fig. 4.13 [134]. In this converter a 7-bit segmentation is combined

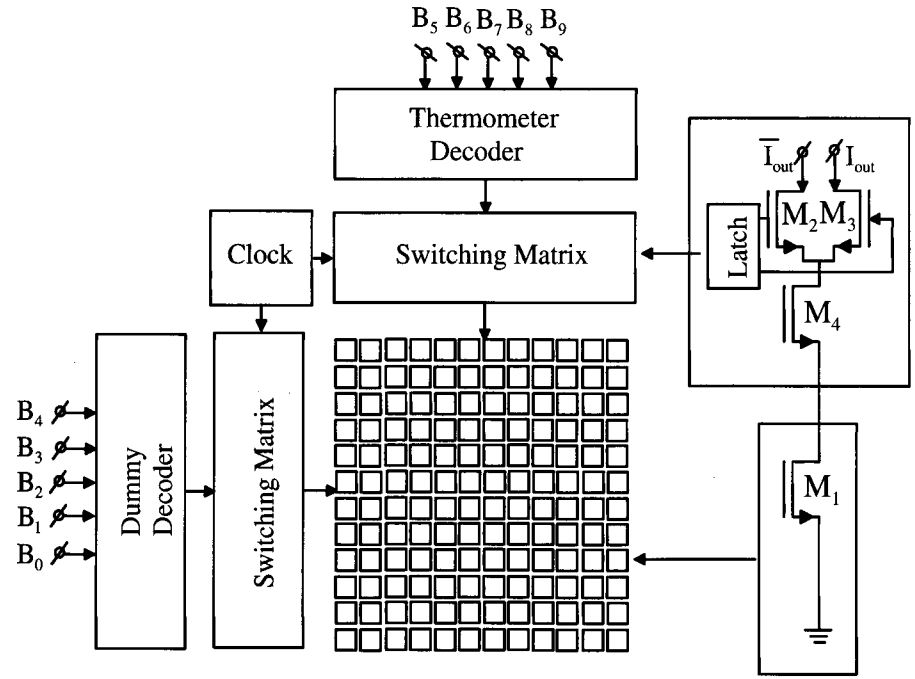


Figure 4.13: 10-bit 1-Gsample/s digital-to-analog converter architecture [134]

with a 3-bit binary weighting. All used current sources are implemented in a matrix structure of 6 by 6 elements. This gives 36 unit elements that are needed in the segmented part of the architecture while the extra 5 places are used to obtain the binary weighting and biasing of the current sources. This will be shown in one of the upcoming figures. Fig. 4.13 consists of the following parts: current source matrix, switching matrix, digital decoder and dummy decoder to obtain equal loading of the switching matrix and the clock driver. An important difference with the design from Fig. 4.8 is found in the design of the switching matrix. This matrix is placed external to the current division network. The current division matrix consists of only one transistor (M_1) that generates the segmented reference current. The cascode transistor (M_4) and the switching differential pair (M_2, M_3) are

outside the reference current matrix. In this way it seems to be possible to obtain a better control of the sampling moment of the bit currents resulting in a better high frequency performance. A special designed latch circuit controls the current bit switches and stores the digital information during conversion.

4.4.4 Current matrix floor plan

The floor plan of the current source matrix is shown in Fig. 4.14. In this floor

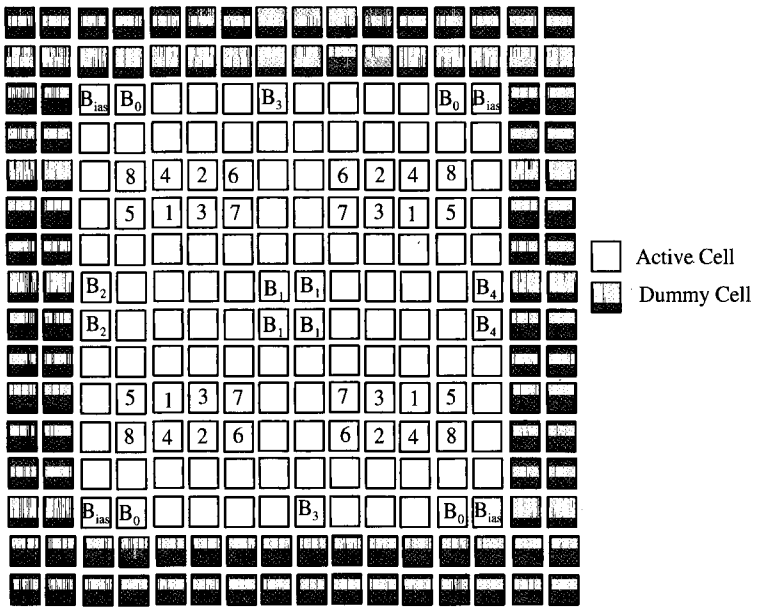


Figure 4.14: Floor plan of D/A current network [134]

plan a quad structure has been used to obtain the 128 segmented current sources. These sources are more or less randomly spaced across the total area. Furthermore the binary bits are shown occupying with the biasing transistors the remaining part of the 144 places in the matrix. Two rows of dummy devices outside the matrix are placed again to obtain the maximum in matching accuracy.

4.4.5 Switch and latch circuit

The detail of the switch and latch are shown in Fig. 4.15. The differential current switch consisting of M_2 and M_3 are directly driven from the

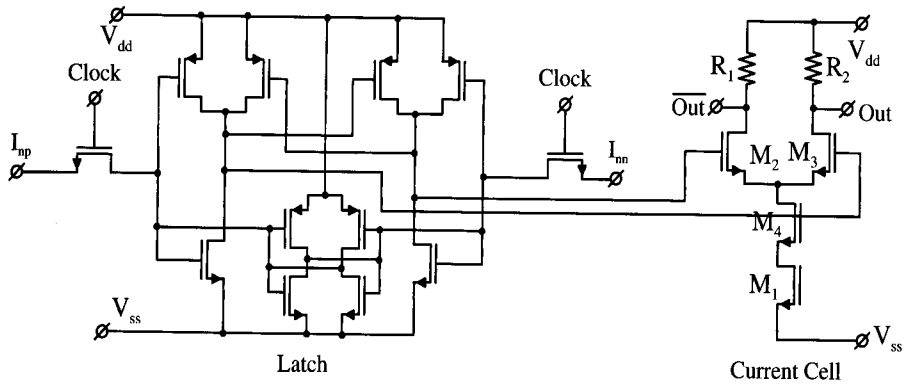


Figure 4.15: Switch and latch circuit diagram [134]

Process	0.35 μm digital CMOS
DC resolution	10 bit
Differential non-linearity	< 0.15 LSB
Integral non-linearity	< 0.2 LSB
SFDR	74 dB
Nominal supply voltage	3 V (analog)
	1.9 V (digital)
Power (f_s = 1 GHz)	110 mW
Die size	0.35 mm^2 (active)

Table 4.3: 10-bit 1-G-sample/s D/A converter data [134]

high-speed latch circuit that forms part of the switching matrix. The pass transistors shown in this circuit apply new digital input data to the latch. This latch is optimized for high-speed switching. When clock is high, the new data is written into the latch consisting of two cross-coupled inverter stages with input gates. Immediately the data change is applied to the differential current switch and the analog output data is reconstructed.

4.4.6 Measurement results of 1-Gsample/s 10-bit converter

The measured data of the 10-bit design are shown in table 4.3. The measurement results of the spurious free dynamic range (SFDR) for this converter are seen as very important information for a user and are given in Fig. 4.16. Although the data for this converter are limited it shows so far that at 490

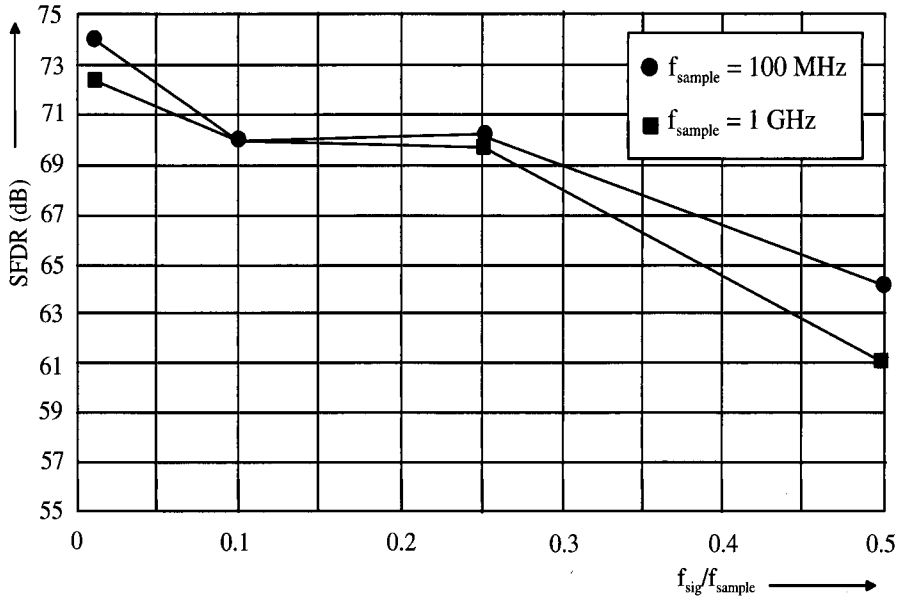


Figure 4.16: SFDR measurements of 1-Gsample/s D/A converter [134]

MHz signal frequency a SFDR of more than 61 dB has been obtained.

4.4.7 12-bit 500 Msample/s digital-to-analog converter

The architecture and floor plan of a 12-bit 500 Msample/s digital-to-analog converter is shown in Fig. 4.17 [135]. This architecture uses a 5-bit segmentation combined with a 7-bit binary weighting. The 5 most significant bits use a thermometer decoder to address the unit bit weights, while in the 7 least significant binary weighted bits a dummy decoder is used to obtain the same delay as found in the MSB encoder. The latch and switching stages are identical to the circuit shown in Fig. 4.15. The current source array is extended and uses an extra compensation to reduce gradient effects on the chip. The clock generator is in between of the MSB and LSB switches and the output current signal is combined and transferred to the output load at the left side of the floor plan. This is performed in the real design in the same manner.

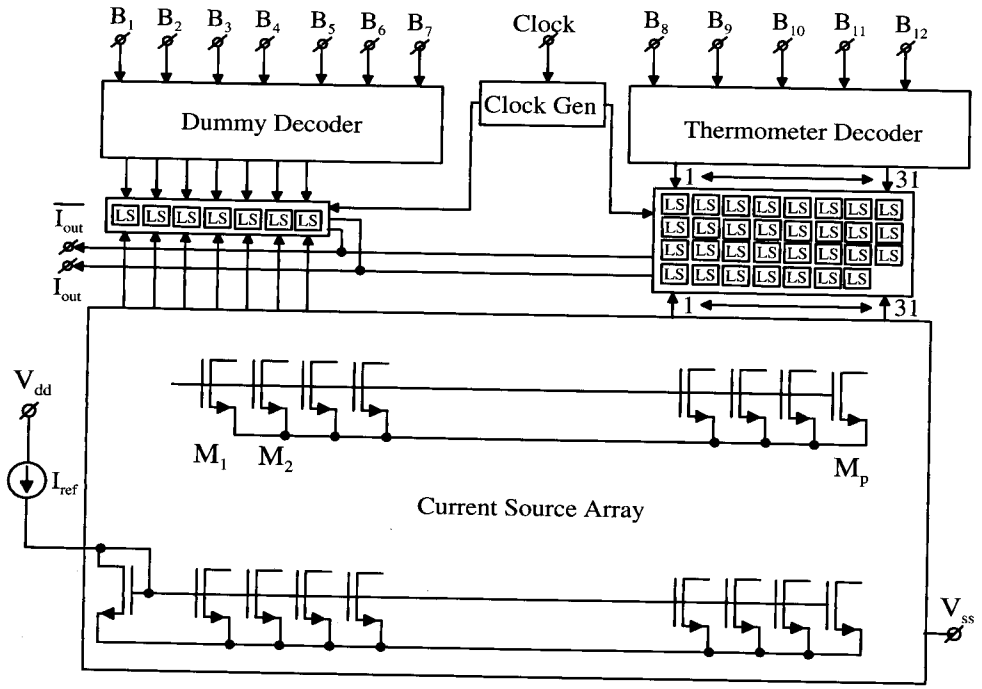


Figure 4.17: 12-bit 500 Msample/s digital-to-analog converter architecture [135]

4.4.8 Measurement results of the 12-bit 500 Msample/s digital-to-analog converter

In Table 4.4 the measurements of the converter are given. Furthermore the SFDR measurements are shown in Fig. 4.18. This is an important criterion for high speed signal reproduction applications. Although this converter uses only a 5-bit segmentation in combination with a 7-bit binary weighting still a good performance is obtained. Unfortunately data about small signal glitches has not been published.

4.4.9 Influence of wire delay on high-frequency performance

The delay over the interconnection wires in digital-to-analog converters can significantly influence the high-frequency performance. In sub micron CMOS technologies the interconnection wires have a substantial resistance while at the same time the capacitance between the wires increases. This is due to the fact that in these technologies the wires seem to be vertical

Process	0.35 μm digital CMOS
DC resolution	12 bit
Differential non-linearity	< 0.25 LSB
Integral non-linearity	< 0.3 LSB
SFDR	79 dB
Nominal supply voltage	3 V (analog)
	2.2 V (digital)
Power	110 mW
Die size	1.0 mm^2 (active)

Table 4.4: 12-bit 500 Msample/s D/A converter data [135]

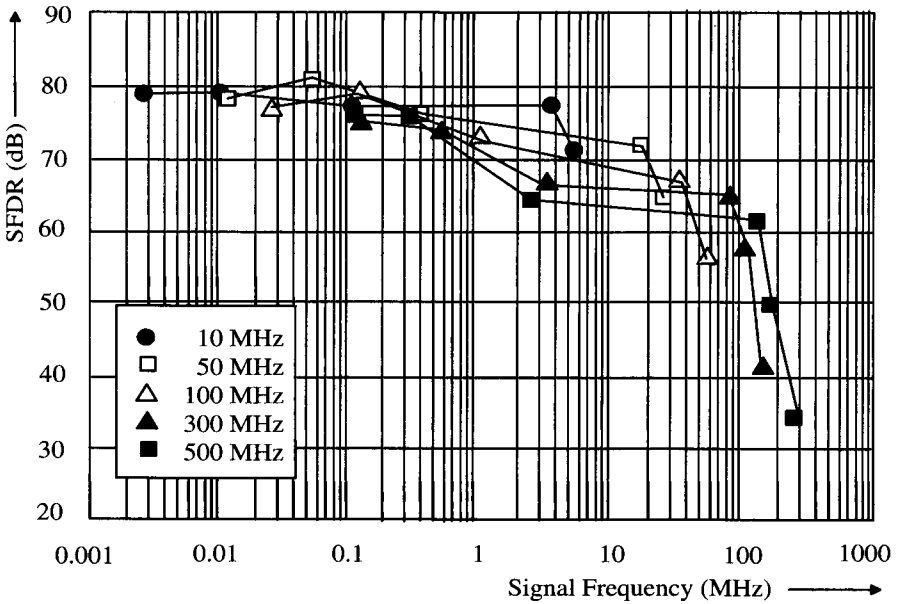


Figure 4.18: 12-bit 500 Msample/s SFDR measurements [135]

placed because of the very small pitch of the first number of interconnection wires. In Fig. 4.19 a simple model of the first and second level of metal is shown. Concentrating on wire W_2 then the largest parasitic capacitances

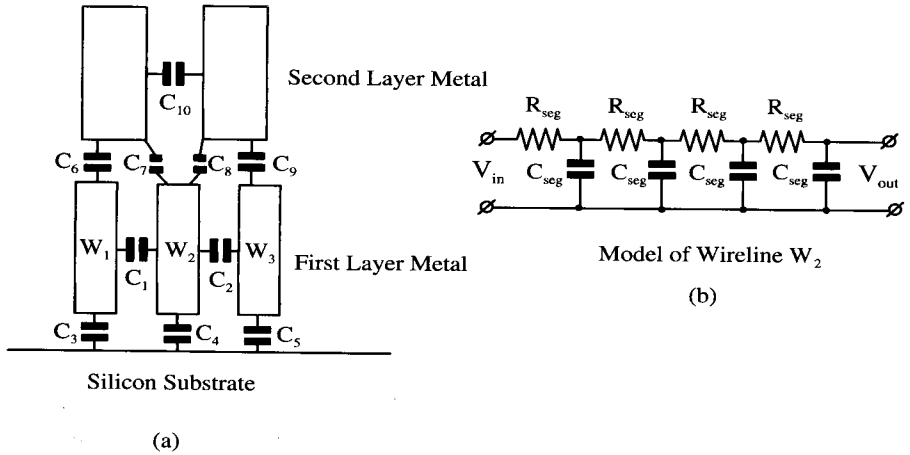


Figure 4.19: Wireline model

are C_1 and C_2. The value of these capacitors depends on the oxide used in the applied technology and the distance between the layers W_1, W_2 and W_3. Furthermore the capacitor C_4 adds to the parasitic while C_7 and C_8 show the coupling between wires on the second interconnection layer. In Fig. 4.19(b) a calculation model as a distributed RC network is shown. The values per unit length for R_{seg} and C_{seg} can be inserted and the delay over the interconnection line can be calculated. From literature it can be found that in sub-micron technology a 1 psec wire delay is already found over a wire length of 10 to 15 μm. This means that with very dense interconnect, the wire delay has a significant influence on the performance of high-frequency systems [137].

4.4.10 Digital-to-analog converter switching network model

A model of the switching part of a high-speed digital-to-analog converter is shown in Fig. 4.20. This model has been setup for the segmented part of a digital-to-analog converter. It consists of a digital part performing the binary to thermometer decoding, the analog bit switches and the cascoded current sources of the converter. The pass transistors shown apply the digital data to the switching differential pairs at the moment the clock signal becomes low. In a practical situation all differential switching pairs show

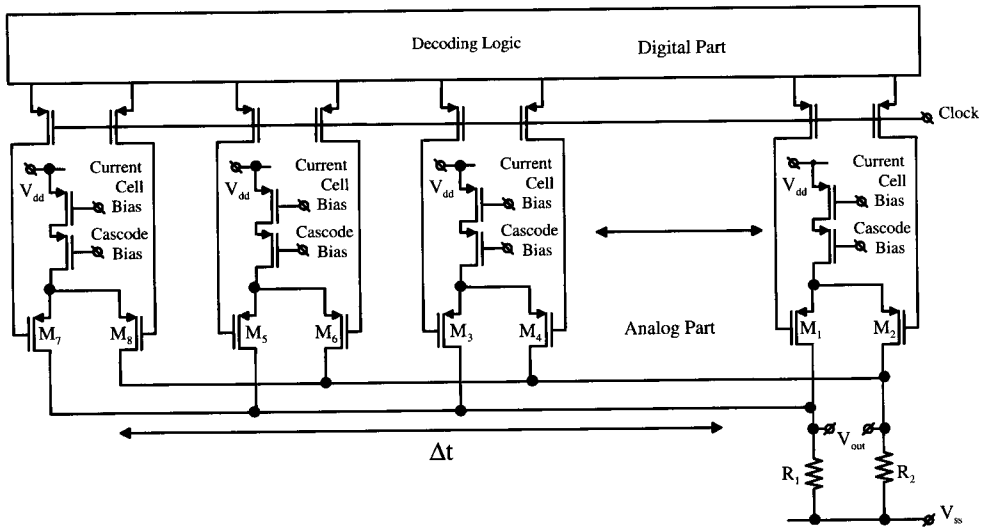


Figure 4.20: D/A switching network model

a finite size. This means that clock and reconstructed data travel over the distance between the individual stages. In this model it is assumed that between the first differential switching pair M_1, M_2 and the last differential pair M_7, M_8 a wire delay of Δt is found. This Δt is in a first approximation present in the clock line too. This means that the first differential pair and analog output data practically do not have any delay, but the last differential pair shows a delay equal to 2Δt. In this model a linear increase in delay is supposed. In practical situations this delay will be an average over the whole segmented section. This segmented section usually is combined with a binary weighted section introducing an extra delay. However, to get an idea of the effect of this wire delay on the high-frequency performance a linear increase in delay with the switching on of the succeeding stages in the segmented converter is modeled. This delay will result in a decrease of the spurious free dynamic range (SFDR) of the converter with increasing signal frequency. Furthermore we suppose that the model is only used at Nyquist frequencies. This eliminates the problem of rise and fall time of the different reconstructed waveforms. During Nyquist operation every reconstructed pulse has the same rise or fall time. At lower signal frequencies more "coupled" pulses appear that introduce extra distortion due to the lack of a rise or falling edge between these coupled pulses. The model is furthermore usable for the design of high-speed converters and obtain layout rules

to optimize Nyquist SFDR data.

4.4.11 SFDR and delay calculation model

Suppose that the delay with clock and reconstructed data equals Δt. Then the timing moment of the reproduce sine wave will change according to this delay as:

$$V_{out} = a\sin(\omega(t + \frac{1}{2}\Delta t\sin(\omega t)). \tag{4.3}$$

Mostly a differential operation of a converter is used so we obtain for the second output signal:

$$\overline{V_{out}} = -a\sin(\omega(t - \frac{1}{2}\Delta t\sin(\omega t)). \tag{4.4}$$

Here a is the amplitude of the output sine wave. In a converter this amplitude becomes:

$$a = \frac{1}{2}2^{Nbits} = 2^{Nbits-1}. \tag{4.5}$$

Furthermore the second output might have a gain error defined by k, with $0 \leq k \leq 1$. The differential output V_{out} - $\overline{V_{out}}$ becomes:

$$V_{out} - \overline{V_{out}} = a\sin(\omega(t+\frac{1}{2}\Delta t\sin(\omega t)) + (1-k)a\sin(\omega(t-\frac{1}{2}\Delta t\sin(\omega t)). \tag{4.6}$$

Working out this equation and using a series expansion we obtain:

$$V_{out} - \overline{V_{out}} = (1+k)a\sin(\omega t) + (1-k)\frac{a}{2}\frac{\omega\Delta t}{2}\sin(2\omega t) + \frac{a}{4}\omega^2\Delta t^2\sin(3\omega t). \tag{4.7}$$

The second order distortion of the converter becomes:

$$d_2 = \frac{1-k}{2(1+k)}\omega\Delta t. \tag{4.8}$$

The third order distortion becomes:

$$d_3 = \frac{\omega^2\Delta t^2}{4(1+k)}. \tag{4.9}$$

At high signal frequencies d_2 and d_3 determine for an important part the spurious free dynamic range (SFDR). At low frequencies the SFDR is determined by:

$$SFDR_{lowfreq} = \frac{2^{Nbits}}{|INL|}. \tag{4.10}$$

The spurious free dynamic range as a function of signal frequency can now be modeled as:

$$SFDR = \frac{1}{|INL|2^{-Nbits} + \frac{1-k}{2(1+k)}\omega\Delta t + \frac{\omega^2\Delta t^2}{4(1+k)}}. \quad (4.11)$$

In decibels this equation becomes:

$$SFDR = -20\log(|INL|2^{-Nbits} + \frac{1-k}{2(1+k)}\omega\Delta t + \frac{\omega^2\Delta t^2}{4(1+k)}). \quad (4.12)$$

With INL in LSB's.
The above described model has been applied to the data of the 10-bit 500 Msample/s digital-to-analog converter of Fig. 4.8 and the 12-bit 500 Msample/s digital-to-analog converter from Fig. 4.17. The results of the curve fits are shown in Fig. 4.21 and Fig. 4.22 respectively.

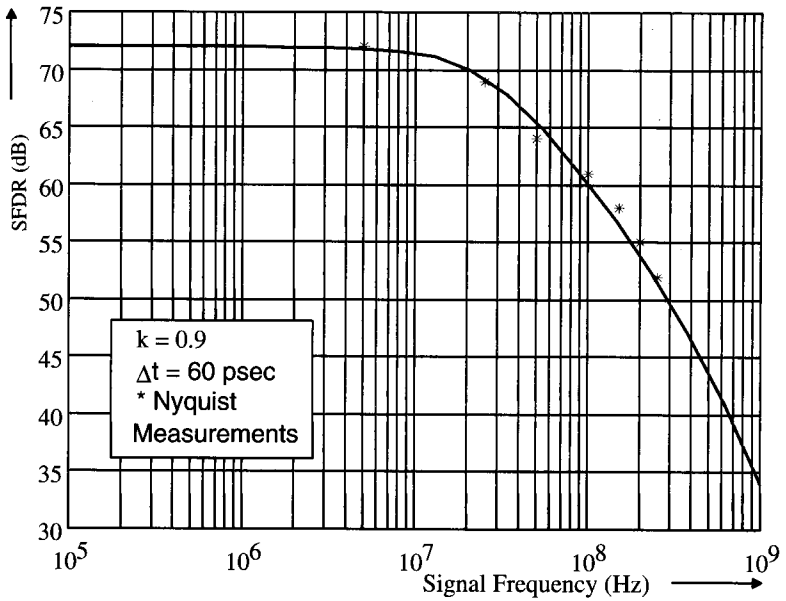


Figure 4.21: SFDR model and measured data 10-bit D/A

The results of the curves show a pretty well fit with the measured data. The low-frequency SFDR has been used to obtain a limited SFDR at normal signal frequencies as has been determined by the low frequency SFDR. Much attention has to be paid to the delay between the clocking of the switch

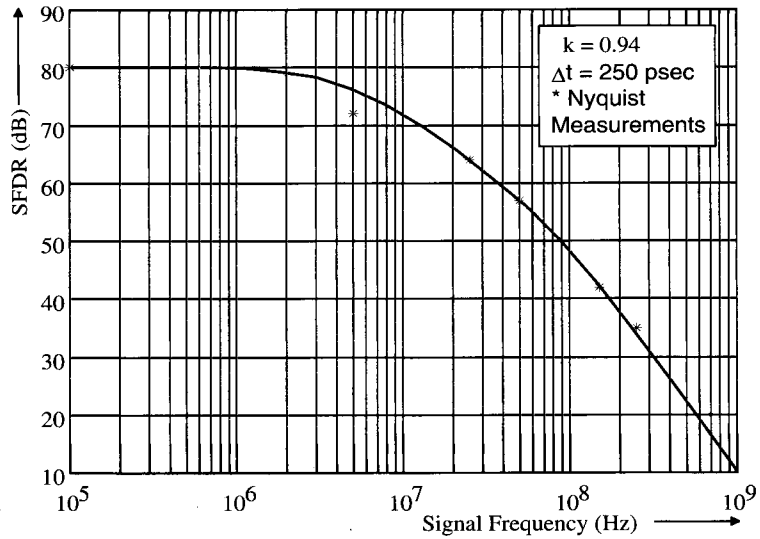
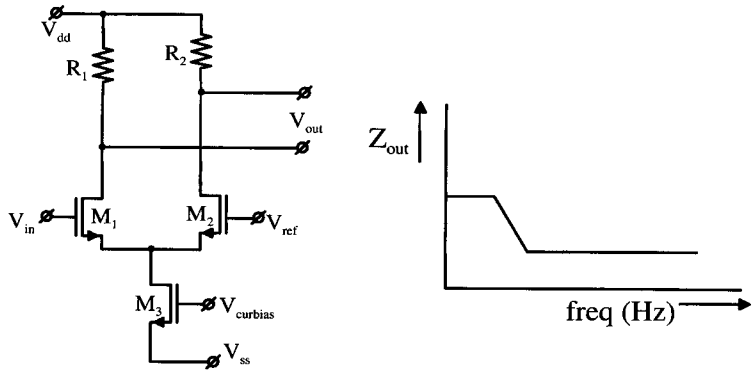


Figure 4.22: SFDR model and measured data 12-bit D/A

data and the generation and reproduction of the output signal of digital-to-analog converters. It might be that here tree type structures can improve the Nyquist SFDR performance of converters.

4.4.12 Output impedance of current cells

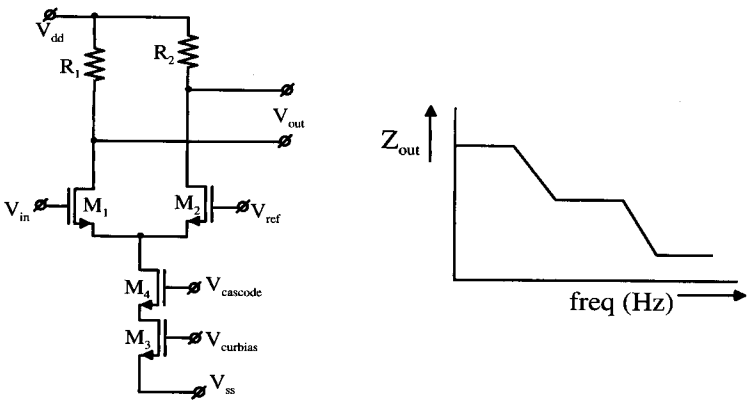
The output impedance of the current cells need to have a minimum value to reduce the distortion in the system. This output impedance influences the output signal of the converter while mostly with a limited channel matching a second order distortion is introduced. In a segmented structure the output impedance of the digital-to-analog converter reduces at the moment more current cells are used to generate the output signal. In Fig. 4.23 the output impedance of a single current cell with a switch is shown. At low frequencies the output impedance of the current source is equal to the impedance of the transistor itself. With increasing frequency this impedance reduces due to the drain capacitance of the system. This is true when the switch is operated as a low impedance switch. At the moment the switch M_1, M_2 is operated in the saturated mode, then a cascode effect appears and the output impedance increases with a factor $g_{m1,2}R_{outM1,2}$. Depending on the



(a) (b)

Figure 4.23: Single transistor current source

channel length of transistors M_1 and M_2 this multiplication effect can be between 5 to 20. Again at high frequencies the drain capacitance of in this case M_1 or M_2 reduces the impedance as shown. When a cascode is added to the current cells, the circuit is modified into Fig. 4.24. The output



(a) (b)

Figure 4.24: Cascoded current cell

impedance of the current cell increases with $g_{m4}R_{outM4}$ in case the switches are operated as low impedance switch. At the moment the switches are operated in the saturated mode, then an extra multiplication of the output impedance of the current cell with a factor $g_{m1,2}R_{outM1,2}g_{m4}R_{outM4}$. A high

output impedance is possible.

4.4.13 Calculation of minimum current cell output impedance

It is important to know the minimum required output impedance of the current source in a segmented digital-to-analog converter. Except from the fact that the output signal of the converter can modulate the segment currents due to channel modulation in the MOS devices an additional effect might occur introducing distortion. Suppose that the channel modulation of the segment currents is small enough to obtain the accuracy in the converter, then in a segmented converter, every time a current source is added, then the output impedance of this current source results in a decrease of the output signal. Suppose that the output impedance of a segment current source is R_{outc}, then in a converter with the number of segmented currents equal to N_{seg}, we obtain for the output impedance of the digital-to-analog converter in case a sine wave is applied:

$$R_{DAC} = \frac{R_{outc}}{2^{N_{seg}-1}(1+\sin\omega t)}. \tag{4.13}$$

When the current digital-to-analog converter is loaded with an output resistor R_l, then the output voltage becomes:

$$V_{out} = \frac{i_{DAC}\sin\omega t R_l}{(1+\frac{2^{Nseg-1}R_l}{R_{outc}})+\frac{2^{Nseg-1}R_l}{R_{outc}}\sin\omega t}. \tag{4.14}$$

In a differential output converter the opposite signal phase becomes:

$$\overline{V_{out}} = -k.\frac{i_{DAC}\sin\omega t R_l}{(1+\frac{2^{Nseg-1}R_l}{R_{outc}})-\frac{2^{Nseg-1}R_l}{R_{outc}}\sin\omega t}. \tag{4.15}$$

In this equation $k \approx 1$ determines the matching between the two differential output signals. In an ideal case $k = 1$, however, in practice $.9 < k < 1.1$ because of mismatches between output impedances, interconnect line impedances and mismatches between the load resistors. All these mismatches will be included in k. Working out these equations will result in a second order distortion d_2 of the output differential signal $V_{diff} = V_{out}$ - $\overline{V_{out}}$ equal to:

$$d_2 = \frac{\frac{2^{Nseg-2}R_l}{R_{outc}}(k-1)}{(k+1)(1+\frac{2^{Nseg-2}R_l}{R_{outc}}(k+1))}. \tag{4.16}$$

In case

$$R_l \ll R_{outc}, \tag{4.17}$$

then the distortion is approximated by:

$$d_2 \approx 2^{N_{seg}-2} \frac{R_l}{R_{outc}} \frac{(k-1)}{(k+1)}. \tag{4.18}$$

Inserting the following values into equation 4.18 we obtain:

$$k = 1.1 \tag{4.19}$$
$$R_l = 50\Omega \tag{4.20}$$
$$R_{outc} = 100k\Omega \tag{4.21}$$
$$N_{seg} = 5 \tag{4.22}$$
$$d_2 \approx -74dB. \tag{4.23}$$

In a 10-bit converter this distortion is small enough not to influence the overall performance too much. Furthermore in case the number of segmented bits is increased from $N_{seg} = 5$ to $N_{seg} = 7$, then the output impedance R_{outc} of the current source must increase with a factor $2^2 = 4$ to obtain the same second order distortion. Modifying equation 4.18 it is possible to calculate the minimum required output impedance of a segmented current source to obtain a specified distortion d_2, then we get:

$$R_{outc\ min} > 2^{N_{seg}-2} \frac{R_l}{d_2} \frac{(k-1)}{(k+1)}. \tag{4.24}$$

Equation 4.24 is very useful for a designer to obtain the minimum required current source output impedance as a function of the number of segmented elements and the required distortion in a digital-to-analog converter.

4.5 Conclusion

In this chapter specifically high-speed converter architectures and a number of practical designs have been discussed. The specific problems encountered with high-speed conversion include time jitter of the clock, matching problems of devices and how these problems can be solved. Architectures that use segmentation to reduce the glitch problems and at the same time improve linearity and timing problems encountered by interconnect and practical size of devices on a chip have been given. A model that describes best the delays introduced by the interconnect and the effect on the spurious free dynamic range (SFDR) has been developed and tested on two of the described digital-to-analog converters. This model gives a designer extra information about the layout of such a converter and how this layout can be optimized to

obtain the best SFDR at Nyquist frequencies. Furthermore a model is used to determine the minimum current source output impedance in a segmented converter. This output impedance introduces second order distortion that in a practical converter with finite matching between the differential outputs is found. A matching coefficient between 0.9 and 1.1 seems to be large, however, interconnect lines at a 50 Ω output impedance can already have a significant influence on the channel matching. This is true when long wires are used in the layout that do not walk parallel through this layout.

Chapter 5

High-resolution A/D converters

5.1 Introduction

High-resolution monolithic A/D converters are subject to growing interest due to the rapidly expanding market for digital signal processing systems. The introduction of digital audio recording equipment such as Super Audio Compact Disc (SACD) players requires resolutions from 16 to 24 bits. Monolithic converters with such a high linearity are difficult to design and require special circuit configurations. When a low conversion speed is needed, integrating types of converters can be used. In integrating types of high-resolution A/D converters basically the analog input signal is converted into a time which is proportional to the input signal. Time is measured using a counter with an accurate clock. These systems are relatively slow because of the counting operation in the time-to-number conversion cycle. A speed improvement is obtained by using a coarse and fine conversion cycle in the time-to-number counting operation. A well-known analog-to-digital converter based on this system is the dual slope converter. This converter is mostly used in digital voltmeters.

In fast and highly accurate A/D converters, the successive approximation method is commonly used. Accuracy and linearity in this system are determined by the D/A converter, while the conversion speed depends on the comparator response time and the settling time of the D/A converter. In a successive approximation system the analog input signal is approximated by the step-by-step built-up analog output voltage of the D/A converter,

starting with the most significant bit. To obtain the high accuracy for the D/A converter needed to construct a 14- to 16-bit A/D converter, *Dynamic Element Matching* is used. In the 16-bit A/D converter, that will be discussed in the following sections, the 16-bit D/A shown in Figure 6.40 is used. Due to the construction of the bit switches, which in the high-accuracy part consist of a diode-transistor configuration, the output voltage swing at the D/A current output must be small. This voltage swing, called output voltage compliance, reduces the bit switching accuracy of the D/A converter. To avoid problems in this system, a special comparator operation is needed. In general-purpose A/D converters, a general nonlinear comparator circuit with high gain around the zero-crossing level is used. Such comparators generally have a certain voltage compliance which is above the range needed for the D/A converter from Figure 6.40. Therefore, a wide-band, high-speed operational amplifier with diode clamps is applied in the inverting mode. The voltage compliance in this case remains below a few milli volts. This is accurate enough to obtain the full accuracy of the D/A converter.

The ease with which a hold operation can be constructed allows an A/D converter implementation using a cyclic converter algorithm. In the cyclic converter the number of components is drastically reduced and consists of two sample-and-hold amplifier circuits with an accurate times two amplifier stage and a subtracter circuit. Per conversion step the remaining signal is compared with a reference signal. If the remainder is larger than the reference signal, a subtraction of the reference signal from the remainder is performed. The error signal that is then generated is amplified by two and compared with the reference signal again. This operation is repeated until the total number of bits that can be converted is obtained. Finally self-calibration schemes are shown, which use an additional cycle to calibrate the complete converter. During calibration, however, it is not possible to use the converter effectively in the system.

5.2 Single slope A/D converter system

In Figure 5.1 a block diagram of a single slope A/D converter is shown. The circuit consists of a resettable integrator, which generates the accurate reference ramp signal, a comparator, and a counter. The input signal is applied to one input of the comparator. At the moment the conversion starts, the counter is set at zero and the integrator is reset by closing switch S_p. When a positive input signal V_{in} is applied, the integrator starts generating

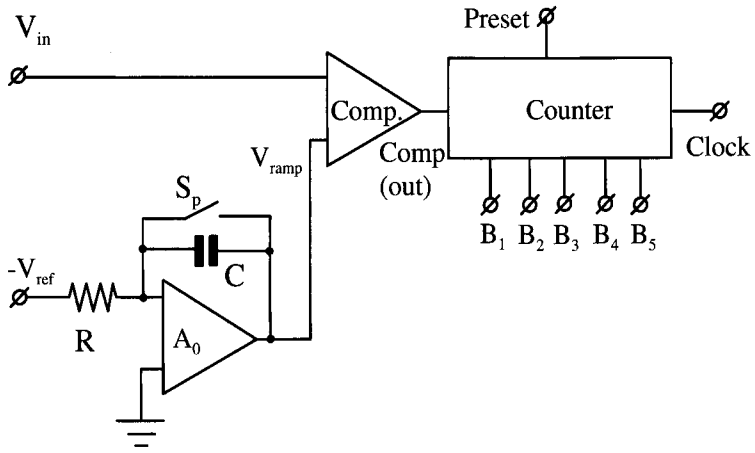


Figure 5.1: Single-slope A/D converter system

the ramp function. In the meantime a gate is opened that applies counting signals to the counter. At the moment the output signal of the integrator equals the input signal, the gate is closed and the counter stops. In Fig. 5.2

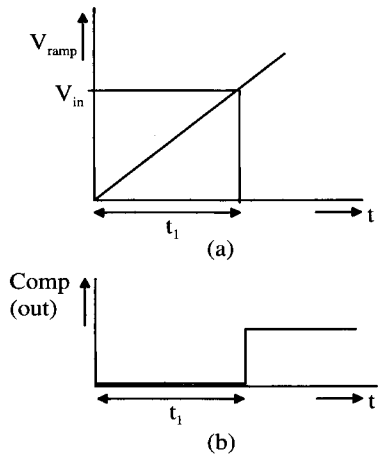


Figure 5.2: Single-slope A/D converter timing

the timing diagram of the converter operation is shown. The analog input signal is converted into a time that is measured by counting clock pulses during that time. An accurate time-to-number conversion is obtained. The accuracy of the system is determined by the clock generator, the RC time constant of the integrator, and the reference source V_{ref}. A simple calcu-

lation shows that the time to which an input signal is converted is equal to:

$$t_1 = RC\frac{V_{in}}{V_{ref}}. \tag{5.1}$$

The digital output value then becomes:

$$N_{digital} = t_1 \times f_{clock}. \tag{5.2}$$

Offset of the comparator can be canceled by measuring the offset with a zero input signal. This offset number can be used to preset the counter. In this way an automatic offset compensation is obtained.

5.3 Dual-slope A/D converter system

To overcome a number of the accuracy problems encountered with the system from Figure 5.1 a dual-slope system has been designed. A system diagram is shown in Figure 5.3. The system consists of an input switch, an

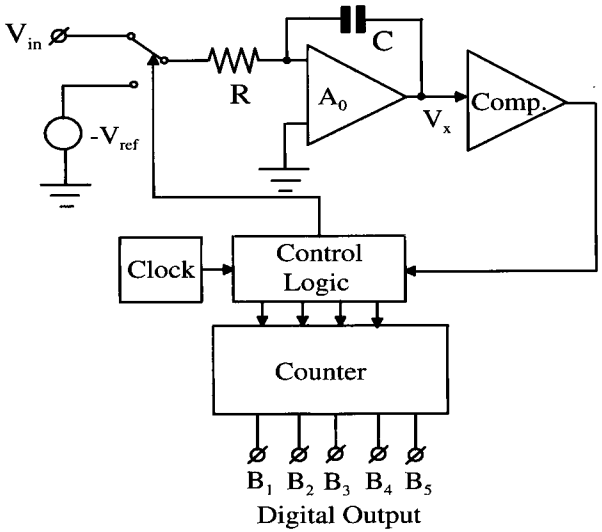


Figure 5.3: Dual slope A/D converter system

integrator with a comparator, a clock generator with control logic, and a counter. The operation of the system is as follows. Starting from a reseted integrator, the input signal V_{in} is integrated during a time t_1 which corresponds with a full count of the counter. Then the input is switched to the reference voltage V_R having the opposite sign compared to the input

signal. The integrator is now discharged. During the discharge time pulses are counted. Counting stops when the comparator detects zero. As a result, the counts in the counter represent the digital value of the input signal. The timing of the operation is shown in Fig. 5.4. A simple calculation shows:

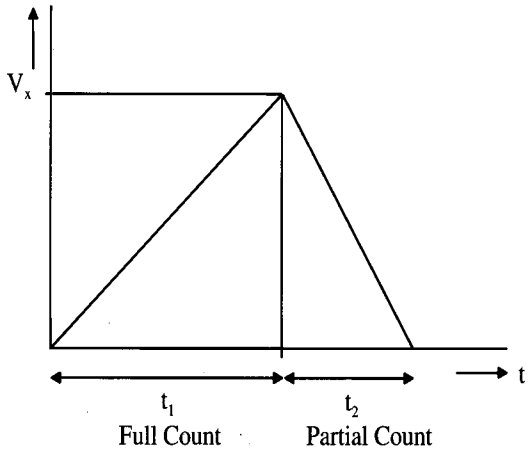


Figure 5.4: Dual slope A/D converter timing

$$V_{in} = V_R \times \frac{t_2}{t_1}. \tag{5.3}$$

Here t_2 is the time during which the integrator is discharged from the integrated input signal to zero. As is shown in equation 5.3 the clock is not critical; only the ratios between the charge and discharge times is important. A disadvantage of this system is the low conversion speed if a high resolution is required. In digital voltmeters these systems are very popular.

5.4 Dual-ramp single-slope A/D converter system

To decrease the conversion time of the single-slope A/D converter as shown in Figure 5.1 a dual-ramp system has been designed. The block diagram of the dual ramp converter is shown in Figure 5.5 [29]. The system consists of an inverting sample-and-hold amplifier with feedback resistors R and hold capacitor C, two reference current sources with current values I and $\frac{I}{256}$, comparator $comp_1$ with threshold voltage V_t, and comparator $comp_2$ which control the coarse and fine counting operation using the control logic function, a clock generator, and a coarse and fine counter. At the start

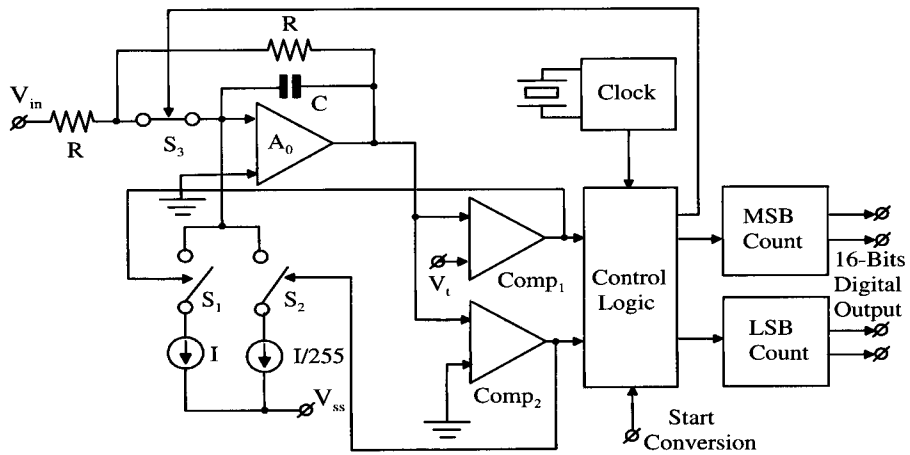


Figure 5.5: Dual-ramp single-slope A/D converter system

of a conversion, the counters are set to zero and the switch S_3 is closed. Switches S_1 and S_2 are open, so no current flows into the sample-and-hold integrator. Closing switch S_3 causes the operational amplifier to act as an inverter charging the hold capacitor C. At the moment switch S_3 is opened, the input signal is sampled and held on the capacitor C. Then switch S_1 is closed and the reference current I starts discharging the capacitor until the output signal of the integrator reaches the threshold voltage V_t. During the discharge time pulses are counted in the MSB counter which is able to store a maximum of 255 pulses. However, the threshold voltage V_t applied at comparator $comp_1$ is larger than the voltage that can be obtained during a full count of the fine counter (255 pulses) and integrating a current $\frac{I}{256}$ on the capacitor C. This threshold voltage is not at all critical, as will be explained later.

After comparator $comp_1$ detects the threshold voltage V_t, switch S_1 is opened and switch S_2 is closed. At the same time the fine counter starts counting clock pulses until comparator $comp_2$ detects zero. If the number of clock pulses applied to the fine counter is larger than the number it can store (in this case 255 pulses), then a carry is generated which is applied to the coarse counter and increases the count of this counter with one count. In this way an automatic adjustment of the threshold voltage V_t is obtained. At the output of this system a 16-bit digital number is obtained that corresponds with the analog input signal. The speed of this system is increased with a factor 256 divided by 2 equals 128 times. Using a very high counting clock,

it is possible to obtain a 16-bit A/D conversion with a conversion speed of about 44 kHz.

In Figure 5.6 the output signal of the sample-and-hold amplifier/integrator as a function of time is shown. The coarse and fine discharging period are

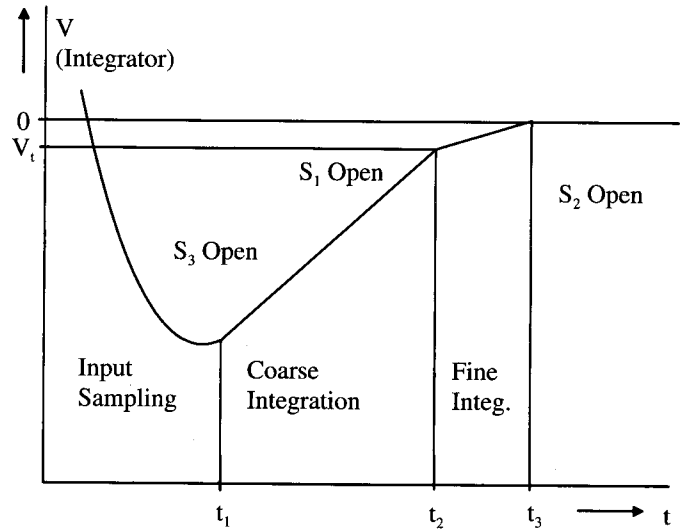


Figure 5.6: Output signal of the sample-and-hold/integrator amplifier

clearly distinguishable in the figure.

5.4.1 Accuracy analysis of the dual ramp A/D converter

In Figure 5.7 the output signal of the sample-and-hold amplifier/integrator is shown. Note that the coarse current value is equal to $I + \frac{I}{255}$ and the fine current value is equal to $\frac{I}{255}$. This construction is used because a large current can be switched better at high speeds than a small current. This means that $\frac{I}{255}$ is always switched to the integrator. The ratio between the currents is 1 to 256 which is required in this system.

Suppose that the current $\frac{I}{255}$ has an accuracy of $(1 - \delta)$; then after a full count of the fine integrator the error between the coarse current and the full fine integrated current value must be smaller than k LSB or:

$$I + \frac{I}{255} \times (1 - \delta) - 256 \times \frac{I}{255} \times (1 - \delta) \leq k \times \frac{I}{255}, \qquad (5.4)$$

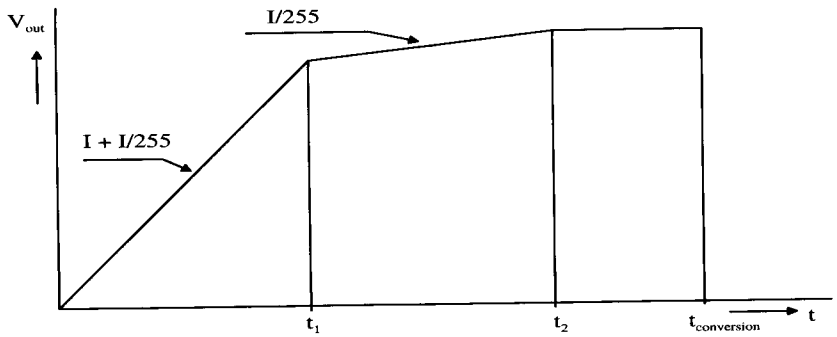


Figure 5.7: Styled output signal of the sample-and-hold/integrator amplifier

or

$$\delta \leq \frac{k}{255}. \tag{5.5}$$

In a 16-bits system a matching between the coarse and fine discharge currents better than 0.2 % is needed to obtain $\frac{1}{2}$ LSB differential linearity.

The accuracy with which the currents must be switched can be determined. Suppose that the clock time $t_0 = \frac{1}{f_{clock}}$, then with a time uncertainty in switching the current I of δt we obtain in case the fine full-scale integrated value must be smaller than k LSB error:

$$I \times (t_0 + \delta t) + \frac{I}{255} \times t_0 - 256 \times \frac{I}{255} \times t_0 \leq k \times t_0 \times \frac{I}{255}, \tag{5.6}$$

or

$$\delta t \leq \frac{k}{255} t_0. \tag{5.7}$$

With $t_0 = 40$ nsec and k = $\frac{1}{2}$ LSB we get $\delta t = 80$ psec.

5.5 Successive approximation converter system

The architecture of a successive approximation analog-to-digital converter is shown in Figure 5.8 The basic converter consists of a comparator stage (Comp.), the successive approximation register (SAR) and the digital-to-analog converter. A sample-and-hold and an anti-alias filter are added to limit the maximum analog input frequency and to convert the continuous time input signal into a discrete time signal. At the beginning of the conversion the MSB is switched on and the input signal is compared to the

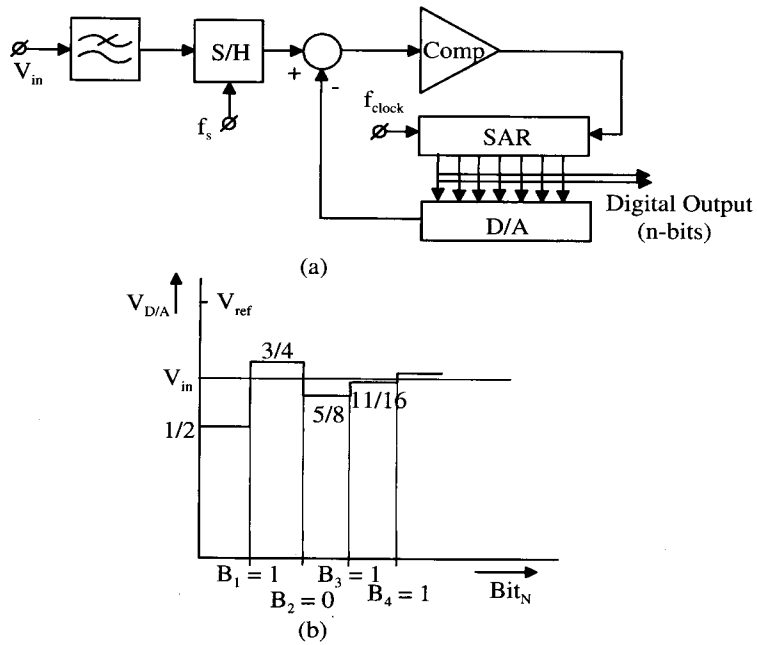


Figure 5.8: Basic successive approximation A/D converter

output signal of the D/A converter. When the input signal is larger than the output signal of the D/A converter, then the MSB remains on and the next bit is switched on and a comparison will be performed. A bit by bit operation is performed in this system to bring the D/A output signal within 1 LSB to the time discrete input signal. In the lower part of fig. 5.8 the conversion procedure as a function of bit weighting is shown. The output value in the figure equals 1011. A complete conversion in this system requires N switching and comparison operations to convert the input signal into a N-bit digital output value. The conversion time equals:

$$T_{conversion} = N.T_{settling}. \tag{5.8}$$

The settling time is defined as the time required to settle within $\frac{1}{2}$ LSB of the D/A converter. The linearity and accuracy of this system depends on the D/A converter.

5.5.1 Successive approximation A/D converter examples

A block diagram of a practical A/D converter system is shown in Figure 5.9 [155]. The most important parts are the successive approximation logic,

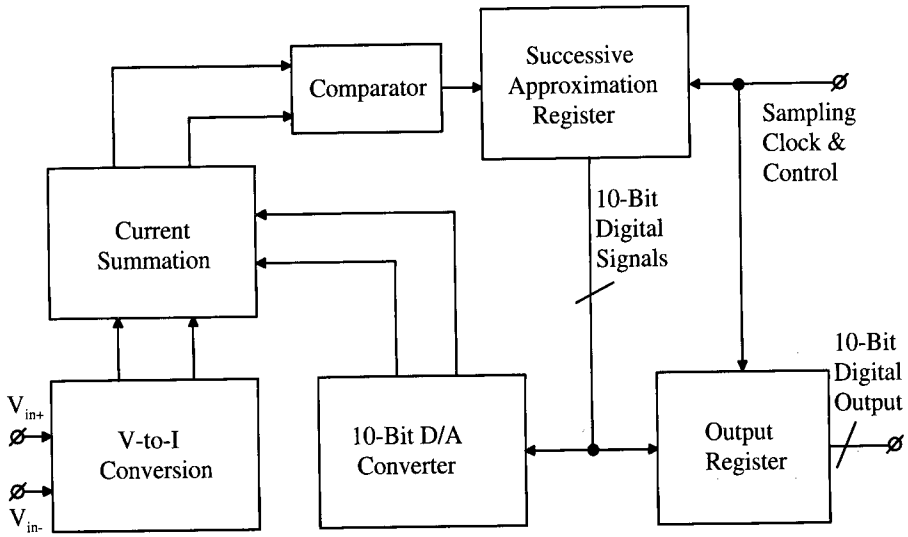


Figure 5.9: MOS only 10-bit SAR A/D converter architecture [155]

the 10-bit D/A converter with the reference current source, the current subtracter, the comparator circuit and the input voltage-to-current converter. The digital data are stored in the output register. In a successive approximation converter two main parts determine the accuracy and linearity of the system. First the digital-to-analog converter will be discussed followed by the current subtracter circuit. A standard comparator circuit can be used, while the successive approximation logic can use addressable latches to perform the step-by-step conversion algorithm. The input voltage-to-current converter uses an accurate source degenerated differential stage with additional operational amplifiers to obtain the required conversion accuracy.

5.5.2 Digital-to-analog converter

The digital-to-analog converter used in this architecture uses CMOS devices to obtain a binary weighted current network. This converter is shown in Fig. 5.10. From the 10-bit D/A converter only a 4-bit implementation is shown. Extending this circuit diagram into a 10-bit scheme does not add extra information. The input current (in this example 16I) is divided into

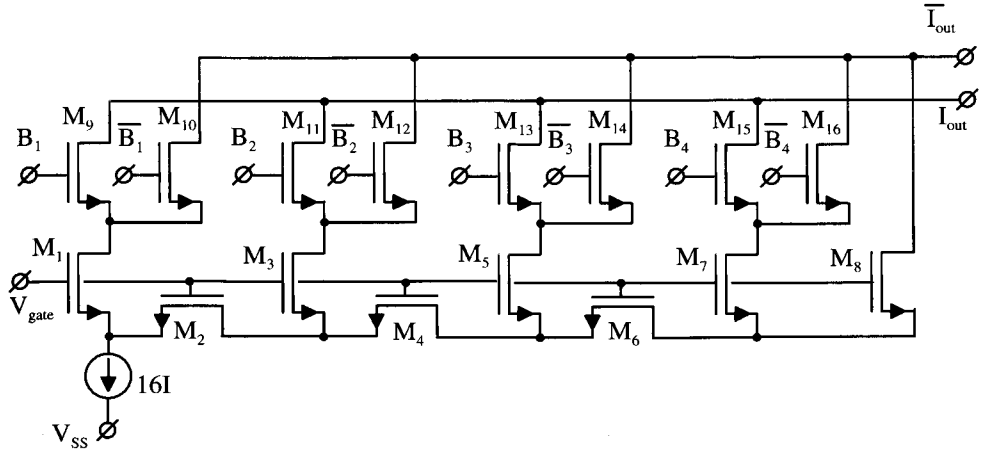


Figure 5.10: MOS only 10-bit D/A converter architecture

two 8I current parts using transistors M_1 and M_2. The output current of the first divider is applied to the second divider consisting of transistors M_3 and M_4 to obtain the second output current 4I. In the following stages the same current division takes place resulting in output currents 2I and I finally. At the end the extra current I is applied to the fixed not used output terminal $\overline{I_{out}}$. The switches that control the DAC currents use differential control signals B_1, B_2, B_3 and B_4 respectively and are high in case these currents are required at the output terminal I_{out}. If these currents are not required then the inverted control signals supply the currents to $\overline{I_{out}}$. At the output a constant level is required to overcome the problem that the current division accuracy determined by transistors M_1 to M_8 is influenced by the reconstructed output signal. This is an important part of the current subtracter circuit. Furthermore the size of the division transistors determines the overall accuracy of the system. In the given example an overall accuracy of 12-bits has been obtained. As has been discussed before this D/A converter works fine in case the division transistors are operated in saturation mode or in case they are in the triode region.

5.5.3 Current subtraction circuit

The current subtracter circuit is shown in Fig. 5.11. The system consists of two differential improved common gate stages having a very low input impedance. The DAC input current is applied at DAC_{in1}, while at DAC_{in2} a dc current is applied required for compensation. The operational amplifiers

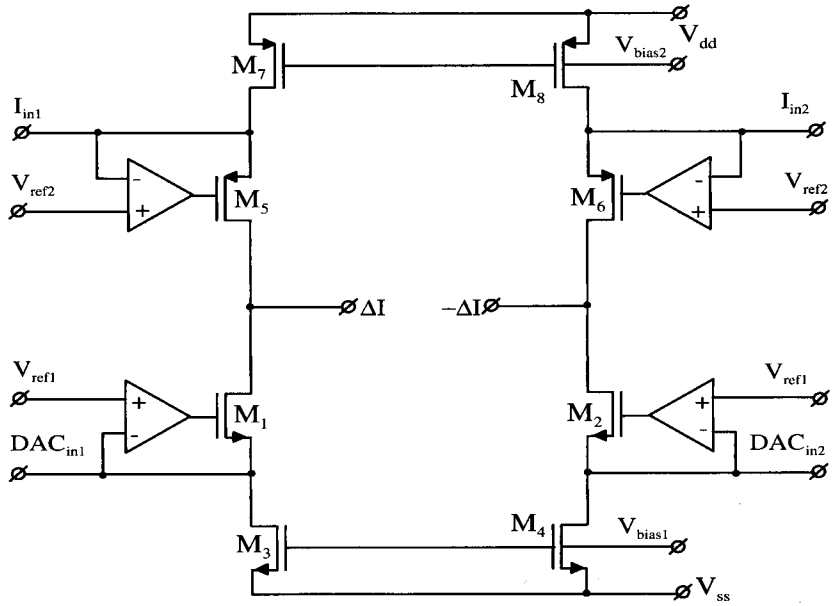


Figure 5.11: Current subtraction circuit diagram [155]

shown in the circuit diagram reduce the input impedance of the system from $R_{in} = \frac{1}{g_{m1,2}}$ into $\frac{1}{A_0 g_{m1,2}}$, with A_0 the low frequency gain of the operational amplifiers. The input signal is differentially applied at terminals I_{in1} and I_{in2}. Again the operational amplifiers with transistors M_5 and M_6 reduce the input impedance to a very low value. At the same time the operational amplifiers increase the output impedance in the drains of M_1, M_5 and M_2, M_6 to a very large value. The output impedance increases roughly with the factor A_0. This means that the error currents ΔI and $-\Delta I$ generate a large voltage across the high output impedance of this stage. This results in a large gain before comparison takes place. The voltages V_{ref1} and V_{ref2} determine the dc bias levels for the D/A converter input current and the signal input currents. In table 5.1 the specifications of a practical converter using this architecture are shown.

5.5.4 Micropower successive approximation A/D converter

An example of a micropower successive approximation A/D converter is shown in reference [156]. The important part of this design is the digital-to-analog converter and the current subtracter circuit. The architecture is identical to the previous system. In Fig. 5.12 the D/A converter architecture

Resolution	10 bits
Conversion Speed	200 ksample/s
Core area	1490x1446 μm^2
ENOB @ 10 ksample/s	9.8 bit
ENOB @ 100 ksample/s	9.4 bit
ENOB @ 200 ksample/s	9.1 bit
Power dissipation	2.4 mA
Power Supply	5 V
Process	1 μm Single Poly CMOS

Table 5.1: 10-bit A/D converter data [155]

is shown. In the digital-to-analog converter segmentation in combination

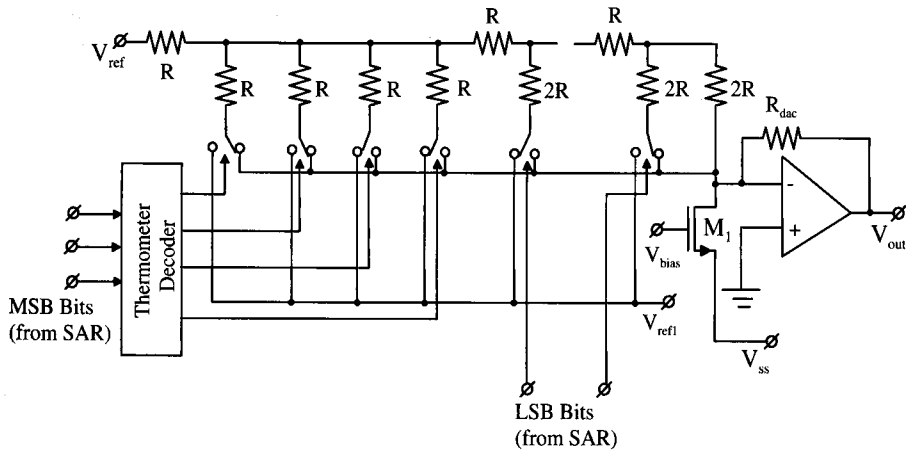


Figure 5.12: Micropower D/A converter architecture [156]

with an R/2R resistor network is shown. The segmented section is driven by the segment decoder. This segmentation is used to insure monotonicity of this converter, while the R/2R network reduces the total amount of elements to a practical applicable size. In this system a 3-bit segmentation is used. Note that not all segmented resistors have been drawn in this circuit diagram. Then a 5 to 7 bit binary weighted R/2R network completes the D/A converter. At the output of the network an operational amplifier is shown. This amplifier guarantees the output level after the bit switches to be at ground level. The bit switches have to be designed in such a manner

that equal voltage drops across the switches are generated to avoid accuracy problems. Furthermore a DC bias current via transistor M_1 is applied to the system to obtain a proper dc biasing adjustment. The R_{dac} determines part of the gain in the subtracter/comparator chain. The successive approximation logic drives the MSB and LSB bit switches. Because of the segmentation more clock pulses are needed to obtain a conversion. In a full binary weighted 10-bit system only 10 clock cycles are required while in this system with a 3-bit segmentation the total amount of clock cycles increases to 7 plus 7 = 14 clock cycles. This can be seen as a disadvantage of this system.

5.5.5 Current subtracter/comparator circuit diagram

The current subtracter and comparator circuit diagram are shown in Fig. 5.13. In this system again a single ended D/A converter input and signal

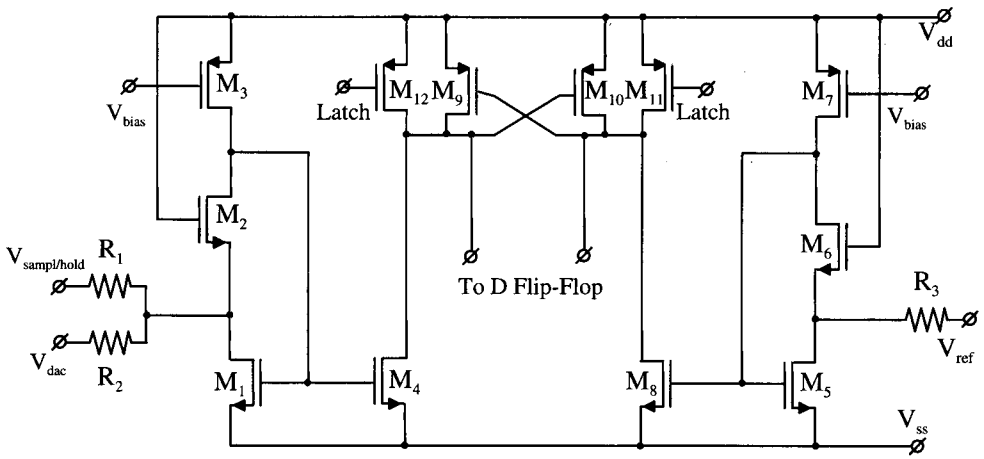


Figure 5.13: Current subtracter/comparator circuit diagram [156]

input is used. Via resistor R_1 the signal from an input sample-and-hold amplifier is applied to the converter, while the digital-to-analog converter signal is applied to the current subtracter via resistor R_2. This resistor is shown as the replacement of the complete D/A converter from Fig. 5.12. The input impedance at the connection of resistors R_1 and R_2 is low because of the applied feedback loop via common gate transistor M_2. At the drain of M_2 a part of the input signal appears. This current is converted into a voltage across the high output impedance of M_2 and M_3. This output is connected to the gate of the current mirror M_1 and M_4. This feedback

loop forces the input current to flow through M_1 and thus M_4 to obtain the current difference between the input signal current and the D/A converter current. The input voltage swing at the source of M_2 is reduced by the gain of the feedback loop consisting of M_1 with the high output impedance of M_2 and M_3. Via resistor R_3 a compensating bias current is applied to the system using an identical current mirror with feedback loop consisting of transistors M_5 to M_8. The difference between the input current and the dc bias current is applied to the comparator stage consisting of M_9 and M_{10}. This stage has been in reset mode when M_{12} and M_{13} are switched on. Then the drains of M_4 and M_8 are connected to V_{dd}. The output signal of the comparator is applied to a D flip-flop to freeze the comparator data. The data of a practical implemented 8-bit converter is shown in table 5.2.

Resolution	8 bits
Conversion Speed	50 ksample/s
Core area	1.8x1.8 m^2
DNL	0.47 LSB
INL	1.14 LSB
Input swing	850 mV
ENOB @ f_{in} = 1 kHz	7.9 bit
Power dissipation	340 μW
Power Supply	1 V
Process	1.2 μm CMOS

Table 5.2: 8-bit A/D converter data [156]

5.5.6 12-bit switched capacitor successive approximation converter

The architecture of a 12-bit non-calibrated switched capacitor successive approximation analog-to-digital converter is shown in Fig. 5.14 [157]. The digital-to-analog converter used in this successive approximation converter combines a binary weighted capacitor main D/A converter with a resistive division sub D/A converter. The binary weighted capacitor network is used as the sample-and-hold capacitor in the system. Switches S_3 short the binary weighted capacitor network during reset. Then during sampling mode, switches S_2 and S_1 are closed. At that moment the input signal is sampled on the D/A capacitors that are all connected together. After sampling the input signal, then the charge redistribution takes place using the reference

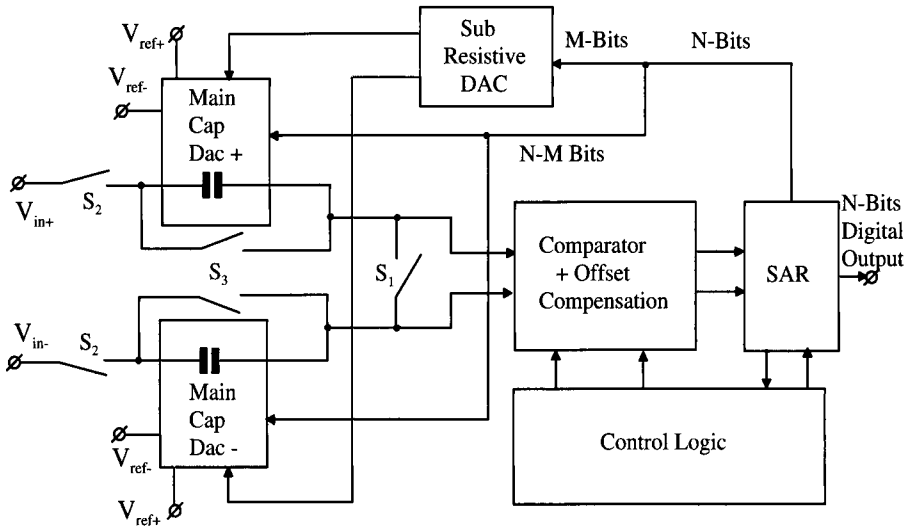


Figure 5.14: Switched capacitor 12-bit successive approximation A/D converter architecture [157]

voltages V_{ref+} and V_{ref-}. This is done using the successive approximation algorithm. The offset of the preamplifier in the comparator uses an auto zero cycle to avoid accuracy problems during the charge redistribution and comparison cycle. With the auto zero setting the offset of the 12-bit system can be made small avoiding overrange problems in case a comparator shows large offsets. This maximizes the input signal range with respect to the supply voltage in the system. The combination of a binary weighted capacitor D/A converter with a resistive sub-D/A converter gives a good optimum with respect to die size and system performance. In Fig. 5.15 the basic combined D/A converter is shown. In this circuit diagram only a 6-bit binary weighted capacitor D/A converter with a 6 bit resistive sub D/A converter is shown. The sub D/A converter uses a resistor string shown as M-Bit D/A converter. When in this system the input signal is sampled on the capacitor array, then this charge is compensated for to obtain again an identical output signal after the charge redistribution has taken place. This means however, that an input buffer at the input of the converter is needed to obtain a constant input impedance of this system. Such a buffer might be difficult to design. The results of a 12-bit implementation are shown in table 5.3. The data given in the table shows a converter without an input buffer. Furthermore it must be noted that the given examples of successive

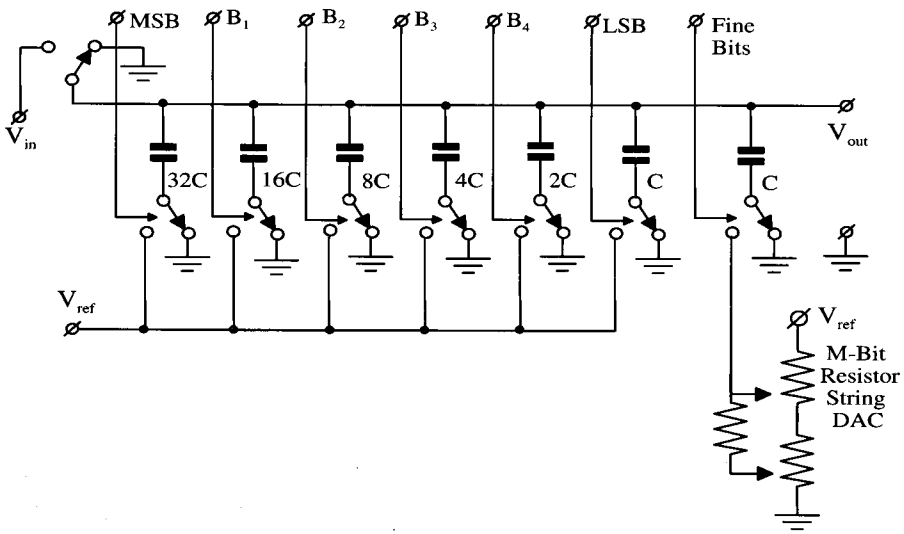


Figure 5.15: C2C capacitor/resistor combined D/A converter architecture

Resolution	12 bits
Conversion Speed	1 Ms/s
Core area	1.5 m^2
Input capacitance	21 pf
DNL	0.5 LSB
INL	0.5 LSB
Input swing	850 mV
ENOB @ $f_{in} = 1$ kHz	11.6 bit
Power dissipation	15 μW @ 5 V
Power Supply	3-5.5 V
Process	0.6 μm CMOS

Table 5.3: 12-bit A/D converter data [157]

approximation converters are used as examples only. Using more advanced technologies an improved performance of these architectures is expected.

5.6 Algorithmic A/D converter

A block diagram of a cyclic (algorithmic) A/D converter is shown in Figure 5.16 [34, 86, 87]. In a cyclic system the output code is generated in

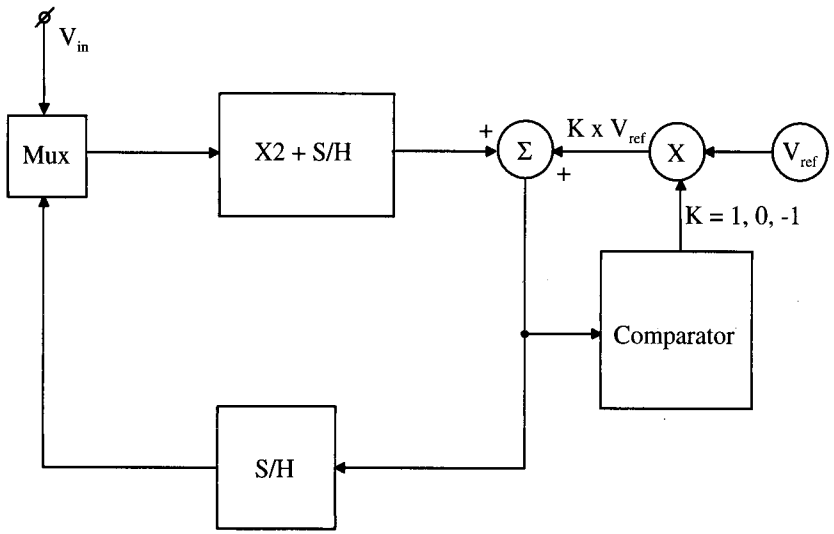


Figure 5.16: Algorithmic A/D converter system [86]

a serial way. In every cycle the comparator, subtracter, and multiply by two amplifier are used. A very compact converter system is obtained at the cost of a larger conversion time (p times the time of one cycle operation). The system consists of a times two differential amplifier with a built-in hold function, a summer/subtracter circuit, a comparator, a reference source, and a sample-and-hold amplifier. The multiplexer at the input switches the input of the sample-and-hold amplifier between the input terminal and the output of the summer/subtracter. The conversion starts by sampling the input signal V_{in} and amplifying this signal with an accurate factor of two. The signal is then applied to the comparator which subtracts or adds the reference voltage V_{ref} to the two times amplified input signal. A reference source operation is performed when the comparator detects a signal larger than zero. The positive error signal is transferred to the sample-and-hold amplifier. In the meantime the multiplexer has been switched to the out-

put of the sample-and-hold amplifier. The remaining signal is amplified by the two times amplifier and a reference operation is performed again. This cyclic comparison, subtraction, and signal transfer are repeated, depending on the number of bits with which the converter is operating. A serial code appears at the output of the comparator. The only accurate element in the system is the times two amplifier and the subtracter/summer circuit with the reference source.

In Figure 5.17 a detailed operation of the accurate times two amplifier system is shown. The operation of the system is based on the addition of two

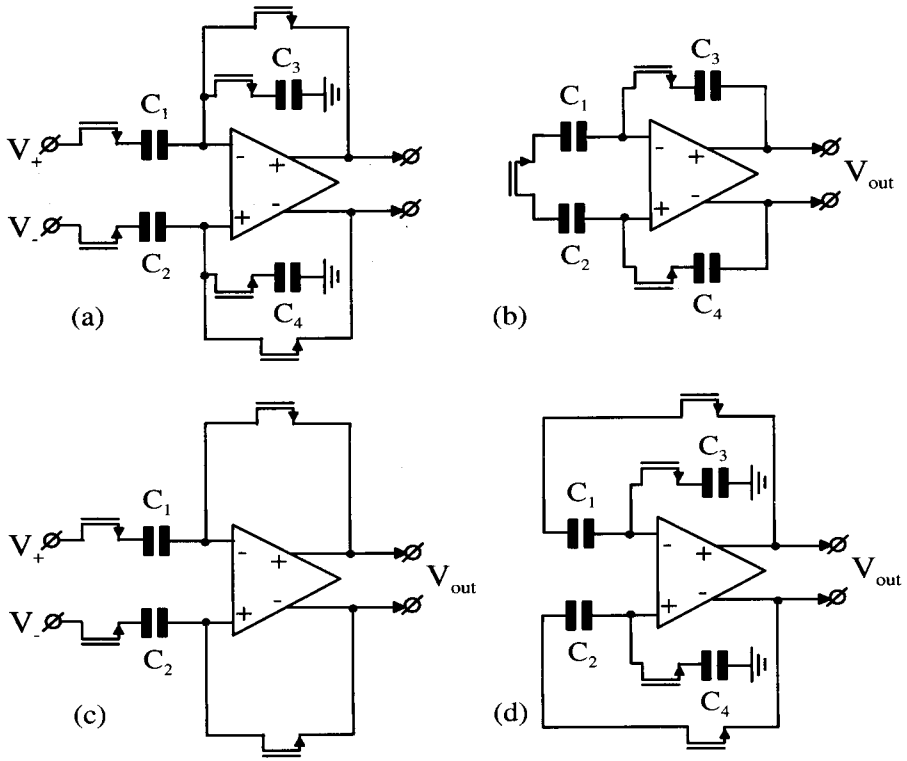


Figure 5.17: Detailed operation of the accurate times two amplifier [86]

sampled signals on two capacitors. In Figure 5.17a the input differential signal is sampled on the capacitors C_1 and C_2, while at the same time the input offset voltage is sampled on capacitors C_3 and C_4. In Figure 5.17b the input signal charge is transferred from capacitors C_1 and C_2 to capacitors C_3 and C_4. The second input sample is taken as shown in Figure 5.17c. Capacitors

C_3 and C_4 are disconnected and therefore do not get any charge. The input sample is stored on capacitors C_1 and C_2. The repeated addition of the two samples is shown in Figure 5.17d. The voltage across C_3 is added to the voltage across C_1 and gives a doubling of the input signal. An identical operation is found for the voltages across C_4 and C_2. The sampling of the signal accurately stores the input voltage on a capacitor, while due to the charge transfer it can be shown that an offset correction occurs. Furthermore, the system is nearly independent of the capacitor mismatching. The differential operation of the system compensates for charge feed-through errors due to the switching operation that is performed in this system. A larger dynamic range can be obtained, while, furthermore, such a system is less sensitive to supply voltage variations. In Figure 5.18 the complete analog part of the A/D converter is shown. Amplifier A_1 with the surrounding switches performs the accurate times two amplification with the subtraction or addition of the reference value. Note that by inverting the reference voltage to capacitor C_5 or capacitor C_6, a subtraction or addition can be performed without loosing accuracy. Amplifier A_2 with capacitors C_7 and C_8 perform an offset independent sample-and-hold amplifier function. Capacitors C_9 and C_{10} with the amplifier perform an accurate comparison with zero. The output signal of the comparator is stored in the output latch and can be transferred as a series output signal of the converter. A single-ended sampling of the input signal is used. No amplification by two is obtained during the sampling of the input signal.

5.7 Cyclic Redundant Signed Digit A/D converter

A cyclic converter that is less dependent on component matching and comparator offset voltages uses the Redundant Signed Digit Coding [71]. The main advantage of this coding is that it gives the option to perform a subtraction as well as an addition. The RSD coding is well known from digital multiplier coding using special algorithms (Booth). Because of the subtraction operation decision, errors introduced by offset in the comparators can be corrected for. In Figure 5.19 the basic implementation of an RSD algorithm is shown. The system consists of a sample-and-hold amplifier, an accurate times two amplifier, a switchable adder-subtracter circuit, and two comparators. The comparison levels P and Q are arbitrary but can best be chosen at half the reference voltage (P = -Q = $\frac{1}{2}V_{ref}$).

The operation of the comparison is shown in Table 5.4. Starting with a

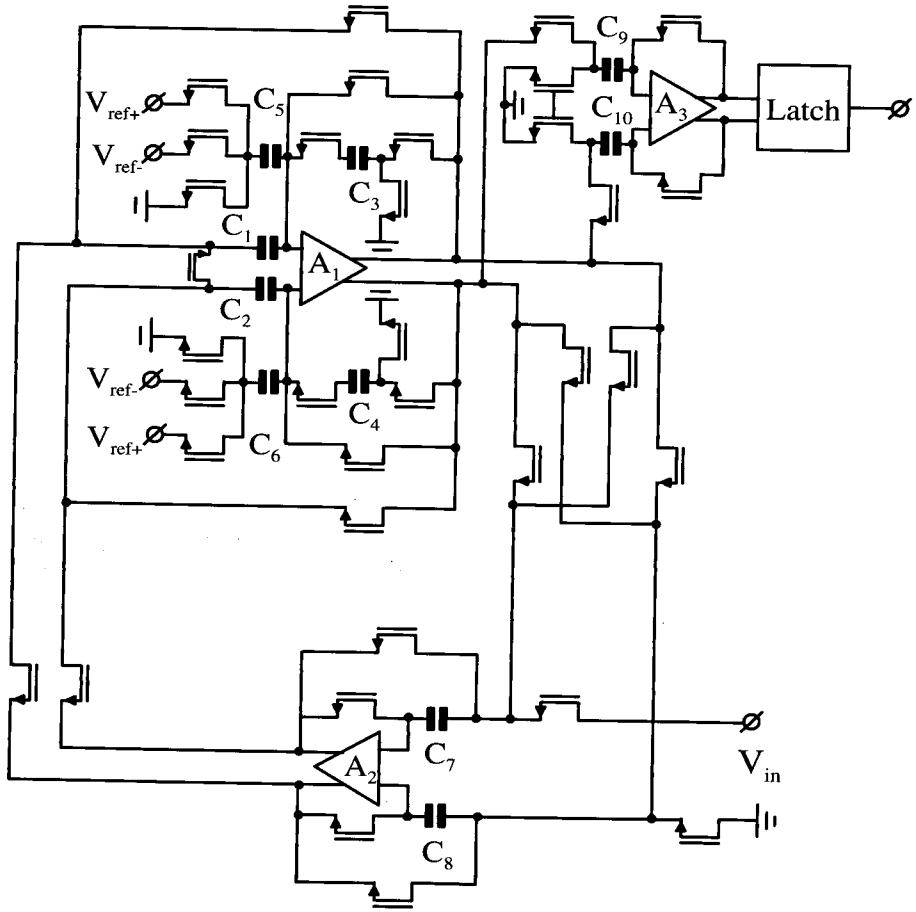


Figure 5.18: Complete analog part of the A/D converter [86]

b^0	b^{00}	b
1	0	+1
0	0	0
0	1	-1

Table 5.4: Signed Digit coding

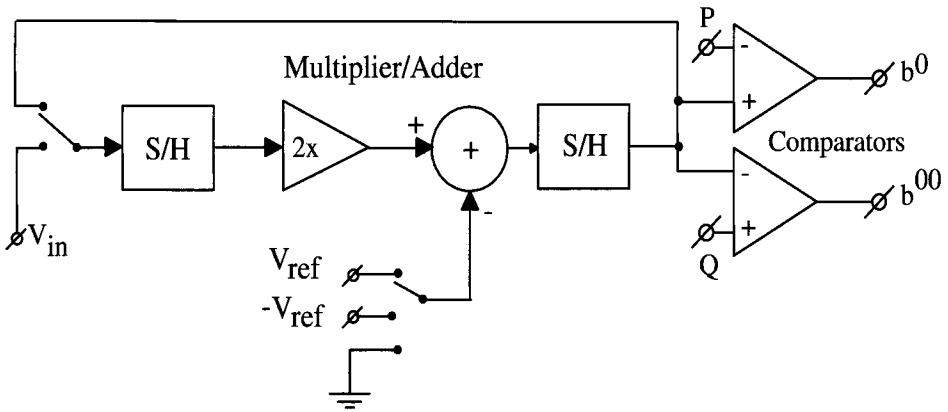


Figure 5.19: Basic RSD converter implementation

sample of the input signal V_{in} in the sample-and-hold amplifier, this signal is amplified by two and compared with the levels P and Q. At the moment the signal is in between of the levels P and Q corresponding to b = 0, then no addition or subtraction of the reference voltage is performed. The signal is amplified by two and again a comparison is performed. At the moment b = -1, then the reference voltage is subtracted and the remainder is amplified by two again to perform a new bit value determination. At the moment b = +1, then a reference voltage addition is performed. The remainder is multiplied by two again and a new comparison takes place. This cycle is repeated until the required amount of serial bits is obtained. Because of this restricted comparison method with the ability to add or subtract a reference voltage from the partial remainders, a comparator offset independent operation is found. The serial output code containing 0, +1 and -1 bits can be converted into a binary-weighted code by the appropriate subtraction operation of the -1 valued bits. In Figure 5.20 a switched capacitor implementation of the system is shown. The circuit consists of an input sample-and-hold amplifier, a multiplier/adder circuit, and the two comparators with appropriate decision levels. In the multiplier/adder circuit a times two operation is performed. Note that only capacitor C_2 has a value 2C while all other capacitors have a value C. The operation starts by closing switch Φ_I and sampling the input signal. Then by sequentially closing switches Φ_A and Φ_B, respectively, the cyclic conversion takes place. Depending on the output of the signed bit b, which is generated according to Table 5.4, the voltages applied to the terminals V_A and V_B are applied according to Table 5.5. The output bits of the comparators are again converted into a binary

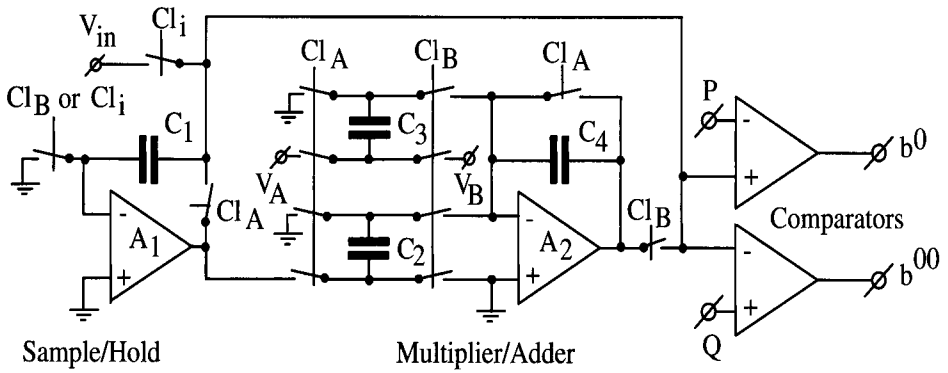


Figure 5.20: Switched capacitor RSD converter implementation

Signed bit b	V_A	V_B	Transfer function
-1	V_{ref}	Gnd	$\hat{V}_x = 2\ V_x + V_{ref}$
0	Gnd	Gnd	$\hat{V}_x = 2\ V_x$
+1	Gnd	V_{ref}	$\hat{V}_x = 2\ V_x$ - V_{ref}

Table 5.5: Switching and operation schemes of converter

code by the appropriate subtraction of the negative values from the output signal. The shown implementation is a simplified schematic of the preferred embodiment of the system. Especially in the switched capacitor CMOS implementation, a differential operation of the circuit is required to minimize the switch feed-through on the overall performance. The only important factor in the system is the times two amplifier.

5.8 Self-calibrating capacitor A/D converter

In Figure 5.21 a block diagram of a self-calibrating A/D converter is shown [73]. The system consists of a 10-bit weighted capacitor D/A converter com-

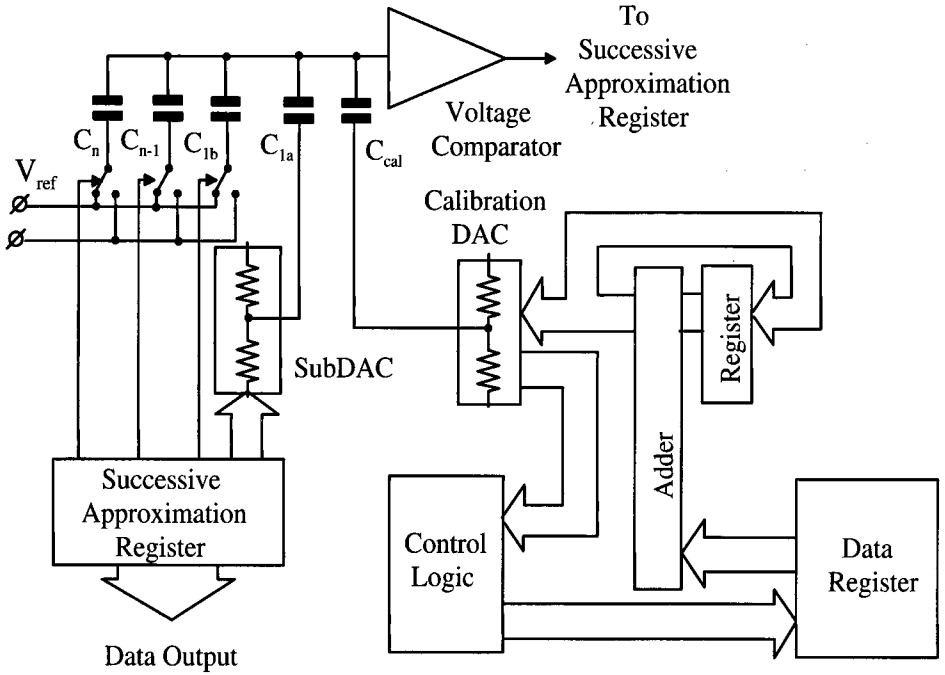


Figure 5.21: Self-calibrating A/D converter [73]

bined with a 5-bit resistive divider sub-D/A converter. A 7-bit calibration D/A converter is used to calibrate the errors from the binary-weighted capacitor D/A converter and the resistive divider sub-D/A converter. The accuracy of a 10-bit binary-weighted D/A converter is so good that only the five most significant capacitor values need to be calibrated to obtain a 15- to 16-bit overall accuracy. The calibration of the main D/A converter

plus the sub-D/A converter is performed by comparing every major carry transition of the main D/A converter. The calibration principle is shown in Figure 5.22. In the first calibration cycle as shown in Figure 5.22(a) the

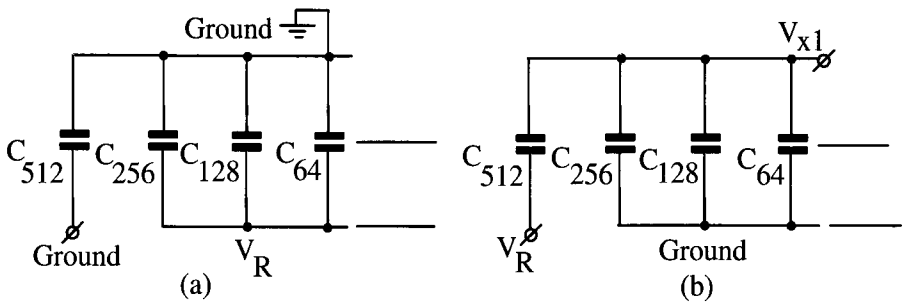


Figure 5.22: C-2C calibration principle [73]

most significant capacitor C_{512} is compared with the sum of the residual capacitor values $C_{residual}$.

$$C_{residual} = C_{256} + C_{128} + C_{64} + ...C_1 + C_1. \tag{5.9}$$

In the ideal case the value of the capacitor $C_{residual}$ is equal to C_{512}. The deviation from the ideal value can be measured by using a charge redistribution technique. This is performed by reversing the reference voltage across the capacitor network. In the left part of Figure 5.22 the reference voltage is applied to the bottom plates of the residual capacitors $C_{256}, C_{128}, ..C_1$ and the voltage across C_{512} is made zero and this capacitor is connected to ground. In the right part of Figure 5.22 ground (GND) and V_R are exchanged. As a result the voltage at terminal V_{x1} in case of ideal matching must be zero. With mismatches in capacitor values a voltage at V_{x1} appears that is a linear measure for the capacitor mismatch. With use of a successive approximation conversion cycle the voltage V_{x1} is measured and the data are stored in a random access memory (RAM). The sub-D/A converter is used during this error search. During subsequent cycles the remaining capacitors of the capacitor D/A converter are calibrated and the errors are stored in the RAM. To overcome problems with noise during calibration, a number of error cycles are averaged. Furthermore, a longer word length in the error correction system is used to avoid the surpassing of the accumulated correction errors of the half LSB linearity error. Usually two extra bits are sufficient. When the calibration cycle is finished, then the normal successive approximation conversion is performed. Every time a bit value is "true,"

then the calibration signal accompanying this bit is called from the memory and via the calibration D/A converter the correction signal is added. In this way it is possible to extend the linearity of a converter into the 16- to 18-bits linearity range. At predetermined time intervals the calibration of the system is repeated and new data are stored in the calibration data register. The only disadvantage of this system is that during calibration the A/D converter is not able to operate. In certain systems this cannot be tolerated.

5.9 Conclusion

In this chapter some basic circuits have been presented. Systems with low conversion speed can use integrators to obtain a high-accuracy voltage-to-time conversion. This time is converted into a digital number by simply counting pulses. Accuracies up to 20 bits are possible. A good compromise between speed and accuracy is obtained by the successive approximation system. Maximum resolution is determined by the bandwidth and the noise generated in the comparator circuits. A practical limitation is about 16 bits with 100 kHz conversion rate. The use of a multi-level comparator increases the speed at the cost of power dissipation and die size. The ease of implementation of sample-and-hold amplifiers results in simple algorithmic analog-to-digital converters. The most difficult part in such a system is the accuracy with which the times two amplification with addition or subtraction is performed. A special Redundant Signed Digit algorithm does not need a low-offset requirement for the comparators.

Finally, self-calibration systems make a circuit less sensitive to component variations; however, during warming up of the system a re-calibration might be needed. A very high accuracy, between 16 to 18 bits, is possible with such a calibration system. However, during this calibration cycle the system is not able to produce an output signal. This might be a large drawback for many systems applications.

Chapter 6

High-resolution D/A converters

6.1 Introduction

High-resolution monolithic D/A converters are subject to growing interest due to the rapidly expanding market for digital signal processing systems. An example of such a market is digital audio. The large dynamic range of a digital audio system requires converters with resolutions from 16 to 24 bits. Monolithic converters with such a high linearity are difficult to design and require special circuit configurations. The most simple types of D/A converters are obtained with pulse-width modulation systems. These systems require fast logic circuits. In a pulse-width D/A converter structure an output low-pass filter reconstructs the analog signal and removes the modulation signal. Maximum speed of these types of converters is limited to the kHz range or low Mega Hertz range. The advantage of these systems is the small amount of accurate components that are needed in a practical implementation.

In integrating types of converters, an analog signal is reconstructed by integrating a current during a signal-dependent time. The output signal of the converter is applied to a sample-and-hold amplifier. The sample-and-hold amplifier reconstructs the stepped quantized waveform. With a low-pass filter the final analog output signal is reproduced. The sample-and-hold amplifier and the low-pass filter can be combined to obtain a first order filtering.

With matched components (resistors, capacitors, or transistors) it is possible to directly convert a digital number into an analog quantized signal. However, the limited accuracy with which components can be matched maximizes the resolution to about 10 to 12 bits. In that case a converter still fulfills the linearity specification. Modifying the design can result in *monotonic by design* types of converters that do not have a $\frac{1}{2}$ LSB linearity specification but may have an excellent differential nonlinearity specification.

In this Chapter a special circuit configuration called "Dynamic Element Matching" will be described. This technique combines an accurate passive current division with a time division method to obtain the very high accuracy needed in monolithic converters without using trimming techniques. This system is, furthermore, insensitive to element aging and remains accurate over a large temperature range and with varying elements. However, filtering capacitors are needed to reduce the ripple on the output currents introduced by the interchanging technique. In references [62, 1, 2] examples of circuits realized in practice are given.
Furthermore "Dynamic Element Matching" is applied in very high resolution sigma-delta converters. In these systems a randomization of the interchanging algorithm is used. The idea here is to randomize the errors introduced by the mismatch between currents or resistors and have the spectral components transferred outside the signal band of interest. In this way no filtering capacitors are needed and still the advantages of this method are obtained.

An improved MOS solution of "Dynamic Element Matching" will be described. This technique uses a continuous current calibration using an extra current source that is taken out of the current reference network and then will be calibrated and inserted again. This current calibration technique results in a very high matching accuracy without the need for an extra filtering operation to reduce a calibration ripple.

A third self-calibration scheme is shown, which uses an additional cycle to calibrate the complete converter. During calibration, however, it is not possible to use the converter effectively in a system.

6.2 Pulse-width modulation D/A converters

In Figure 6.1 an example of a pulse-width D/A converter is shown. The system consists of a digital buffer in which the input data are stored. These

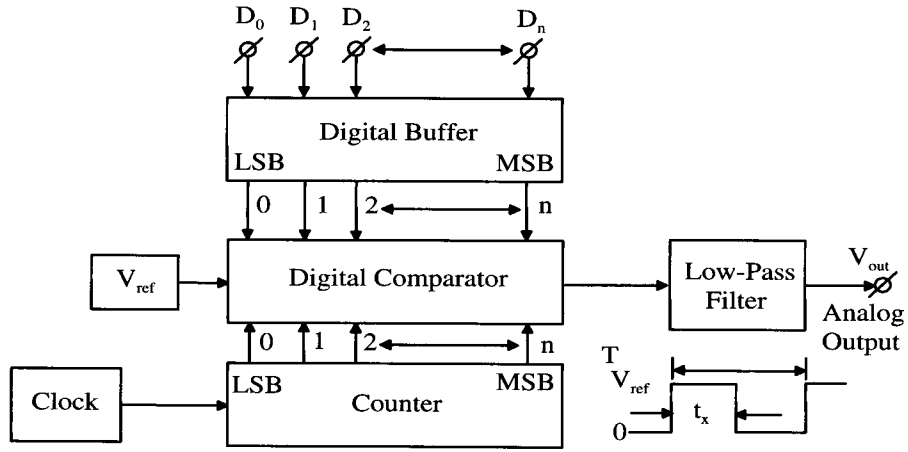


Figure 6.1: Pulse-width modulation D/A converter

data are compared with a ramp signal that is generated by a counter operating with a clock frequency f_{clock}. The digital comparator compares the buffer data with the ramp signal generated by the counter. When the counter signal is smaller than the buffer signal, then the output of the comparator is high. At the moment the counter signal is equal or larger than the buffer signal, then the comparator output is low. The output signal of the converter is a pulse-width modulated signal. This signal is filtered by a low-pass output filter and the analog signal is reconstructed again. A simple calculation gives for the output signal:

$$V_{out} = \frac{t_x}{T} \times V_{ref}. \tag{6.1}$$

Here t_x is the time that the comparator output signal is high and T is the repetition time of the ramp signal. V_{ref} is the reference signal that is modulated by the comparator output signal. Moreover, it can be shown that the conversion time is equal to:

$$T_{conversion} = \frac{2^n}{f_{clock}}. \tag{6.2}$$

Here n is the number of bits of the counter. f_{clock} is the frequency of the counter clock.

A disadvantage of this system is the low repetition rate of the pulse-width modulated signal. To reconstruct the analog output signal a low-pass output filter with a large stop-band attenuation is required. The stop-band

attenuation must be at least equal to the dynamic range of the converter.

In Figure 6.2 a system implementation is shown that has the ability to randomly generate the high level signals of the comparator over the whole conversion period [18]. From the figure, which uses exactly the same building

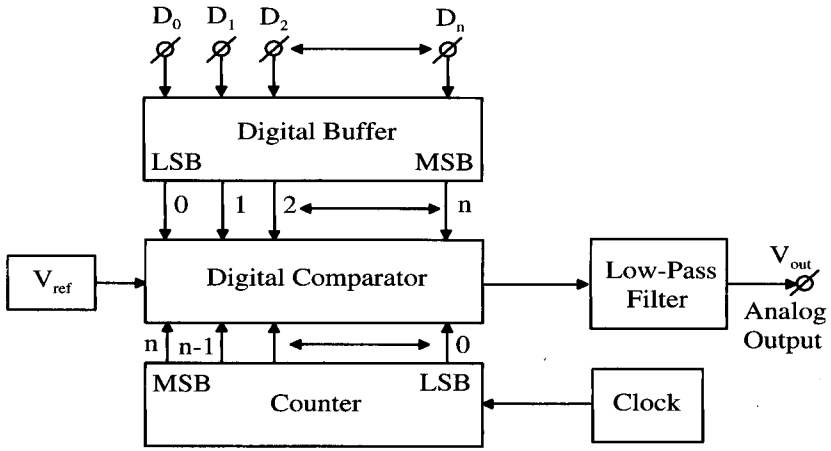


Figure 6.2: Reverse comparing pulse-width modulating D/A converter

blocks, it can be seen that the most significant bits of the digital buffer and the least significant bits of the ramp signal generated by the counter are compared. As a result of this operation the output pulse of the comparator is better randomized during the conversion period T. Around the middle range of the converter the frequency components are shifted to a higher frequency band. As a result the requirements of the output filter can be reduced. Table 6.1 shows an example of this randomization for a 3-bit code 110.
From the table the randomizing of the comparator output in the case of the reverse bit-weight connected counter can be easily distinguished.

6.3 Integrating D/A converters

In Figure 6.3 an example of a single slope D/A converter is shown [61]. The system consists of digital input latches that store the input information, a digital comparator, and a counter operating from a crystal controlled oscillator. In this part of the circuitry the input data are converted into a time signal which is the output of the digital comparator. The comparator output

Buffer	Reverse Counter	Normal Counter	Reverse Comparator	Normal Comparator
	0 0 0	0 0 0	S	S
	0 0 1	1 0 0	L	S
	0 1 0	0 1 0	S	S
1 1 0	0 1 1	1 1 0	L	E
	1 0 0	0 0 1	S	L
	1 0 1	1 0 1	L	L
	1 1 0	0 1 1	E	L
	1 1 1	1 1 1	L	L

Table 6.1: Comparison Table

Notation:
S = Smaller
L = Larger
E = Equal.

signal switches the reference current I to the integrator which converts the current signal into an analog output voltage across the capacitor C. At the end of the integration cycle the sample-and-hold using an operational amplifier and feedback elements R_1, R_2, and C_2 samples the final analog value of the converter and holds the signal during the time the next conversion is performed. Note that during the hold mode of the sample-and-hold amplifier the resistor R_2 remains in parallel with the hold capacitor C_2. A first order output filtering is combined with the hold operation in this system. Finally the output signal can be applied to a low-pass filter that reconstructs the analog output signal. At the start of a conversion the integrator is reset by closing switch S_2. The sample-and-hold amplifier remains in the hold mode. When an input data word is loaded into the buffer, the reset switch S_2 is opened and the reference current I_{ref} starts charging the capacitor C during the time the counter value is smaller than the buffer value (S_1 is closed). At the moment the comparator detects a counter value which equals the buffer value, then the reference current is switched off (S_1 is opened), and the integrator remains at the converted analog value. The sample-and-hold amplifier samples the output signal of the integrator (switch S_3 is closed). When the next start conversion comes, the sample-and-hold amplifier is switched in the hold mode (switch S_3 is opened), storing the analog infor-

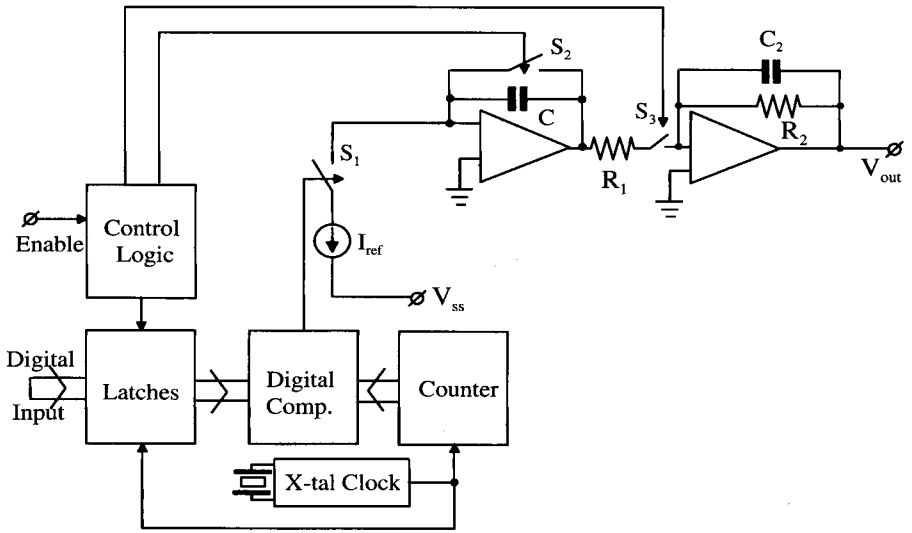


Figure 6.3: Single-slope integrating D/A converter

mation during the time the next digital-to-analog conversion is performed. The first order filter consisting of R_2 and C_2 already filters out a part of the sampling images. The conversion speed of this systems depends on the number of bits that must be converted and the maximum clock speed that can be applied to the system.

$$T_{conversion} \approx \frac{2^n}{f_{clock}}. \tag{6.3}$$

Here f_{clock} is the frequency of the crystal clock.

To increase speed the input data word can be split-up into a coarse (MSB)and fine value (LSB). At the same time the reference currents are split-up into two weighted values which correspond with the splitting of the coarse and fine digital values [29].

In Figure 6.4 a simplified form is shown. In this system the number of clock pulses to obtain a full coarse and fine counter is reduced. In a 16-bit system using an 8-bit coarse and an 8-bit fine split-up a 256 times larger conversion speed can be obtained compared to the circuit of Figure 6.3 having a 16-bit resolution.

A conversion starts with the reset of the integrator by closing switch S_3.

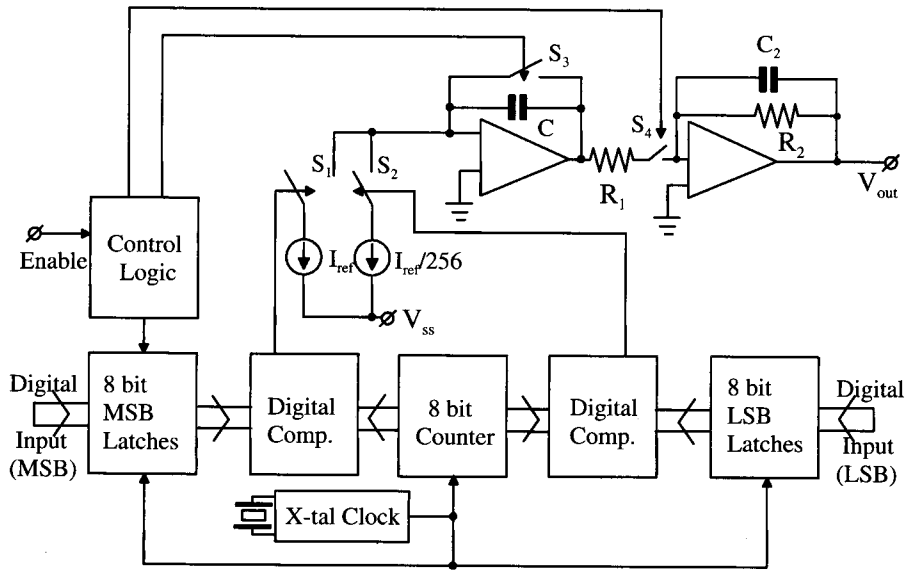


Figure 6.4: Dual-ramp D/A converter system

At the same time the coarse and fine digital data are loaded into the input latches. Then switch S_3 is opened and the counter, which is reset to zero, starts counting. As long as the counter data are smaller than the input data, the comparator outputs are closing switches S_1 and S_2, respectively. The reference currents I_{ref} and $\frac{I_{ref}}{256}$ are charging the integrator capacitor C. This charging stops at the moment the contents of the counter is larger than the coarse or the fine input data. Finally, the analog data are sampled by the succeeding sample-and-hold amplifier consisting of an operational amplifier with feedback elements R_1, R_2, and C_2. The sample-and-hold circuit is switched into to hold mode during the time a new sample is loaded and converted into an analog value. Again R_2 and C_2 form a first order low-pass filter that filters out the sampling images of the signal. An output low-pass filter can be used to reconstruct the analog signal further.

A disadvantage of single integrator systems is that full scale accuracy is dependent on the reference current value I_{ref} and the integrator capacitor C. Furthermore the accuracy with which the switches can be operated determines the linearity of the system. Dynamic performance is determined by the performance of the sample-and-hold amplifier.

6.4 Current weighting using ladder networks

Different systems using ladder networks to obtain an accurate current weighting will be discussed. These ladder networks are simple to implement in integrated circuits. Furthermore, the very well matched value and thermal tracking of components on the same die improve the overall performance of the system.

6.4.1 *R*-2*R* ladder network

An *R*-2*R* ladder network with terminating transistors to generate binary weighted currents is shown in Figure 6.5. This system is a general solution to the problem of generating binary weighted currents. The good matching and excellent thermal tracking of integrated resistors is an important design criterion of this circuit. The circuit consists of equal resistors with a value *R*.

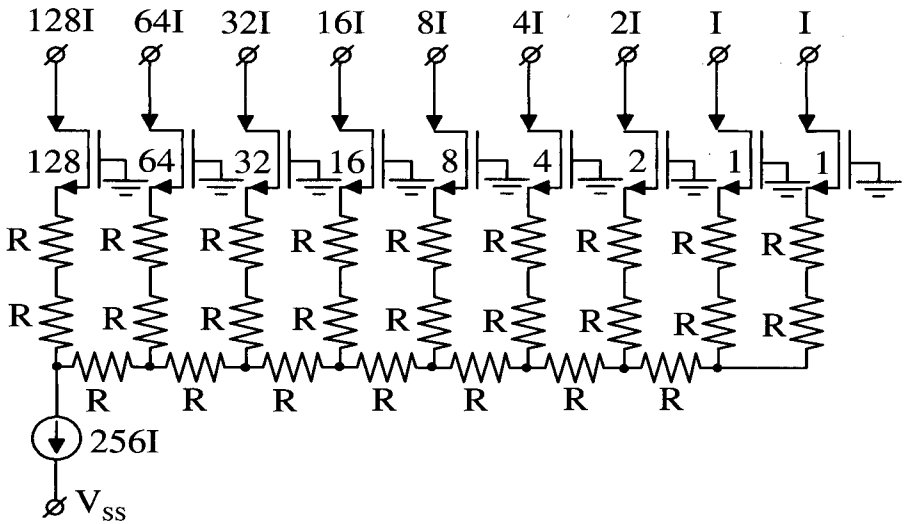


Figure 6.5: R-2R ladder network D/A converter system

The 2*R* resistor is formed by connecting two resistors in series to obtain the best resistor matching. Because the output currents are binary weighted, the gate-source voltages of the terminating transistors will decrease if no special measures are taken. From Figure 6.5 it can be seen that the transistor sizes decrease by a factor two every time the current is reduced. An equal voltage at the sources of the current source transistors is needed for an accurate operation of the *R*-2*R* ladder network. The division using such a

network depends on a divide by two voltage division every time a section is added. The voltage drop across the 2*R* resistors decreases with a factor two when the output current decreases with a factor two. At the time a low bit current value is reached, the voltage drop across the resistors is small compared to the gate-source voltage of the transistors. At that moment the resistors do not determine the current division ratio anymore. The current division is then performed by the scaling of the transistors. In practice the current source transistors have a constant current density obtained by the binary scaling of the device size. To improve weighting accuracy the transistor with size 128 consists of 128 equal sized devices in parallel. In sub-micron MOS technology the supply voltage is small and tends to reach the 1 V region. This means that a sufficient voltage drop across the resistors in the *R*-2*R* network between 0.5 and 1.0 V can not be used anymore. Such a large voltage drop across the resistors is needed to make the current division accuracy mainly dependent on the resistor matching. This means that the resistors have to be eliminated and the current source devices must be tailored in such a way that the required matching accuracy is obtained. In practice this means that 10 to 12 bit with $\pm$ 0.5 LSB linearity is the limit of transistor scaling. This limit depends on the technology used.

6.4.2 MOS only binary weighted current network

An example of a binary weighted current network using scaled MOS devices only is shown in Fig. 6.6. The circuit consists of binary weighted MOS

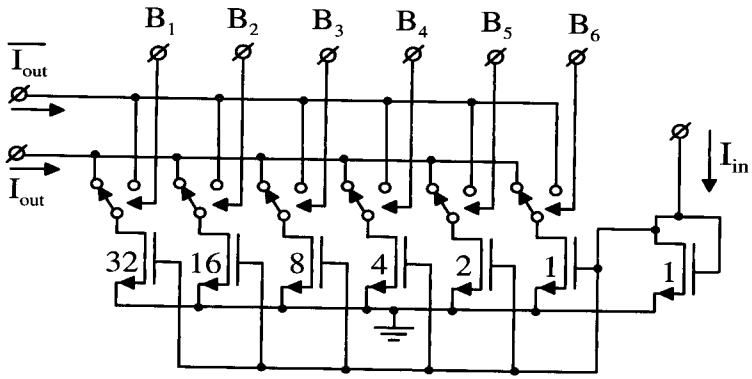


Figure 6.6: MOS only binary weighted current network

devices using parallel connection of the required amount of transistors to get the weighting. At the output of the current sources switches determine the

analog output current depending on the digital input value. A differential output current is obtained. this current can be converted into a voltage using output load resistors. However, to avoid channel length modulation of the current division transistors due to the output voltage developed across the applied load resistor, a differential current to voltage output amplifier is needed. In this way no drain voltage variation due to the output signal is found. The reference current is applied to a MOS diode with size 1 as shown in Fig. 6.6. This input current is multiplied by the sizing of the current sources. An accurate matching is obtained, although the absolute accuracy of the full scale value of the reference network is not guaranteed in this way. In case a high full scale accuracy is required, then the size of the input bias diode must be increased to the same size as the MSB current in the network. In this example a size of 32 is needed. Special layout techniques and dummy devices in the circuit layout must be used to obtain a maximum in accuracy. This will be discussed in the high-speed converter chapter. In case an input current must be divided into binary weighted output currents then the system shown in Fig. 6.7 can be used. As will be

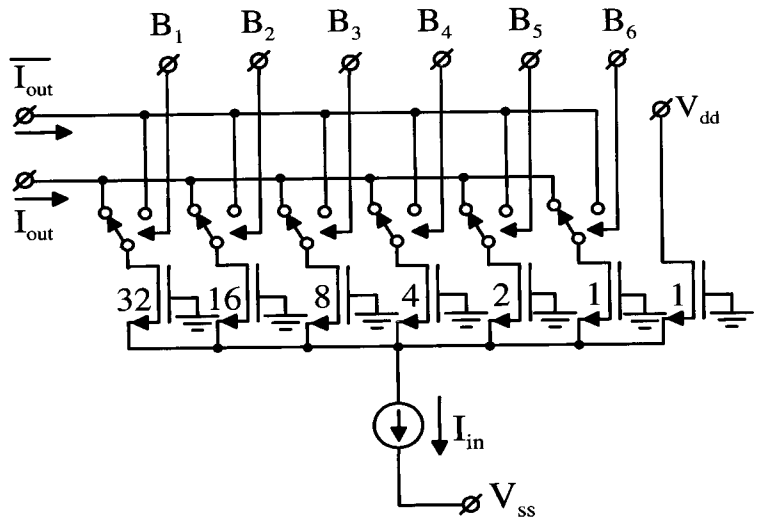


Figure 6.7: Binary weighted current division network

shown later, this system divides the lower bit currents into binary weighted output currents depending on the tail current I_{in} applied to the system. At the output binary weighted currents are obtained, while an extra current with value 1 is required to obtain a good division. This extra current I

could be subdivided again if needed. Such a division system is used in high-resolution converters from which the most significant bit currents are generated using special circuit systems.

6.4.3 MOS R-$2R$ implementation

A different MOS implementation of an R-$2R$ network is shown in Fig. 6.8. In this figure the basic *R-2R cell* is shown with a possible combination with the bit current switch. All transistors in this system are equal. Depending

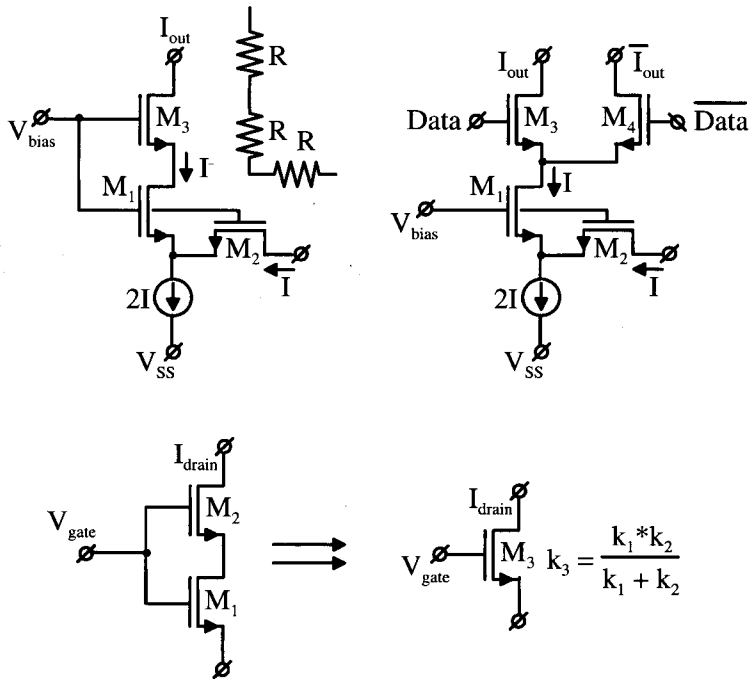


Figure 6.8: R-2R MOS elements

on the input current $2I$, transistors M_1 and M_2 can operate in saturated mode or in triode mode. In saturated mode transistors M_1 and M_2 divide the input current $2I$ into two equal currents I. In this case transistor M_3 acts as a cascode transistor and supplies the output current to the load. At the moment transistors M_1 and M_2 are in triode region, then these transistors can be seen as a resistor with value R. In this case transistor M_3 performs an equal resistor of value R. In this way the R-$2R$ network is implemented and with careful termination an accurate binary weighted current division is obtained. However, it is possible to include the switches

into this R-$2R$ network by adding transistor M_4. At the moment Data is high, then transistor M_3 is used in the network as described before and the output current $I_{out} = I$ is supplied to the output load. At the moment $\overline{Data}$ becomes high, then transistor M_4 is conducting and the $\overline{I_{out}} = I$ is supplied to the output load. As can be seen from the figure, if M_3 or M_4 is conducting, the current division is not changing because the basic system does not change. The only thing that is happening is, that the divided currents are routed to the output terminal or $\overline{output}$ terminal. As is shown further, the series connection of two equal transistors in triode mode is equal to a transistor with double gate length (L) and therefore is equivalent to a resistor of $2R$.

6.4.4 4-bit R-$2R$ MOS converter example

An example of a 4-bit R-$2R$ MOS converter is shown in Fig. 6.9. By

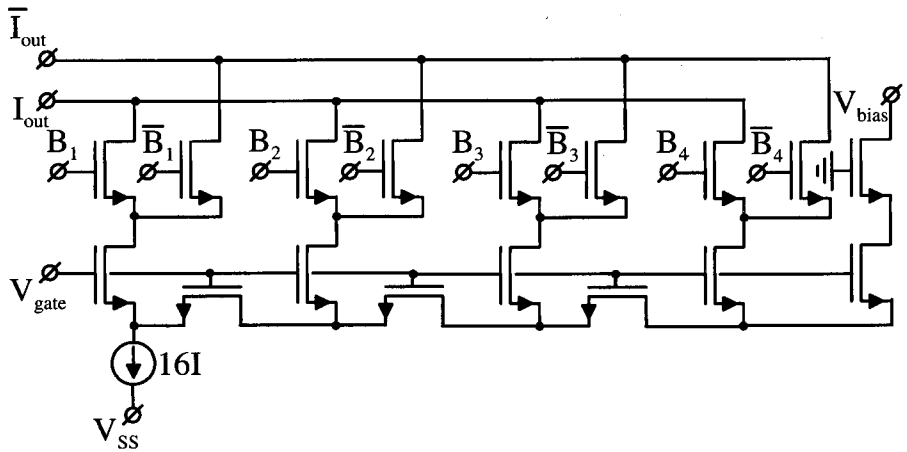


Figure 6.9: 4-bit R-2R MOS converter example

cascading the basic elements from Fig. 6.8 a 4-bit converter can be designed. The transistors in the system can be scaled depending on the current value flowing through the individual stages. In this system the tail current $16I$ is divided into $8I$, $4I$, $2I$, I and I. The extra current I obtained in the last stage is supplied to the bias voltage and is not required for the digital-to-analog conversion. With large sizes for the division transistors it is possible to obtain 10-bit resolution with $\pm$ 0.5 % linearity. An example using this technique will be described as an analog-to-digital converter with practical measured results. An accurate switching of the currents is required to obtain

a small glitch when the digital-to-analog converter is switched around the MSB value in an offset binary coded converter system. Timing is very important here.

6.4.5 Two-step current division network

By using a two-step current division principle basically the number of elements needed to perform a binary weighted current division can be reduced. In Figure 6.10 an example of a 12-bit converter is shown. As can be seen

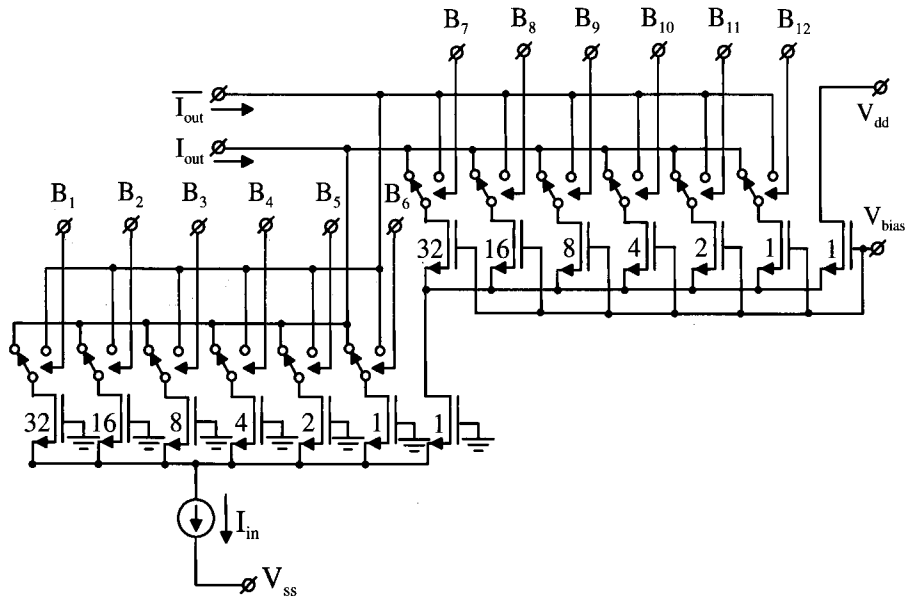


Figure 6.10: Two-step current division network

from the figure, two identical current division networks are used. The number of MOS devices connected in parallel to obtain the binary weighting is indicated by the numbers in front of the devices. The current I_{in} is split-up into 6 MSB currents. The extra current I obtained in this network is supplied to the LSB division network and again split-up into 6 LSB currents. The extra current I in the LSB network is not used and this current flows to V_{dd}. It seems easy to increase the resolution of a current division network by cascoding two or more simple networks. However, in a 12-bit system a very good matching (better than 0.1%) in the MSB network is needed to avoid non-monotonicity or missing codes. Furthermore the cascoding of networks increases the supply voltage and in submicron CMOS technology this extra

supply voltage is not available. Therefore this network is only shown as a step-up into *Monotonic by design* systems.

6.4.6 MOS ladder network converter system

In a special MOS technology thin film process steps to construct the R-$2R$ ladder network are used in combination with CMOS switches to design a D/A converter. Thin film resistors show a better matching than poly silicon resistors which are available in a MOS technology. Moreover, thin film devices can be trimmed to improve the accuracy of the converter. In Figure 6.11 a basic circuit diagram as part of a 10-bit D/A converter is shown. As

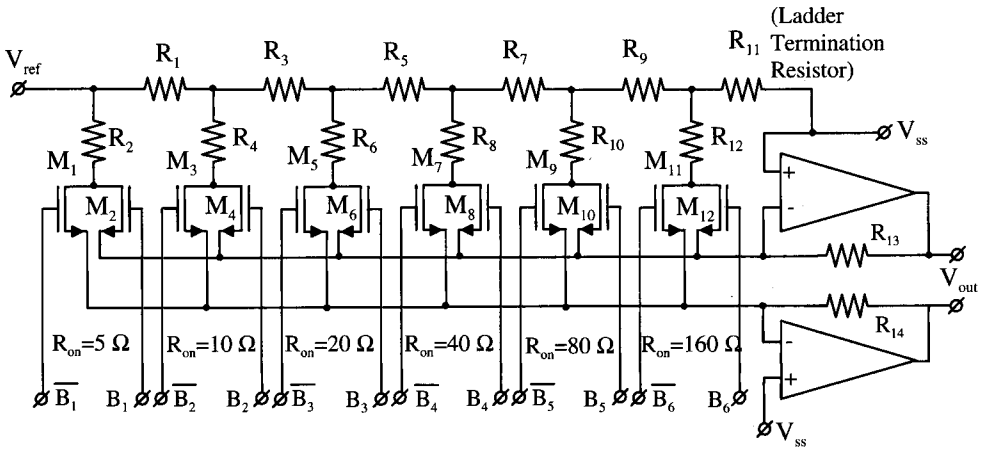


Figure 6.11: MOS ladder network D/A converter system

can be seen from Figure 6.11, the ON resistance of the MOS bit switches is scaled to obtain a good accuracy of the converter. The reference voltage is applied at the analog input terminal. In this special situation a maximum of 10 Volts can be used as a reference. The resistor values are chosen depending on the size of the MOS switches and the ON resistance of these switches. A special application of this system is found if the analog input voltage is modulated. In that case a multiplying D/A converter structure is obtained. Such a construction can be used to increase the maximum dynamic range of the system or for digitally controlling an ac signal that can be used as analog reference voltage. The output signal of the ladder network is a current. This current is converted into a voltage using an operational amplifier with feedback resistors R_{13} and R_{14}. These feedback resistors are included with the ladder resistor network to obtain the same temperature coefficient

and the same matching. Using thin film resistor trimming techniques the linearity of this converter can be increased to 12 bits.

6.4.7 Weighted capacitor converter system

In a MOS technology capacitors with MOS switches perform an identical operation as resistors and transistors in a bipolar technology. In Figure 6.12 an example of a binary weighted capacitor D/A converter system is shown [27, 30, 28]. The system consists of n binary weighted capacitors, an

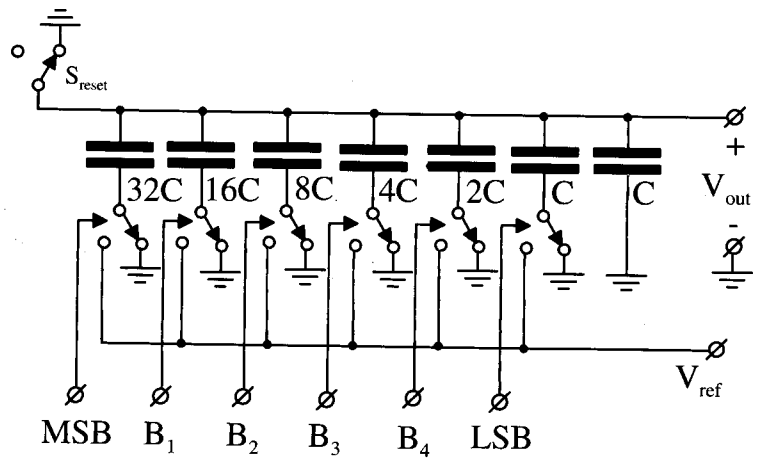


Figure 6.12: Binary-weighted capacitor D/A converter

additional capacitor with the unit capacitance C and a set of switches that can connect the weighted capacitors to the reference voltage V_{ref}. S_{reset} discharges all the capacitors with digital inputs at "0". At the start of the conversion all capacitors are discharged and the reset switch is opened. The capacitors are connected to the reference voltage or remain connected tyo ground depending on the digitaql input code. A charge redistribution occurs and finally at the output the reconstructed analog value is obtained. This value must be applied to an output buffer to avoid discharging of the unit capacitor C. This buffer amplifier is not shown. Furthermore it must be noted that parasitic capacitance such as for example the drain to substrate capacitance of the reset switch S_{reset} influence the accuracy of the system, while the nonlinearity of these capacitors introduce distortion. Furthermore the layout of the capacitors must be in such a way that the wire connecting every capacitor to the output terminal has the same binary weighted value. This is required to maintain an accurate binary weighting of this network.

Mostly unit capacitors are used with equal interconnect wiring to obtain the high accuracy required. In todays technology capacitor digital-to-analog converters can be designed with resolutions between 10 to 12 bit and INL errors below 0.5 LSB. A careful layout is required in such a capacitor array and mostly a dummy array is put around such an array to obtain equal neighbours for the outside capacitors.
Suppose that the total capacitance value in the system is equal to: C_{total}, then the unit capacitance C is equal to:

$$C = \frac{C_{total}}{2^N}. \tag{6.4}$$

The value of the capacitor connected to bit n, C_n becomes:

$$C_n = 2^{N-1} \times C. \tag{6.5}$$

The output voltage of the capacitor network can now be expressed in terms of capacitor values and the corresponding digital input code D_i. A calculation of the output voltage gives:

$$V_{out} = \frac{V_{ref}}{C_{total}} \sum_{i=1}^{N} C_i D_i. \tag{6.6}$$

This equation can be simplified into:

$$V_{out} = \frac{V_{ref}}{2^N} \sum_{i=1}^{N} D_i * 2^{i-1}. \tag{6.7}$$

This equation shows the binary weighting that is obtained by the charge redistribution technique. These techniques can be successfully applied in 10 to 12 bits D/A converters in a CMOS technology.

6.4.8 Weighted capacitor network with output amplifier

To eliminate most of the parasitic capacitance of a binary weighted capacitor digital-to-analog converter an output amplifier with a capacitor as feedback element is added. The value of the feedback capacitor C_f depends on the required gain of the converter system. With $C_f = 64C$ a gain of 1 is obtained. The converter system is shown in Fig. 6.13. During the reset mode of the converter, the input and feedback capacitors are discharged. In this system the low input impedance of the operational amplifier acts as a short circuit, so the input capacitors are discharged. At the moment the reset switch is

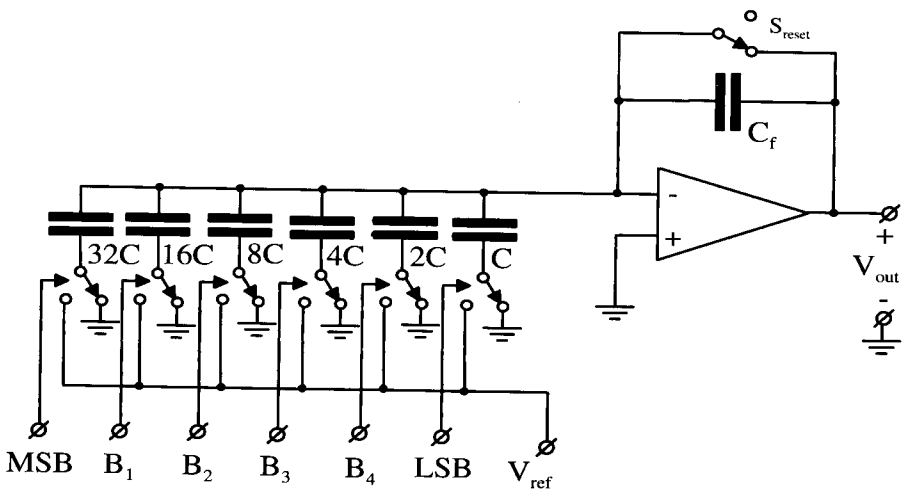


Figure 6.13: Binary-weighted capacitor D/A converter with output amplifier

opened, then the digital value can be applied and when a digital value of "1" is applied, the bit switch connects the capacitor to V_{ref} and this capacitor will be charged. The charge current flows through the feedback capacitor C_f. The output signal is generated across C_f dependent of the digital input code. This output voltage appears at the output of the operational amplifier and can be loaded by an external load. Because the signal voltage at the input of the operational amplifier is virtual zero, parasitic capacitance due to the construction of the capacitors and the interconnection wires does not influence the output signal and therefore linearity of the converter is only determined by the matching between the binary weighted capacitors. A resolution between 10 to 12 bit is practically obtainable.

6.4.9 Weighted capacitor network with resistive interpolation

To increase the resolution of a binary weighted capacitor digital-to-analog converter without increasing the number of weighted capacitors requires an extra interpolation step. The system using such an interpolation is shown in Fig. 6.14. A five bit binary weighted capacitor array converting the MSB bits is combined with a resistive divider determining the value of the fine bits N_{fine}. This resistive divider can use a two-step resistive interpolation method in case a rather large number of fine bits have to be converted or a single resistive ladder in case the number of bits is limited (between 3 to 5

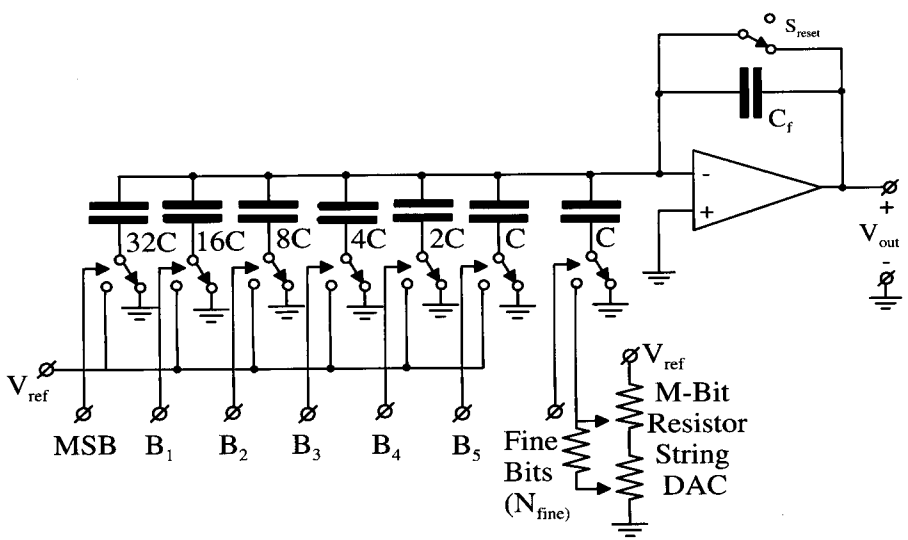


Figure 6.14: Binary-weighted capacitor D/A converter with resistive interpolation

bits for example). Again an operational amplifier with a capacitive feedback is used. The value of the feedback capacitor C_f can be adjusted to obtain the required converter gain. With digital input zero and the reset switch closed, all capacitors are discharged. The reset switch is opened and the digital input data sets the bit switches in the right position. At that moment a bit value "1" charges the connected capacitor and the current charging this capacitor flows through the feedback capacitor C_f and generates at the output of the operational amplifier the reconstructed analog value. A large resolution can in principle be obtained using this system, however, the binary weighting accuracy of the capacitor array determines the maximum resolution in case no calibration is used. In some systems a capacitor calibration is used for the most significant bits and then a resolution between 14 to 18 bits can be obtained with this system.

6.5 Monotonic by design network systems

So far systems have been discussed that have a potential to obtain a high resolution but at the same time no guarantee is obtained if such a system is accurate or will be monotonic or have no missing codes. In this section attention will be paid to special circuit configurations that by construction

give a guaranteed monotonic behavior of the converter.

6.5.1 Voltage division operation

An example of a 16-bit monotonic by design voltage division converter is shown in Figure 6.15 [22]. As can be seen from this figure, the system con-

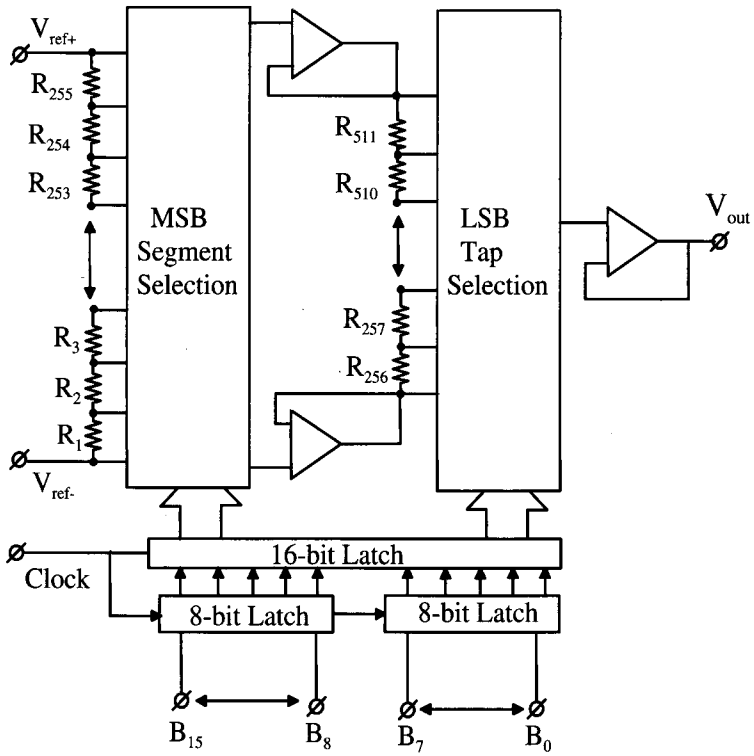


Figure 6.15: Voltage division monotonic converter [22]

sists of two resistor strings with 256 taps using resistors R_1 to R_{255} for the coarse divider part and R_{256} to R_{511} for the fine divider part. Two operational amplifiers connected in the follower mode apply the tap voltage of the coarse section across the total resistor string of the fine divider part. The MSB segment selection block consists of two sets of switches that are driven by the segment decoder. In the LSB tap selection block a set of switches is used to select a resistor tap and apply the output voltage to the output buffer. This output buffer consists of an operational amplifier in follower mode. A special operation of the switches in the MSB segment encoder is used to make the system independent of the offset voltage of the voltage

followers. In Figure 6.16 a detailed circuit diagram of the circuit including the switch drivers is shown. From the figure it can be seen that one side

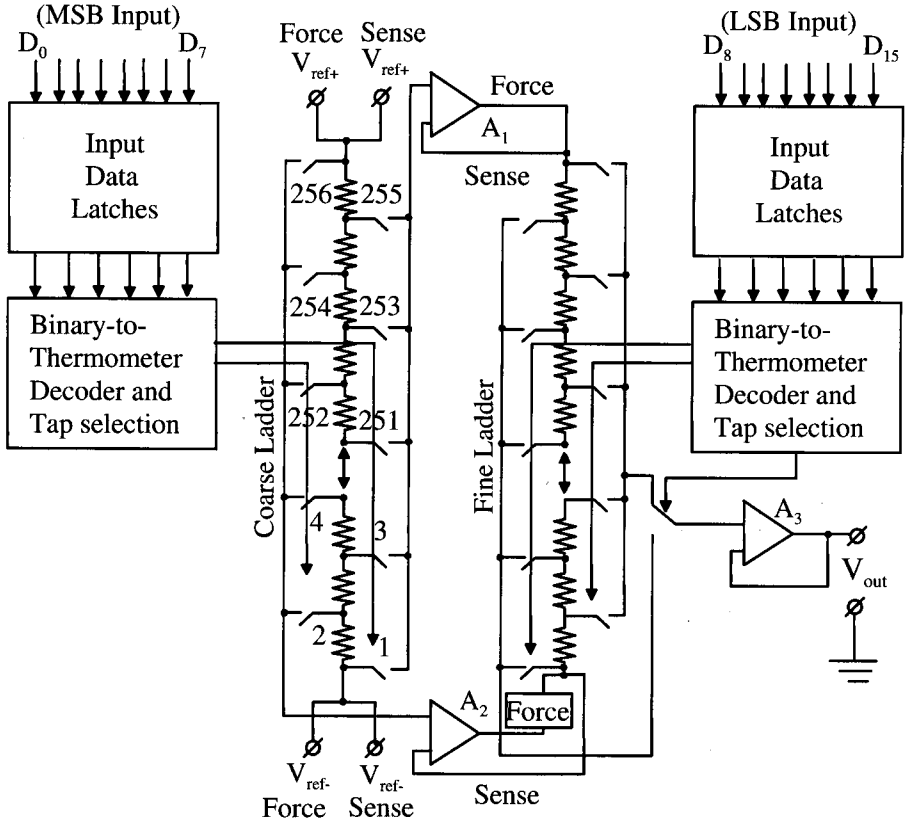


Figure 6.16: Detailed circuit diagram of monotonic voltage converter [22]

of the even numbered coarse switches is connected to voltage follower A_2, while one side of the odd numbered switches is connected to voltage follower A_1. An identical connection is obtained for the switches of the fine voltage divider. However, the output lines of the odd- and even-numbered fine switches are connected to an additional output switch. This decoding is used to simplify the logic circuit part.

The special connection used in the coarse voltage divider allows the analog signal to "roll-off" against the coarse divider without jumping from one position into another. In this way a continuous output voltage change can be guaranteed independent of the offset voltage of the voltage followers A_1

and A_2. By using this system, it is possible to construct a 16-bit guaranteed monotonic converter without needing the high division accuracy to obtain the integral nonlinearity of $\frac{1}{2}$ LSB.

6.5.2 Current weighting operation

Sometimes it is not necessary to obtain a converter with a full integral linearity specification, but it is enough to guarantee monotonicity of the system. In that case a different design technique can be adopted [21].

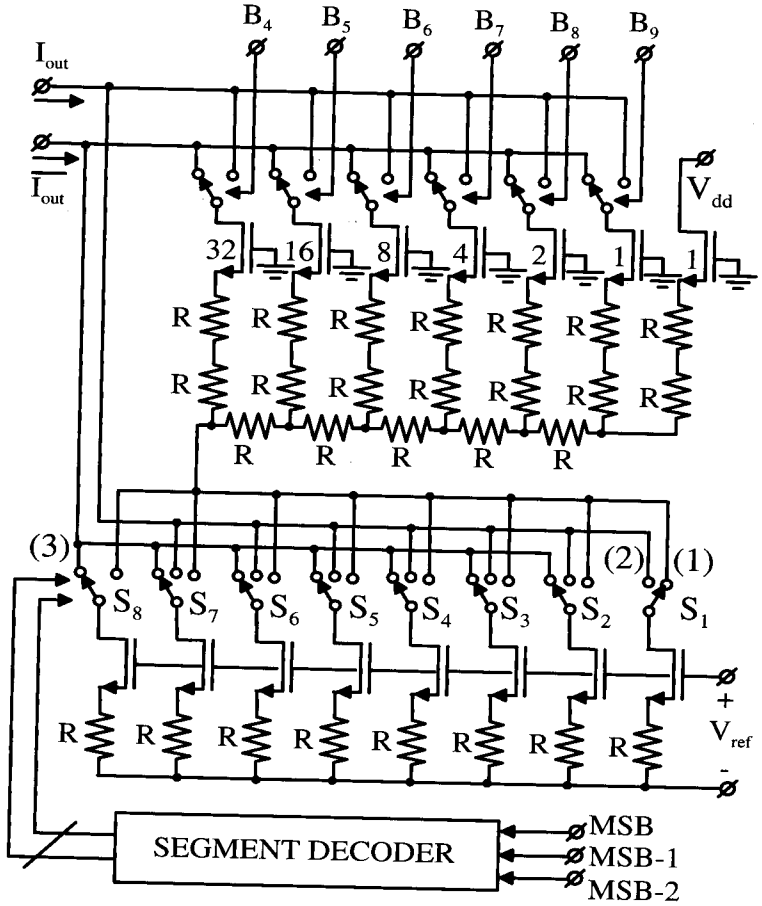


Figure 6.17: Monotonic current based D/A converter system

Monotonicity of a converter is obtained if with an increasing digital input signal an increase in analog output signal can be guaranteed. In such

a case always a current is added and not switched off and replaced by a larger current value. In Figure 6.17 a basic example of a current based *monotonic by design* converter type is shown. In the most significant 3 bits of the converter equal currents are used. The binary coded digital input signal uses a segment decoder to obtain for six of the eight switches a three-position condition. The current value of the segmented currents is I_0. The next 6 bits use an R-$2R$ network with device scaling to obtain an accurate current division.

The implementation of an R-$2R$ network must improve the weighting accuracy. Because of the small value of the current and the limited value resistors can be given in an integrated circuit this voltage drop in practice is difficult to make large enough so that the resistor network determines the weighting accuracy. The operation of the system can be explained by supposing that a sawtooth like digital input code is applied at the input of the converter. First the current I_0 is switched to the 6-bit current weighting network. S_1 is at position (1) and all other switches are at position (3). This current is switched to the output node I_{out} by the bit switches B_4 to B_{12}. The position of the switches for bit B_4 to B_9 depends on the digital input data. At the moment the output current I_{out} must be larger than I_0, then the bit current I_0 is switched directly to the output terminal I_{out} by the segment current switches. S_1 is now at position (2). At the same time the current I_1 is switched to the 6-bit current network by the switch S_2 to perform the next quantization steps until the output currents exceeds $I_1 + I_0$. At that moment the current I_1 is switched directly to the output terminal I_{out} (S_2 is in position (2)) and the current I_2 is switched to the 6-bit current network. Using this procedure *monotonicity* of the converter can be guaranteed. Integral linearity basically depends on the matching accuracy of the used elements and can not be guaranteed to be less than $\frac{1}{2}$ LSB. The use of source degeneration resistors R and the R-$2R$ network in this system is only symbolically. In practical CMOS converters the supply voltage is too small to allow source degeneration resistors. Therefore in a practical solution these resistors will be omitted. Furthermore the supply voltage in such a system must be large enough to allow cascoding of two division systems to perform the *monotonic by design* operation.

6.5.3 MOS only monotonic by design system

In a practical *monotonic by design* the resistors are eliminated and MOS devices only are used. In Fig. 6.18 a solution for a 9-bit converter is shown. In the 3-bit segmented system part equal currents using equal sized devices

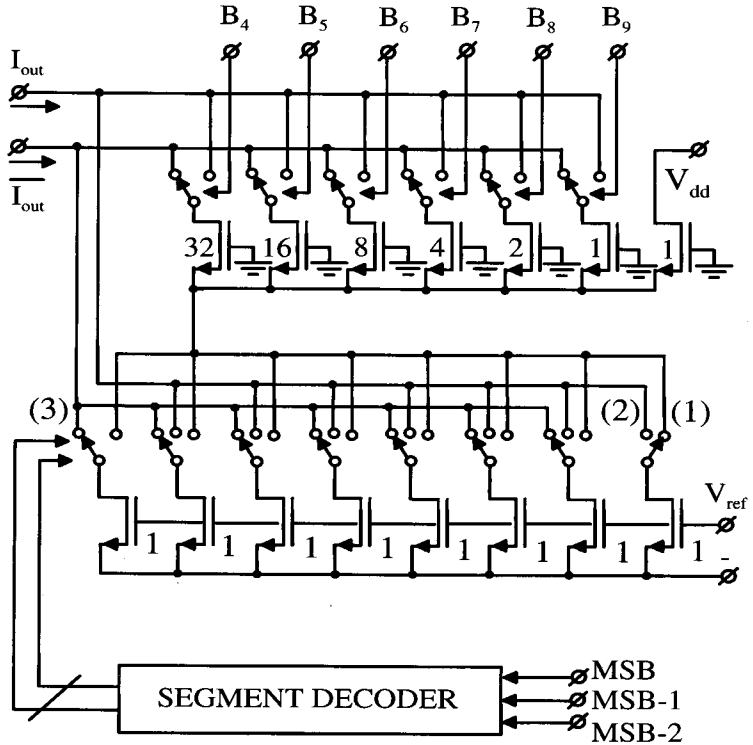


Figure 6.18: Mos only monotonic by design system

are used. Then one of the output currents of the segmented converter section is applied to the binary weighted converter part to obtain the fine bit conversion. Normally this system is applied in case monotonicity is required for converters between 12 and 16 bits. This means that the binary weighted section has a resolution between 10 to 12 bit. The 12-bit solution will require a large die size to obtain the required weighting accuracy. The segmented section can be set-up with resolutions up to 6 bits (64 equal current sources). this means that 16 to 18 bit monotonic by design systems are possible.

6.5.4 Active division MOS only monotonic by design system

The principle of monotonic by design can be applied to the active MOS only architecture too. In Fig. 6.19 a simple solution is shown. The system consists of a 2-bit segmented converter section that controls a 4-bit binary weighted section. In the segmented section a binary to segment decoder is used. The first and the last current source need only a two position switch

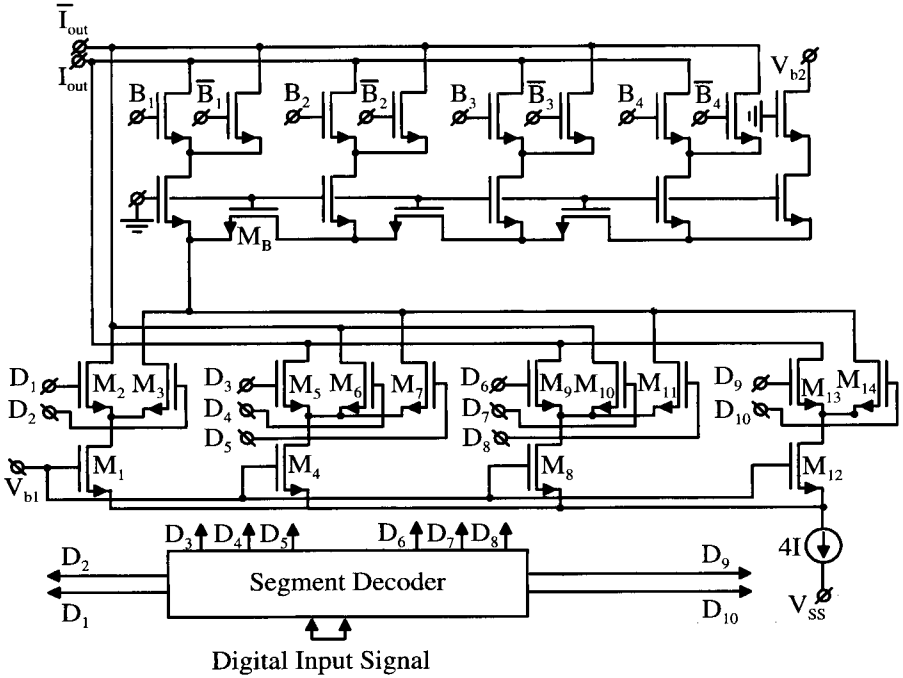


Figure 6.19: Monotonic current based D/A converter system

while the other currents need a three position switch. These switch signals are generated in the segment decoder part. The switches in the segmented and the binary part are part of the current division networks. In case a very low voltage is needed, then all current division devices operate in the triode region needing only a few hundred millivolts of supply. The switches can be driven with a large gate voltage. A bootstrapping of the gate voltage can be used in case a very low R_{on} is designed for, otherwise a normal V_{dd} high voltage is used. In this system again always an increase in bit current is used by switching one of the segmented currents to the binary weighted fine converter section as described before. At the output of this system a current to voltage stage is required to maintain under all conditions a constant drain-source voltage for the current division transistors. In Fig. 6.20 an example of a current-to-voltage converter stage is shown.

6.5.5 Current-to-voltage converter

The current-to-voltage converter is applied in nearly all MOS only digital-to-analog converter stages. Such a converter prevents a variation of the

drain-source voltage of the division devices due to the generated output voltage of the converter. In this system two operational amplifiers are used.

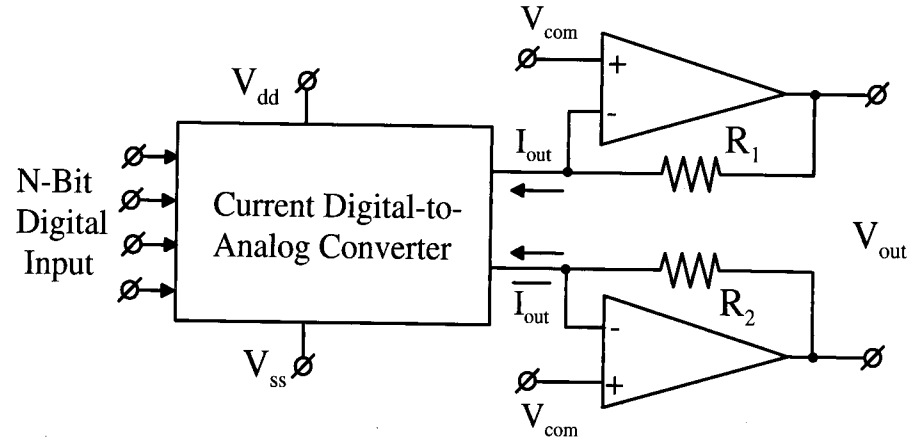


Figure 6.20: Current-to-voltage converter stage

These amplifiers have a transfer resistance of R_1 and R_2 respectively. The output currents I_{out} and $\overline{I_{out}}$ are converted into an output voltage across the resistors R_1 and R_2. The common mode output voltage V_{com} determines the DC level of the converter. As the negative terminal of an operational amplifier in this feedback condition shows a virtual zero, the common mode voltage at the converter outputs remains at this level independent of the output signal. No modulation of the drain-source voltages of the divider devices from which the digital-to-analog converter is built up occurs. Different configurations of the output amplifiers can be obtained but are not discussed here.

6.6 Self calibrating D/A converter system

If D/A converters are not continuously is use, a calibration procedure can be used to eliminate in accuracies of elements [72]. In Figure 6.21 an example of a D/A converter system that uses a self-calibration cycle is shown. The system consists of a main D/A converter and a sub-D/A converter used to eliminate the errors in the main D/A converter. During the calibration cycle an analog ramp is generated using a ramp generator. The output of the main D/A converter is compared with the ramp signal by the comparator. The correction logic generates a digital correction signal that is stored in

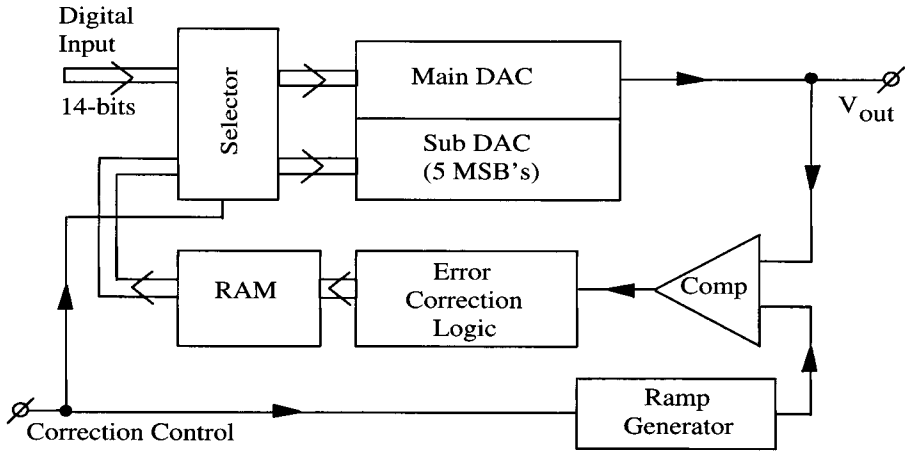


Figure 6.21: Self-calibrating D/A converter system [72]

the RAM unit. The RAM data control the sub-D/A converter to correct the output signal of the total D/A converter function to obtain the full $\frac{1}{2}$ LSB integral nonlinearity. In Figure 6.22 the calibration operation is shown. At the moment the main D/A output signal does differ from the

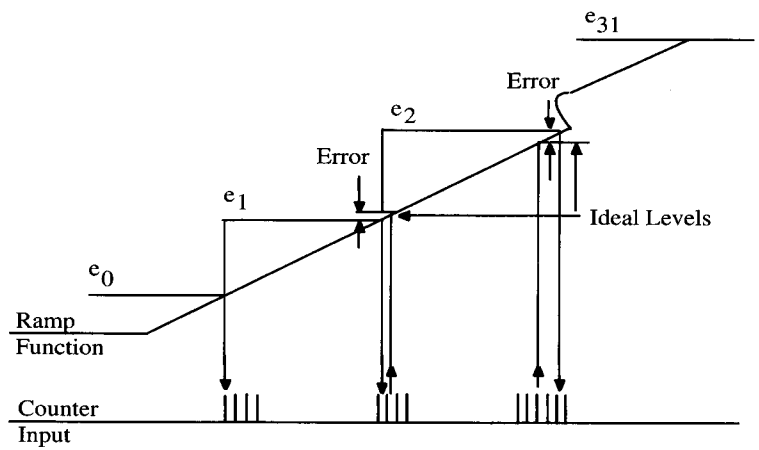


Figure 6.22: D/A correction cycle [72]

ideal D/A converter output, which is generated by the ramp signal source, then a counting operation starts that controls the output of the sub D/A converter to add a small correction value to the main D/A converter output to obtain the ideal output value. The correction value is stored for every

weighting value of the main D/A converter. This means that in a 14-bit system 14 correction values of 6 to 8 bits must be stored to correct the main D/A converter output. When a code is applied to the D/A converter, then the correction value is called from the RAM and applied to the sub D/A to correct the output. Note that during calibration the D/A converter cannot be used for conversion. In some applications this can be a disadvantage. To overcome this problem a different method will be used. Self-calibration techniques of converters have become fairly popular during the last few years. In references [66] and [73] examples of these techniques are given, applied in a D/A and an A/D converter.

6.7 Dynamic Element Matching

In this section a system will be described that combines a good passive division with a dynamic time accurate interchanging operation to obtain an element independent highly-accurate current division [62]. Practical implementations of the system will be shown in a CMOS technology. The designer in this technology can optimize his/her design with respect to matching, noise, and minimum supply voltage.

6.7.1 Basic dynamic divider scheme

A simplified circuit diagram of the basic dynamic current divider is shown in Figure 6.23. The circuit consists of a passive current divider and a set of switches driven by the clock generator f. The passive divider divides the total current $2I$ into two nearly equal parts: $I_1 = I + \Delta I$, $I_2 = I - \Delta I$. The currents I_1 and I_2 are now interchanged during equal time intervals with respect to the output terminals 3 and 4. At these terminals currents then flow whose average values are exactly equal and have a dc value I. In Figure 6.24 the currents as a function of time are shown. The figure shows that a small ripple current with a value of $2\Delta I$ and frequency f is also present at the output terminals. This ripple is a measure of the matching accuracy of the passive divider. With a simple low-pass filter this ripple can be removed from the output current and, as a result, accurate output currents with a value of I are obtained. In principle, a current divider with an exact division ratio of one-to-two is obtained with this system. Moreover, if the matching of the passive divider stage changed during operation, for example, because of a slowly changing temperature, then the accuracy of the system would not change. The only variation which occurs is the increase or decrease of the ripple current value depending on the direction in which the matching

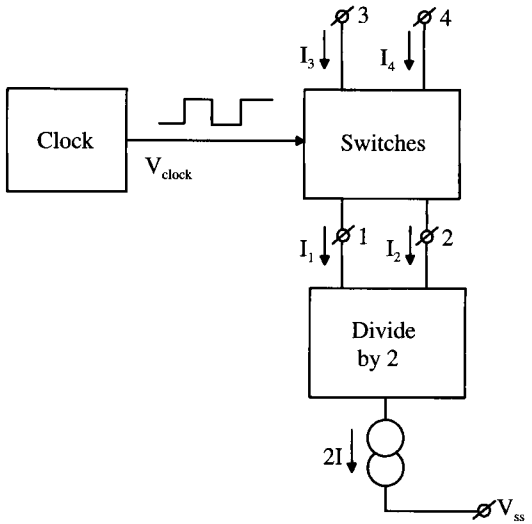


Figure 6.23: Basic dynamic current divider

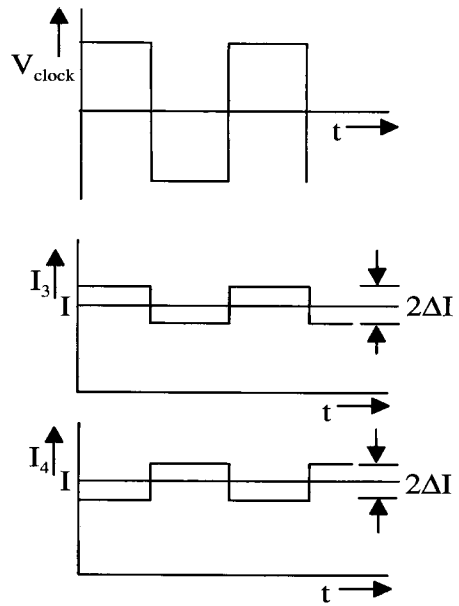


Figure 6.24: Currents as a function of time in the dynamic current divider

in the passive divider changes. In the previous analysis an accurate time division by two is supposed. If there is a slight difference in the timing of the two clock cycles, then a high-accuracy is still possible. Suppose that the clock time periods differ by a value Δt, then we obtain:

$$t_1 = t + \Delta t, \tag{6.8}$$

and

$$t_2 = t - \Delta t. \tag{6.9}$$

Also, using the already defined values for I_1 and I_2

$$I_1 = I + \Delta I, \tag{6.10}$$

and

$$I_2 = I - \Delta I. \tag{6.11}$$

The current differences ΔI are equal because the sum of the two currents must be equal to $2I$, which is the starting current of the divider stage. During the first phase of the clock cycle the output currents become:

$$I_{out11} = (t + \Delta t) \times (I + \Delta I) \tag{6.12}$$

and

$$I_{out21} = (t + \Delta t) \times (I - \Delta I). \tag{6.13}$$

In the second phase of the clock cycle the output currents change into:

$$I_{out12} = (t - \Delta t) \times (I - \Delta I) \tag{6.14}$$

and

$$I_{out22} = (t - \Delta t) \times (I + \Delta I). \tag{6.15}$$

Now at every output terminal the currents must be added and averaged over the total clock time $2t$. We obtain:

$$\frac{I_{out11} + I_{out12}}{2t} = I(1 + \frac{\Delta t \times \Delta I}{t \times I}) \tag{6.16}$$

$$\frac{I_{out21} + I_{out22}}{2t} = I(1 - \frac{\Delta t \times \Delta I}{t \times I}). \tag{6.17}$$

As is seen from equations 6.16 and 6.17 the final accuracy in this system is determined by the product of two small errors. In practice it is not difficult to make $\frac{\Delta t}{t} \leq 0.1\%$ and the matching of the passive divider can easily be made smaller than 1% so $\frac{\Delta I}{I} \leq 1\%$. An overall accuracy better than 10^{-5}

is obtained without using extremely difficult circuitry or elements which are difficult to match. The ripple which is present at the output of the divider scheme is a measure of the matching accuracy in the passive divider. This method which obtains a high accuracy without using highly matched and highly accurately trimmed elements is called *Dynamic Element Matching*. The value of the ripple can be reduced by optimizing the matching characteristics of the passive divide-by-two stage. A small ripple on the output values of the circuit allows the use of a simple low-pass filter network to reject this ripple below the quantization noise of the system. Usually such a network consists of a single *RC* stage.

Generally speaking, *Dynamic Element Matching* can be used to increase the accuracy of a divider scheme when the network can be split up into a number of nearly equal elements. The accuracy improvement is obtained by a continuously cyclic interchanging of the elements with respect to the respective output terminals. The output signals must be averaged over the total interchanging time period. At least an order of magnitude improvement in accuracy is obtained in this way. Furthermore, this system is independent of element aging and does not need highly accurate elements.

In reference [65] an example is shown that does not use binary weighting of current. Instead a decimal weighting is used to generate reference currents for resistor measurements.

6.7.2 Practical dynamic divider circuit

In Figure 6.25 a circuit diagram of a practical divider in a CMOS technology is shown. The passive divide-by-two current division is performed by transistors M_1, M_2. Two cross-coupled differential stages (M_3 to M_6) interchange the currents I_1 and I_2 for equal time intervals between the output terminals 3 and 4. The already discussed improvement in division accuracy with respect to the basic current divider M_1, M_2 is now obtained. The value of the output ripple current depends on the matching of the current mirror M_1, M_2. The minimum supply voltage drop across the circuit to operate under linear condition is about 1 to 1.5 V.

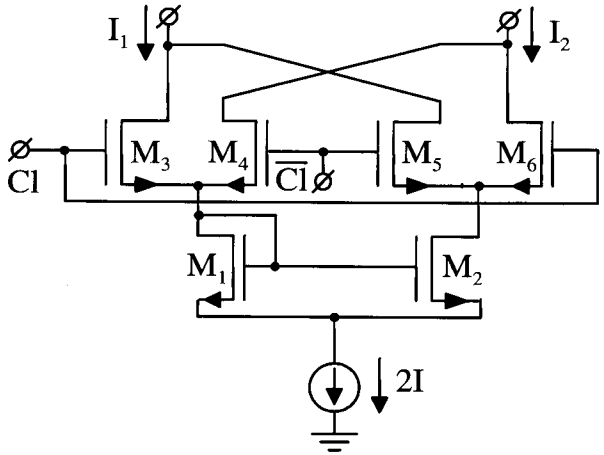


Figure 6.25: Practical dynamic divider scheme

6.7.3 Two-bit dynamic current divider scheme

In the circuit of Figure 6.25 per dynamic divider stage only one accurately matched bit current is generated. When such stages are cascaded, the supply voltages will increase to an impractically high voltage level. To overcome this problem a 2-bit system will be used. The basic system diagram is shown in Figure 6.26. In this system the passive divider is extended to divide a current $4I$ into four nearly equal currents: $I_1 = I + \Delta_1 I$, $I_2 = I + \Delta_2 I$, $I_3 = I + \Delta_3 I$, and $I_4 = I + \Delta_4 I$. Note that $\Delta_1 + \Delta_2 + \Delta_3 + \Delta_4 = 0$, because the total current which is divided into four nearly equal parts is $4I$. These currents are now fed into a switching network that interchanges all currents during equal time intervals with respect to the output terminals 1, 2, and the combined terminal 3. At these outputs averaged currents with values I, I, and $2I$ are obtained. In Figure 6.27 the output currents as a function of time are shown. From Figure 6.27 it can be seen that the currents with a value I have the same frequency as the clock f, while the current with a value $2I$ has a ripple with a frequency $\frac{f}{2}$. Timing errors have the same influence as in the one-bit divider scheme. In Figure 6.28 a circuit diagram of a practical divider circuit is shown. It consists again of a passive divide by four stage using transistors M_1, M_2, M_3, and M_4. This stage divides the current $4I$ into four nearly equal values of I. These currents are applied to the interchanging system consisting of MOS switches. In a 2-bit Dynamic Element Matching stage the number of interchanging switches becomes 4x4 = 16 switches. In Figure 6.28 the gates of the passive divider are connected to a reference voltage

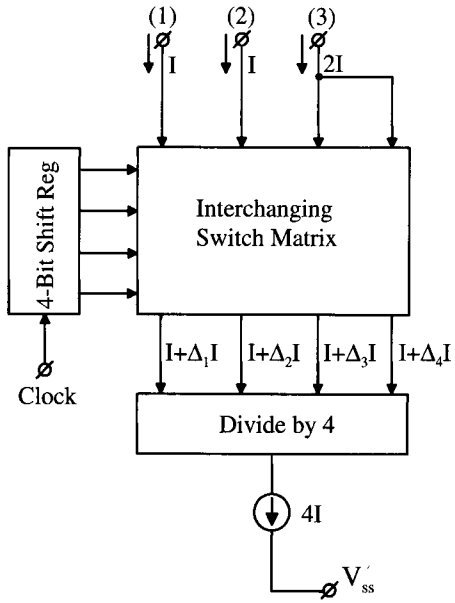


Figure 6.26: 2-bit current divider scheme

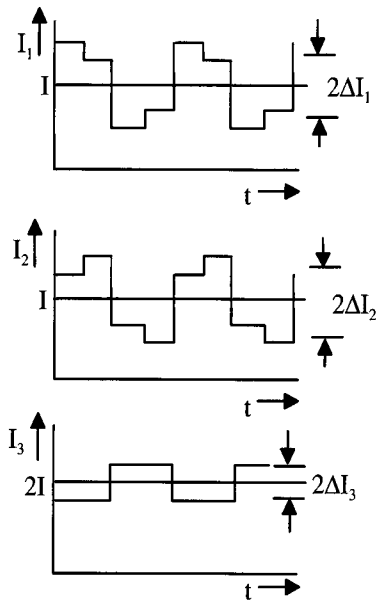


Figure 6.27: Output currents as a function of time for the 2-bit divider system

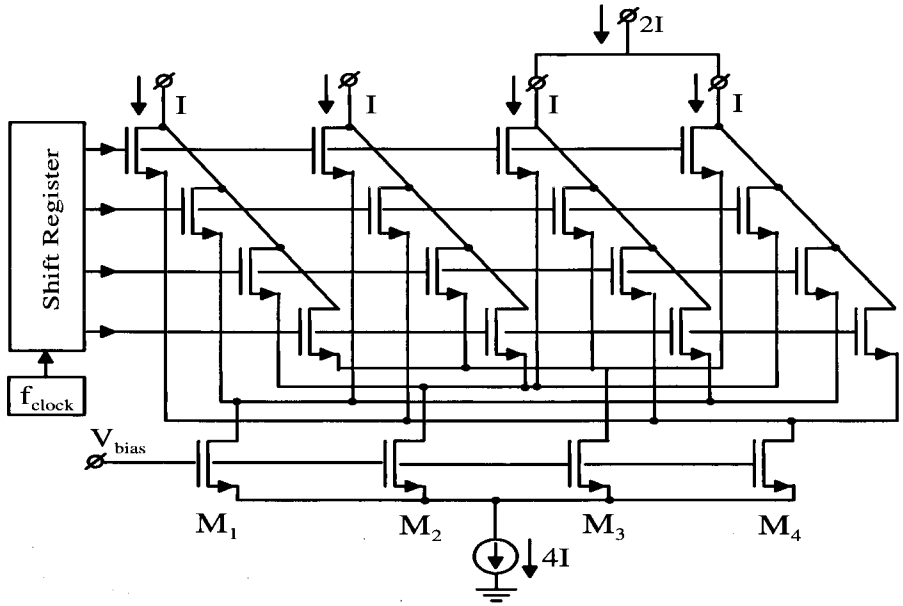


Figure 6.28: Practical 2-bit dynamic current divider

V_{bias}. Usually this reference voltage is the drain terminal of, for example, transistor M_1. In this way a current mirror circuit with four output signals is obtained. A four-bit shift register provides the time-accurate signals for the interchanging of the currents. In this circuit a high time division accuracy is easily obtained. The only additional criterion to improve the accuracy of the system is a high division accuracy of the passive current divider. Such a high accuracy reduces the amount of ripple current on the output signals of the active divider.

The number of accurate output currents in a multi-bit dynamic divider can be increased rather easy. However, the number of switches needed in the interchanging switching matrix increases as:

$$Number\ of\ Switches = 2^{2N_{bit}}. \tag{6.18}$$

In case a 4-bit divider is required, then the number of switches increases to 256. Such a switching matrix shows already a substantial die size. Furthermore in very high accuracy systems, leakage currents may play an important role at high die temperatures.

6.7.4 Dynamic current mirror circuit

In some applications it is useful to obtain an accurately matched current mirror. A circuit diagram which uses *Dynamic Element Matching* to obtain a device matching independent accurate current mirror is shown in Figure 6.29. The basic current mirror consists of transistors M_1 and M_2. Switching

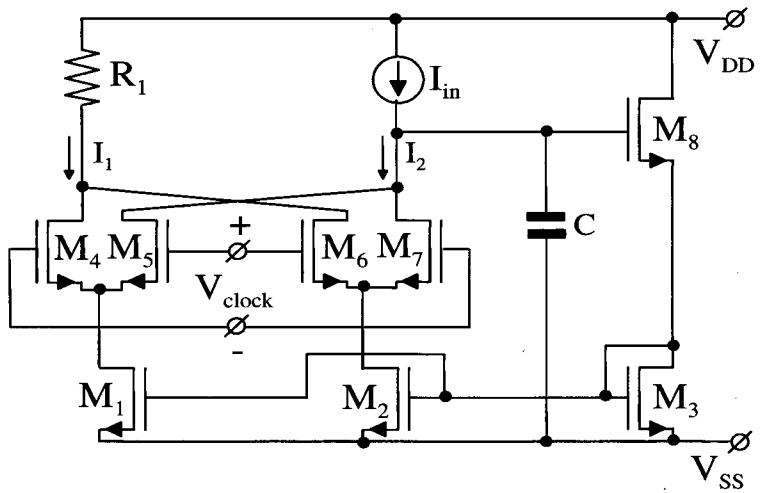


Figure 6.29: Dynamic current mirror circuit diagram

stages M_4 to M_7 interchange the currents of M_1 and M_2 with respect to the sum and output terminal of the mirror. M_8 with M_3 form the current-source feedback loop. Two cases of operation can now be distinguished.

1. An averaging capacitor is connected across the diode connection of the current mirror. This means that the gate of transistor M_8 is decoupled to ground with a capacitor C. The average value of the drain currents from switches M_5 and M_7 is made equal to I_{in}. Then the average output current I_{out} is the average value of I_2. As a result, an accurate current mirror $I_{out} = I_{in}$ is obtained.

2. The capacitor C is omitted. During the first half period of the clock phase the drain current of M_2, I_{M2}, is controlled in such a way that $I_{M2} = I_{in}$. By supposing an error Δ between the transistors M_1 and M_2, an output current equal to $I_{out} = I_{in} \times (1 + \Delta)$ is obtained. During the second phase of the clock cycle, I_{M1} and I_{M2} are interchanged,

resulting in an output current $I_{out} = \frac{I_{in}}{1+\Delta}$. When Δ is made small, by obtaining a good matching between the transistors M_1 and M_2 then the division by $(1 + \Delta)$ can be approximated by a finite series expansion. As a result we obtain:

$$I_{out} \cong I_{in}(1 - \Delta + \Delta^2). \tag{6.19}$$

After averaging the results over the total clock period we obtain:

$$I_{out} \cong I_{in}(1 + \frac{1}{2}\Delta^2). \tag{6.20}$$

Inserting a value for $\Delta < 0.5\%$ the mirroring error term is below 10^{-5}. The current mirror without the capacitor C shows a less accurate performance than the one with a large capacitor C.

6.7.5 Binary-weighted accurate current network

A binary-weighted current network is formed by cascading current division elements. In Figure 6.30 a simplified block diagram using single current divider stages is shown. In the first divider stage a combination with a ref-

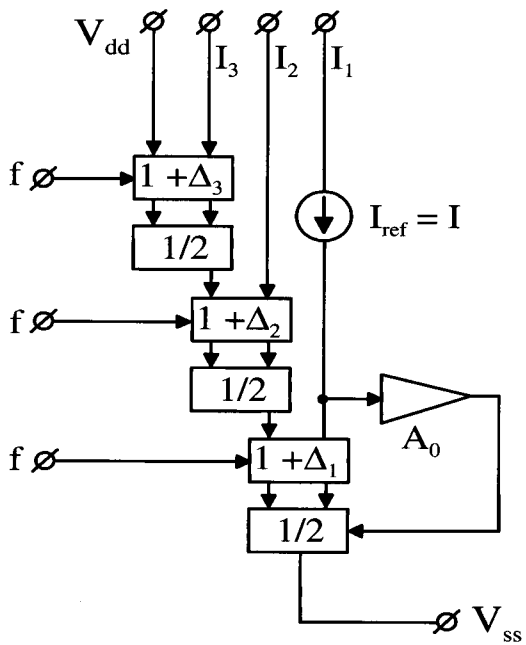


Figure 6.30: Binary-weighted current network

erence current source I_{ref} and a current amplifier A_0 is made to obtain an accurate current mirror.

Now two possibilities exist with respect to the interchanging frequency of the cascaded current divider stages.

1. Every following divider stage is operated at half or double the switching frequency of the first divider stage.

2. Every divider stage obtains the same interchanging frequency.

6.7.6 Binary-weighted current network with divided interchanging clock

In this case digital clock circuitry that accurately divides the interchanging clock frequency by two is needed. Supposing that we lower the interchanging frequency every time a current is divided by two, then we will not have any interaction between the individual current dividers concerning the finite matching accuracy of every divider. Suppose that the output current of the first divider I^* shows the inaccuracy Δ_1. In the output current $\frac{I}{2}$ of the second divider stage we can recognize the error Δ_2 with a frequency $\frac{f}{2}$ and the error Δ_1 of the first stage with a frequency f. During a half period of the clock $\frac{f}{2}$ the average value of the current $\frac{I}{2}$ does not contain an error term originating from the first divider stage of frequency f. The same is valid for the second half clock period of the frequency $\frac{f}{2}$. As a result of this operation no interaction of the division accuracy of the first stage on the second stage is found. If the clock frequency division is continued, the same arguments can be used for the next stage, and so on. An independent operation of the individual stages in the total divider chain is obtained. A disadvantage of the division of the interchanging clock frequency by factors of two is the large increase in digital circuitry that is needed to accurately drive the individual divider stages. Moreover, the ripple frequency decreases with decreasing current value. This means that the filtering capacitors that are used in the passive ripple filter increase and might need impractically large values.

6.7.7 Binary-weighted current network using equal interchanging clock frequencies

When all divider stages are operated with the same interchanging clock, it is expected that in the error analysis interactions between the individual divider stages will occur. Timing errors in this case are equal for all the divider stages. These timing errors can therefore be separated from the division errors in the individual stages.

Suppose the error in the first stage is denoted as Δ_1, then the total error of the first stage including the timing error can be written as:

$$I^* = I_{ref}(1 + \Delta_1 \times \frac{\Delta t}{t}). \tag{6.21}$$

In the expression given in equation 6.21 the filtering capacitor as described with regard to the accurate current mirror circuit is ignored. The average value of the output current of the second stage can be calculated:

$$\frac{I}{2} = I_{ref}\frac{(1+\Delta_1)(1+\Delta_2)(t+\Delta t) + (1-\Delta_1)(1-\Delta_2)(t-\Delta t)}{4t}. \tag{6.22}$$

This long formula can be simplified into:

$$\frac{I}{2} = \frac{I_{ref}}{2}(1 + \Delta_1\Delta_2 + (\Delta_1 + \Delta_2)\frac{\Delta t}{t}). \tag{6.23}$$

The average value of the output current of the third stage is again determined. The simplified result is shown in the following equation:

$$\frac{I}{4} = \frac{I_{ref}}{4}(1 - \Delta_1\Delta_2 + \Delta_1\Delta_3 - \Delta_2\Delta_3 + (\Delta_1 - \Delta_2 + \Delta_3)\frac{\Delta t}{t}). \tag{6.24}$$

If the error terms of the individual stages are made small ($\Delta_{1\to n} \leq 0.5\%$), then the influence of the interactions between the individual divider stages on the overall accuracy of the binary-weighted current network can be kept very small. To increase the resolution of the active divider stages, a 2-bit-per-switching-level configuration can be used advantageously.

6.7.8 16-bit binary network example

An example of a 16-bit binary-weighted current network using 3-bit-per-level divider stages is shown in Figure 6.31. In this system 2 active divider stages are cascaded followed by a 10-bit passive divider using scaling of

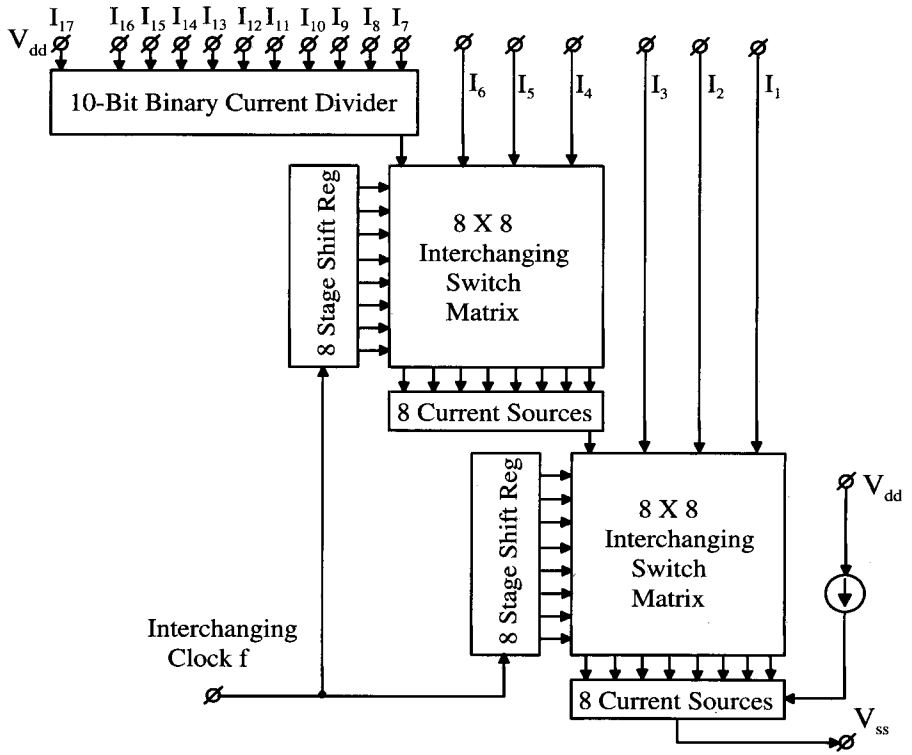


Figure 6.31: 16-bit binary-weighted current network

MOS devices. The two active dividers give 6 bit accurate binary weighted currents that have a ripple current determined by the matching of the 8 current sources. An equal interchanging frequency can be used in case the matching error between the 8 current sources is within a certain range. These ripple currents can be filtered out before they are applied to the bit switches. In this way an accurate 16-bit binary weighted current network is obtained without needing extreme matching requirements of components. The 10-bit passive divider is identical to the circuit shown in Fig. 6.6. Such a network not only consists of the required 1024 devices to obtain the binary weighting accuracy, but includes 2 extra rows and columns of dummy transistors to reduce the neighbouring effects.

6.7.9 Filtering and switching

An example of the implementation of the error current filtering and the switching of the bit currents is shown in Fig. 6.32. The filtering of the ripple

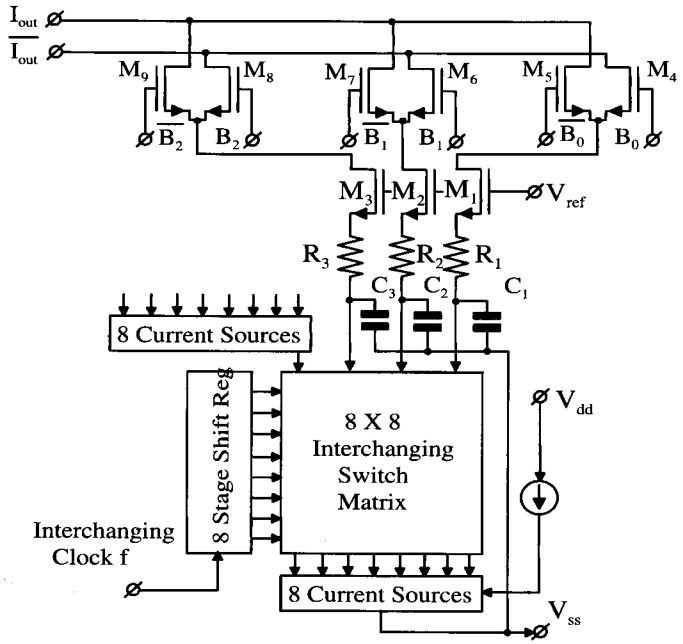


Figure 6.32: Filtering and switching of bit currents

currents obtained by dynamic element matching is performed by adding a resistor (R_1, R_2 and R_3)and an extra cascode stage (M_1, M_2 and M_3) to the system. With (external) capacitors (C_1, C_2 and C_3) this ripple current is filtered out. In some cases, when the interchanging frequency is high enough and the value of internal capacitors can be made large, these filtering capacitors can be included on the chip. The filtered currents are applied to differential pairs that perform the switching of the bit current in relation to the digital input information. A high performance system can be built in this way. A differential output current is obtained. Depending how the bit switches are operated, the output load can be directly applied to the system. However, in many cases to avoid signal kickback on the switching and current generation operation an operational amplifier is used as a current-to-voltage converter. In this way extra output filtering can be obtained and loading of the system with an external load is possible.

6.7.10 Randomizer to avoid ripple filtering

In case a good matching between the MOS devices in the input current divider that provides input currents to the dynamic interchanging network is

obtained, then it is possible to avoid the extra cascode with the resistor and capacitor to perform ripple filtering. In Fig. 6.20 this solution is shown. In

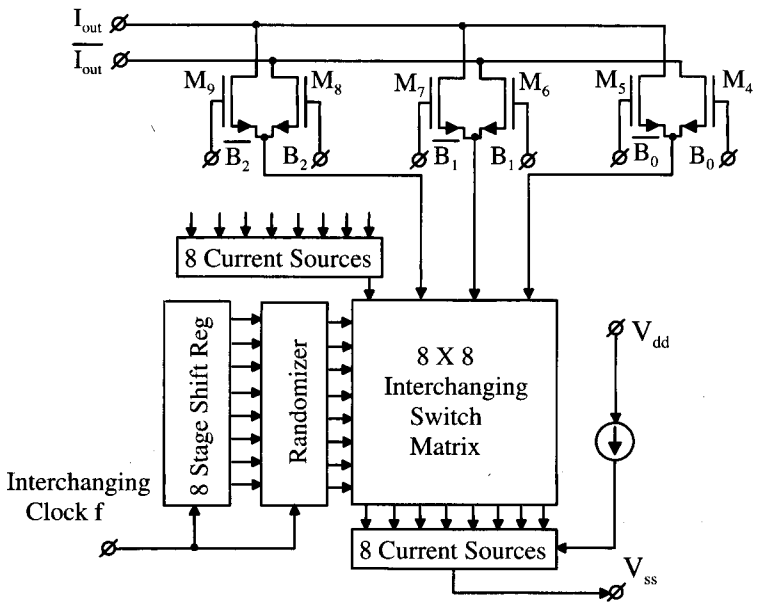


Figure 6.33: Randomized dynamic element matching

this system between the 8 stage shift register and the interchanging switch matrix a randomizer is introduced. This randomizer avoids the regularity in the interchanging system and as a result of this randomizing, the spectra of the ripple currents is spread over the Nyquist interval with smaller amplitudes. In case an oversampling in the converter is used, then part of the ripple spectra is filtered out by the output anti-aliasing filter.
This system is with great success applied to sigma-delta converters with a small number of bits in the reconstruction digital-to-analog converter.

6.8 Current calibration principle

In an MOS system it is possible to use a charge storage principle in an accurate current calibration system [66, 67, 68, 69, 70]. In Figure 6.34 the basic operation of the current calibration system is shown. The figure shows the calibration and the operational cycle. During calibration of the MOS current source, the MOS device M_1 is connected as a diode by closing switch S_1. The current I_{ref} is applied to the system and because of the diode

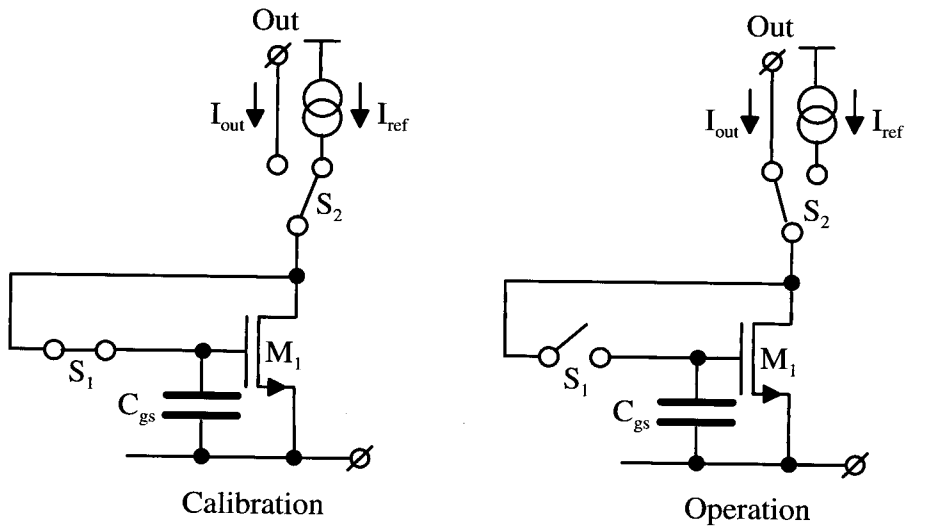


Figure 6.34: Current calibration principle [66]

connection of M_1, the gate-source voltage V_{gs} is adjusted in such a way that the drain current is made equal to I_{ref}. After the current has been calibrated to the reference value I_{ref}, the switch S_1 is opened and the gate-source voltage of the transistor M_1 remains at the calibration value. The output switch S_2 is switched to the output terminal. At that moment a current I_{ref} will start to flow through the output terminal. As long as the capacitor C_{gs} is not discharged, the drain current remains at the value I_{ref}. In a practical configuration, however, the capacitor is discharged because of the drain-substrate leakage current of the switch S_1. Moreover, the charge feed-through of the switch S_1, in case this switch is switched off, is added to the charge in C_{gs}. This means that the output current is not exactly equal to the calibration current value I_{ref}. In Figure 6.35 the two dominant error sources are shown. The leakage current of the source-to-substrate diode of transistor M_2 discharges the capacitor C_{gs}, while the charge feed-through of this switch is added or subtracted from the charge on the capacitor C_{gs}. These error sources result in variations of the gate-source voltage of M_1 which results in output current variations between two repeating calibration cycles. In Figure 6.36 the drain-source current of M_1 as a function of time is shown. During the time the current is compared with the reference current I_{ref} the same drain current is found. At the moment the switch S_1 is opened, the feed-through charge is subtracted from the charge on the capacitor C_{gs}.

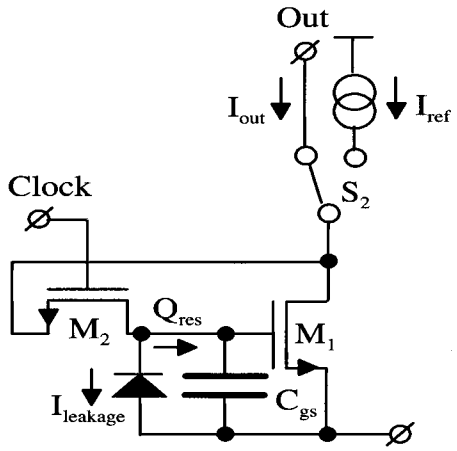


Figure 6.35: Two dominant error sources [66]

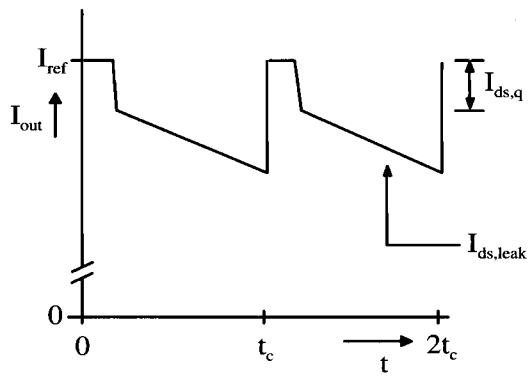


Figure 6.36: Drain current of calibrated device as a function of time [66]

As a result, a decrease in output current is obtained. This is shown with the steep decrease in current just after switching of S_1. Then the leakage current discharges the capacitor resulting in a roughly linear decrease in output current. If at time t_c the calibration cycle starts again, the current is adjusted to I_{ref} and the cycle repeats.

6.8.1 Improved current calibration principle

To overcome some of the problems encountered with the system shown in Figure 6.35, the calibration is applied to the error current value only. The improved system is shown in Figure 6.37. The basic system is equal to

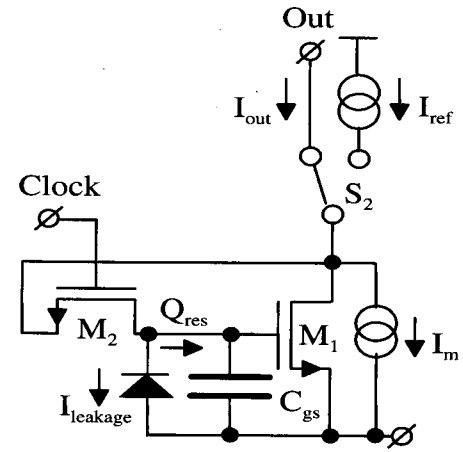


Figure 6.37: Improved current calibration principle [66]

the circuit shown in Figure 6.35. However, a current source I_m is added to the system. The current value of I_m is close to the value of I_{ref}. The difference between I_{ref} and I_m is stored in M_1 during the calibration cycle. This means that $I_m < I_{ref}$. In a practical case the difference current that can be stored in M_1 is between 0.1 and 0.05 of I_{ref}. Using this system the $\frac{W}{L}$ ratio of transistor M_1 can be chosen to minimize the g_m of the device. Moreover, due to this device choice a large V_{gs} voltage is needed to drive the device. Charge feed-through and leakage current influences can at least be reduced with a factor ten. As a result the calibrated current is much more accurate than was the case in the former system solution.

6.8.2 Continuous current calibration system

A system that uses a continuous current calibration is shown in Figure 6.38. The systems consists of a $N+1$ -bit shift register and $N+1$ current sources.

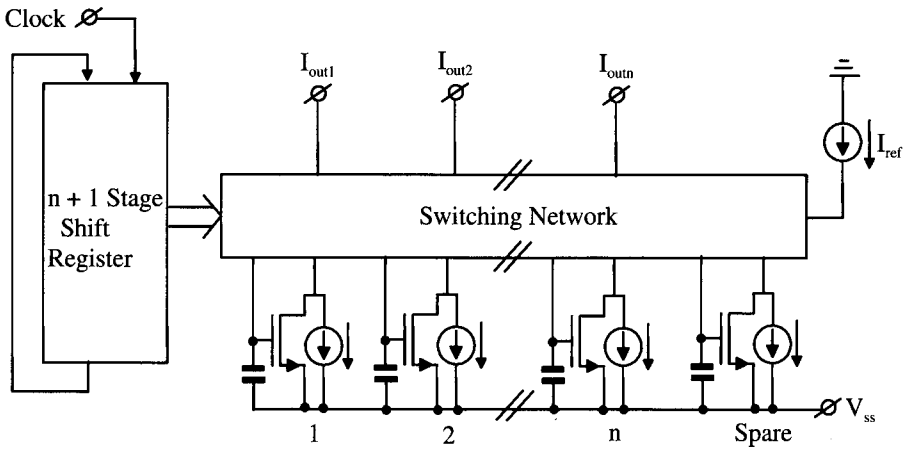


Figure 6.38: Continuous current calibration system [66]

The $N+1$ current source is called the "spare" source. The output of this system is N calibrated currents. The operation of the system is as follows. The $N+1$ stage shift register determines which current of the network is switched to the calibration source to be adjusted to the reference value I_{ref}. Successively every current is compared with the reference source I_{ref} and then inserted back into the system. The switching network performs the necessary switching operation to perform the calibration of every current source in the system. By using $N+1$ current sources no time is lost during calibration, because the current which is calibrated is replaced by the spare current source. In this way a continuous calibrated current network is obtained.

6.8.3 Practical current calibration implementation

In Figure 6.39 an example of a practical current calibration stage is shown. In the circuit transistor M_4 supplies the current I_m from the previous circuit. This is the main current source. Transistor M_1 holds the calibration current which is added to obtain an accurate value of I_{ref} of the total output current. The switches M_5, M_6, and M_7 perform the switching from calibration to operation of the current cell. When transistor M_5 is switched on, the switch

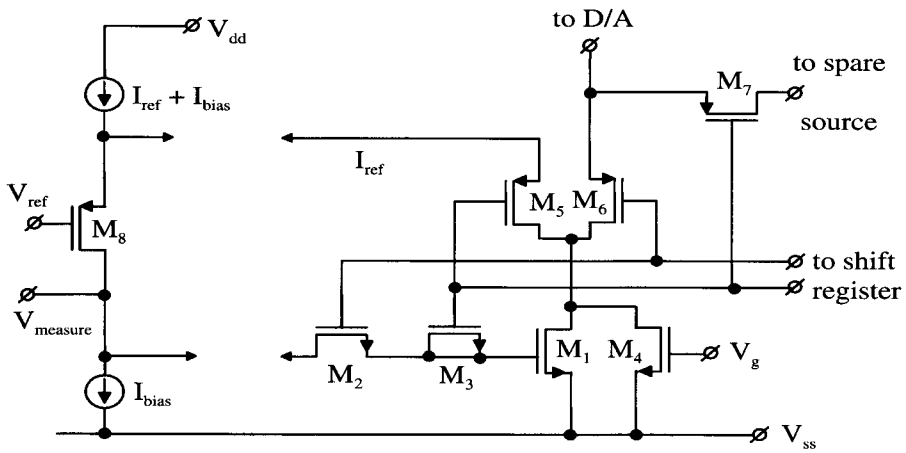


Figure 6.39: Practical current calibration circuit [66]

M_7 is switched on as well and the spare current is applied to the bit switches in the D/A converter part. At the same time switch M_2 is on and transistor M_8 connects the drain of M_1 with the gate. Note that a current I_{bias} is added to the reference current I_{ref}. This bias current is forward biasing transistor M_8 and is subtracted from this reference current by the current source I_{bias}. In this way a good speed of transistor M_8 is obtained under all conditions. Transistor M_3 is added to the system to compensate for the charge feed-through of M_2. Therefore, the gate of M_3 is connected to the inverse control voltage applied to M_2.

6.8.4 16-bit D/A converter system

An example of an MOS calibrated 16-bit D/A converter system is shown in Figure 6.40. The system consists of a 6-bit segmented current calibrated network to generate the six most significant bits. Current "64" is applied to a 10-bit binary weighted network using source scaling. In this way a 16-bit binary weighted current network is obtained. The digital input data which must be converted into an analog value are stored in the data register. The outputs of this data register controls the bit switches that switch the weighted currents to the output to obtain the converted analog value. The output current of the converter is converted into a voltage using an operational amplifier with a resistive feedback. To minimize the glitches that occur during the switching from calibration into output current generation of the MSB calibrated currents, a deglitcher can be implemented before the

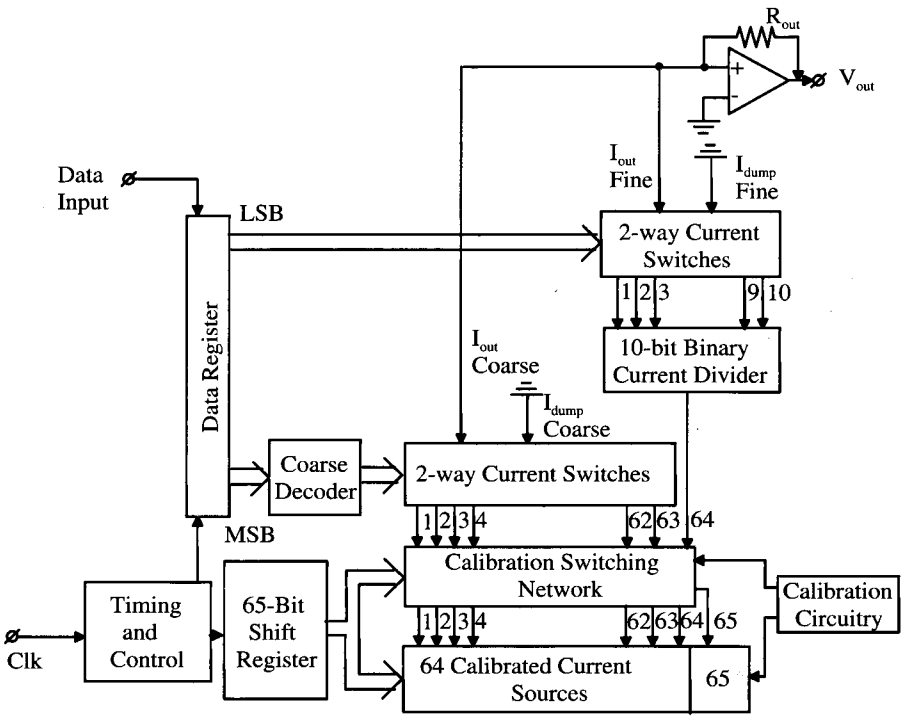


Figure 6.40: 16-bit current calibrated D/A converter system [66]

total output current is applied to the current to voltage converting operational amplifier. Another possibility exists by operating the deglitcher and calibration cycle at the same time the digital data applied to the switches are refreshed. A synchronization between shift register clock and input data clock is required.

6.8.5 Integral nonlinearity measurement

In Figure 6.41 the result of the integral nonlinearity measurement of the system shown in Figure 6.40 is shown. Due to the segmented construction

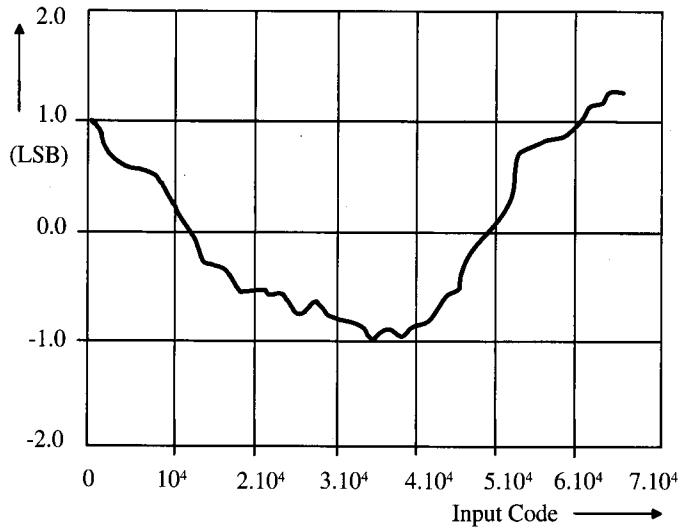


Figure 6.41: Integral nonlinearity measurement result [66]

of the converter, *monotonicity* is guaranteed while the integral nonlinearity in this case equals ± 1 LSB. The curve characteristic shows a strong dependence of the calibration accuracy on the position of the calibrated weighted current values. Layout improvements are possible to obtain a full 16-bit accuracy.

6.8.6 Dynamic performance measurement

In Figure 6.42 the measurement result of signal-to-noise plus distortion is shown as a function of the output amplitude. The measurement result shows that the dynamic performance is close to the expected theoretical value.

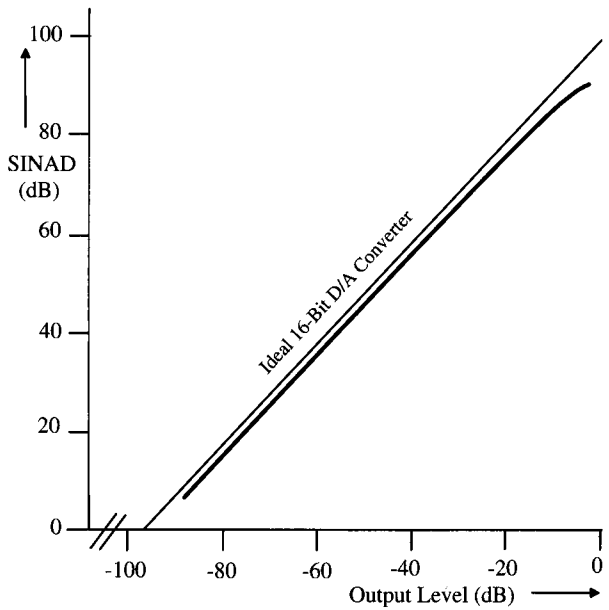


Figure 6.42: Signal-to-noise plus distortion as a function of amplitude [66]

6.8.7 D/A converter specifications

In Table 6.2 the specifications of the complete MOS 16-bit D/A converter are shown.

6.8.8 Some remarks about the ladder converter systems

In a 10-bit system, for example, the largest transistor has a size which is $2^{N-1} = 512$ times the size of the transistor in the least significant bit. Such a ratio in transistor size requires a large die size. Moreover, the output capacitance of the most significant bit current source is large due to the parallel connection of 512 transistors. Such a large capacitance has a drawback for the switching of this current to the output terminal. As a result it is difficult to operate all switches at the same speed. This switching at the exact same moment is required to obtain a small output glitch. Mostly a reference source is added to accurately determine the value of the MSB current of the converter. Technology studies in a bipolar or CMOS implementation of these types of converters show that without trimming an accurate converter of up to 10 bits can be designed. In that case this converter does not need any trimming to obtain the required linearity and monotonicity

Resolution	16 bits
Dynamic range	94 dB
S/(N + THD) at 0 dB	92 dB
S/(N + THD) at -10 dB	84 dB
Supply voltage range	3 to 5 V
Power dissipation	20 mW at 5 V
Temperature range	-10 to 70 degree C
Process	1.6 μm CMOS
Active chip area	3 mm^2

Table 6.2: 16-bit D/A converter specifications [66]

specification. Modifying the design in a multiple equal current generation and switching of two or more of the MSBs improves the monotonicity of the converter. Furthermore, the accuracy is increased by using more elements in parallel to generate the high current values. The law of the numbers increases the weighting accuracy by the square root of the number of elements used. To increase the accuracy of the R-$2R$ system a trimming procedure is needed. With trimming it is possible to obtain the high accuracy. However, the system becomes sensitive to material stresses and therefore needs to be trimmed after the die has been mounted in its encapsulation. An example of a trimmed high-resolution converter is given in reference [64]. Such procedures are fairly expensive.

6.9 Conclusion

In this chapter an overview of basic circuits has been presented. Systems with resolutions up to 10 bits do not require a calibration system. In monotonic designs resolutions up to 16 bits are possible. The only requirement is that with an increasing input code the output at least increases. This can be obtained by special circuit implementations that have a limited absolute accuracy.

At the moment the full specification for the converter is needed, calibration or trimming procedures are required. A special system is presented that makes it possible to divide currents with a very high accuracy without needing accurate elements. The method presented uses a combination of a passive divider with a dynamic interchanging method to improve the

final accuracy. After removing the error ripple by simply using low-pass filter structures D/A converters with accuracies from 14 to 18 bits can be designed. The circuits presented show a high accuracy and, by optimizing the dynamic behavior of the systems, an overall performance is obtained that is close to the theoretically possible behavior. In practice the *Dynamic Element Matching* system can be extended into generally applicable systems to obtain high-accuracy integer ratios of currents. A second method, which uses a continuous calibration principle of a multiple of equal reference currents, is very suitable for implementations in a CMOS technology. This system does not need external filtering. Furthermore, the use of an additional (spare) current makes a continuous calibration possible during the operation of the converter in a system.

A third self-calibration method makes a circuit less sensitive to component variations; however, during warming up of the system a re-calibration might be needed. During the calibration cycle the system is not able to produce an output signal. This might be a large drawback for many systems.

Chapter 7

Sample-and-hold amplifiers

7.1 Introduction

In this Chapter sample-and-hold amplifiers are discussed. In most cases practical implementations of these amplifiers are track-and-hold amplifiers. During the sampling mode the input signal is "tracked" and a sample is taken at the moment the system is switched into the hold mode. A sample-and-hold amplifier samples the analog input signal during a short time and then holds the signal during the full clock period giving the analog-to-digital converter about twice the time to perform the conversion as in the case of a track-and-hold amplifier.

The terminology sample-and-hold amplifier will be used in this chapter although most systems are track-and-hold amplifiers.

A sample-and-hold amplifier is a crucial part in a high-speed or high-resolution A/D converter system. Using a very simple model of a sample-and-hold amplifier, a number of specifications will be analyzed and the optimum switch configuration will be defined. Next, different circuit configuration options for sample-and-hold amplifiers will be discussed. An important factor is charge feed-through when a sample-and-hold amplifier is switched from the track mode (or sample mode) into the hold mode. Furthermore, this charge feed-through must be signal level independent to avoid distortion. Single ended circuit implementations are limited by charge feed-through. An optimum circuit configuration is obtained with a differential system implementation. Overall A/D converter system performance, such as dynamic range, distortion, SFDR, and noise, are largely dependent on the sample-and-hold

amplifier. Examples of single ended and differential sample-and-hold circuits will be discussed.
In submicron CMOS technology the supply voltage is reduced to about 1 V. This reduction in supply voltage has significant influence on the switching performance of PMOS or NMOS switches. Especially when switches are bias around half the supply voltage, then the on resistance will become large. This is not allowed because of the large distortion and noise such a switch introduces. To overcome this problem, clock bootstrapping with high voltage MOS devices is used for the switches. Different system implementations will be discussed. Furthermore a distortion analysis is given showing the influence of the rise or fall time of the sampling clock when a single MOS device is used as a sampling switch.
Separate designs of sample-and-hold amplifiers are very limited described in literature. Mostly the S/H amplifier is part of a converter design and many times even there the description of this functional block is very limited.

7.2 Basic sample-and-hold configuration

The simplest form of a non-inverting sample-and-hold circuit consists of a switch S with ON resistance R_s and the hold capacitor C_H. At the input of the circuit a voltage source V_{in} is applied. A circuit with basically an infinite input impedance must be used to sense the output voltage V_{out} available across the hold capacitor. In this simple system this "hold" mode amplifier is not shown. The information is stored as charge on the capacitor C_H. To avoid voltage droop a low leakage capacitor must be used with a small dielectric adsorption. The dielectric adsorption can result in voltage changes during the hold mode. As an example, a fully discharged capacitor may still show a voltage across the terminals after the short circuit switch, used to discharge the capacitor, is opened. The basic system is shown in Figure 7.1. This simple circuit can be used to determine some of the most important limitations of a sample-and-hold system.

7.2.1 Signal bandwidth

The small signal bandwidth of the system is determined by the ON resistance of the switch R_s optionally enlarged with the output impedance of the signal source driving this system. We obtain for the small signal bandwidth:

$$f_{-3\ dB} = \frac{1}{2\pi R_s C_H}. \tag{7.1}$$

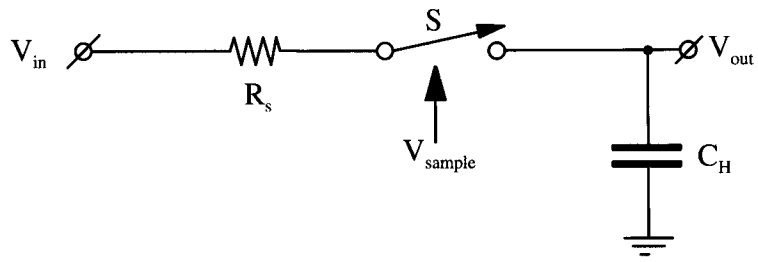


Figure 7.1: Basic sample-and-hold configuration

Suppose that the maximum input signal voltage the system can operate with is V_{max} then the large signal bandwidth is equal to the small signal bandwidth when the current through the switch and the current of the input driver stage is equal to:

$$I_{max} = \frac{V_{max}}{R_s}. \tag{7.2}$$

When the input driver cannot supply enough current or the ON resistance of the switch R_s is dependent of the signal, then a smaller large signal bandwidth will be obtained. Mostly the switch resistance R_s increases when the input signal reaches the maximum supply voltage of the system. The smaller current results in a "slewing" of the signal across the capacitor during the track mode. The maximum rate of change during the "slewing" is equal to:

$$\frac{dV}{dt} = \frac{I_{source}}{C_H}. \tag{7.3}$$

Here I_{source} is the maximum current the source can apply to charge the capacitor C_H.

7.2.2 Acquisition time

The acquisition time of the sample-and-hold circuit can be calculated by applying a full-scale step to the system. The output signal becomes:

$$V_{out} = V_{in}(1 - e^{\frac{-t}{R_s C_H}}) \tag{7.4}$$

Equation 7.4 is very easy to analyze in regard to the final settling. In Table 7.1 the settling time as a function of the final accuracy is shown. The results of Table 7.1 are valid as long as the input signal source can deliver the maximum current defined by equation 7.2. When the signal source or

Accuracy	Time constants R_sC_H
10 %	2.3
1 %	4.6
.1 %	6.9
.01 %	9.2
.001 %	11.5
.0001 %	13.8

Table 7.1: Accuracy as a function of acquisition time

the switch cannot deliver such a large current, then the acquisition time will increase. The acquisition time in this situation is equal to the "slew" time plus the settling time during the non-slew operation of the system.

7.2.3 Aperture time accuracy

In the circuit shown in Figure 7.1 the switch S is controlled by the sample pulse. In an ideal case this pulse has infinitesimal small fall times. However, in a practical application a finite rise and fall time of the sampling pulse is found. When we assume, furthermore, that the switching from track to hold occurs at the moment the analog input signal and the sample signal are equal, then an alteration of the sample moment is found. This sample moment alteration is previously defined as aperture uncertainty time. In Figure 7.2 this phenomenon is shown as $\Delta\ t_s$. As a result of this signal-

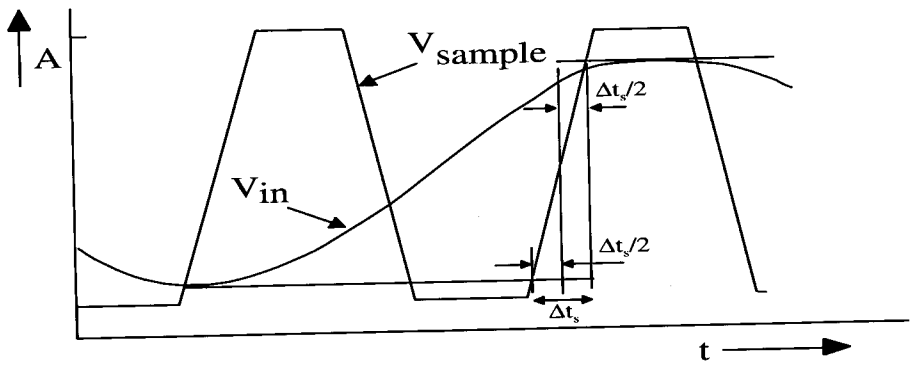


Figure 7.2: Signal-dependent sampling moment

dependent sampling, the aperture time of the sample-and-hold circuit is not constant. Sampling of the input signal is not performed at equidistant time intervals, resulting in distortion after the signal is reconstructed at equal time intervals. This problem can be overcome by bootstrapping the switch control signal with the analog input signal. The switch is always controlled at equidistant time intervals. Another solution is obtained by changing the system implementation in such a way that the switch is always activated around a fixed bias point, which preferably is ground level. A further advantage of this switch operation is found in a signal independent feed-through of the control signal on the "hold" signal. Furthermore, the switch performance is not influenced by the back-bias of the substrate which is the case in a bootstrapped system configuration.

7.2.4 Sampling moment distortion calculation

At the moment an input signal is applied to a sample-and-hold switch then the sampling moment varies according to the input signal. This variation in sampling moment will result in distortion.
Suppose that the sampling clock has a linear rise and/or fall time. Then the timing variation can be found as:

$$\Delta t_s = 2\frac{a}{V_{clock}} t_{rise}. \tag{7.5}$$

With a the amplitude of the input signal and V_{clock} the amplitude of the (linear) rising or falling sampling clock.
In case an input signal $a\sin(\omega t)$ is applied then a sampling time variation due to the input signal amplitude is obtained. So we get:

$$\frac{\Delta t_s}{2} = \frac{a}{V_{clock}} t_{rise} \sin(\omega t) = \Delta t_a \sin \omega t. \tag{7.6}$$

The output sampled signal can be calculated from:

$$V_{out} = a \sin \omega (t + \Delta t_a \sin \omega t). \tag{7.7}$$

Working out this equation gives:

$$V_{out} = a \sin \omega t \cos(\omega \Delta t_a \sin \omega t) + a \cos \omega t \sin(\omega \Delta t_a \sin \omega t) \tag{7.8}$$

When the rise and/or fall time of the sampling clock is small then

$$\omega \Delta t_a \sin \omega t \ll 1. \tag{7.9}$$

The output signal can be approximated by:

$$V_{out} \approx a \sin \omega t + a\omega \Delta t_a \cos \omega t \sin \omega t. \tag{7.10}$$

This equation shows that a dc component and a second order component will be found in the sampled output signal. Working out the equation gives:

$$V_{out} \approx \frac{a}{2}\omega \Delta t_a + a \sin \omega t + \frac{a}{2}\omega \Delta t_a \sin 2\omega t. \tag{7.11}$$

The second order distortion can be found as:

$$d_2 = \frac{\omega \Delta t_a}{2} = \frac{a}{2V_{clock}}\omega t_{rise}. \tag{7.12}$$

In decibels this becomes:

$$d_2(dB) = 20 \log(\frac{a}{2V_{clock}}\omega t_{rise}) = 20 \log(\frac{a}{V_{clock}}\pi f_{sig} t_{rise}). \tag{7.13}$$

Inserting values for $t_{rise} = 100$ psec, $V_{clock} = 1.2$ V, $a = 200$ mV and $f_{sig} = 100$ MHz the second order distortion due to finite clock rise time becomes:

$$d_2 = -45.6dB. \tag{7.14}$$

With the limited signal swing of 200 mV and the maximum clock signal of 1.2 V the second order distortion is low enough to obtain 7-bit resolution in a high-speed converter. To reduce the second order distortion two options are possible:

- Differential circuit configuration
- Bootstrapping of clock signal

7.2.5 Differential sample-and-hold circuit

By using a differential circuit solution the second order distortion will be reduced and in the ideal case a third order distortion component might be dominant. In Fig. 7.3 a differential circuit implementation is shown. In practical situations the on resistances R_{s1} and R_{s2} are not exactly equal, while the hold capacitors C_{H1} and C_{H2} might have a certain mismatch. To incorporate these mismatches a mismatch parameter k will be used. In the ideal case k =1 while practical mismatches between the switch on resistances

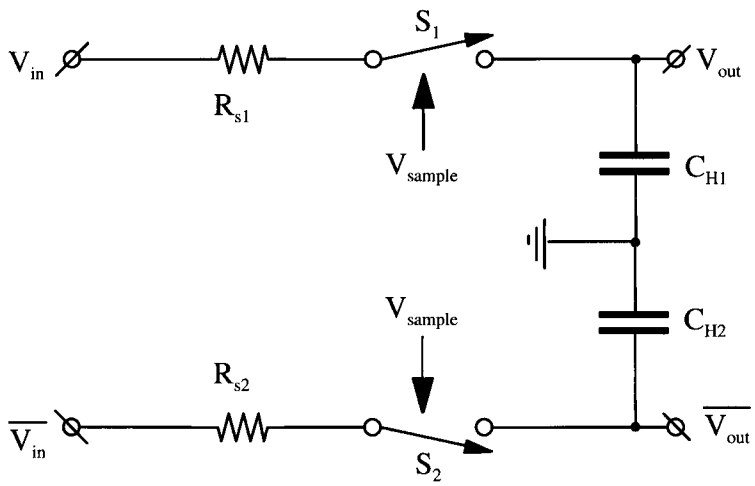


Figure 7.3: Differential S/H circuit implementation

in the order of 10% are possible. In the distortion calculation the mismatch parameter k will be used. The output signals become:

$$V_{out} = a \sin \omega(t + \Delta t_a \sin \omega t) \tag{7.15}$$

$$\overline{V_{out}} = -ka \sin \omega(t - \Delta t_a \sin \omega t). \tag{7.16}$$

The differential output signal becomes:

$$V_{out} - \overline{V_{out}} = a \sin \omega(t + \Delta t_a \sin \omega t) + ka \sin \omega(t - \Delta t_a \sin \omega t). \tag{7.17}$$

Working out this equation then we obtain for the second order distortion:

$$d_2 = \frac{1-k}{2(1+k)}\omega \Delta t_a = \frac{1-k}{1+k}\frac{a}{V_{clock}}\pi f_{sig} t_{rise}. \tag{7.18}$$

In Decibel this becomes:

$$d_2(dB) = 20 \log(\frac{1-k}{1+k}\frac{a}{V_{clock}}\pi f_{sig} t_{rise}). \tag{7.19}$$

In case $k = 0$ then the earlier derived result is obtained.
With $k = 1$ then an ideal cancelation of the second order distortion is found.
The third order distortion independent of k becomes:

$$d_3 = \frac{1}{8}\omega^2 \Delta t_a^2 = \frac{\pi^2}{2}(\frac{a}{V_{clock}})^2 (f_{sig} t_{rise})^2. \tag{7.20}$$

Again in Decibels the third order distortion becomes:

$$d_3(dB) = 40\log(\frac{\pi}{\sqrt{2}}(\frac{a}{V_{clock}})(f_{sig}t_{rise}). \quad (7.21)$$

Inserting values for $t_{rise} = 100$ psec, $V_{clock} = 1.2$ V, $a = 200$ mV and $f_{sig} = 100$ MHz the third order distortion due to finite clock rise time becomes:

$$d_3 = -97.3dB. \quad (7.22)$$

This result is obtained with $k = 1$.
In case $k = 0.9$ then a second order distortion component appears equal to:

$$d_2 = -71.2dB. \quad (7.23)$$

This calculation shows that a good matching between the two channels is required to obtain a very low distortion.

7.2.6 Sample clock bootstrapping

From the distortion equations derived it is found that with an increase in sampling clock amplitude V_{clock} the distortion can be reduced. The distortion reduction, however, goes linear with the clock amplitude. This means that with an increase in clock amplitude with a factor of 2 a distortion reduction with about 6 dB is obtained. This might be enough under certain design constraints. To obtain a bootstrapping of the sample clock the circuit shown in Fig.7.4 can be used. In this circuit the transistor indicated with "Switch" is the sampling switch of the sample-and-hold circuit. The operation will be explained starting with the input clock signal to be high. At the output of the first inverter a low signal is obtained. The capacitor C_1 will then be charged to V_{dd} - V_{gs1}. Transistor M_1 acts as an MOS diode and connects one side of the capacitor C_1 to V_{dd}. Furthermore the output signal of the second inverter is high. This means that transistor M_3 is in the triode region and connects the gate of the switch to ground. Transistor M_2 is open because the V_{gs3} of this transistor is zero or even reversed due to the on voltage of diode M_1. When the input clock signal becomes high, then the output of the first inverter becomes high. Capacitor C_1 is charged to about V_{dd}. This voltage adds to the output voltage of the first inverter and reverse biases the diode M_1. The output of the second inverter becomes low and as a result transistor M_2 will be switched on and connects one side of the bootstrapped voltage of the capacitor C_1 to the gate of the switch. This bootstrapping results roughly in a doubling of the gate-source voltage

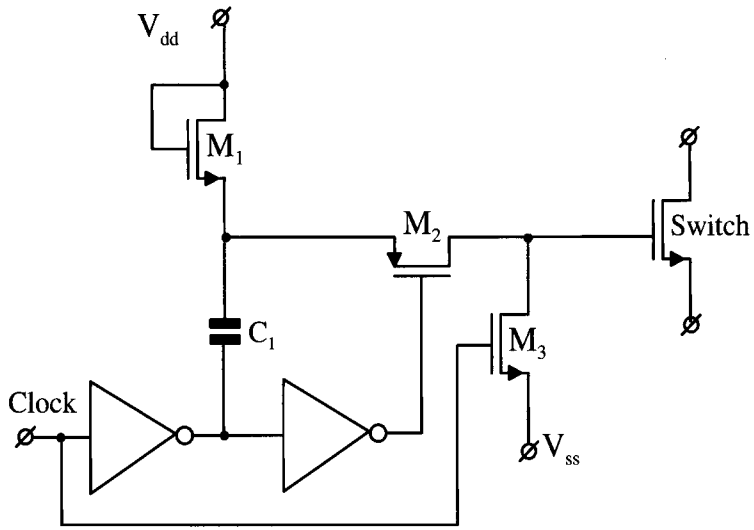


Figure 7.4: Sampling clock bootstrap circuit

of the switch transistor. With a low of the input clock signal transistor M_3 is switched off. As already indicated before a reduction in distortion with about 6 dB can be obtained with this circuit. In many cases this will not be enough. Therefore improved circuits are needed. Furthermore the switch transistor must of a "high"voltage type. In most CMOS processes such a device is available.

7.2.7 Differential sampling clock bootstrap circuit

A modification to the circuit of Fig. 7.4 uses a differential operation of the system shown in Fig. 7.5. The capacitors C_1 and C_2 with the transistors M_1 and M_2 and the inverter perform the clock bootstrapping. Suppose the system starts with the clock signal high, then the output of the inverter is low and with discharged capacitors C_1 and C_2, the gate of M_2 becomes high and the capacitor C_2 will be charged to the supply voltage V_{dd}. Transistor M_3 is switched off and M_4 connects the gate of the switch to ground (V_{ss}). When the clock becomes low, then the output of the inverter becomes high and the voltage across C_2 will be added to obtain the nearly doubled output switch voltage. The gate of M_3 is low so this transistor connects the bootstrapped clock voltage to the gate of the switch transistor. At the same time transistor M_4 is switched off. The high voltage at the gate of M_1 puts this transistor into the triode region giving a small R_{on} resulting in the supply voltage to

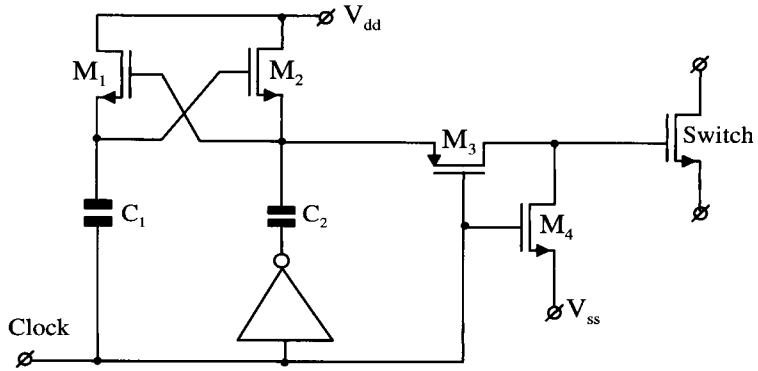


Figure 7.5: Differential clock bootstrap circuit

be fully applied to the capacitor C_1. During the next clock phase transistor M_2 will obtain a large gate voltage so this transistor will go into the triode region resulting in a full V_{dd} to be applied to capacitor C_2. A doubling of the sampling clock signal is obtained with this circuit.

7.2.8 Low signal feedthrough switch

In case a single sampling switch is used, then during the open position of the switch only a parasitic capacitance between the source and the drain terminal of the switching device is present. In high resolution and/or high frequency applications this capacitance can introduce capacitive feedthrough of high frequency signals. This might influence the "hold" information on the capacitor and result in distortion. To overcome this problem a more complex switch must be used. The circuit in Fig. 7.6 gives a solution to the feedthrough problem. The system uses a double sampling switch using M_1 and M_2 and a ground switch M_3. When the system is in sampling mode, then the clock signal is high and switches M_1 and M_2 are on. The signal passes through the switch to the output terminal. Transistor M_3 is off and shows a very high impedance. When the clock signal is low, then M_1 and M_2 are off and show a parasitic capacitance between source and drain only. Transistor M_3 is on and switches the sources of the switch transistors to ground (V_{ref}). The parasitic source to drain capacitance of M_1 is switched to ground and a large reduction in switch feedthrough is obtained.

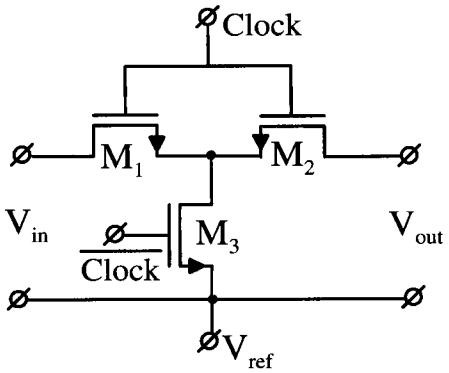


Figure 7.6: Low signal feedthrough switch

7.2.9 Time interleaved sample-and-hold

An example of a time interleaved sample-and-hold system is shown in Fig. 7.7 [115]. A single channel solution of a time interleaved solution is shown.

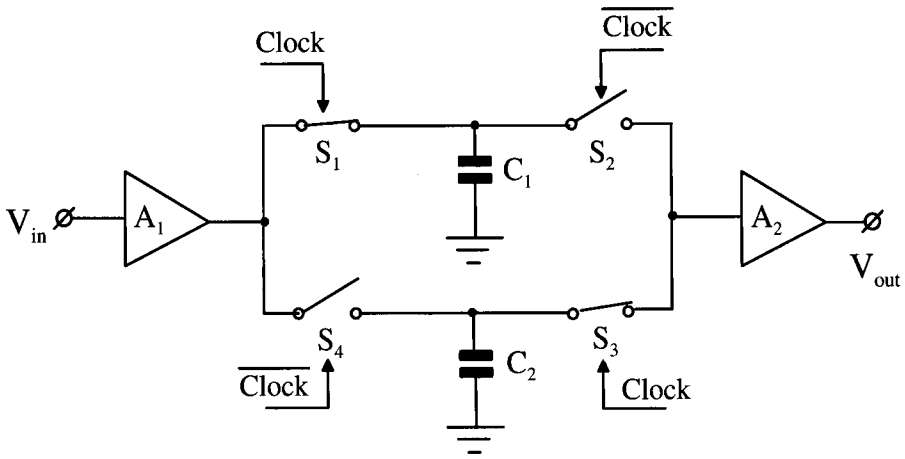


Figure 7.7: Time interleaved sample-and-hold system [115]

The system uses an input amplifier A_1, and output amplifier A_2, 4 switches S_1 to S_4 and two hold capacitors C_1 and C_2. Mostly the input and output amplifiers are buffer stages with a limited gain. Suppose that the clock signal is high, then switches S_1 and S_3 are closed. The other two switches are open as shown in Fig. 7.7. The input signal during this clock mode is sampled on capacitor C_1 while the previous sample held on capacitor C_2 is

applied to the output amplifier to obtain the sampled output signal. At the moment the clock signal becomes low, then switches S_2 and S_4 are closed. The next sample is sampled on capacitor C_2 and the sampled signal held on capacitor C_1 is applied to the output amplifier to obtain the sampled output signal. As a result of this operation, at the output of amplifier A_2 a stream of sampled analog data is available for conversion into a digital value by a connected analog-to-digital converter.

7.2.10 Signal dependent clock bootstrapping

To reduce the distortion of a single switch furthermore an even more enhanced clock bootstrapping system is needed. As long as the switching on or switching off moment of a CMOS transistor occurs at the same time moment, then the variation in sampling moment due to the input signal to be sampled is avoided. This means that the switching signal must be applied directly between the gate and the source of a switching device independent of the applied signal level. The only problem that is left in such a system is the back-gate modulation of the gate-source threshold voltage. This problem will be discussed in a following section. The basic solution discussed here is shown in Fig. 7.8. In this circuit the fixed clock signal is added to the input

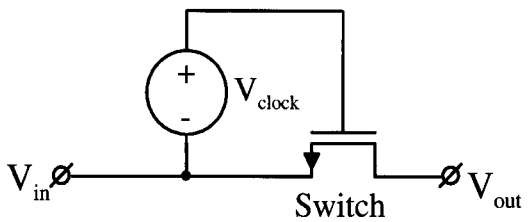


Figure 7.8: Basic clock bootstrap solution

signal and drives the switch. As a result of this operation the gate-source voltage of the switch is driven by a nearly constant clock voltage equal to V_{dd}. The on resistance and the moment of switching are only modulated by the back-gate modulation of the threshold voltage of the switch. A rather large reduction in distortion is obtained using this construction.

7.2.11 Simple signal clock bootstrap system

A circuit solution using the principle of Fig. 7.8 is shown in Fig. 7.9. A single capacitor C_3 is used to bootstrap the sampling clock signal. The

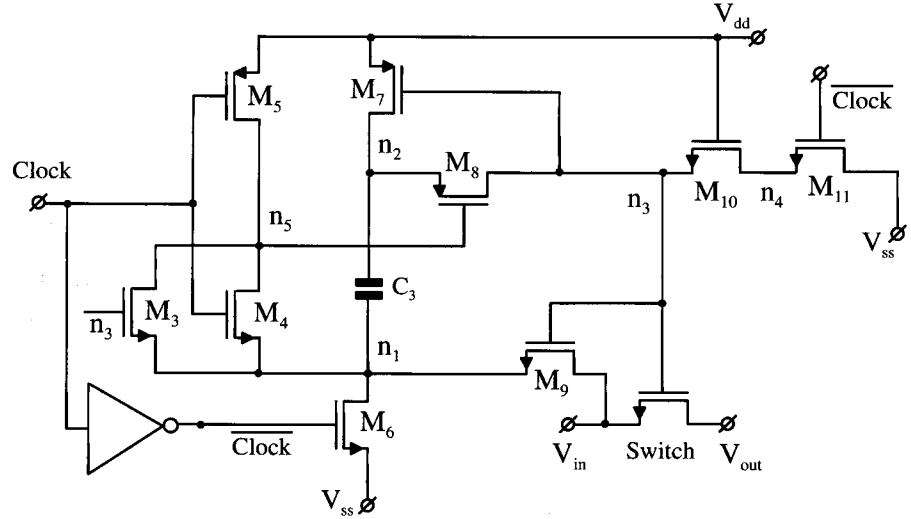


Figure 7.9: Simple clock signal bootstrap system

operation of the system is as follows. Suppose the clock signal is low, then transistor M_5 will be switched on making node n_5 high. This results in a switching of transistor M_8. At the same time $\overline{clock}$ is high. This means that transistor M_6 is switched on and node n_1 will be at V_{ss}. At the same time transistor M_{11} will be switched on and via M_{10} the gate of M_7 will be at V_{ss}. This connects node n_2 to V_{dd}. As a result of this operation the capacitor C_3 will be charged to V_{dd} - V_{ss}. Because node n_3 is at V_{ss} transistor M_9 will be off so is the switch. When the clock goes high, then node n_5 will become low. This will switch on M_8 making M_7 acting as an MOS diode. The voltage at node n_3 becomes high and M_9 will be switched on. The input signal is now applied at node n_1 and the stored voltage on capacitor C_3 will increase furthermore the node voltage n_2 and via M_8 node voltage n_3. As a result the switching voltage of the switch is added to the input signal level and with the full voltage on C_3 a low impedance of the switch is obtained. During this operation M_{11} and M_{10} are switched off so no effect on node voltage n_3 is found. The input signal applied to this switch is loaded with extra parasitics from the bootstrapping transistors M_6, M_7, M_8 M_4 and M_3. This might require a low source impedance of the input signal. This can be obtained using an extra input buffer.

7.2.12 Modified signal clock bootstrap system

A modification using a differential clock bootstrapping system is shown in Fig. 7.10 [119]. A differential system is used to bootstrap the input clock.

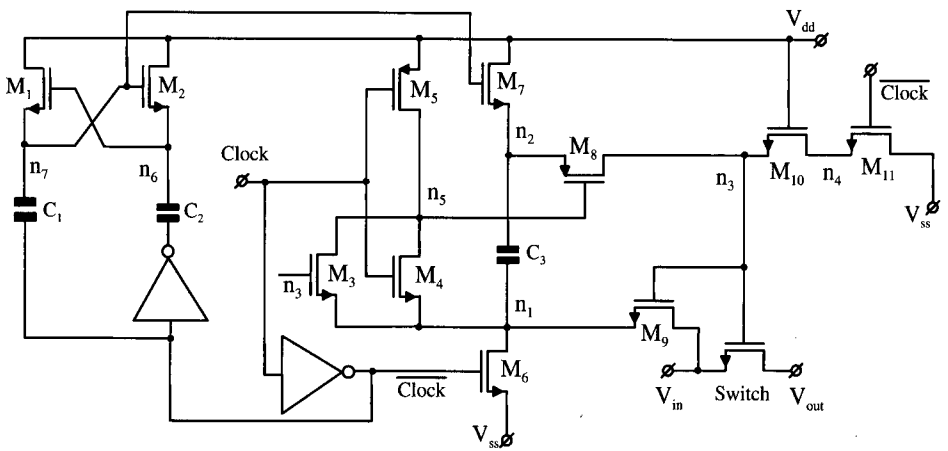


Figure 7.10: Modified signal clock bootstrap system [119]

This system uses transistors M_1 and M_2 with capacitors C_1 and C_2 and the inverter stage to obtain at the gate of M_2 a nearly doubled clock signal. This clock signal switches transistor M_7 on at the moment bootstrap capacitor C_3 must be charged. As can be seen from this figure transistor M_7 is modified from a p-channel device into an n-channel device. Furthermore the same operation as found from the circuit from Fig. 7.9 is obtained. The advantage of this circuit is that the maximum supply and signal swings do not exceed double the supply voltage of this circuit.

7.2.13 Gate and bulk bootstrapping system

At the moment the influence of the bulk voltage on the switching moment has to be reduced, then a bootstrapping of the bulk and gate voltage of the switching device is needed [140]. In many CMOS processes the p-channel devices have a separate connection to the bulk. This bulk can be controlled by an external voltage depending on the signal voltage applied to the switch. In Fig. 7.11 a system that uses gate and bulk bootstrapping is shown. The generation of the different required clock signals is shown in the bottom part of the figure. Note that in this system p-channel devices are used instead of n-channel devices from the previous designs. The switch is shown

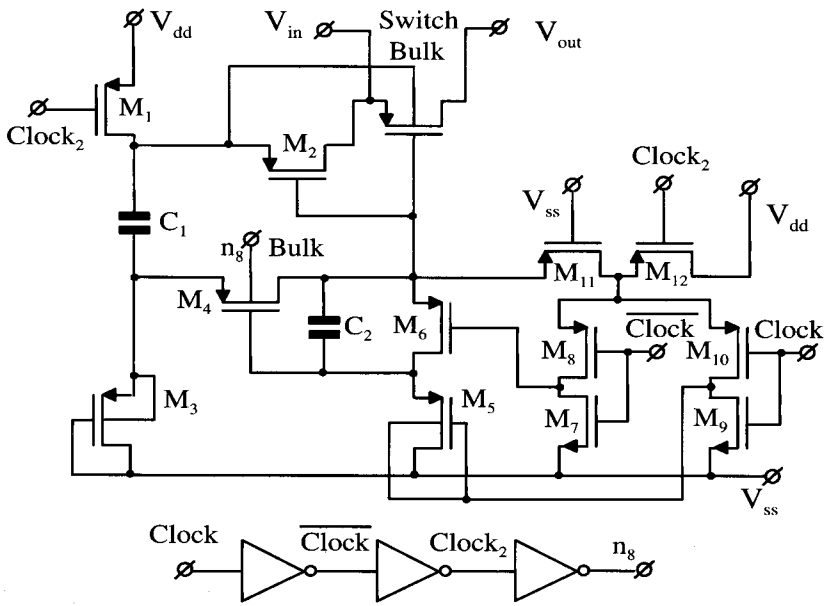


Figure 7.11: Bulk and signal clock bootstrap system [140]

in the top part of the figure with an indication that the bulk voltage is bootstrapped with the input signal too. Gate bootstrapping is introduced via capacitor C_1, while with capacitor C_2 the required switching voltages are generated to obtain the bulk bootstrapping via transistor M_2 and the gate bootstrapping via M_4. M_1 and diode M_3 perform the simple charging of the supply voltage on the bootstrap capacitor C_1 as has been shown before with n-channel devices. The extra negative voltage required to switch on M_4 is obtained via the bootstrap capacitor C_2. Using this system it is possible to reduce the uncertainty in sampling moment and the modulation of the on resistance of the switch further.

7.2.14 Double sided bootstrapping

In some applications it might be important that the on switching of the switch is controlled depending on the input and output voltages across the switch [140]. To perform such an operation the input and output voltages of the switch are sensed. A double bootstrap system is introduced as shown in Fig. 7.12. The system consists of two simple bootstrap circuits. One circuit senses the input signal of the switch, the other senses the output signal of the switch. In some applications, the output signal might be at a higher

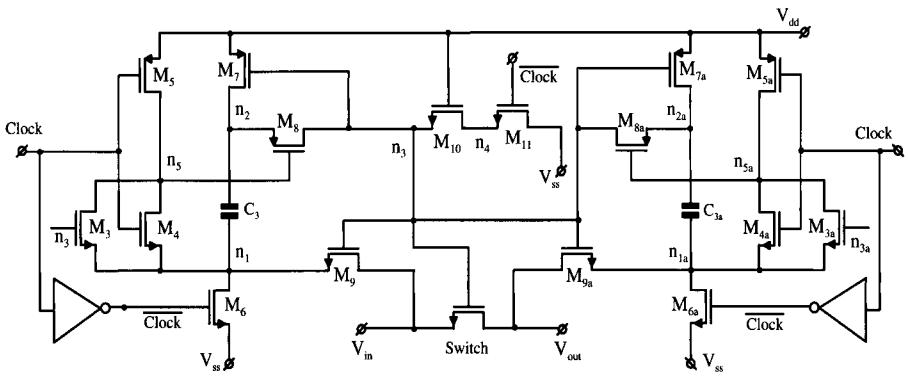


Figure 7.12: Double sided bootstrap system [140]

signal level then is the case of the input signal. This can be the case that the top of a sine wave is sampled and stored on the hold capacitor, then the switch is opened and the input signal will go to the lowest signal level. Switching on then occurs between the gate signal and the input signal, while in the opposite condition with the lowest signal stored on the hold capacitor, then the switch will be controlled by the gate-drain voltage. In this case the drain becomes a source and the switch will then be switched on with positive gate to drain (source) voltage. Different moments of on- switching might occur. By sensing the input and the output signal levels, the switching on can be controlled. In the given circuit of Fig. 7.12 the average bootstrap signal is applied to the gate. Capacitors C_3 and C_{3a} can have half the value of the original single bootstrap design. During the switching on of M_9 and M_8 and M_{9a} and M_{8a} the charge on C_3 and C_{3a} is redistributed and the average bootstrap gate voltage is applied to the system. In case an accurately determined switching on is required, then a minimum signal detection has to be included in the system to perform this operation.

7.2.15 Sample and hold mode errors

In this simple example an ideal switch is used. As a result, no track mode offset is introduced. Furthermore, at the moment the switch is opened no hold mode error is found. When practical switches are used, the following will be found:

1. Bipolar technology
   During track mode a switch offset can be introduced resulting in a track mode offset.
   Track-to-hold step is obtained by feed-through of the sampling pulse and possible charge stored in the device.

2. MOS technology
   No offset during track mode. A MOS device in the triode region behaves like a resistor. In a switch the MOS device is mostly used in the triode region.
   Track-to-hold step introduced by feed-through of the sampling pulse and channel charge in the device. The size of the step depends on the speed the switch is turned off.

7.2.16 MOS switch charge injection

To a designer it is important to know what effects are causing the charge feed-through and charge injection of MOS devices when used as a switch. In Figure 7.13 a simplified model of a sample-and-hold is shown [108, 109]. The system consists of the input signal source V_i with source resistance R_i

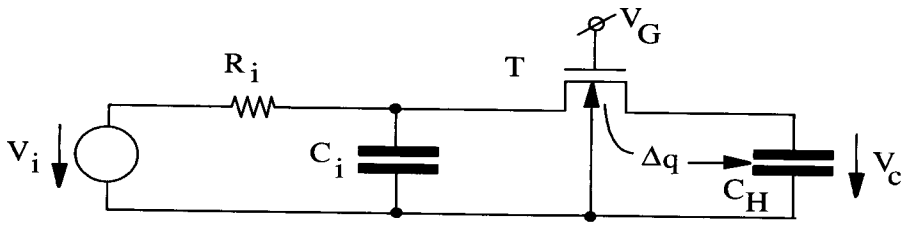


Figure 7.13: Simplified model of a MOS sample-and-hold [108, 109]

and source capacitance C_i, the MOS switch T, and the hold capacitor C_H. C_i includes the junction capacitance of the drain or source of the device. Turning ON of the switch is obtained when the gate voltage V_g equals V_{gon}. Switching OFF occurs when the gate voltage is below the threshold voltage V_{th} of the device. In this case sub-threshold effects are neglected.

At the moment a device is turned off, then the gate charge Q_g must be released. The amount ΔQ_g that flows to the hold capacitor C_H causes the charge feed-through, resulting in a track-to-hold step $\Delta V_H = \frac{\Delta Q_H}{C_H}$. In [108] is has been shown that the amount of charge that flows to the substrate can be neglected in most practical cases.

To obtain an accurate sample-and-hold system the switch-off time of the MOS transistor is much smaller than the time constant R_iC_i. In this case a small aperture time is obtained. This assumption simplifies the analysis of the problem. In Figure 7.14 a distributed model for the MOS device embedded as a switch in the sample-and-hold system is shown. The to-

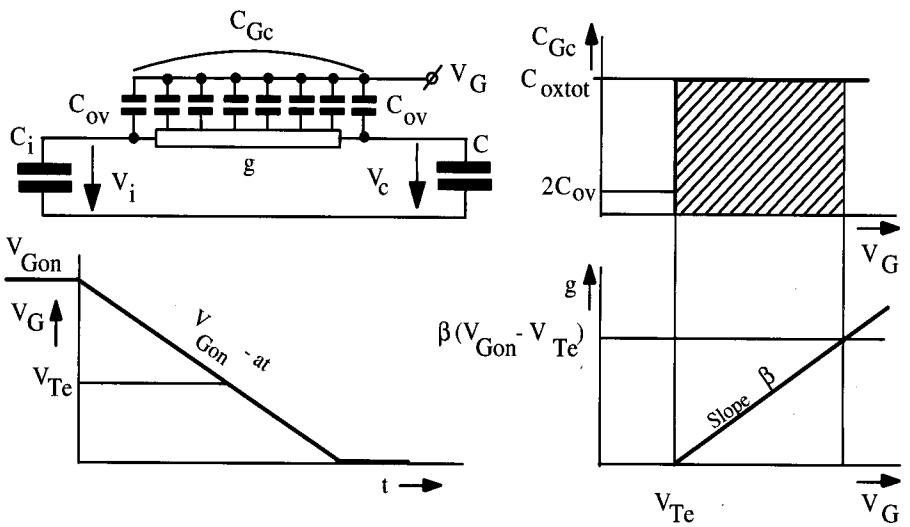


Figure 7.14: Distributed MOS sample-and-hold model [108]

tal gate capacitance C_{GC} of the device is built-up from a distributed gate capacitance (total value WLC_{ox}) and two overlap capacitances C_{ov}. In a symmetrical device both overlap capacitors are equal. W is the width of the device and L is the length. Furthermore, in this model g_{ch} is the channel conductance of the device. The channel conductance g_{ch} can be expressed in device parameters resulting in:

$$g_{ch} = \beta(V_g - V_{Te}), \tag{7.24}$$

with

$$\beta = \mu C_{ox}\frac{W}{L} \tag{7.25}$$

and

$$V_{Te} = V_{T0} + bV_{CH_n}. \tag{7.26}$$

Here V_{Te} is the effective threshold voltage of the device. This threshold voltage is influenced by the bulk modulation effect b and the voltage across the hold capacitor V_{CH_n} during the track mode. When the switch is ON,

then the total gate capacitance C_{GC} is equal to $WLC_{ox} + 2\ C_{ov}$.

At the moment the switch is OFF, the total gate capacitance C_{GC} becomes $2\ C_{ov}$, because g = 0.

Assume, furthermore, that the gate voltage linearly decreases with time starting from the ON voltage V_{GON}:

$$V_G = V_{GON} - at. \tag{7.27}$$

The slope a of the gate control pulse can be expressed in fall time t_{fall} (10 % to 90 %) and maximum amplitude V_{max} or:

$$a = \frac{0.8V_{max}}{t_{fall}}. \tag{7.28}$$

Inserting 7.28 into equation 7.27 gives:

$$V_G = V_{GON} - \frac{0.8V_{max}}{t_{fall}}t. \tag{7.29}$$

Suppose that due to charge feed-through on the hold capacitor the voltage change ΔV_{CH} is small with respect to $V_{GON} - V_{Te}$, then the potential at each end of the channel conductance g may be considered equal. When, furthermore, it is assumed that the voltage drop across the channel is neglectable even during the decrease of the gate voltage, then the model of Figure 7.14 can be decomposed into the model shown in Figure 7.15. The validity of

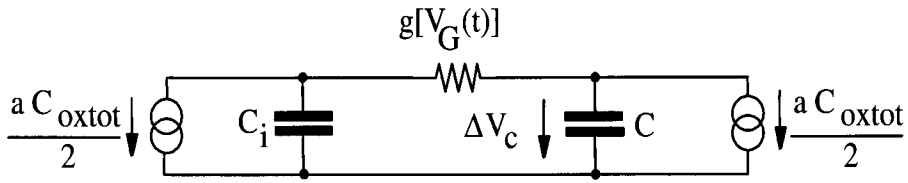


Figure 7.15: Decomposed sample-and-hold charge injection model [108]

this model has been proven in [108] and [109]. The linear decrease of the gate voltage V_G from V_{GON} across C_{GC} is thus equivalent to current sources $\frac{aC_{GC}}{2}$ flowing at both ends of the channel. Now the following differential equation holds for the model of Figure 7.15 including 7.24 and 7.27:

$$\frac{dU}{dT} = (T - B)[(1 + \frac{C}{C_i})U + 2\frac{C}{C_i}T] - 1. \tag{7.30}$$

The following normalized variables are introduced:

$$U = \frac{\Delta V_{CH}}{\frac{C_{ox}}{2}\sqrt{\frac{a}{bC}}} \qquad \text{(normalized voltage error)} \qquad (7.31)$$

$$T = \frac{t}{\sqrt{\frac{C}{a\beta}}} \qquad \text{(normalized time)} \qquad (7.32)$$

and

$$B = (V_{GON} - V_{Te})\sqrt{\frac{\beta}{aC}} \qquad \text{(switching parameter).} \qquad (7.33)$$

For U = 0 and T = 0, the numerical integration of 7.30 from T = 0 to T = B yields the value for U until the transistor is switched off ($V_G = V_{Te}$). The value of $\frac{\Delta Q_H}{Q_H}$ can then easily be deducted from U. The value of $\frac{\Delta Q_H}{Q_H}$ is plotted in Figure 7.16 as a function of the switching parameter B with the ratio $\frac{C}{C_i}$ as a parameter. The first design choice a designer can make is:

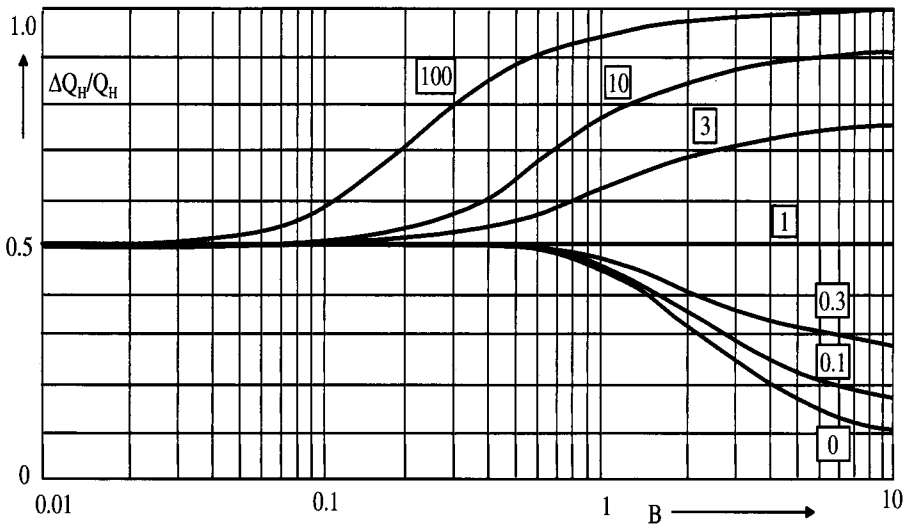


Figure 7.16: Hold charge injection plot [108]

$$\frac{C}{C_i} \ll 1 \qquad \text{and} \qquad B \gg 1. \qquad (7.34)$$

This choice results in most of the charge to flow back onto C_i. The large B is obtained by using a small fall time for the sampling pulse. At the moment

the device is switched off, a residual effect due to the overlap capacitance C_{ov} remains. This overlap results in a small charge injection on the hold capacitor C_H. A minimum over-drive of the gate voltage below V_{Te} minimizes this charge injection.

A second design choice is to choose a symmetrical (mostly differential) circuit configuration:

$$C = C_i. \qquad (7.35)$$

A fully symmetrical device with equal overlap capacitances is needed. As a result of this operation, half the charge is stored on the input capacitance C_i and the other half is stored on the hold capacitor C_H. A compensation of the charge feed-through is possible by introducing at both ends of the switches dummies that are half the size of the switching device. In Figure 7.17 this compensation scheme is shown. The half-sized dummy switches

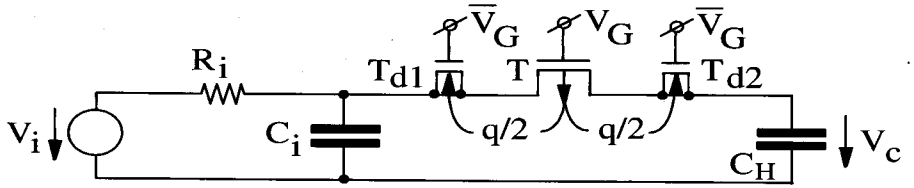


Figure 7.17: Charge-injection compensation with half-sized dummy switches [108]

have an opposite clock signal with respect to the main switch. As a result, half the charge will flow through the dummy switches, thus compensating the charge injection into C_i and C_H. Basically under this condition the injection is not strongly dependent on the variable B. However, mismatches in the circuitry have less influence on the charge division at the moment a slow pulse (small B) is used. In section 7.3.8 an example of a full differential implementation of a sample-and-hold amplifier in MOS technology is shown.

7.2.17 Noise in sample-and-hold circuits

The noise in the system originates from the ON resistance of the switch and the source resistance of the input source. Both resistances are incorporated into the resistor R_s shown in Figure 7.1. The noise generated by this resistor is equal to:

$$\bar{e}^2 = 4kTR_s\delta f. \qquad (7.36)$$

The total amount of noise generated across the capacitor C_H at the output of the sample-and-hold circuit is found by integration of the following equation:

$$\bar{e}^2_{total} = 4kTR_s \int_0^\infty \frac{1}{1+(\omega R_s C_H)^2} df. \tag{7.37}$$

Working out this equation we obtain:

$$\bar{e}^2_{total} = \frac{kT}{C_H}. \tag{7.38}$$

From equation 7.38 it is found that the noise does not depend on the bandwidth but is determined by the value of the hold capacitor C_H. To obtain the given noise calculation results some practical assumptions have been made.

At first the acquisition time of a sample-and-hold amplifier must be small compared to the sampling time. This assumption results in the fact that switching the system from the hold mode into the track mode, only a short time is needed before the signal is settled into the "steady state mode." As a result of this settling, the input signal is applied to a low-pass filter consisting of R_sC_H. When the sampling operation is performed, this operation is performed on the filtered input signal. At the moment signals such as noise with a much larger bandwidth than half the sampling frequency are applied, then these signals are folded back into the base band. In case of noise, the amount of noise over half the sampling frequency is reduced, but due to the folding operation the total amount of noise increases with the same factor as the reduction over half the sample frequency band. As a result the total amount of noise is equal to the wide-band noise as is given by formula 7.38.

Using power definitions, the result of equation 7.38 can be correlated to the signal power using:

$$P_{signal} = \frac{1}{2} C_H V^2_{in} \tag{7.39}$$

$$P_{noise} = \frac{1}{2} C_H \left(\frac{kT}{C_H}\right) = \frac{1}{2} kT. \tag{7.40}$$

V_{in} is the amplitude of the input sine wave.

The signal-to-noise ratio becomes:

$$S/N_{power} = \frac{P_{signal}}{kT/2}. \tag{7.41}$$

Equation 7.41 shows that for a defined signal-to-noise ratio in the system a minimum signal power is required.

At the moment a "hold"amplifier is added to the system, then the noise of this hold-amplifier must be added to the noise given by equation 7.38. This hold-mode noise is time continuous and the noise bandwidth is equal to $\frac{\pi}{2}$ times the small signal bandwidth of this hold amplifier.

7.3 Generalized non-inverting configurations

In this section different circuit implementations are shown based on the basic circuit from Figure 7.1. Mostly these circuit implementations make the system independent of the output impedance of the input signal source and show a low-output impedance to drive a low-impedance load resistor.

7.3.1 Double-buffered sample-and-hold circuit

In Figure 7.18 a double-buffered system is shown. The system consists of

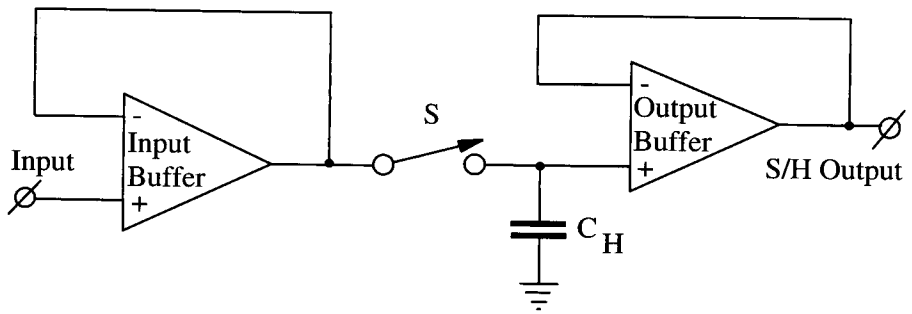


Figure 7.18: Double-buffered sample-and-hold circuit

two unity gain operational amplifiers that act as buffer, a switch S and the hold capacitor C_H. The input current of the output buffer amplifier must be very low to obtain a low droop rate during hold mode. The input buffer is used to supply a large charging or discharging current to the hold capacitor. The overall accuracy of the system is determined by the gain of the operational amplifiers and distortion of the system is determined by the linearity of these amplifiers. Offsets of both amplifiers will add, while charge feed-through of the switch determines the track-to-hold step. Stability of this system in determined by the individual amplifier stabilities and is not influenced by the system configuration.

7.3.2 Feedback improved sample-and-hold circuit

To overcome the accuracy problem of the system shown in Figure 7.18, the gain of the input amplifier-buffer is used to fix the overall accuracy. In Figure 7.19 the basic system configuration is shown. In this system the

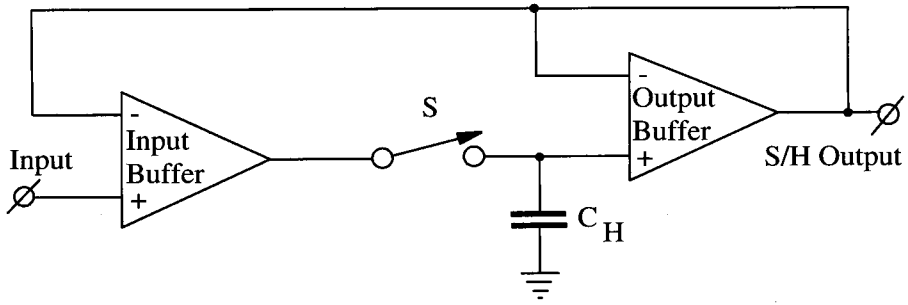


Figure 7.19: Feedback improved sample-and-hold circuit

output buffer amplifier is still in the follower mode, but the input amplifier is used in a feedback mode to obtain during track mode a high overall accuracy. The offset of the output buffer is canceled out by this feedback configuration. Switch offsets during track mode also cancel. The total offset during track mode is only determined by the input amplifier. Common mode rejection of the input amplifier stage must be high to avoid errors. In the hold mode operation of the system the charge feed-through of the switch results in a track-to-hold step. Aperture uncertainty is still determined by the rise or fall time of the sampling clock due to the changing signal levels at the switch. Furthermore, additional circuitry is needed to switch off the input amplifier from the input signal source. This is not drawn in Figure 7.19, but will be discussed in practical implementations. System stability is obtained when the unity gain bandwidth of the input feedback amplifier is much smaller than the unity gain of the output buffer amplifier. Furthermore, care must be taken to obtain a large enough phase margin for the total system. A small gain or phase margin results in overshoot during the signal acquisition of the system.

7.3.3 Integrating sample-and-hold circuit

The preferable switch configuration can be obtained by using the gains of both amplifiers in feedback configurations. In Figure 7.20 the circuit configuration is shown [107]. In this system the output buffer is replaced by

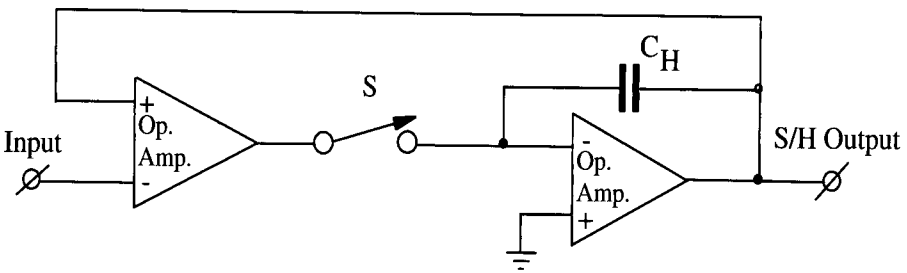


Figure 7.20: Integrating sample-and-hold circuit

an integrator function. The hold capacitor is connected between the output and the negative input terminal of the output amplifier. The switch drive is around the level of the non-inverting integrator amplifier terminal. Therefore, the switching moment and charge feed-through can be controlled very well. The optimum in switching accuracy can be obtained. The input amplifier is again connected in a feedback loop to increase the overall accuracy of the system. Note, however, that the input buffer is connected as a non-inverting amplifier. This connection is needed because the integrator already introduces an inversion in the loop. Stability of this system is more complex. A more detailed analysis will be given during the discussion of a practical circuit implementation. The only important factor concerning the overall accuracy of the system is the common mode rejection, especially at high input frequencies, of the input amplifier. Again special circuitry is needed to stabilize the input amplifier during the hold mode.

7.3.4 Practical integrating S/H circuit

A simplified practical example of an integrating sample-and-hold amplifier is shown in Fig. 7.21. The circuit consists of an input differential amplifier pair M_1, M_2 loaded with a current mirror M_3, M_4. The output of the current mirror is integrated into the hold capacitor connected between the drain and the gate of the Miller stage M_6. Biasing is performed by current source transistors M_7 and M_8 with the gates connected to an appropriate bias source V_{bias}. Switch M_5 performs the sampling in this track-and-hold amplifier. During track mode the switch M_5 is closed and the output current of the input amplifier/current mirror is integrated into the hold capacitor C_H. Because a full feedback is applied in this system, the output signal is made equal to the input signal applied at the gate of M_1. During track mode follows the output voltage follows the applied input signal. At the moment

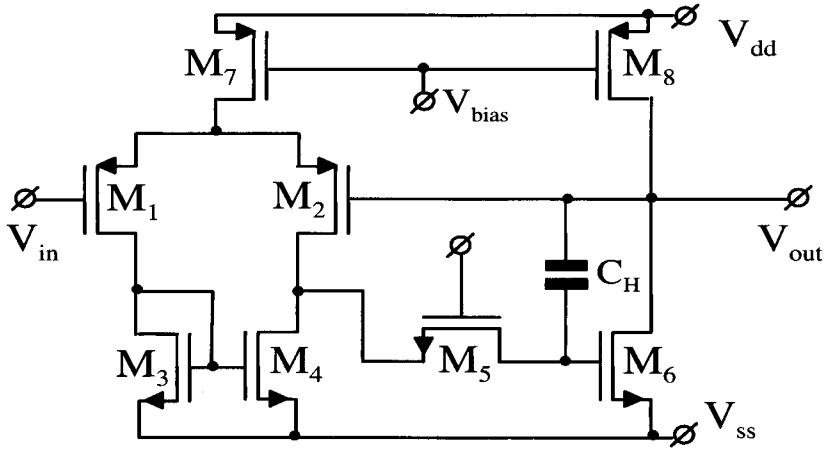


Figure 7.21: Integrated sample-and-hold circuit implementation

the system is switched from track into hold mode, then switch M_5 is opened and the information stored into capacitor C_H generates the output signal. In this system the switch M_5 is nearly always operated around the same gate-source voltage of M_6. Therefore the aperture uncertainty can be made small and no extra clock boosting circuits are required.

7.3.5 Switched capacitor sample-and-hold circuit

A special switched capacitor sample-and-hold circuit configuration is shown in Figure 7.22. A minimal system consists of three switches, S_1, S_2 and S_3,

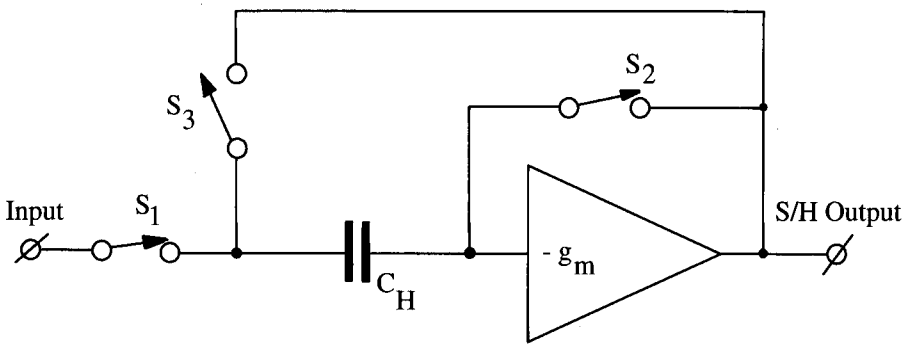


Figure 7.22: Switched capacitor sample-and-hold circuit

a hold capacitor C_H, and a transconductance amplifier g_m. During the track

mode the transconductance amplifier is in a full feedback mode, resulting in a low input impedance $(1/g_m)$. The capacitor is charged to the input voltage using switch S_1 and switch S_2. Bandwidth of this system during track mode is determined by:

$$f_{-3dB} = \frac{1}{2\pi(1/g_m + R_s)C_H}. \tag{7.42}$$

In this equation R_s includes the "on" resistance of switch S_1 and the signal source impedance.

When switches S_1 and S_2 are opened and switch S_3 is closed, the circuit switches into the hold mode. The stored signal value on the capacitor C_H is connected between the output and the input of the transconductance amplifier. As a result, nearly the same sampled input signal appears at the output terminal. Amplifier offset is automatically canceled. Only a small input signal variation occurs due to the generation of the output signal by the transconductance amplifier. When the gain of this amplifier is large, only a small variation is found. Charge feed-through and aperture uncertainty are determined by the switches. Switch S_2 must be opened before switch S_1 to avoid switching delays introducing distortion. Because switch S_2 always switches around the same signal level due to the full feedback configuration, this switch must be opened first to minimize aperture uncertainty. A very simple and compact unit can be designed in this way.

7.3.6 Switched capacitor sample-and-hold circuit with gain

In case the sample-and-hold amplifier requires gain, then the circuit configuration shown in Fig. 7.23 can be used. This circuit is known from high-speed pipelined analog-to-digital converters. The circuit consists of two capacitors C_s and C_f, three switches S_1, S_2 and S_3 and an amplifier. During sampling mode the switches are in the drawn position and the input signal is sampled on capacitor C_s and C_f. Then switch S_1 is opened to determine the sampling moment of the circuit and switches S_2 and S_3 change from position. The capacitor C_f with the input signal sampled is connected between the input and output of the amplifier, while capacitor C_s is grounded. This operation with the operational amplifier forces the charge of capacitor C_s to be transferred to capacitor C_f because the input voltage of the amplifier due to the feedback configuration is reduced to nearly zero. As a result of this charge redistribution the output signal is amplified. The gain of the

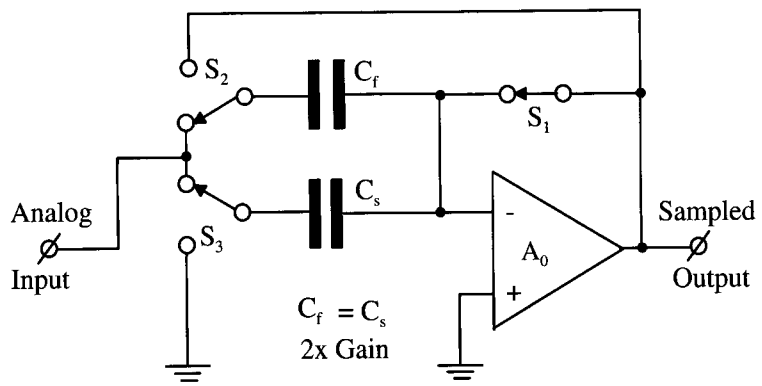


Figure 7.23: Switched capacitor S/H with gain

circuit becomes:

$$\frac{V_{out}}{V_{in}} = 1 + \frac{C_s}{C_f} = 2 \text{ with } C_s = C_f > \tag{7.43}$$

The gain accuracy is determined by the ratio of the capacitors.

7.3.7 CMOS non-inverting mode S/H example

As a high-speed, simple-to-implement switch, a diode bridge can be used. The basic circuit implementation of the sample bridge is shown in Figure 7.24 [84]. The system consists of four as a bridge connected diodes, a set of current sources that are switched to the bridge to make it active, a hold capacitor C_H, and an output buffer amplifier. When the currents I_1 and I_2 are switched to the bridge, then the diodes in the bridge are forward biased. With equal diodes and only a small signal current flowing through the bridge diodes, then the voltage level at the input of the circuit is equal to the voltage across the capacitor. A proper biasing of the diode bridge compared to the charging or discharging current of the hold capacitor results in a small distortion of the sample-and-hold amplifier. At the moment the current through the bridge is switched off, the impedance of the diodes becomes very high and the input signal is sampled. The currents I_1 and I_2 are reversed, resulting in a forward biasing of the diodes D_5 and D_6. These diodes are "bootstrapped" with the hold mode output voltage to maintain a constant "off" voltage of the diode bridge equal to about $2V_{diode}$. Capacitive feed-through due to the reverse biased bridge diodes between the input and the hold capacitor is reduced as well. During this "off" mode of

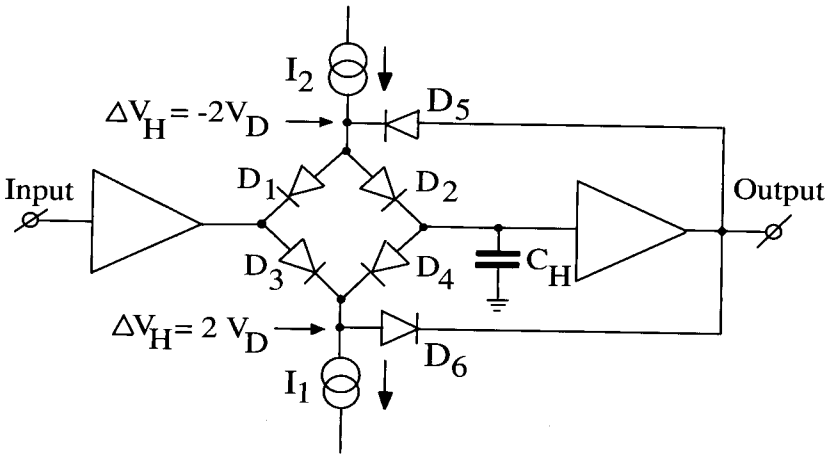


Figure 7.24: Sampling bridge circuit implementation

the bridge circuit a "large" ($2V_{diode}$) input signal can be applied without disturbing the voltage across the capacitor. Analyzing the circuit shows that under all conditions always a diode is reverse biased. When diodes with low reverse bias currents are used, a low droop rate due to the switch is obtained. In ultra high-speed applications mostly Schottky diodes are used in the sampling bridge, while in a discrete circuit solution the biasing of the bridge is performed with a pulse transformer. A well-known example of this diode bridge is used in sampling oscilloscopes. A practical CMOS circuit implementation of a diode bridge switch is shown in Figure 7.25. In this system the sample bridge is controlled by a differential amplifier and the biasing sources PM_9 and PM_{10}. At the moment transistor M_2 is conducting, a current I_0 is flowing through the diode bridge. During this time the circuit is in the track mode. At the moment transistor M_1 is conducting, then the diode bridge is reverse biased. Diodes D_5 and D_6 are used to prevent transistor M_1 from bottoming. The voltage level is kept at one diode voltage above the hold signal and one diode voltage below the hold signal. At the output of the system a PMOS differential buffer is used having a very low input bias current. Droop rate, is therefore, low. A source follower in the buffer stage allows a large output current to be supplied to the external load.

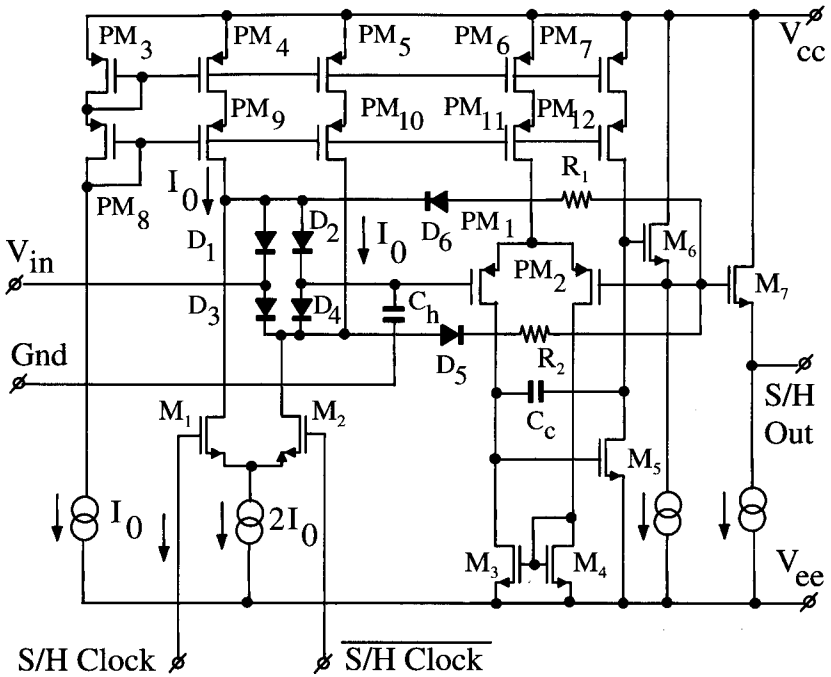


Figure 7.25: CMOS S/H circuit implementation

7.3.8 MOS differential sample-and-hold

In Figure 7.26 a basic example of a MOS differential sample-and-hold circuit is shown [105, 104]. In principle the first approach consists of two circuits of Figure 7.22 in parallel. Charge feed-through introduced by the sampling switches cancels when a differential output signal is sensed by the analog-to-digital converter. A disadvantage of this system is the variation of the input signal from track-to-hold caused by the variation in output voltage during the track and the hold mode. This problem can be overcome by modifying the system into the circuit shown in Figure 7.27. During the sampling mode the clock Φ_1 is high closing the accompanying switches. The input signal is sampled on the input capacitors C_1 and C_2. During this phase the output of the differential amplifier is shorted to prevent over-drive of the amplifier. An analog sample is taken at the moment the clock phase Φ_2 is made high. When switches S_1 and S_2 are opened, charge feed-through is stored on the capacitors C_1 and C_2. Furthermore, the opening of switches S_4, S_5 and S_6, S_7 results in feed-through effects that are common mode for hold capacitors C_3 and C_4. Only differences are stored that result from

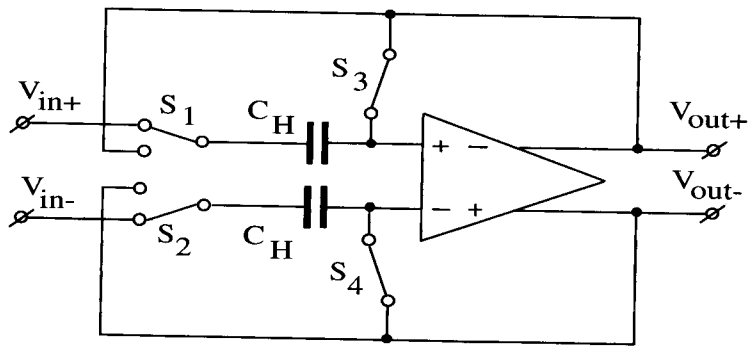


Figure 7.26: MOS differential sample-and-hold circuit [105, 104]

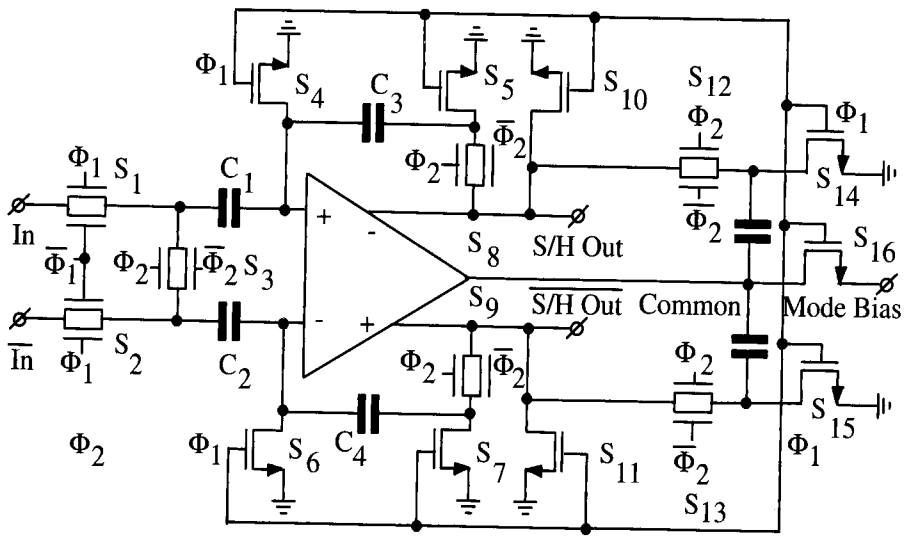


Figure 7.27: Improved differential sample-and-hold circuit [105, 104]

circuit un-symmetries. At the moment switch S_3 is closed, the opposite feed-through charge on capacitors C_1 and C_2 cancels out. As a result, an accurate sample charge is transferred onto capacitors C_3 and C_4. At the same time the high clock Φ_2 closes switches S_8, S_9, S_{12}, and S_{13}. During the high level of Φ_2 the sampled signal is available at the output of the system. A high-performance low-feed-through sample-and-hold amplifier is obtained.

7.3.9 Sample-and-hold amplifier with full hold time

An example of a sample-and-hold with a full clock time hold information is shown in Fig. 7.28 [116]. This sample-and-hold uses a number of capacitors

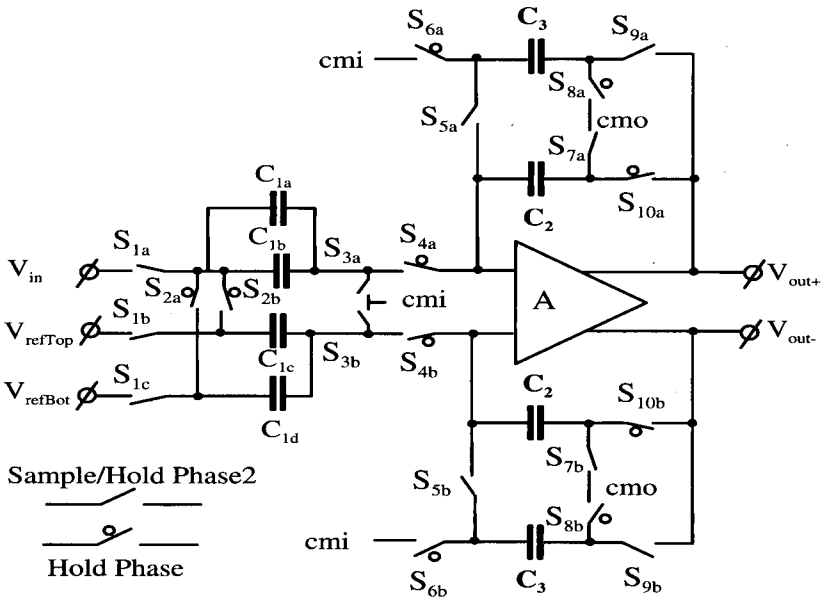


Figure 7.28: Sample-and-hold with full hold time [116]

to sample and transfer the input data. A single ended input is used and after sampling this single ended information is converted into a differential output signal. The single ended signal is sampled by the input switches on capacitors C_{1a} and C_{1b}. At the same time the midpoint of the reference voltage V_{reftop} and V_{refbot} is sampled on capacitors C_{1c} and C_{1d}. All these capacitors are equal. To avoid aperture uncertainty problems bottom plate sampling is used by opening first the switches S_{3a} and S_{3b} that ground the input capacitors and then opening switches S_{1a}, S_{1b} and S_{1c}. Suppose

furthermore that capacitors C_2 are fully discharged, then by closing switches S_{2a}, S_{2b} and switches S_{4a}, S_{4b} and switches S_{10a}, S_{10b} the charge sampled on C_{1a} and C_{1b} is transferred into capacitors C_2. The charge on C_{1c} and C_{1d} cancels and gives the mid point information to which the input signal is referenced. At the output a differential output voltage appears with a gain depending on the capacitor ratios between C_{1abcd} and C_2. Then switches S_{4a}, S_{4b} and S_{10a}, S_{10b} are opened and switches S_{7a}, S_{7b} and S_{5a}, S_{5b} and S_{9a}, S_{9b} are closed. The charge from capacitors C_2 is then transferred into capacitors C_3. These capacitors have been discharged before this operation to the difference between the input common mode voltage *cmi* and the output common mode voltage *cmo*. The output voltage remains basically the same during these two parts of the clock cycle. As a result of this operation during the full clock time the sampled output signal is available to the following analog-to-digital converter to perform the conversion.

7.4 Inverting sample-and-hold circuit

The gain of a sample-and-hold circuit can be well determined with an overall feedback applied. In Fig. 7.29 an example of such a circuit is shown. The

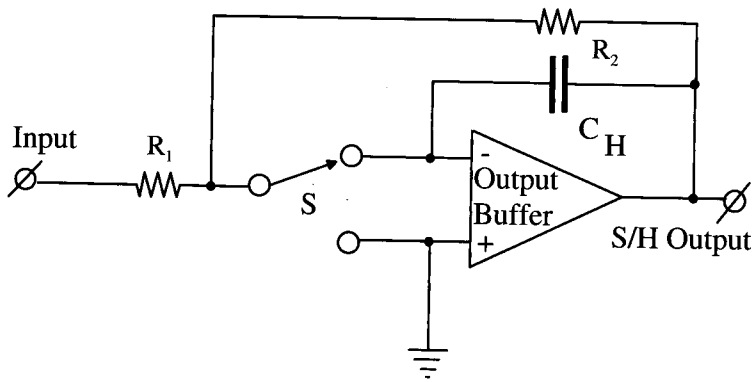


Figure 7.29: Inverting sample-and-hold circuit

circuit consists of an amplifier with feedback resistors R_1 and R_2 determining the gain and the hold capacitor C_H. The sampling switch connects during sampling the input of the amplifier with the feedback resistor node. During the hold mode the resister node is connected to ground to prevent signals to modulate over the finite output impedance of the amplifier the output signal. During the track mode the resistor R_2 is connected in parallel to the

hold capacitor C_H. This determines the maximum signal bandwidth:

$$f_{-3dB} = \frac{1}{2\pi R_2 C_H}. \tag{7.44}$$

The input impedance of the circuit is equal to:

$$z_{in} = R_1. \tag{7.45}$$

This rather low impedance can be a problem in some applications and then a different choice in sample-and-hold system must be done. The advantage of this system is that the switch S is always operated at the same signal levels. Therefore no variation in the switching moments is introduced and a high performance is obtained.

7.5 Operational range of simple sample-and-hold amplifiers

The operational range of sample-and-hold amplifiers is depicted in Fig. 7.30. At the moment no sample clock bootstrapping is used, then the modulation

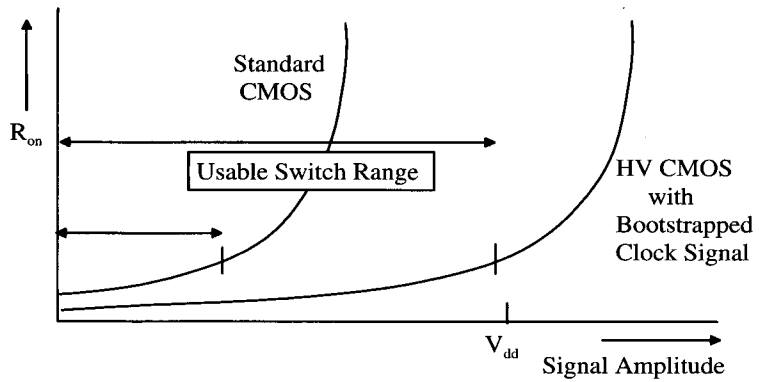


Figure 7.30: Operational range of simple S/H amplifiers

of the on resistance of the sampling switch with the rise and/or the fall time of this sampling clock determines the operational application range. With n-MOS devices this range is in between 0 and about $\frac{1}{4}$ of the supply voltage. At the moment a clock bootstrapping is used, then this range increases to roughly the supply voltage range. When high-resolution converters are used, then the application range is reduced because of the distortion introduced due to the finite differential channel matching.

7.6 Conclusion

Different system implementations that can be applied for high-performance or high-speed sample-and-hold amplifiers have been analyzed. In MOS applications a differential solution seems to be the best concerning switch feedthrough, distortion and ground bounce. The highest sampling rates are still obtained using a diode bridge as a sampling switch. Sampling oscilloscopes are examples of such an application.
The application of resistive loads in input stages in comparison with active loads using current mirrors reduces the noise in the amplifier system resulting in an increase in dynamic range of the overall system. Sampling clock bootstrapping increases the application range of simple sample-and-hold amplifiers. With signal dependent clock bootstrapping the dynamic range can be increased to practically the full supply voltage range without sacrificing distortion.

Chapter 8

Noise-shaping D/A conversion

8.1 Introduction

In this chapter noise-shaping techniques to improve the dynamic range of a system will be described. Noise-shaping can be very useful when speed can be exchanged with accuracy. The quantization errors in a noise-shaping system are removed from the signal band of interest. Mostly the suppressed quantization errors appear enlarged as out-of-band noise in the system. With a simple filter these errors are removed. An increased dynamic range of the coder is obtained. In digital systems word length can intelligently be reduced using a noise-shaping operation without losing dynamic range significantly. An ultimate in bit reduction is obtained when the noise-shaping operation reduces the number of bits to 1. Examples of such an operation is sigma-delta analog-to-digital conversion or noise-shaping digital-to-analog conversion based on single-bit word-lengths. The advantage of a 1-bit converter is the extreme linearity of such a device. A very good differential linearity is obtained with these converters. The most important design criteria for these converters will be given. At the moment the dynamic range of a system must be enlarged, but the maximum clock rate of the system cannot be increased because of technology limitations, then a multi-bit digital-to-analog converter can be used in the feedback loop. At that moment, however, the linearity of the digital-to-analog converter determines the linearity and the distortion in the system. To overcome this problem *Dynamic Element Matching* or *Continuous Current Calibration* techniques can be used to obtain the extreme linearity of the D/A converter without

needing extra trimming steps. In the stability analysis of the noise-shaping coders the root-locus method can be successfully applied. A model for the quantizer will be introduced using a gain AND a phase uncertainty. This model shows good prediction of idle patterns and predicts the limits of stability of a higher order coder very well comparable to practical simulations. Examples for first-, second-, and third-order coders will be treated. A coder is said to be stable when idling occurs at the highest possible frequency. In this case a maximum of oversampling ratio is obtained resulting in a maximum dynamic range. Mostly an idle pattern having a frequency around half the sampling frequency gives the best result. However, instability of a coder results in limit cycles that can not be influenced by the input signal and remain disturbing the coder even when the input signal is removed. This is the main cause of instability in an oversampling converter. Idle patterns at other frequencies depending on the input signal randomly generated are also allowed. In this case the quantization errors are randomized and appear as noise. Examples of designed 16- to 24-bits digital-to-analog converters will be shown [100, 93, 94]. Furthermore a combination of the analog output filter with the digital-to-analog converter will be described. This results in a completely integrated oversampling digital-to-analog converter system needing no external analog filtering or no accuracy with respect to analog on chip filtering. Furthermore non-filtered multi-bit converters using a randomized Dynamic Element Matching algorithm will be shown.

8.2 Digital oversampling filtering

In this section an example of oversampling and noise-shaping to increase the dynamic range of a digital-to-analog converter including a combined digital and analog output filtering will be described. With oversampling the dynamic range is increased as has been shown in one of the beginning chapters. However, the linearity of the converter must be in accordance with the extended resolution obtained by oversampling. Noise-shaping is a technique for increasing the resolution of a converter by using quantization error feedback. The basic idea behind noise shaping is to exchange resolution in time for resolution in amplitude. Many times more speed is avaliable than is required by the signal bandwidth. At that moment oversampling is used, while a combination with error feedback in a noise-shaper increases the resolution of the overall converter. The concept of oversampling and noise-shaping will be explained using a practical example of an audio digital-to-analog converter.

8.2.1 Combined digital-analog D/A output filter

In Figure 8.1 a block diagram of a combined digital-analog output filter for audio applications including the filter response is shown [13]. The sys-

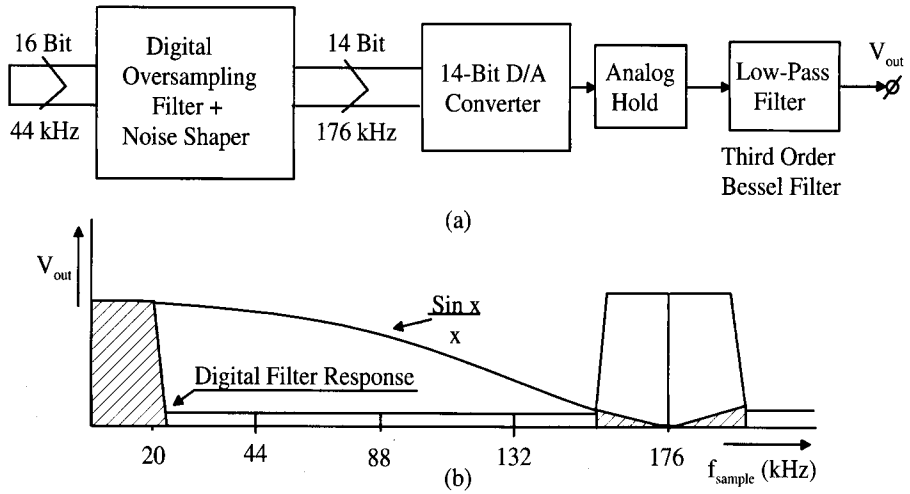


Figure 8.1: Combined digital-analog low-pass output filter

tem consists of a Finite Impulse Response (FIR) digital filter followed by a noise shaper to reduce the number of bits. The reduction in number of bits with the noise shaper even increases the effective resolution of the following digital-to-analog converter over the passband. Nearly no rounding errors are introduced. A third-order Bessel filter with a nearly linear phase removes the signal bands around the high sampling frequency and multiples of the sampling frequency. A sufficiently clean base-band signal is found at the output of the system. The digital filter performs the steep signal filtering at the pass band edge, while the analog filter reduces the repeated spectrum of the input signal at a frequency that is equal to four times the sampling frequency. In this system the input word-length is 16 bits. The filter coefficients have a word-length of 12 bits. As a result, at the output of the filter a minimum word-length of 28 bits is obtained. By using a noise-shaping operation, the output word-length is reduced to 14 bits without a significant loss in signal-to-noise ratio. In the next sections the noise-shaping operation will be explained. Noise-shaping is an intelligent reduction of the word-length in a digital signal processing system without significantly reducing the dynamic range. The word-length is reduced so much until a small decrease in dynamic range is found.

8.2.2 Digital filter configuration

In Figure 8.2 a simplified block diagram of an oversampling digital low-pass filter is shown. The filter uses a 96-tap FIR structure to perform the

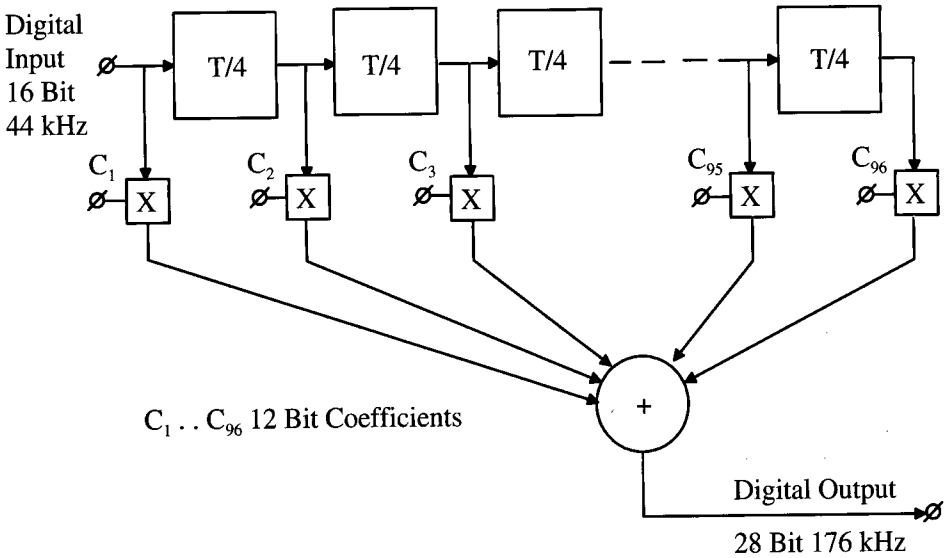


Figure 8.2: Block diagram of an oversampling filter

low-pass filtering operation. The input word-length is 16 bits, while the coefficients have a 12-bit word-length. To obtain the oversampling operation, four sets of 24 coefficients having a word-length of 12 bits are used to calculate the output data at a four times higher sampling frequency. These data appear at the filter output with a 28-bit word-length at the higher sampling rate. At least 12 of the least significant bits do not contribute to the overall performance of the system. With a noise-shaping technique the number of significant output bits can be further reduced. The total dynamic range of the system in this case is only slightly reduced when a D/A converter with only 14 bits is connected to the output. However, to obtain the increased dynamic range of the system at the full output signal range, a 16-bit linearity of the 14-bit converter is needed. When the 14-bit converter gives a good 14-bit linearity performance, then the quantization noise is reduced and the distortion of the converter determines the dynamic range of the system. When offset-binary coding is used, then glitches are important and may introduce extra distortion. The operation of the oversampling will graphically be explained.

8.2.3 Quantization errors

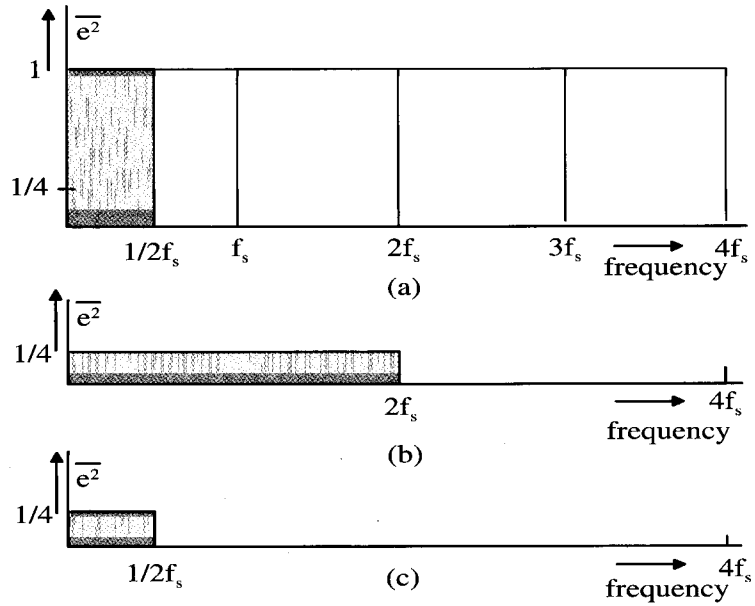


Figure 8.3: (a), (b) and (c) Quantization errors as a function of oversampling ratio

In Figure 8.3 the quantization error as a function of frequency is shown. The shaded area equals the quantization error over half the sampling frequency. Part (a) of the figure shows the quantization error of the input signal, while part (b) shows the effect of the four times oversampling operation. From Chapter 1 it is known that the noise density with a four times oversampling ratio is reduced with a factor four. Limiting the bandwidth of the system to $\frac{1}{2}f_s$ shows a four times reduction in the total quantization error (part (c) of the figure). As a result, an increase in dynamic range with 1 bit is obtained. A second operation is needed to improve further the dynamic range of the system in the signal band of interest.

8.3 Noise-shaping

In this section noise-shaping techniques are described that can be applied to increase the dynamic range of digital-to-analog converters without increasing the number of bits. In case a large oversampling is used, the number of bits in the digital-to-analog converter can be decreased to 1 bit. These 1-bit coders

will show a large dynamic range and have a very low distortion without needing accurate elements.
A circuit diagram of a noise-shaper is shown in Figure 8.4. At the input of the system a 28-bit input signal is applied. The word-length is reduced into a minimum number of significant bits using an intelligent reduction algorithm. As can be seen from Figure 8.4, the most significant 14 bits are applied to

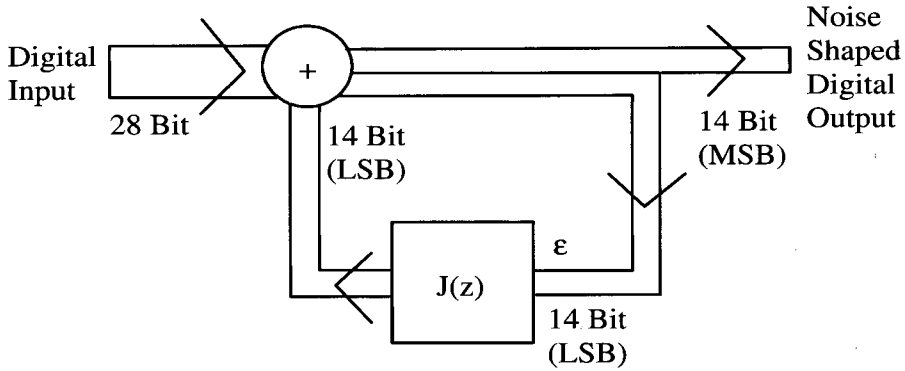


Figure 8.4: General noise-shaper

the output that drives the D/A converter. The lower 14 bits, denoted with ε, are filtered by the error filter $J(z)$ and added to the input word. The simplest implementation of $J(z)$ is one clock delay so: $J(z) = z^{-1}$. In this way a first-order filtering operation will be performed. The error that is obtained by this operation can be calculated. A general expression for a noise-shaping function using Figure 8.4 yields:

$$B_{in}(z) + \varepsilon(z)J(z) = B_{out}(z) + \varepsilon(z). \tag{8.1}$$

After rearranging equation 8.1 the output signal can be expressed as:

$$B_{out}(z) = B_{in}(z) - \varepsilon(z)(1 - J(z)). \tag{8.2}$$

Normalizing equation 8.2 we obtain:

$$\frac{B_{out}(z)}{B_{in}(z)} = 1 - \frac{\varepsilon(z)}{B_{in}(z)}(1 - J(z)). \tag{8.3}$$

From equation 8.3 it is found that the signal transfer function (STF) is equal to 1, while the second part of the equation

$$\varepsilon(z)(1 - J(z)) \tag{8.4}$$

determines the error at the moment the output word length is reduced.

The term $(1 - J(z))$ is usually called the *noise transfer function* (NTF) and determines the coloring of the output noise. Because the signal gain equals 1, this error can be related to the input signal as well. In case the word length of a system is reduced to N bits, then a value

$$\frac{\varepsilon}{B_{in}} = \frac{1}{2^N - 1} \approx 2^{-N} \tag{8.5}$$

is obtained. The value of ε is thus equal to the LSB value of the N-bits output word. The noise-shaping operation reduces this error even more, as will be shown later. From equation 8.2 it is seen that the spectral density of the error signal at the output of the system is determined by the filter operation $(1 - J(z))$.

To obtain zero error at z = 1 (f_{in} = 0 Hz) the term $(1 - J(1))$ must be zero. This requires a suitable choice for $J(z)$.

8.3.1 Single bit digital-to-analog converter

When a very large oversampling ratio is used in a noise shaper, then the number of output bits can be reduced to one. The single bit digital-to-analog converter output code is shown in Fig. 8.5. The one bit converter

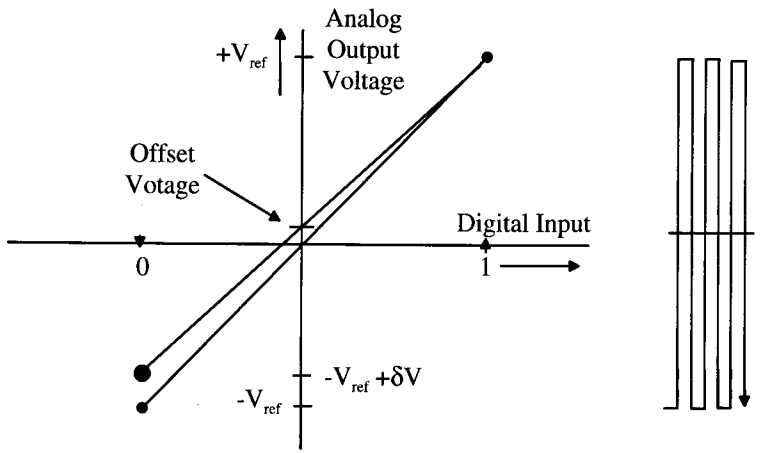


Figure 8.5: 1-bit digital-to-analog converter

uses two reference voltages V_{ref+} and V_{ref-}. In case these reference voltages are not exactly equal, then with zero digital input code an offset voltage is found. In many applications of these converters offset can be avoided with ac coupling. This means that the introduced offset by mismatch between the two reference voltages is not important. The linearity of the converter is excellent, because between the two reference levels a straight line can be drawn. No further mismatches are found in this system. When zero is applied, then the system switches between V_{ref+} and V_{ref-} with an equal number of "one's" and "zero's". The result of this switching is a large high frequency output signal. This "idling" as it is called is usually occuring at half the sampling frequency of the 1-bit converter. This large amount of signal must be reduced with an analog output filter. The large idling signal can be seen as a disadvantage of a single bit converter.

8.3.2 Multi-bit digital-to-analog converter

In case more bits are used in the following digital-to-analog converter, then accuracy requirements appear. In Fig. 8.6 the output signal of a 4-level digital-to-analog converter is shown. From this figure it is seen that with

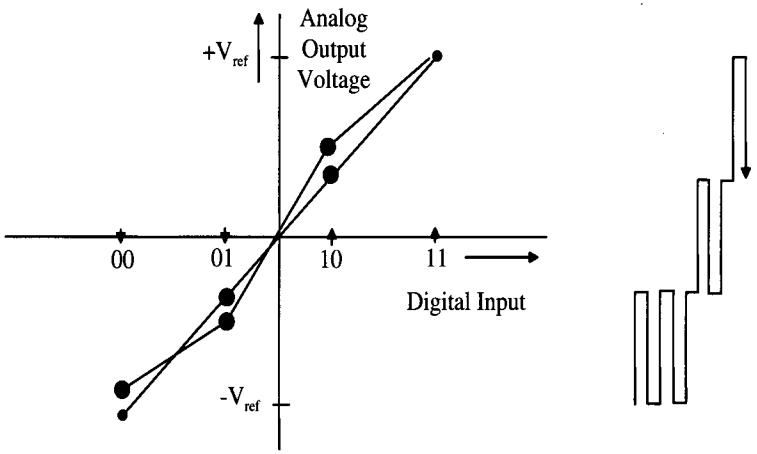


Figure 8.6: 4-level digital-to-analog converter

an ideal converter all output steps are exactly on the straight line between V_{ref-} and V_{ref+}. However, in a practical environment the matching of the levels is determined by the element accuracy used in the converter. A non-ideal converter curve is shown too. From this curve it is seen, that with full scale output signals a non-linearity occurs resulting in distortion of the

reproduced output signal. In 16 to 24-bit digital-to-analog converters an extreme linearity is required. Special techniques must be used in this case. The advantage of the multi-level converter is found in the fact that with zero input signal the idle channel signal is reduced with a factor three. This can be seen from the Fig. 8.6. When more output levels are used, then the idle channel signal will be reduced even more and is about equal to the LSB level of the converter. Furthermore to obtain a large resolution of the overall digital-to-analog converter, less oversampling ratio is required in case a multi-bit digital-to-analog converter is used.

8.3.3 First-order noise-shaper

The analysis of the audio digital-to-analog converter system will be continued. A first order noise shaper is used and the effect and quantization noise density will be shown. In Figure 8.7 a first order noise-shaper is given. A first-order noise-shaper uses a one clock delay ($J(z) = z^{-1}$). Then we

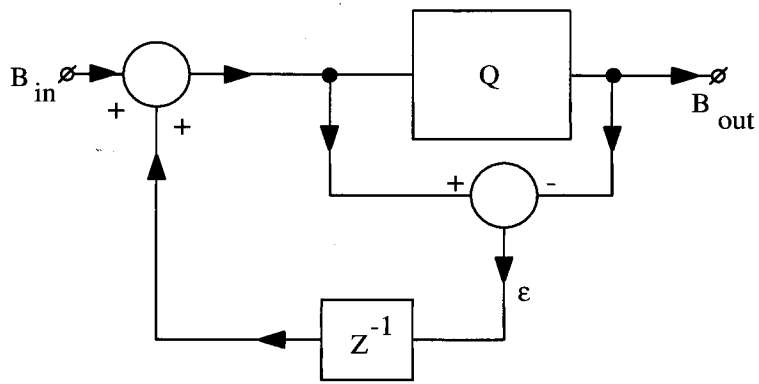


Figure 8.7: First-order noise-shaper

obtain:

$$B_{out}(z) = B_{in}(z) - \varepsilon(z)(1 - z^{-1}). \tag{8.6}$$

The first order filter operation reduces the error $\varepsilon(z)$. Especially at low frequencies ($z \approx 1$) a large reduction is obtained. The total amount of quantization error is found by integrating $\varepsilon(z)$ over the signal bandwidth f_b. Supposing that the quantization error density is frequency independent in the band (f = 0 to f = $\frac{f_s}{2}$), then the result becomes:

$$e_{tot}^2 = \int_0^{\theta_1} \varepsilon^2 |\, 1 - z^{-1} \,|^2 d\theta. \tag{8.7}$$

In this equation $|\,1-z^{-1}\,|$ is the amplitude characteristic of a first-order noise filter and $\theta_1 = \frac{2\pi f_b}{f_s}$.

Note that f_s is equal to the *output* sampling frequency!

Inserting $z = e^{j\theta}$ we obtain:

$$|\,1-z^{-1}\,|^2 = \frac{|\,e^{j\theta}-1\,|^2}{|\,e^{j\theta}\,|^2}. \tag{8.8}$$

Working out equation 8.8 the following result for the amplitude characteristic is obtained:

$$|\,1-z^{-1}\,|^2 = 2(1-\cos\theta). \tag{8.9}$$

In Figure 8.8 the square of the amplitude response as a function of frequency is shown. Note that at half the sampling frequency the gain is 2 ($z=-1$). Inserting equation 8.9 into equation 8.7 and integrating the function results

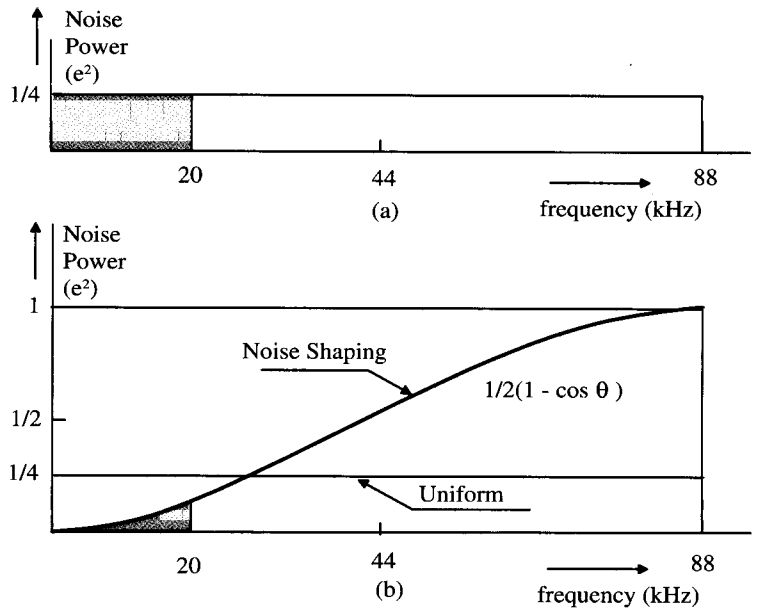


Figure 8.8: Square of the filter amplitude response

in:

$$e_{tot}^2 = 2(\theta_1 - \sin\theta_1)\varepsilon^2. \tag{8.10}$$

Without noise-shaping the total uniformly distributed noise over the band 0 to θ_1 is equal to:

$$e_{uniform}^2 = \varepsilon^2 \int_0^{\theta_1} d\theta = \varepsilon^2\theta_1. \tag{8.11}$$

In comparing the results of equations 8.10 and 8.11, the improvement with respect to noise and dynamic range of the system is obtained. Using F_1 as the dynamic range improvement factor we get:

$$F_1 = \frac{e_{tot}}{e_{uniform}} = \sqrt{2(1-\frac{\sin\theta_1}{\theta_1})}. \tag{8.12}$$

In this equation $\theta_1 = \frac{2\pi f_b}{f_s}$.

The oversampling factor obtained by the digital filtering operation introduces an extra decrease in noise with a factor G. This factor can be expressed in terms of sample rate f_s and signal bandwidth f_b or:

$$G_1 = \sqrt{\frac{\theta_1}{\pi}} = \sqrt{\frac{2f_b}{f_s}}. \tag{8.13}$$

The total improvement H_1 in the signal-to-noise ratio due to noise-shaping and oversampling becomes:

$$H_1 = \frac{1}{F_1 G_1} = \frac{1}{2\sqrt{\frac{f_b}{f_s}(1-\frac{sin2\pi f_b/f_s}{2\pi f_b/f_s})}}. \tag{8.14}$$

Inserting values for $f_s = 176$ kHz and $f_b = 20$ kHz, H_1 becomes 14.2 dB. The signal-to-noise ratio of a 14-bit D/A converter with oversampling filter and noise-shaping becomes 86.0 + 14.2 = 100.2 dB. At the input of the filter an infinite word length is assumed. This is not true for a practical system. At the input of the system a 16-bit input word is applied. The input noise and the rounding noise of the noise-shaper must be added to obtain the total noise in the system. In this calculation it is supposed that the rounding errors are not correlated and behave like noise sources. As a result of the noise-shaping operation the signal-to-noise of the system becomes:

$$S/N_{system} = \frac{S/N_{16bits}}{\sqrt{1+k^2}}. \tag{8.15}$$

k is the ratio between the signal-to-noise ratio of the 16-bits input word (98.1 dB) and the signal-to-noise ratio of the noise shaped oversampled 14-bit

digital-to-analog converter (100.2 dB). With $k = 0.776$, the signal-to-noise ratio of the system becomes:

$$S/N_{system} = 96.0\ dB. \tag{8.16}$$

The total operation of noise-shaping and a four times oversampling results in an increase of the dynamic range of the 14-bits D/A converter with nearly 2 bits. An excellent digital-to-analog conversion system including linear phase low-pass filtering with a dynamic range of nearly 16 bits, is obtained.

8.3.4 Second-order noise-shaper

At the moment the order of the noise-shaping filter is increased from a first-order into a second-order, then an improvement in dynamic range is expected. The filter function in the feedback loop can be determined using equation 8.2. We obtain:

$$1 - J(z) = (1 - z^{-1})^2. \tag{8.17}$$

In case of a second-order noise-shaper $J(z)$ becomes:

$$J(z) = z^{-1}(2 - z^{-1}). \tag{8.18}$$

In Figure 8.9 the implementation of equation 8.18 is shown. The improvement in dynamic range due to noise-shaping with a second-order noise-shaping function can be performed in the same manner as was done to get F_1 (8.12). After some calculations we obtain:

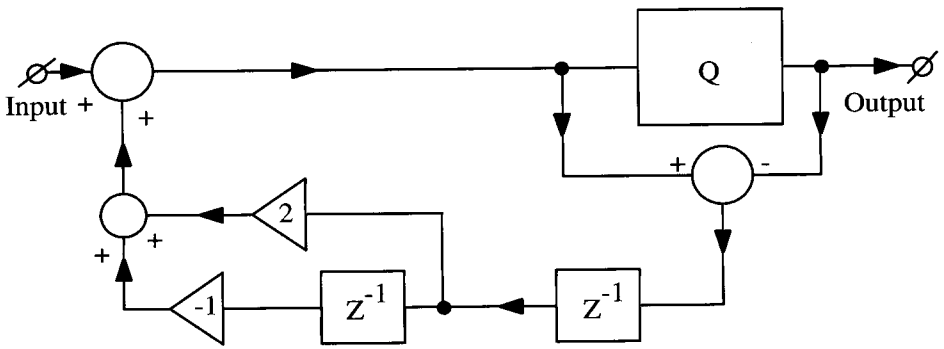


Figure 8.9: Second-order filter implementation

$$F_2 = \sqrt{6 + \frac{2\sin\theta_1\cos\theta_1 - 8\sin\theta_1}{\theta_1}\theta_1} \tag{8.19}$$

The improvement due to oversampling remains identical to 8.13 so:

$$G_2 = \sqrt{\frac{\theta_1}{\pi}} = \sqrt{\frac{2f_b}{f_s}}. \tag{8.20}$$

The total improvement in dynamic range H_2 of a second-order system becomes:

$$H_2 = \frac{\sqrt{\pi}}{\sqrt{6\theta_1 + 2\sin\theta_1\cos\theta_1 - 8\sin\theta_1}}. \tag{8.21}$$

By inserting values for $f_s = 176$ kHz and $f_b = 20$ kHz, H_2 becomes 19.5 dB. In Figure 8.10 the noise-shaping operation as a function of frequency for a first- and second-order filter function are shown. Note that over the signal band of interest (0 to f_b) the total noise is reduced with the second-order filtering operation. The improvement in dynamic range when the noise-shaping filter order is increased from a first-order into a second-order equals 5.3 dB, which is close to 1 bit.

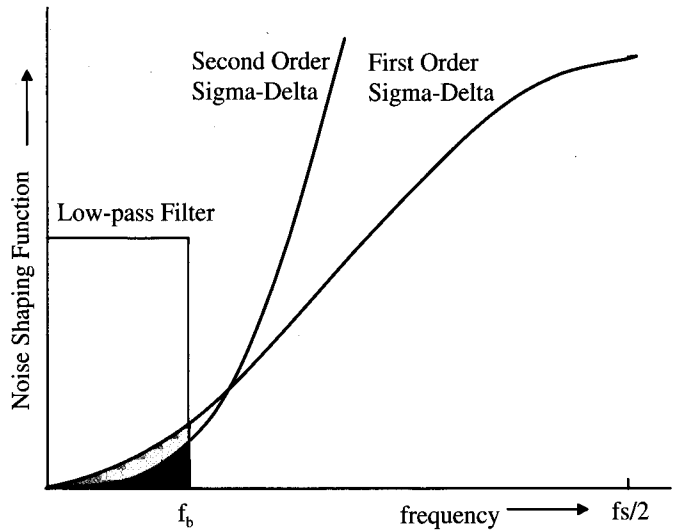


Figure 8.10: First- and second-order noise-shaping functions

8.3.5 Third-order noise-shaper

The filter order of the noise-shaper can again be increased from second order into third order. However, problems with stability of the system can arise. Therefore it is important to discuss two possibilities:
In Figure 8.11 an implementation of equation 8.29 is shown.

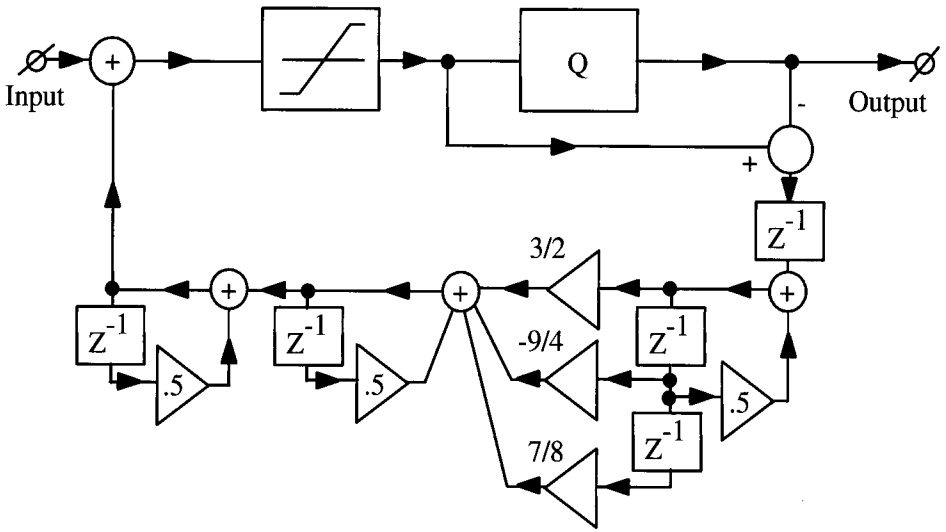


Figure 8.11: Third-order filter implementation

1. The output number of bits is larger than 1 (multi-bit converter).
2. The output number of bits is limited to 1 (Sigma-delta converter).

Case 1)

The number of output bits is larger than 1.
The noise transfer function in this case becomes:

$$1 - J(z) = (1 - z^{-1})^3, \tag{8.22}$$

giving for the filter function:

$$J(z) = z^{-1}(3 - 3z^{-1} + z^{-2}). \tag{8.23}$$

The improvement in dynamic range due to noise-shaping with a third-order noise-shaping function is calculated in the same manner as was done to get F_1 (8.12). After some calculations we obtain:

$$F_3 = \sqrt{20 + \frac{-30\sin\theta_1 + 6\sin 2\theta_1 - \frac{2}{3}\sin 3\theta_1}{\theta_1}} \tag{8.24}$$

The improvement due to oversampling remains identical to 8.13, so:

$$G_3 = \sqrt{\frac{\theta_1}{\pi}} = \sqrt{\frac{2f_b}{f_s}}. \tag{8.25}$$

The total improvement of a third-order multi-bit noise-shaper becomes:

$$H_3 = \frac{\sqrt{\pi}}{\sqrt{20\theta_1 - 30\sin\theta_1 + 6\sin 2\theta_1 - \frac{2}{3}\sin 3\theta_1}}. \tag{8.26}$$

By inserting values $f_b = 20$ kHz and $f_s = 176$ kHz we obtain $H_3 = 16.02$ or 24.1 dB.

Case 2)

The number of output bits is reduced to 1.

The loop gain in the system increases in such a way that the stability of the system must be analyzed. This stability analysis will be performed in section 9.5. To generalize the problem the approach used in reference [11] will be applied here. The noise-shaping function is changed into:

$$1 - J(z) = \left(\frac{1 - bz^{-1}}{1 - az^{-1}}\right)^n. \tag{8.27}$$

In case of a third-order noise-shaper 8.27 changes into:

$$1 - J(z) = \left(\frac{1 - z^{-1}}{1 - az^{-1}}\right)^3. \tag{8.28}$$

In reference [11] a stable operation of the system is obtained when $b = 1$ and $a = 0.5$. The transfer function for $J(z)$ becomes:

$$J(z) = z^{-1}\frac{1.5 - 2.25z^{-1} + 0.875z^{-2}}{(1 - 0.5z^{-1})^3}. \tag{8.29}$$

The improvement in noise performance due to a third-order noise shaper can be calculated again. However, because of the stability problem the implemented function is more difficult to integrate.

Using $b = 1$ but keeping the variable a in the equation, we obtain with:

$$\begin{aligned} T_{3a} &= \frac{1}{a^3} \\ U_{3a} &= \frac{2(1 + 5a + 10a^2 - 10a^3 - 5a^4 - a^5)\arctan\left[\left(\frac{a+1}{a-1}\right)\tan\frac{\theta_1}{2}\right]}{\theta_1 a^3(1+a)^5} \end{aligned}$$

$$V_{3a} = \frac{3(a-1)^2(1+4a+a^2)\sin\theta_1}{\theta_1 a^2(1+a)^4(1+a^2-2a\cos\theta_1)}$$
$$W_{3a} = \frac{(a-1)^4\sin\theta_1}{\theta_1 a^2(1+a)^2(1+a^2-2a\cos\theta_1)^2} \quad (8.30)$$

and $0 < a \leq 1$ for F_3:

$$F_{3a} = \sqrt{T_{3a}+U_{3a}+V_{3a}-W_{3a}}. \quad (8.31)$$

The notation (3a) is used to indicate that we are talking about a third-order noise-shaper having an extra stabilizing function $(1-az^{-1})$ in the filter section. The total improvement in noise-shaping H_{3a} can be calculated, resulting in:

$$H_{3a} = \frac{\sqrt{\pi}}{\sqrt{\theta 1(T_{3a}+U_{3a}+V_{3a}-W_{3a})}}. \quad (8.32)$$

Inserting values in 8.32 of $a = 0.5$, $f_b = 20$ kHz and $f_s = 176$ kHz, we obtain: $H_{3a} = 4.52$ or 13.1 dB. The expected improvement in signal-to-noise ratio is smaller then expected with a third-order noise-shaper. This is due to the term $(z-a)^3$ required to obtain a stable system.

8.3.6 Fourth-, fifth-, and sixth-order noise-shaper

Depending on the number of output bits used in the system, again a split-up has to be made into:

1. The number of output bits is larger then 1,
2. The number of output bits is 1.

Case 1)

The noise shaping function becomes:

$$1-J(z) = (1-z^{-1})^n \text{with n} = 4,\ 5,\ \text{and } 6. \quad (8.33)$$

The improvement in noise-shaping becomes:

$$F_n = \sqrt{\frac{\int_0^{\theta_1}[2(1-\cos\theta)]^n d\theta}{\theta_1}}. \quad (8.34)$$

Even with higher-order filter functions, the improvement due to oversampling remains equal to:

$$G_n = \sqrt{\frac{\theta_1}{\pi}}. \quad (8.35)$$

The total improvement due to noise-shaping and oversampling generalizes into:

$$H_n = \frac{1}{H_n G_n} = \frac{\sqrt{\pi}}{\sqrt{\int_0^{\theta_1}[2(1-\cos\theta)]^n d\theta}}. \quad (8.36)$$

The analytical results of the integrals for n = 4 to 6 are not given in this section because of the complexity of the formulas.

In Figure 8.12 the improvement in signal-to-noise ratio of a multi-bit system as a function of oversampling ratio and filter order n are shown. From Figure

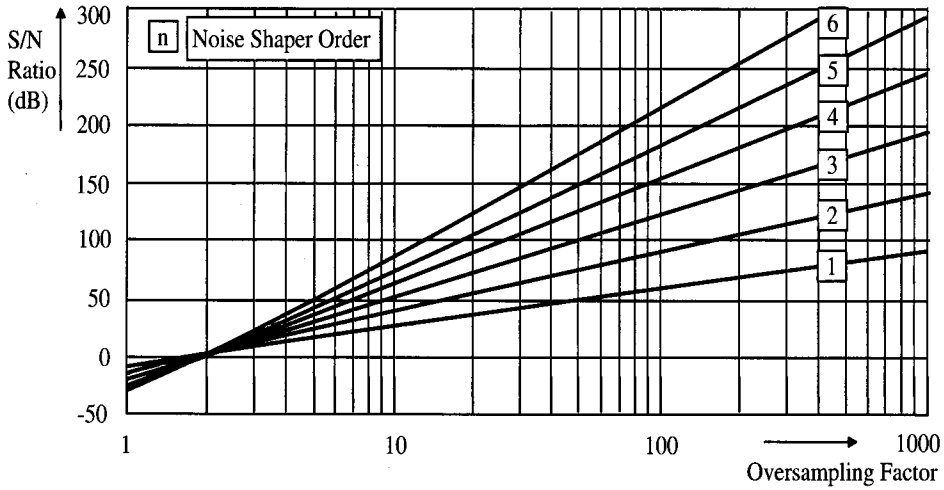


Figure 8.12: Signal-to-noise improvement as a function of oversampling ratio and filter order in a multi-bit system

8.12 it is seen that at the moment the oversampling ratio is larger then 4 nearly a linear relation between oversampling and increase in signal-to-noise ratio is obtained. In Figure 8.13 a detailed part of Figure 8.12 with an oversampling ratio between 1 and 10 is shown. From Figure 8.13 it is found that oversampling ratios smaller than 4 do not give an increase in signal-to-noise ratio of the system when the order of the noise shaper is increased.

Case 2)

The noise-shaping function $1-J(z)$ is again assumed to be:

$$1-J(z) = \left(\frac{1-z^{-1}}{1-az^{-1}}\right)^n. \quad (8.37)$$

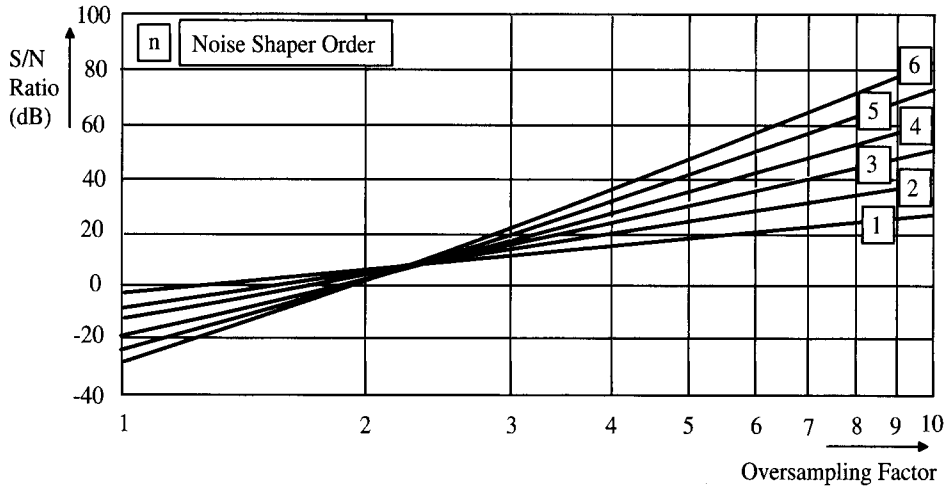


Figure 8.13: Signal-to-noise improvement of multi-bit system with a 1 to 10 oversampling ratio

However, in cases for n = 4 to 6, the integrals are more difficult to obtain. By using advanced computer programs [88] it is possible to get analytical expressions for the noise-shaping improvement function H_n. These analytical expressions are quite large and are therefore not presented in this section. However, from a designer's viewpoint it is important to get an insight in the improvement in dynamic range or signal-to-noise ratio at the moment the order of the noise-shaping function is increased and at the same time a large oversampling ratio is used. To simplify the understanding of the results, the improvement factor H_n is normalized with respect to the oversampling factor G_n, so:

$$H_{normalized} = H_n \sqrt{\frac{\theta_1}{\pi}}. \tag{8.38}$$

As a result of the normalization operation the improvement reduces to 1 at the moment the factor $a = 1$. Depending on the order of the noise-shaper not all values of a result in a stable operation of the system. However, when the number of output bits is increased the value of a tends to decrease while maintaining stability of the system. In Figure 8.14 the improvement in dynamic range due to noise-shaping as a function of the value of a, the order of the noise-shaper from a third-order to a sixth-order noise-shaping function are shown. A large oversampling factor of 400 is used in this figure. Note, furthermore, that this figure is only valid for a 1-bit noise-shaper!

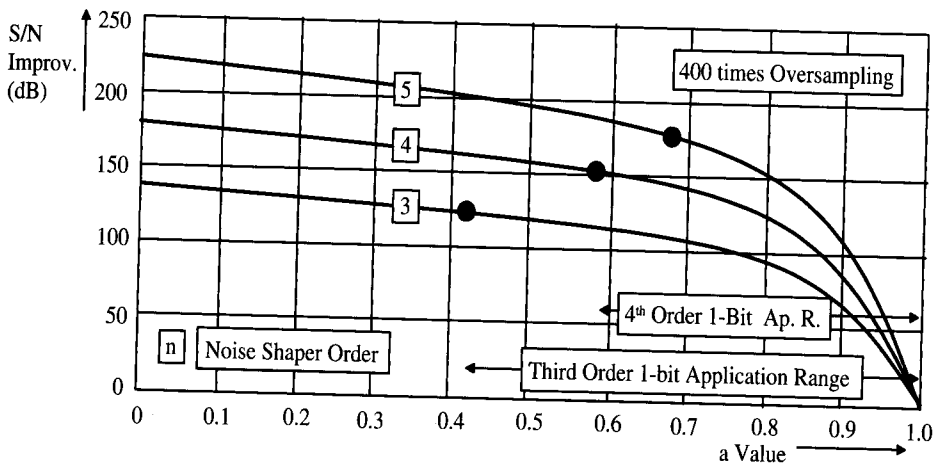


Figure 8.14: Normalized noise-shaping improvement function

In practical systems the stability of the noise-shaping system must be determined resulting in minimum values for the factor a. In the following table 8.1 an indication of practical values for a as a function of filter order are given.

See: Jurgen van Engelen et al, Bandpass Sigma Delta Modulators, Stability Analysis, Performance and Design Aspects, Kluwer Academic Publishers 1999.

These values are valid for a **1-bit output code!** In this book the values

n	a	a	a	a
	Rule of Thumb	DF method	Experimental	Lee's Rule
3	0.449	0.412	0.416	0.587
4	0.611	0.587	0.619	0.682
5	0.698	0.679	0.717	0.741
6	0.753	0.736	0.771	0.782

Table 8.1: Filter order and minimum stability value

obtained with the Describing Function method (DF) will be used. These values are very close to the values obtained from extensive simulations. The

other values obtained from different methods are just shown for completeness.
It must be noted that the presented values for a are indications for systems that are at the edge of stability. Larger values of a show an optimum between noise-shaping improvement, stability at large signals, and implementation complexity. In Figure 8.15 the improvement in signal-to-noise ratio due to oversampling and noise-shaping for a 1-bit system as a function of the filter order is shown. The presented results use values for the stabilization term according to Table 8.1. From Figure 8.16 it is found that for a filter order

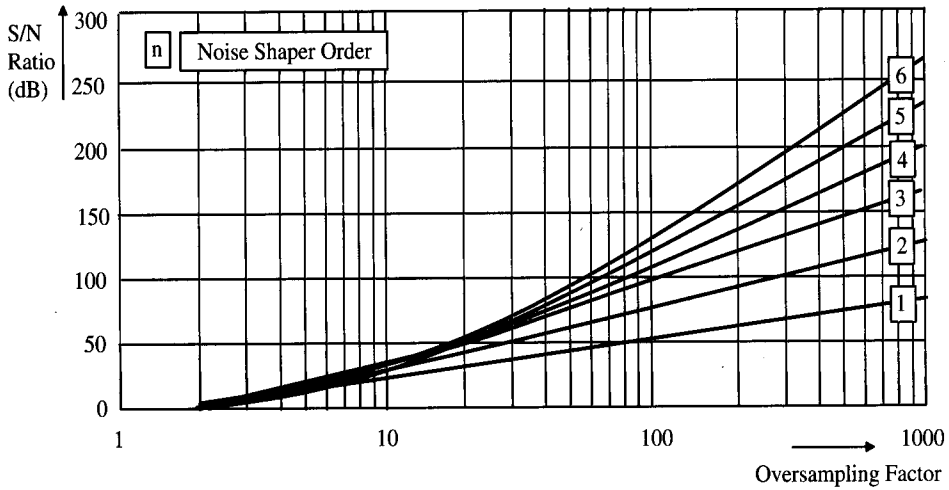


Figure 8.15: Signal-to-noise improvement of a 1-bit system as a function of oversampling ratio and filter order

above 2 the increase in signal-to-noise ratio is only obtained when the oversampling ratio is larger than about 25. Below an oversampling ratio of 25 a lower order filter gives a better improvement. To show this in more detail, Figure 8.16 gives the signal-to-noise improvement in case of an oversampling ratio between 10 and 100. Again from Figure 8.15, it is seen that for large oversampling ratios (more than 40) a linear increase in dynamic range with increasing oversampling ratio is obtained.

In the next section an approximation of the increment in signal-to-noise ratio as a function of filter order and oversampling ratio for a multi-bit system will be given.

At this point it must be noted that at the moment the number of output

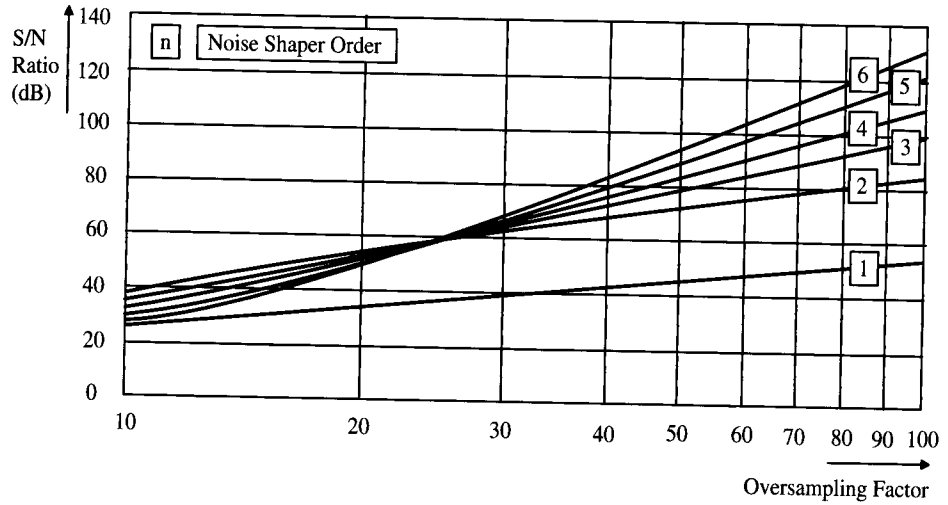


Figure 8.16: Detail of signal-to-noise improvement of a 1-bit system with oversampling ratios between 10 and 100

bits is between 2 and 6 for systems having third- to sixth-order noise-shaping functions, the value of a must be determined and the increase in dynamic range according to Figure 8.14 can be used to determine the improvement in signal-to-noise ratio of such a system. Mostly designers use simulations to come to the required results.

8.3.7 Largely oversampled noise-shaper

Assume that the filter function in the feedback loop is given by:

$$1 - J(z) = (1 - z^{-1})^n. \tag{8.39}$$

Using this filter in an nth order noise-shaper, then equation 8.12 changes into:

$$F_n = \sqrt{\frac{\int_0^{\theta_1} [2(1 - \cos\theta)]^n d\theta}{\theta_1}}. \tag{8.40}$$

When the sampling frequency f_s in a system is much larger than the signal bandwidth f_b, then $\cos\theta_1$ can be approximated by:

$$\cos\theta_1 \approx 1 - \frac{\theta_1^2}{2!}. \tag{8.41}$$

Inserting 8.41 into 8.40, this equation simplifies into:

$$F_n \approx \sqrt{\frac{\int_0^{\theta_1} \theta^{2n} d\theta}{\theta_1}}. \tag{8.42}$$

After integration we obtain:

$$F_n \approx \frac{\theta_1^n}{\sqrt{(2n+1)}}. \tag{8.43}$$

Because of the oversampling the additional factor G_n is equal to:

$$G_n = \sqrt{\frac{\theta_1}{\pi}}. \tag{8.44}$$

The total improvement of a largely oversampled nth order noise-shaper becomes:

$$H_n \approx \theta_1^{-(n+\frac{1}{2})} \sqrt{\pi(2n+1)}. \tag{8.45}$$

When the oversampling ratio being ($\frac{\pi}{\theta_1}$ *or* $\frac{f_s}{2f_b}$) is increased with a factor two, the signal-to-noise ratio increases according to equation 8.45 with a factor: $2^{n+\frac{1}{2}}$.

When a limited oversampling ratio is used, then the exact solution of the integrals 8.40 must be used.

8.4 Multi-bit largely oversampled noise-shaper

The signal-to-noise ratio at the output of a multi-bit system can easily be calculated. Suppose that m output bits are used, then the signal-to-noise ratio becomes:

$$S/N_{quantizer} = (2^m)\sqrt{1.5} H_n. \tag{8.46}$$

m is the number of output bits.
In equation 8.46 H_n represents the improvement in dynamic range due to the *nth* order noise-shaping filter. When the oversampling ratio is large then equation 8.46 can be expressed as:

$$S/N_{quantizer} = (2^m)\sqrt{\frac{1.5 f_s}{2 f_b}} \left(\frac{f_s}{2\pi f_b}\right)^n \sqrt{2n+1}. \tag{8.47}$$

It must be noted that the calculated results of equations 8.46 and 8.47 are *only* valid for multi-bit systems or systems that have $a = 0$ and are stable.

At the moment 1-bit systems are used, a correction for the stability term in the noise-shaping function is required that results in deviations from the given equation. The correction factor must be introduced at the moment third-order or higher-order 1-bits systems are analyzed. Use Figure 8.14 to obtain the correction factor depending on the stabilization variable a.

Equation 8.47 predicts that the signal-to-noise ratio increases with more than 6 dB per bit when the number of output bits is increased from a 1-bit signal into a multi-bit signal. The nonlinear relation of the signal-to-noise ratio on the number of bits with a small number of used bits causes this phenomenon.
Furthermore when these quantizers are included in a system with a finite number of input bits, then the dynamic range of the total system is calculated from:

$$S/N_{system} = \frac{S/N_{input}}{\sqrt{1 + (S/N_{input}/S/N_{quantizer})^2}}. \tag{8.48}$$

The signal-to-noise ratio of the input is determined by the number of input bits applied to the system, while the signal-to-noise ratio of the quantizer is determined by the construction of the quantizer. Equation 8.47 determines in this case the S/N of the quantizer.

8.5 Stability analysis of noise-shapers

A noise-shaping system shows an idling pattern with the error signal being noise like or consisting of limit cycles that can be disturbed by the input signal and occur at sub-multiples of the sampling frequency such as $\frac{f_s}{2}$, $\frac{f_s}{3}$ and so on. These limit cycles are part of the error signal and must be distinguished from unstable behavior. Instability of the noise-shaping feedback loop gives rise to limit cycles at relatively low frequencies ($\frac{f_s}{25}$). These limit cycles are usually not affected by the input signal, and if such a limit cycle is present, it persists even if the input signal is removed. Hence the stability of a noise-shaper cannot be related to the stability of conventional linear systems.

Therefore, the criterion that will be used in this book is:

A noise-shaper is unstable if a large signal limit cycle can be present that disturbs the noise-shaping mechanism and that re-

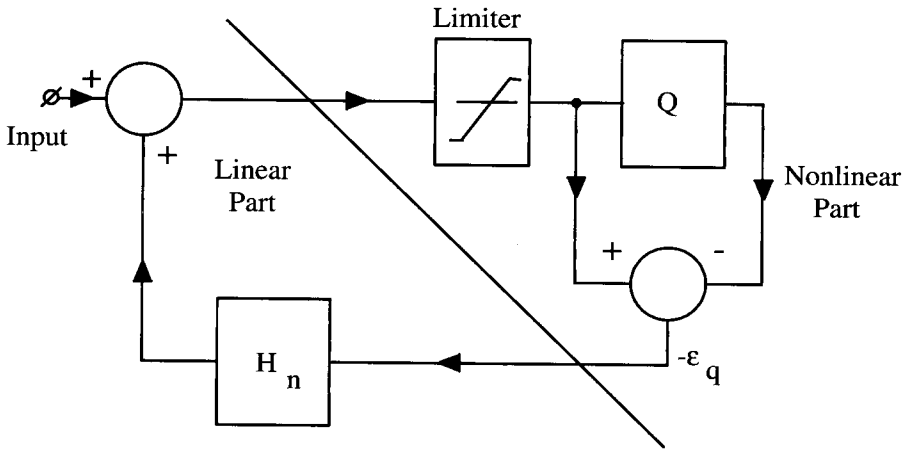


Figure 8.17: Partitioning of a noise-shaper for stability analysis

mains present even when the input signal is removed from the system.

8.5.1 Noise-shaper stability model

To perform the stability analysis of noise-shapers, a simple model will be used. In Figure 8.17 a partitioning of the noise-shaper into a linear part and a nonlinear part is shown. The linear part of the system comprises the loop filter and all additional loop delays. The nonlinear part consists of the quantizer Q and the subtracter from which the quantization error is obtained. The limiter represents a limitation of the signal caused by overload of the system by large input signals. As a result of the nonlinear operation of the quantizer this function will be replaced by a global transfer λ. The global transfer λ represents the transfer of the fundamental waveform that is assumed to be present in the loop. In Figure 8.18 the stability model to be used during the analysis is given. In case of a multi-level quantization, the quantizing steps are small when related to the input of the quantizer. As a result, the quantization error that is applied to the noise-shaping filter is small related to the input signal. Thus the global transfer λ is small, requiring a large value for $\mid H_N(\theta) \mid$ of the loop filter to sustain a stable limit cycle. Moreover, since there is no or very limited correlation between the input signal and the error signal, an unwanted limit cycle is not to be expected in this case.

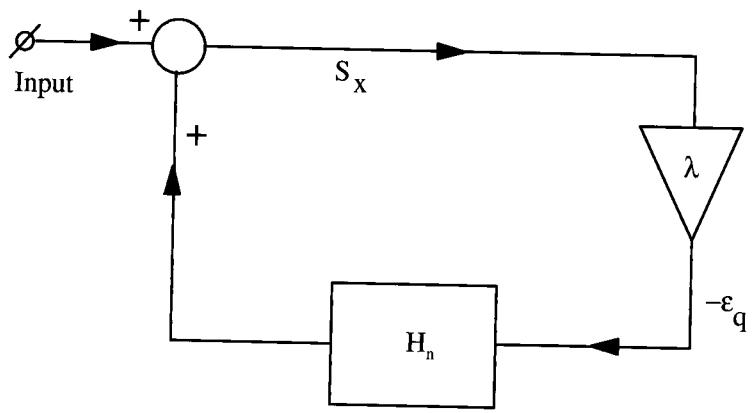


Figure 8.18: Stability analysis model for noise-shapers

8.5.2 Root Locus stability analysis method

The Root Locus method is a simple and easy to apply method to analyze the stability of a system. In case of a sampled data system, a stable region of the system is obtained when this region is inside the unit circle. The stability criterion using Figure 8.18 we have to analyze is:

$$\lambda H(z) = 1. \tag{8.49}$$

A system is stable when for all values of λ the roots of 8.49 are within the unit circle $\mid z \mid = 1$.

The following rules apply for the construction of a root locus.

1. Loci originate on poles and terminate on zero of $H(z)$.
2. The root locus on the real axis always lies in a section of the real axis to the left of an odd number of poles and zeros on the real axis.
3. The root locus is symmetrical with respect to the real axis.
4. The number of asymptotes is equal to the number of poles of $H(z)$, n_p, minus the number of zeros n_z.
5. The breakaway points are given by the roots of: $\frac{d(H(z))}{dz} = 0$

or by: $\mathrm{D(z)}\frac{dN(z)}{dz} - \mathrm{N(z)}\frac{dD(z)}{dz} = 0.$
with $H(z) = \frac{N(z)}{D(z)}$.

8.5.3 First-order system

In a first-order system $J(z) = z^{-1}$. The root locus starts at $z = 0$ and ends at $z = \infty$. Because of the feedback loop λ cannot be positive. In Figure 8.19 the root locus of the first order system is shown. The figure shows that

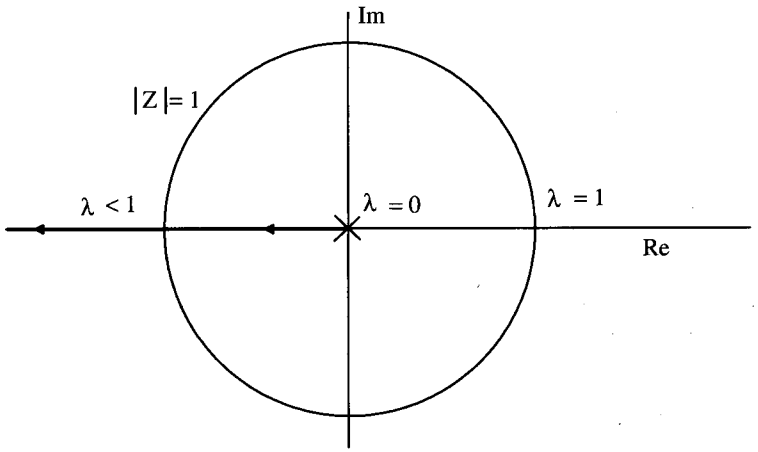


Figure 8.19: Root locus of a first-order system

for $z = -1$ ($f = \frac{1}{2}f_s$) and $\lambda = -1$ the system becomes instable. This instability, however, is required for the idle pattern of a noise-shaper.

8.5.4 Second-order system

In a second-order coder the filter function $J(z)$ is implemented by:

$$J(z) = z^{-1}(2 - z^{-1}) = \frac{2z - 1}{z^2}. \tag{8.50}$$

The root locus starts at the double pole $z = 0$ and ends at $z = 0.5$ and $z = \infty$. The breakaway points are obtained from:

$$z(1 - z) = 0, \tag{8.51}$$

resulting in $z = 0$ and z =1. The root locus of this system is shown in Figure 8.20. The circle is centered at $z = (0.5, 0)$ and has a radius of 0.5. Again this system becomes unstable for $z = -1$ and $\lambda = -\frac{1}{3}$. However, this instability is required and gives the idle pattern at half the sampling frequency.

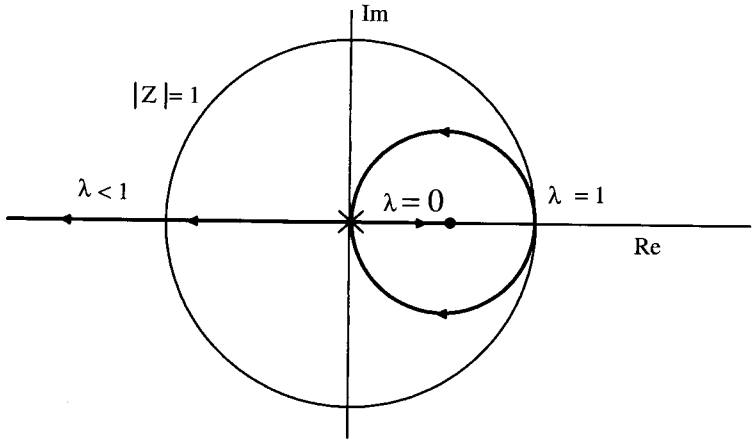


Figure 8.20: Root locus of a second-order system

8.5.5 Simulation of second order system

At the moment a second order 1-bit noise-shaping system is simulated, then the spectrum of the output signal with a small input signal is shown in Fig. 8.21. From this figure it can be seen that the expected idle pattern at half the sampling frequency is not found. The idle pattern is generated at one fourth of the sampling frequency. The given stability analysis does not predict this idle pattern at the practical found frequency. This means that the modeling of the 1-bit system is not covering this phenomenon. An improvement in modeling of this system seems to be required. This improved modeling will be discussed in one of the following sections.

8.5.6 Third-order system

A split-up between a 1-bit coder and a multi-bit coder is needed.

1-bit Coder implementation

A general implementation of a third-order coder filter can be written as:

$$J(z) = \frac{3(1 - a)z^2 - 3(1 - a^2)z + (1 - a^3)}{(z - a)^3}. \tag{8.52}$$

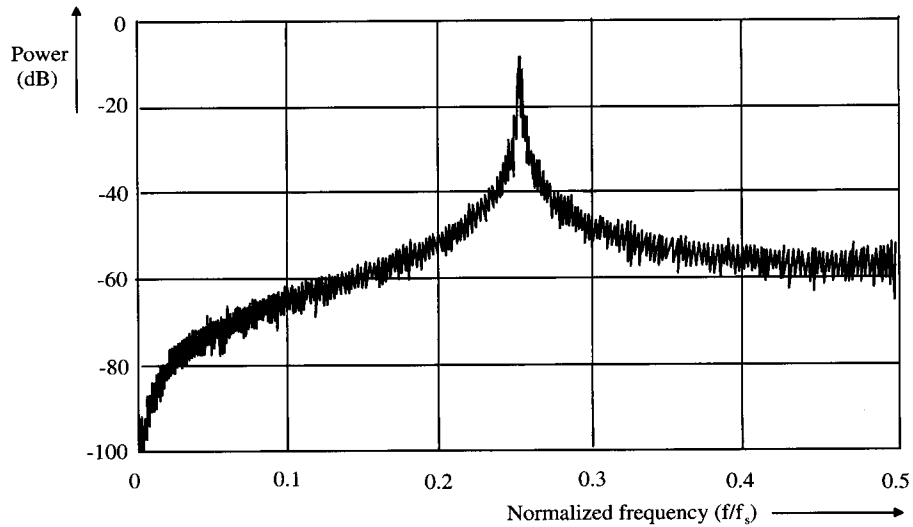


Figure 8.21: Small signal second order output spectrum

Here a determines the value of the stabilization function and $b = 1$. Inserting $a = 0.5$ in equation 8.52 we obtain:

$$J(z) = \frac{1.5z^2 - 2.25z + 0.875}{(z - 0.5)^3}. \tag{8.53}$$

The root locus of 8.53 starts at the three-fold pole $z = 0.5$ and ends at $z = \infty$ and

$$z_{1,2} = \frac{3}{4} \pm j\frac{1}{12}\sqrt{3}. \tag{8.54}$$

The breakaway points are found from:

$$(z - 0.5)^2(z - 1)^2 = 0. \tag{8.55}$$

The results are double points at $z = 0.5$ and $z = 1$. The circles are centered at $z = (\frac{3}{4}, \pm\frac{1}{12}\sqrt{3})$. The root locus of this system is shown in Figure 8.22. From the root locus figure it can be seen that the system becomes unstable with increasing λ. The value of λ for which the unit circle is crossed is determined by:

$$\lambda_0 = \frac{1}{1 + \left(\frac{2\cos(\alpha)}{1+a}\right)^n}. \tag{8.56}$$

n determines the filter order (n = 3, 4, 5, 6, etc.) and $\alpha = \frac{\pi}{n}$.
The derivation of equation 8.56 will be given in subsection 8.5.8.

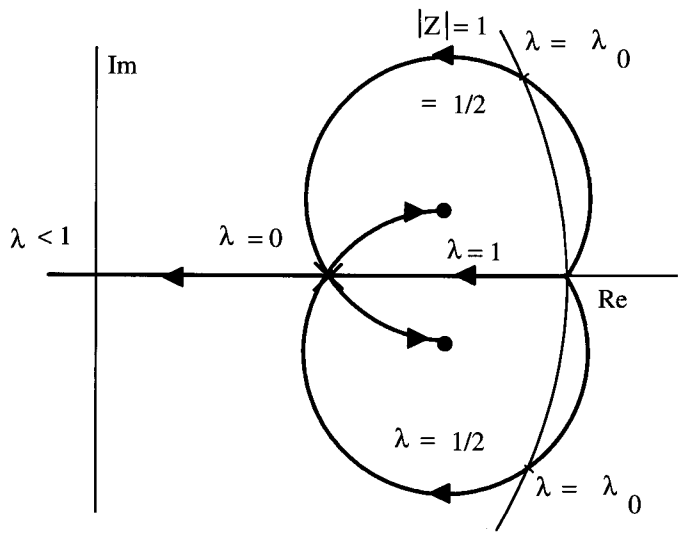


Figure 8.22: Root locus of a 1-bit third-order system

Inserting $n = 3$ and $a = 0.5$, we obtain for $\lambda_0 = 0.771$.
The value for λ_0 can also be obtained from the root locus plot. By graphically measuring the distance between the unity circle cross point and the zero and pole positions we obtain λ_0 from:

$$\frac{1}{\lambda_0} = \frac{1.5z_1z_2}{p_1^3}. \tag{8.57}$$

From the root locus plot we obtain: $z_1 = 0.29$, $z_2 = 0.55$, and $p_1 = 0.57$, resulting in $\lambda_0 \approx 0.774$. This graphically determined value is close to the exactly calculated value of 0.771. This means that the maximum gain of the quantizer in the loop may not exceed the value 0.771 to avoid unwanted limit cycles. A proper choice of input and output levels of the quantizer is required. Finally with $z = -1$ λ becomes -0.73.
So far using this analysis method it is not possible to determine the minimum value for a resulting in a stable value. Using extensive simulations it is possible to obtain this value as already given in an earlier section. Again a modification of the system modeling is required to be able to calculate rather accurately the edges of stability with a minimum value for a.

Multi-bit third-order system

In a multi-bit third-order system the value of a can be chosen 0. Then the filter function $J(z)$ changes into:

$$J(z) = z^{-1}(3 - 3z^{-1} + z^{-2}). \tag{8.58}$$

The root locus of this system starts from a triple pole at $z = 0$ and ends at $z_1 = \infty$ and

$$z_{2,3} = \frac{1}{2} \pm j\frac{1}{6}\sqrt{3}. \tag{8.59}$$

The circles are centered around $z = (\frac{1}{2}, \pm\frac{1}{6}\sqrt{3})$. The root locus of this system is shown in Figure 8.23. As can be seen from Figure 8.23, this system

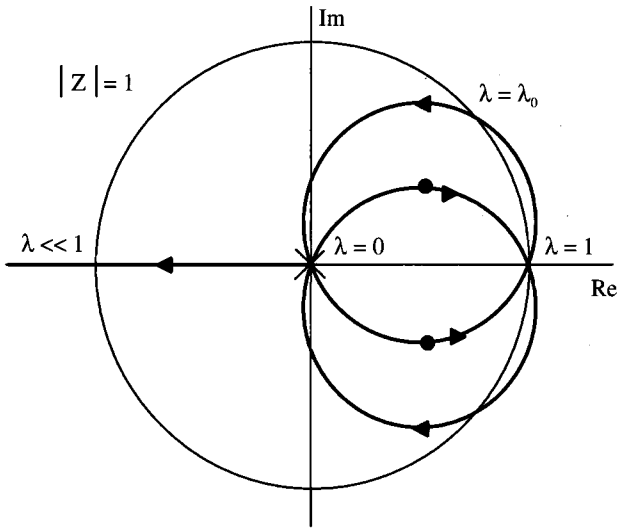


Figure 8.23: Root locus of a third-order multi-bit system

is unstable for $z = -1$. However, this instability is required as idle pattern at half the sampling frequency.

Using equation 8.56 the value of λ_0 for which the unit circle is crossed with $a = 0$ is found to be 0.5. When a multi-bit system is used, then the error is $(2^N - 1)$ times smaller than in a 1-bit system. As a result the value of

$$\frac{\lambda_0}{2^N - 1} \tag{8.60}$$

is smaller than 1 and the system will be stable. As a result, the third-order system becomes stable with $N \geq 2$, because the quantizer gain never exceeds 1.

8.5.7 Quantizer describing function model

In noise-shaping coders and sigma-delta converters a 1-bit quantizer is used. During stability analysis it is important to know the maximum or minimum gain of such a nonlinear system. Mostly a *describing function method* is used to obtain a first-order approximation of the gain as a function of the input signal [11].

In Figure 8.24 the nonlinear part of a quantizer including a limiter function is shown. The quantizer input signal is S_x, the output signal is S_0 and the error signal $-e_q = -(S_x - S_0)$. The limiter function is added to the system

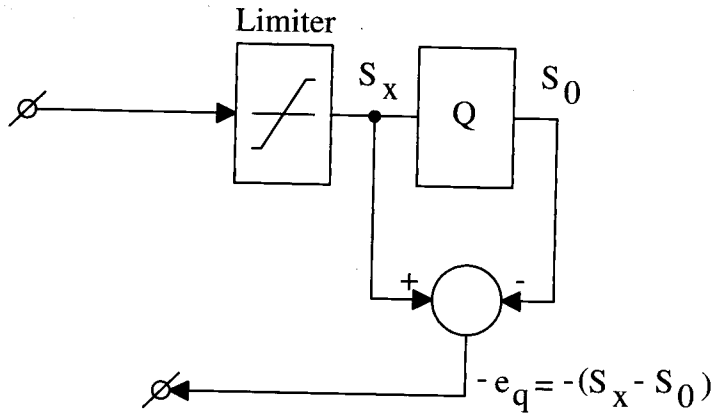


Figure 8.24: Nonlinear part of a quantizer function

to determine the maximal gain of the 1-bit quantizer, as will be shown in this section.

In a 1-bit coder two output levels $+A_0$ and $-A_0$ are available.
For a small input value, the quantizing error exceeds the input signal value, whereas for a large input value the limiter restricts the modulus of the quantizing error to $A_l - A_0$ in which with $A_l > A_0$ is the value at which overload starts. In Figure 8.25 the transfer function is shown. The global transfer λ of the nonlinear part of this system can be determined. A describing function of a non sampled system will be calculated.

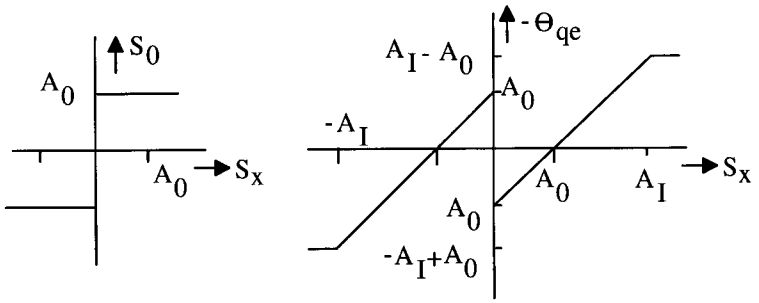


Figure 8.25: Input versus output of the nonlinear part of a 1-bit quantizer

Suppose at the input a square wave with amplitude A_b ($A_b > 0$) is present, then the error signal A_e also represents a square wave and A_e is obeying the following relations:

$$A_e = A_b - A_0 (A_b \leq A_l) \tag{8.61}$$

$$A_e = A_l - A_0 (A_b > A_l). \tag{8.62}$$

The global transfer λ_b in case of a square wave becomes:

$$\lambda_b = \frac{(A_b - A_0)}{A_b} (A_b \leq A_l) \tag{8.63}$$

$$\lambda_b = \frac{(A_l - A_0)}{A_b} (A_b > A_l). \tag{8.64}$$

The maximum value λ_m is obtained in case $A_b = A_l$.

In Figure 8.26 the global transfer λ as a function of input amplitude is shown. If a sine wave with an amplitude A_s ($A_s > 0$) is applied at the input, then the error signal is the sum of a square wave and a sine wave as shown in Figure 8.27. If $A_s \leq A_l$, then the amplitude of the fundamental A_f in the input signal is given by:

$$A_f = A_s - \frac{4}{\pi} A_0. \tag{8.65}$$

At the moment the input amplitude increases $A_s > A_l$, the limiter involves the addition to A_f of a term:

$$-A_s + \frac{2}{\pi} A_s \arcsin\left(\frac{A_l}{A_s}\right) + \frac{2}{\pi} \frac{A_l}{A_s} \sqrt{A_s^2 - A_l^2}. \tag{8.66}$$

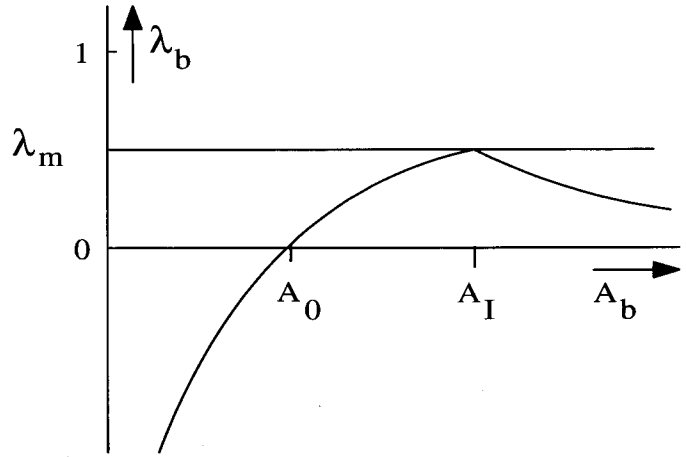


Figure 8.26: Global transfer λ as a function of the input amplitude A_b

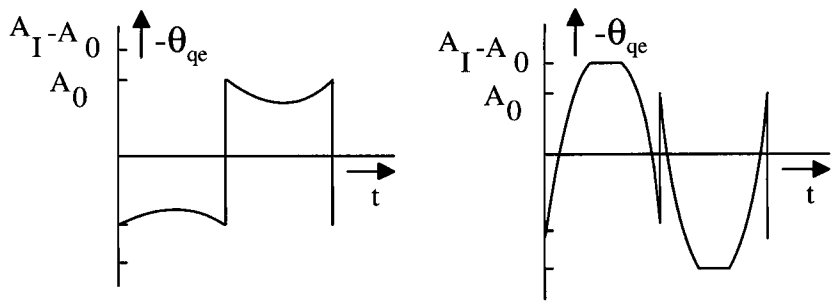


Figure 8.27: Quantizer error signal with a sine-wave input signal

The maximal value of the global transfer in case of a sine wave λ_s is slightly larger than the value of λ_s for $A_s = A_l$. Putting $A_s = A_l$ in 8.66 results in the approximation of λ_m in:

$$\lambda_m = 1 - \frac{4}{\pi}\frac{A_0}{A_l}. \tag{8.67}$$

In Figure 8.28 λ_s as a function of the input sine wave A_s is shown. From

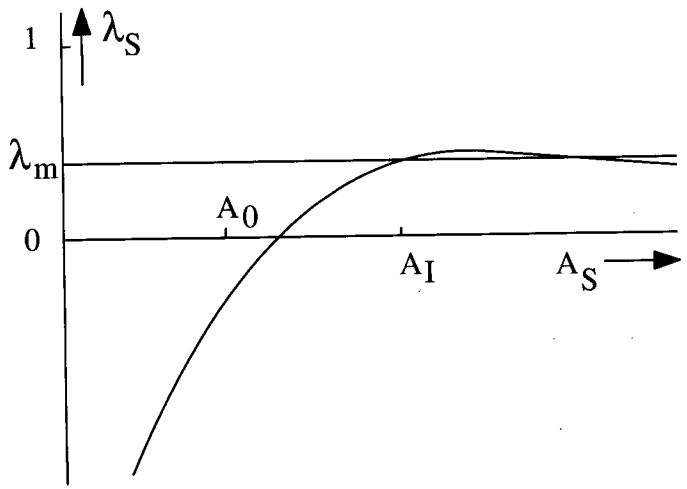


Figure 8.28: Global gain λ_s as a function of the input sine wave A_s

Figure 8.28 it can be estimated that the approximated maximal global gain λ_s is about 7.5 % too small at the moment $A_l = 2A_0$. With increasing A_l the error decreases showing that 8.67 is a sufficient approximation for gain and stability calculation purposes. The values of λ_b or λ_s range from $-\infty$ for small input values to a positive maximum λ_m in the proximity of A_l. The value of λ_m depends on the input waveform and is a function of the maximal input signal amplitude A_l and the output amplitude A_0. In Figure 8.29 the comparison of λ_m for the cases of a sine wave and a square wave as a function of the ratio $\frac{A_l}{A_0}$ show that the square wave gain is slightly larger than the sine wave gain. In a worst-case stability calculation, therefore, the square wave gain must be used. Furthermore, from Figure 8.29 the maximal gain as a function of the input limiter value and the output amplitude A_0 gives an important design parameter for noise-shaping coders (Chapter 8) or sigma-delta converters (Chapter 9). Using properly adjusted input limiter values A_l and output quantizer levels A_0, the maximal loop gain is fixed under nearly all input signal conditions.

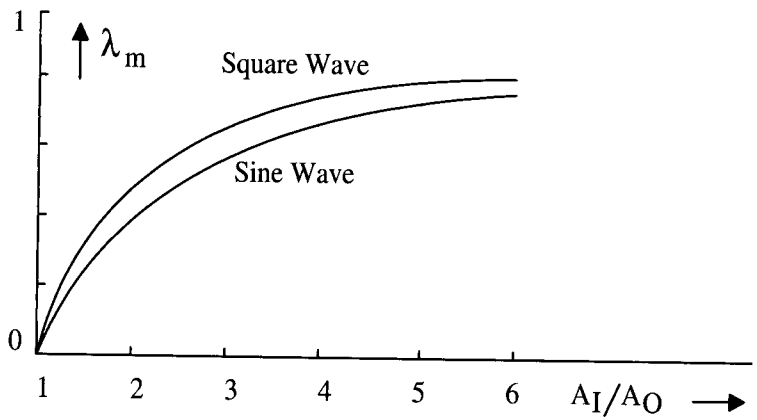


Figure 8.29: Comparison of sine wave and square wave maximal gain as a function of $\frac{A_l}{A_0}$

8.5.8 Maximum global gain calculation

The maximum global gain of higher-order system starting with a third-order system giving the edge of stability can be calculated.
Starting from the stability criterion:

$$\lambda J(z) = 1. \tag{8.68}$$

and inserting for $J(z)$:

$$J(z) = 1 - \frac{(z-b)^n}{(z-a)^n}. \tag{8.69}$$

we obtain:

$$\frac{(z-b)^n}{(z-a)^n} = 1 - \frac{1}{\lambda}. \tag{8.70}$$

Introducing the variable Λ with $\pm\Lambda^n = 1 - \frac{1}{\lambda}$ equation 8.70 changes into:

$$\frac{(z-b)^n}{(z-a)^n} = \pm\Lambda^n. \tag{8.71}$$

Taking the nth root of equation 8.71 we obtain:

$$\Lambda = \frac{(z-b)}{(z-a)}e^{-j\alpha}, \tag{8.72}$$

with $\alpha = k\frac{\pi}{n}$ and $k = 0, 1, .. , n-1$. Solving equation 8.72 for z we obtain:

$$z = \frac{\Lambda a e^{j\alpha} - b}{\Lambda e^{j\alpha} - 1}. \tag{8.73}$$

At the moment the root locus touches the unit circle we obtain: $\mid z^2 \mid = 1$. Inserting this value in equation 8.73, we obtain:

$$1 = \mid z^2 \mid = \frac{b^2 - 2ab\Lambda\cos(\alpha) + a^2\Lambda^2}{1 - 2\Lambda\cos(\alpha) + \Lambda^2}. \tag{8.74}$$

Solving Λ from equation 8.74 in case $b = 1$ we obtain:

$$\Lambda = \frac{2\cos(\alpha)}{(1+a)}. \tag{8.75}$$

The value of λ_0 can be found from $-\Lambda^n = 1 - \frac{1}{\lambda}$ and we obtain:

$$\lambda_0 = \frac{1}{1 + \left(\frac{2\cos(\alpha)}{(1+a)}\right)^n}, \tag{8.76}$$

with $\alpha = \frac{\pi}{n}$ and n is the filter order.

Note that only the negative value of Λ is used in equation 8.76 because the smallest value of λ_0 is restrictive for the stability.

The value of λ_0 is valid for values of a starting from 0 to nearly 1.

In Figure 8.30 the values of λ_0 as a function of a and the order of the loop filter are shown. When the maximum global gain is determined in a system, then the filter order and the stabilizing factor can be determined using Figure 8.30. Having determined the filter order and the stabilizing factor a, then the improvement in signal-to-noise ratio can be obtained using the curves from Figure 8.12 and Figure 8.14. The filter order can be optimally chosen in this way.

8.5.9 Extended quantizer model

In a single bit quantizer used in a noise shaping converter, an additional phenomenon is found. In the standard describing function method only the amplitude of the signal is used. However, in case the sampling of a sine wave at about one quarter of the sampling frequency is analyzed, then the following figure can be drawn (see Fig. 8.31) [142]. From this figure it can be deducted that at $\frac{f_s}{4}$ a phase uncertainty of $\pm\frac{\pi}{4}$ is introduced by the quantizer without changing the digital output data. The sine wave can change position as indicated by the dotted line without changing the output data of the quantizer. At other signal frequencies other phase uncertainties

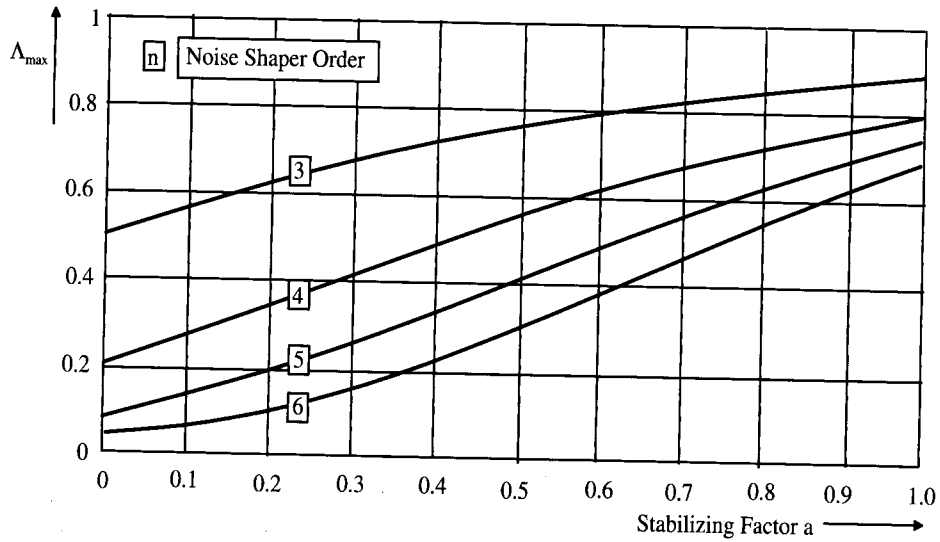


Figure 8.30: Global gain as a function of a and the loop filter order

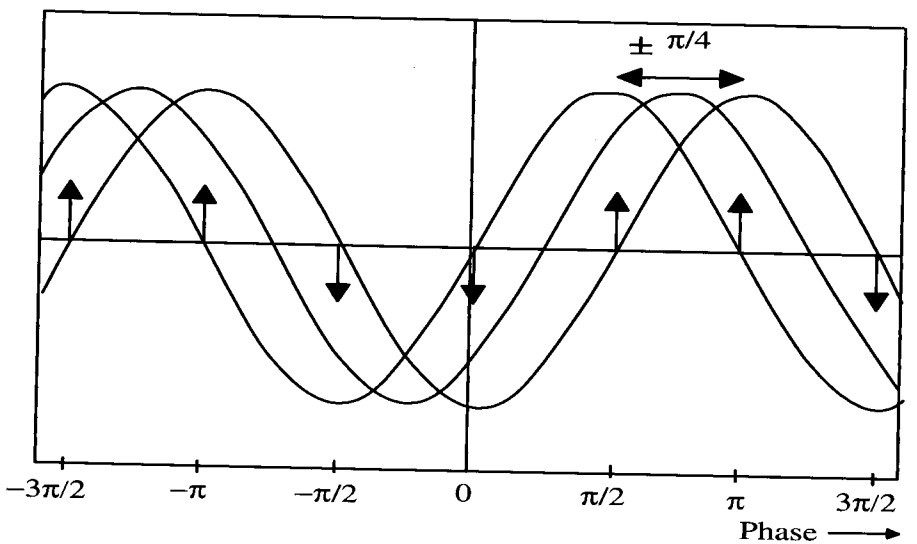


Figure 8.31: Phase uncertainty of a one bit quantizer at $\frac{f_s}{4}$

are found. The phase uncertainty will have a large influence on the stability of the 1-bit noise shaping converter as will be shown later on. The contour of the maximum phase uncertainty introduced by the quantizer is shown in Fig. 8.32. It must be noted, however, that at 0 Hz and at exactly $\frac{f_s}{2}$ the

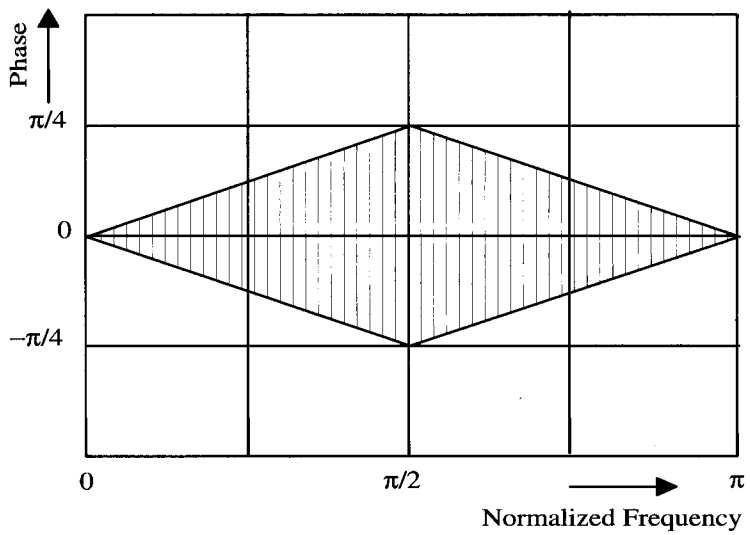


Figure 8.32: Maximum phase uncertainty piecewise linear model

phase of the quantizer and signal is not determined. When a small deviation from these frequencies is analyzed, then the phase uncertainty drops to a very small value as can be seen from Fig. 8.32. At other discrete frequencies again the phase uncertainty can drop to zero, however, the given piecewise linear plot marks the maximum phase uncertainty over the frequency range from 0 to half the sampling frequency. As a result of this operation the describing function method (from the previous sections) must be **extended** with a **gain and phase** component or:

$$Q(z) = \lambda e^{j\alpha\Delta\phi_{max}(\theta)} \tag{8.77}$$

with:

$$z = r.e^{j\theta} \tag{8.78}$$
$$\lambda \in [0, \infty) \tag{8.79}$$
$$\alpha \in [-1, 1] \tag{8.80}$$
$$\tag{8.81}$$

The criterion to predict limit cycles in a noise shaping converter changes into:

$$\lambda e^{j\alpha\Delta\phi_{max}(\theta)} H(z) = 1. \tag{8.82}$$

This criterion can be modified into an amplitude and phase requirement:

$$\lambda \mid H(e^{j\theta}) \mid = 1 \tag{8.83}$$
$$\alpha\Delta\phi_{max}(\theta) + Arg(H(e^{j\theta})) + \pi = 0. \tag{8.84}$$
$$\tag{8.85}$$

In this case $\alpha = \pm 1$ to obtain the worst case condition.

8.5.10 Root locus of second order system using extended quantizer model

Applying the extended criterion to a second order noise-shaper then the root locus as shown in Fig. 8.33 is obtained. This analysis clearly shows that a

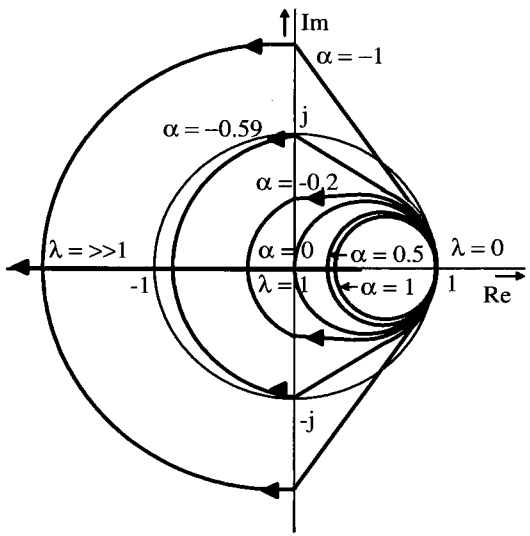


Figure 8.33: Root locus of a second order system using the extended quantizer model

second order system has an idle pattern at $\frac{f_s}{4}$.

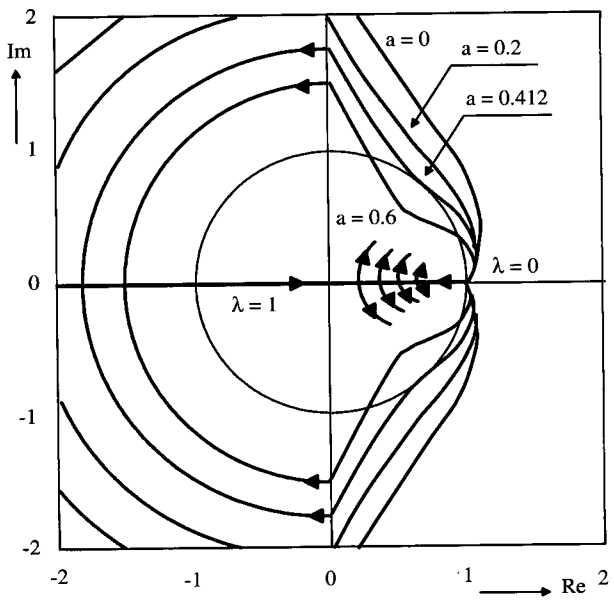


Figure 8.34: Root locus of a third order system using the extended quantizer model

8.5.11 Third order 1-bit system using the extended quantizer model

At the moment the extended quantizer model is applied to a third order system with a noise shaping filter specified by:

$$J(z) = 1 - \frac{(z-b)^n}{(z-a)^n} \quad \text{with n } = 3, \tag{8.86}$$

then the value of a can be determined using the root locus method. The value of b will be set at 1.
An extensive search gives the following result shown in Fig. 8.34. This search requires special software to obtain the shown result. The worst case value for $\alpha = \pm 1$ is used to determine this figure. The value of a can be determined from the figure and is obtained when the root locus intersects with the unit cycle determining the stability. It must be clear that the given figure shows a result optimized for a to be at the edge of stability. This result gives $a = 0.412$.
At the moment a larger value for a is used, then the root locus enters the unit circle. This means that the system becomes stable for small signals.

This intersection criterion can be applied for noise-shaping coders with orders larger than 3. The result has been given in table 8.1. In case a more detailed analysis is required then see [142]. These intersection results fit very well with simulations on practical systems and will therefore be used to determine the stability of noise-shaping coders. It must be noted that this criterion has only be applied to 1-bit systems. With multi-bit systems the criterion needs to be modified to reduce the phase uncertainty of the quantizer below the values used.

8.5.12 Multi-bit system analysis

The phase uncertainty criterion has been applied to multi-bit systems too. In Fig. 8.35 the phase uncertainty for a 3-level system (-0.5,), 0.5) has been shown. The phase uncertainty in this case is obtained by analyzing the phase difference of a sine wave at a quarter of the sampling frequency. The phase of the sine wave can be varied over the interval $\pm\frac{\pi}{6}$ before a change in digital output appears. This can be seen in general as:

$$\Delta\phi = \pm \arcsin(\frac{2}{n_{level}+1}), \text{ with } n_{level} \textit{ odd}. \tag{8.87}$$

Here n_{level} is the number of quantization levels in the A/D and D/A quantizer loop. In case of a 3-level quantizer the phase uncertainty becomes:

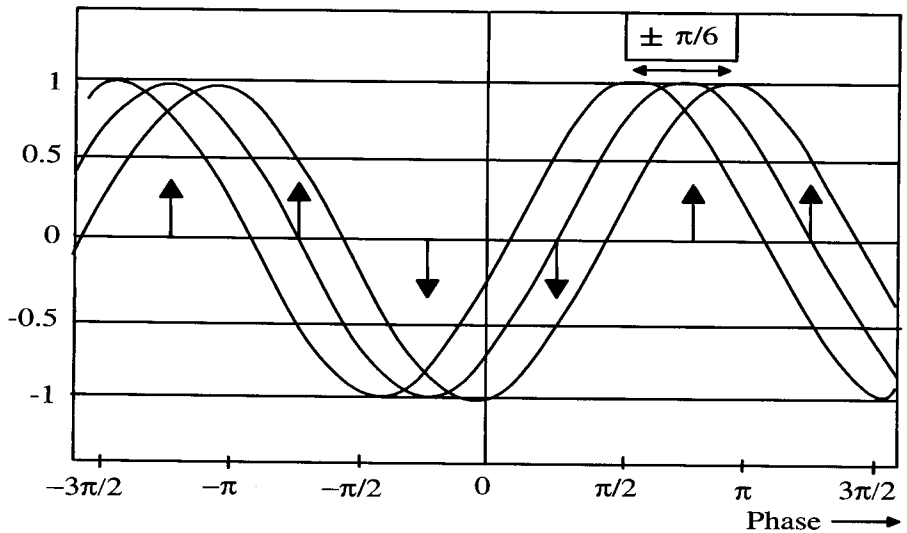


Figure 8.35: Multi-level phase uncertainty

$$\Delta\phi = \pm\frac{\pi}{6}. \tag{8.88}$$

At the moment the number of levels in the quantizer increases, then the phase uncertainty $\Delta\phi$ will decrease. The stability analysis using a variable phase uncertainty has been performed on noise-shaping coders using the following general noise-shaping filter specification:

$$1 - J(z) = \left(\frac{1 - bz^{-1}}{1 - az^{-1}}\right)^n. \tag{8.89}$$

Here $b = 1$ and a will be varied to obtain stability as a function of the phase uncertainty $\Delta\phi$. In Fig. 8.36 the results of this analysis for converters with noise-shaping filter of order 3 to 6 are shown. From this figure it is shown

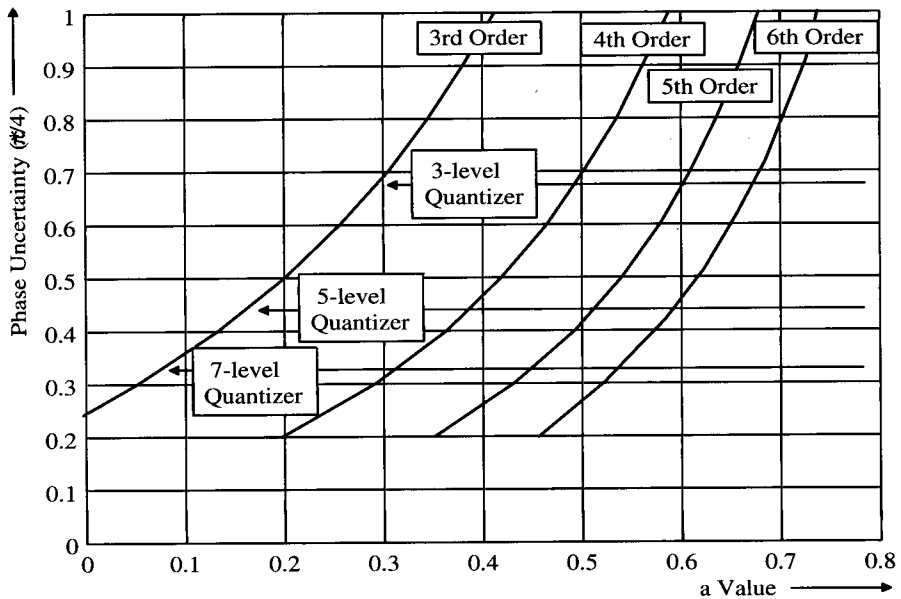


Figure 8.36: Multi-level phase analysis stability result

that up till a 7-level quantizer (3-bit) the phase uncertainty determines the stability of the converter. When more quantization levels are used, then the phase uncertainty has a minor influence on the small signal stability of the converter and therefore the standard root locus method can be applied. The values for a for the converters with different quantization levels and filter order can be determined from this figure. The following table shows the values for a as a function of quantizer levels and noise-shaping filter order.

	3rd Order	4th Order	5th Order	6th Order
3-level	0.29	0.49	0.60	0.67
5-level	0.16	0.38	0.51	0.59
7-level	0.07	0.31	0.44	0.54

Table 8.2: a-value data

From this table design values for small signal stability can be found for the most common filters. Systems with quantizers using more than 7-levels can be designed using the standard root locus method and for large signal stability limiters might be needed to obtain a stable system.

8.6 Practical noise-shaping D/A converters

In this section practical applications of noise shaping converters will be shown. Most of the practical examples are intended for digital audio system applications.

8.6.1 16-bit D/A converter system

In this section an example of a 16-bit noise-shaping D/A converter system will be described.

When an oversampling ratio of about 100 is used with a second-order noise-shaper, a 16-bit D/A converter for applications in digital audio systems can be designed.
In Figure 8.37 a block diagram of the total D/A converter is shown. At the input of the converter the 16-bits serial data are converted into 16-bits parallel data words with a sampling frequency f_s. This conversion is performed by the block called SIPO. The 16-bit parallel data is then increased in sample rate with a factor 4 using the first oversampling filter. This filter can be of the type shown in Figure 8.2. The output sampling rate is $4f_s$. A sharp filtering in the first four times oversampling filter is needed to reject the repeated input spectra of the digital signal with frequencies of f_s = 44.1 kHz, 88 kHz and 132 kHz. Then a second oversampling with a factor 64 is introduced. In this filter a linear interpolation with a factor 64 is used between two data points. As a result of this linear interpolation, a filtering with an amplitude response of $(\frac{\sin x}{x})^2$ is obtained. The output sample rate is now increased to $256f_s$. The second oversampling filter is

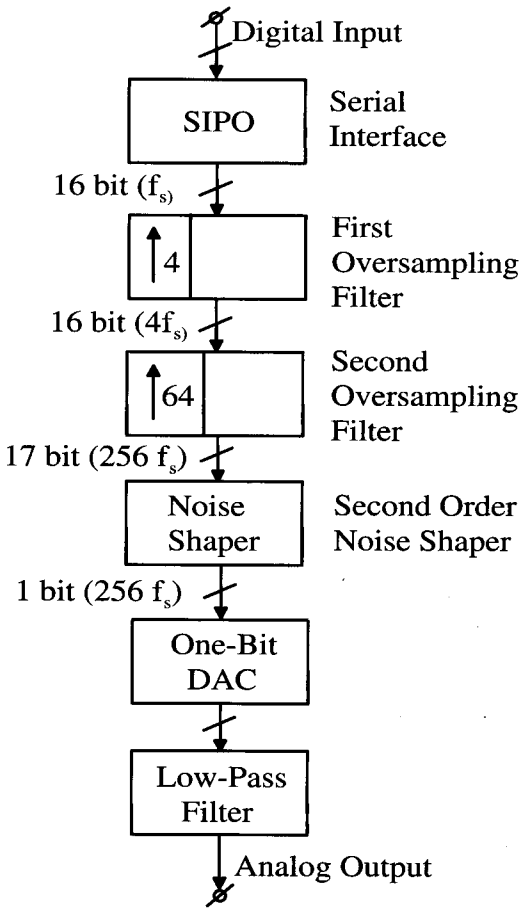


Figure 8.37: Block diagram of an oversampled D/A converter system [93]

followed by a second-order noise-shaper. The output of this noise-shaper is a 1-bit signal with a sample rate of $256 f_s$. This signal is applied to a 1-bit D/A converter that reproduces the analog signal. The output of the 1-bit D/A converter is followed by a linear phase low-pass filter to remove the high-frequency components from the audio signal.

In Figure 8.38 the amplitude response of the pass band of the total filter is shown. The amplitude decrease of the analog low-pass filter (Thomson Butterworth Thomson) is compensated for by an amplitude increase of the digital filter. As a result, a very accurate filtering characteristic is obtained with a very small pass-band ripple (less than 0.01 dB).

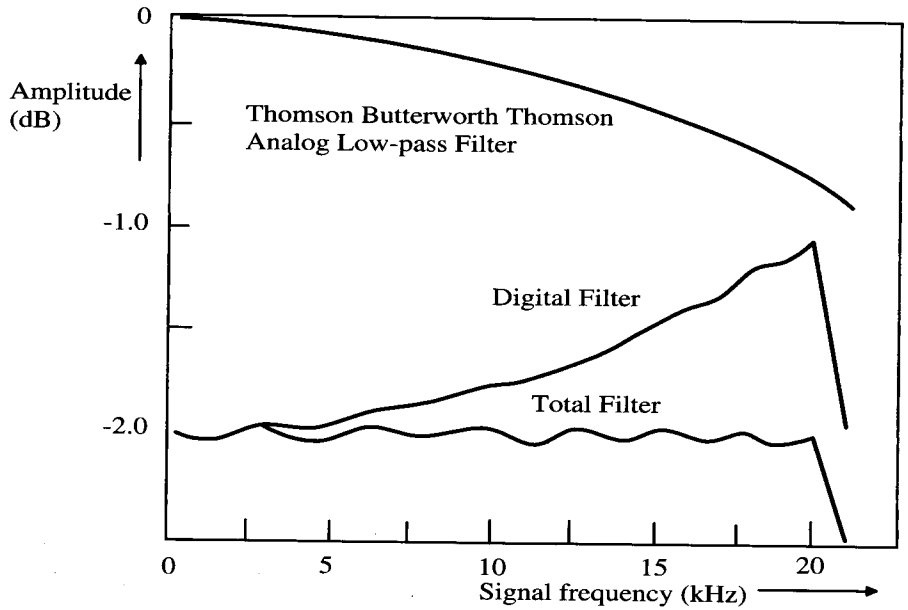


Figure 8.38: Pass band amplitude response [93]

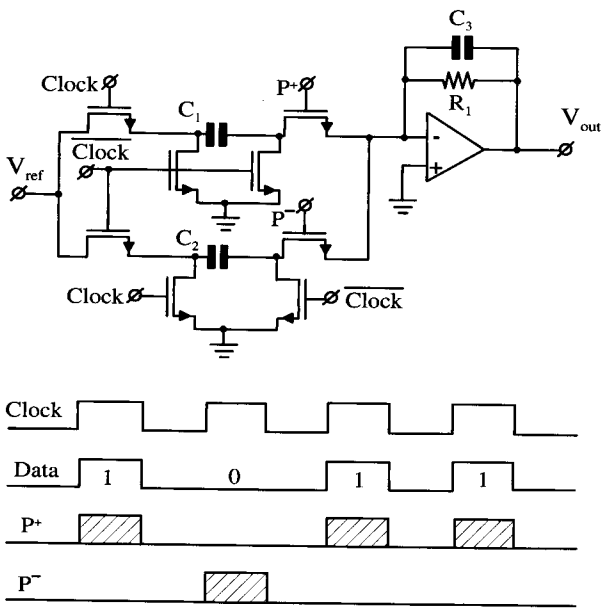


Figure 8.39: Switched capacitor 1-bit D/A converter [93]

In Figure 8.39 a switched capacitor implementation of a 1-bit D/A converter using a single reference voltage V_1 is shown. The system consists of a set of switches driven by the two phases of the clock signal CL. A charge "bucket" is stored in capacitors C_1 and C_2, respectively. The two switches driven by the signals P^+ and P^- determine if a charge packet ($Q = C_1V_1 = C_2V_1$) is added or subtracted from the output signal. The output signal is generated and filtered by C_3 and R_1 using an operational amplifier to keep the voltage swing at the input of this amplifier very small. The filter constant C_3R_1 is part of the analog low-pass output filter which suppresses the high frequency spectra of the signal. This analog output filter removes the high-frequency spectrum not sufficiently for audio applications. So extra analog filter sections are required to perform this operation. This means that pass-band flatness is determined by the analog output filter. So accurate elements are needed to construct this filter. Furthermore it is not possible to integrate such a filter together with the digital system part. Therefore a better solution is needed to obtain a fully integrated solution. In Fig. 8.40 the frequency spectrum of a 1-bit digital-to-analog converter output is shown. This figure shows that in the band of interest the quantization error is very small so a large dynamic range is obtained.

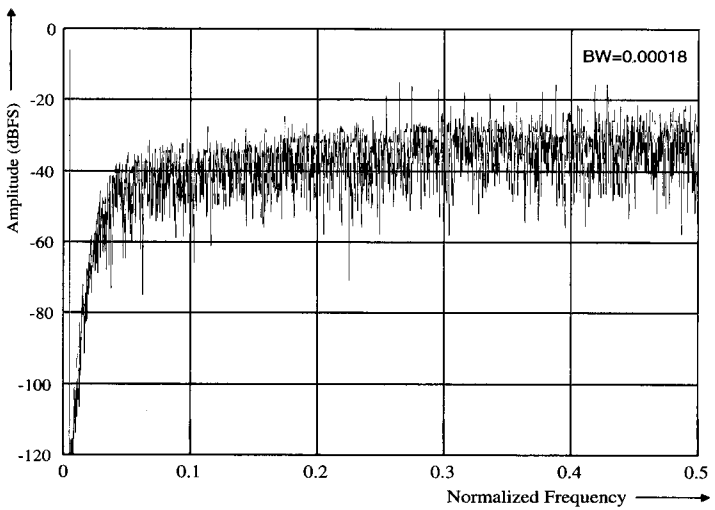


Figure 8.40: 1-bit D/A converter output spectrum

8.6.2 18-bit D/A converter system

The limiting factor in high resolution D/A converters based on 1-bit D/A converters with a large oversampling factor and a higher-order noise-shaper is found to be the analog switching part with the output operational amplifier(s) and analog output filters. In a practical design much attention must be paid to the analog signal reconstruction part of the converter [93]. The 18-bit example described in this section uses basically the same digital signal processing part as the system of the previous section. In a 5 V CMOS

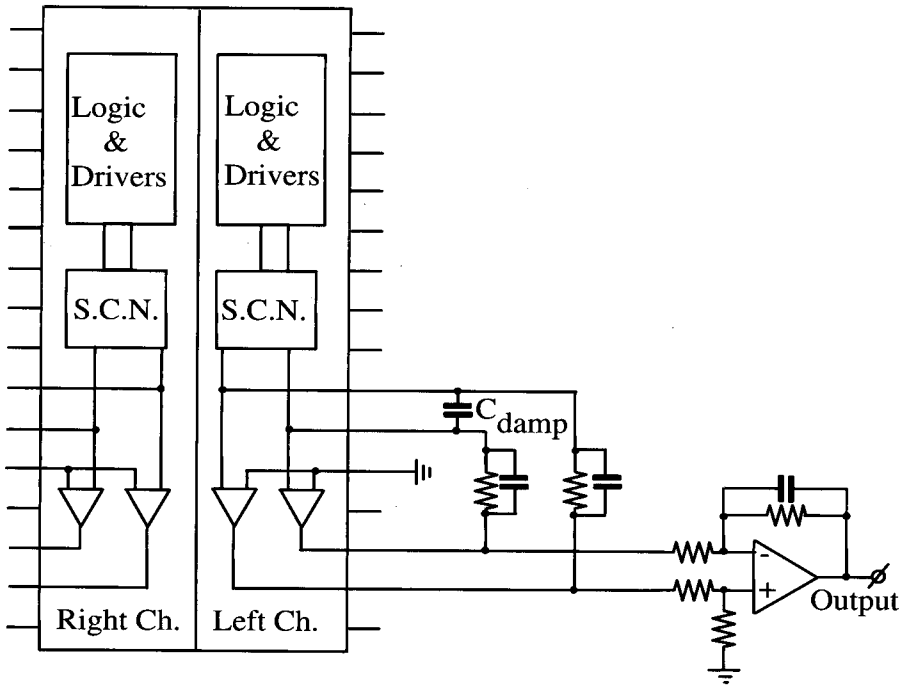


Figure 8.41: Differential 1-bit D/A converter implementation [93]

process the maximum analog signal swing is limited. The noise floor present in a system determines the maximum dynamic range of such a system. In a full differential system implementation the signal swing can be doubled without increasing the supply voltage. A maximum increase in dynamic range with 3-6 dB can be obtained, depending on the construction of the output amplifiers. The differential circuit implementation compensates for imperfections of, for example, switches and reduces the sensitivity of a system for supply voltage variations. In Figure 8.41 a fully differential circuit implementation of a dual 1-bit D/A converter is shown. The 1-bit D/A

converter part consists per channel out of a logic part with switch driver circuitry, a switched capacitor differential D/A network and two operational amplifiers with highly linear feedback elements and a differential-to-single ended output amplifier. The external feedback elements are used to obtain the extreme linearity required for 18-bits resolution and linearity. At the output of the two operational amplifiers driven by the differential switched capacitor network two counter phase analog signals appear. These two signals are subtracted to obtain the analog output signal of the converter. An external operational amplifier with feedback elements is used to perform this function. Although this amplifier can be seen as a disadvantage because not all elements are integrated with the digital chip, in case a breakdown of the system due to external large signals is performed, only this amplifier will break down. A low cost repair is then possible. Protection systems with extreme large power handling capability are difficult to design and can introduce extra distortion. In Figure 8.42 the circuit diagram of the differential switched capacitor D/A converter is shown. Note that in this

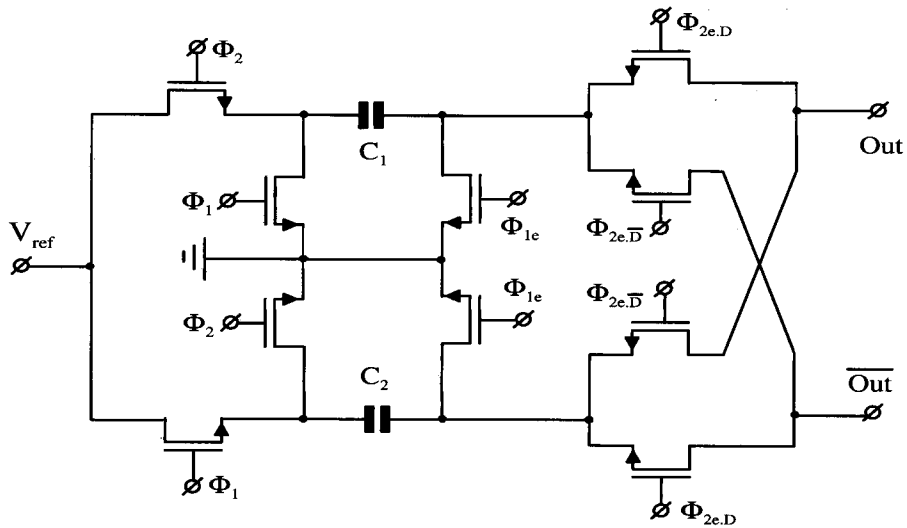


Figure 8.42: Differential switched capacitor D/A converter [93]

system again a single reference voltage is used for charging and discharging. Non overlapping clocks are needed to drive this system. The digital data are entered with the switches marked D and $\bar{D}$. In Figure 8.43 the timing diagram of the non-overlapping clocks is shown. Note that the output of the differential switched capacitor D/A converter is a charge. This charge is

converted into a voltage by the two operational amplifiers with the external feedback resistors.

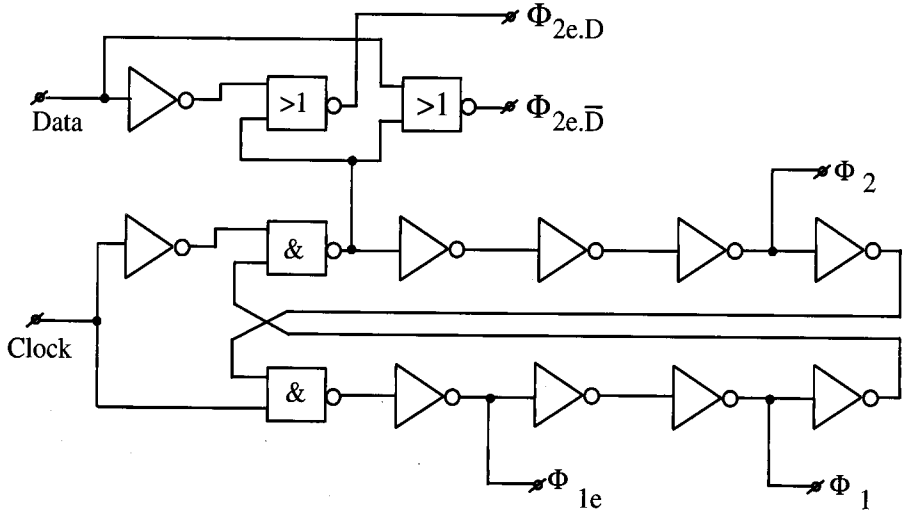


Figure 8.43: Timing diagram of non-overlapping clock signals [93]

The specifications of the 1-bit D/A converter are given in Table 8.3. These

THD + Noise (Input signal 0 dB)	-104 dB
Dynamic range (Input signal -24 dB)	108 dB
Signal to silence (idle pattern)	112 dB
Crosstalk between channels (f_{in} = 1 kHz)	110 dB
Power dissipation (+5 V and -5 V supply)	750 mW
Maximum clock frequency	10 MHz
Chip size	2.31 × 3.16 mm

Table 8.3: 1-bit D/A converter data [93]

measurements are performed with a third-order noise-shaper operating at a frequency of 192 times f_s. An 18-bit input data word with a sampling frequency of 44.1 kHz is applied to the system.

8.6.3 Continuous time FIR reconstruction filter D/A converter

A converter architecture that uses a Finite Impulse Response (FIR) reconstruction filter to avoid accuracy problems in the analog reconstruction filter is shown in Fig. 8.44 [151]. The system consists of a digital interpolation

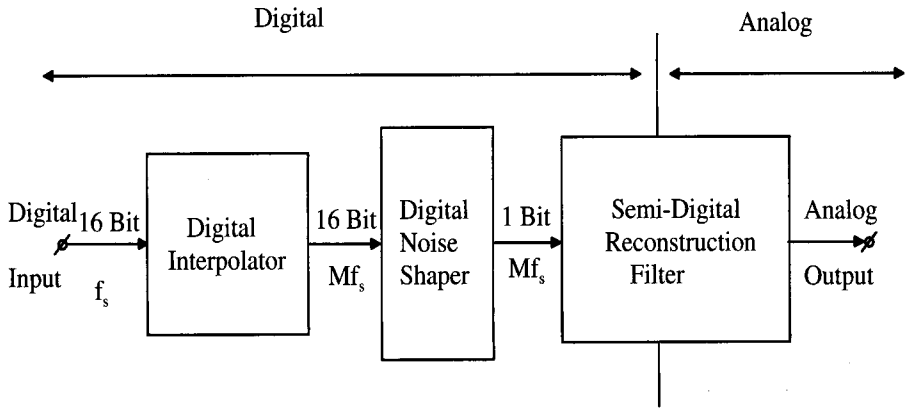


Figure 8.44: Continuous time FIR reconstruction filter D/A converter [151]

filter to perform the sample rate conversion, a digital second order noise shaper followed by the semi-digital reconstruction filter. The output of the noise-shaper is a 1-bit signal.
In the FIR reconstruction filter this signal is delayed and the different delayed signals switch analog currents that perform the digital to analog reconstruction. The filter is designed in such a way that with a simple analog output filter all the information above the base-band is rejected. Depending on the length of this filter the attenuation of the out of band signal can be adjusted to fulfill the required analog specification. The operation of the different parts in the filter are shown in Fig. 8.45. In Fig. 8.45(a) the spectrum of the digital input signal is shown. At the sampling frequency f_s and multiples of this sampling frequency the spectra are repeated. This repetition must be rejected so only the base-band part remains and will be reconstructed at the output terminal.
In Fig. 8.45(b) the output of the interpolation filter is shown. This operation is mostly performed in two or more stages to minimize hardware and power needed in this operation. The stopband attenuation is limited to 70 to 90 dB depending on the application. This is shown in the figure with a finite stopband attenuation range.

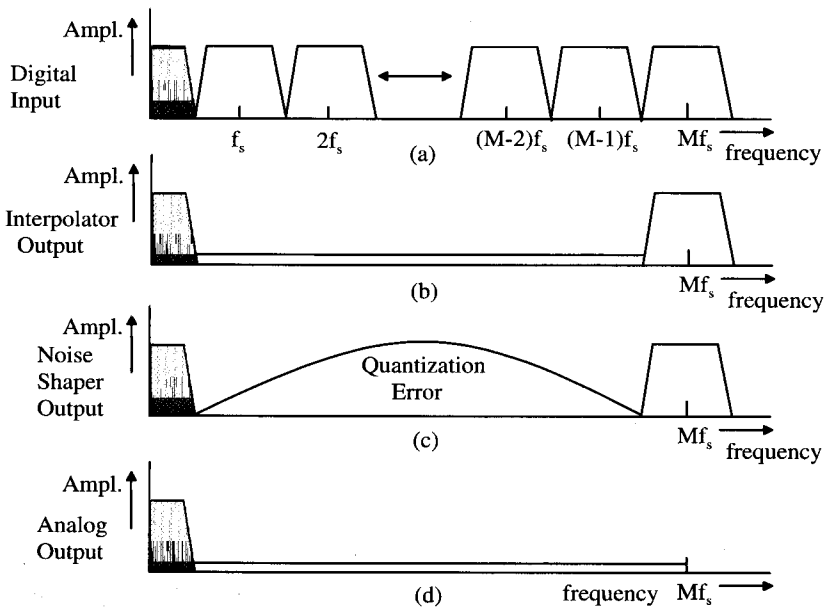


Figure 8.45: Different spectra of the filter response [151]

Then the noise-shaping takes place. The output data of the digital filter function is reduced to a 1-bit output signal. As a result of this noise-shaping operation the quantization error increases and is at its maximum at half the sampling frequency. This quantization error must be rejected by the reconstruction filter. This means that the stopband attenuation of the FIR reconstruction filter must increase strongly above the signal band. This depends on the coefficients of the design and the filter length as will be shown in one of the next figures.
Finally Fig. 8.45(d) shows the analog output signal including all the filtering performed in this converter.

8.6.4 Combined digital-analog FIR filter architecture

The architecture of the combined digital-analog FIR filter is shown in Fig. 8.46. In Fig. 8.46 the advantage of the single bit noise-shaper is shown. Using a n-bit shift register the digital information is delayed and the output signals of every delay stage switches the analog bit currents. These bit currents determined by the coefficients a_1 to a_n are summed to obtain the analog output signal. In this way an analog FIR filter has been constructed. The accuracy of the coefficients only determine the stop band attenuation

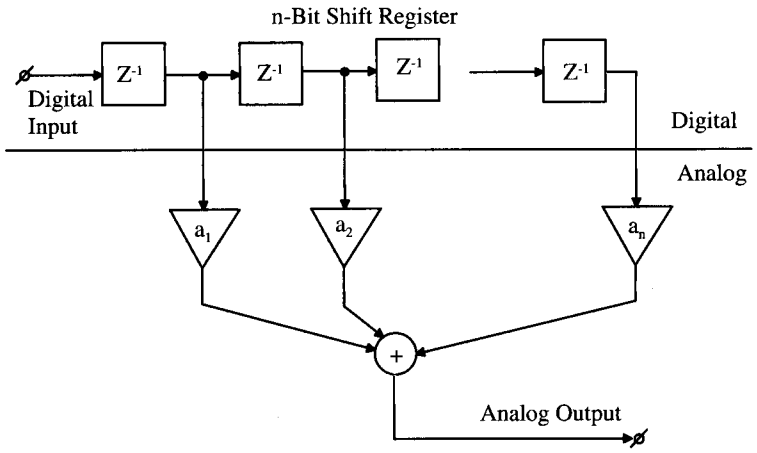


Figure 8.46: Combined digital-analog FIR filter implementation

in a certain frequency band. The 1-bit currents, if ideally switched, do not have any influence on the distortion of the converter. The practical implementation of the system is shown in Fig. 8.47. The value of the currents a_1, a_2 to a_{128} is determined by sizing the lower transistors connected to a reference voltage V_{ref}. As mentioned before the absolute accuracy only influences the stopband attenuation and not the linearity and distortion. The cascode stages are added to make the currents independent of supply voltages and furthermore reduce the output capacitance of the current sources before these are applied to the switches. The switches determine if a current is added to the output reconstructed current or not. In this filter the stopband attenuation is more than 70 dB. As a result of this requirement a 128 bit filter length is required. The output signal of the filter is converted into a voltage using an operational amplifier with the feedback resistor R_l. The capacitor C_l forms with the resistor a first order low-pass filter that rejects the high frequency base-band image at 176 times the input sampling frequency. A 176 times oversampling ratio is used in this design. With this large oversampling ratio the high frequency image can be reduced sufficiently as will be shown in one of the following figures.

8.6.5 FIR filter response

The response of the 128 bit analog FIR is shown in Fig. 8.48. From this figure it is good to see that at high signal frequencies the stopband attenuation increases to a very high value ($\geq$ 80 dB). This increase in attenuation is

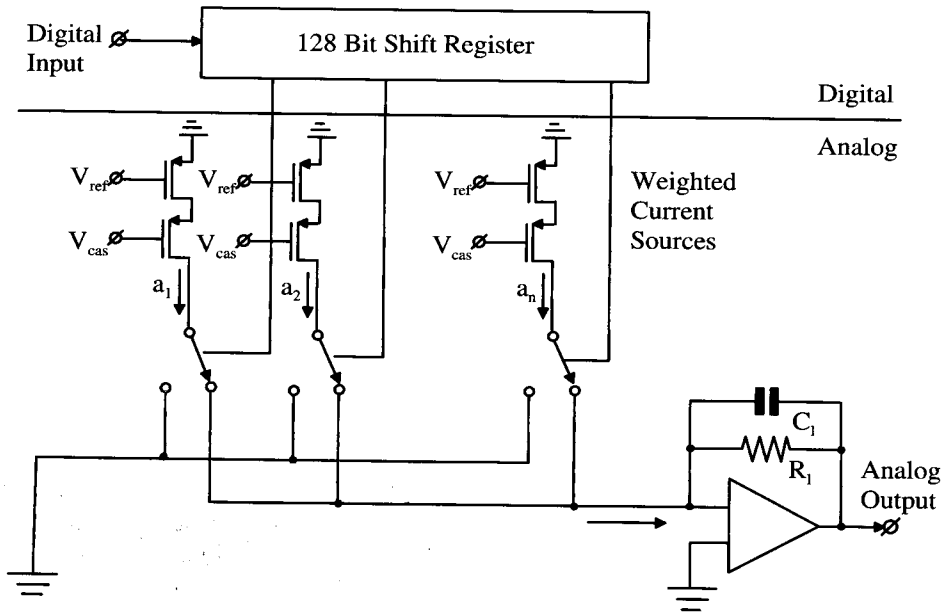


Figure 8.47: Practical FIR filter implementation [151]

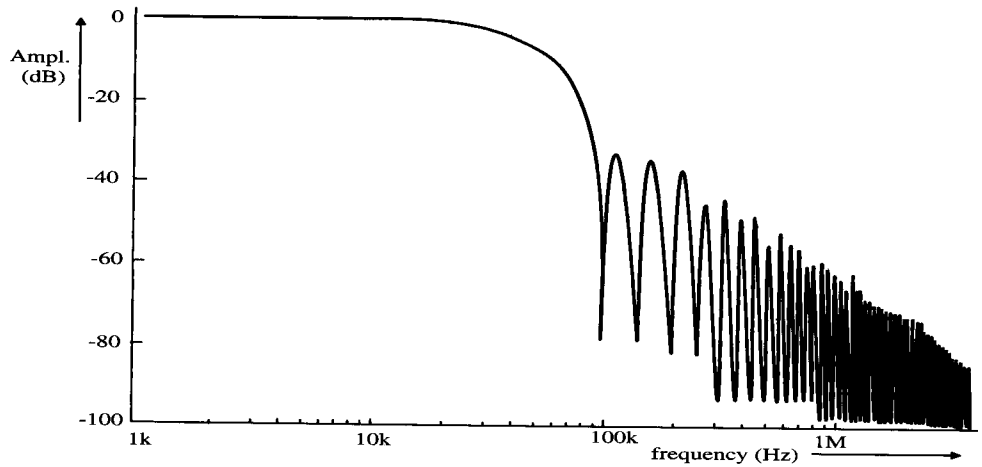


Figure 8.48: 128-bit FIR filter response [151]

required to filter out the quantization error introduced by the noise shaper.

8.6.6 Total filter response

Finally the combination of digital and analog filtering results in the overall filter characteristic shown in Fig. 8.49. In this figure the output signal of

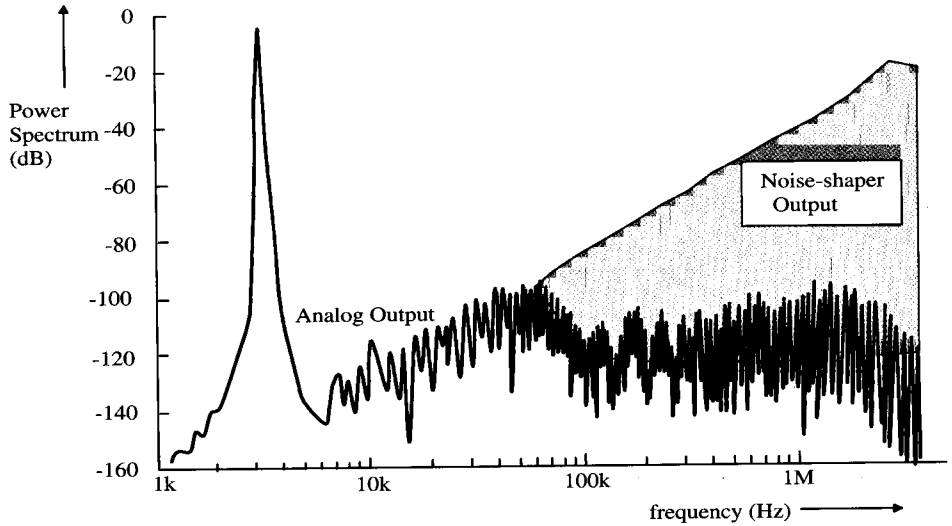


Figure 8.49: Total filter response [151]

the noise shaper is shown in gray color. This single part is rejected by the increased FIR stopband attenuation so nearly a flat stopband attenuation is obtained in the whole filter. An attenuation in the order of 80 dB is shown. Due to some decrease in rejection at the stopband edge the specification of at least 70 dB is obtained.

8.6.7 Converter specification

The specifications of the converter are shown in table 8.4. These specifications show that a fully integrated oversampling digital-to-analog converter with an on chip full performance analog output filter can be designed. Depending on the requirements these specifications can still be improved without increasing the die size. Furthermore it is possible to use a differential output signal by converting the non-used output currents into an output voltage using a second operational amplifier with feedback elements. In this way a doubling of the output signal is obtained with only a 3 dB increase in

Noise Shaping	Second Order
Oversampling Ratio	176
Dynamic Range	94 dB
Peak SNDR	88 dB
Power dissipation (+5 V and ± 1 mA Output Current)	59 mW
Stopband Attenuation	72 dB
Active Die Size (1.2 μ m CMOS)	3 mm^2

Table 8.4: FIR filter D/A converter specification [151]

output noise. This means again an improvement in dynamic range with 3 dB. This is very important in low-voltage designs with a very high dynamic range.

8.7 Multi-bit noise-shaping D/A converter

The only way to increase the dynamic range of an oversampling converter without increasing the sampling frequency or the order of the filter function is obtained by using a multi-bit D/A converter function. The advantage of the 1-bit converter over the multi-bit converter is found in the inherent linearity of such a converter. A disadvantage of the 1-bit approach is the shaping of the noise into the high-frequency band. A large signal and noise amplitude may cause inter-modulation errors in the analog part of the D/A converter. These inter-modulation products often appear in the audio band giving, audible non-harmonic distortion. The multi-bit approach reduces the level of the out-of band quantization signals at high output levels, while at small signal levels the well-known 1-bit operation is obtained. Furthermore the smaller out-of band signals can be rejected with a simpler analog post filter before this output signal is applied to for example an audio power amplifier. However, the multi-bit approach requires a D/A linearity equal to the full resolution of the system. Such a linearity is difficult to obtain without using calibration techniques. In this section multi-bit noise-shaping converters will be described.

8.7.1 Multi-bit system configuration

The architecture of the multi-bit D/A converter is shown in Figure 8.50 [94]. Before the oversampled signal can be applied to this converter a pre-

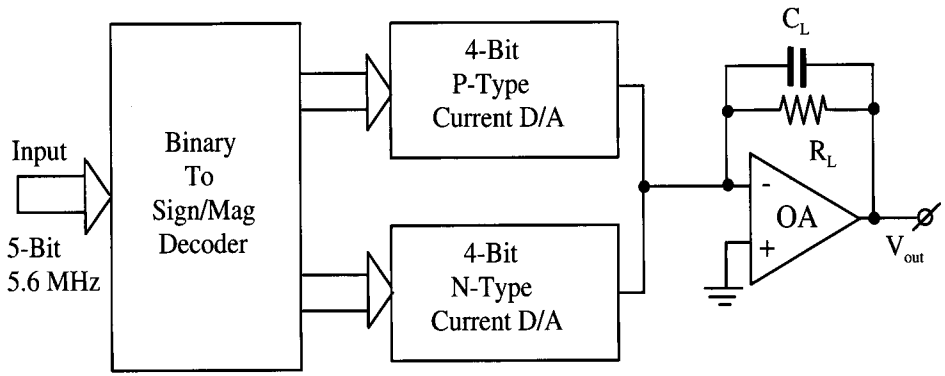


Figure 8.50: Multi-bit D/A converter architecture [94]

processing of the data will take place. In general an oversampling filter that converts the input data with a sampling rate of 44.1 kHz into a 5.6 MHz sampling rate is mostly used. This oversampling can take place in a couple of cascaded digital filters to minimize the system complexity and reduce the element count. Then a noise shaper will be applied. In this special application a third-order noise-shaper converts the data of the oversampling filter into a 5-bit noise-shaped code that is applied to the 5-bit D/A converter to reconstruct the analog output signal. In this section only the 5-bit D/A converter will be discussed. The preprocessing part has been already shown in previous sections of this chapter.

When in a D/A converter the dynamic range is increased, then the noise present on the individual bit-values may become in the same order of magnitude as the quantization noise of the system. This is especially true when offset binary coding is used and small signals are generated. The noise present on the most significant bit values in such a case may have the same order of magnitude as the quantization noise. To overcome this problem a sign-magnitude coding is used to drive the multi-bit D/A converter. In the sign-magnitude coding the bit values in case of a bipolar signal depend linearly on the signal amplitude. As a result, the noise depends on these bit-values, thus increasing the dynamic range of the D/A converter. The sign-magnitude D/A converter consists of a 4-bit P-type D/A converter and a 4-bit N-type D/A converter implemented in a CMOS technology. The output currents of both D/A converters are converted into a voltage using an operational amplifier with a feedback network. To obtain the required linearity of the P- and N-type D/A converters a self-calibration procedure is used. The combination of the two 4-bit D/A converters results in an overall

resolution of 5-bits.

8.7.2 Detail of sign-magnitude converter

In Figure 8.51 a more detailed system diagram of the sign-magnitude D/A converter is shown. In a 4-bit D/A converter system 15 equal current sources

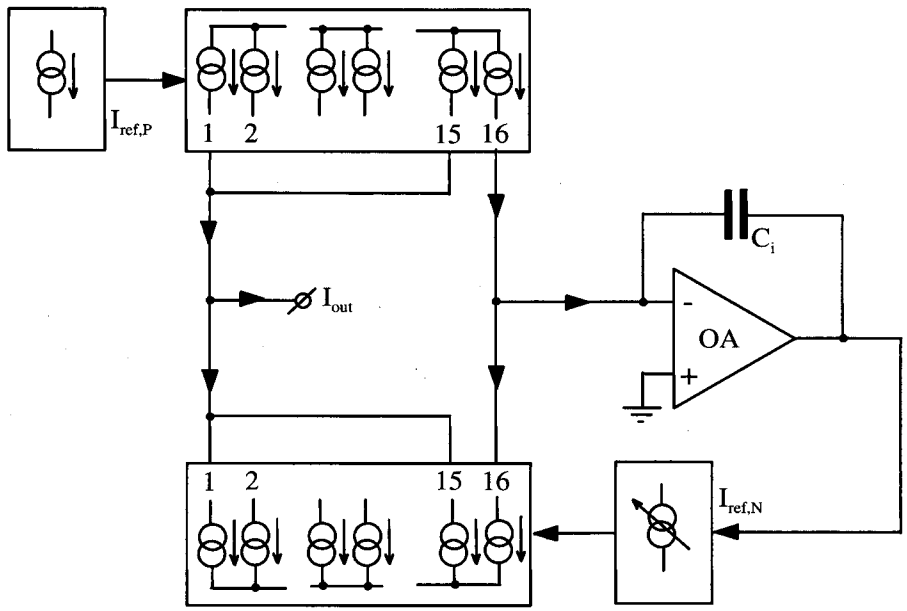


Figure 8.51: Detailed sign-magnitude D/A converter system [94]

can be used to obtain the required resolution. In this system an extra current source is used to calibrate the scale factor of the P-type D/A converter current to the N-type converter current. An operational amplifier is used to control the reference current source I_{refN} of the N-type D/A converter. In this way an accurate calibration of the N-type scale factor is obtained. The operational amplifier is configured as an integrator. In this way an averaging of the signals is obtained.

8.7.3 Sign-magnitude self-calibration system

In Figure 8.52 a detail of the self-calibration system is shown. The part inside the dashed line and marked *common* is used for all of the current sources of the converter. Concentrating on the P-type converter part the transistor M_{P1} is biased by the voltage V_{refP} and conducts about 90% of the reference

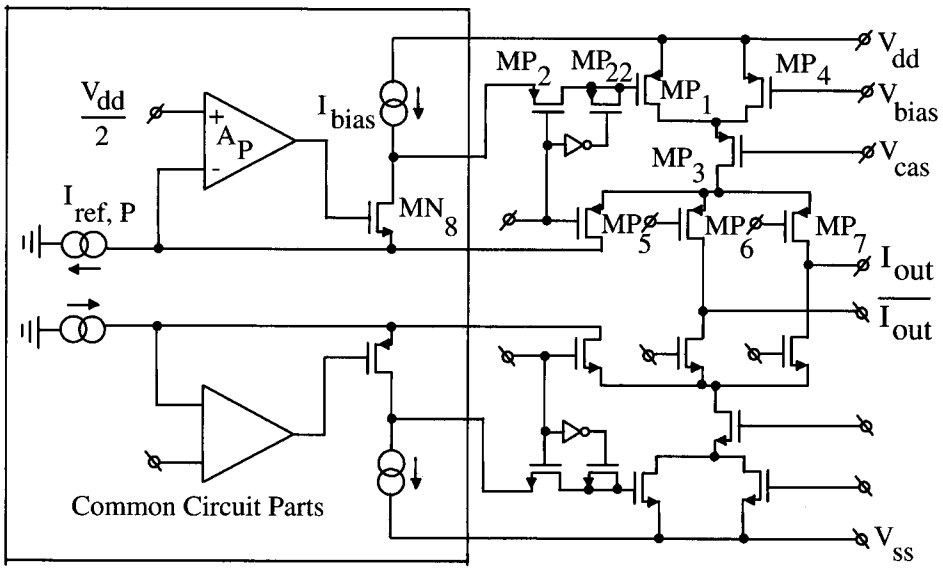


Figure 8.52: Detail of a sign-magnitude self-calibration system [94]

current. Transistor M_{P2} conducts the error current necessary to calibrate the total current of M_{P1} plus M_{P2} to I_{refP}. During the calibration cycle transistor M_{P4} is active. At the end of the calibration cycle the current is available to the converter. Depending on the input data word, either transistor M_{P5} or transistor M_{P6} is active. The current in either case is applied to the *dump* line or the output line I_{out}. The operational amplifier A_P controls the drain voltage of transistor M_{P5} at the level V_{refOUT} resulting in equal biasing conditions during calibration and during output current generation. An identical explanation is valid for the N-type D/A converter. A more detailed explanation of the self-calibration system has been given in Chapter 6.

8.7.4 Total system implementation

The total analog subsystem has been implemented in a 1.6μm CMOS technology. The integral non-linearity of the system is limited to 90 dB at full scale. No special attention has been paid to push this linearity to 120 dB. At smaller signal levels the dynamic range increases while distortion remains at 90 dB. In Figure 8.53 the measured spectrum of a 1 kHz output signal attenuated -84 dB with respect to full scale is shown. The spectral component at 2.75 kHz introduced by the self-calibration system is found at a level of -130

dB referred to full scale. In Table 8.5 the specifications of the analog D/A

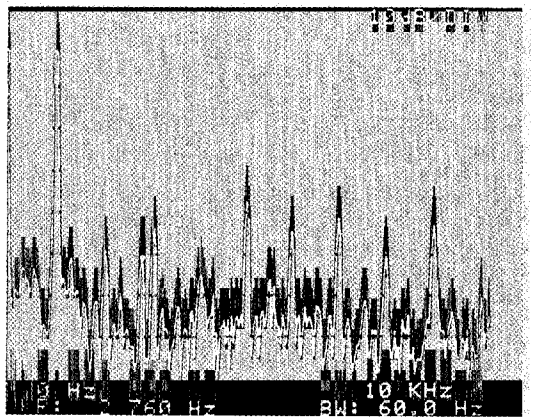


Figure 8.53: Output spectrum of a 1 kHz signal attenuated 84 dB [94]

converter system are given. Using the multi-bit system configuration a high

Output current	$\pm$ 1 mA
S/(N + THD) at 0 dB	90 dB
at -60 dB	55 dB
Sample frequency	5.6 MHz
Supply voltage	5 V
Power dissipation	100 mW
Temperature range	-10 to 70^0 C
Process	1.6 μm CMOS
Active chip area	7.5 mm^2

Table 8.5: Multi-bit D/A converter specification [94]

performance D/A converter can be designed with a limited oversampling frequency.

8.7.5 Multi-bit digital-to-analog converter using randomized Dynamic Element Matching

In noise shaping coders a large oversampling ratio is used. This means that only a small part of the output spectrum contains the wanted information while the remaining part is rejected by the output filtering. Using this idea it

is possible to use Dynamic Element Matching without filtering to obtain the very high matching accuracy needed in 24-bit digital-to-analog converter for super audio signal reconstruction. Different architectures using non-filtered dynamically matched elements will be discussed.

8.7.6 Non-filtered DEM D/A architecture

The basis architecture using non-filtered Dynamic Element Matching routines is shown in Fig. 8.54. In this figure only the digital-to-analog converter

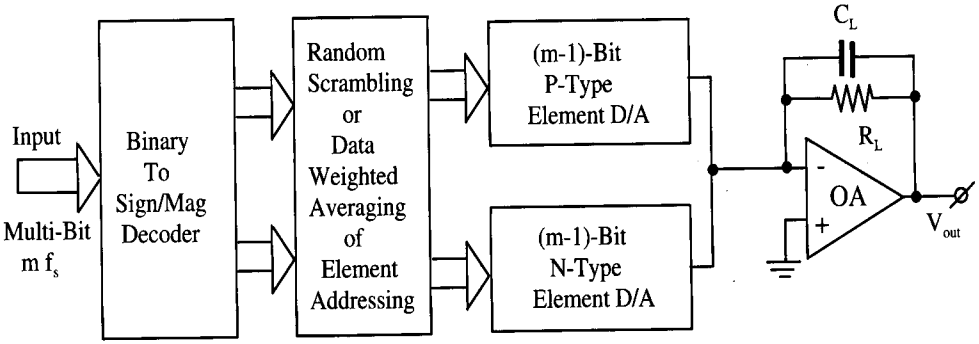


Figure 8.54: Non-filtered DEM D/A architecture

architecture is shown. At the input a multi-bit digital input is applied with a sampling frequency equal to mf_s with f_s the sampling frequency of the non-oversampled D/A input signal. The oversampled binary input data is converted into a Sign-magnitude thermometer code. The output of the encoder is applied to the randomizer. This randomizer shuffles the output data in such a manner that the correlation between the different D/A samples is minimized. In this manner the errors introduced by the DEM algorithm are randomly distributed over the out-of band quantization signal. In this way no extra filtering is required in the D/A converter. The output of the randomizer drives the P-type and N-type D/A elements that perform the digital-to-analog conversion and reconstruct the analog value. The output signal is filtered in the operational amplifier with the feedback elements R_L, C_L. In literature different ways of designing the randomizer are used. [152, 153, 159, 158].

8.7.7 Resistive element DEM D/A converter

The implementation of a differential resistor based DEM digital-to-analog converter using a randomizer to minimize the repetitive element mismatch errors is shown in Fig. 8.55. In this example only a 4 level D/A converter

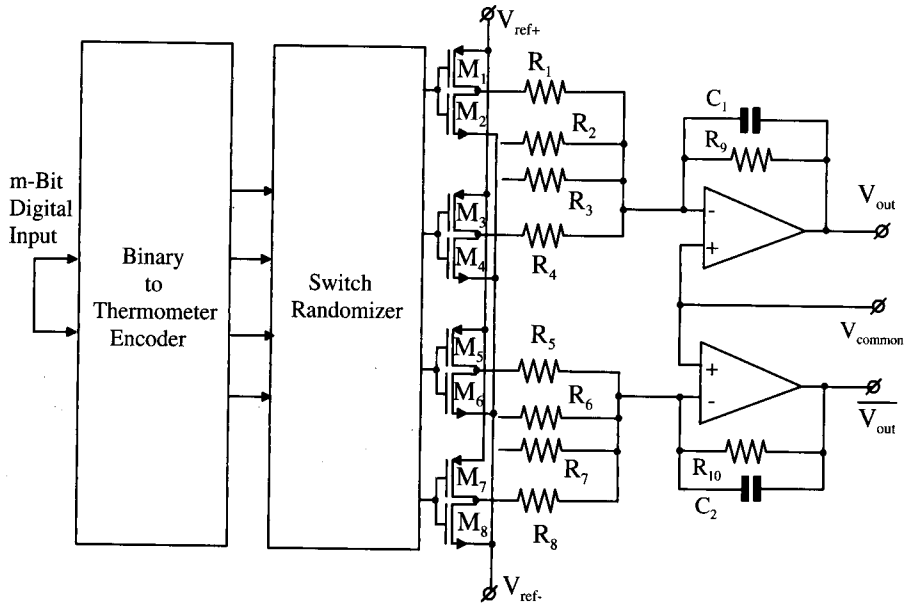


Figure 8.55: Resistive element randomized DEM D/A converter [152]

using resistors is shown. In practice this system can be extended to more bits (5 to 6 binary coded bits). The output of the binary to thermometer encoder is applied to the switch randomizer. This randomizer addresses the switches that are needed to reconstruct the analog output signal. The digital-to-analog converter uses equal valued resistors with a finite matching accuracy. By randomly addressing the resistor network and filtering the output with the differential output amplifiers having feedback networks R_9, C_1 and R_{10}, C_2, the averaging takes place. It must be noted that the frequency with which the randomization takes place must be as high as possible to obtain a good averaging and smearing out of the error spectra over the out-of band quantization band. With the switches the resistors are connected to the positive reference voltage V_{ref+} or the negative reference voltage V_{ref-} depending on the input data. In this way per output channel a bipolar output signal is obtained. It must be clear that opposite data is applied to the second channel to obtain the $\overline{V}_{out}$ signal. In general resistors

show a very good matching (better than 0.1 % depending on the size), so the error ripple introduced by the DEM algorithm is already small. During the design of this D/A converter the "on" resistance of the switches must be small with respect to the resistor value. This will make the matching of the resistors independent of the MOS devices.

8.7.8 Randomizer system

The architecture of a randomizer is shown in Fig. 8.56 [152]. This is a so called butterfly randomizer because of the cross coupling between the different channels. At the positions indicated with S_p switches are present that transfer the (digital) data to the same channel or couple it to a neighbouring channel. The switches are driven with a random signal generator. In this way a randomization between the input data and the output data takes place. It must be clear that as a randomizer more possibilities exist. This is up to the designer to determine what structure he wants to use.

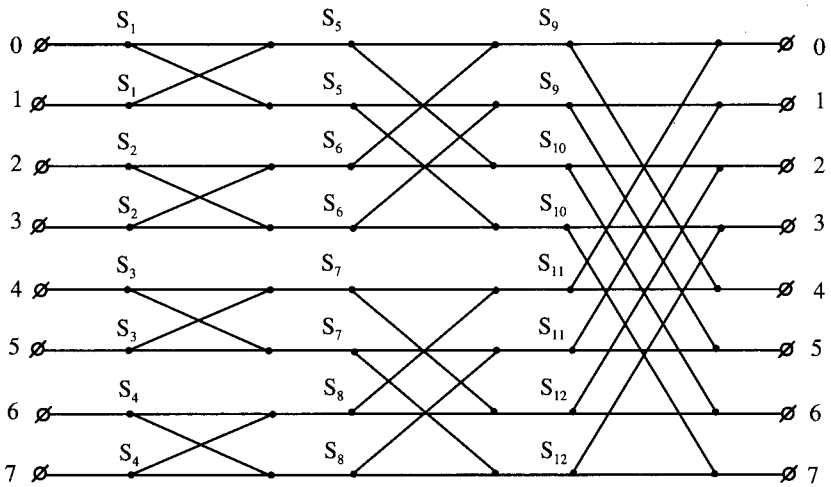


Figure 8.56: Butterfly randomizer [152]

8.7.9 Super audio 24-bit D/A converter

The architecture of a 24-bit super audio digital-to-analog converter using capacitive multi-bit randomization is shown in Fig. 8.57. This architecture performs as a complete digital-to-analog conversion for super audio reproduction with 24-bit resolution. At the input a programmable 50/15 μsec

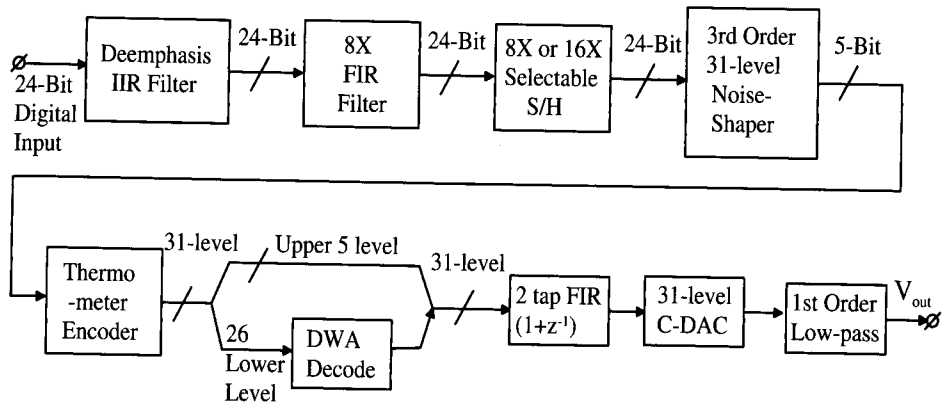


Figure 8.57: Super audio 24-bit D/A converter architecture [161]

deemphasis is used followed by an eight times FIR interpolation filter. After this filter a fist order hold function is used. With this hold function it is possible to obtain a second interpolation with eight or sixteen times increase in sampling frequency. Then a third order noise shaper is used to reduce the number of bits in the system from 24-bit to 5-bit. The 5-bit binary coded signal is converted into a 31-level thermometer code. The output of the thermometer encoder is applied to the randomizer that will apply signals to the DEM capacitive D/A reconstruction converter. In this system only the 26 lower bits are applied to the randomizer. Here a Data Weighted Averaging is applied. The upper 5-bits are directly coupled to the D/A converter. In this converter two time delayed capacitive D/A converters are used for the reconstruction. This time delay reduces the jitter sensitivity of the converter. This delay is introduced by the 2 tap FIR filter having a transfer of $1 + z^{-1}$. The data of the 2 tap FIR filter are applied to two 31-level capacitive D/A converters to perform the signal reconstruction. At the output a first order filtering is used to reduce the high frequency signal band from the output spectrum. The DWA algorithm minimizes the errors introduced by the mismatch of the unit capacitors used in the D/A converter.

8.7.10 15-level capacitive DEM D/A converter

The circuit diagram of a 15-level unit capacitive digital-to-analog converter is shown in fig. 8.58 [161]. This 15-level circuit is used to explain the operation of the circuit. When the clock ϕ_1 is high, then all input capacitors C_1 to C_{15} are at one side connected to ground. Then depending on the input data

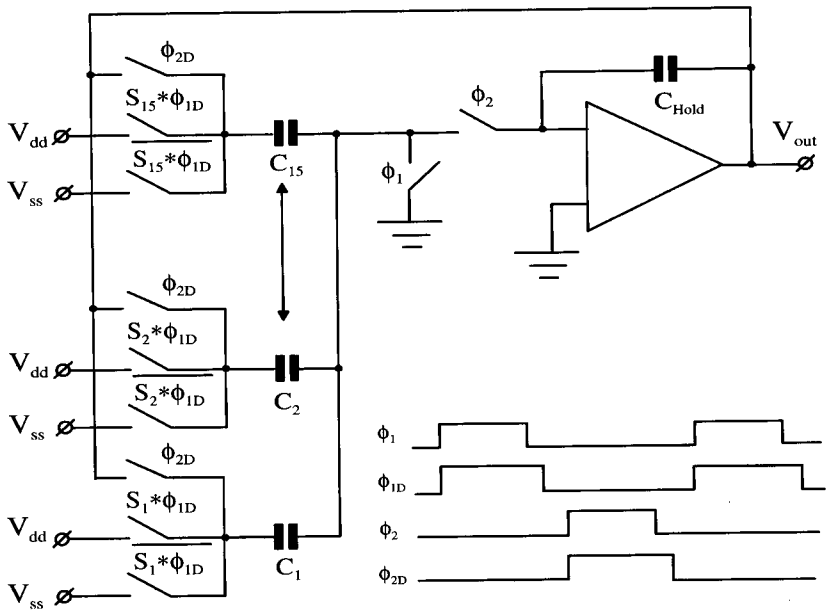


Figure 8.58: Switched capacitor 15-level DEM D/A converter [161]

the capacitors are charged to V_{dd} or V_{ss} by closing the appropriate switches $S_1, \overline{S_1}$ to $S_{15}, \overline{S_{15}}$. Then switch ϕ_1 is opened and delayed in time $S_1, \overline{S_1}$ to $S_{15}, \overline{S_{15}}$ are opened. Input data is stored as charge on the capacitors C_1 to C_{15}. Then switches ϕ_2 and ϕ_{2D} are closed. The charge on the input capacitors is now redistributed with the hold capacitor C_{hold} to obtain the analog output signal. Then the switches are opened and the following data are applied to the input capacitors. The connection of the input capacitors with the hold capacitor avoids slewing of the operational amplifier resulting in a reduced distortion at this point.

8.7.11 Differential dual 31-level DEM D/A converter

A differential dual 31-level switched capacitor DEM D/A converter circuit diagram is shown in Fig. 8.59 [160]. The circuit uses two times interleaved 31-level capacitor array D/A converters per channel. Charge redistribution is a again used between the input capacitors and the hold capacitor C_1 or C_2. The operation of the circuit is identical to the circuit given in Fig. 8.58. The input data is supplied by the partial Data Weighted Averaging system. This data is delayed with 1 clock cycle in the Register before it is applied to the second 31-level capacitive array. Furthermore the charge redistribution

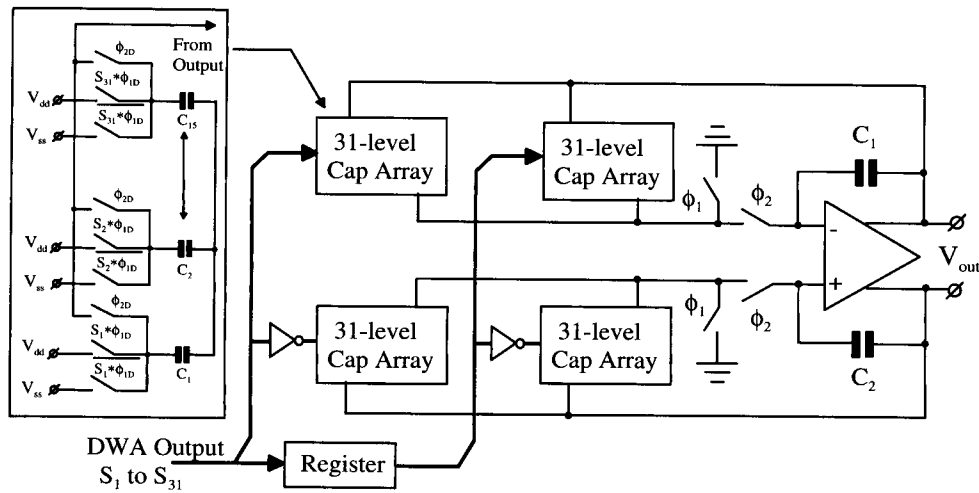


Figure 8.59: Dual 31-level switched capacitor DEM D/A converter [160]

takes place at the same moment. This construction reduces the effect of circuit clock jitter on the performance of the total converter.

8.7.12 Third order noise-shaper architecture

The architecture of the third order noise-shaper used in the 24-bit converter is shown in Fig. 8.60. The gain stage G_1 is introduced to avoid large signal limit cycles. Furthermore the feedback path B_1 introduces an extra notch in the noise shaping function at 20 kHz to decrease the quantization error over the total audio signal band. The input 24-bit data signal is reduced into a 5-bit output data signal with nearly no reduction in dynamic range.

8.7.13 Comparison between conventional DWA and partial DWA system architecture

The effect of the partial DWA algorithm is compared to the conventional DWA algorithm. The simulated result is shown in Fig. 8.61. A capacitor matching of 0.2 % is used. From this figure it is clearly seen that the partial DWA algorithm decreases the distortion and the deviation from the ideal S/N curve significantly.

8.7.14 24-bit D/A converter performance

The performance data of a 24-bit converter is shown in table 8.6. The

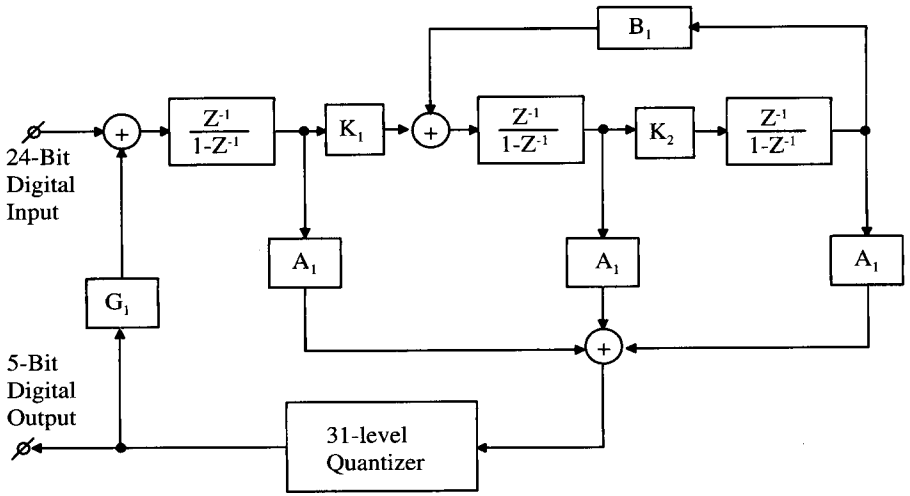


Figure 8.60: Third order noise-shaper architecture [160]

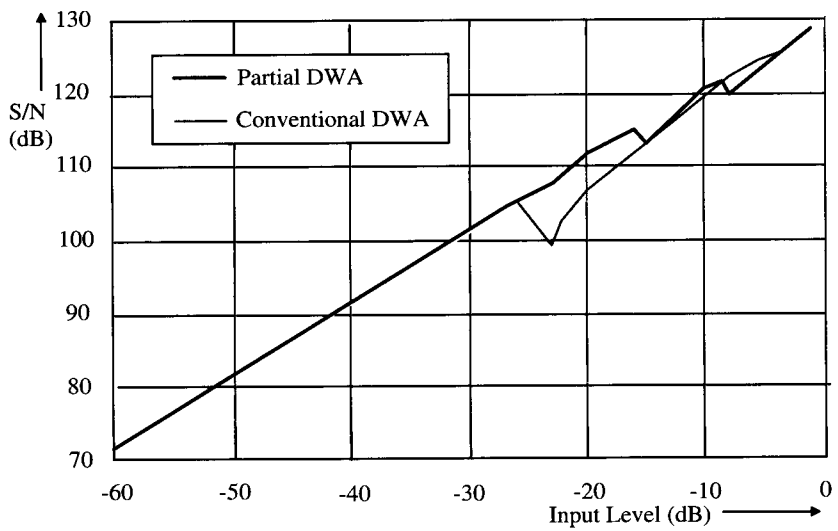


Figure 8.61: Comparison between conventional and partial DWA algorithm [160]

Output Voltage	$\pm$ 2.5 V_{pp} (differential)
Dynamic range	117 dB (20 kHz)
(-60 dB, 1 kHz)	120 dB (A-weight)
S/(N + THD) (0 dB, 1 kHz)	98 dB (20 kHz)
Supply voltage	5 V (analog)
	3.3 V (digital)
Power dissipation	290 mW (total)
	278 mW (analog)
Process	0.5 μm DPTM CMOS
Active chip area	7.8 mm^2

Table 8.6: 24-bit converter specification [160]

analog bandwidth used for measuring is 20 kHz while the input sampling frequency is 44.1 kHz. This table shows that a very good performance for the oversampling converter can be obtained. Scaling of technology using for example a 1.2 V supply will have a large impact on the dynamic range of the system. The output swing is expected to be reduced to 1.4 V_{pp} differential. This means that the noise in the system must be reduced with a factor two, resulting mostly in a large increase in current and thus analog power dissipation. In case the high voltage option of a submicron technology is used, then the output swing can be maintained at 2.5 V_{pp} differential and the power dissipation will not increase significantly.

8.8 Conclusion

Noise-shaping coders are excellent alternatives to conventional digital-to-analog converters for applications in largely oversampled digital audio and digital video systems. The 1-bit digital-to analog converter needs only two, or in special configurations one, reference voltage to perform the conversion. In these systems an excellent differential linearity with small input signals is obtained. The noise-shaping action randomizes the quantization noise rather well. Especially at small input signals the performance of the total conversion system is improved. The combination of the noise-shaping oversampling filter with the output filter function minimizes the component count, introduces a nearly linear phase response, and seems to be a very attractive alternative for digital audio signal conversion. A combination of an analog transversal filter function with a current based digital-to-analog converter

shows a fully integrated digital-to-analog converter function without needing external out-of band analog signal filtering. When the maximum clock rate is limited, an increase in dynamic range can be obtained by combining a multi-bit D/A converter function with a noise-shaping function. This multi-level system optimizes the performance of a D/A converter with respect to dynamic range, filtering capability, and system complexity. An architecture that uses continuous current calibration in a bipolar (sign/magnitude) operation shows already excellent performance. However, to simplify a system design, examples of non-filtered Dynamic Element Matching converters using a randomization of the elements have been shown. The architectures of the randomizers can be seen as company confidential and are not published. Especially for high-resolution D/A converters, the noise-shaping functions result in a maximum obtainable dynamic range. The dynamic range calculations performed in this chapter are only valid for ideally operating noise-shaping converters. Some care must be used in handling these results. A real-time simulation of the practically designed converter gives the final result of the system. However, the given data give a good idea about the performance capabilities of noise-shaping coders. Furthermore, the stability analysis given proves to be useful for small signal conditions. The extended quantizer model using a phase uncertainty together with the quantizer gain results in a good prediction of the frequencies where the idle pattern will be generated. Furthermore the boundaries of small signal stability and the design of the noise shaping filters is in close approximation with real time simulations. When input signal levels close to maximum are applied, then the non-linearity of the quantizer influences the stability margin that usually results in an instable coder. Limiters are in such a case used to improve stability. This will be discussed in the following chapter. Again, overall system simulations are required to prove the stability of the final system.

Chapter 9

Sigma-delta A/D conversion

9.1 Introduction

In this chapter noise-shaping techniques applied to analog-to-digital converter systems will be described. Noise-shaping is very useful when speed can be exchanged with accuracy. In reference [95] an overview of theoretical and practical aspects of oversampling converters is given. The quantization errors in a noise-shaping system are removed from the signal band of interest. Furthermore, in an analog-to-digital converter system the input noise is filtered out by the input noise-shaping function. As a result, a reduced bandwidth can be used compared to, for example, successive approximation conversion methods. Again, the removed quantization errors appear with larger amplitudes as out-of-band noise in the system. With a digital filter these errors are removed. An increased dynamic range of the system is obtained. An example of such an operation is sigma-delta analog-to-digital conversion using single bit word-lengths [92, 97, 96]. The advantage of a 1-bit converter is the extreme linearity of such a device. A very good differential linearity is obtained with these converters. The most important design criteria will be given. The dynamic range performance is related to the noise-shaping coders described in Chapter 8. At the moment the dynamic range of a system must be enlarged, but the maximum clock rate of the system cannot be increased because of technology limitations, then a multi-bit digital-to-analog converter can be used in the feedback loop. At that moment, however, the linearity of the digital-to-analog converter determines the linearity and the distortion in the system. To overcome this problem *Dynamic Element Matching* or *Continuous Current Calibration* techniques can be used to obtain the extreme linearity of the D/A converter without

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needing extra trimming steps. Examples of this method will be described. In the stability analysis of the sigma-delta converters the root-locus method can be applied. However, for small signal stability the root locus method of 1-bit converters must be extended using the phase uncertainty criterion. With multi-bit systems, the phase uncertainty will be reduced, while furthermore the gain of the A/D and D/A converter loop can better be determined. The root locus method shows in these cases a better result. In most cases an idle pattern close to half the sampling frequency gives the best result. However, idle patterns at other frequencies, depending on the input signal randomly generated, are also allowed. In this case the quantization errors are randomized and appear as noise. Different architectures to implement higher-order sigma-delta converters will be introduced. These converters use special system architectures to avoid stability problems. The MASH structure uses a cascade of second or first order stages to avoid stability problems. A higher order noise-shaping is obtained. A special system that uses a signal-level-dependent filtering order introduces a feed-forward like filter coupling. At low signal levels the highest filter order is used, while with increasing signals the filter order is reduced. The reduced filter order results in a stable system with reduced dynamic range. Usually this reduction in dynamic range at large input signals is not a problem. A large dynamic signal range can be covered. A good optimum between filter order and stable system operation is found. Bandpass noise-shaping filters can be used to convert carrier signals into a stream of digital data. The filter structures can be of the switched capacitor form or continuous time form. The advantage of continuous time is that the sampling frequency can be varied without changing the tuning frequency of the system. However, the tuning frequency of the continuous time filter depends on the absolute accuracy of the elements used. In an IC technology a variation in the order of 10% to 20 % must be expected. This requires an adjustment of the tuning frequency of the filter. Different examples of bandpass modulators will be discussed. At the end of this chapter a first-order implementation to be used in a 5-digit digital voltmeter with automatic offset compensation will be given.

9.2 General form of Sigma-delta A/D converters

In Figure 9.1 a general form of a sigma-delta A/D converter system is shown. The system uses a multi-bit quantizer (analog-to-digital converter) and a multi-bit digital-to-analog converter to reconstruct the analog signal. When multi-bit D/A converters are used to reconstruct the analog signal, then the

linearity of such a converter is important. In case of high-resolution converters an accuracy problem in the D/A system is encountered. To overcome this accuracy problem a 1-bit system is used. In a 1-bit D/A converter the linearity is determined by the accuracy of switching between the reference signals. If a high switching accuracy can be guaranteed, then a very linear system is obtained. In the explanation a 1-bit system will be discussed. From the input signal the output signal of the 1-bit D/A converter is sub-

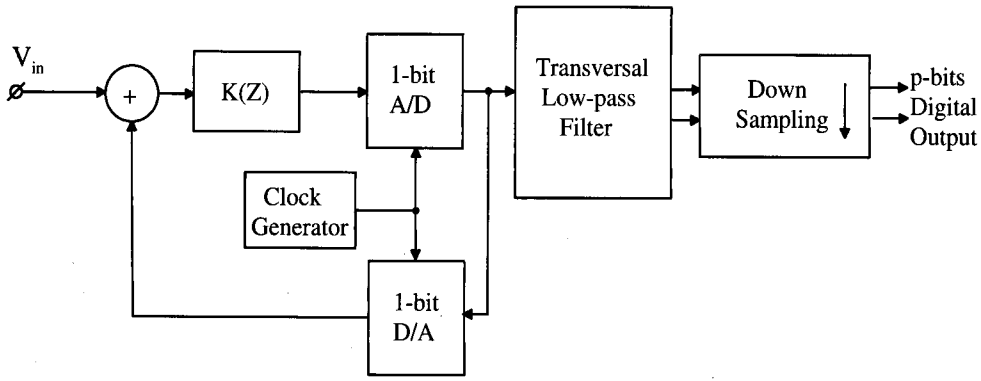

Figure 9.1: Sigma-delta A/D converter system

tracted. The difference of these two signals is filtered by the loop filter, and the output signal of the loop filter is applied to the 1-bit quantizer or A/D converter. The clock frequency of the system is high compared to the maximum analog input frequency while the order of the loop filter determines the dynamic range of the system. Equivalent equations apply for this system as given in the noise-shaping D/A converter chapter. Noise-shaping filters can be re calculated into sigma-delta filters showing nearly identical performance. In this way an identical analysis can be performed. The output of the 1-bit A/D converter is usually applied to a digital low-pass which rejects signals above the signal band of interest. Then sub-sampling or decimation is applied to obtain a multi-bit output code. The whole operation results in a binary-weighted digital output signal that can have a minimum sampling ratio equal to twice the signal bandwidth.

When the loop filter that is applied in this system consists of a continuous-time filter, then the analog signal band is filtered with the same filtering characteristic as is applied for noise-shaping. A cost-effective solution is obtained in this way. In the case of a discrete-time loop filter the anti-alias filtering must be performed before the analog signal enters the A/D

converter. Discrete-time filters are mixing the high frequency input signals with the sampling clock, resulting in aliasing of signals which is not allowed.

The relationship between the sigma-delta modulator and the noise-shaper can be revealed by a transformation method shown in Figure 9.2. The transformation starts with the noise-shaper shown in Figure9.2(a). First the limiter is relocated according to Figure 9.2(b). This relocation is allowed because the output of the quantizer is not influenced by the omission of the limiter in its input. In the second step, shown in Figure 9.2(c), the loop filter is relocated. This operation does not change the output noise spectrum, and the influence on the signal transfer is canceled by an inverse filtering operation performed on the input signal. In the third step the two addition points in the loop are interchanged. The resulting system contains two nested feedback loops. The minor loop contains the noise-shaper loop filter and the limiter whereas the major loop contains the quantizer, the addition function, and the minor loop function as shown in Figure 9.2(d).

When the minor loop filter is considered as $K(z)$ and the limiter function is replaced by one, then the relationship between the noise-shaper filter $J(z)$ shown in Figure 8.4 and $K(z)$ is given by:

$$K(z) = \frac{J(z)}{1 - J(z)}. \tag{9.1}$$

Solving equation 9.1 for $J(z)$ we obtain:

$$J(z) = \frac{K(z)}{1 + K(z)}. \tag{9.2}$$

Equation 9.1 or 9.2 can be used to convert a noise-shaping filter $J(z)$ into a sigma-delta filter $K(z)$ or vice versa. The transformation is valid as long as the limiter is not active.

From Figure 9.1 the general transfer function of a sigma-delta A/D converter is obtained. Here N_q is the quantization error introduced by the analog quantizer.

$$\frac{Y(z)}{X(z)} = \frac{C_g K(z)}{1 + C_g K(z)} + \frac{N_q}{X(z)} \frac{C_g}{1 + C_g K(z)}. \tag{9.3}$$

In this equation C_g is the (non)linear gain of the quantizer. This constant is used for calculation purposes and depends on the signal level and the loop filter characteristic of the system. The root locus method that has been used

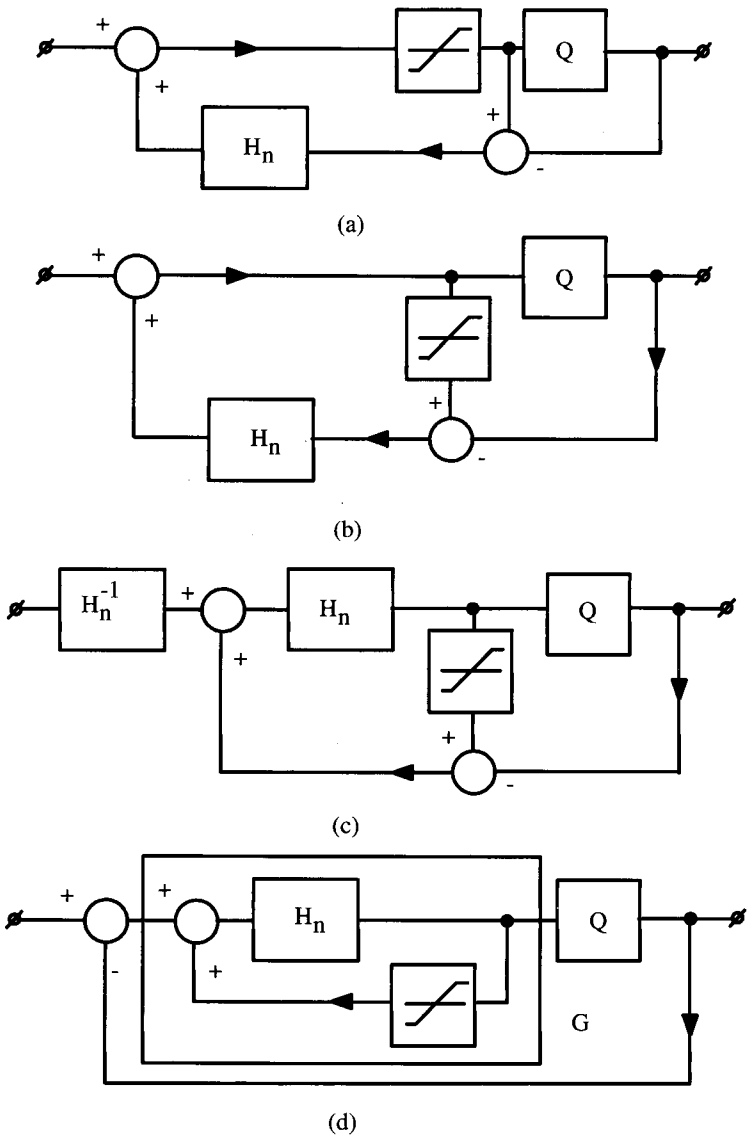

Figure 9.2: Transformation of a noise-shaper into a sigma-delta modulator

for $J(z)$ in case of a noise-shaping coder can be used in the same manner for the sigma-delta converter. The characteristic equation in this system is:

$$1 + C_g K(z) = 0. \tag{9.4}$$

The root locus of $C_g K(z)$ as a function of C_g will be examined. Furthermore, it is possible to transform $K(z)$ into $J(z)$ according to equation 9.2 and then perform the root locus analysis. In practice this means that first- and second-order systems are mostly stable. Higher order systems require special measures for stabilization. The nonlinearity results in a signal dependent stability of the system. This is especially true when higher-order filter structures are used and the input signal increases towards the maximum input signal level.

9.2.1 Dynamic range

Formula 9.3 giving the transfer function of the system can be split-up into a signal transfer part and a noise transfer part what is very useful in case of stability and dynamic range (S/N) analysis.

Then the dynamic range of the system is found from:

$$S/N \approx \frac{X(z)}{N_q} K(z). \tag{9.5}$$

From equation 9.5 it is expected that the signal-to-noise ratio of the system is independent of the input signal amplitude. This is not true because with an increase in input signal the quantizer gain C_g decreases and therefore the efficiency of the filter operation is reduced.

To obtain an estimate of the signal-to-noise ratio as a function of the input signal the term $K(z)$ is analyzed. When the sigma-delta converter operates with a small input signal, the idle pattern is obtained when:

$$1 + C_g K(z) = 0 \tag{9.6}$$

or

$$C_g = \frac{-1}{K(z)}. \tag{9.7}$$

When the input signal increases, the value of C_g will decrease.

Putting $C_g = C_{g0}$ as the gain value for $A_{in} = 0$, with A_{in} is the amplitude of the input signal; then an estimate for C_g as a function of input signal amplitude A_{in} can be found from the describing function of a quantizer:

$$C_g = C_{g0}(1 - \frac{A_{in}}{A_{ref}}). \tag{9.8}$$

Here, A_{ref} is a reference-fitting amplitude.

The input amplitude dependent dynamic range can now be estimated as:

$$S/N \approx \frac{A_{in}}{N_q} K_0(z)(1 - \frac{A_{in}}{A_{ref}}). \tag{9.9}$$

$K_0(z)$ is the noise transfer function of the coder for $A_{in} = 0$.

It must be noted that equation 9.9 is a simplified model of a general decrease in dynamic range observed in these coders.

9.3 General filter architectures

During the design of sigma-delta converters a numerous of noise-shaping filter structures have been used. To obtain an overview of most of the filter structures two generalized schemes will be shown. In Fig. 9.3 a feedback filter architecture is given. In most applications the input coefficients b_2 to

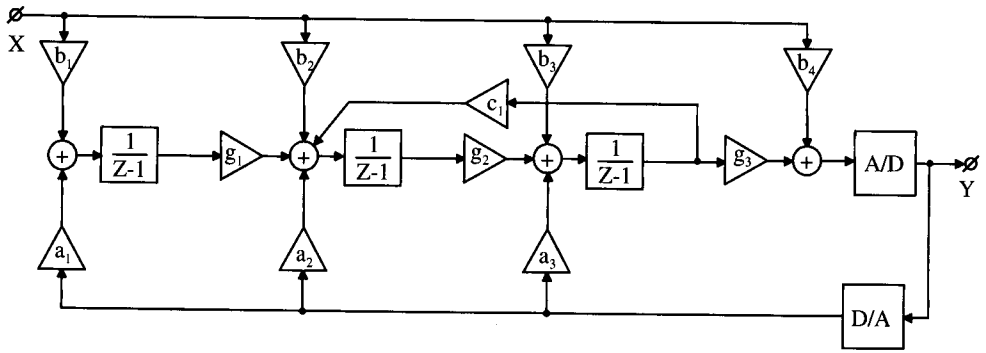

Figure 9.3: Generalized feedback filter architecture

b_n are set at zero, while $b_1 = 1$ to optimize signal-to-noise ratio. In case these coefficients are not zero, then an accuracy problem might be introduced for signals in the passband of the converter. A careful design is needed in that

case.
Coefficients a_1 to a_n in the feedback path of the digital-to-analog converter determine the noise transfer function and are required to obtain a stable operation of the converter. The coefficient c_1 is introduced to obtain an extra zero at a signal frequency in the passband of the converter. In this manner an increase in dynamic range over the passband is obtained. g_1 to g_n determine the gain of the integrator stages. An alternative to this architecture using feed forward coefficients is shown in Fig. 9.4. The feed

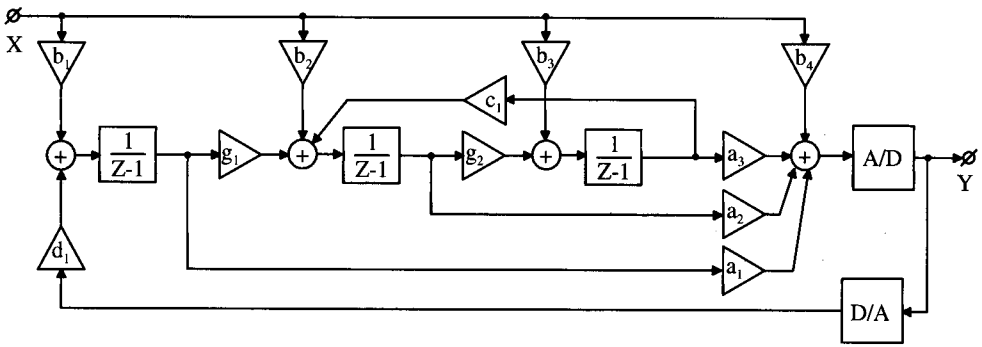

Figure 9.4: Generalized feed forward filter architecture

forward coefficients a_1 to a_n sometimes in combination with limiters in the last integrator stages are used for stability of the converter. At small signals the signal levels in the system must remain small. At the moment a strong increase might occur, then limit cycles are present in the system and these limit cycles can disturb completely the operation of the system. To overcome such a problem a limiter is included. This limiter reduces the gain of the last stage and at the same time the amount of forward integrators in the loop are reduced. This results in an easier to stabilize converter, however, the noise transfer function efficiency is reduced. Mostly this is not a problem. Again the input signals can be applied via a single input terminal with b_1 = 1 and all other b coefficients zero. Such a configuration does not have a passband inaccuracy. At the moment the input signal is applied using the input coefficients b_1 to b_n then a requirement for the passband ripple is introduced. A careful design of the filter function is required and the accuracy of the components used have influence on the passband ripple. These described architectures will appear in different forms in this chapter.

9.3.1 1-bit Sigma-delta signal examples

If no analog input signal is applied to the A/D converter, then an idle pattern consisting of "1" and "0" signals at half the sampling frequency is obtained. The "1"-"0" pattern changes when an analog input signal is applied to the converter. The number of ones or zeros changes in such away that the analog input signal is nearly equal to the average output signal generated by the 1-bit D/A converter. The maximum output signal can be nearly equal to the positive or the negative reference voltage. As long as the switches in the D/A converter show a nearly ideal performance, the linearity of the converter is not determined by the reference voltages, because by changing the one-zero pattern, the output signal of the D/A converter varies according to a straight line between the minus reference voltage and the plus reference voltage.

In Figure 9.5 an example of the output signal of the A/D converter with a sine wave analog input signal is shown. To make the figure understandable the one-zero idle pattern at half the sampling frequency is removed with a simple digital filter. Note that in the top of the sine wave a large amount of "ones" is generated while in the bottom part of the sine wave a large amount of "zeros" is obtained. It must be noted that the large amount of

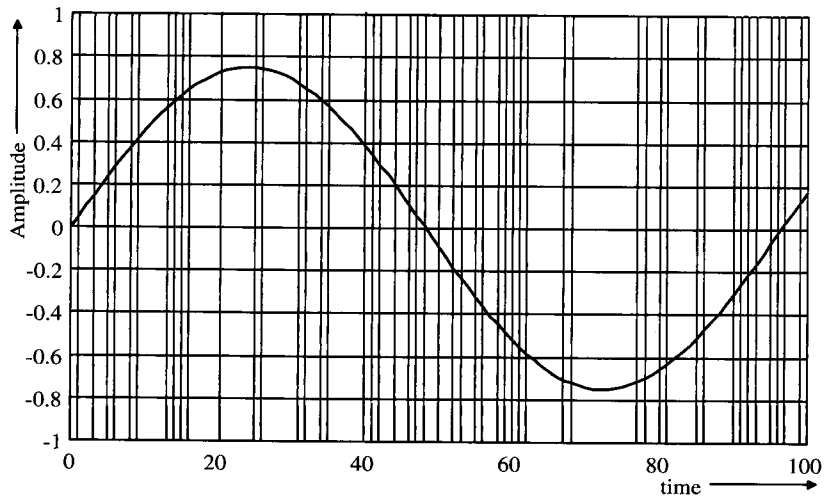

Figure 9.5: 1-bit Sigma-delta A/D converter input and output signals

"ones" or "zeros" can result in non linearity of the converter because two

zeros or two ones in a row do not have a rise and fall time error as is the case with a single one followed by a single zero. This is the case when an idle pattern is generated in the converter. To overcome this problem a very small rise and fall time of the digital-to-analog output pulse is required or the system will use a Return To Zero (RTZ) architecture. In this case every pulse is shaped in the same way by having so called non overlapping pulses. After every "one" a zero will be generated before the "zero" pulse applies the negative reference voltage to the system. In this manner a train of ones is always build up with a train of identical pulses with the return to zero architecture.

9.3.2 Multi-bit Sigma-delta signal examples

At the moment a multi-bit converter is used, then the idle pattern changes. The basic pattern with small input signal must be equal to a LSB pattern of the applied multi-bit converter. In fig. 9.6 the simulation of a 15-level sigma-delta converter with a small input signal is shown. The figure shows

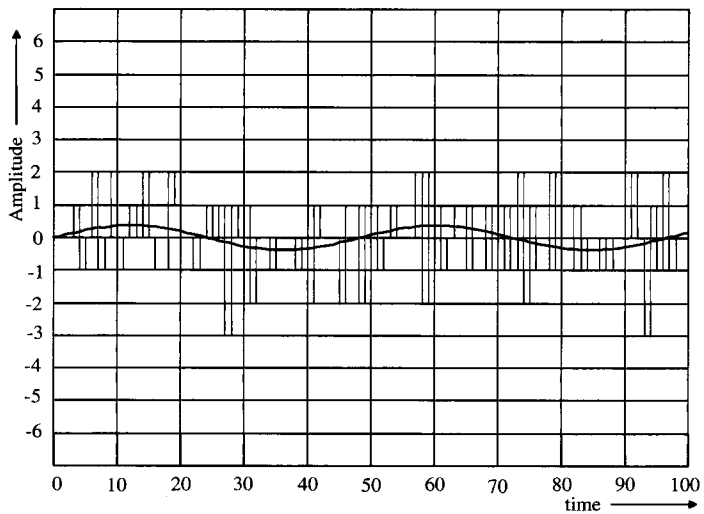

Figure 9.6: Multi-bit sigma-delta A/D converter small input and output signals

that with small input signals not always the smallest idle pattern is obtained. This depends on the stability of the converter. When the stability margin is small, then a larger idle pattern is expected. The result of a larger input

signal applied to the converter is shown in Fig. 9.7. Again this figure shows

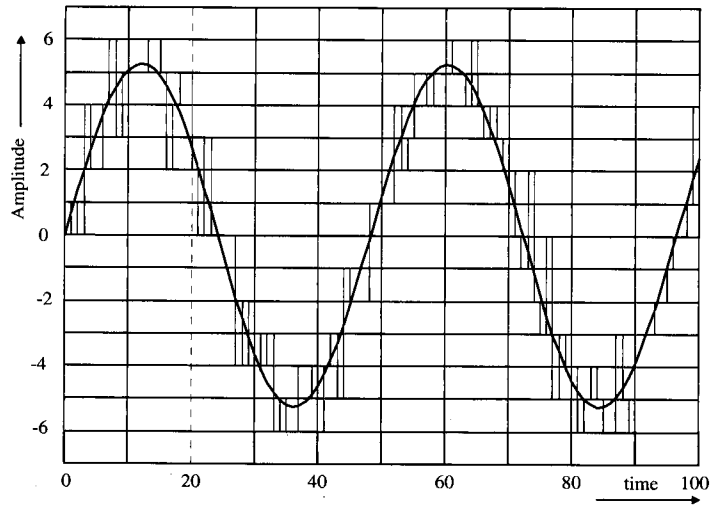

Figure 9.7: Multi-bit sigma-delta A/D converter large input and output signals

that the idle pattern is larger than 1 LSB of the digital-to-analog converter used in the system. In case the stability margin is increased, then the idle pattern becomes more a 1 LSB sized idle pattern.

9.3.3 Return-to-zero D/A pulse

The output pulse train of an oversampled converter is shown in Fig. 9.8. In case a Non Return to Zero code is used as shown in Fig.9.8(a), then in case a double code "1" or a double code "0" is reproduced, the amount of current or charge that is filtered out by the output filter to obtain the analog output signal shows a larger average signal than is required. The rise and/or fall time of the reproduced pulses does not appear in the output signal of a double "1" or a double "0". This results in distortion of the reproduced output signal. The v-shaped curves show this phenomenon. To avoid this distortion a double "1" or double "0" is split up in a train of identical pulses. This is shown in Fig. 9.8(b). This train of pulses uses a return to zero (RTZ) coding by shaping the output pulses in smaller parts starting every time from zero or returning every time to zero after a positive or negative pulse is generated by the D/A converter. Mostly the width of

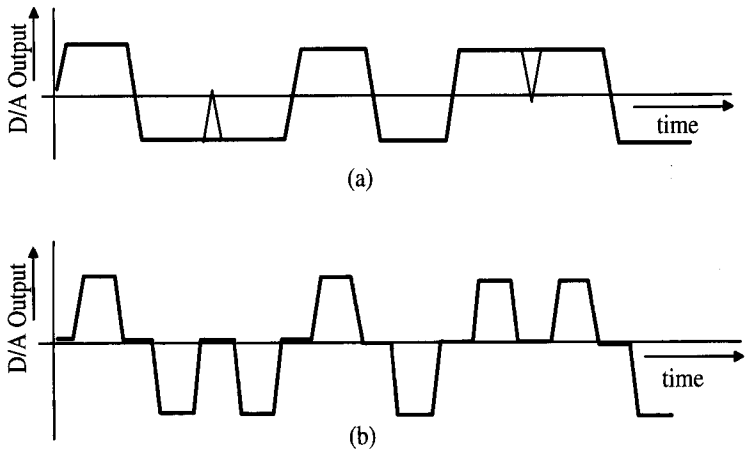

Figure 9.8: D/A output pulses (a) NRZ (b) RTZ

the pulse is reduced to 50 % of the clock time giving 25 % for the rise time and 25 % for the fall time of the pulse as a worst case condition. In this way the distortion of the pulses is avoided.

9.3.4 Continuous time filter first order converter

An A/D converter using a continuous-time first-order filter with a time-discrete 1-bit D/A converter is shown in Figure 9.9. In the D/A converter a switched capacitor circuit is used. This construction is less sensitive to sampling clock uncertainties because a charge "bucket' is transferred to the integrator at every clock moment. The amount of charge is determined by the reference voltage V_{ref} and the capacitors C_1. Furthermore, the switches in the D/A converter are arranged in such a way that only a single reference voltage V_{ref} is needed to transfer a charge or discharge packet into integrator. Furthermore at the moment the charge packet is applied to the integrator only a small delay depending on the speed of the operational amplifier is introduced before the output signal appears at the input of the quantizer. This fast action is important for the idle pattern to be generated at half the sampling frequency. When the phase criterion is used for the stability analysis then the result shown in Fig. 9.10 is found. The phase plot shows that due to the phase uncertainty in the comparator only a small phase margin is left for frequencies from $\frac{f_s}{4}$ to $\frac{f_s}{2}$. Due to this small margin the system will show an idle pattern at $\frac{f_s}{2}$. This will change when extra phase shift is introduced in the loop. Then the pattern will move. Note that in this

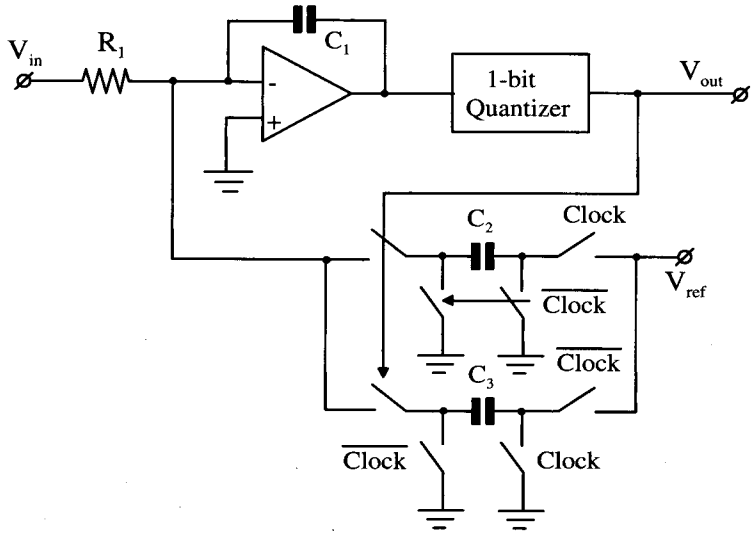

Figure 9.9: A/D converter with continuous-time loop filter

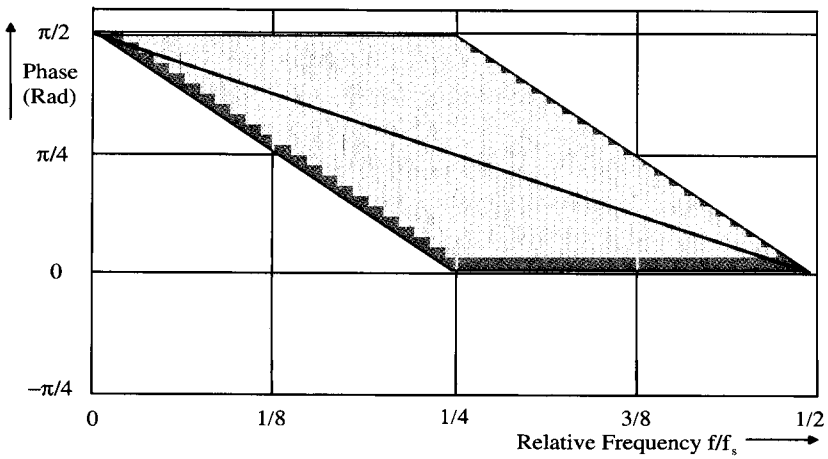

Figure 9.10: First order switched capacitor A/D phase criterion

system the analog input signal is filtered by the integrator as well. Although the filtering attenuation is small it helps to simplify the anti-alias filter at the analog input (this filter is not shown in the figure).

The root locus of the first order switched capacitor A/D converter is shown

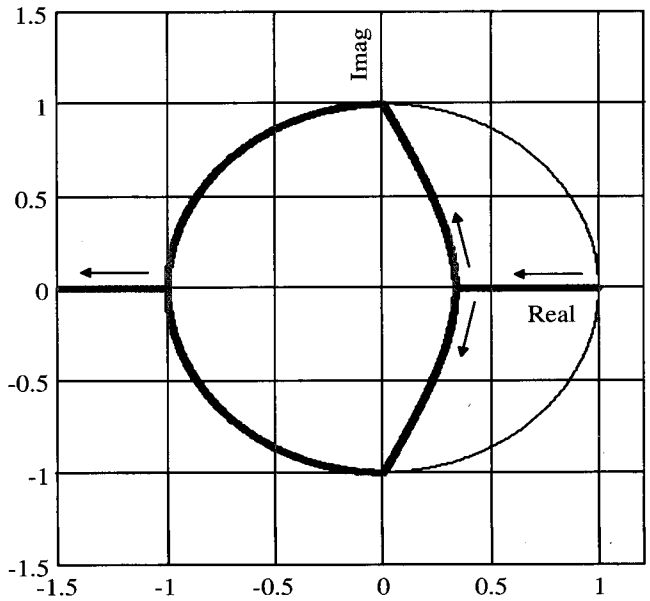

Figure 9.11: First order switched capacitor A/D root locus

in Fig. 9.11. This root locus has been calculated in case the maximum phase uncertainty is present in the one-bit quantizer system. The root locus starts at z =1 and then bends to z = ±j. From ±j the root locus follows the unit circle until z = -1. From z = -1 the root locus follows the negative real axis. At the moment an extra phase shift is present in the system, then the root locus includes ±j and the idle pattern at $\frac{f_s}{4}$ is obtained. The extra phase shift is introduced for example in a continuous time system. This is shown in the next section.

9.3.5 Fully continuous time first order converter

A first order converter using a continuous time digital-to-analog converter is shown in Fig. 9.12. In this system the continuous time digital-to-analog converter applies during the sampling moment the positive or negative reference voltage to resistor R_2. In this way an integration takes place of this signal resulting in a triangular signal across capacitor C_1. When the resistor

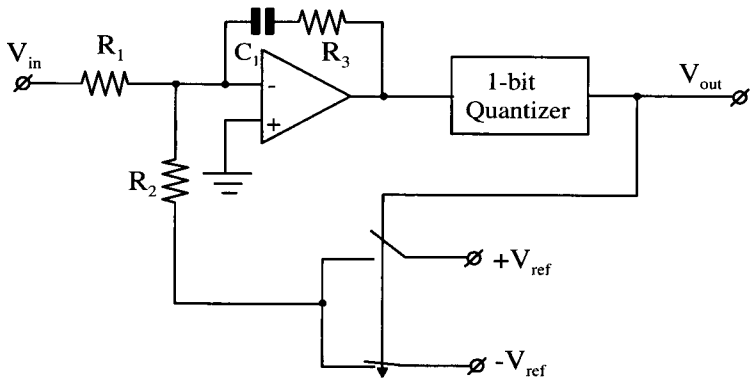

Figure 9.12: Fully continuous time A/D converter

R_3 is not inserted in the system $R_3 = 0$, then the first order hold function of the digital-to-analog converter introduces an extra phase error. The effect of this phase error on the phase stability criterion is shown in Fig. 9.13. As can be seen from this figure, the phase passes before $\frac{f_s}{4}$ the zero line

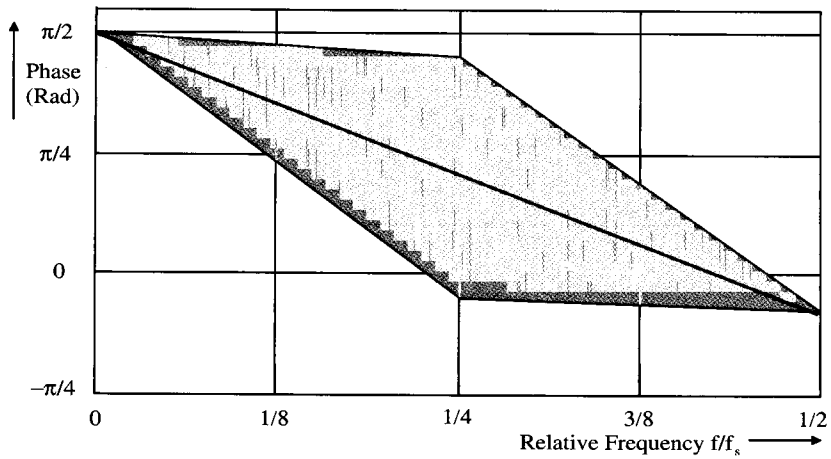

Figure 9.13: First order full continuous time A/D phase criterion

resulting in an idle pattern at $\frac{f_s}{4}$. This results in less oversampling of small signals giving a reduction in dynamic range. This idle pattern at $\frac{f_s}{4}$ can be avoided by introducing an extra zero in the loop filter. This extra zero is obtained via resistor R_3. As a result of this feed forward coupling a small part of the D/A signal is added to the triangular integrated signal. As a

result it can be said that the zero crossing of the signal at the quantizer is earlier obtained. The idle pattern moves to half the sampling frequency.

9.4 Discussion of basic converter architectures

In this section some parameters of basic converters will be discussed. The stability analysis will not be given here. The extended quantizer model can be applied to obtain the root locus of the system. Furthermore the transformation of the noise shaping digital-to-analog converter with the filter function in the feedback into the filter function preceding the comparator stage does not change the stability criterion for converters with filter order starting at order three and above. The same criteria remain valid.

9.4.1 First-order A/D converter

In Figure 9.14 the basic circuit diagram of a first-order analog-to-digital converter is shown. The signal transfer function for this system using C_g as

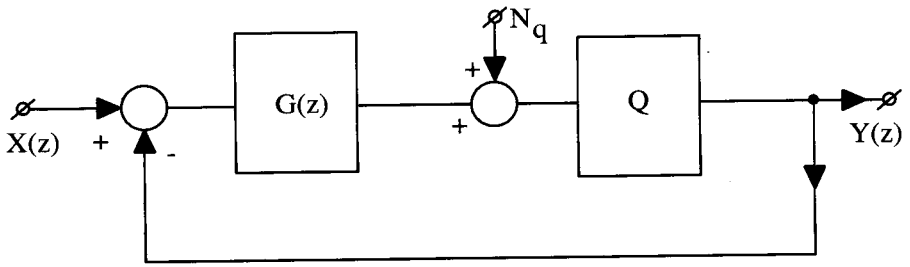

Figure 9.14: First-order A/D converter

the gain of the quantizer becomes:

$$\frac{Y(z)}{X(z)} = \frac{C_g G(z)}{1 + C_g G(z)}. \tag{9.10}$$

The error signal E(z) becomes:

$$E(z) = N_q \frac{C_g}{1 + C_g G(z)}. \tag{9.11}$$

With

$$G(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{9.12}$$

we obtain:

$$\frac{Y(z)}{X(z)} = \frac{C_g z^{-1}}{1 + (C_g - 1)z^{-1}} \tag{9.13}$$

or

$$\frac{Y(z)}{X(z)} = \frac{C_g}{z - (1 - C_g)}. \tag{9.14}$$

The error of the system can be calculated by substituting G(z) into equation 9.11. The result is:

$$E(z) = N_q \frac{C_g(1 - z^{-1})}{1 + (C_g - 1)z^{-1}} = N_q \frac{C_g(z - 1)}{z - (1 - C_g)}. \tag{9.15}$$

With z $\approx$ 1, what corresponds with $f_{signal} \approx 0$, the error signal E(z) from equation 9.15 is nearly zero. This corresponds to the expected noise-shaping operation of the system.

The stability is analyzed by means of the root locus method using C_g as the parameter. In the first order system we have to analyze:

$$C_g G(z) = \frac{\lambda e^{j\alpha\Delta\phi_{max(\theta)}} z^{-1}}{1 - z^{-1}} = -1. \tag{9.16}$$

Here the quantizer with gain C_g is replaced by:

$$C_g = \lambda e^{j\alpha\Delta\phi_{max(\theta)}} \tag{9.17}$$

as has been discussed in chapter 8. The root locus starts at z =1 and ends at $z = -\infty$.

9.4.2 Second-order A/D converter

In Figure 9.15 a second-order sigma-delta modulator is shown [90]. As the figure shows, the reproduced analog signal is subtracted after each integrator. The coefficient a_0 that determines the amount of analog signal to be subtracted from the output signal of the first integrator determines the total loop filter characteristic. The signal transfer function of the second-order coder becomes:

$$\frac{Y(z)}{X(z)} = \frac{C_g G(z) H(z)}{1 + C_g H(z)[a_0 + G(z)]}. \tag{9.18}$$

The error transfer function becomes:

$$E(z) = N_q \frac{C_g}{1 + C_g H(z)[a_0 + G(z)]}. \tag{9.19}$$

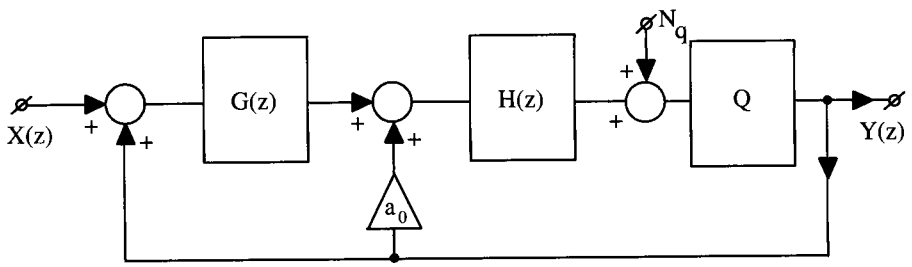

Figure 9.15: Second-order sigma-delta modulator

The coefficient a_0 can be chosen in such a way that an optimum performance of the converter is obtained.

Substituting for G(z) = H(z) = $\frac{z^{-1}}{1-z^{-1}}$ and simplifying this function, we obtain for:

$$K(z) = H(z)(a_0 + G(z)), \tag{9.20}$$

with $K(z)$ is the equivalent transfer function as shown in the general sigma-delta modulator Figure 9.1,

$$K(z) = \frac{z^{-1}(a_0 - z^{-1}(a_0 - 1))}{(1 - z^{-1})^2}. \tag{9.21}$$

Now $K(z)$ can be converted into an equivalent noise-shaper function $J(z)$ resulting in:

$$J(z) = \frac{z^{-1}(a_0 - (a_0 - 1)z^{-1})}{1 + (a_0 - 2)z^{-1} - (a_0 - 2)z^{-2}}. \tag{9.22}$$

By making $a_0 = 2$, equation 9.22 reduces into:

$$J(z) = z^{-1}(2 - z^{-1}), \tag{9.23}$$

which is equivalent to the second-order noise-shaper loop filter shown in Figure 8.20. $a_0 = 2$ is a good choice for a second-order system.

Stability analysis is performed on $C_g K(z)$. With $a_0 = 2$ we obtain:

$$C_g K(z) = \lambda e^{j\alpha\Delta\phi_{max(\theta)}} \frac{2z - 1}{(z - 1)^2} = -1. \tag{9.24}$$

The root locus starts at the double pole $z = 1$ and ends at $z = 0.5$ and $z = -\infty$ respectively.

9.4.3 Third-order A/D converter

A third-order sigma-delta converter is shown in Figure 9.16. Again after each integrator the reconstructed analog value is subtracted from the quantized signal. Putting C_g for the quantizer gain again and having coefficients a_0, a_1, and a_2, the transfer function of the system can be calculated. The coefficient a_0 is added to obtain an extra variable in converting the sigma-delta coder into a noise-shaping coder.

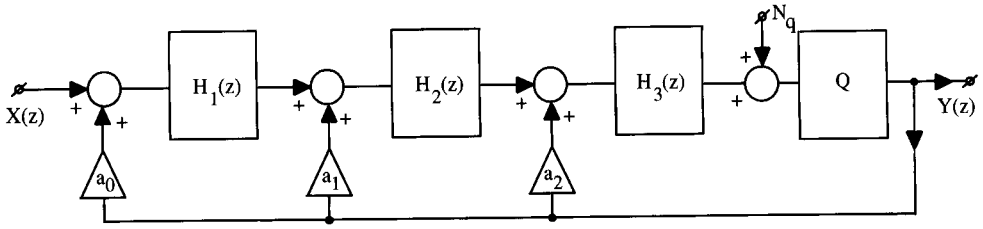

Figure 9.16: Third-order noise-shaping coder

$$\frac{Y}{X} = \frac{C_g H_1(z) H_2(z) H_3(z)}{1 + C_g H_3(z)[a_2 + H_2(z)(a_1 + a_0 H_1(z))]}. \tag{9.25}$$

By inserting $H_1(z) = H_2(z) = H_3(z) = \frac{z^{-1}}{1-z^{-1}}$, the equivalent transfer function $K(z)$ becomes:

$$K(z) = \frac{z^{-1}}{(1 - z^{-1})^3}(a_2 + (a_1 - 2a_2)z^{-1} + (a_2 - a_1 + a_0)z^{-2}) \tag{9.26}$$

or

$$K(z) = \frac{(a_0 - a_1 + a_2) + (a_1 - 2a_2)z + a_2 z^2}{(z - 1)^3}. \tag{9.27}$$

By converting $K(z)$ into the noise-shaping filter $J(z)$, we obtain:

$$J(z) = \frac{(a_0 - a_1 + a_2) + (a_1 - 2a_2)z + a_2 z^2}{(a_0 - a_1 + a_2 - 1) + (a_1 - 2a_2 + 3)z + (a_2 - 3)z^2 + z^3}. \tag{9.28}$$

A filter function already used as a third-order noise-shaper in the previous Chapter is:

$$J(z) = 1 - \left(\frac{z - 1}{z - a}\right)^3 \tag{9.29}$$

or

$$J(z) = \frac{(1 - a^3) - 3z(1 - a^2) + 3z^2(1 - a)}{(z - a)^3}. \tag{9.30}$$

The coefficients of equations 9.28 and 9.30 must be equal we obtain:

$$a_2 = 3(1-a) \tag{9.31}$$
$$a_1 = 3a(1-a)^2 \tag{9.32}$$
$$a_0 = (1-a)^3. \tag{9.33}$$

By inserting $a = 0.5$ as a good choice for an optimum third-order performance, we obtain:

$$a_2 = 1.500 \tag{9.34}$$
$$a_1 = 0.375 \tag{9.35}$$
$$a_0 = 0.125. \tag{9.36}$$

The value of coefficient a_0 can be made equal to 1 using equation 9.27 and modifying the gain C_g; thus we obtain:

$$a_{20} = \frac{3}{(1-a)^2} \tag{9.37}$$
$$a_{10} = \frac{3a}{(1-a)} \tag{9.38}$$
$$C_{g0} = a_0 C_g. \tag{9.39}$$

Basically the small gain change is not a problem, and the quantizer does not show a change in performance. 1-bit sigma-delta converters are not dependent on the quantizer gain.

The stability of the system is found from:

$$C_g K(z) = \lambda e^{j\alpha\Delta\phi_{max(\theta)}} \frac{(a_0 - a_1 + a_2) + (a_1 - 2a_2)z + a_2 z^2}{(z-1)^3} = -1. \tag{9.40}$$

The root locus starts at $z = 1$ with a triple pole and ends at:

$$z_{1,2} = (1 - \frac{a_1}{2a_2}) \pm \sqrt{(\frac{a_1}{2a_2} - 1)^2 - (\frac{a_0 - a_1}{a_2} + 1)} \tag{9.41}$$

and $z_3 = -\infty$.

From the third-order noise-shaper implementation it was shown that the coefficients as used in equation 9.40 results in a maximum dynamic range.

9.5 Multi-stage sigma-delta converter (MASH)

To avoid the stability problem of, for example, a third-order noise-shaping coder, a so-called "MASH" converter system consisting of three cascaded first order coders is used. In Figure 9.17 this system is shown [98]. From the

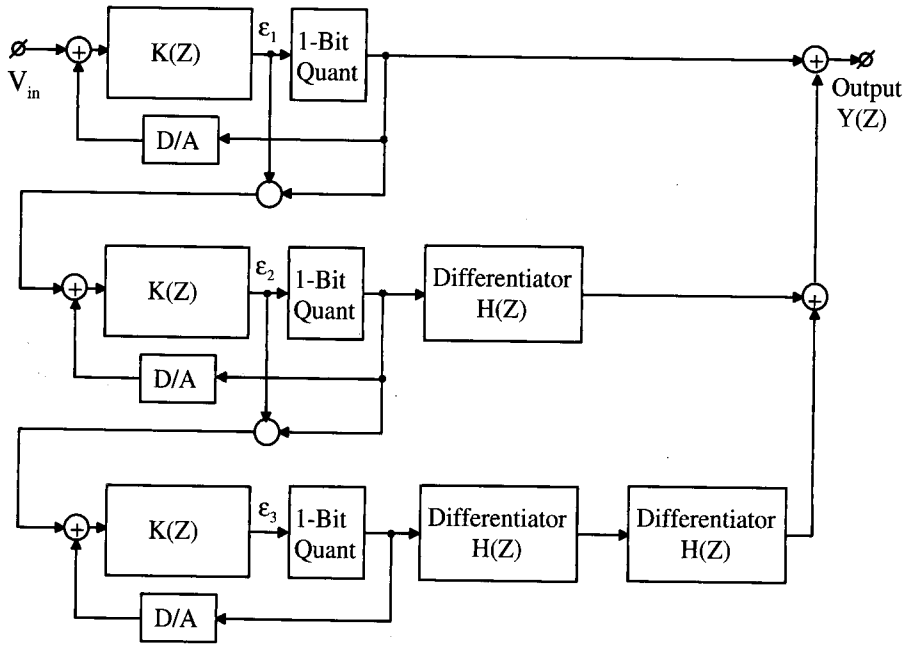

Figure 9.17: MASH noise-shaping coder system [98]

figure it is seen that the error signal ϵ_1 of the first first-order noise-shaping coder is applied to the second first-order coder. This second-order coder quantizes the error signal and after differentiation of this second output signal the total output signal is corrected. Then the error signal ϵ_2 of the second coder is applied to the third coder which quantizes this signal again. After a two times differentiation, the signal of the third quantizer is added to the output signal again. As a result of this operation, the order of the noise-shaping coder is increased from a first order of the first encoder up to a third order. This increase in noise-shaping filtering performance is obtained without introducing a stability problem because every individual stage of the encoder is a first-order noise-shaper. The transfer function of this coder is given by:

$$K(z) = C_g(\frac{z^{-1}}{1-z^{-1}})^3. \tag{9.42}$$

The transfer function of the integrators in the loop including the z^{-1} delay of the quantizer is given by:

$$I(z) = \frac{z^{-1}}{1 - z^{-1}}. \tag{9.43}$$

A problem in this system is the accuracy with which the output signal ϵ_1 is encoded with respect to the full resolution of the total system. The accuracy of the 1-bit digital-to-analog converter recovering the analog output signal of the first encoder influences the accuracy of signal ϵ_1 and so does the subtracter determining the input signal to the second encoder. In the second encoder an accuracy problem is again found but less stringent requirements are needed here. As a result of this subtraction accuracy the total reduction in quantization is reduced. In literature this effect is called "quantization noise leakage". This accuracy problem is more sever in case more than three stages are cascaded. After the first stage a very high gain and subtraction accuracy is required to obtain a sufficient quantization noise cancelation and make additional stages effective in the total quantization noise contribution. At the output of the MASH converter a multi-bit digital word is found due to the addition of the output signals of the successive 1-bit quantizers. By using an extra noise-shaper, this multi-bit output word can be reduced into a 1-bit largely oversampled output signal.

In reference [91] an example of MASH structure using a 1-bit "coarse" quantizer and a $N = 3$-bit "fine" quantizer is presented. The block diagram of this converter system is shown in Figure 9.18. In the first "coarse" quantizer a 1-bit system approach is used because of the very high accuracy that can be obtained in a 1-bit system without needing trimming. The second "fine" quantizer uses a multi-bit quantizer. Because the multi-bit operates on the "error" signal from the coarse quantizer, the accuracy requirements are relaxed. The advantage of the multi-bit "fine" quantizer is the increase in dynamic range compared to a 1-bit implementation and the reduction in out-of-band noise.

9.6 Quantizer overload avoidance

In converters with noise shaping filters starting with a second order and above, problems with quantizer overload can become a problem. Overloading a quantizer results in a strong increase in distortion and might result in instability of the converter. To overcome this problem different techniques can be used.

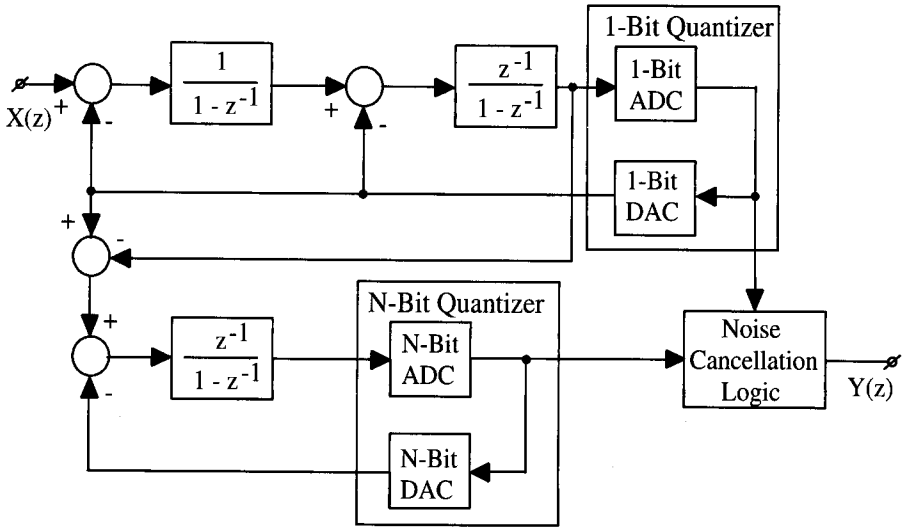

Figure 9.18: Block diagram of cascaded multi-bit sigma-delta modulator [91]

9.6.1 Interstage gain scaling in cascaded converters

The interstage gain between converters in a cascaded architecture can avoid quantizer overload [172, 170]. In Fig. 9.19 an example of a 2-1 (second order first stage, first order second stage) cascaded converter is shown. In this architecture 1-bit quantizers are used. In this case the output of the second order noise shaping filter can become large with large input signals. Then the error signal applied to the second stage must be reduced in amplitude to avoid overload of the second first order quantizer. This means that $Hc_1 < 1$. A good choice is $\frac{1}{8} < Hc_1 < \frac{1}{2}$. However, the reduction in error signal applied to the second noise shaper results in a reduction in overall dynamic range of the converter. As an example in this case with $Hc_1 = \frac{1}{8}$ the total reduction in quantization error is about 24 dB. Full scale input signal increases in this case from -6 dB to -1 dB. The attenuator is an analog attenuator in an analog-to-digital converter and therefore this attenuation shows a limited accuracy resulting in quantization error leakage. In the digital part $1/Hc_1$ is a shift with 1 to three bits and this does not show an accuracy problem. At the moment multi-bit quantizers are used, then the error signal is reduced due to the multi-bit quantization. In an ideal case with a 4-bit quantizer the error signal will be reduced to the 1 LSB of the multi-bit quantizer. However, mostly a multi-bit quantizer concerning stability is designed to have a couple of LSB's idle pattern and quantization error. Therefore the

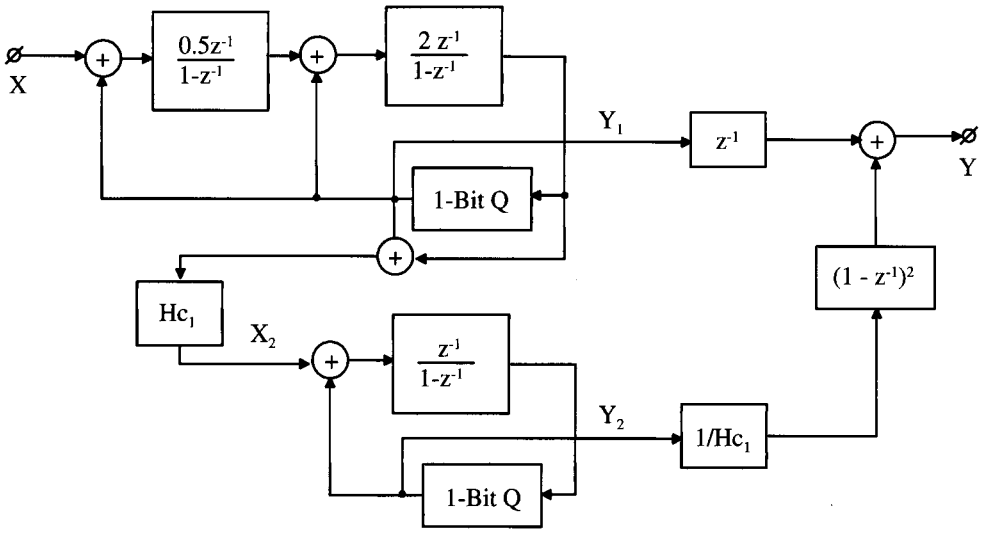

Figure 9.19: Interstage gain scaling in a 2-1 cascaded converter [172, 170]

error signal increases. This means that with a 4-bit quantizer, the error signal could be about 3 to 4 LSB's. In this case an interstage gain between 2 to 4 can be applied for Hc_1 resulting in an improved converter.

9.6.2 Local feedback system across individual integrators

In higher order converters the output signal of the individual integrators used in the noise shaping filter can be controlled using local feedback. This is shown in fig. 9.20. The local feedback using 3-level quantizers avoids growth of integrator output signals. Via coefficients J_1 to J_n this output signal control is applied. At the same time coefficients H_1 to H_n cancel the signals introduced by these quantizers at the output signal combiner. This is identical to the noise cancelation circuits in cascaded architectures.

9.6.3 Gain scaling and local feedback in cascaded converters

A combination of gain scaling and local feedback in a cascaded converter to avoid overloading of the quantizers is shown in Fig. 9.21 [162]. In this 2-2 cascaded system local feedback is applied in the second integrator of the first quantizer. This feedback limits the input signal to this second integrator preventing it from overloading. The accuracy in this system introduces quantization noise leakage limiting the total overall dynamic range. The

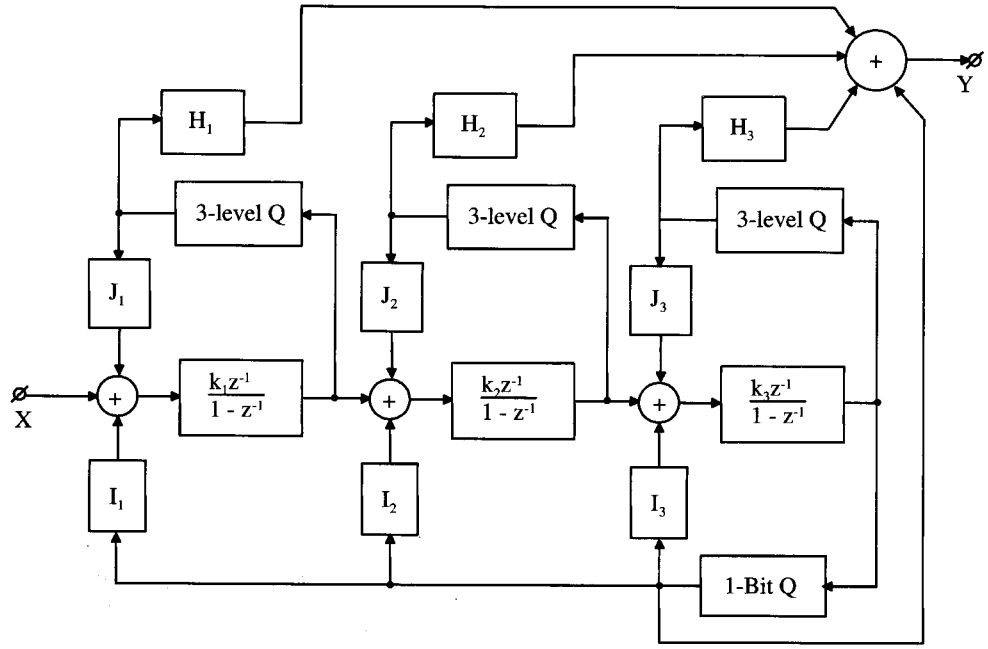

Figure 9.20: Local feedback to avoid quantizer overload

interstage gain Hc_1 can be applied to increase the full scale range and avoid second quantizer overload. However, this is less critical due to the local feedback stage.

9.7 Converter input circuitry

In high resolution noise shaping analog-to-digital converters the input switched capacitor circuits are very important. These circuits determine distortion and dynamic range. The standard solution is shown in Fig. 9.22. The reference charge is continuously applied to the reference capacitors C_{ref} by closing switches ϕ_1 and ϕ_{1D}. After opening these switches the switches ϕ_{2D} are closed and depending on the quantizer data switches Y_1 or $\overline{Y_1}$ are closed to apply the charge to the integrator capacitors C_j. The cross coupling of the switches performs the addition or subtraction of the reference charge from the charge in the integrator capacitors C_j. Switches ϕ_2 perform this final charge transfer. During identical clock phases the input signal is applied to the sampling capacitors C_s and then applied to the integrator capacitors C_j. The value of the capacitors is important because they determine the

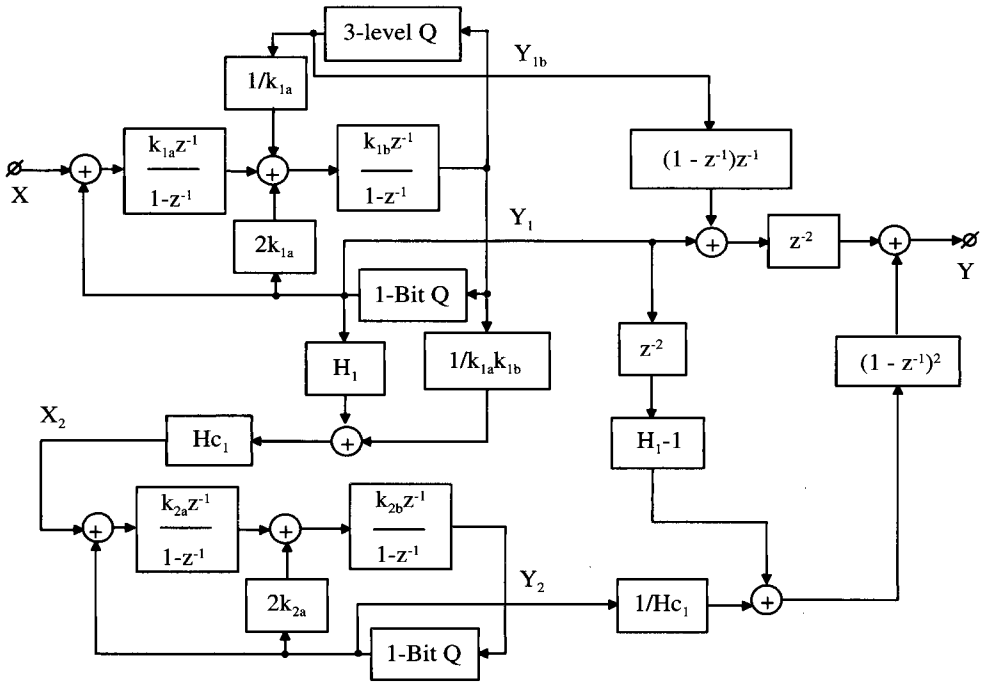

Figure 9.21: Combined gain scaling and local feedback avoidance [162]

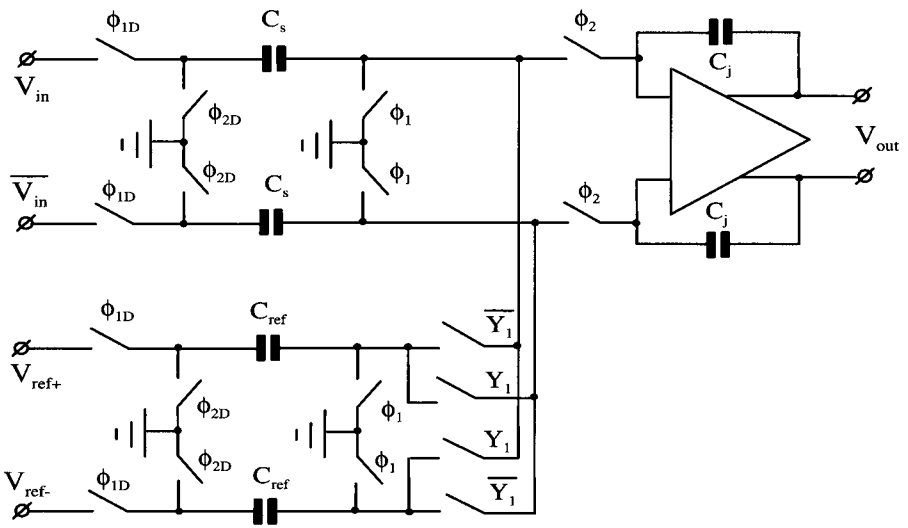

Figure 9.22: Standard switched capacitor input circuit [162]

noise level. The maximum signal to $\frac{kT}{C}$ noise determines the dynamic range of the system. This might result in large input capacitors.

9.7.1 Cross-coupled input sampling

A system that increases the input signal by double sampling is shown in Fig. 9.23. In this system the input signal will double due to the double

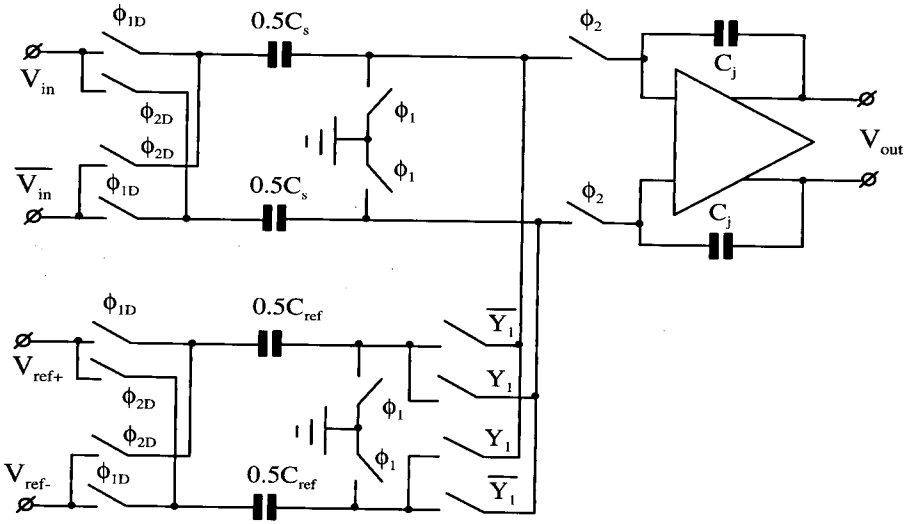

Figure 9.23: Cross-coupled double input sampling [162]

sampling operation. As a result the input capacitors can be reduced as shown. The double sampling is obtained in the following way. First switches ϕ_1 and ϕ_{1D} are closed to sample the input signal on the input capacitors $0.5C_s$. Then these switches are opened and switches ϕ_2 and ϕ_{2D} are closed. A second sampling takes place and at the same time the charge from the previous sample moment is added. This doubles the input signal amplitude on the integrator capacitors C_j. Furthermore the double sampling subtracts common mode voltages resulting in a certain common mode rejection of this input circuit. When the capacitors are halved with respect to the previous circuit, then the noise increases with 3 dB. However, the signal has been doubled resulting in an overall increase in dynamic range with 3 dB. The reference sources are loaded with the reference capacitors $0.5C_{ref}$ resulting in a constant load.

9.7.2 Clock timing scheme

The timing diagram of the clock signals used in these circuits is shown in Fig. 9.24. Bottom plate sampling is used to avoid inaccurate input signal

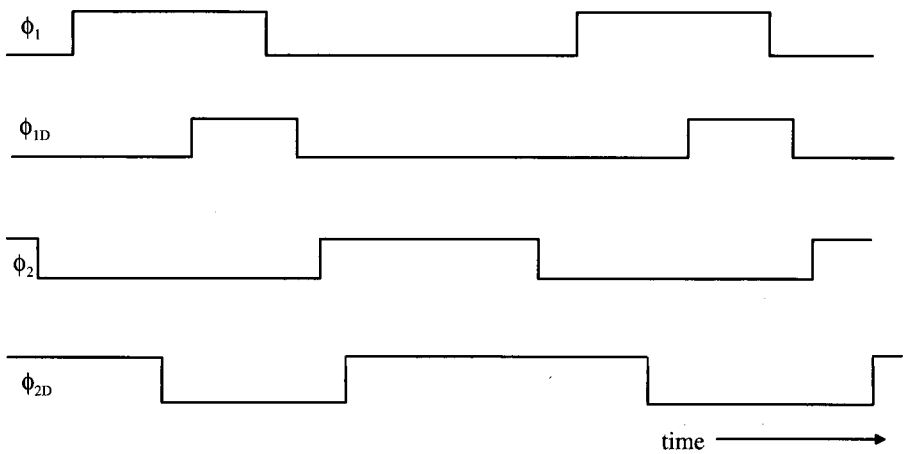

Figure 9.24: Timing diagram of clock signals

sampling.

9.7.3 Shared capacitor input circuit

An input circuit that uses a shared input sampling capacitor is shown in Fig. 9.25. The input signal is sampled on capacitors C_s when switches ϕ_1 and ϕ_{1D} are closed. Then depending on the data of the quantizer the positive or the negative reference voltage is connected to the sampling capacitors performing the addition or subtraction of the reference signal. This construction is not suitable for single bit converters, but can be used in intermediate stages of a converter and multi-bit converters. The loading of the reference source is influenced by the pre-charge of the capacitors and therefore the impedance of the reference source must be very low. Furthermore the clock scheme from Fig. 9.24 avoids a large amount of data dependent reference source loading. A small amount of modulation with the input signal of the reference source introduces second harmonic distortion.

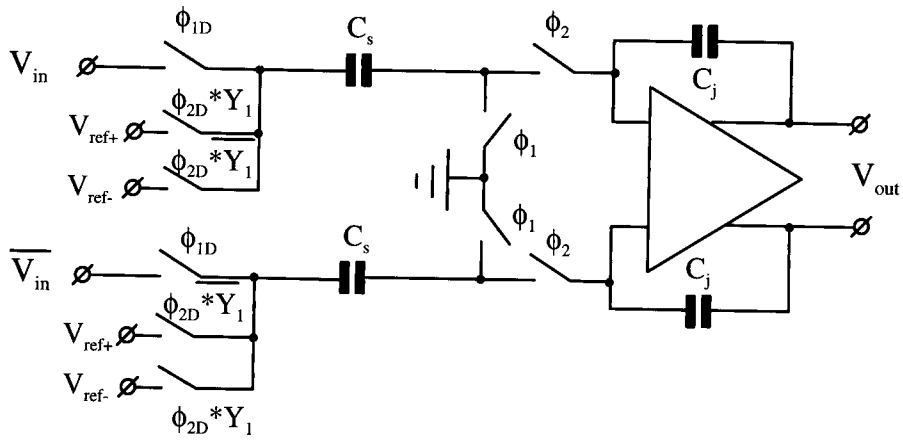

Figure 9.25: Shared input sampling capacitor circuit

9.8 Practical 16-bit cascaded converter

The architecture of a 16-bit 2.5 MHz cascaded analog-to-digital converter is shown in fig. 9.26 [163]. In this architecture a 2-1-1 cascaded structure is used. The quantizers have a 4-bit resolution. Dynamic Element Matching is used in the quantizers to obtain the very high linearity required for the 16-bit resolution. Furthermore interstage gains of 4 times and 8 times are used to optimize the noise shaping performance of the system. At the same time the limited gain (4 times and 8 times in stead of 16 times) avoids overloading of the succeeding quantizer stages.

9.8.1 Converter specifications

The following converter specifications have been obtained. This converter shows a very good performance over a signal bandwidth of 1.25 MHz with a low oversampling ratio.

9.9 Feed-forward A/D converter system

A system that combines the higher-order filter function for small signals with a gliding filter order function depending on the signal amplitude tending to reduce into a first-order for large signals is shown in Figure 9.27 [164, 165, 166]. Basically the system consists of a cascade of integrator sections. A feed-forward technique using coefficients A_N with N, depending on the

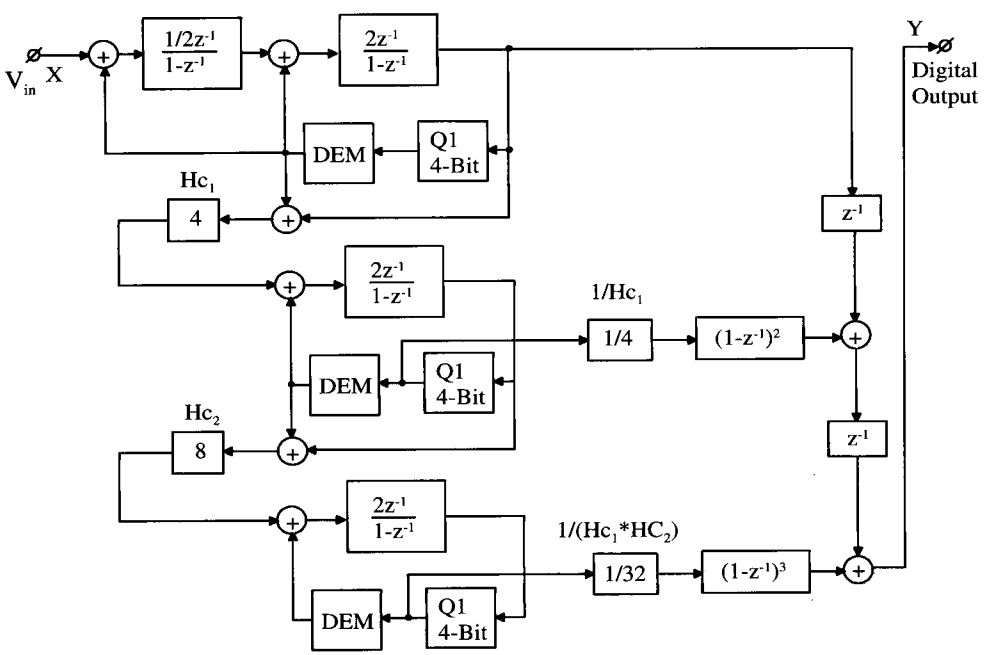

Figure 9.26: 16-Bit cascaded A/D converter architecture [163]

Input voltage	$\pm$ 2 V_{pp} differential
Resolution	16 Bits
Output data rate	2.5 MHz
Sample frequency	20 MHz
SNR (1.25 MHz BW)	90 dB (SD = 0.3 dB)
THD (-0.1 dBFS, 100 kHz)	-98 dB (SD = 1.2 dB)
SFDR (-0.1 dBFS, 100 kHz)	102 dB
SFDR (-10 dBFS, 100 kHz)	110 dB
IM3 (975 kHz/1 MHz, -6.5 dBFS	-92 dB
Power supplies	5 V analog, 3 V digital
Power dissipation	270 mW (105 mW DSM)
Technology	0.5 μm DPTM CMOS
Chip size	4.6 x 5.4 mm^2

Table 9.1: 16-Bit converter data [163]

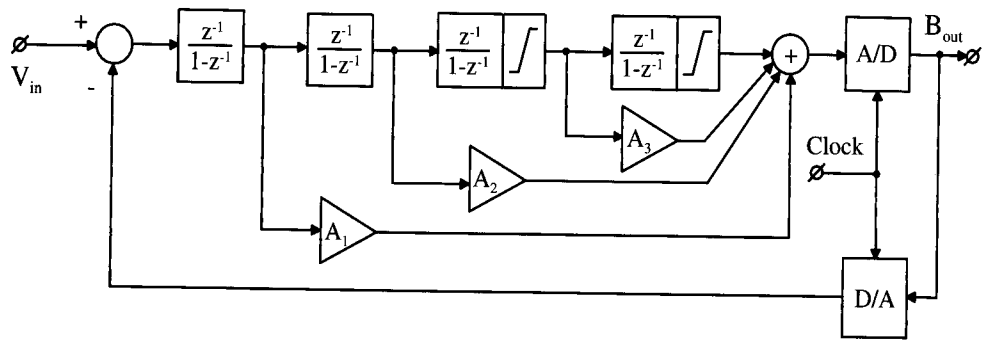

Figure 9.27: Feed-forward A/D converter system [164, 165, 166]

number of stages, feeds signals directly to the comparator stage (1-bit A/D). When the input signal increases, then the signals are amplified so much that a clamping occurs. In the two last integrators a predetermined clamping of the signal is included. At that moment, the feed-forward operation takes over and a stable system is obtained. When the transfer function of an integrator is determined by:

$$I(z) = \frac{z^{-1}}{1 - z^{-1}}, \tag{9.44}$$

then the transfer function of a third-order filter implementation is given by:

$$K(z) = \frac{z^{-1}}{(1 - z^{-1})^3} A_1 (1 + \frac{A_2 - 2A_1}{A_1} z^{-1} + \frac{A_3 + A_1 - A_2}{A_1} z^{-2}). \tag{9.45}$$

In this equation the coefficients $A_{(n)}$ determine the weighting of the output signals of the integrators. Expressions for the coefficients $A_{(n)}$ can be obtained starting with a third-order noise-shaping filter:

$$1 - J(z) = \left(\frac{z - 1}{z - a}\right)^3 \tag{9.46}$$

Converting the noise-shaping filter $J(z)$ into the sigma-delta filter $K(z)$ results in expressions for the coefficients $A_{(n)}$, we obtain:

$$A_1 = 3(1 - a) \tag{9.47}$$
$$A_2 = 3(1 - a)^2 \tag{9.48}$$
$$A_3 = (1 - a)^3. \tag{9.49}$$

With $a = 0.5$ equation 9.45 becomes:

$$K(z) = \frac{z^{-1}}{(1-z^{-1})^3} 1.5(1 - 1.5z^{-1} + \frac{7}{12}z^{-2}). \tag{9.50}$$

giving a stable coder which already was shown in a previous analysis.

Basically the gain A_1 can be incorporated into the quantizer gain in case of a 1-bit system. It is clear that other choices for filter coefficients are possible to obtain the required performance of the converter and give a sufficient stability. At this moment the special architecture of this coder will become active.

In practical solutions a filter order between three and five seems to be a good optimum. Due to the higher order filtering operation, a better randomizing of the quantization errors occurs at small input signals. Therefore, the small signal performance is extremely good, while with increasing signals the filter order decreases until in extreme circumstances the final first-order stage is reached. The outputs of the integrators that are closest to the quantizer have a predetermined maximum signal value before limiting occurs. During limiting no signals are transferred, and therefore this part of the filter function is eliminated.
A more detailed implementation of a feed forward converter is shown in Fig. 9.28. This system shows a continuous time filtering operation including the digital-to-analog converter. In the integrators g_m stages are used. The feed forward coefficients A_1 to A_5 determine the noise transfer function and the stability for small signals and large signals. Two extra feedback loops are added in the converter using stages B_1 and B_2. These stages increase the dynamic range of the system over a larger signal bandwidth by including two extra zero's in the noise transfer function. Resistive coupling at the input is used to get the signal and the D/A signals into the system.

9.9.1 Continuous time input circuit

The circuit diagram of the continuous time input circuit is shown in fig. 9.29. The input amplifier consisting of M_1, M_2 uses a cascode stage M_3, M_4 to increase the output impedance. This input stage is loaded with a cascoded current source consisting of transistors M_8 to M_{11}. The bias current is adjusted by controlling the gate source voltage of M_{10} and M_{11}. The tail current of the input pair consists of a controlled coupled pair M_6, M_7 biased by the output signal of the system. The gates of these devices are connected to the output terminals of the amplifier. With relative small differential

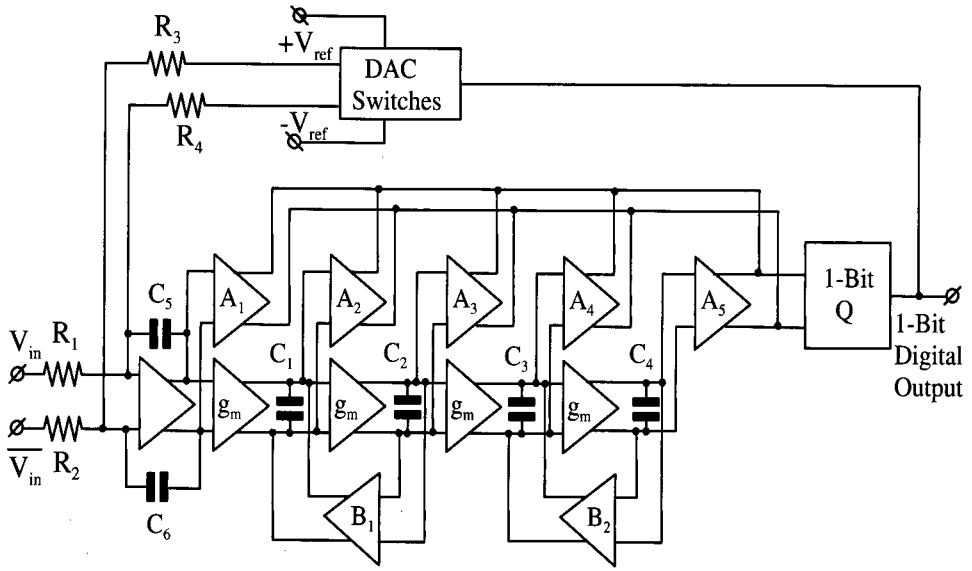

Figure 9.28: Feed forward architecture using gm stages [164, 165, 166]

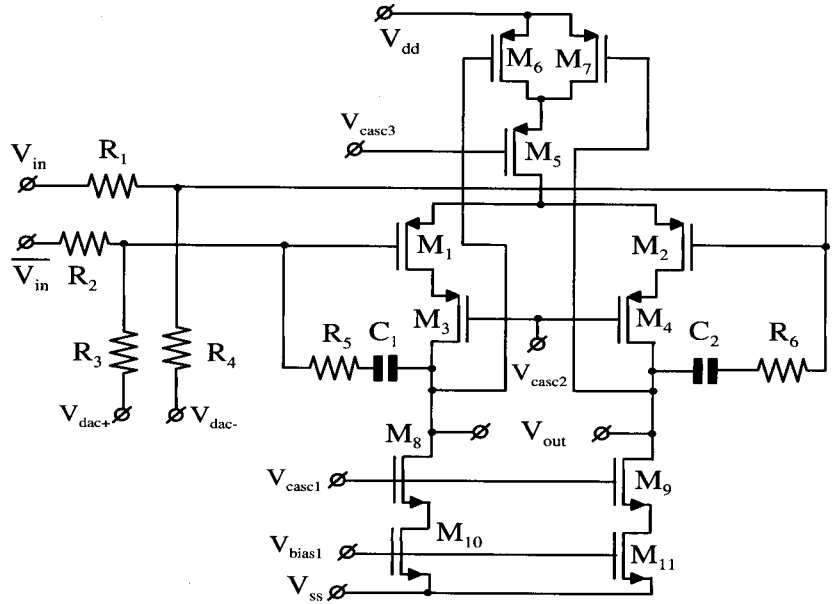

Figure 9.29: Continuous time input circuit [164]

output signals the total sum of the drain currents of M_6 plus M_7 flowing through cascode transistor M_5 remains constant. In this way the tail current is adapted to the current applied by the drain current sources. In case a too large output signal is generated, then or M_6 or M_7 obtains a connection from drain to gate and form in that case a low MOS diode impedance loading the system. This might help to prevent large overload signals. The input signal is applied via resistors R_1, R_2 and the DAC output signal is subtracted via resistors R_3, R_4. The feedback elements C_1 and C_2 are the first integrator in the system. Resistors R_5 and R_6 are used to obtain an extra zero in the filter loop and can compensate for the extra delay introduced by the continuous time D/A converter.

9.9.2 Intermediate stage circuit diagram

The circuit diagram of an intermediate filter stage with a local feedback to obtain an extra zero in the noise transfer function is shown in Fig. 9.30. In

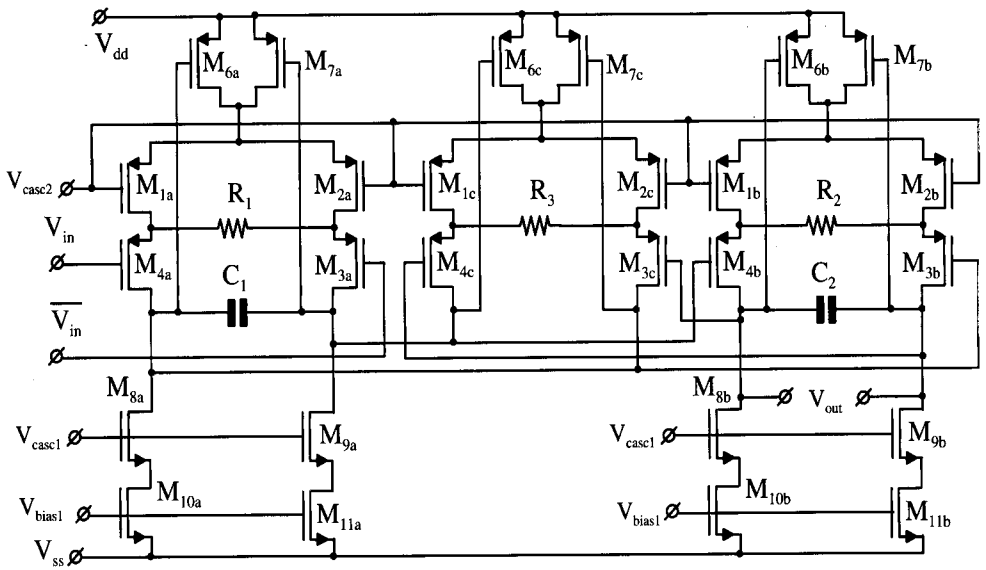

Figure 9.30: Intermediate stage circuit diagram [164]

the amplifier stages the same configuration as shown in Fig. 9.29 is used. However, these amplifier stages use a degeneration register to determine accurately the transconductance. This transconductance is approximately $g_m \approx \frac{1}{R_{1,2,3}}$. Resistor R_1 with the capacitor C_1 form an integrator stage. The same is found for R_2 with C_2. The transconductor with resistor R_3

couples signals back to the first integrator capacitor C_1. In this way an extra zero is introduced in the noise transfer function.

9.9.3 Simulated noise transfer function

The results of a simulation to obtain the noise transfer function is shown in Fig. 9.31. Note that this curve only gives the shape of the noise transfer

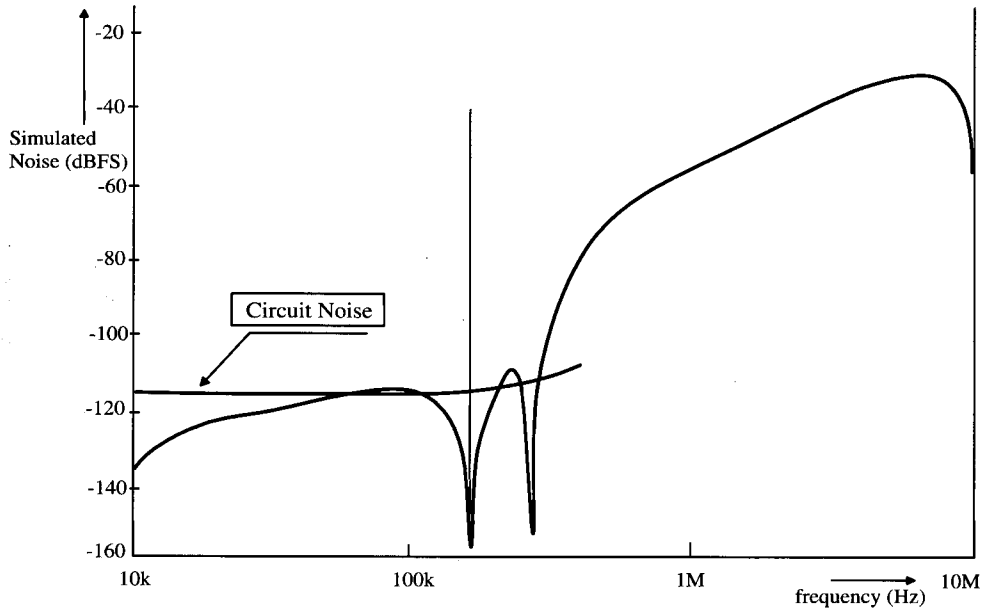

Figure 9.31: Noise transfer function (simulation) [164]

function. Furthermore the noise of the circuits is shown to obtain information about the limitation in the system.

9.10 Nth-order sigma-delta architecture

A general form of an Nth-order sigma-delta converter is shown in Figure 9.32. The system consists of a feed-forward path of integrators determined by the coefficients A_N and a feedback path determined by the coefficients B_N. When the coefficients B_N are not implemented, the converter of the previous section is obtained. At the moment the coefficients B_N are introduced, additional "zero" transmissions at different frequencies in the pass-band of the low-pass filter are introduced. These additional zeros reduce

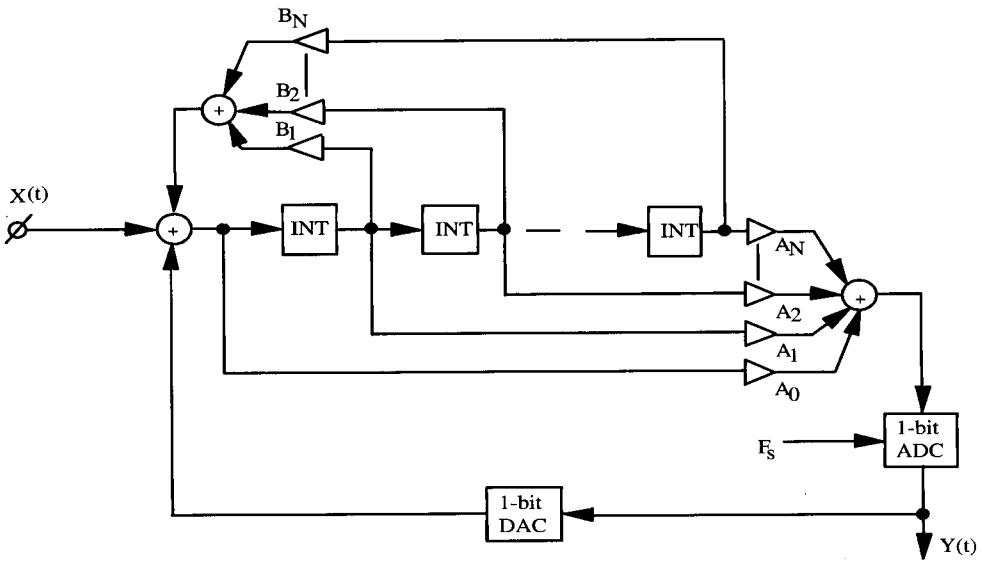

Figure 9.32: Nth-order sigma-delta converter architecture [99]

the quantization errors in the total signal band, resulting in an increase in dynamic range. In Figure 9.33 the noise transfer functions of a fourth-order sigma-delta converter according to Figure 9.32 are shown. Splitting up the transfer of the sigma-delta converter into a signal and an error term we obtain:

$$Y(z) = C_g K_x(z) X(z) + C_g K_e(z) N_q. \tag{9.51}$$

Here $K_x(z)$ represents the signal transfer function, and $K_e(z)$ is the noise-transfer function. In case of Figure 9.32 we obtain:

$$K_x(z) = \frac{\sum_{i=0}^{N} A_i (z-1)^{N-i}}{z[(z-1)^N - \sum_{i=1}^{N} B_i (z-1)^{N-i}] + \sum_{i=0}^{N} A_i (z-1)^{N-i}} \tag{9.52}$$

$$K_e(z) = \frac{(z-1)^N - \sum_{i=0}^{N} A_i (z-1)^{N-i}}{z[(z-1)^N - \sum_{i=1}^{N} B_i (z-1)^{N-i}] + \sum_{i=0}^{N} A_i (z-1)^{N-i}}. \tag{9.53}$$

As can be seen from $K_e(z)$, the coefficients B_i result in zero transmissions in the passband of the noise transfer.

In reference [99] a fourth-order converter design has been presented. Coefficient values for A_i are determined using a Butterworth filter design. The results are given here; we obtain:

$$A_0 = 0.865300 \tag{9.54}$$

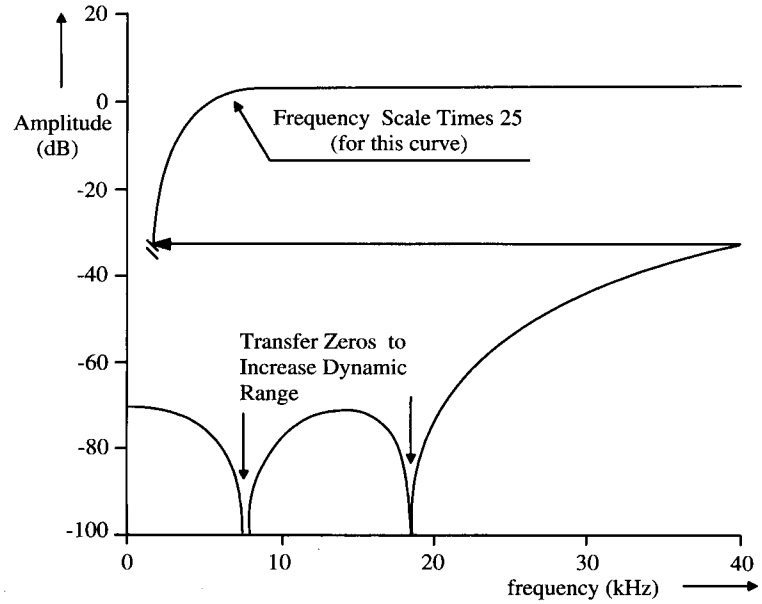

Figure 9.33: Noise transfer function of a sigma-delta converter [99]

$$A_1 = 1.192000 \tag{9.55}$$

$$A_2 = 0.390600 \tag{9.56}$$

$$A_3 = 0.069260 \tag{9.57}$$

$$A_4 = 0.005395. \tag{9.58}$$

The B_i coefficients are obtained by using a Chebyshev equi-ripple design. The coefficients obtained in this way are:

$$B_1 = -3.54010^{-3} \tag{9.59}$$

$$B_2 = -3.54210^{-3} \tag{9.60}$$

$$B_3 = -3.13410^{-6} \tag{9.61}$$

$$B_4 = -1.56710^{-6}. \tag{9.62}$$

The sample frequency of the converter is $f_s = 2.1$ MHz and the audio bandwidth is $f_b = 20$ kHz. The filter order $N = 4$.

9.11 Bandpass sigma-delta converters

Bandpass sigma delta converters are interesting for applications in all kind of radio applications such as AM/FM radio, GSM, UMTS and personal radio transceivers. Using digital signal processing the radio can be adapted to the specific needs at that moment. Bandwidth switching and adaptive filtering are possible. However, bandpass signal conversion might need more power than base band conversion. In some cases signal conversion into the low frequency band is applied. However, at that moment the performance of the system, especially image rejection in radio receivers, is determined by the analog quadrature mixer stages in front of the converter. Part of the flexibility is in that case lost. In this chapter different approaches to the problem will be discussed.

9.12 Low-pass to band-pass transformation

It is possible to transform a well known low-pass filter into a bandpass filter. This requires the substitution of:

$$z^{-1} \text{ by } -z^{-2}. \tag{9.63}$$

Applying this transformation to a second order filter $G(z)_{lp}$:

$$G_{lp}(z) = \frac{z^{-1}(2 - z^{-1})}{(1 - z^{-1})^2}, \tag{9.64}$$

then we obtain:

$$G_{bp}(z) = \frac{-z^{-2}(2 + z^{-2})}{(1 + z^{-2})^2}. \tag{9.65}$$

The noise transfer function of the low-pass filter with a notch around zero is transformed into a notch at z = ± j. This means that at $\frac{f_s}{4}$ a notch is obtained resulting in a bandpass character. Putting the notch at a quarter of the sampling frequency is not always the best solution. One of the problems that can occur is that third order distortion generated in the modulator appears at $\frac{3}{4}f_s$. At this frequency the repeated notch is present and this distortion is directly mixed into the signal band. This requires extreme linearity of the converter what is not always possible.

9.12.1 Switched capacitor implementation

An implementation using switched capacitor circuits is shown in Fig. 9.34 [150]. This converter system is a direct transformation from low-pass to

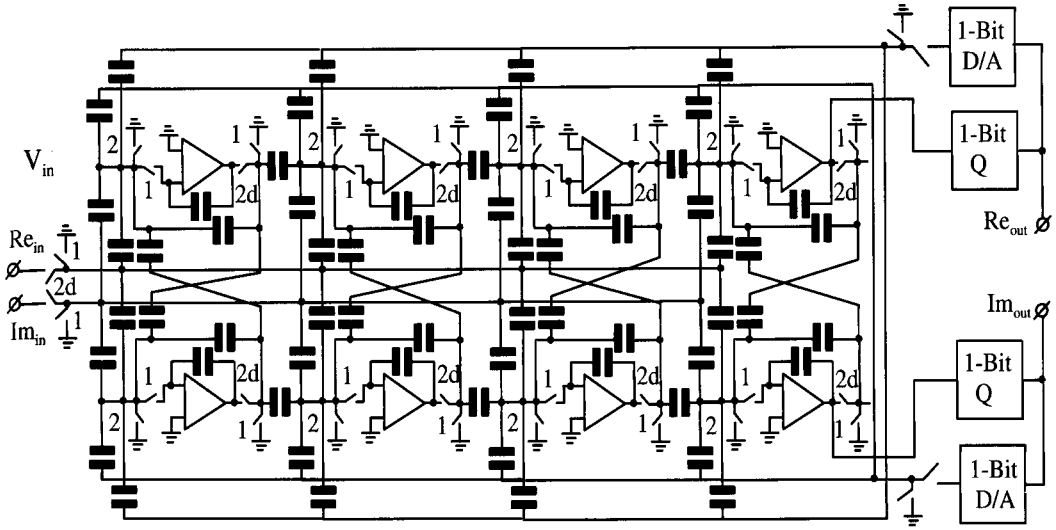

Figure 9.34: Switched capacitor band-pass converter architecture [150]

band-pass. The advantage of a switched capacitor implementation is that when the sampling clock frequency is changed, the performance remains the same and the frequency where the notch is obtained moves with the sampling clock. The disadvantage is the problem with third order distortion and furthermore aliasing of out-of band input signal frequencies with the sampling clock may introduce additional unwanted signal spectra.

9.12.2 Switched capacitor N-path architecture

Using an N-path architecture it is possible to transform z^{-1} into z^{-n}. This requires n identical stages to be connected in parallel using an input and output multiplexer to address one of the converters. In Fig. 9.35 this general architecture is shown. The N-path structure transforms the transfer function of the single converter $H_1(z)$ into $H_1(z^n)$. This means that multiple notches are found due to this transformation. Furthermore it gives the impression that too much hardware is used to perform this operation.

9.12.3 Two-path band-pass converter architecture

A two-path solution will be discussed [149] being an optimum in complexity and circuit speed. This solution is shown in fig. 9.36. Two identical high-pass noise shaping converters are connected in parallel. The switches ϕ_1 and

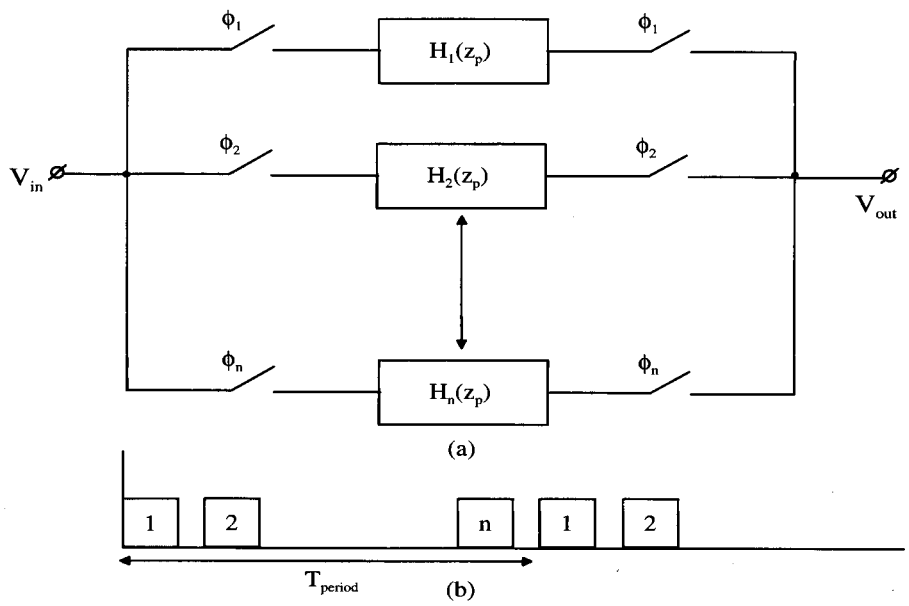

Figure 9.35: N-path converter architecture

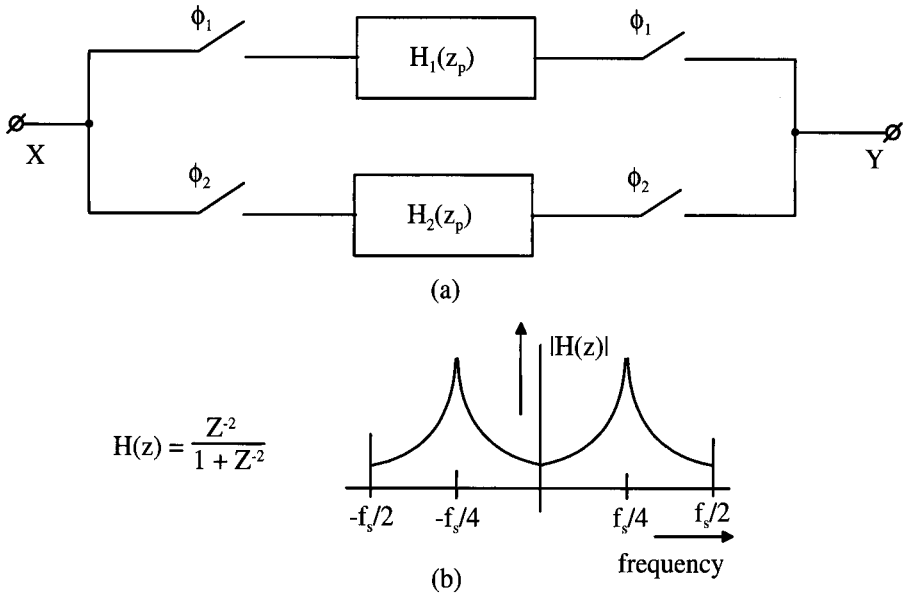

Figure 9.36: Two-path band-pass architecture [149]

ϕ_2 determine what converter is used to perform the conversion. A high-pass structure to obtain at $\frac{f_s}{4}$ the notch is needed for the bandpass character. The input sampling frequency f_s is 80 MHz in the practical solution so the notch appears at 20 MHz. In case mismatches are present in the system then distortion will appear and especially images will be mixed into the signal band. In a practical solution a mismatch of about 1 % is possible. This results in an image rejection of about 40 dB. In many cases this image rejection is not good enough for radio applications. GSM radios, however, do not require such a tremendous image rejection because the system is designed to avoid the image of a direct neighboring channel. This is a special case of band-pass conversion application.

9.12.4 Two-path circuit implementation

The implementation of a two-path band-pass converter is shown in Fig. 9.37. In this circuit two second order switched capacitor converters are connected

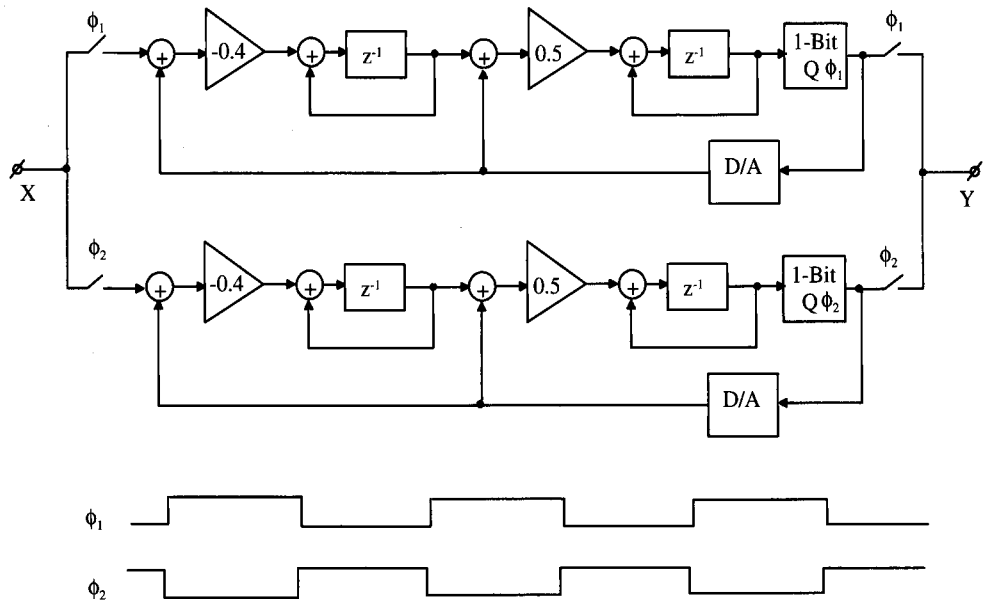

Figure 9.37: Two-pass band-pass circuit implementation [149]

in parallel. The input and output switches perform the selection of one of the high-pass converters. Sampling frequency of every converter is $\frac{f_s}{2}$. This means a limited requirement on the individual units.

9.13 Continuous time band-pass converter

At the moment a continuous time filter is used in the band-pass converter, then the notch frequency is independent of the sampling clock frequency. This can be an advantage because in some cases the digital signal processing system uses a clock frequency that is not related to the receiver intermediate frequency (IF). Tuning the bandpass to this intermediate frequency allows the use of a different sampling frequency that can be optimized to perform the digital signal processing. In fig. 9.38 the simplest form of a continuous time band-pass converter is shown [148]. The band-pass filter passes the

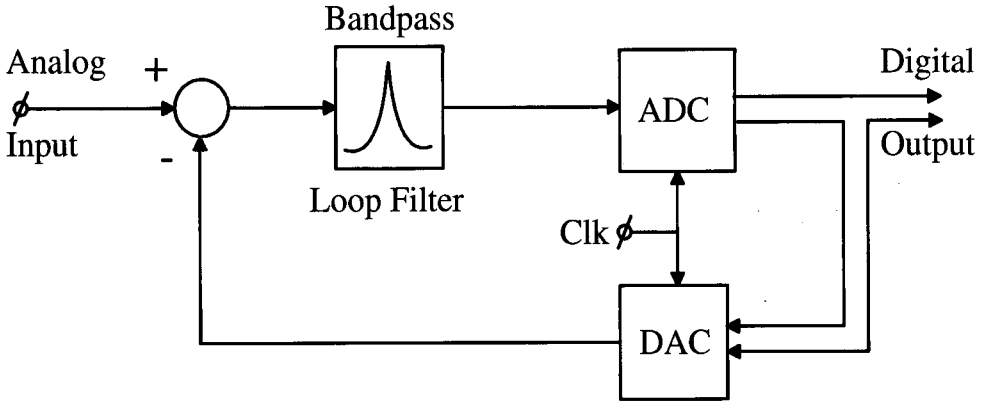

Figure 9.38: Band-pass converter architecture

signal to the quantizer at the tuning frequency of the filter. Outside this range signals are removed. Especially signal frequencies above the tuning frequency are removed because of the continuous time character of the filter. This can be an advantage of this system.

9.13.1 Band-pass filter architecture

The architecture of the band-pass filter is shown in Fig. 9.39. This filter consists of three resonators. These resonators are build up using a differential circuit structure. The coefficients C_{nI} and C_{nQ} are required to obtain a stable operation of the converter. The implementation of the resonator is shown in fig. 9.40. This is a sixth order band-pass converter obtained from a transformation from a stable third order converter. The resonators use

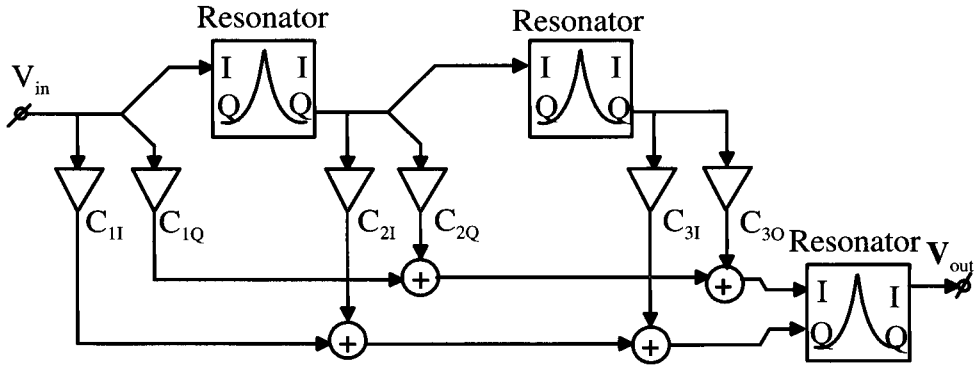

Figure 9.39: Band-pass loop filter architecture

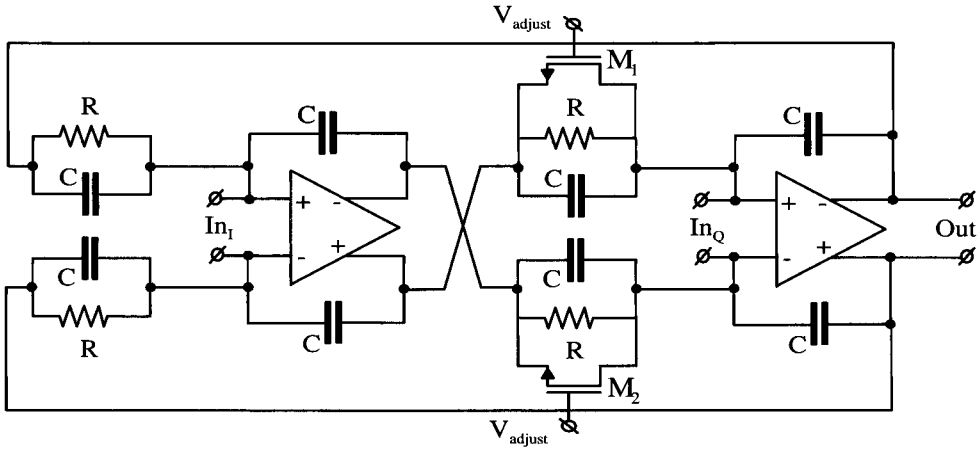

Figure 9.40: Resonator architecture

two balanced integrators. The tuning frequency is determined by:

$$f_{res} = \frac{1}{2\pi RC}. \tag{9.66}$$

The two capacitors C in parallel with the resistors R limit the quality factor of the tuned circuit. Furthermore MOS transistors M_1 and M_2 perform a tuning of the notch frequency. Usually capacitors and resistors in an integrated circuit have an absolute inaccuracy that can be in the order of 10%. By changing the value of the tuning resistor R it is possible to set the notch at the required frequency. This very simple tuning function included in the design has a small influence on the total circuit performance.

9.13.2 Differential amplifier implementation

The circuit diagram of the transconductance amplifier used in the balanced integrator filter is shown in Fig. 9.41. The input signal is applied to the

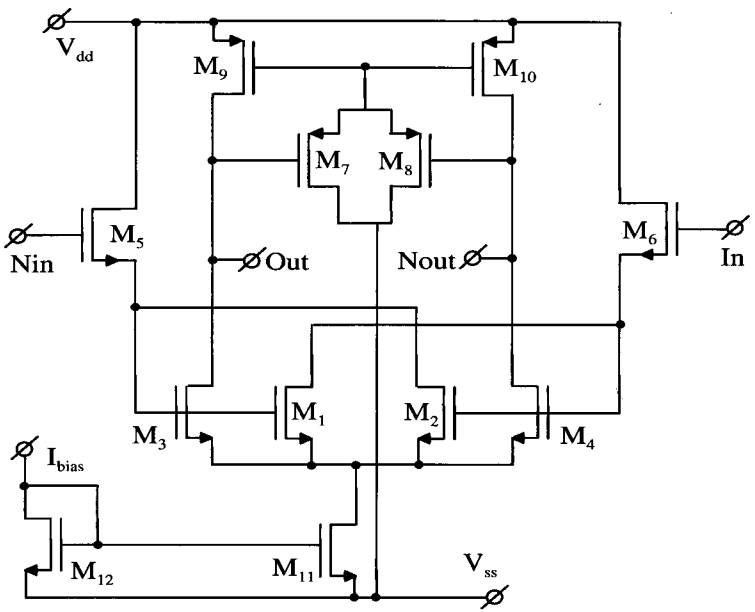

Figure 9.41: Differential CMOS amplifier circuit

source followers M_5, M_6. The output of these source followers is applied to the transconductance amplifier M_3, M_4. Biasing of the source followers is performed by the cross-coupled pair M_1, M_2. This cross-coupling gives an

extra positive feedback to the gates of M_3, M_4 resulting in a large transconductance. At the output transistors M_9, M_{10} are applied as active current source load. The biasing of these devices is performed by M_7, M_8. With small output signals M_7, M_8 perform a constant biasing for M_9, M_{10}. When a large output signal is generated, then only M_7 or M_8 remains active and the load is transformed into a current mirror. Such an operation is not preferred.

9.13.3 Measurements sixth order band-pass converter

In Fig. 9.42 the frequency response measurements of the sixth order band-pass converter are shown. The inter modulation measurements using signals

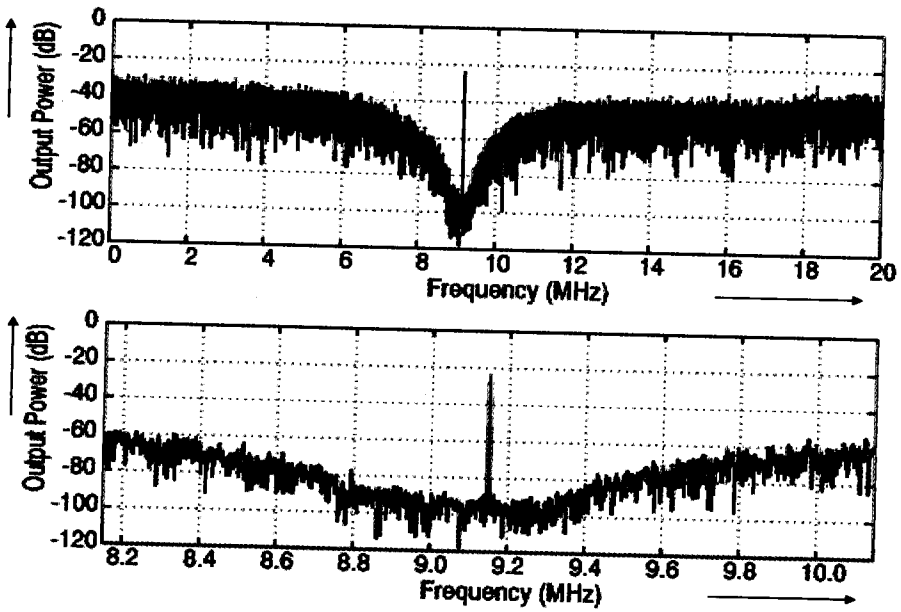

Figure 9.42: Frequency response of sixth order band-pass converter

with a carrier separation of 9 kHz, 100 kHz and 200 kHz at a center frequency of 9.15 MHz are shown in Fig. 9.43. From these measurements it is seen that the noise level in the circuit is coinciding with the inter modulation distortion in the system. The specifications of the converter are given in table 9.2. In this table only a limited amount of data has been presented. For more information see [142]. The performance of continuous time band-pass converters is already at a very high level. Still with scaled technology and some modifications in design the improvement in performance is at a

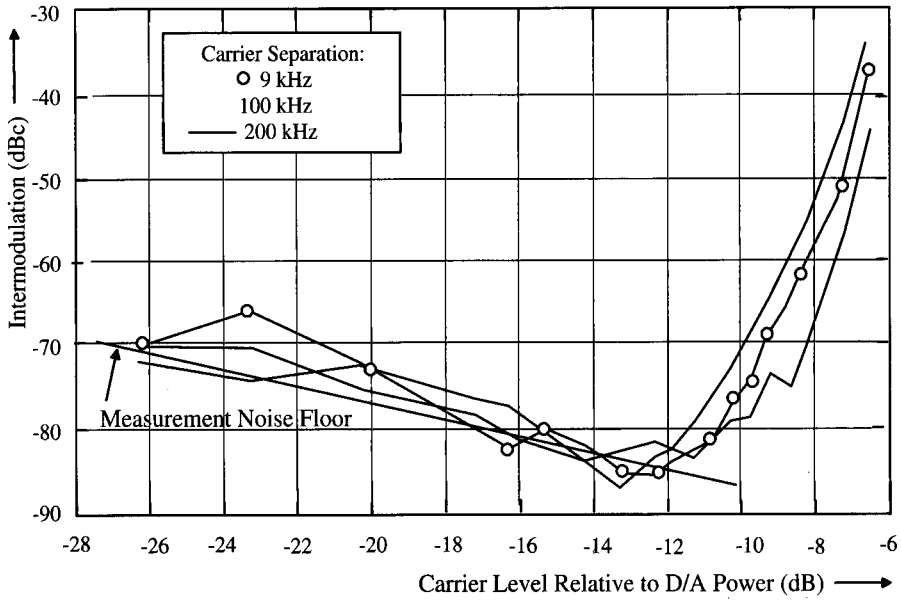

Figure 9.43: Inter modulation measurement

Technology	0.5 μm DPTM CMOS
Power supplies	5 V analog, 3 V digital
Power dissipation	60 mW (f_s = 40 MHz)
Sample frequency	30-80 MHz
Tuning frequency	9.15 MHz
Input voltage	200 mV_{pp} differential
Bandwidth	200 kHz
Idle channel noise	-78.5 dB
Dynamic Range	72 dB
SNDR (peak)	67 dB
THD (-0.1 dBFS, 100 kHz)	-98 dB (SD = 1.2 dB)
ENOB	10.8 Bit
IM3 relative to carriers	-82 dBc
Chip size	0.4 x 0.9 mm^2

Table 9.2: 6th Order band-pass converter data

level that this concept can be applied in very high quality integrated AM/FM receivers.

9.14 Limited gain in loop filter

When the gain of the loop filter is limited, then the poles of the transfer function can not be placed exactly on the unit circle. This results in a loss of gain of the noise transfer function. The dynamic range of the system decreases at that moment. In practical converters the gain of the integrators is limited by the implementation. An estimate of the loss in dynamic range can be obtained. Suppose the general class of low-pass loop filters is used:

$$G(z) = \frac{(1 - az^{-1})^N}{(1 - bz^{-1})^N} - 1. \tag{9.67}$$

In ideal operation of a converter the coefficient b is exactly 1. However, due to limited gain this coefficient deviates from 1. this will be modeled by:

$$b \approx 1 - \frac{1}{G_{DC}}. \tag{9.68}$$

Here G_{DC} is the low frequency gain of the low-pass filter function. The in-band idle channel noise can be calculated by integrating:

$$N_{idle\ channel} = \frac{q^2}{12\pi} \int_0^{\theta_b} | \frac{(1 - be^{-j\theta})^N}{(1 - c_g)(1 - be^{-j\theta})^N + c_g(1 - ae^{-j\theta})^N} |^2 \, d\theta. \tag{9.69}$$

The ratio between the solution of this equation for $b = 1$ and $b \neq 1$ gives the reduction in dynamic range due to the limited gain in the amplifiers. In Fig. 9.44 the result of the dynamic range reduction for converters with a filter order from 1 to 4 and a range of b form 1 to 0.95 is shown. The parameter a is zero for first and second order loop filter and a = 0.412 for a third order loop filter and a = 0.587 for a fourth order loop filter.

9.15 Idle pattern

The idle pattern generated in sigma-delta converters depends on the order of noise-shaping used in the coder. In Figure 9.45 an example of an idle pattern with zero input and with a sine wave input signal are shown.
When well-determined dc input signals are applied to a first-order converter, some stable patterns can be found. The following analysis gives some of the

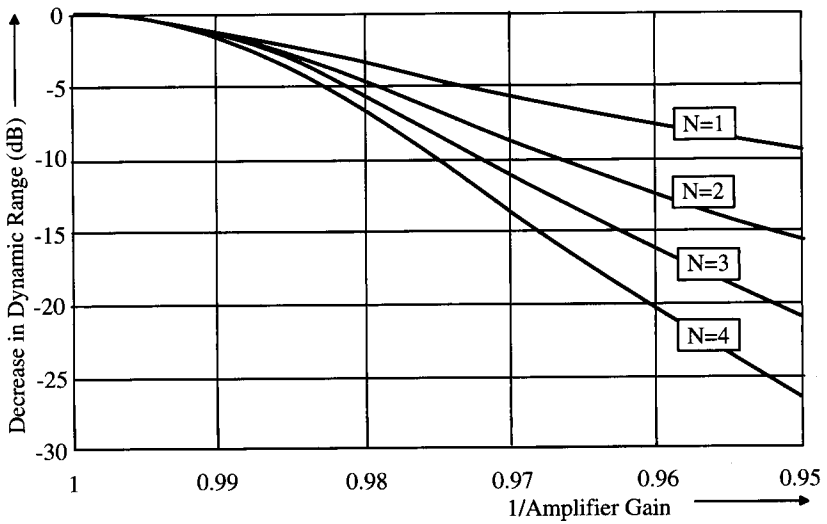

Figure 9.44: Reduction of dynamic range due to finite loop filter gain

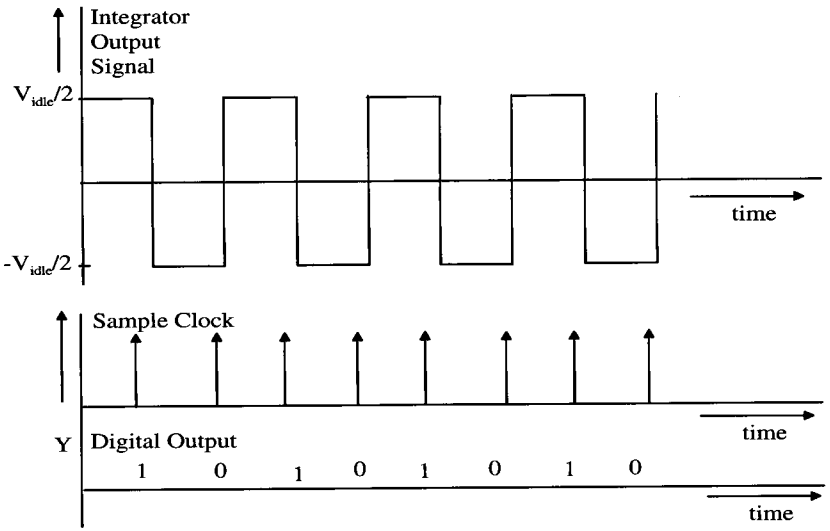

Figure 9.45: Idle pattern of a sigma-delta A/D converter with zero input signal

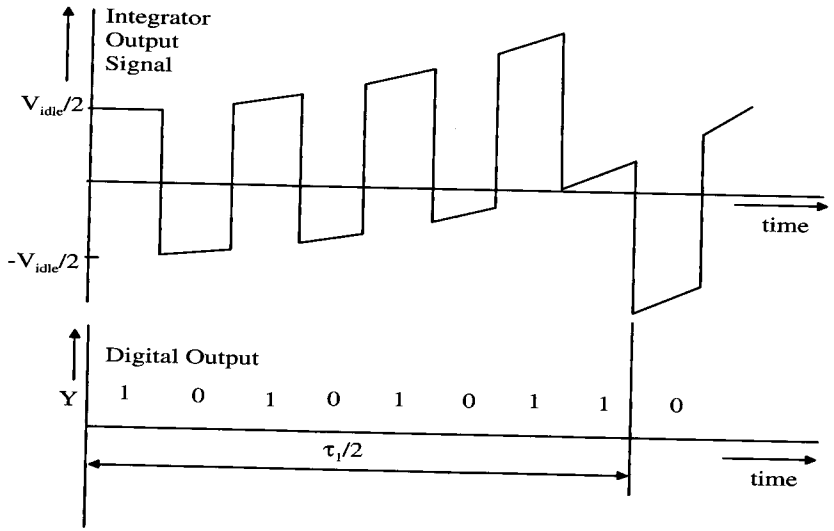

Figure 9.46: Idle pattern of a sigma-delta A/D converter with a sine wave input signal

most common patterns.

Suppose that during n_1 successive clock pulses the capacitor is charged and during n_2 clock pulses the capacitor is discharged. Suppose furthermore that after n_r repetitions of the previous pattern during one clock pulse an additional charge pulse is added; then we obtain for the total charge:

$$Q_{charge} = n_r \times n_1(Q_{ref} - Q_{analog}) + Q_{ref} - Q_{analog}. \tag{9.70}$$

The amount of charge discharged from the integration capacitor becomes:

$$Q_{discharge} = n_r \times n_2(Q_{ref} + Q_{analog}). \tag{9.71}$$

The operation of the A/D converter forces the total charge and discharge to cancel, which means:

$$Q_{charge} = Q_{discharge}. \tag{9.72}$$

After rearranging, we obtain:

$$\frac{Q_{analog}}{Q_{ref}} = \frac{n_r(n_1 - n_2) + 1}{n_r(n_1 + n_2) + 1}. \tag{9.73}$$

Note that if a positive input signal is applied, then the number of discharge pulses n_2 must be equal to 1 to obtain the required idle pattern at half the

sampling frequency. At the same time n_1 becomes 1 for a negative input signal.

A special class of stable patterns is obtained when the repetition n_r becomes very large ($n_r \gg 1$). Equation 9.73 simplifies into:

$$\frac{Q_{analog}}{Q_{ref}} = \frac{n_1 - n_2}{n_1 + n_2} \tag{9.74}$$

Again, with a positive input signal n_2 is 1 and with negative input signals n_1 is 1.

By using $n_2 = 1$ and varying n_1 from 1, 2, 3, and so on, an analog input signal of 0, $\frac{1}{3}Q_{ref}$, $\frac{1}{2}Q_{ref}$, and so on, must be applied.

The drawback of stable patterns is found in the frequency distribution of the quantization error. At that moment correlations with the input signal are obtained. Such correlations may results in whistles and birdies in the quantized signal. In audio applications such a correlation is not allowed because the human ear is very sensitive for repetitive signals.

9.15.1 Threshold effect of a first-order converter

The idle pattern generated in a sigma delta A/D converter introduces a threshold effect below which no signal quantization is obtained. A signal is quantized at the moment the integrated input signal is equal to half the amplitude of the idle pattern. An example of such a quantization is shown in Figure 9.45(b). The figure shows that at the moment the amplitude of the integrated input sine wave crosses the zero line, an extra discharge pulse is needed. This extra pulse changes the 1 0 1 0 . . pattern into a 1 0 1 0 1 1 0 pattern. The extra 1 contains the quantization information.

The threshold effect of the A/D converter shown in Figure 9.9 can be calculated rather simply. Assume that no input signal is applied to the converter and suppose, furthermore, that all elements are ideal; then the amplitude of the idle pattern becomes:

$$V_{id} = \frac{C_1}{C_2} V_{ref}. \tag{9.75}$$

Here V_{id} is the peak-to-peak amplitude of the idle pattern and V_{ref} is the reference voltage applied to the converter. The discrete-time D/A converter used results in a gain ratio determined by the capacitors C_1 and C_2. The

input signal is integrated using the continuous-time integrator with R and C_2.

If a sine wave $V_p \sin \omega_{in} t$ with a small amplitude is applied to the converter, this signal is integrated and added to the charge generated by the capacitive D/A converter circuit. Suppose that the amplitude of the input signal is so small that it takes a time τ_1 before the idle pattern is disturbed. The amplitude of the sine wave signal over the time τ_1 then becomes:

$$\int_0^{\tau_1} \frac{V_p}{R} \sin 2\pi f_{in} t dt = C_2 V_{out}. \tag{9.76}$$

By reworking equation 9.76 the output voltage V_{out} becomes:

$$V_{out} = \frac{1}{2\pi f_{in}} \frac{V_p}{C_2 R} [\cos(2\pi f_{in} \tau_1) - 1]. \tag{9.77}$$

The minimum value of equation 9.77 is obtained if:

$$2\pi f_{in} \tau_1 = \pi \text{ or } \tau_1 = \frac{1}{2 f_{in}}. \tag{9.78}$$

Inserting the value of 9.78 into equation 9.77 results in:

$$V_{out} = -\frac{1}{\pi f_{in}} \frac{V_p}{C_2 R}. \tag{9.79}$$

The maximum value of equation 9.77 is obtained when $\cos 2\pi f_{in} \tau_1 = 1$. Then a maximum output signal $V_{out} = 0$ is obtained. The peak-to-peak value of the output signal V_{out} is equal to the value given by equation 9.79. The idle pattern is disturbed when the output voltage $V_{out} = \frac{1}{2} V_{id}$. The following result is then obtained:

$$V_{out} = V_{id}. \tag{9.80}$$

To obtain a relation between the maximum input signal value V_{max} and the threshold effect of the converter, a relation between the reference voltage V_{ref} and the maximum signal level is needed. Using a charge balance equation, the following relation is valid:

$$\frac{V_{max}}{R} \frac{1}{f_s} = V_{ref} C_1. \tag{9.81}$$

By combining equations 9.75, 9.76, 9.79, and 9.81, the following result is obtained:

$$V_p = -\pi \frac{f_{in}}{f_s} V_{max}. \tag{9.82}$$

The peak threshold voltage can be defined as:

$$V_{th} = \mid V_p \mid . \tag{9.83}$$

Inserting equation 9.83 into equation 9.82 results in:

$$V_{th} = \frac{\pi f_{in}}{f_s} V_{max}. \tag{9.84}$$

From equation 9.84 it is seen that the threshold voltage linearly increases with the input signal frequency. The result of the threshold is the introduction of signal distortion. This distortion increases with increasing input frequency. The threshold voltage can be reduced by increasing the order of the loop filter.

9.15.2 Threshold effect of a second-order converter

In the second-order sigma-delta A/D converter an extra integrator is inserted in the loop. To obtain stability, which means an idle pattern around $\frac{f_s}{2}$, a zero must be added. A good practical approach is found when the frequency f_n of the zero is at about $\frac{1}{10} f_s$. Because of the increased loop gain, a reduction of the threshold voltage is obtained at lower frequencies. An estimate of the threshold voltage can be determined. The result becomes:

$$V_{th} = \frac{\pi f_{in}^2}{f_s f_n} V_{max}. \tag{9.85}$$

From equation 9.85 it is found that the threshold reduces with a factor $\frac{f_{in}}{f_n}$. With large oversampling ratios the improvement is obtained. However, a second-order system results in an increase in dynamic range. In practice this results in the fact that the frequency for which the threshold is reached is still in the signal band of interest.

At that moment the threshold determines the dynamic range and not the loop filter. To overcome this problem a dither signal is usually added. Such a dither signal linearizes and reduces the threshold, resulting in an improvement is dynamic range and a lower distortion.

9.15.3 Dither signals

To avoid correlation of idle patterns with the input signal in an A/D converter, a dither signal can be applied. Such a dither signal can be a small

noise signal or a signal at half the sampling frequency. The amplitude of this dither signal is small to avoid a reduction in dynamic range of the total converter system. The purpose of the dither signal is to disturb the fixed signal patterns in the converter. In this way no correlation of the quantization noise and the input analog signal exists so a mere noise-like error signal is obtained. At the same time the dither signal reduces the threshold of the converter, resulting in a reduction in distortion of the signal and a coding of low-level, high-frequency input signals.

9.15.4 Threshold signal distortion

When a signal is applied to a transfer function with a threshold around zero, distortion is obtained. By applying a sine wave at the input of the converter, the output signal can be approximated by a sine wave minus a square wave with an amplitude equal to the threshold voltage and a frequency equal to the input sine wave.

By using equation 9.84, the amplitude of the square wave is found. This square wave is expanded in its Fourier series. This gives:

$$V_{sq} = \frac{4V_{th}}{\pi}(\sin f_{in} + \frac{\sin 3f_{in}}{3} + \frac{\sin 5f_{in}}{5} + ... \tag{9.86}$$

The series in 9.86 only contains odd harmonics. In Figure 9.47 the result of a simulation is shown. The simulation result shows the increase of the distortion and noise at the high-frequency band edge of the system. This is because of the noise-shaping. At the moment a dc offset is added to the system, the series expansion changes and even order terms will appear as well. Equation 9.86 now changes into:

$$V_{sqdc} = \frac{Vth}{2}[k + \frac{2}{\pi}(\sin k\pi \cos f_{in} + \frac{1}{2}\sin 2k\pi . \cos 2f_{in} + .. \tag{9.87}$$

In a practical situation k is between $\frac{1}{2}$ and $\frac{1}{4}$ for a dc offset between zero and about $\frac{V_{th}}{2}$. In equations 9.86 and 9.87 V_{sq} and V_{sqdc} are the amplitudes of the fundamental and the distortion products introduced by the threshold effect of the converter. The ratio between these components and the maximum signal level V_{max} results in the distortion of the converter.

9.16 Sigma-delta digital voltmeter

An example of a first-order sigma-delta modulator used as a five-digit digital voltmeter A/D converter will be discussed. The system uses full-time pulses

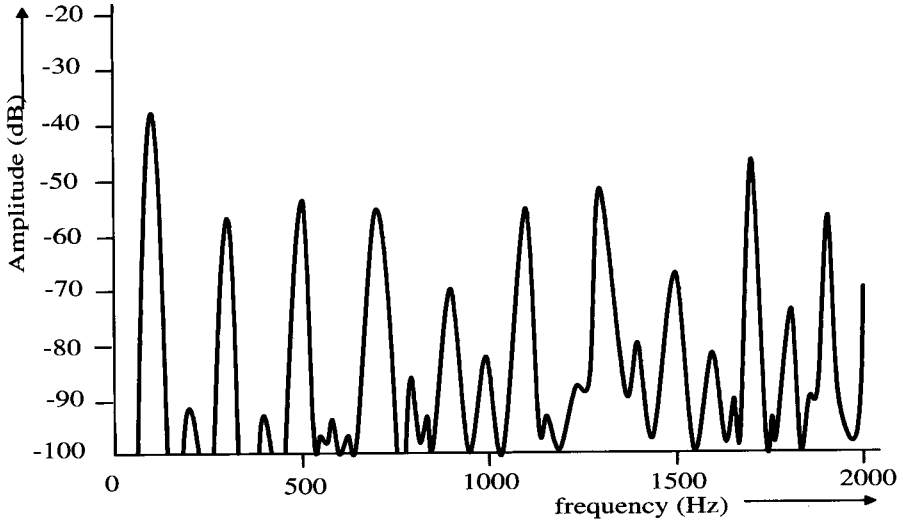

Figure 9.47: Distortion simulation of a sigma-delta A/D converter

in the D/A converter together with a continuous-time first-order filtering operation. The basic converter system is shown in Figure 9.48. The input signal is applied to the converter as a current I_{in}. The charge and discharge reference currents are called I. The signal is integrated across the capacitor C. The voltage across the capacitor is monitored by the comparator *comp* that drives the flip-flop FF. This flip-flop is toggled by the system clock f. The output of the flip-flop controls the switch S that switches the charge or discharge currents I to the capacitor C. When no input signal is applied to the system, then a triangular wave is generated across the capacitor C. The average value of the capacitor voltage is zero. When an input signal is applied, then the one-zero pattern changes. The output of the flip-flop called *Data* is applied to an up-down counter which performs the conversion of the 1-bit sigma-delta signal into a binary-weighted output signal. In Figure 9.49 the total digital voltmeter system is shown. The sigma-delta converter is enlarged with a timer ($Timer(N)$), an up/down counter and a gating function. The timer function counts the total amount of up and down pulses $N = n_{up} + n_{down}$. During this time the gate is opened and the difference between the up and down pulses $n = n_{up} - n_{down}$ are counted in the up-down counter. Then the gate is closed and the system must be reset to start the next conversion cycle. It can be shown that the ratio between

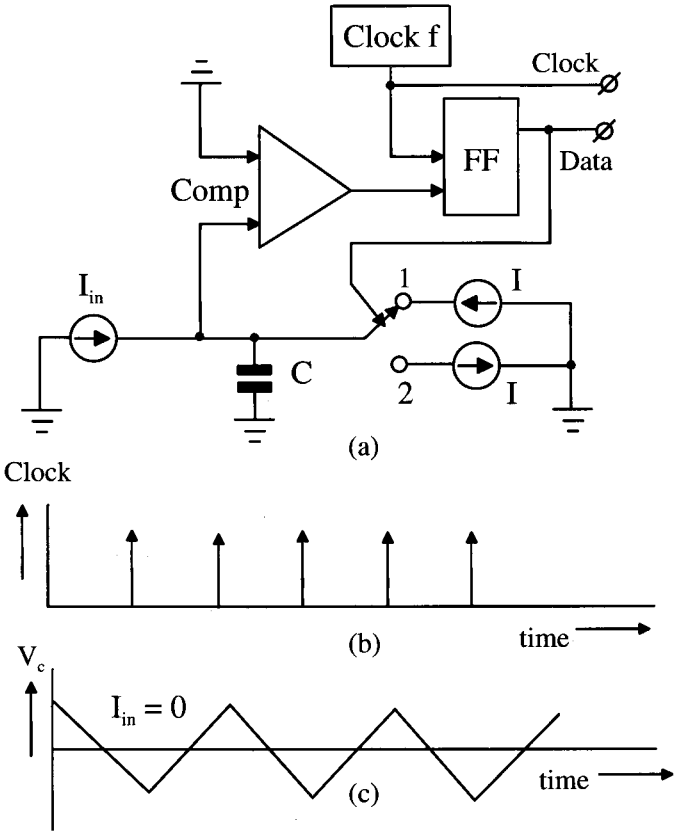

Figure 9.48: Basic sigma-delta digital voltmeter system

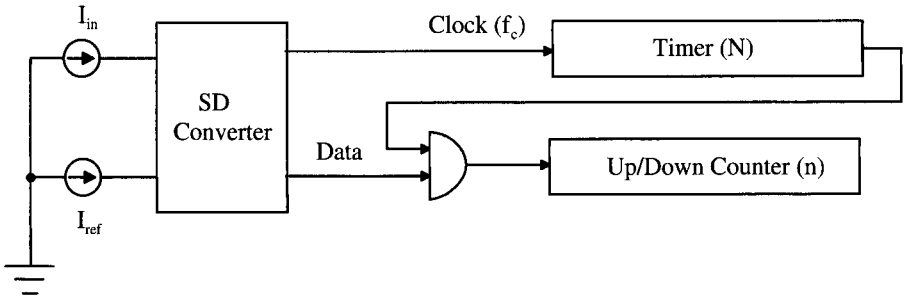

Figure 9.49: Total digital voltmeter system

the analog input signal I_{in} and the reference current I_{ref} is equal to:

$$\frac{I_{in}}{I_{ref}} = \frac{n_{up} - n_{down}}{n_{up} + n_{down}} = \frac{n}{N}. \tag{9.88}$$

The resolution of the converter is determined by the length N of the timer circuit, while the conversion time T_c at a certain resolution N is determined by the clock frequency f_c, so

$$T_c = \frac{N}{f_c}. \tag{9.89}$$

When the conversion time T_c is related to the mains frequency, then due to the integration of a full- or a multiple period of the mains frequency, a very good rejection of this frequency is obtained.

9.16.1 Auto-zero circuit

In high-resolution analog systems dc offset is a problem because it adds or subtracts from small input signals. To overcome the offset problem in the analog circuit part of the converter, an auto-zero system is used. The basic configuration is shown in Figure 9.50. In Figure 9.50 the offset of the analog subsystem is given by V_{off}. At the input of the system a set of switches is added. These switches invert the analog input signal with respect to the A/D converter. At the output the data pulses are inverted, depending on the input switch settings. In this way the input "inversion" is removed from the data which are applied to the counter section. The system basically operates by dividing the conversion time T_c into two equal parts $T_c/2$. During the first part of the conversion time input terminals 1 and 3 are connected as is done with 2 and 4. In the second part terminals 3 and 4 are interchanged. During the first part of the measuring time, a voltage V_{m1} equal to $V_{in} - V_{off}$ is measured. During the second half of the measuring time a voltage V_{m2} equal to $-V_{in} - V_{off}$ is converted. The difference between V_{m1} and V_{m2} must be calculated. By inserting the data inverter during the second part of the measuring time, the data inversion is performed and the subtraction is transformed into an addition. An addition is very easy to implement by counting of pulses. As a result, the measured voltage is equal to:

$$V_m = \frac{1}{2}(V_{in} - V_{off} + V_{in} + V_{off}) = V_{in}. \tag{9.90}$$

As can be seen from equation 9.90, the auto-zero circuit ideally cancels the offset voltage without increasing the conversion time. A second advantage

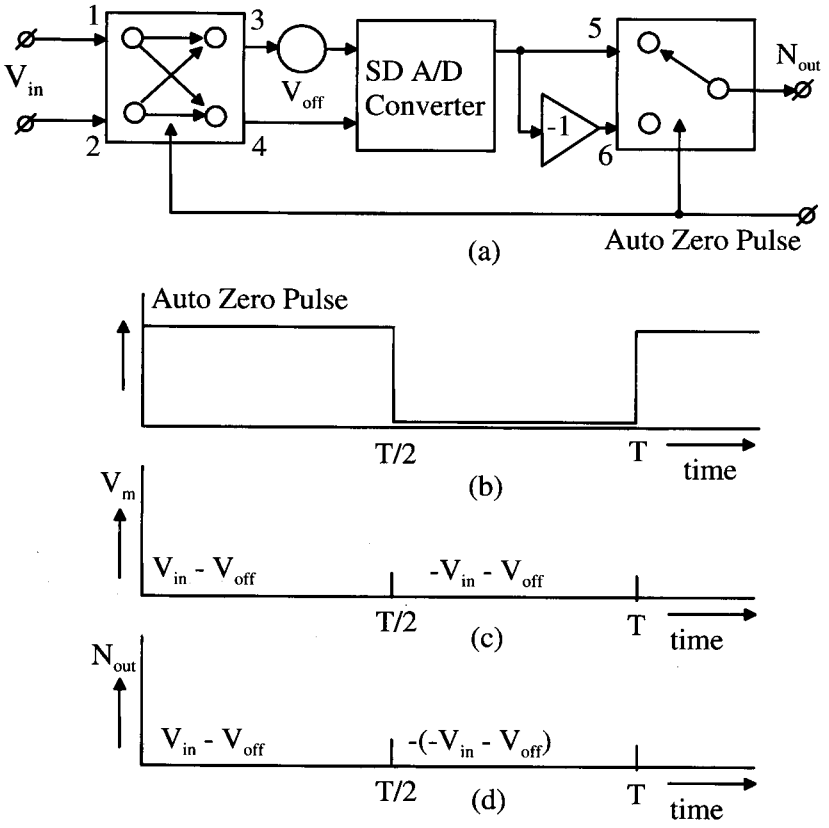

Figure 9.50: Auto-zero system

of this system is that the measured values for positive and negative signals is exactly equal because there is no difference between measuring a positive signal or a negative signal according to equation 9.90 except from the sign determining algorithm.

9.16.2 Analog subsystem implementation

A simplified diagram of the analog subsystem is shown in Figure 9.51. The system consists of a voltage-to-current converter V *to* I, the differential PMOS transistor pair M_3 and M_4 controlled by the flip-flop FF, a comparator *comp*, the integration capacitor C, and the reference current source I_{ref}. An additional operational amplifier *Op. Amp.* controls the current sources I_1 and I_2 in the voltage-to-current converter. The voltage-to-current converter is drawn as the differential amplifier pair M_1 and M_2 with source

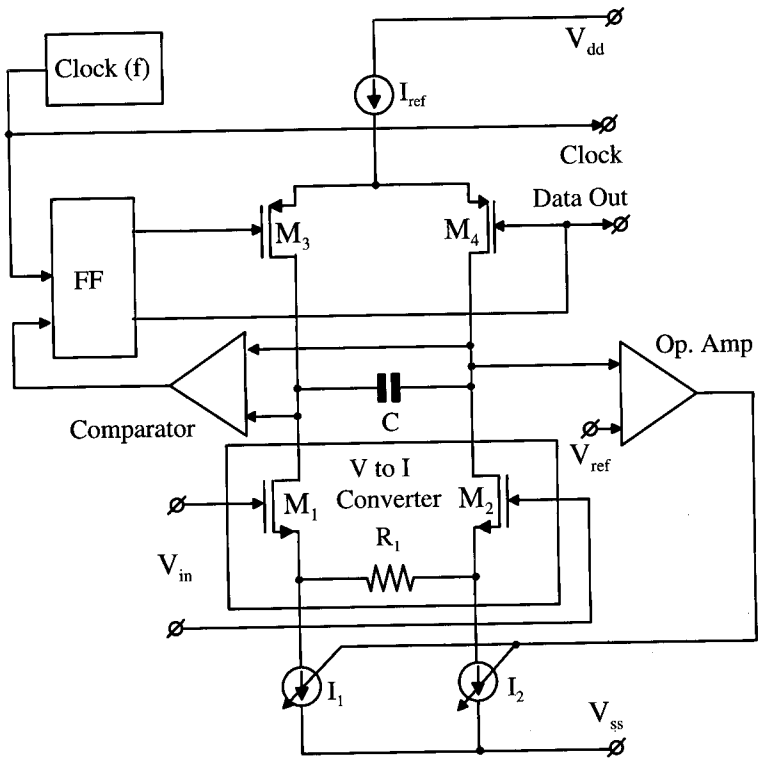

Figure 9.51: Analog subsystem implementation

degeneration resistor R_1.

The equal charge and discharge currents are generated by the reference current I_{ref} and the differential pair M_3 and M_4. The operational amplifier *Op. Amp.* controls the currents I_1 and I_2 in such a way that the potential of the drain voltages of M_2 and M_4 is at zero volt. The sigma-delta converter operation performs the same with the drain voltages of M_1 and M_3. The input system is a full-differential system that is required for the auto-zero function. Digital output signals of the conversion section are *clock out* and *data out*. These signals are applied to the digital counting section.

9.16.3 Complete digital voltmeter system

The complete digital voltmeter system is implemented in a CMOS digital part for control and display function and an analog part that contains the complete sigma-delta A/D converter section with reference source and gain

selection. In Table 9.3 the performance of the system is shown. The internal

Input voltage	100 mV and 1 V (bipolar)
Resolution	5 digits plus sign (f_{clock} = 200 kHz)
Linearity	$\pm$ 10^{-5} of full scale
Zero stability	$< 10^{-6}$ per degree C
Temp. coefficient. of reference source	5.10^{-6} per degree C over Δ T = 80^0 C
Supply voltage dependence of reference source	5.10^{-6} per V
Power supply	$\pm$ 7.5 V 20 mW

Table 9.3: Digital voltmeter performance data

reference voltage is based on the band-gap principle of silicon.

9.17 Conclusion

Sigma-delta converters are excellent alternatives for high-resolution analog-to-digital converters for applications in digital audio, digital video and digital voltmeter systems. Bandpass modulators are furthermore attractive for the implementation of digital AM/FM radio receivers. Continuous time filters are preferred in this case. With variable sampling frequency the tuning frequency remains at the same place. The single-bit sigma-delta system needs only two or, in special configurations one reference voltage to perform the conversion. In these systems an excellent differential linearity with small input signals is obtained. The combination of the noise-shaping filter with the anti-alias function minimizes the components count and seems to be a very attractive alternative for digital audio signal conversion. Even a larger dynamic range can be obtained compared to direct conversion methods (e.g. successive approximation algorithm). When the maximum clock rate is limited, an increase in dynamic range can be obtained by combining a multi-bit D/A converter function with a noise-shaping function. At the moment a filtering order above a second-order is used, then feed-forward techniques can be used to obtain a stable operation of the converter under all signal conditions. The MASH structure as a cascade of first or second order noise-shapers shows an excellent performance. A higher order noise-shaping

is obtained without problems with stability. In a multi-bit application even a larger dynamic range is obtained. Dynamic element matching architectures are needed in this case to obtain the extreme linearity of the system. Data Weighted Averaging uses a dynamic element matching technique without filtering the error signals introduced by the interchanging method. By randomizing the error spectrum over the out-of band interval the filtering function of the element errors can be eliminated. The presented dynamic range calculations are for idealized systems. Care must be taken in using the presented results. However, the results help to understand the operation of the sigma-delta converter.

Chapter 10

Voltage and current references

10.1 Introduction

In A/D and D/A converters the full-scale value is determined by the reference source. A low noise and low temperature coefficient of the output signal of the reference source is very important for high-resolution, high-accuracy converters. A well-known device for stabilizing a reference voltage is a zener diode. In integrated circuits, however, the zener diode can cause problems with the reliability of the circuit. In modern technologies it is not always possible to reverse-bias the emitter-base junction of a transistor to obtain a zener diode operation. The yield of circuits is reduced by reverse-biasing transistors. Today's reference sources are built using the band-gap voltage of silicon as a low-temperature dependent reference voltage. In this chapter different circuits will be described that use the band-gap principle to stabilize a voltage or a current. Examples of band-gap reference voltages are given in references [75, 76, 78].

10.2 Gate-source voltage used as a reference

The gate-source voltage of a transistor can be used as a very simple reference voltage. A simple practical example of such a stabilizer is shown in Figure 10.1. The circuit consists of two transistors M_1, M_2 and two resistors R_1, R_2. As a stabilized voltage the gate-source voltage of transistor M_1 is used. The voltage stabilization is obtained because of the quadratic characteristic of the transistor. When a large mutual conductance (g_m) is used, then a good

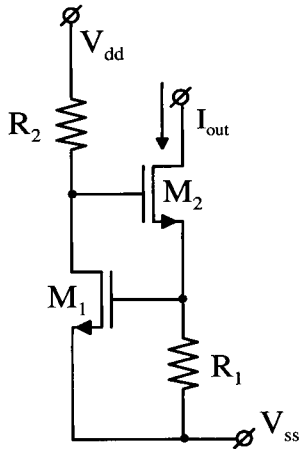

Figure 10.1: Gate-source voltage stabilizer example

stabilization is found. A simple calculation gives:

$$\frac{\delta I_{out}}{\delta V_{dd}} \approx \frac{1}{R_1(1+g_{m1}R_2)} \tag{10.1}$$

A good stabilization factor is obtained if a large supply voltage is used. Furthermore this circuit is difficult to use with small supply voltages.

10.2.1 Improved gate-source voltage stabilizer

The stabilization factor of the circuit given in Figure 10.1 can be improved. A simplified circuit diagram of the improved system is shown in Figure 10.2. Basically this system consists of a current mirror consisting of transistor M_2 connected as a diode and transistor M_1 acting as the output current device. Between the gate and drain of transistor M_2 an extra resistor R_1 is connected. The purpose of this resistor is to compensate for the increase in the gate-source voltage of M_2 with increasing supply voltage V_{dd}. With an increasing voltage V_{dd} the voltage drop across the resistor R_1 increases, and this voltage drop is subtracted from the increase in gate-source voltage of transistor M_2. The output voltage applied to the gate of transistor M_1 in this way is nearly constant, resulting in a constant output current. A simple calculation results in the following condition to obtain the supply voltage cancelation condition:

$$g_{m2}R_1 = 1. \tag{10.2}$$

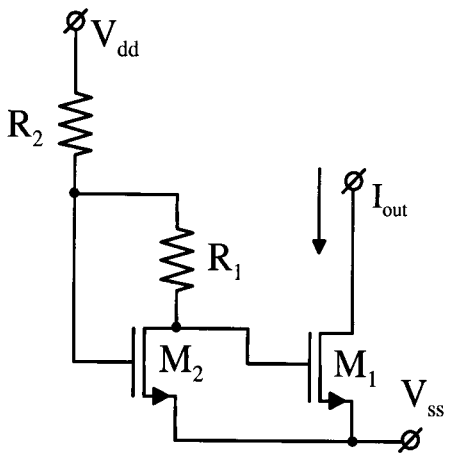

Figure 10.2: Improved gate-source voltage stabilizer

With this condition the increase in gate-source voltage of M_2 is inverted and subtracted from the gate-source voltage of M_2. The size of the output transistor must be increased to obtain the same output current as is applied at the input. Furthermore this system can only be applied in case a large g_m of transistor M_2 can be designed at reasonable drain current. The voltage drop across R_1 can be so large that this transistor operates in the triode region and then no output current can be generated by M_1. This means that a limited application range for this circuit is found.

10.3 Basic band-gap reference voltage source

The basic band-gap voltage stabilizer is shown in Figure 10.3. It consists of a current source with a well-determined temperature relation, a resistor R and a transistor that is switched as a diode. The output voltage of the system is generated across the resistor R and the transistor T_1. The temperature dependence of the current source I_T is given by:

$$\frac{1}{I_T}\frac{dI_T}{dT} = \frac{1}{T}. \tag{10.3}$$

The output voltage of the system which is made nearly temperature independent is given by:

$$V_{out} = RI_T + V_{be}. \tag{10.4}$$

In the following simplified analysis we assume that the base current of the transistor can be ignored with respect to the collector current. This simpli-

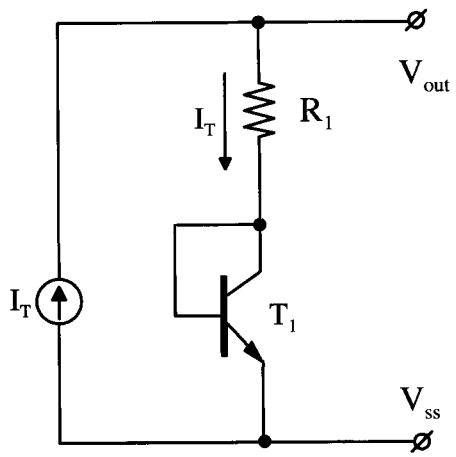

Figure 10.3: Basic band-gap voltage reference source

fication does not change the results considerably and makes it much easier to understand the operation of the system. The basic idea behind the band-gap voltage stabilization is the following: With increasing temperature it is known that the base-emitter voltage of a transistor decreases. At the same time, the positive temperature coefficient of the current source I_T generates a voltage across resistor R that increases linearly with temperature. The output voltage of the circuit can be adjusted to a value that is nearly equal to the band-gap voltage of silicon. The decrease in base-emitter voltage in that case is compensated by the increase in the voltage across the resistor R.

It is known that for a bipolar transistor the following equation is valid for the relation between collector current and base-emitter voltage:

$$I_c = I_0(e^{\frac{q}{kT}V_{be}} - 1). \tag{10.5}$$

I_0 is the base-emitter reverse current. The temperature relation for I_0 can be expressed in the following parameters:

$$I_0 = CT^n e^{-\frac{qV_g}{kT}}. \tag{10.6}$$

In equation 10.6 the value of V_g is given by the band-gap voltage of silicon which is equal to 1.208 V. In silicon n is approximately 1.4 and C is a constant depending on the size of the device.

If we assume that $e^{\frac{q}{kT}V_{be}} \gg 1$, then we can approximate equation 10.5 and equation 10.6 by:

$$I_c = CT^n e^{\frac{q}{kT}(V_{be}-V_g)}. \tag{10.7}$$

After differentiation of equation 10.7 with respect to temperature we obtain:

$$\begin{aligned} dI_c = {} & CnT^{n-1}e^{\frac{q}{kT}(V_{be}-V_g)}dT - \\ & CT^n e^{\frac{q}{kT}(V_{be}-V_g)}\frac{q(V_{be}-V_g)}{kT}\frac{dT}{T} + \\ & CT^n\frac{q}{kT}e^{\frac{q}{kT}(V_{be}-V_g)}dV_{be}. \end{aligned} \tag{10.8}$$

This equation can be simplified using the expression given in equation 10.7. After the insertion we obtain:

$$dI_c = \frac{n}{T}I_c dT - \frac{q}{kT}I_c\frac{V_{be}-V_g}{T}dT + \frac{q}{kT}I_c dV_{be}. \tag{10.9}$$

With a negligible base current of the transistor, the collector current variation now equals the variation of the current source I_T. By inserting equation 10.3 into equation 10.9 we end up with the following relation for the temperature dependence of the base-emitter voltage of the transistor:

$$\frac{dV_{be}}{dT} = \frac{k}{q}(1-n) + \frac{V_{be}-V_g}{T}. \tag{10.10}$$

The temperature relation of the output voltage V_{out} can be expressed in the following terms, assuming that R is temperature-independent:

$$\frac{dV_{out}}{dT} = R\frac{dI_T}{dT} + \frac{dV_{be}}{dT}. \tag{10.11}$$

Inserting equation 10.3 and equation 10.10 into equation 10.11 results in, after rearrangement of the terms:

$$\frac{dV_{out}}{dT} = \frac{I_T R}{T} + \frac{k}{q}(1-n) + \frac{V_{be}-V_g}{T}. \tag{10.12}$$

The output voltage of the reference source can be adjusted in such a way that at $T = T_0$ the temperature coefficient of the reference source $\frac{dV_{out}}{dT} = 0$. The following value for the output voltage at $T = T_0$ is obtained:

$$V_{out}(T = T_0) = V_{beT_0} + I_{T0}R = V_g - \frac{kT_0}{q}(1-n). \tag{10.13}$$

The remarkable point is now obtained that at $T = T_0$ the temperature coefficient of the output voltage is zero. The temperature dependence of

the output voltage can be calculated. By substituting equation 10.13 into equation 10.12, the following result is obtained:

$$\frac{dV_{out}}{dT} = \frac{k}{q}(1-n)(1-\frac{T}{T_0}). \tag{10.14}$$

This equation shows that there is a change in sign of the temperature coefficient of the output voltage around $T = T_0$.

After integration of equation 10.14 we obtain an expression for the output voltage of the band-gap reference source as a function of temperature T. The integration and substitution of the boundary conditions result in:

$$V_{out}(T) = V_g - \frac{k}{q}T(1-n)(1-\ln\frac{T}{T_0}). \tag{10.15}$$

The expression given in equation 10.15 represents a parabolic temperature dependence around $T = T_0$. The temperature dependence of the reference source as expressed by equation 10.15 is calculated, and the result is shown in Figure 10.4.

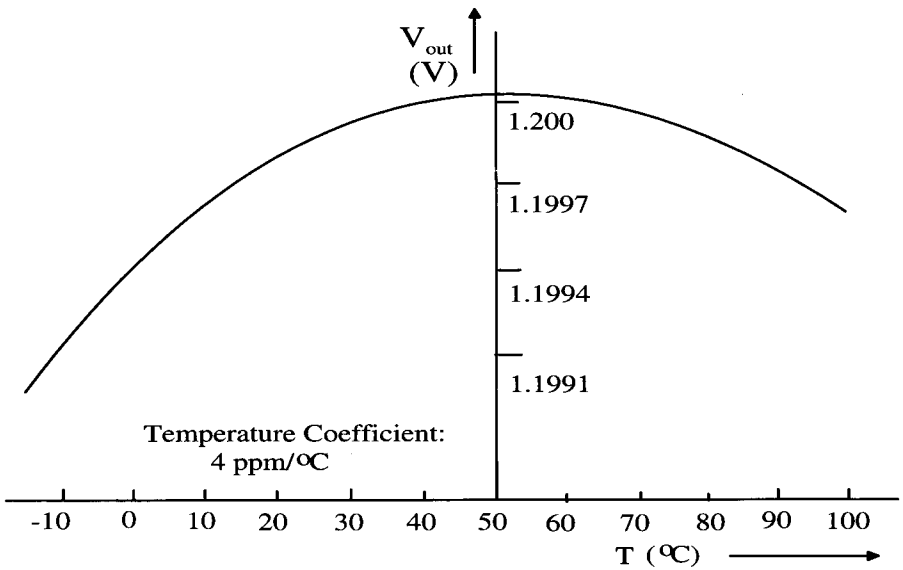

Figure 10.4: Temperature dependence of a band-gap reference source

10.3.1 Practical band-gap voltage source

A practical circuit implementation of a voltage source is shown in Figure 10.5 [77]. In MOS technologies only substrate bipolar PNP transistors are available. This means that the collectors of these transistors are connected to substrate and thus V_{ss}. The circuit consists of PNP transistors T_1 and

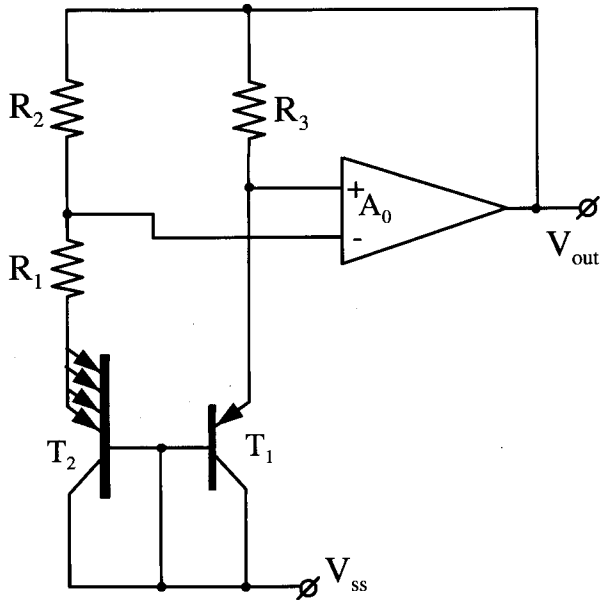

Figure 10.5: Practical band-gap reference source

T_2 with an emitter ratio of p, resistor $R1$, an operational amplifier A_0 and two equal resistors R_2 and R_3. The operational amplifier controls the output voltage in such a way that equal currents will flow through T_1 and T_2 ($R_2 = R_3$). The offset voltage of the operational amplifier must be small to obtain an accurate current ratio of one for the currents flowing through T_1 and T_2. In some cases chopper stabilization of the offset might be required. The output voltage is generated across the base-emitter voltage of T_1 plus the voltage across resistor R_3. The voltage across the resistor R_3 is linearly increasing with temperature, while the base-emitter voltage of transistor T_1 nearly linearly decreases with temperature. A cancelation of both temperature effects can be obtained with a proper adjustment of the resistor R_1. The current flowing in the circuit is determined by:

$$I_{R1} = \frac{kT}{qR_1}\ln(p). \tag{10.16}$$

With p the ratio in emitter areas between transistor T_2 and T_1. Mostly p is between 4 to 8. This results in a practical optimum for the voltage drop across R_1. Because $R_2 = R_3$ the current through T_2 is equal to the current flowing through T_1. Equation 10.16 shows that the current increases linearly with temperature.
When the output voltage is adjusted to:

$$V_{out}(T = T_0) = V_g + (n-1)\frac{kT_0}{q}, \tag{10.17}$$

then the parabolic temperature dependence of the band-gap source is found.

10.4 Conclusion

In MOS integrated circuits accurate and stable reference sources can be designed. These reference sources use the band-gap of silicon as the reference voltage. As bipolar devices substrate PNP transistors can only be used having no free collector terminals. This limits the number of applicable designs. The band-gap voltage is nearly temperature-independent. The noise performance of band-gap circuits is good, but improvements are still necessary to be able to apply these reference sources in wide band, high-resolution converters.

Chapter 11

Limitations of comparators

11.1 Signal delay in limiting amplifiers

11.1.1 Introduction

In most A/D converters the input signal is applied to an amplitude-limiting circuit. This amplitude-limiting circuit can be a differential amplifier stage or the input stage of a comparator. The amplitude of the input signal is usually much larger than the linear range of the input amplifier stages. In this way a limitation of signals for the individual amplifier stages occurs. This amplitude limitation results in variations of the delay times of the zero crossings of the differential stages. This can be explained in the following way. When a sine wave is applied at the input of the A/D converter, it looks as if this sine wave is cut into pieces with a variable slope. This slope depends on the level at which the input signal is equal to a reference voltage level. The variable slope introduces a variable delay of the zero crossing of the output signal. These delays are accordingly signal-slope-dependent. As a result, a nonlinear distortion of the input signal occurs while it travels through the A/D converter system. The moments at which ideal amplifiers would show zero crossings are shifted in time. These time shifts result in errors in the output code of the A/D converter. This delay variation is caused by the frequency limitation which is always present in practical amplifier stages. This distortion occurs in particular in bipolar amplifier stages that have a limited linear range. MOS amplifier stages have a larger linear range because of the much higher threshold voltage of the individual devices with respect to a bipolar transistor. A simple calculation and design model will be presented in this chapter. For additional information see [59].

A/D converters which use a sample-and-hold amplifier at the input are less sensitive to this slope-dependent delay phenomenon. In reference [60] the improvements in performance of flash-type A/D converters proceeded by a high-speed sample-and-hold amplifier are shown. The time constant with which the sampling of the analog signals occurs can be made smaller than is the case with the large number of amplifier stages used in parallel or folding types of converters.

When master-slave flip-flops are used as clocked comparators, it is very important to know the sensitivity of such a comparator. Furthermore, the number of meta-stable conditions such a comparator can have determines the errors an analog-to-digital converter introduces as a function of time. A meta-stable condition is defined as the output signal a comparator obtains after a well-defined comparison time and cannot be used as a logical "1" or "0". The encoding logic under such a condition does not give a unique output code, which results in quantization errors. A simple model of the master-slave flip-flop is used to calculate these meta-stable conditions and the design criteria needed to overcome these problems. Basically this method can be applied for a bipolar as well as a MOS technology.

11.2 Definition of the delay problem

In a flash-type A/D converter usually the input signal amplitude is much larger than the linear range of the individual input amplifiers or the input stages of a clocked comparator. The input stages are over-driven by the input signal, and the zero crossings at the outputs of the amplifiers-comparators are delayed in time. In Figure 11.1 the input signal is shown with the reference voltages V_{refn} drawn at the moment the sine wave amplitude equals the input signal level. In the circle the nonlinear input characteristic of the input amplifier-comparator stage is shown. Here V_{lin} is the linear range of the amplifier stage. Depending on the level of the zero crossing, the shaped ramp function which can be used to model the system shows a signal level dependent slope with a maximum around the mid value of the sine wave and a minimum slope in the tops and valleys of the sine wave. This graphic approach to the over-drive of amplifier-comparator stages leads to a simple calculation model to analyze the behavior of these stages as a function of input frequency and signal level.

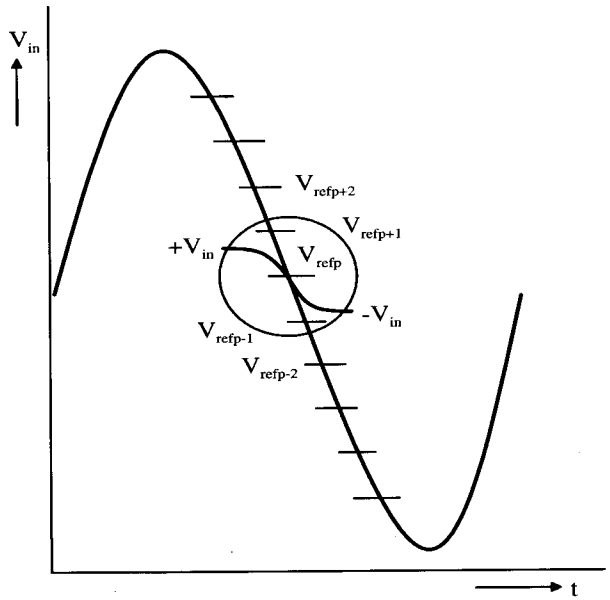

Figure 11.1: Over-drive model of a flash converter

11.3 Delay calculation model

A simple model that represents the nonlinear behavior of an amplifier pair with a frequency-limiting circuit is modeled in Figure 11.2. The model consists of an amplitude-limiting stage followed by a bandwidth-limiting circuit. The amplitude-limiting circuit is modeled by a linear transfer curve that saturates on both sides without any smooth transitions. Although practical amplifier stages show a certain smoothing in saturation, this simple model

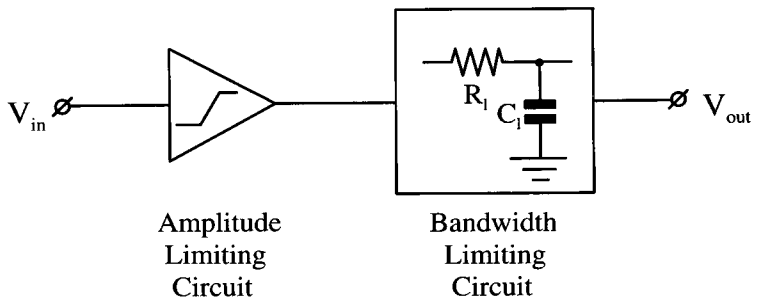

Figure 11.2: Simple nonlinear model of a limiting amplifier stage

turns out to be good enough for understanding the problem and deriving design requirements for the amplifiers. The bandwidth limitation is modeled by a simple *RC* network. Now assume that the input signal is increasing with a constant slope within the linear region of the amplitude-limiting circuit. Then the first part of the output signal of the *RC* network equals the response of an *RC* network to a ramp function (see Figure 11.3). After the

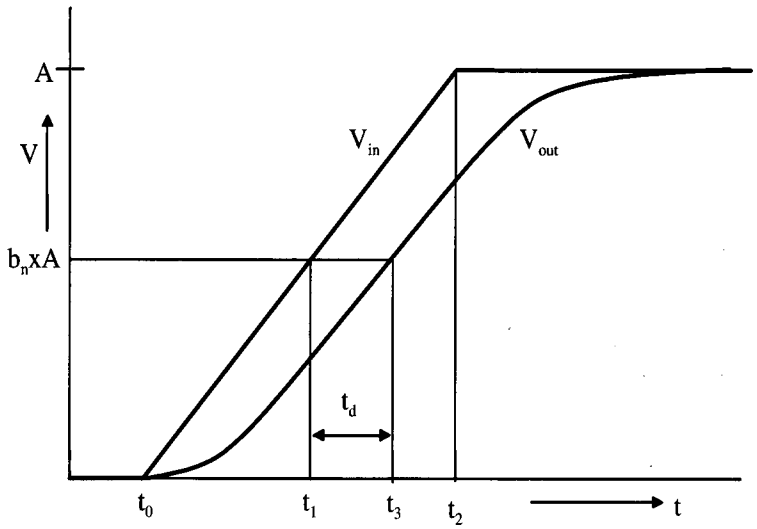

Figure 11.3: Output signal of an amplitude-limiting circuit with a ramp input signal

output signal of the amplitude-limiting circuit reaches its maximum value, the output of the *RC* network equals the response to a step function. During normal operation of an A/D converter, the input signal source, which can be a sine wave, over-drives the differential comparator amplifier stages. When the input signal passes a differential stage at the zero crossing of the signal, a waveform like an input step is applied to the *RC* network. The delay in this case equals the response of an *RC* network to a step input signal. This delay, at half the output signal value, equals about 0.7 *RC*. When the input signal reaches the tips of the sine wave, a signal that can be modeled by a ramp signal is applied to the *RC* network. In this case the delay will become *RC*. The result of this operation is that, depending on the slope of the input signal, the output zero crossings will have a variable delay, which changes from $0.7RC$ to *RC* when the signal changes from maximum to minimum slope. The input slope variations occur because at the high

end frequency range a sine wave is always compared with the reference levels. The anti-alias filter, which must precede a practical converter to avoid aliasing, performs this signal filtering. This variable delay will cause signal distortion, which is not allowed. A more exact analysis of this phenomenon will be presented in the next section.

11.4 Variable delay calculation

In a practical situation a step input response is never obtained. Therefore, a ramp with variable slope is used to model the limited input signal. Using Figure 11.3, the following notations for the variable signal delay are used:

V_{in} input signal
V_{fs} full-scale value of the A/D converter
G_A amplifier gain
$V_{lr} = \frac{A}{G_A}$ input amplifier linear range
f_{in} input signal frequency
$f_b = \frac{1}{2\pi RC}$ -3 dB bandwidth of the input amplifier
$\omega = 2\pi f_{in}$
S slope of the A/D converter input signal
S_{out} slope of the output signal of the amplitude-limiting circuit
A maximum output voltage
b_n relative output voltage level at which the signal delay is determined
t_0 start time of the ramp signal
t_1 time at which the ramp signal reaches the level b_nA
t_2 time at which the output signal of the limiting stage reaches the maximum value A
t_3 time at which the output ramp-shaped signal reaches the level b_nA
$t_d = t_3 - t_1$

Suppose an input signal equal to

$$V_{in} = \frac{V_{fs}}{2} \sin \omega t \tag{11.1}$$

is applied to the input of the A/D converter. Because of the anti-alias filtering that is required at the input of an A/D converter, this sine wave is a good model for an input signal at the high end of the input frequency band. The slope of the signal depends on the level at which the reference level crossing occurs. After differentiating the input signal, we obtain for

the slope of the signal

$$S = \frac{V_{fs}}{2}\omega \cos \omega t. \tag{11.2}$$

The input slope is increased by the gain factor G_A of the amplifier/limiter circuit. As a result, the output slope that is applied to the RC network becomes

$$S_{out} = G_A \frac{V_{fs}}{2}\omega \cos \omega t. \tag{11.3}$$

The output slope of the amplitude-limiting circuit can be compared with the slope of the ramp function of Figure 11.3. This means that:

$$G_A \frac{V_{fs}}{2}\omega \cos \omega t = \frac{A}{t_2 - t_0}. \tag{11.4}$$

The value of $\frac{A}{G_A}$ can be replaced by the linear input voltage range of the amplifier v_{lr}, so then equation 11.4 can be rearranged into:

$$t_2 - t_0 = \frac{2V_{lr}}{V_{fs}\omega \cos \omega t}. \tag{11.5}$$

With the use of Laplace transforms, the response of the ramp signal applied to the RC network can be calculated. We obtain using the notations of Figure 11.3:

$$V_{out}(t) = (\frac{t - t_0}{t_2 - t_0}A - \frac{RC}{t_2 - t_0}A(1 - e^{-\frac{t-t_0}{RC}}))U(t - t_0) \tag{11.6}$$

$$-(\frac{t - t_2}{t_2 - t_0}A - \frac{RC}{t_2 - t_0}A(1 - e^{-\frac{t-t_2}{RC}}))U(t - t_2). \tag{11.7}$$

In this equation $U(t - t_0)$ is the unit step response. The time delay t_d between the input and output ramp signal can be expressed in the circuit parameters when the output signal crosses the amplitude level $b_n A$.

After some rearranging and inserting $t = t_3$ we obtain:

$$b_n(t_2 - t_0) = (t_3 - t_0 - RC(1 - e^{-\frac{t_3-t_0}{RC}}))U(t_3 - t_0) \tag{11.8}$$

$$-(t_3 - t_2 - RC(1 - e^{-\frac{t_3-t_2}{RC}}))U(t_3 - t_2). \tag{11.9}$$

The time t_3 can be expressed as follows:

$$t_3 = t_0 + b_n(t_2 - t_0) + t_d. \tag{11.10}$$

Depending on the value of the time t_3, two cases can be distinguished:

1. $t_3 < t_2$, and
2. $t_3 \geq t_2$.

Inserting the boundary value $t_3 < t_2$ into equation 11.10 results in:

$$t_2 - t_0 > \frac{t_d}{1 - b_n}. \tag{11.11}$$

Combining equation 11.5 and equation 11.11 and rearranging results in:

$$\frac{t_d}{RC} < 2(1 - b_n)\frac{V_{lr} f_b}{V_{fs} f_{in}}. \tag{11.12}$$

Equation 11.12 determines the switching between case 1) and case 2). Suppose $t_3 < t_2$, then only equation 11.8 is valid to express the output voltage. Inserting equation 11.10 into equation 11.8 results in:

$$t_d = RC(1 - e^{-\frac{b_n(t_2-t_0)+t_d}{RC}}). \tag{11.13}$$

When $\cos \omega t$ equals 0 or 1, then using equation 11.4 a value for $t_2 - t_0$ of ∞ or $\frac{2V_{lr}}{V_{fs}\omega}$ is obtained, respectively. Inserting the value of ∞ for $t_2 - t_0$ into equation 11.13 gives:

$$t_d = RC. \tag{11.14}$$

Now an estimate of the switching point between case 1) and case 2) can be made. Inserting equation 11.14 into equation 11.12 gives the estimate:

$$\frac{f_{in}}{f_b} < 2(1 - b_n)\frac{V_{lr}}{V_{fs}}. \tag{11.15}$$

When the slope of the input signal varies, the interesting parameter is the variation of the delay time with respect to the slope of the signal. Define:

$$t_d = RC - \delta t_d. \tag{11.16}$$

Proceed with case 1): Substitution of equation 11.16 into equation 11.13 results in the following relation between the input signal and the delay variation δt_d:

$$\delta t_d = RC e^{-\frac{2b_n V_{lr}}{V_{fs} RC\omega \cos \omega t} + \frac{\delta t_d}{RC} - 1}. \tag{11.17}$$

In Figure 11.4 the variation of the delay as a function of the input signal slope is shown. In the figure V_{in} represents the input sine wave which is offsetted by 0.5 V at which level the maximum slope is found. 0 and 1.0 V

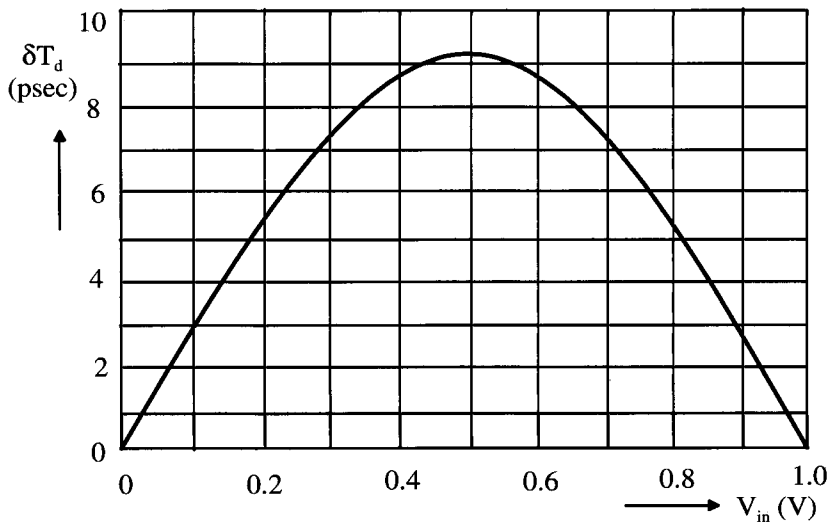

Figure 11.4: Variation of the delay as a function of the input signal

are the bottom and top parts of the sine wave, respectively. The following values for the different parameters are substituted: RC = 200 psec
$b_n = .5$
$V_{lr} = 140$ mV
$V_{fs} = 1$ V
$\omega = 2\pi 50MHz.$
Inserting $\cos \omega t = 1$ into equation 11.17 results in a simplified expression for the maximum delay variation:

$$\delta t_d = RCe^{-2b_n \frac{V_{lr} f_b}{V_{fs} f_{in}} + \frac{\delta t_d}{RC} - 1}. \tag{11.18}$$

A further useful simplification is introduced by replacing $\frac{\delta t_d}{RC}$ by the normalized delay variation g. Then equation 11.18 becomes:

$$g = e^{-2b_n \frac{V_{lr} f_b}{V_{fs} f_{in}} + g - 1}. \tag{11.19}$$

From equation 11.19 the following can be concluded for a minimum delay variation:

1. The linear range V_{lr} of the input amplifier must be large.
2. A large amplifier bandwidth f_b is needed.

3. A small full scale range of the converter is needed.

The linear range V_{lr} of an amplifier is determined by the technology used. In a bipolar system without using emitter degeneration elements a linear range of about 120 to 180 mV is obtained. In MOS devices this linear range depends on the threshold voltage of the devices.

The bandwidth of a system is mostly determined by the dc bias condition of the amplifier stage. A large bias current results in a large power dissipation. Due to the complexity of the overall system, bias currents must be kept within certain limits, preventing the power dissipation of the total circuit from growing to excessive values. A small-size high-frequency technology is needed to increase the analog bandwidth of the amplifier system. The minimum full-scale range of the converter is determined by the resolution and the matching of the input devices of the input amplifier. In bipolar devices in general a much better matching is obtained than is possible in an MOS technology. On the other hand, the noise generated in the input amplifiers determines the minimum tap spacing in a converter. In practice a minimum full-scale value of 1 V can be used for an 8-bit converter.
To solve the implicit equation 11.19 a computer program is needed. However, it is possible to simplify equation 11.19 by putting g $\ll$ 1:

$$g \approx e^{-2b_n \frac{V_{lr} f_b}{V_{fs} f_{in}} - 1}. \tag{11.20}$$

Proceeding to case 2), the combined equation for the output voltage $V_{out}(t)$ to reach the crossing point $b_n A$ is obtained by adding equations 11.8 and 11.9. The result becomes:

$$(1 - b_n)(t_2 - t_0) = RC(e^{-\frac{t_3 - t_2}{RC}} - e^{-\frac{t_3 - t_0}{RC}}). \tag{11.21}$$

Inserting equation 11.10 for t_3, we obtain:

$$(1 - b_n)(t_2 - t_0) = RC(e^{\frac{t_2 - t_0}{RC}} - 1)e^{-\frac{b_n(t_2 - t_0) + t_d}{RC}}. \tag{11.22}$$

Rearranging the terms in equation 11.22 results in:

$$e^{-\frac{t_d}{RC}} = (1 - b_n)(\frac{t_2 - t_0}{RC} e^{b_n \frac{t_2 - t_0}{RC}} (e^{\frac{t_2 - t_0}{RC}} - 1)^{-1}. \tag{11.23}$$

The limit value of $\frac{t_d}{RC}$ when t_2 reaches t_0 equals:

$$\frac{t_d}{RC} = -\ln(1 - b_n). \tag{11.24}$$

Inserting a value of 0.5 for b_n gives $t_d = RC\ln(2)$. This value equals the delay of an RC time constant on a unity step response as expected.
A further simplification of formula 11.23 is obtained by inserting equation 11.16 and equation 11.5 for $\cos\omega t = 1$. After rearranging the terms we obtain for a maximum in the normalized delay variation:

$$g = 1 - \ln(e^{2\frac{V_{lr}f_b}{V_{fs}f_{in}}} - 1) + 2b_n\frac{Vlrf_b}{V_{fs}f_{in}} + \ln(2(1-b_n)\frac{Vlrf_b}{V_{fs}f_{in}}). \qquad (11.25)$$

In Figure 11.5 the normalized delay variation ($g = \frac{\delta t_d}{RC}$) for the combination of case a) and b) are shown as a function of the ratio between the amplifier bandwidth and the input frequency. The ratio between full-scale value and the linear range (V_{fs}/V_{lr}) is inserted as a parameter. This model is verified

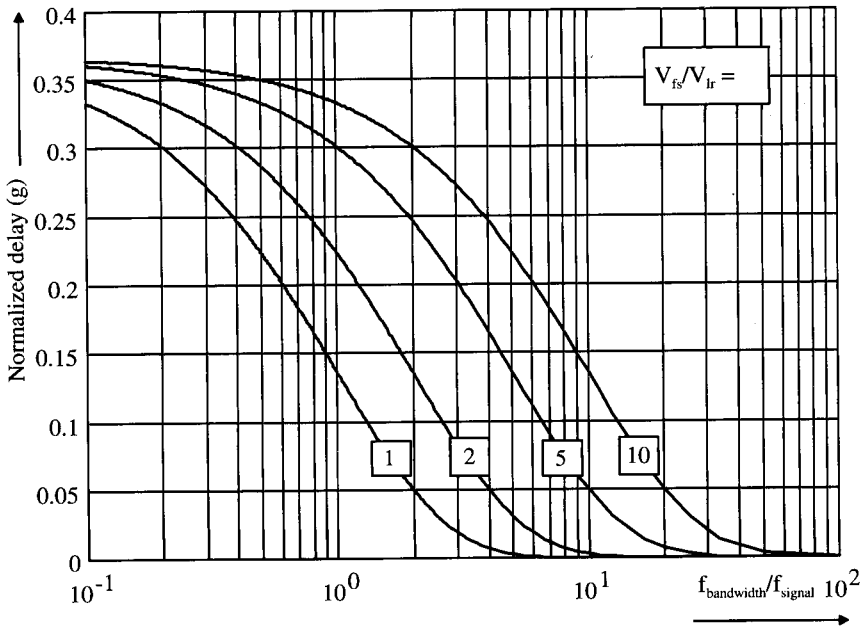

Figure 11.5: Total normalized delay variation as a function of input amplifier bandwidth/input frequency

by extensive simulations at transistor level of chords of input amplifiers performing an A/D input signal operation.
These results can be used in an equation which will determine the third-order distortion in the converter system. This equation will be evaluated in

the next section.

11.5 Distortion calculation

Suppose an input signal $V_{in} = \sin(\omega t + \psi)$ is applied at the input of the converter. In this formula ψ is an arbitrary phase shift introduced at the input to compensate for the various delays in the converter system. This phase shift is constant and independent of the slope of the input signal. At the output of the converter a digitized signal is found that obeys the following equation:

$$V_{out} = \sin(\omega(t + \delta t)). \qquad (11.26)$$

From Fig 11.4 it can be seen that a good approximation for the delay difference δt_d as a function of the input frequency is:

$$\delta t \cong -\delta t_d \mid \cos\omega t \mid . \qquad (11.27)$$

The absolute value for the cosine is inserted because regardless of the signal polarity the delay must have the same sign. In Figure 11.6 the input sine wave is shown that is applied to the signal dependent delay function of the amplifier. The delay function is normalized for zero variations at the tops of the sine wave. This results in a negative delay for the mid-points of the sine wave as shown in the figure. At the output of the system a sine wave appears with timing errors equal to the δt_d curve. The expectation of this shifting of the time axis of the sine wave is a third-order distortion. When the input signal is subtracted from the time shifted output curve then the result shown in Figure 11.7 is obtained. The error signal contains still an important part of the input fundamental sine wave. When an amplitude and phase adjustment is applied during the subtraction of the input signal from the time shifted output signal then the result shown in Figure 11.8 is obtained. From this figure it is clear that a dominant third order distortion is obtained. This third-order distortion will be calculated now. Inserting equation 11.27 into equation 11.26 results in:

$$V_{out} = \sin\omega t\cos(\omega\delta t_d \mid \cos\omega t \mid) - \cos\omega t\sin(\omega\delta t_d \mid \cos\omega t \mid). \qquad (11.28)$$

Equation 11.28 can be simplified using series expansion and assuming that δt_d is small with respect to t. When only the first-order terms in the series expansion are used, equation 11.28 becomes:

$$V_{out} = \sin\omega t - \cos\omega t\omega\delta t_d \mid \cos\omega t \mid . \qquad (11.29)$$

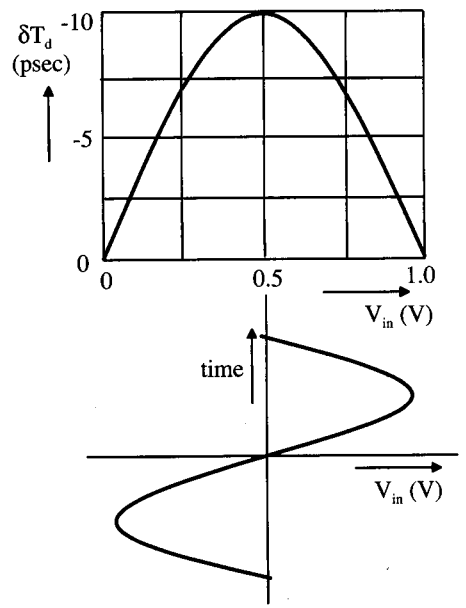

Figure 11.6: Signal shifting of the output sine wave by the signal dependent delay

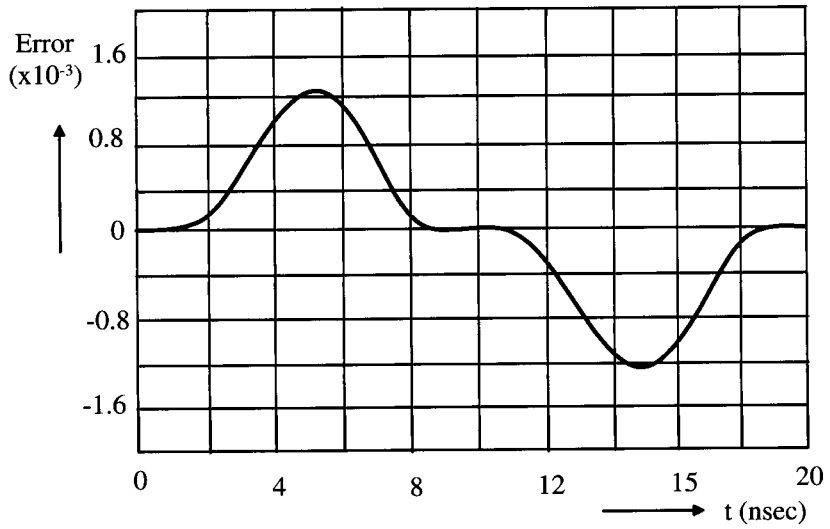

Figure 11.7: Error signal after subtraction of the input signal

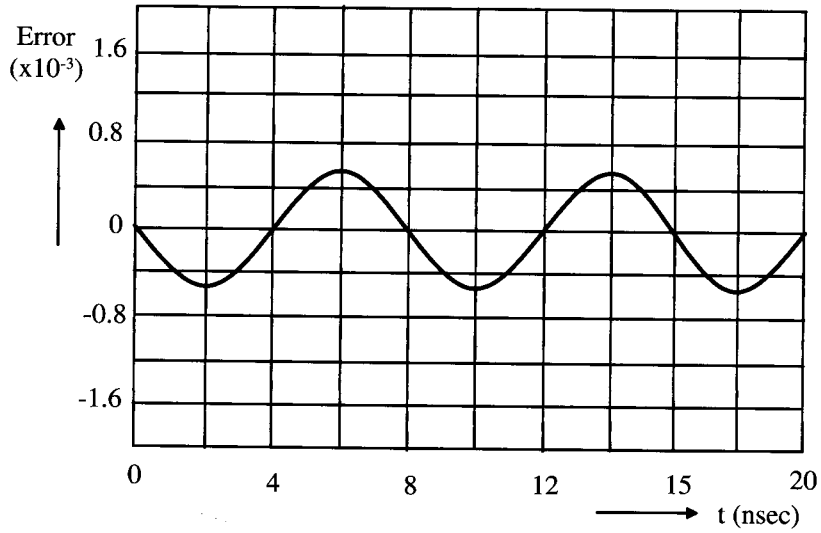

Figure 11.8: Error signal after subtraction using an amplitude adjustment

A further simplification is obtained when $|\cos\omega t|$ is expressed in a Fourier series. We obtain:

$$|\cos\omega t| \simeq \frac{2}{\pi} + \frac{4}{3\pi}\cos 2\omega t. \tag{11.30}$$

Substitution of the series expansion from equation 11.30 into equation 11.29 results in:

$$V_{out} = \sin\omega t + \frac{2}{\pi}\omega\delta t_d \cos\omega t + \frac{4}{3\pi}\omega\delta t_d \cos\omega t \cos 2\omega t. \tag{11.31}$$

Reworking the product of $\cos\omega t$ and $\cos 2\omega t$ into a sum of cosine terms gives:

$$\frac{2}{3\pi}\omega\delta t_d \cos\omega t + \frac{2}{3\pi}\omega\delta t_d \cos 3\omega t. \tag{11.32}$$

Inserting this simplification into equation 11.31 results in:

$$V_{out} = \sin\omega t + \frac{8}{3\pi}\omega\delta t_d \cos\omega t + \frac{2}{3\pi}\omega\delta t_d \cos 3\omega t. \tag{11.33}$$

From equation 11.33 it is shown that the signal-dependent delay results in a third-order distortion of the input signal after the conversion takes place in an absolutely linear A/D converter.

The small cosine term can be included in the sine wave expression by substituting $\tan\eta = \frac{8}{3\pi}\omega\delta t_d$. This results in a small phase shift of the sine term; we obtain:

$$V_{out} = \sqrt{\tan^2\eta + 1}\sin(\omega t + \eta) + \frac{2gf_{in}}{3\pi f_b}\cos 3\omega t. \qquad (11.34)$$

The third-order term is a direct expression for the distortion in the A/D converter. In Figure 11.9 the distortion as a function of the ratio $\frac{f_b}{f_{in}}$ is shown. This curve gives a general insight into the effective bits of a converter as a function of the ratio bandwidth/input signal frequency. Care must

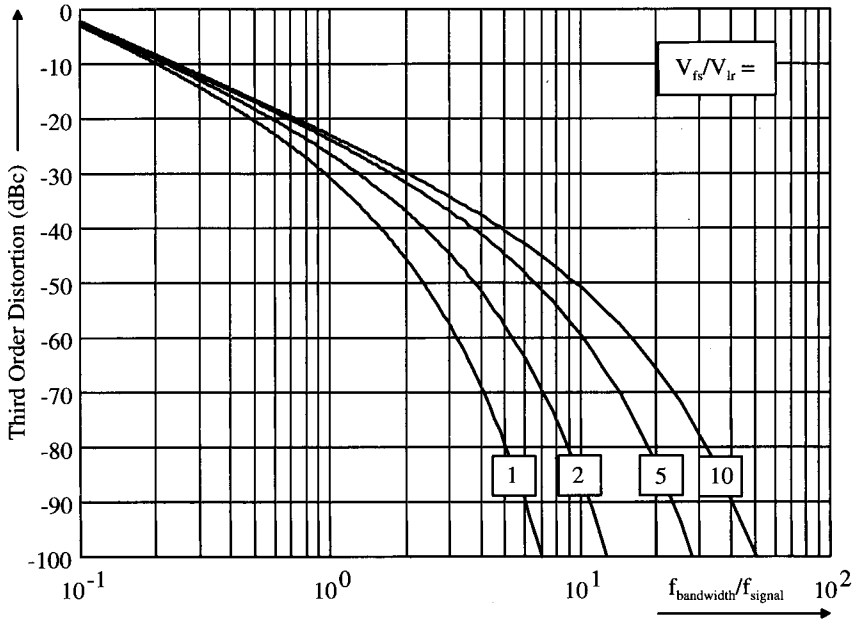

Figure 11.9: Total distortion versus bandwidth/input frequency ratio of an A/D converter

be taken in using the total distortion equation at the high-frequency end limit. It must be verified that the comparators or amplifiers at those high frequencies settle to the final signal value. Otherwise wrong conclusions are drawn.

11.6 Failure analysis of comparators

When flip-flops are used as comparators, at the beginning of a decision cycle the input signal can be so small that at the end of the decision cycle no digital "1" or "0" value is obtained. Such a condition is called a meta-stable state (MSS) [12]. In Figure 11.10 a generalized curve showing the two logical states V_1 and V_2 and the meta-stable state of a flip-flop are shown. During the design of comparators it is very useful to obtain a criterion that

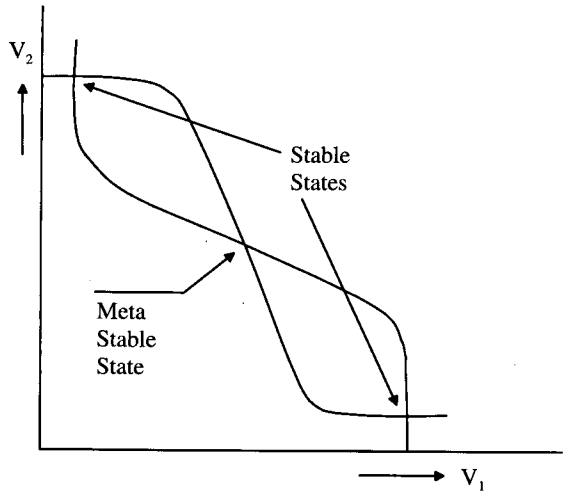

Figure 11.10: States of a flip-flop used as a comparator

determines the number of times such a state occurs. An analysis will be given that determines the failure rate of a comparator with respect to the sample frequency and the unity gain bandwidth of the amplifiers used in the flip-flop. Noise in the system is supposed to have basically no influence on the number of meta-stable states of the comparators. Using the superposition principle the noise can be referred to the input of the circuit and adds to the input signal. In this way a disturbance of the comparison by noise is obtained but no influence on the number of meta-stable states is found.

11.6.1 First-order model of a flip-flop

In a first approximation a flip-flop can be modeled as two positively feedbacked first-order amplifiers. The small signal model is shown in Figure 11.11. The amplifier stages are modeled as inverters with a gain $-A$ and a time constant $\tau = RC$. Using feedback theory, the condition for "os-

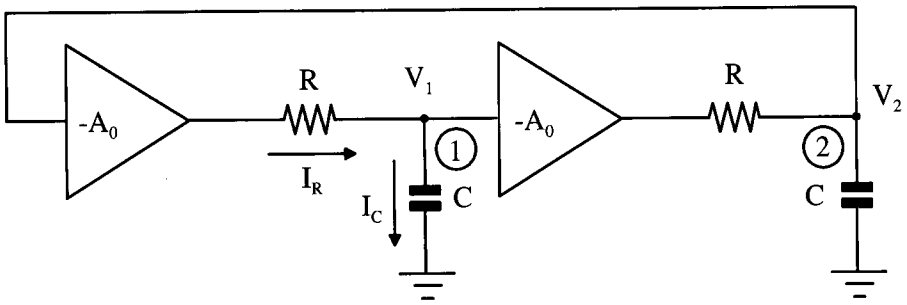

Figure 11.11: Small signal model of a flip-flop

cillation" can be used to determine the meta-stable condition. This results in:

$$1 - A^2 = 0. \tag{11.35}$$

In equation 11.35 A is expressed as:

$$A = \frac{A_0}{1 + s\tau}. \tag{11.36}$$

In solving equation 11.35 with respect to time, the following general relations are found:

$$V_1 = \lambda_1 e^{\frac{A_0-1}{\tau}t} + \lambda_2 e^{-\frac{A_0+1}{\tau}t} \tag{11.37}$$

and

$$V_2 = -\lambda_1 e^{\frac{A_0-1}{\tau}t} + \lambda_2 e^{-\frac{A_0+1}{\tau}t}. \tag{11.38}$$

V_1 and V_2 are the output voltages of amplifiers 1 and 2, respectively. In these equations λ_1 and λ_2 are integration constants. These constants can be determined by inserting the initial conditions at $t = 0$ into equations 11.37 and 11.38. These initial conditions are:

$$V_1 = V_{01} = \lambda_1 + \lambda_2 \tag{11.39}$$

and

$$V_2 = V_{02} = -\lambda_1 + \lambda_2. \tag{11.40}$$

In solving λ_1 and λ_2 from equations 11.39 and 11.40, the following result is obtained:

$$\lambda_1 = \frac{V_{01} - V_{02}}{2} \tag{11.41}$$

and

$$\lambda_2 = \frac{V_{01} + V_{02}}{2}. \tag{11.42}$$

Furthermore, by analyzing equations 11.37 and 11.38 with increasing time t, only the terms with the positive exponent show an increase in signal. Putting

$$V_{01} - V_{02} = 2\delta V_0, \tag{11.43}$$

the solutions for the dominating output voltages can be obtained. The result is:

$$V_1 = \delta V_0 e^{\frac{A_0-1}{\tau}t} \tag{11.44}$$

and

$$V_2 = -\delta V_0 e^{\frac{A_0-1}{\tau}t}. \tag{11.45}$$

In general the input signal values δV_0 are uniformly distributed over the decision interval, the same is now found for the output signal values V_1 and V_2 after a time t_d (= decision time) has been elapsed. Note that the differences between the final states of V_1 and V_2 are equal to the logical swing V_l of the system.

This can be related to the probability that a meta-stable state occurs after the sampling time t_d:

$$P(t > t_d) = e^{-\frac{A_0-1}{\tau}t_d}. \tag{11.46}$$

Equation 11.46 is valid when one sample is taken. If we take $f_s = \frac{1}{t_s}$ samples, then the number of meta-stable states per second becomes:

$$M_n = f_s e^{-\frac{A_0-1}{\tau}t_d}. \tag{11.47}$$

Equation 11.47 can be rewritten into general design parameters. Mostly $t_d = \frac{t_s}{2}$ when a symmetrical clocking scheme is used. During half the sampling time the flip-flop is in input position while during the second half sampling time the decision is taken. Furthermore, the time constant τ can be expressed into the unity gain bandwidth of the individual amplifiers. This results into:

$$\tau = \frac{1}{2\pi f_{3dB}} \tag{11.48}$$

and with $f_{ugb} = A_0 . f_{3dB}$ equation 11.47 can be rewritten into:

$$M_n = f_s e^{-(1-\frac{1}{A_0})\frac{f_{ugb}}{f_s}\pi}. \tag{11.49}$$

When a moderate gain is used in the amplifier stages, then equation 11.49 gives a direct relation between the unity gain bandwidth (f_{ugb}) of the amplifiers and the sampling rate which can be applied to the system. At the

moment the number of meta-stable states needs to be determined over longer time periods (1 minute, 1 hour, 1 day, or even 1 year), then equation 11.49 becomes:

$$M_n = T_p f_s e^{-(1-\frac{1}{A_0})\frac{f_{ugb}}{f_s}\pi}. \tag{11.50}$$

Here T_p is the time period over which the number of meta-stable states is determined. In equation 11.50 the relation between the unity gain bandwidth of a system and the sampling frequency is shown for different time intervals T_p. Figure 11.12 shows a very powerful relation in designing flip-flops with

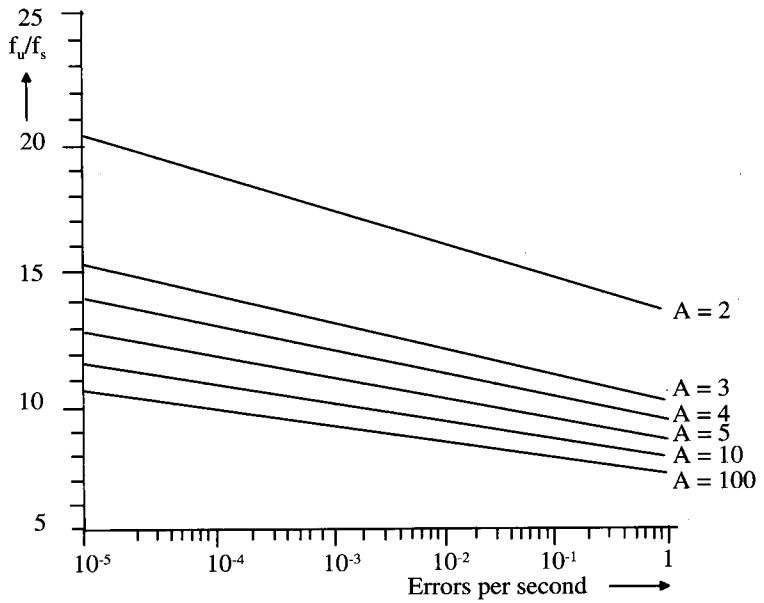

Figure 11.12: Relation between unity gain bandwidth and sampling frequency ratio and the number of meta-stable errors per second

a high decision accuracy. A sampling frequency of 1 GHz is used in the calculations.

When the tap voltage of an A/D converter is not equal to the logic swing of the output signal of the flip flop, then an extra correction of equation 11.50 is required. Suppose that the tap voltage of the A/D converter is equal to V_{tap} and the gain of the input differential amplifier during sampling of the input signal is equal to A_{dif}, then equation 11.50 must be modified into:

$$M_n = T_p f_s \frac{V_l}{A_{dif} V_{tap}} e^{-(1-\frac{1}{A_0}).\frac{f_{ugb}}{f_s}\pi} \tag{11.51}$$

In a practical application the introduced correction factor between the logical swing V_l and the tap voltage of the converter V_{tap} gives only a small modification on the result of Figure 11.12 because of the very steep exponential relationship in the formula.

11.6.2 BER simulation

In designing high-performance high-speed analog-to-digital converters the BER is an important design criterion. To optimize a comparator for this parameter it is important to obtain good simulation data. In Fig. 11.13 a setup for a simulation of the BER of a comparator circuit is shown. To

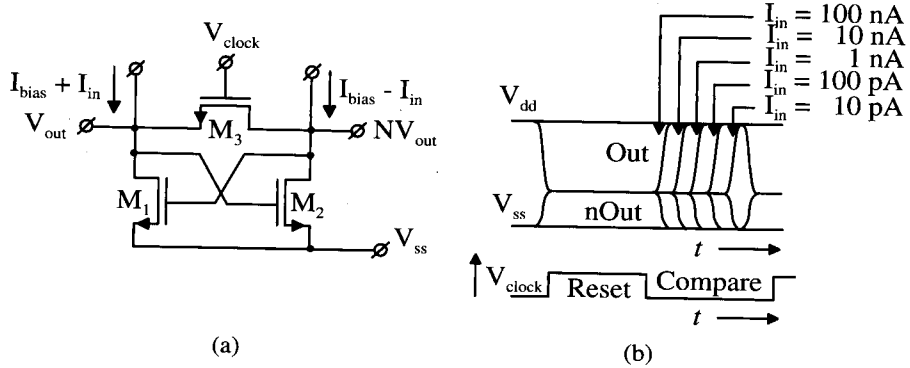

Figure 11.13: BER simulation setup

obtain convergence in the simulation all elements are exactly equal. The comparator consists of two cross-coupled transistors M_1 and M_2 with a sampling switch M_3. The sampling switch connects the drains of transistor M_1 with M_2 with a resistance equal to R_{on} of the switch M_3. The circuit is biased with the bias current sources I_{bias}. The input differential signal to be compared is specified as I_{in}. When the switch is closed, then this comparator stage is in reset mode. Opening the switch gives the regeneration condition and a very fast and accurate comparison takes place. During simulation the input current is reduced. Normally a reduction in steps of a factor 10 is used. In Fig.11.13(b) the results of a simulation with reduced input signal steps are shown. At the moment the input signal current is reduced, it takes more time to obtain an output decision for the comparator. Depending on the time available for comparison an extrapolation can be made at what minimum input current level still a good decision is possible. The total compare time must be used for this extrapolation. Using this result, then

the BER is determined as the ratio between the maximum input (logic level) signal and the minimum input signal current to obtain a good decision. It is also possible to calculate the BER of the circuit. Using

$$V_1 = \delta V_0 e^{\frac{A_0-1}{\tau}t} \tag{11.52}$$

it is possible to determine the important factor

$$\frac{A_0 - 1}{\tau} \tag{11.53}$$

that determines the BER of the circuit. Using a ratio of 10 between the input signals δV_0 and determining from the simulation result the time difference δt a comparison result is obtained the BER determining factor becomes:

$$\frac{A_0 - 1}{\tau} = \frac{\ln(10)}{\delta t}. \tag{11.54}$$

With a comparison time t_{comp} the BER becomes:

$$BER = e^{-\frac{A_0-1}{\tau}t_{comp}}. \tag{11.55}$$

It must be noted, however, that δt must be determined at small input signal levels for the comparator.

11.7 Current mode comparator circuit

An example of a current mode comparator is shown in Fig. 11.14. The input signal to this comparator is applied at the gates of transistors M_1 and M_2. The basic comparison takes place using the cross-coupled transistor pair M_7 and M_8 with the resistive load R_1 and R_2. Switches M_3 to M_6 perform the current mode switching from amplification to decision. To simplify the understanding of the circuit the two phases used in the comparator are drawn separately in Fig. 11.15. During the input amplification phase of the comparator the input signal is amplified by transistors M_1 and M_2 and flows through the cascode devices M_3 and M_6 to the resistive loads R_1 and R_2. The amplified signal is stored on the parasitic capacitors consisting of the drain capacitance of M_3 and M_6 and the output load capacitors (not drawn) during switching from amplification to decision mode (see Fig. 11.15 (a)). During the decision phase (Fig. 11.15 (b)) the output currents of the input differential pair M_1 and M_2 are added via switches M_4 and M_5 and applied to the connected sources of the cross-coupled pair M_7 and M_8. During this

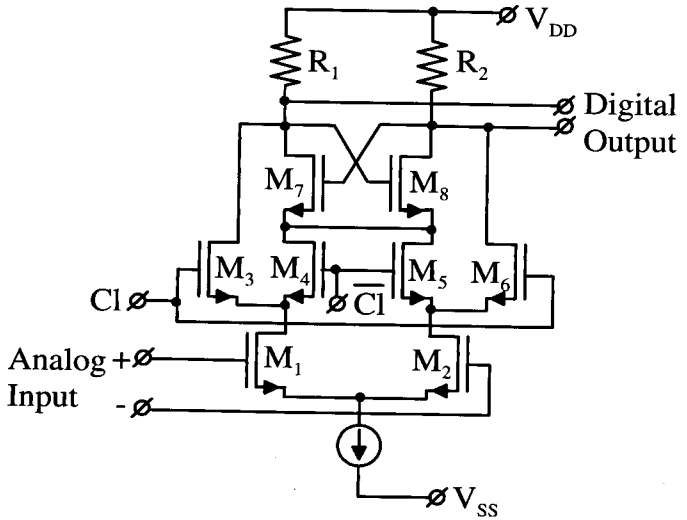

Figure 11.14: Current mode comparator circuit

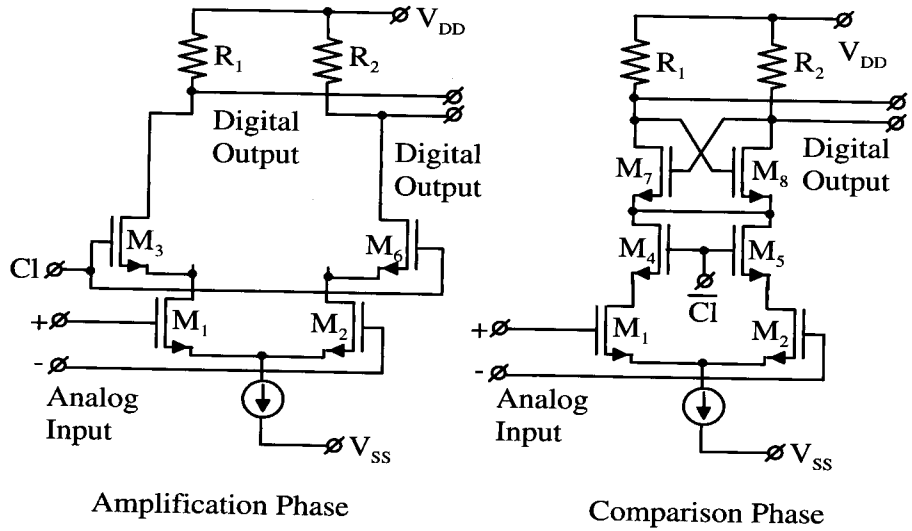

Figure 11.15: Two operational phases of the current mode comparator circuit

phase, the cross-coupling acts as a very sensitive amplifier and amplifies the difference signal stored and amplified across the load resistors R_1 and R_2 with the parasitic capacitances formed by the drains of M_7 and M_8. An output signal with a limited swing is obtained. The maximum logic swing of this circuit is:

$$V_{logic} = I_{tail} R_{1,2}. \tag{11.56}$$

Here I_{tail} is the biasing current source connected to the input differential pair. This comparator shows a good performance although a large supply voltage is required. Furthermore the limited output voltage swing might be a problem. An extra output amplifier or slave flip flop is needed to obtain CMOS logic swings. Kick-back effects from the output signal to the input signal are avoided because current mode switching is used in the drain currents of the amplifier stage.

11.8 Differential auto-zero comparator

To overcome the problems of power supply noise sensitivity of MOS comparators, a fully differential auto-zeroed comparator circuit has been designed [56]. This circuit is shown in Figure 11.16. The circuit consists of the

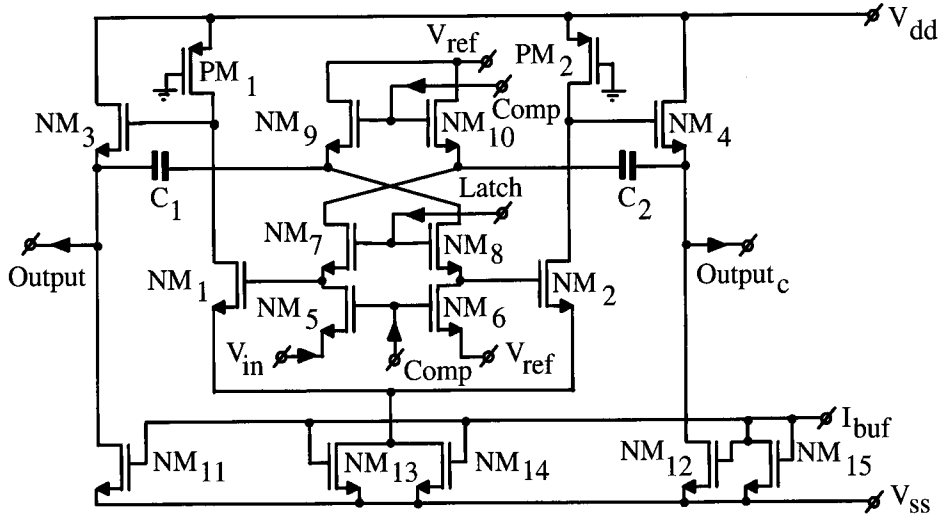

Figure 11.16: Differential auto-zero comparator circuit

input differential pair NM_1, NM_2 with the PMOS devices PM_1 and PM_2

as active loads. Switches NM_5 to NM_{10} perform the switching between amplifying and comparison mode. Furthermore, buffer stages NM_3 and NM_4 are added to reduce the loading of the storage capacitors C_1 and C_2 on the input amplifier stage NM_1 and NM_2. A continuous biasing of the system is performed. To make the understanding easier of the operation of the circuit a simplified diagram showing separately the amplifying and the latching mode are given in Figure 11.17(a, b). In analyzing Figure 11.17(a) the input

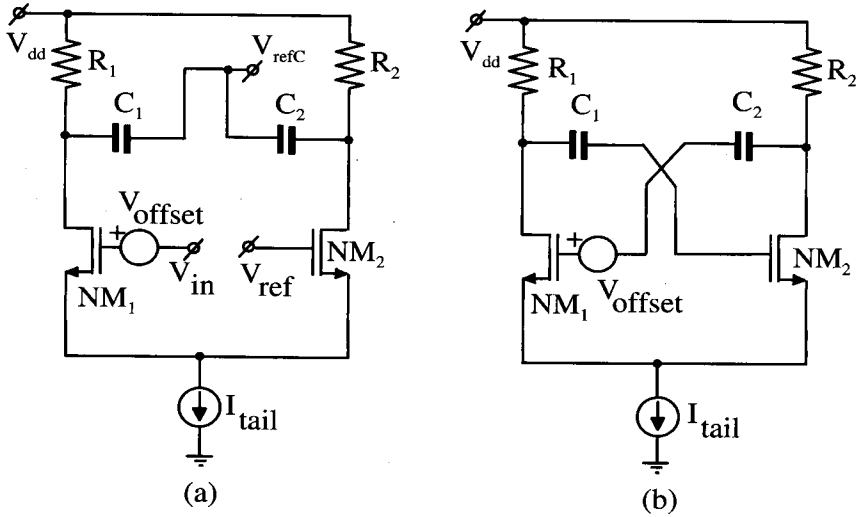

Figure 11.17: Amplification (a) and latching mode (b) of the comparator

signal plus the offset signal are amplified, and the output signal of the system is stored on capacitors C_1 and C_2. The PMOS loads are replaced by the resistors R_1 and R_2 for simplification. The bandwidth limitation that could occur because of the storage capacitors C_1 and C_2 with the load resistors has been overcome in the final circuit by implementing extra buffer stages NM_3 and NM_4 as discussed before. During the comparison mode shown in Figure 11.17(b) the input is switched off. The bottom plates of the capacitors C_1 and C_2 are cross-coupled to the input of the amplifier stage NM_1 and NM_2. In this way a flip-flop stage, which acts as a very sensitive comparator, has been obtained. Because of the cross-coupling of the capacitors, the offset voltage V_{offset} is compensated for by an identical signal stored on the capacitors. As a result, without needing an additional clock cycle

information and offset are separated and removed. A sensitive, high-speed, offset-free differential comparator stage has been obtained. In a practical situation, however, feed-through of the switches onto the capacitors gives a deterioration of the ideal offset compensation. Practical implementations show offsets between 100 μV and 1 mV.

11.9 Complementary comparator with latch

To increase speed and sensitivity many times a combination of a NMOS and PMOS comparator stage is used. A circuit implementation is shown in Fig. 11.18 [171]. The input signal is applied to the differential pair M_1 and M_2.

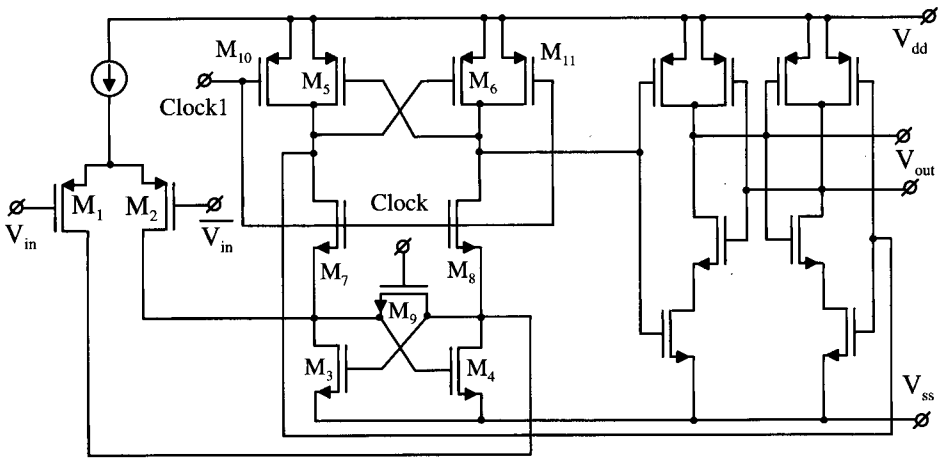

Figure 11.18: Complementary comparator with output latch [171]

This differential pair is loaded with the cross-coupled n-channel comparator stage M_3 and M_4. Transistor M_9 shorts the drains of M_3 and M_4 and resets the system. Clock and Clock1 are complementary non-overlapping clock signals. This means that with Clock high, the system is in reset mode. With Clock1 low, transistors M_7 and M_8 are switched off, so no signal is applied to the p-channel cross-coupled pair M_5 and M_6. Transistors M_{10} and M_{11} are switched on and connect the gates of M_5 and M_6 to the positive supply V_{dd}. At the moment a decision is needed, then Clock becomes low, switching off transistor M_9. Then the cross-coupled pair M_3 and M_4 start making a decision. At the same time transistors M_7 and M_8 are switched on, while transistors M_{10} and M_{11} are switched off. The p-channel cross-coupled differential pair M_5 and M_6 starts to make a decision too. This parallel

connection of the comparator stages results in a very large regeneration gain making this comparator very sensitive. However, when a decision has been obtained, then the output signals of this comparator stage equal V_{ss} and V_{dd}. This results in a large logic signal to be generated in the drains of the input pair M_1 and M_2. Such a large signal results in kick-back effects to the input of the comparator system. These signal glitches might disturb the operation of an analog-to-digital converter if no extra amplifier stages are connected in front of this unit. Furthermore during comparison a dynamic offset might be introduced due to the fact that during reset the voltages at the drain terminals of M_3 and M_4 are at $V_{gs} + V_{th}$. When the p-channel comparator stage is connected in parallel to the n-channel then the voltage levels at the drains of M_3 and M_4 can be as high as half the supply voltage applied to this system. In case the parasitic capacitance is not very well matched, then due to this voltage change a mismatch will occur influencing the decision level of the comparator. This effect is called "dynamic offset". The output signals of the comparator is applied to a set/reset flip flop to hold the information during the reset mode. Furthermore an extra gain is introduced resulting in an improvement of the BER.

11.10 Low kick back comparator implementation

To obtain a low kick back effect in comparators and at the same time having a large CMOS logic output swing the circuit shown in Fig. 11.19 can be used [126]. In this comparator system the input differential stage M_1 and M_2 is

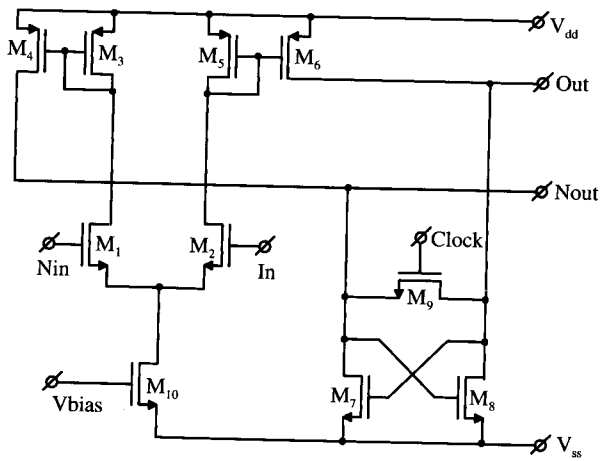

Figure 11.19: Low kick back comparator system [126]

loaded with a current mirror consisting of M_3, M_4 and M_5, M_6. The output of this current mirror is applied to the comparator stage consisting of M_7 and M_8 with the reset transistor M_9. During reset mode, transistor M_9 shorts the drains of M_7 and M_8. The output voltage is equal to the gate-source voltage of these devices. The input stage sees as a load the diode connected transistors M_3 and M_5. At the moment transistor M_9 is switched off, then the cross-coupled differential stage M_7 and M_8 start making a comparison with a large regenerative gain. As a result a CMOS output signal appears at the drains of M_7 and M_8. In case a high level is obtained then for example current mirror transistor M_6 connects the output to V_{dd}. The diode input load remains roughly at the same level with small input signals. No kick-back effect is found with this connection. Furthermore during comparison the signal levels at start conversion do not change as was the case with the previous described circuit. So no "dynamic offset" is generated. A very good performance is obtained with this comparator system.

11.11 Input frequency decision moment variation

When clocked comparators are used to quantize varying input signals, the sampling moment changes with increasing input frequencies. Usually the sampling moment is shifted a small bit in time, depending on the clock rise or fall time, if sampling occurs at the rise or the falling edge of the clock signal. This change in sampling moment finds its origin in the gain decrease at high input frequencies. When clocked flip-flops are used as a comparator then a decision takes place at the moment the total loop gain equals 1. At that moment no change in decision can be made anymore. In a CMOS system a larger tail current in the decision flip-flop is needed to compensate for the loss in gain at high frequencies. By using the slope of the sampling clock pulse, this larger tail current occurs at a later time moment. As a result a frequency dependent sampling moment is obtained which will result in third-order distortion components in the output signal of an analog-to-digital converter using these comparators.

11.12 Conclusion

In this chapter a generalized relation between amplifier bandwidth and maximum input frequency for an A/D converter is calculated. When no other distortion products due to ladder nonlinearity, and so on, occur, then the given expressions determine the effective resolution bandwidth of a con-

verter. There is no difference in analysis between a full-flash converter or a folding converter. The relations given are verified using extensive simulations on A/D converter circuits. These simulations are performed at transistor level. Furthermore, measurements on a flash-type A/D converter show the predicted increase in third-order signal distortion at high frequencies.

A simplified analysis about decision failures of flip-flops used as comparators has been carried out. This analysis results in design criteria for master-slave flip-flops as a function of the maximum analog input frequency and the maximum clock rate to be applied to the converter with the failure rate as a parameter.

Chapter 12

Technology and device matching

12.1 Introduction

Designing converters with unit elements, then the matching accuracy between the elements as a function of the number of bits is known. A 10-bit converter for example needs for 1σ yield and $\pm\frac{1}{2}$ LSB INL an element matching of 2.5 %. In case we want to increase the yield to 3σ then the matching must be increased to 1.25 %. In this section matching parameters of devices in MOS technology will be given. It must be noted, however, that mostly the matching parameters depend on the technology used and can differ from one supplier to the other. Furthermore these parameters are company confidential. The numbers given here are only an indication of what can be expected in a real technology. No guarantee is given about the exact values!

12.2 Technology road map

The SIA road map concerning the availability of CMOS technologies is shown in Fig. 12.1. This road map shows that in 2003 0.13 μm is the most advanced technology available. However, 0.09 μm is already available for test and small volume designs. This is earlier than expected from the road map. Although the mask costs are very high, the advantages of the faster and smaller technology still seem to pay off for the large costs. In some cases, such as very high speed circuits it is the only MOS technology available to perform the function. From the road map it is seen that the sup-

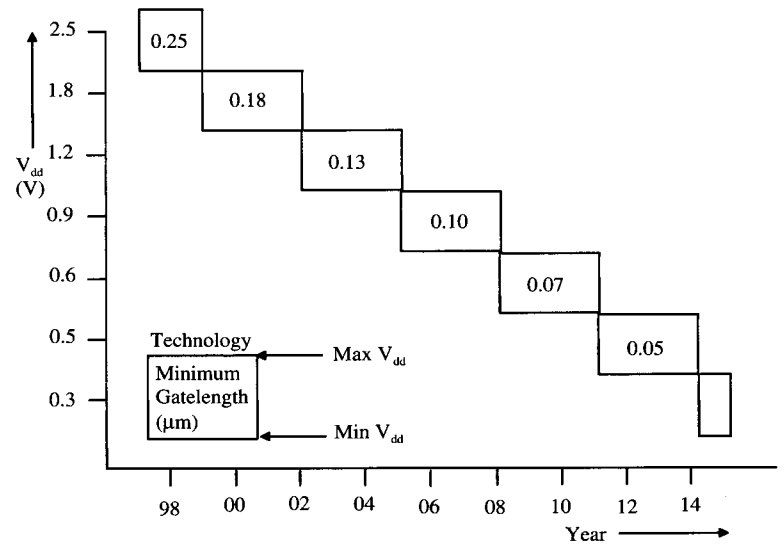

Figure 12.1: SIA Technology road map

ply voltage decreases every time a new technology is introduced. The 0.13 μm has a supply voltage of 1.2 V $\pm$ 10 % with a 2.5 V high voltage device for PCI bus connections. This range of supply voltage is still high enough to perform most of the analog and combined analog/digital functions. However, the next step, 0.09 μm has a supply voltage of 1.0 V $\pm$ 10 % with the high voltage option too. At this moment the design of analog circuits with high performance becomes more challenging. Not too many solutions are known at this moment to obtain for example 12-bit sample-and-hold amplifiers and preamplifiers to have a signal range of 1 V_{pp} differential. Furthermore the number of interconnect layers is increasing. 6 to 8 layers of interconnect is more or less standard. However, the thickness of the layers increases while the width is reduced to below the layer thickness. This means that the interconnect capacitance between two adjacent layers increases and as a result the delay over these wires increases. Including copper decreases the resistance while with low ϵ_r material the capacitance can be reduced.

12.3 MOS matching models

In MOS technology information about matching of components is available as a function of technology and a limited amount of model parameters [32].

Suppose the MOS devices are in saturation then:

$$I_{D1} = \frac{\beta_1}{2}(V_{gs1} - V_{th1})^2 \tag{12.1}$$

$$I_{D2} = \frac{\beta_2}{2}(V_{gs2} - V_{th2})^2 \tag{12.2}$$

$$\tag{12.3}$$

The first condition that will be considered is:
1) Equal Drain Currents so:

$$I_{D1} = I_{D2} \tag{12.4}$$

This results in:

$$\frac{\beta_1}{2}(V_{gs1} - V_{th1})^2 = \frac{\beta_2}{2}(V_{gs2} - V_{th2})^2 \tag{12.5}$$

$$\frac{\beta_1}{\beta_2} = (\frac{V_{gs2} - V_{th2}}{V_{gs1} - V_{th1}})^2 \tag{12.6}$$

$$\sqrt{\frac{\beta_1}{\beta_2}} = \frac{V_{gs2} - V_{th2}}{V_{gs1} - V_{th1}} \tag{12.7}$$

Defining small difference between the two MOS devices using:

$$\beta_1 = \beta_2 + \Delta\beta_2 \tag{12.8}$$

$$V_{gs2} = V_{gs1} + \Delta V_{gs1} = V_{gs1} + V_{off} \tag{12.9}$$

$$V_{th2} = V_{th1} + \Delta V_{th1} \tag{12.10}$$

We obtain:

$$\sqrt{\frac{\beta_2 + \Delta\beta_2}{\beta_2}} = \sqrt{1 + \frac{\Delta\beta_2}{\beta_2}} = \frac{V_{gs1} + \Delta V_{gs1} - V_{th1} - \Delta V_{th1}}{V_{gs1} - V_{th1}} \tag{12.11}$$

Working out this equation we obtain:

$$\Delta_{gs1} = V_{off} = \Delta V_{th1} + \frac{\Delta\beta_2}{2\beta_2}(V_{gs1} - V_{th1}) \tag{12.12}$$

The matching of an MOS pair is equally influenced by the threshold matching ΔV_{th} or by the slope mismatch $\frac{\Delta\beta}{\beta}$ if:

$$V_{gs1} - V_{th1} = \frac{2\Delta V_{th1}}{\frac{\Delta\beta_2}{\beta_2}}. \tag{12.13}$$

In practical MOS technologies

$$\Delta V_{th1} = A_{Vth}.t_{ox} \text{ with} \tag{12.14}$$

$$A_{Vth} = 1.5 \text{ V}/\mu \text{ and} \tag{12.15}$$

$$\frac{\Delta\beta}{\beta} = 1 - 3\% \tag{12.16}$$

$$\tag{12.17}$$

In Fig. 12.2 the threshold matching of MOS devices having a 1 μ by 1 μ device size versus the gate oxide thickness of the technology is shown. From this figure it can be seen that the mismatch reduces with decreasing gate oxide thickness. The validity of this relation has been proven even for sub-micron technologies. As is shown in this figure, the supply voltage decreases with the minimum gate length (to keep the field strength at roughly the same value) while furthermore when the effective gate area remains 1 μ^2, the noise reduces too. The ratio between supply voltage and offset does not change much, however, the reduction of noise changes according $\sqrt{L}$. This means that the signal-to-noise ratio decreases. More bias current is needed in this case to obtain the same S/N ratio, resulting in an increase in power. The gain mismatch ($\frac{\Delta\beta}{\beta}$) of MOS devices versus gate oxide is shown in Fig.

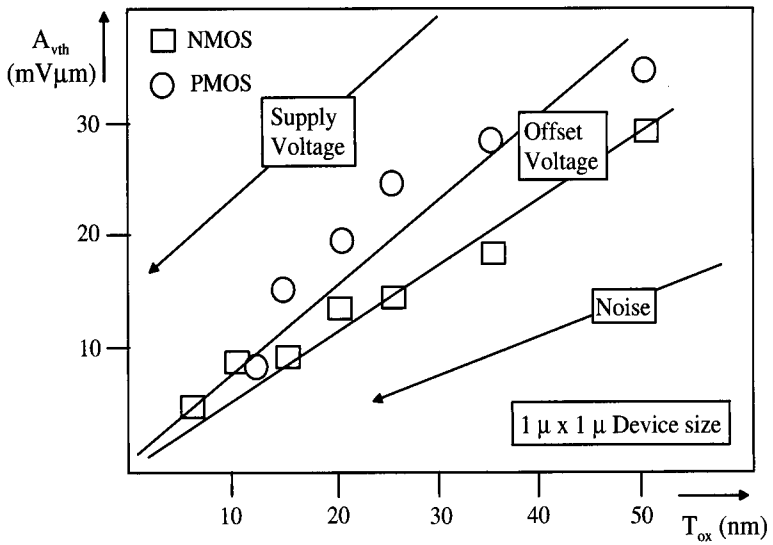

Figure 12.2: Unit area threshold mismatch versus gate oxide thickness

12.3. From this figure we see that the gain mismatch is nearly independent of

the gate oxide thickness. This means that with increasing drain current the mismatch of a differential pair or a current mirror will become independent of technology (β limited). If

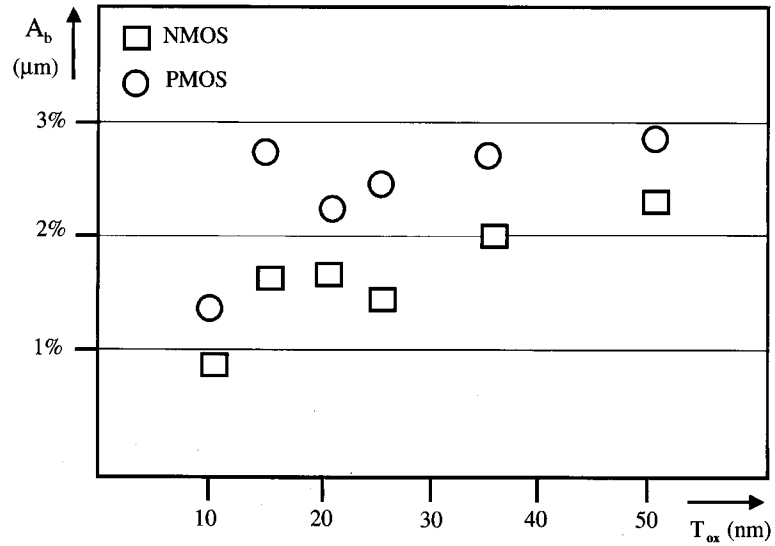

Figure 12.3: Unit area gain mismatch versus gate oxide thickness

$$V_{gs1} - V_{th1} \leq \frac{2\Delta V_{th1}}{\frac{\Delta\beta_2}{\beta_2}}, \tag{12.18}$$

then

$$V_{off} = A_{Vth}.t_{ox}. \tag{12.19}$$

In practice this means that the current density in the MOS device must be below a value corresponding with the given $V_{gs1} - V_{th1}$ gate-source voltage. The calculated offset is valid for MOS devices with a 1 μ by 1 μ gate size. Increasing the size of the devices it is known from literature that the offset decreases with increasing device area as $\sqrt{WL}$ or:

$$V_{off} = \frac{A_{Vth}}{\sqrt{WL}}.t_{ox}. \tag{12.20}$$

In Fig. 12.4 the measured threshold mismatch has been plotted against the device size $\sqrt{WL}$ of an MOS transistor. Increasing the size reduces the mismatch according to equation 12.20. The designer has the option to size the devices regarding offset. In a practical situation the device size

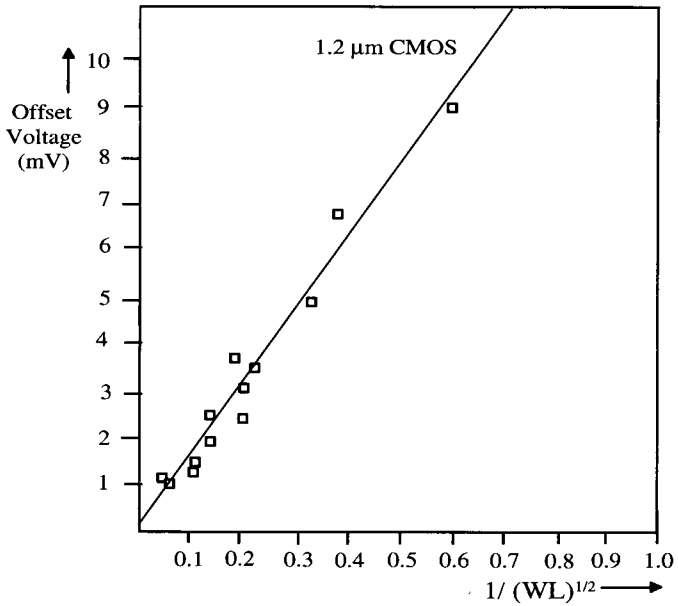

Figure 12.4: Threshold mismatch versus $\sqrt{WL}$ of a MOS transistor

variations are limited. A 1 to 100 size variation is still possible, however, the capacitance of the devices increases. This results mostly in an increase in biasing current and thus power.

2) Equal gate-source voltage:

$$V_{gs1} = V_{gs2}. \tag{12.21}$$

With the devices in saturation we obtain:

$$V_{gs1} = V_{th1} + \sqrt{\frac{2I_{D1}}{\beta_1}} \tag{12.22}$$

$$V_{gs2} = V_{th2} + \sqrt{\frac{2I_{D2}}{\beta_2}} \tag{12.23}$$

$$\tag{12.24}$$

Solving these equations for a difference in drain currents:

$$V_{th1} + \sqrt{\frac{2I_{D1}}{\beta_1}} = V_{th2} + \sqrt{\frac{2I_{D2}}{\beta_2}} \tag{12.25}$$

$$V_{th1} - V_{th2} = \sqrt{\frac{2I_{D2}}{\beta_2}} - \sqrt{\frac{2I_{D1}}{\beta_1}} \tag{12.26}$$

Inserting small difference between the drain currents using:

$$I_{D2} = I_{D1} + \Delta I_{D1}, \tag{12.27}$$

we obtain

$$\Delta V_{th2} = \sqrt{\frac{2I_{D1}}{\beta_1}}\left(\sqrt{\frac{1+\frac{\Delta I_{D1}}{I_{D1}}}{1+\frac{\Delta\beta_1}{\beta_1}}} - 1\right). \tag{12.28}$$

Using a first order approximation for the square root we get:

$$\frac{\Delta I_{D1}}{I_{D1}} = \frac{\Delta\beta_1}{\beta_1} + 2\Delta V_{th1}\sqrt{\frac{\beta_1}{2I_{D1}}}. \tag{12.29}$$

The variable I_{D1} can be replaced by:

$$\sqrt{\frac{\beta_1}{2I_{D1}}} = \frac{1}{V_{gs1} - V_{th1}}. \tag{12.30}$$

Then we obtain for the current mismatch:

$$\frac{\Delta I_{D1}}{I_{D1}} = \frac{\Delta\beta_1}{\beta_1} + \frac{2\Delta V_{th1}}{V_{gs1} - V_{th1}}. \tag{12.31}$$

At small current densities we have that:

$$V_{gs1} - V_{th1} \leq \frac{2\Delta V_{th1}}{\frac{\Delta\beta_1}{\beta_1}}. \tag{12.32}$$

The current mismatch at small current densities can be simplified into:

$$\frac{\Delta I_{D1}}{I_{D1}} = \frac{2\Delta V_{th1}}{V_{gs1} - V_{th1}}. \tag{12.33}$$

At large current densities the matching is determined by:

$$\frac{\Delta I_{D1}}{I_{D1}} = \frac{\Delta\beta_1}{\beta_1}. \tag{12.34}$$

Note that the calculated current offset is again valid for 1x1 μ sized devices! When the size of the devices is changed then the offset varies depending on $\sqrt{WL}$ of the gate area.

The final mismatch at small current densities and device size dependent becomes:

$$\frac{\Delta I_{D1}}{I_{D1}} = \frac{2}{V_{gs1} - V_{th1}}\frac{A_{Vth}t_{ox}}{\sqrt{WL}}. \tag{12.35}$$

In case of large current densities we obtain finally for the current mismatch:

$$\frac{\Delta I_{D1}}{I_{D1}} = \frac{\Delta\beta_1}{\beta_1}\frac{1}{\sqrt{WL}}. \tag{12.36}$$

In Fig. 12.5 the measured gain mismatch ($\frac{\Delta\beta}{\beta}$) versus the device size WL is shown. The designer has again the option to scale the device size to reduce

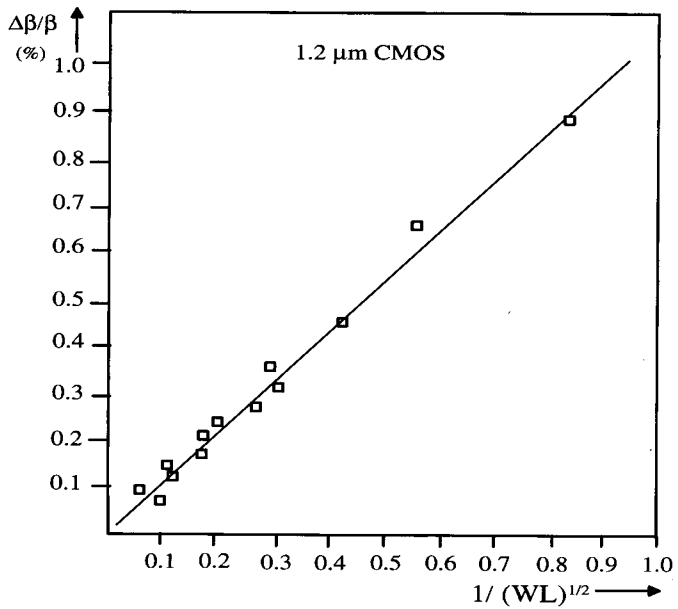

Figure 12.5: Gain mismatch versus $\sqrt{WL}$ of a MOS transistor

the current offset.

It is possible to increase the complexity of the matching relations between MOS devices, but it practice these quite easy relations perform good enough to get a sufficiently accurate estimate. Therefore no attempt has been made to increase the complexity.

12.4 Capacitor matching

In many circuits shown the ratio between capacitors is an important design criterion. To obtain information about the matching of capacitors is therefore important for a designer. Especially the minimum required capacitor

size with respect to the matching accuracy is an important parameter. The standard formula for a capacitor is:

$$C = \epsilon_0\epsilon_r\frac{WL}{H}. \tag{12.37}$$

With W and L the width and length of the capacitor and H the height or oxide thickness. ϵ_0 and ϵ_r are the dielectric constants of the material. Furthermore MOS capacitors or metal to metal capacitors can be used. The metal to metal capacitors have a very good linearity and are nearly signal level independent, while the MOS capacitors depend on the bias conditions. Here metal to metal capacitors will be considered.
As was the case with MOS devices it is expected that the matching of capacitors depends on the size. Suppose that the matching between two capacitors with a 1 μ x 1 μ W and L size is A_{uc} %, then with changing size the following can be obtained:

$$\frac{\Delta C}{C} = \frac{A_{uc}}{\sqrt{WL}}. \tag{12.38}$$

Suppose that $A_{uc} = 0.01$, then the equation changes into:

$$\frac{\Delta C}{C} = \frac{0.01}{\sqrt{WL}}. \tag{12.39}$$

This means that a capacitor with a size of 10 μ x 10 μ shows a matching of 0.1 %.
The calculation of the value of a designed capacitor depends on the configuration. Using 2D and 3D simulators a very good calculation of the capacitor value is possible.

12.5 Resistor matching

As resistors the source or drain diffusions with appropriate contacts can be used. These resistors are diffused resistors and therefore the linearity as a function of the voltage drop across the resistor is limited. Usually a signal dependent resistivity of 1 % per volt is found. This value depends on the doping of the resistor and the substrate.
Mostly poly resistors will be used. These resistors are nearly signal voltage independent and show a small parasitic capacitance. The general formula for an integrated resistor is:

$$R = 2R_{contact} + \frac{W}{L}R_{\square}\,. \tag{12.40}$$

Here $R_{contact}$ is the value of the contact resistance to the poly layer and $R_\square$ is the resistivity of an equal sized resistance block. The contact resistance is an important and sometimes disturbing factor in determining the value of an integrated resistor. In case voltage sense and current force terminals are used, then this problem can be avoided. In analog-to-digital converters mostly voltage sense taps are used on the reference ladder resistor. Therefore only W and L and the $R_\square$ are important to determine the accuracy of the resistor taps. When again it is supposed that the size of the resistor has a dominant influence on the matching than the following can be used:

$$\frac{\Delta R}{R} = \frac{A_{ur}}{\sqrt{WL}}. \tag{12.41}$$

Again A_{ur} is defined as the matching accuracy between two resistors with a 1 μ x 1 μ W and L size.
Suppose again that $A_{ur} = 1$ % then this equation changes into:

$$\frac{\Delta R}{R} = \frac{0.01}{\sqrt{WL}}. \tag{12.42}$$

This means that a resistor with 10 μ x 10 μ W and L size shows a matching of 0.1 %.

12.6 Conclusion

In this chapter technology and matching parameters between MOS devices, capacitors and resistors have been defined that give an insight in how the practical layout of a converter in IC technology must be done. Furthermore these matching parameters show already what can be obtained in a converter without using calibration or special techniques to improve the performance. The given values, however, just are used as an indication on how this problem can be solved. The real parameters have to be determined per technology and can usually be obtained from the wafer factory. Such parameters are company confidential and can therefore not be given here.

Chapter 13

Testing of D/A and A/D converters

13.1 Introduction

To verify the different specifications of converters and converter systems it is important to set up test facilities and structures and to agree unanimously on the test procedures. In general, static performance tests can be performed by using digital voltmeters which can be a part of an Automatic Test Equipment set (ATE). Dynamic tests, especially in the case of high-dynamic-range tests, require special equipment. Furthermore, these dynamic tests are generally more difficult to standardize and consume more test time (see [35, 36, 16, 17]). Up until now dynamic test results have been listed very briefly in specification sheets. In this chapter we will determine test configurations and test procedures in order to arrive at a unanimous qualification of converters.

13.2 DC testing of D/A converters

DC specifications are obtained by applying a digital signal source to the input of the D/A converter. This digital source can be a personal computer (PC) or a specially developed device. In Figure 13.1 a test set-up for DC measurements is shown. At the output an IEEE bus programmable digital voltmeter (part of ATE) is connected. The measured data can be applied to a (personal) computer to process these data. How the measured data are processed depends on the configuration of the test system. Zero offset, full-scale accuracy, integral and differential nonlinearity can be measured. It is clear that the accuracy of the digital voltmeter must be much higher than

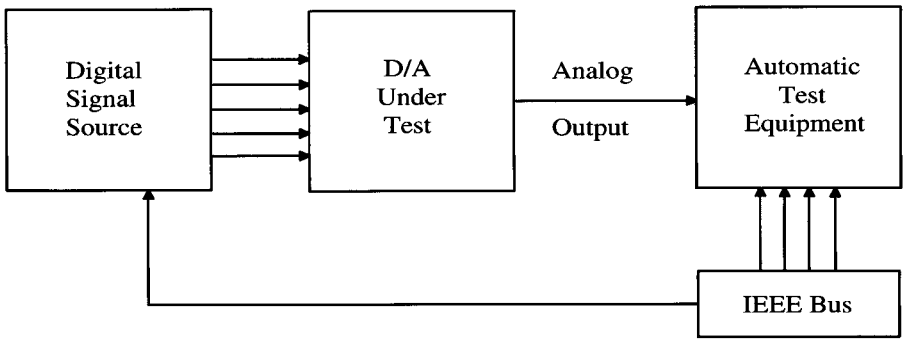

Figure 13.1: DC measurement test set-up

the accuracy of the converter under test. In a binary-coded converter the individual bit weights are measured. By using equations 2.6 and 2.10 shown in Chapter 2 it is possible to calculate the measured nonlinearity of the converter. The nonlinearity of a converter is defined as the deviations from a straight line drawn through zero and full scale. In Figure 13.2 these deviations from a straight line through zero and full scale for the bit weights in a binary-weighted converter are shown. Zero error (offset) is trimmed to zero to obtain a straight line between zero and full scale according to the linearity specification. The errors of the individual bit weights are shown, starting with the MSB error at the left side of the figure to the LSB error at the right side of the figure. The total positive and negative error is shown at the most right side of the figure as $\sum Error$. This converter has a total nonlinearity error of $\pm \frac{1}{2}$ LSB. In a *monotonic by design* type of converter construction

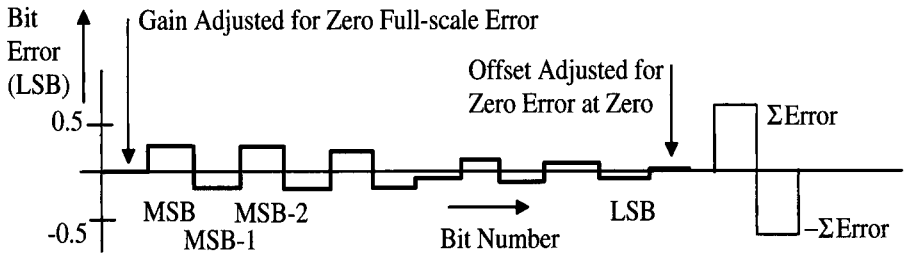

Figure 13.2: Bit-weight error of a binary-weighted converter

every code must be measured and deviations from the straight line through zero and full scale determined. Testing these *monotonic by design* types is more difficult and therefore requires much more test time. Furthermore,

the converter implementation determines how many data points are needed to verify the linearity specification. A resistor string having as many taps as the number of digital codes that can be applied shows a good example of a *monotonic by design* type of D/A converter. From this example it is easily understood that many converter codes must be tested to guarantee a linearity specification. Sometimes it is possible to reduce the amount of test samples to be taken for the linearity specification when the converter implementation is accurately known. Use can then be made of a certain repetitive character which is mostly found in converters. Mostly linearity is determined by the linearity of a number of the most significant bits. The remaining information interpolates between values of the most significant bits resulting in a repetitive character.

13.2.1 Temperature relations

To obtain information about the temperature dependence of DC specifications, the offset, full-scale accuracy, integral and differential nonlinearity tests must be performed at different temperatures. Temperature dependence can then be calculated and specified.

13.2.2 Supply voltage dependence

Information about supply voltage dependence is obtained by performing offset, full-scale, and linearity measurements at the minimum, nominal, and maximum supply voltage specifications of the converter. Mostly information about the supply voltage sensitivity as a function of frequency is added to these specifications. At frequencies around the clock frequency and multiples of this clock frequency the supply voltage rejection ratio must be high to suppress noise generated by the digital circuitry that surrounds the converter (internal and/or external logic circuits). In series with the supply voltage a small signal is added to perform the high-frequency power supply rejection ratio (PSRR) measurements. When these measurements are performed at different temperatures, a full specification is obtained.

13.2.3 Bit weight noise

By applying input codes that switch on the individual bit weights of a binary weighted D/A converter, the noise superimposed on these bit weights can be measured. The value of the total noise of all the bit weights is sometimes specified as the maximum noise of the system. However, it is important to know the bit weight noise values, but this does not define the dynamic

performance (signal-to-noise) of the system. Mostly the noise of the bit weights is well below the total quantization noise value determined by the number of bits in the system. When in some cases bit weights show a high noise value, then these bit weights contribute too much to the total system noise. A reduction in the final signal-to-noise ratio of the system is found.

13.3 Dynamic testing of D/A converters

By using a digital programmable sine wave source at the input of a D/A converter, dynamic tests can be performed. A digital sine wave generator applies a practically ideal sine wave to the D/A converter. When an A/D converter with an analog sine wave generator is used at the input of the D/A converter, then the performance of the A/D converter system influences the accuracy of the measurements. In Figure 13.3 a test set-up is shown. A low-

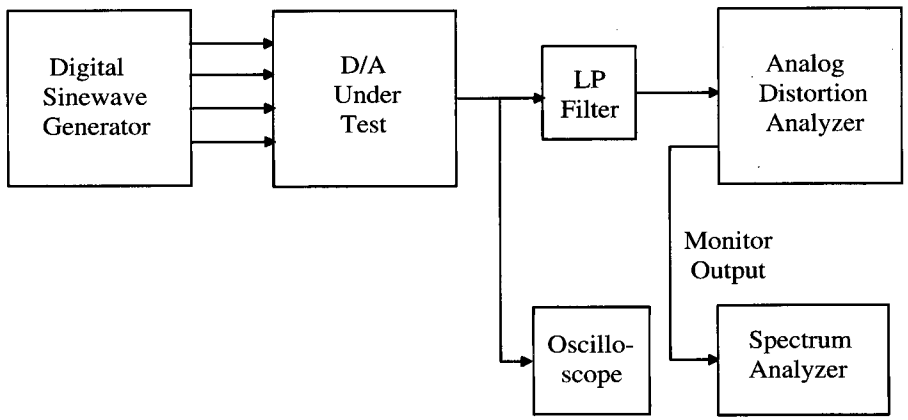

Figure 13.3: Dynamic test set-up

pass filter applies the baseband to the analog distortion analyzer. Usually such a distortion analyzer is equipped with a monitor output, which contains all the signal information except the fundamental signal. This monitor output signal can be analyzed using a spectrum analyzer. Information about distortion and spectrum of the error signal is obtained in this way. The test set-up is extended with an oscilloscope to analyze the high-speed analog output of the converter. The glitch error can be measured by adjusting the input signal at a *major carry* transition in a binary-weighted converter. Only a 1-bit output signal is generated in this case (e.g. 1000... to 0111... code transition). With a distortion analyzer the signal-to-noise plus distortion ratio (SINAD) is measured over a bandwidth equal to the low-pass filter bandwidth. At the monitor output of the distortion analyzer a spectrum analyzer is connected to obtain information about the spectrum of the quantization error and the distortion of the output signal of the converter.

13.3.1 Dynamic integral nonlinearity test

By measuring the signal-to-noise ratio with a full-scale sine wave at the input and over the full input signal bandwidth, information about the dynamic linearity is obtained. In a very well-designed converter the signal-to-noise ratio must be close to the theoretical value given by:

$$S/N = n \times 6.02 + 1.76 \text{ dB}. \tag{13.1}$$

This measurement includes sampling time uncertainty, glitches, and integral nonlinearity. Additional information about the linearity of the converter is obtained when at a constant frequency the signal-to-noise measurement is performed as a function of the signal amplitude. Usually close to the maximum signal amplitude small deviations from the ideal (theoretical) value are found. When close to maximum signal level large deviations are found, then these deviations may be introduced by a large distortion. Therefore, it is important to analyze the quantization error signal as a function of frequency with a spectrum analyzer. If no large distortion components are found, then the clock stability must be determined. Using a spectrum analyzer, the noise level of the clock signal source can be measured. The best information about the noise level of an oscillator is found at $f_m \approx 0$ or $f_m \approx 2f_{osc}$. Determining the signal-to-noise ratio of the clock signal under these conditions must result in a high value per root Hertz. Comparing the results obtained with a crystal oscillator must give small deviations in case a high resolution or high-speed system is measured. Today high-speed oscilloscopes with special software exist to measure the pulse-to-pulse stability of a clock generator. The results of these measurements must comply with converter resolution and maximum analog input signal frequency.

13.3.2 Spurious free dynamic range

The spurious free dynamic range (SFDR) of a D/A converter is measured using a spectrum analyzer. The bandwidth of the analyzer is much smaller than the signal bandwidth of the converter system. When a full-scale signal is applied, the amplitude of the largest distortion component is measured. The ratio between the maximum signal and the largest distortion component

determines the SFDR. Mostly the SFDR is signal frequency and amplitude dependent.

13.3.3 Differential nonlinearity

Dynamic differential nonlinearity is measured by applying a very low frequency signal of, for example, 0.01 Hz superimposed with a 2- to 3- LSBs-sized signal with a higher frequency, for example, 400 Hz. The amplitude of the 0.01 Hz signal is close to the full-scale value of the converter. In this way all the levels in the converter pass by. The variations of the 400 Hz output signal are a measure for the differential nonlinearity of the converter. This measurement can be performed in a short time. A maximum variation of 2 LSBs peak-to-peak is allowed for a binary-weighted converter with an integral nonlinearity of $\pm \frac{1}{2}$ LSB.

13.3.4 Glitches

The glitch energy can be measured using an oscilloscope. At the input of a binary weighted converter a code giving a major carry transition must be applied. For example, a code transition between 100... and 011... can be used to measure the MSB glitch. Usually the largest glitches occur at these major carry transitions. In Figure 13.4 the result of a major carry glitch measurement is shown. The output glitch of a current type D/A converter is measured across a 25 ohm load resistor. Full-scale value is 50 mV equivalent to 2 mA. By measuring the total energy and comparing this glitch energy

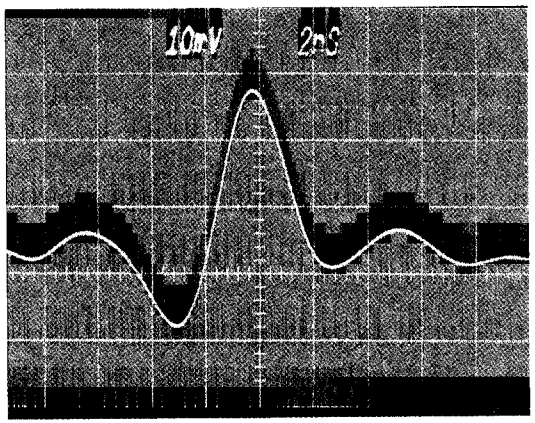

Figure 13.4: Major carry glitch measurement result

with the LSB energy, it is possible to determine the influence of glitches on the total transfer function of a D/A converter. Especially in oversampled offset-binary-coded D/A converter systems, a low glitch energy is very important. In these applications a larger resolution than the basic converter is obtained by using oversampling. When the glitch error cannot be ignored with respect to the LSB size of the emulated higher resolution converter, this oversampling is mostly paid off with a larger distortion. In offset-binary-coded converter systems this problem is encountered when small output signals are reproduced around zero. The addition of a deglitcher circuit can improve the performance of the system. However, such a deglitcher circuit is a critical stage in the D/A conversion process, too.

13.3.5 Distortion measurement

The distortion of a converter system can be measured by applying an appropriate full-scale input test signal. In non-oversampled D/A converters the largest distortion mostly occurs at the high-frequency end of the frequency band. This distortion results from the finite slew rate of output amplifiers. In these amplifiers, the input signal mixes with the "mirrored" signal obtained through the sampling process, resulting in non harmonic distortion products. By analyzing the monitor signal of a distortion analyzer with a spectrum analyzer, it is easy to see if this phenomenon occurs. In oversampled converters distortion must be measured at the low-frequency band edge. Nonlinear distortion occurs here because of the final accuracy of the converter. This final accuracy results in harmonics of the signal frequency as long as these harmonics are within the passband of the system. The oversampling operation transforms the frequency spectra to a much higher sampling frequency. Therefore, it is less probable that non-harmonic mixing products appear in the baseband of the system. Harmonics of the input signal are rejected by the reconstruction low-pass filter for signals above 10 kHz in an audio converter. A better performance is obtained for frequencies between 10 kHz and 20 kHz in such an oversampled audio converter.

13.3.6 Settling time measurement

A dynamic measurement of the settling time of a converter is possible by measuring the signal-to-noise ratio over a fixed bandwidth and with a fixed measuring frequency. By varying the sampling frequency, the signal-to-noise ratio should increase linearly with the square root out of the sampling frequency. At the point when there is no increase in signal-to-noise ratio,

the settling time of the converter has been reached. To obtain an accurate measurement of this condition, a small glitch error is required. Adding a deglitcher, however, can overcome this glitch problem.

Direct measurement of settling time is also possible by applying a special test circuit. In Figure 13.5 this test set-up is shown. The output signal

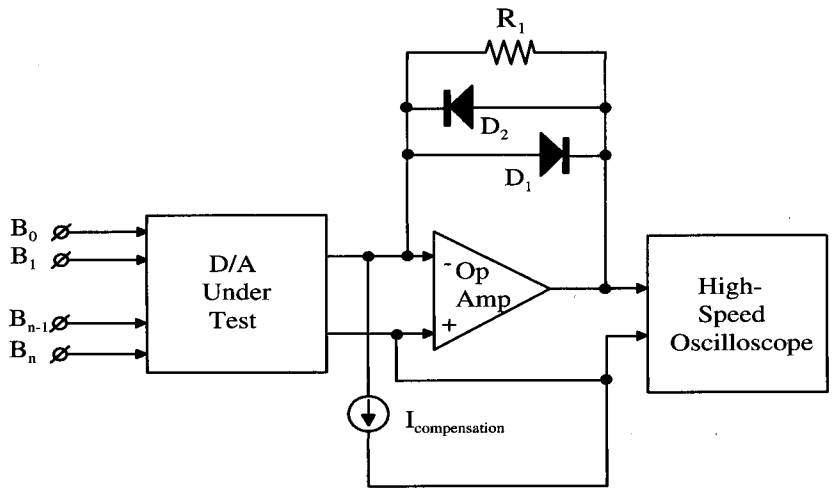

Figure 13.5: Direct settling time measurement set-up

of the D/A converter is applied to a high-speed Schottky diode (D_1, D_2) clamped operational amplifier (OA), which performs a current-to-voltage conversion in this current D/A converter example. Furthermore, a current I_{comp} is subtracted from the output current of the D/A converter. This compensation current determines the current value at which the direct settling time measurement must be performed. Schottky diode clamping is used to prevent overloading of the oscilloscope. The measurement is performed by switching the digital D/A converter input value from zero or full scale to the desired current setting. With the oscilloscope the boundary within which the output signal must settle is determined. In this way a direct measurement is obtained. However, the settling time of the operational amplifier and the Schottky-clamped circuit must be much smaller than the values to be measured. Therefore, a careful layout of the circuit board and a good choice of devices are needed.

13.4 DC testing of A/D converters

In Figure 13.6 a DC test set-up is shown. If DC tests are performed, the sample-and-hold function does not need to precede the converter. An accuracy-limiting circuit can be avoided in this way. The set-up consists

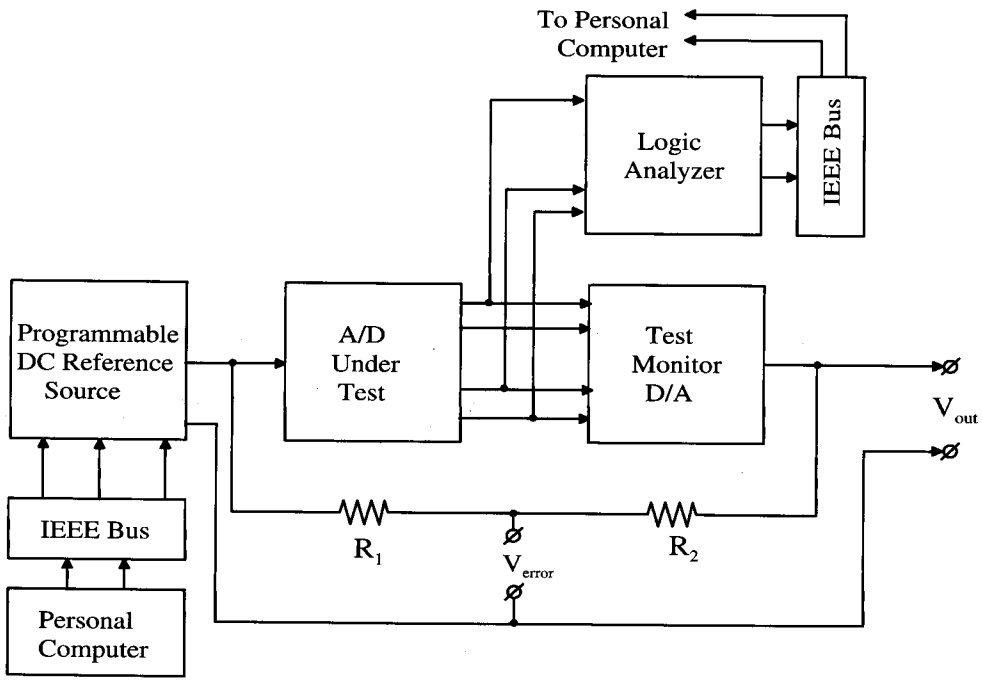

Figure 13.6: DC test set-up for A/D converters

of a programmable high-accuracy DC voltage source, a logic analyzer, and a controller. The output of the A/D converter can be analyzed using a logic analyzer. If a D/A converter with a much higher accuracy than the A/D converter is connected at the output of the A/D, it is advantageous to connect the output data of the A/D to the D/A converter in such a way that an opposite polarity of the output signal compared to the input signal is obtained. By connecting two resistors R_1 and R_2 in a bridge circuit between input and output of the system, the linearity can be measured by monitoring the signal marked V_{error} at a test point between the resistors R_1 and R_2 as a function of the input voltage. Scale errors can be calibrated by changing the value of one of the two resistors in such a way that only differences appear at the node. By programming the analog input source, offset

and full-scale errors can be monitored with the logic analyzer. Differential and integral nonlinearity measurements are performed by slowly varying the analog input signal from zero to full scale. By connecting an X,Y plotter, V_{error} as a function of the input signal can be plotted. A hard copy can be made to determine differential and integral nonlinearity of the converter. The difference between every quantization level shows the differential non-linearity. The deviation of V_{error} from zero gives the integral nonlinearity. All steps are verified with this measurement. In Figure 13.7 a measurement result of such a test is shown. These measurements can be performed over a

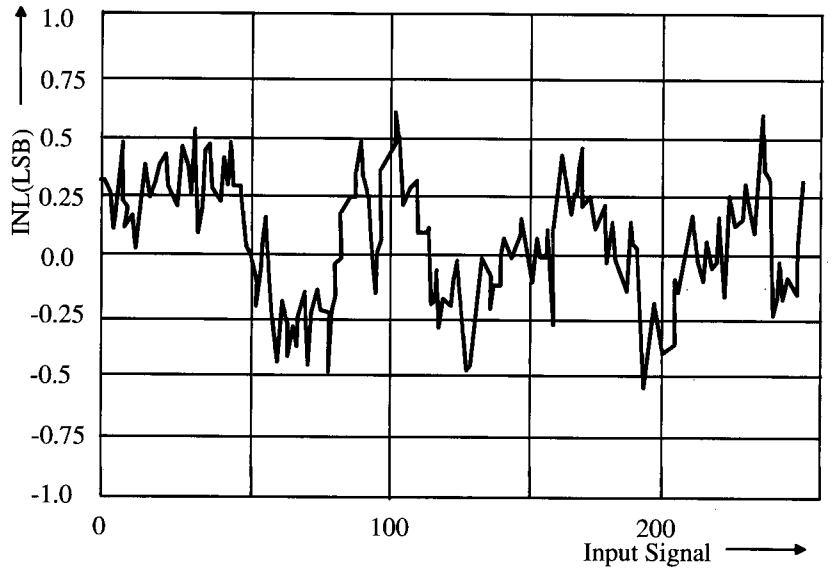

Figure 13.7: Integral Non-Linearity measurement result

large temperature range and with varying supply voltages. In this way the temperature variations and supply voltage dependence of offset, full-scale value and linearity can be determined.

13.5 Dynamic testing of A/D converters

In Figure 13.8 a test set-up for dynamic performance tests of A/D converters is shown. When dynamic tests are performed, a sample-and-hold amplifier must in most cases be added to the input circuitry of the A/D converter to sample the analog input signal. This sample-and-hold amplifier must have a much better performance than the A/D converter to be tested. The sample-

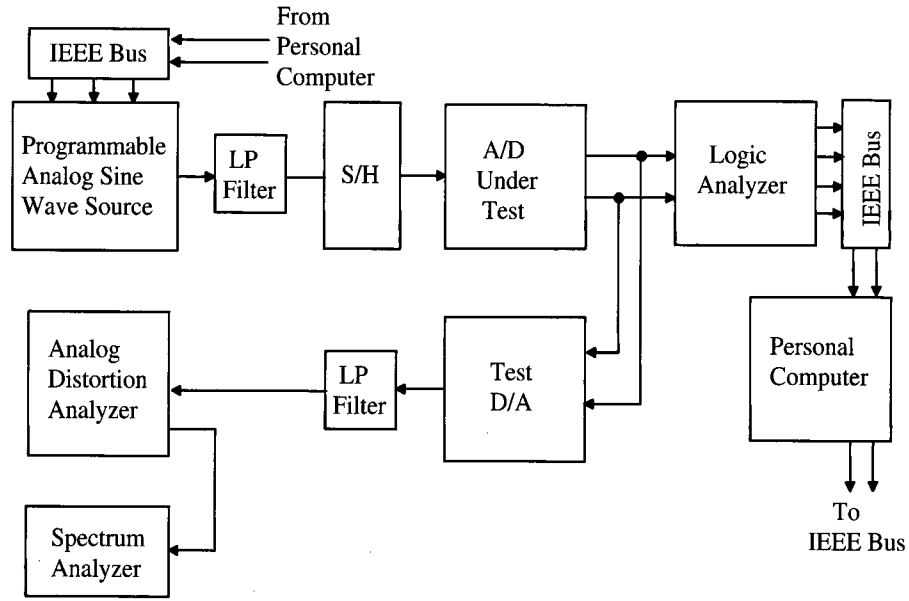

Figure 13.8: Dynamic test set-up for A/D converters

and-hold amplifier samples the input signal and keeps this signal constant during the time the A/D conversion takes place. At the input of the test set-up a low-distortion sine wave source is applied. Moreover, a low-pass input filter is used to filter out possible high-frequency interference and noise signals that may be present on the output signal of the sine wave generator. Digital data can be analyzed using a specially built digital distortion analyzer. If such an instrument is not available, then a high-accuracy D/A converter can be used to convert the digital data into analog signals again. This analog signal is filtered by the reconstruction filter and then analyzed using a distortion analyzer. In most cases distortion analyzers have a monitor output showing the error signal after the fundamental has been removed. This monitor signal can be analyzed with a spectrum analyzer to obtain information about harmonics and glitches. On the other hand, the converted digital signals can be analyzed by using a fast Fourier transform (FFT). In such a case enough samples must be taken to obtain accurate information about the signal to be analyzed. Furthermore, the limited number of samples that can be analyzed calls for a completely random choice of input signal frequency with respect to the sampling frequency. To minimize the problems with "leakage" in the fast Fourier transform, a window function

must be applied. It is important to let the ratio between sampling frequency and input frequency be an irrational number. In that case the quantization errors are randomized so a correct measurement and interpretation of the results is possible. Signal-to-noise measurements as a function of frequency and amplitude must be performed to characterize the A/D converter.

The spurious free dynamic range of the converter is obtained by determining at maximum input signal the amplitude of the largest distortion component. The SFDR is the ratio between the signal amplitude and the largest distortion component. In case more components with nearly equal amplitude are present, the SFDR does not change because of the increase in distortion power. By measuring at a high sample frequency the signal-to-noise ratio of a system, the *effective resolution bandwidth* can be determined. This bandwidth is the maximum analog input frequency for which the resolution (signal-to-noise ratio) of the system decreases with $\frac{1}{2}$ LSB compared to the low-frequency result. During this measurement it must be noted that the low-frequency signal-to-noise ratio does not deviate more than a fraction of an LSB from the theoretical value. At the same time the *Effective Number of Bits* (ENOB's) as a function of input frequency is determined.

13.5.1 Conversion speed

The conversion speed of an A/D converter can be measured by varying the conversion time of the converter and keeping the sampling frequency and input signal conditions constant. Particularly at high input signal frequencies, the measurement is sensitive to conversion speed variations because of the small amount of samples per period of input signal. Additional quantization errors introduced by the A/D converter reduce the signal-to-noise ratio, while mixing of the input signal with the sampling frequency can also result in non-harmonic distortion. In Figure 13.9 the result of such a conversion time measurement is shown. When a long conversion time is used, the optimum signal-to-noise ratio of such a system is found.

A definition of the minimum conversion time of an A/D converter can be specified as: the minimum conversion time for which the signal-to-noise ratio is reduced by 1 dB compared to the optimum long conversion time value.

A 1 dB signal-to-noise reduction is not seen as a disturbing loss. This specification gives a clear definition of the minimum conversion time of a converter.

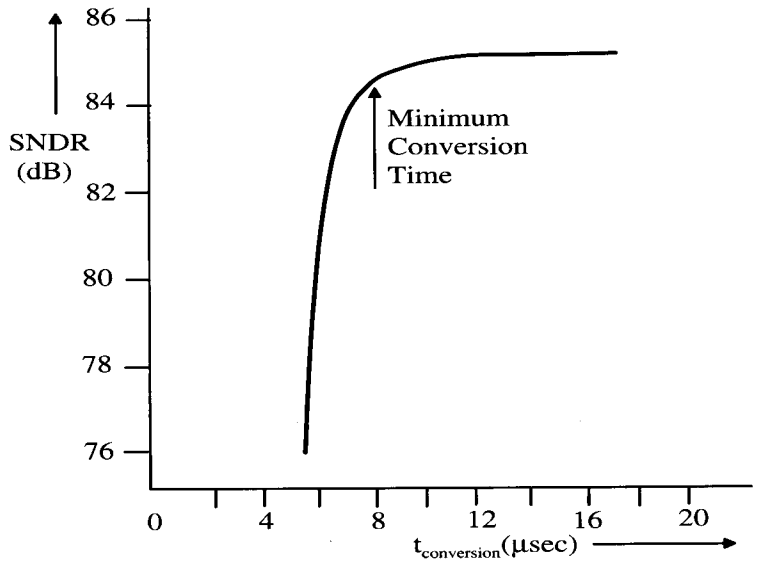

Figure 13.9: Conversion time measurement result

13.6 Bit Error Rate

The bit error rate (BER) of an analog-to-digital converter can be tested by applying an appropriate DC input offset voltage together with an ac input signal of arbitrary frequency. To clarify this measurement the BER of the MSB with the MSB-1 will be explained. The input signal of the converter is shifted to the MSB transition level. The peak amplitude of the ac signal must be smaller than a quarter of the full scale of the converter. At the output of the converter the code transitions between the MSB and MSB-1 are always opposite, for example, 01... and 10..., because of the adjustment of the input DC bias signal. With an Exclusive OR function the MSB and MSB-1 are compared. At the moment an equal code, for example, 00... or 11..., is found a signal appears at the output of the EXOR. This output signal is counted using a counter, and the number of times such a code is found is a measure for the BER. These measurements are performed with increasing sampling frequency. Normally the errors per time unit increase with increasing sampling frequency. The frequency of the input signal is of minor importance, because the measurements concern the number of deci-

sions that have to be taken during the analog-to-digital conversion by the MSB and MSB-1 comparators. In Figure 13.10 the result of a BER measurement as a function of sample frequency is shown. It is clear that, depending

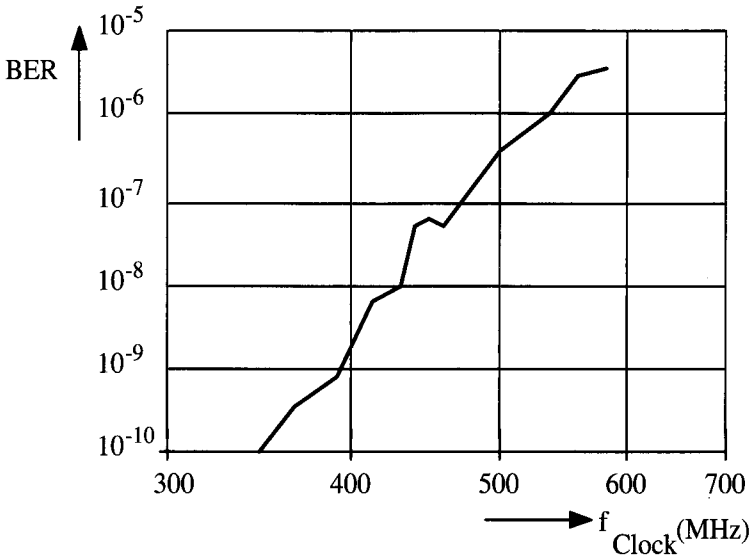

Figure 13.10: BER measurement result

on different DC levels, the same operation can be performed to obtain information about the MSB-1 and MSB-2 error rate. In this case a DC level of one-fourth or three-fourths of full scale must be applied to obtain the transition between 010.. and 001.. with an appropriate smaller ac input signal. Again the EXOR determines coincidences of bits 0100. or 0011. which may not occur during this measurement. In high-quality A/D converters, BER values between 10^{-10} and 10^{-15} are required. Applications of these converters are in digital oscilloscopes.

13.7 Testing very high-speed A/D converters

Testing very high-speed A/D converters is a different subject. A digital distortion analyzer is difficult to build because of the high sampling rates of these converters. As a result, an A/D-D/A converter loop is the preferred test environment. The test configuration and the test boards that contain the different system elements must be optimized for the best dynamic performance. The influence of small changes in the test board (e.g., wiring) can

immediately be analyzed with the spectrum analyzer and the oscilloscope. However, D/A converters that show the required linearity and low glitch error at these speeds are difficult to obtain. Both A/D and D/A converters usually operate at the limit of a technology used to build the devices. Sub-sampling of output signals of the A/D converter is therefore applied. At the lower sub-sampling rates D/A converters with a much better linearity and glitch error specification are available. In this manner the question about errors introduced by the D/A converter can be postponed. In Figure 13.11 a test set-up using a sub-sampling technique is shown. From Figure

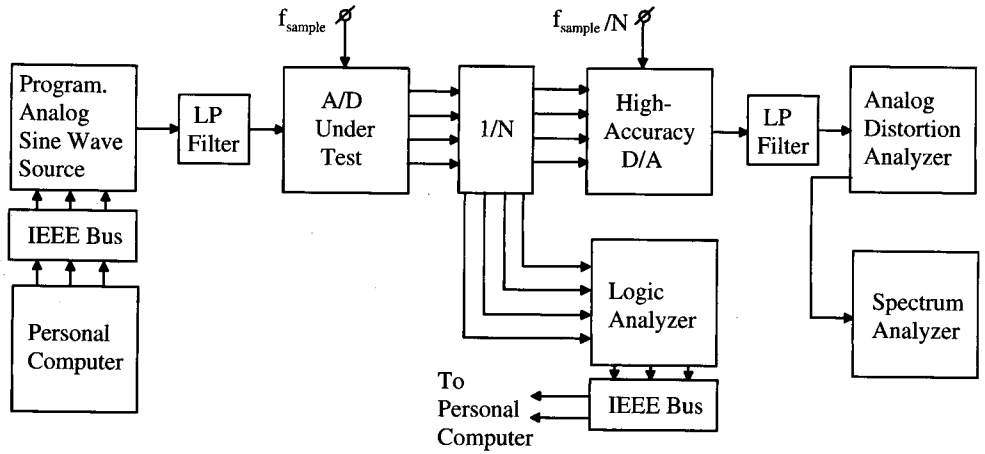

Figure 13.11: Very high-speed A/D converter test set-up using sub-sampling

13.11 it can be seen that the output samples of the A/D converter are reduced by a factor N before they are applied to the D/A converter. The maximum amount of reduction in samples N depends on the speed of the D/A converter used in the test set-up. Moreover, during measurements the sub-sampling rate N can be optimized to get the best performance of the D/A converter over a large sampling frequency range.

Sub-sampling of signals is allowed but the signals, quantization errors, and distortion are folded back into the baseband. It is already known that a reduction in sampling rate by a factor N increases the quantization noise folded back into the baseband by a factor equal to $\sqrt{N}$. At the same time the measurement bandwidth is reduced by a factor N. As a result of this operation the signal-to-noise ratio of the system does not change. In Figure 13.12 the sub-sampling operation is shown, along with a four times sub-sampling factor. Sub-sampling with a factor two results in a "shifting" of frequencies

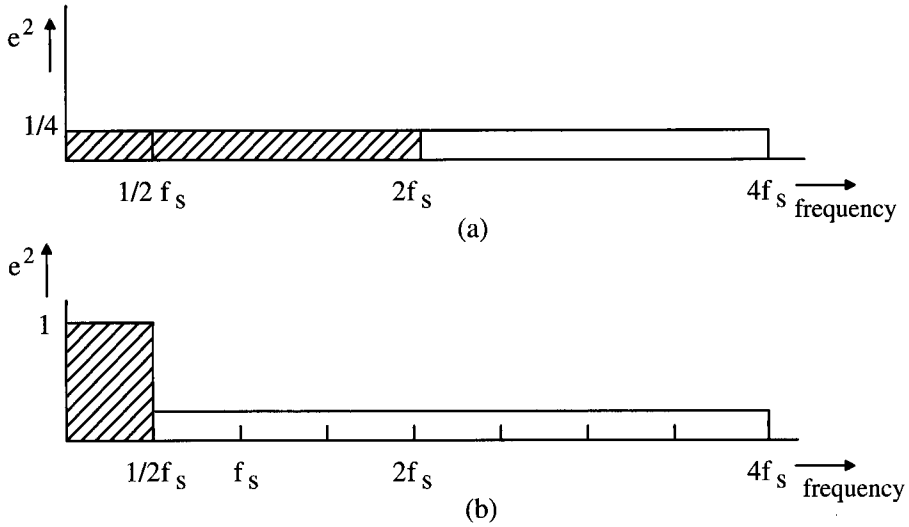

Figure 13.12: Sub-sampling in converter systems

around the sub-sampling frequency $2f_s$ into the baseband from zero to $\frac{1}{2}\ f_s$. An identical operation takes place on the subsamples signal when again a factor two reduction in sampling frequency is performed. Frequencies around f_s are "shifted" into the baseband again. As a result of this operation the quantization noise density is increased by a factor four as long as no filtering operation is performed before the sub-sampling takes place. Higher sub-sampling rates than two can be successfully applied to an A/D-D/A system to obtain accurate information about distortion and signal-to-noise ratio. The D/A converter in such a system can be repeatedly used over the same sampling frequency by changing the sub-sampling factor N depending on the sampling frequency range of the A/D converter. The *Effective Resolution Bandwidth* (ERB) and the *Effective Number Of Bit* (ENOB) of the system can be determined with this test method.

From the measurements on, for example, high-speed A/D converters that do not use a sample-and-hold amplifier at the input, a dominating third-order signal distortion is found. This third-order distortion is a measure for the maximum bandwidth of the input circuitry of the converter under test. In Chapter 11 a theoretical analysis of this phenomenon will be given. The increase in third-order distortion determines the ERB when signal-to-noise plus distortion (SINAD) is measured as a function of frequency. In Figure

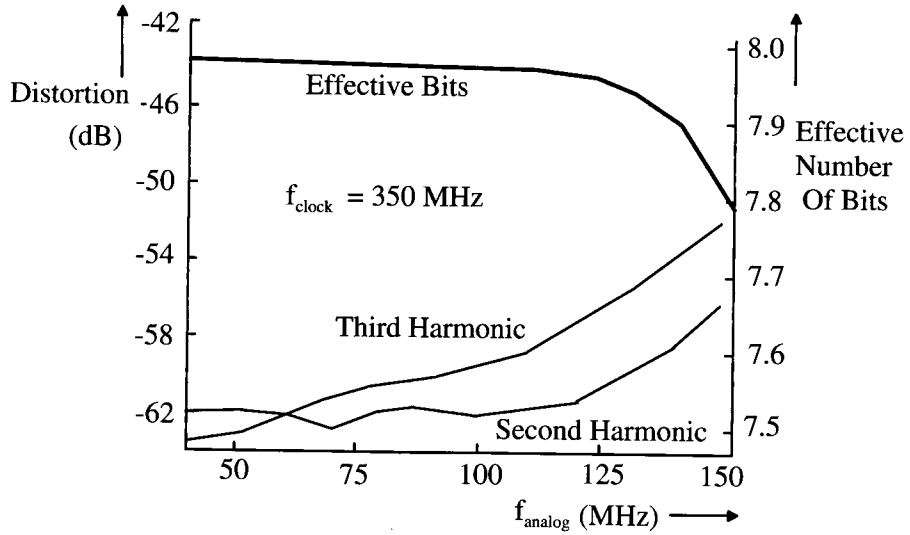

Figure 13.13: High-speed A/D converter distortion measurement result

13.13 the result of a distortion measurement as a function of input frequency is shown. This result is measured on an A/D converter that does not need a sample-and-hold amplifier.

With a high-speed logic analyzer it is possible to measure a large amount of samples. These samples can be stored in the internal memory of the analyzer and then transferred to a computer system to calculate the spectral response. Care must be taken that no correlation exists between the input signal frequency and the sampling frequency in the converter. In that way the quantization errors are randomized and a correct result is obtained. Care must be taken to avoid "leakage" in the fast Fourier transform by applying an appropriate window function.

13.8 Beat frequency test configuration

A quick method to obtain information about the high-frequency performance of a converter can be obtained when the input frequency (e.g., 100.00 MHz) and the sample frequency (e.g., 100.10 MHz) differ only by a small amount. A low-frequency (100 kHz) beat frequency is obtained. In Figure 13.14 an example of a beat frequency signal is shown. This beat frequency signal can be analyzed visually to get information about missing codes or possible

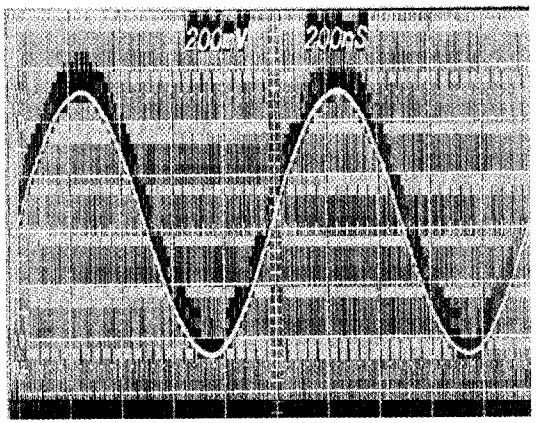

Figure 13.14: Beat frequency output signal

repeating signal parts. Timing errors that may occur in the converter appear as distortion of the beat frequency. Furthermore, step size and quantization levels can be determined accurately. The distortion of the beat frequency is a measure for the linearity and timing errors of the converter. Missing code performance of the system is also shown at these frequencies. Note that in this test condition the sample frequency cannot be much higher than the maximum analog input frequency. This frequency is about half the minimum sampling frequency of the converter. Digital analysis of the beat frequency is preferred because of the high accuracy possible with this measurement method. A D/A converter with good specifications over the total analog input signal bandwidth must be used. Glitches must be small compared to the LSB value to avoid measurement errors.

13.9 Code density DNL and INL measurement

The dynamic differential nonlinearity (DNL) and integral nonlinearity (INL) can be tested using a code density measurement. At the input of an analog-to-digital converter a triangular waveform is applied. The amplitude of this triangular waveform is slightly larger than the full-scale value of the converter. With a logic analyzer the output code is stored. These codes are analyzed for the number of times a code value appears at the output of the converter. To obtain an accurate measurement at least an average of codes per level between 8 and 16 are needed. This results in a storage capacity for the logic analyzer of about 4000 codes, when an 8-bit analog-to-digital

converter is tested. With a triangular input signal, every code in the converter should have an equal density. When a code is missing, then no output occurrence of this code is found during this measurement. In case the differential nonlinearity shows a large step, the number of code occurrences at that specific point in the converter shows an increase. In Figure 13.15 the result of such a code density measurement is shown. No accuracy problems

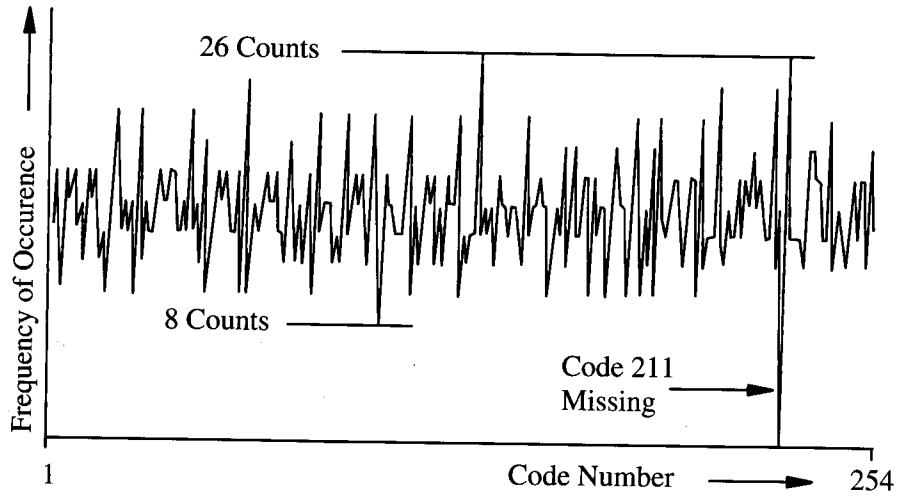

Figure 13.15: Code density (DNL) measurement result with a triangular input signal

exist in the reproduction of the output signal. The result of the code density measurement gives a direct information about the differential nonlinearity (DNL) of the converter. Integrating the measurement result shows the integral nonlinearity (INL). After integration of the measurement result of Figure 13.15 the result shown in Figure 13.16 is obtained. At the moment a sine wave is used as an input source, the density result changes. Because the sine wave shows a flat top and bottom part, the amount of code transitions during these times increases, resulting in a signal level dependent result. In Figure 13.17 the result of a sine wave density (DNL) measurement is shown. The curved result can be declared using the following simplified analysis. Suppose the input sine wave is equal to:

$$V_{in} = V_{max} \sin \omega t, \tag{13.2}$$

then the time difference (Δt) between two quantization levels is a measure for the number of times a code is generated.

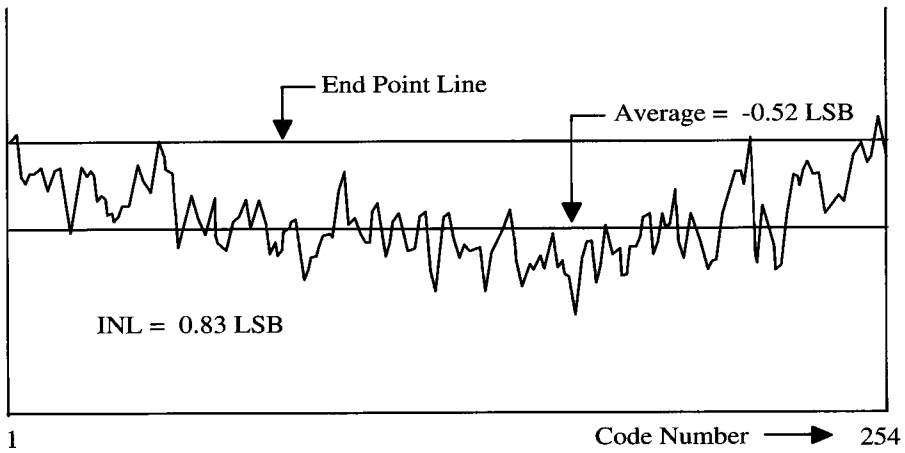

Figure 13.16: Integral nonlinearity density measurement result

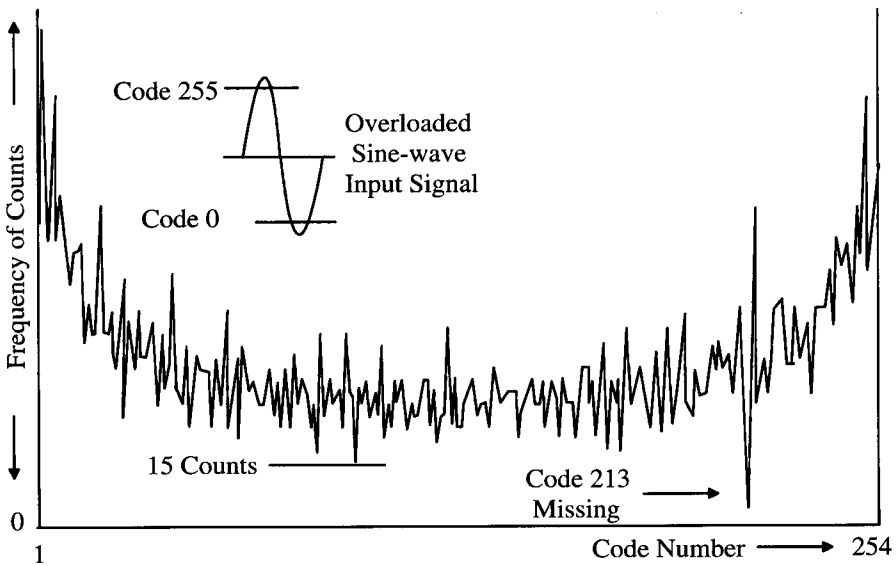

Figure 13.17: Code density (DNL) measurement result with a sine wave input

Using V_{fs} to define the full scale value of the converter, in an n-bit converter the step size (ST) equals:

$$ST = \frac{V_{fs}}{2^n - 1}. \tag{13.3}$$

The time difference Δt can be determined from:

$$ST = V_{max} \sin \omega(t + \Delta t) - V_{max} \sin \omega t = \frac{V_{fs}}{2^n - 1}. \tag{13.4}$$

When a rather large number of bits is used in the converter, then $\Delta t \ll 1$ and equation 13.4 can be approximated by:

$$\omega \Delta t \approx \frac{V_{fs}}{V_{max}} \frac{1}{(2^n - 1)} \frac{1}{\cos \omega t}. \tag{13.5}$$

The equation will be validated over the range:

$$-\frac{V_{fs}}{V_{max}} \frac{\pi}{2} \leq \omega t \leq \frac{V_{fs}}{V_{max}} \frac{\pi}{2}. \tag{13.6}$$

With $\Delta\phi \approx \omega \Delta t$ and $\phi = \frac{V_{fs}}{V_{max}} \pi$ equation 13.5 can be rewritten into:

$$\frac{\Delta \phi}{\phi} = \frac{1}{\pi(2^n - 1)} \frac{1}{\cos \omega t}. \tag{13.7}$$

Suppose that over the total range of ϕ determined by 13.6 a total of Nπ measurement pulses are used, then per quantization level the number of pulses N_q which can be counted is:

$$N_q = \frac{N}{2^n - 1} \frac{1}{\cos \omega t} \tag{13.8}$$

with ωt stepping over the range defined by 13.6 with discrete steps equal to:

$$\frac{V_{fs}}{V_{max}} \frac{\pi}{2^n - 1}. \tag{13.9}$$

From equation 13.8 the curved relation found during the measurement is explained.

Normally the amplitude of the sine wave is made larger than the full-scale value of the analog-to-digital converter. This small over-drive of the input full scale results in a smaller curving of the output data during the code density test. The differential nonlinearity measurement data depend on the time difference a sine wave needs to trip two adjacent levels in the analog-to-digital converter. Integration of the differential nonlinearity measurement result gives the specification for the integral nonlinearity.

13.10 Testing of sample-and-hold amplifiers

In Figure 13.18 a test set-up for measuring the performance of a sample-and-hold amplifier is shown. The set-up consists of a programmable voltage source, a sample pulse generator, and a (differential) digital voltmeter. Depending on the architecture of the sample-and-hold amplifier, a floating digital voltmeter or a bridge type measurement configuration has to be used.

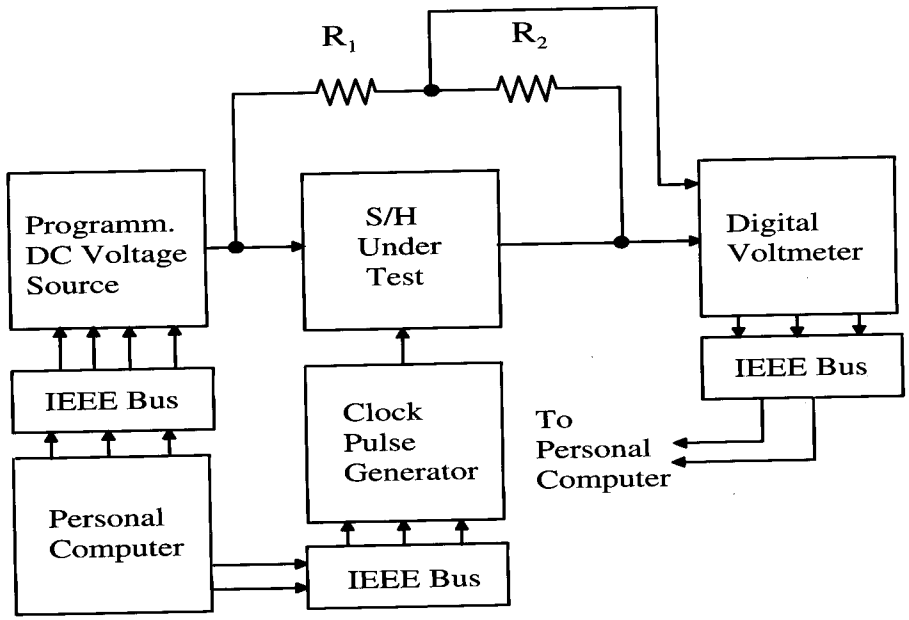

Figure 13.18: Test set-up for measuring S/H amplifiers

A floating digital voltmeter is used to measure the difference between input and output signal of the sample-and-hold amplifier if the circuit performs a non-inverting transfer operation.

When an inverting sample-and-hold amplifier is tested, then the configuration shown in dashed lines can be used. In this way a more accurate testing of the linearity is possible by connecting the digital voltmeter at the interconnection of the resistors R_1 and R_2 and the common signal reference.

13.10.1 Testing DC characteristics

During the *track* mode DC offset and nonlinearity can be measured. If an inverting type of sample-and-hold is tested, then the resistor bridge may be used to measure nonlinearity. In a non-inverting system a floating measurement instrument must be used to measure the difference between input and output signal as a function of the input signal. Information about nonlinearity is obtained in this way. The "track-to-hold step" of a sample-and-hold amplifier is measured by monitoring the difference between the DC input signal during the *track* mode and the signal during the *hold* mode. Most frequently the track-to-hold step is independent of the input signal when an inverting type of sample-and-hold amplifier is used. In the non-inverting type, the switch drive voltage can change with varying input signal which results in a signal dependent feed-through giving distortion. The temperature dependence of all these parameters is obtained by performing the above defined measurements at different temperatures.

13.10.2 Dynamic measurements

In Figure 13.19 a dynamic performance test set-up is shown. The measurement set-up consists of a programmable sine wave source, a pulse generator with an extra delayed output signal terminal, an oscilloscope, and a distortion analyzer to measure the output signal of the sample-and-hold amplifier under test. A test A/D and D/A loop is added to the system to perform additional tests.

Without special measures it is difficult to analyze the sample-and-hold amplifier itself. Usually a "glitch" is generated when the system switches from *track* to *hold* mode. Therefore, it is not possible to analyze the sampled *analog* signal at the output by simply filtering off the harmonics introduced by the sampling process by using a low-pass filter and analyzing the resulting signal with a distortion analyzer and a spectrum analyzer. When the sample-and-hold amplifier is designed as a *deglitcher* at the output of a D/A converter, then the above-mentioned method can be used to obtain information about the dynamic performance of the system.

The acquisition time of a sample-and-hold amplifier is the time needed to switch from the hold mode into a full-accuracy following (tracking) of the analog input signal. The acquisition time of the system is measured by varying, at a fixed sampling frequency, the track-and-hold time. A small

acquisition time is a measure of the performance of a sample-and-hold amplifier. It determines the maximum sample frequency of the sample-and-hold amplifier. The signal-to-noise ratio of the system is measured as a function of the acquisition time. In Figure 13.20 a test result is shown.

The minimum acquisition time is determined at a point where the signal-to-noise of the system is reduced by 1 dB with respect to a measurement value obtained with a large acquisition time.

The aperture time of a sample-and-hold amplifier is the time difference between the start of the *hold* command and the moment the output signal of the *hold amplifier* is settled within the specified accuracy of the amplifier. The aperture or *track to hold* time is measured by varying the delay time T_d between the hold command, applied to the sample-and-hold amplifier, and the start conversion command, applied to the A/D converter. During

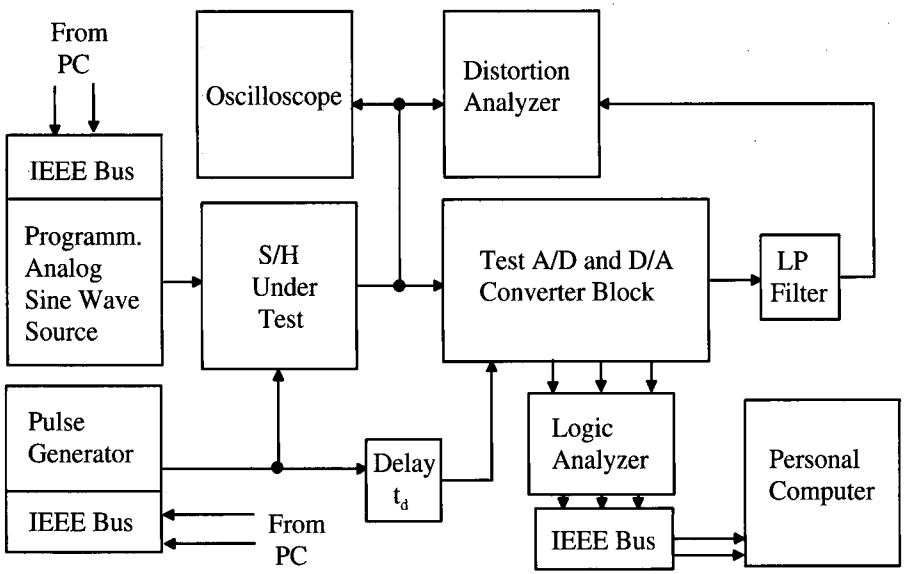

Figure 13.19: Dynamic test set-up for sample-and-hold amplifiers

the *track mode* the distortion of the sample-and-hold amplifier is measured. This measurement includes the distortion of the *hold amplifier*, too. A very important parameter is the *aperture uncertainty* time of a sample-and-hold amplifier. This aperture uncertainty determines the timing accuracy with which analog samples are taken. Especially at high analog input frequencies, this parameter determines the performance of a system, that is signal-to-noise ratio. This *aperture uncertainty* of a sample-and-hold amplifier is difficult to measure. With a large acquisition time the signal-to-noise ratio of the total system is analyzed, and results close to the theoretical value must be obtained. If large differences occur, then the clock jitter has to be reduced and the clock generation circuits improved.

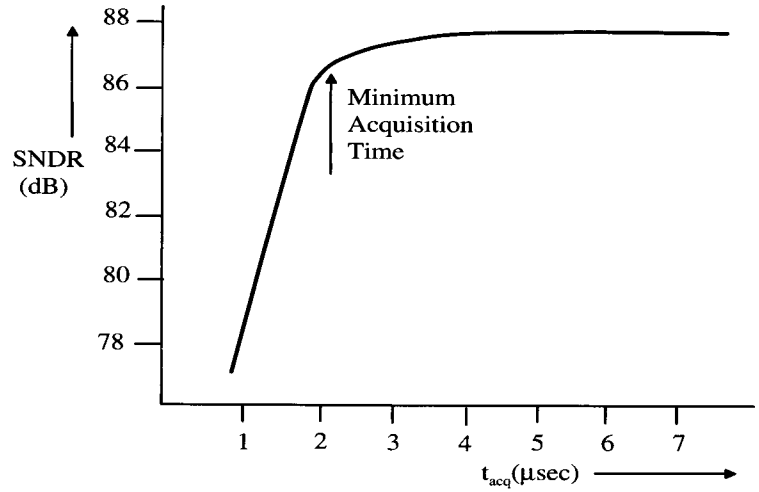

Figure 13.20: Acquisition time measurement result

The small signal bandwidth of the system must be measured to obtain information about the noise bandwidth. Noise tests are performed by analyzing the output noise of the system during the track mode as a function of the DC input signal. The frequency spectrum of the output noise must be analyzed up to very high frequencies to obtain information about the fold-back noise which is finally added to the sampled output signal. The measuring bandwidth is equal to the -3 dB small signal bandwidth of the sample-and-hold amplifier.

Slew rate is part of the acquisition time specification and may be specified as an additional parameter.

Input signal feed-through is measured at the moment the sample-and-hold amplifier is in the hold mode. Parasitic capacitance across the switch limits the signal feed-through in the system at high frequencies. Over the specified signal bandwidth the feed-through must be larger than the dynamic range

of the system to avoid quantization errors. The droop rate of the system is measured during hold mode. The change in output signal as a function of the hold time determines the droop rate. In Figure 13.21 an overview of the measured parameters needed to characterize a sample-and-hold amplifier are shown. Note that some of the parameters are easy to specify, but a

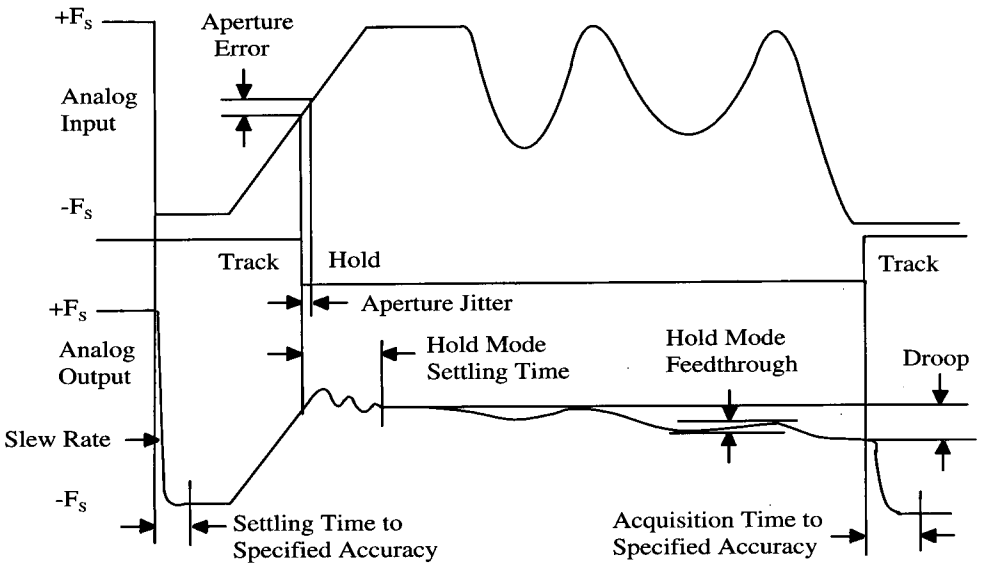

Figure 13.21: Overview of parameters to measure sample-and-hold amplifier

measurement setup and a verification of the parameter sometimes needs an indirect test method.

13.11 Cascading sample-and-hold amplifiers

In Figure 13.22 a cascade of two sample-and-hold amplifiers clocked with different clock signals is shown. Accurate information about the sampled output (hold mode) signal of a sample-and-hold amplifier can be obtained when two of these units are cascaded and operated with different clock signals. This hold information is important for applications with analog-to-digital converters which are only active during the hold mode of the sample-and-hold amplifier. The basic idea behind the cascaded operation is the use of beat frequencies obtained by the different clock signals of the two sample-and-hold amplifiers. At the moment an input frequency close to f_{s1}/n is applied with n = 2, 3, 4, and so on, a beat frequency occurs when the sec-

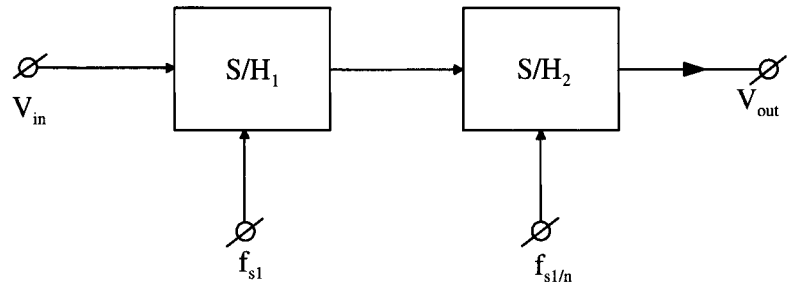

Figure 13.22: Cascade of two sample-and-hold amplifiers

ond sample-and-hold amplifier is clocked with a sampling frequency equal to f_{s1}/n. Note that the beat frequency is chosen at the low-end of the frequency spectrum of the system. The sub-sampling performed by the second sample-and-hold amplifier results in small changes in steps between succeeding samples. The acquisition time accuracy of the second sample-and-hold amplifier is therefore increased while aperture time errors do not contribute to the final sampling accuracy. As a result, a much larger capacitor to store the analog information can be used in the second unit. Furthermore, when the glitches of the second system are minimized, the total waveform can be analyzed, and accurate information about the hold mode performance of the first sample-and-hold amplifier at the high frequency band edge is obtained without using an analog-to-digital converter.

13.12 Conclusion

In this chapter the measurement set-ups and some measurement results of the most important specifications of converters are shown. Many of the DC parameters are fairly easy to measure in contrast with the more difficult to perform dynamic tests. Some results, however, depend on a conglomerate of parameters and are therefore measured as a total. In high-speed A/D converters sub-sampling is used to obtain a high measurement accuracy without using D/A converters operating at the speed limit of a technology. A quick test can be done by using the beat frequency test between the sam-

pling and input signals. This beat frequency signal can be analyzed using a distortion and a spectrum analyzer to obtain information about the distortion and signal-to-noise ratio at these high frequencies. Aperture-time and acquisition-time definitions for sample-and-hold amplifiers are introduced again, together with specific measurement set-ups to perform these tests. A cascade of two sample-and-hold amplifiers operating at different sampling frequencies resulting in a beat frequency at the output of the second unit results in an accurate and independent test method for sample-and-hold amplifiers. High-speed logic analyzers can be used with A/D converters to store the digital data. These data is analyzed using special computer programs to obtain most of the dynamic specifications of the converter. By automating this procedure these tests can be programmed using temperature chambers to obtain the temperature dependence.

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