manufacturing environment on a moving substrate; 2) to find alternative junction partners to replace CdS; and 3) to find new alloys or new deposition methods to give high performance devices with higher band gap alloys.

Polycrystalline layers of CdTe (Chapter 14) have been investigated for photovoltaics since the 1970s. In contrast to limited process options for a-Si or $Cu(InGa)Se_2$, there are over 10 methods to deposit the CdTe films that have produced CdTe solar cells exceeding 10% efficiency. Four have reached precommercialization: spray pyrolysis (SP), electrodeposition (ED), vapor deposition (VD) and close spaced sublimation (CSS). Some take place in liquid baths that are barely warm ~50°C with CdTe deposition rates of μm/hr (ED) while others take place in vacuum systems at temperatures high enough to soften glass ~600°C with CdTe deposition rates of μm/min (CSS). There seem to be three critical steps, however, that all efficient CdTe solar cells require. First, they need a post-deposition anneal in the presence of Cl and O_2 at around 400°C. This chemical/thermal treatment enlarges the grains, passivates the grain boundaries, and improves the electronic quality of the CdTe. Second, all CdTe layers need a surface treatment before applying a contact. This treatment can be a wet or dry process and prepares the CdTe surface by etching away unwanted oxides and leaving a Te-rich layer needed to make a low-resistance contact. Third, all high efficiency devices have a Cu-containing material somewhere in their CdTe contact process but again, there are many ways this can be achieved. Whichever process is used to deposit the CdTe, it has been found that the entire device process is highly coupled since processing steps strongly influence previous layers. This is partially due to the CdTe grain boundaries which act like paths for interdiffusion.

The *pn* junction is formed by first depositing an *n*-type layer of CdS on a transparent conductive oxide substrate followed by the CdTe layer and appropriate chemical annealing. Once the solar cell is made, the CdTe films are slightly *p*-type, typically, 2 to 8 μm thick and have crystallites or grains on the order of 1 μm. The highest reported efficiency for a CdTe/CdS device is presently 16%. Some CdTe modules have been in outdoor field-testing for over five years with negligible degradation, yet other CdTe devices degrade during accelerated life testing indoors. Of the three leading TFSC technologies, CdTe may have the most challenges. The dual role of Cu must be resolved; it seems to be required to produce a high-efficiency device but it is also implicated in long-term stability problems. The various optimizing treatments need to be better understood so they can be simplified and transferred into production. CdTe modules may be more sensitive to atmospheric interaction (O_2, H_2O) requiring better encapsulation methods. Finally, safe and cost-effective Cd usage in the workplace followed by recycling at the end of the module's life need to be determined.

In fact, technically astute investors know that other factors can be more important than efficiency in selecting a technology for development. This point is made loud and clear by examining the relative performance of the three major TFSC technologies – $Cu(InGa)Se_2$, CdTe, and a-Si – in Figure 1.8. Note that a-Si has always had the lowest efficiency. Yet, of the three, it was a-Si that has been commercialized much earlier and more widely. It enjoys by far a much greater manufacturing capacity. As of 2001 [72], a-Si accounted for almost 9% (34 MW) of the world PV power module production, while CdTe and $Cu(InGa)Se_2$ power modules together accounted for less than 0.3% (1 MW), despite a-Si champion-cell-stabilized efficiency lagging the others by several percent. In