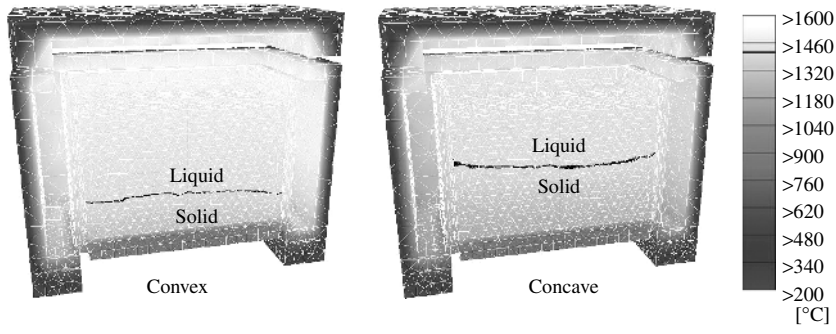

Figure 6.30 Examples of convex and concave liquid–solid interfaces due to the variation of side wall heating power. Both pictures are taken at the same process time

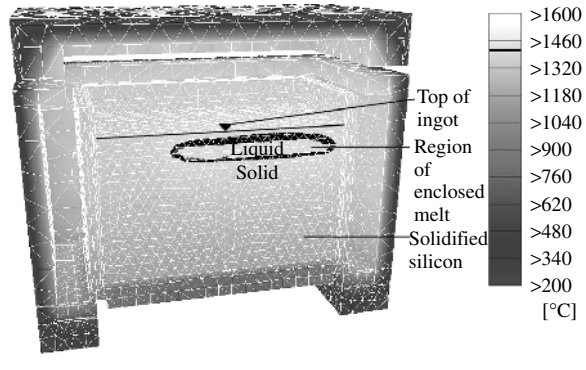

Figure 6.31 Simulation result representing a remarkable decrease of heating power at the top region of the ingot. By this, the solidification time is reduced to half, but solidification ends with an inclusion of silicon melt

the furnace operator to find the balance between material quality, which is known to be high in the case of planar solidification, and process economy.

In Figure 6.31, simulation results are shown, representing a noticeable reduction of heating power at the ingot top. By this, the solidification velocity can be speeded up and the time for solidification is reduced to half. However, in the simulated case study, the solidification ends with an encapsulation of the melt by solidified silicon. Because of the 10% higher density of liquid silicon with respect to the solid phase, this process scenario causes a burst out of melt from ingots volume. This can lead to a crack in the mould and to a damage of the furnace. These case-study simulations can find worst-case process conditions that must be avoided in production. For more simulation results of the SOPLIN process, see [92–94].

6.6.4 Simulation of Silicon Ribbon Growth

As a second example of silicon crystallisation processes, the RGS is taken. The basic idea of this process is the de-coupling of the pulling direction of substrates on which silicon