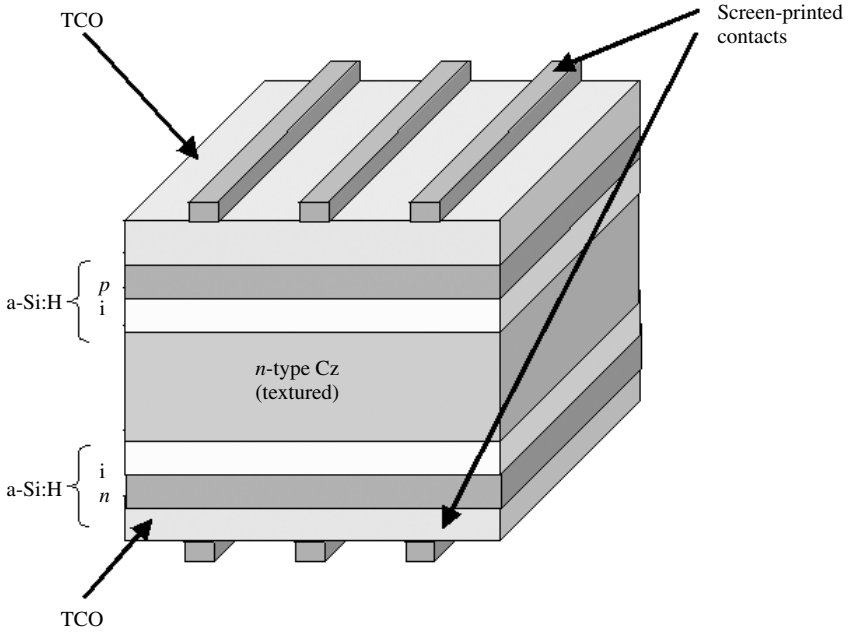

Figure 7.14 Structure of the HIT cell

PECVD [120]. It provides an excellent surface passivation with very low temperature processes (below 200°C), avoiding lifetime degradation of the bulk material. Figure 7.14 shows the structure of the HIT cell. A textured *n*-type Cz-Si substrate is used. The emitter and BSF are made of *p*-type and *n*-type a-Si layers, respectively. Very thin intrinsic a-Si layers are inserted between a-Si and the crystalline substrate, to improve the characteristics of the a-Si/c-Si interface. Thickness of these amorphous layers is on the order of 10 to 20 nm. On both doped layers, transparent conductive oxide (TCO) layers are formed, by sputtering, and metal fingers are screen printed. Back metallization is also comblike to reduce thermal and mechanical stresses, making the cell symmetrical and enabling it to perform as a bifacial cell.

In 1994, 20% efficiency was achieved with a similar HIT structure on a 1 cm^2 cell. Mass production of HIT cells started in 1997, with conversion efficiencies of 17.3% on 100 cm^2 substrates. 180 W modules are fabricated, and special modules exist for roof-tile and bifacial applications.

7.7.3 Buried Contact Technology

The buried contact solar cell process was developed at the University of New South Wales [50]. It is based on forming grooves in the silicon surface, where the metal is deposited by electroless plating, so that high aspect ratios and low metal shading losses are achieved. Several techniques have been proposed for groove formation, laser scribing being the most attractive for large-scale production. A metallized groove, typically 40-μm deep and 20-μm wide, is presented in Figure 7.15. Additionally, other high-efficiency