9.4.2 Three-terminal Voltage-matched Interconnections

In contrast, in the three-terminal configuration the subcells are not electrically isolated; the bottom of each cell is electrically connected to the top of the cell beneath it. The fabrication of a monolithic three-terminal device is relatively straightforward, although more complex than the fabrication of a two-terminal device. The semiconductor structure must be designed to provide a layer for contact to the intermediate terminal, and to accommodate the processing steps necessary to put the intermediate terminal in place. With this intermediate terminal, the different subcells in the stack do not have to have the same photocurrents. Furthermore, in this three-terminal configuration, the different subcells in the stack may have different polarities, for example, p/n for the top cell and n/p for the bottom cell. Module-level interconnection of four- and three-terminal devices is discussed in detail by Gee [17].

9.4.3 Two-terminal Series-connected (Current Matched)

The two-terminal series-connected configuration provides the most restrictions for interconnection of the devices. This configuration requires that the subcells be of the same polarity and that the photocurrents of the subcells be closely matched, since in this series connection the subcell with the least photocurrent limits the current generated by the entire device. This current-matching constraint, about which more will be said shortly, puts relatively tight constraints on the selection of band gaps for the various junctions in this structure. Against these disadvantages, however, are critical advantages. The existence of high-quality monolithic tunnel-junction subcell interconnects means that these stacks can be made as monolithic two-junction structures with metallization at the very top and bottom of the stack only. This, in turn, means that such devices can be integrated into modules with the same simplicity afforded by single-junction devices. The two-terminal, series-connected configuration will be the focus of the following sections, in which we analyze in detail the dependence of the cell performance on the cell design parameters.

9.5 COMPUTATION OF SERIES-CONNECTED DEVICE PERFORMANCE

9.5.1 Overview

This section discusses the quantitative modeling of the performance of series-connected, two-terminal, two-junction devices. This analysis will provide the basis for a qualitative understanding of the general trends in series-connected multijunction devices, as well as the quantitative design of these devices. Emphasis is placed on selecting band gap pairs and predicting the efficiency of the resulting structures. This modeling also lays the groundwork for the analysis of the dependence of the device performance on the spectrum, the concentration, and the temperature. Although the emphasis is on two-junction devices, we will occasionally extend the discussion to the analysis of a three-junction device, GaInP/GaAs/Ge, which is of special interest due to its technical and commercial success in space applications. Following the treatments of References [7, 18], we make