due to circuit inductance [178], and the points off the curves at low frequencies are due to an apparatus anomaly. Typically, a frequency in the middle of the flat region, in this case 75 kHz, is chosen for subsequent $C-V$ measurements.

Capacitance versus voltage data at 75 kHz is plotted in Figure 14.25(b) in the commonly used C^{-2} versus V format, in which the vertical axis is proportional to the square of the depletion width, w, for a given voltage, since $C/A = \varepsilon/w$. The slope is inversely proportional to the carrier density at the depletion edge. In this case, there are two distinct regions. In reverse bias, the C^{-2}, and hence the depletion width, changes very little. Near zero bias and into forward bias, however, the depletion width narrows considerably.

The same data can be plotted (Figure 14.25c) as hole density ρ versus depletion width, which is referred to as the distance from the junction, since the depletion is assumed to be essentially all in the absorber. The two regions suggested by the C^{-2} versus V plot have become extremely clear. For the first 3 μm into the CdTe, the hole density is very low (mid 10^{14} range), but then it increases dramatically. The interpretation is that 3 μm is the thickness of the CdTe layer, and the rapid increase in hole density takes place as the depletion edge enters the back-contact region. In fact, the measured thickness of this particular CdTe was somewhat larger than 3 μm, and in general the electronic thickness is comparable to the physical thickness. The likely explanation is that there are local areas such as grain boundaries and highly defective grains where the back-contact material penetrates into the CdTe and effectively reduces its thickness. Following the elevated temperature cycles that led to Figure 14.23, there can also be a reduction in net CdTe thickness.

CdTe solar cells fabricated by a variety of the techniques illustrated in Figure 14.6 have shown hole densities between 1×10^{14} and $8 \times 10^{14}/\text{cm}^3$ as determined by the capacitance technique. A relatively low carrier density may be an impediment to higher-efficiency cells. It suggests that compensating native donors remain a problem for the CdTe cells made to date. The direct impact of the low hole density is that the Fermi level is 250 to 350 mV from the valence-band maximum, and hence limits the junction barrier, and therefore V_{OC}. A bigger, and probably related, problem is that the low densities are likely to be symptomatic of the excessive recombination states responsible for much of the voltage and fill-factor difference seen in Figure 14.21.

14.3.6 Summary of CdTe-cell Status

During the past 20 years, there has been major progress in refining the basic CdTe cell structure of Bonnet and Rabenhorst. The highest current densities achieved are similar to crystalline GaAs when adjusted for small differences in band gap. Open-circuit voltage and fill factor are limited by excessive forward-current recombination and low carrier density, but have nevertheless achieved values about 80% as large as GaAs, again adjusted for band gap. The recombination current appears to follow the Shockley–Read–Hall mechanism through distributed states in the space charge region [179]. There is some concern about the diffusion of copper atoms, but significant degradation under normal operating conditions for well-fabricated cells is unlikely. Although cell-level basic research should certainly continue, the status of CdTe solar cells is clearly healthy enough to proceed with mainstream commercialization.