



SERVICE MANUAL

DIGITAL TRANSCEIVER

ID-1

S-14120IZ-C1

May. 2005

Icom Inc.

INTRODUCTION

This service manual describes the latest service information for the **ID-1** DIGITAL TRANSCEIVER at the time of publication.

MODEL	VERSION	SYMBOL	RC-24
ID-1	U.S.A.	USA-2	Optional
		USA-3	Supplied
	Europe	EUR-2	Optional
		EUR-3	Supplied
	General	GEN-2	Optional
		GEN-3	Supplied

To upgrade quality, all electrical or mechanical parts and internal circuits are subject to change without notice or obligation.

DANGER

NEVER connect the transceiver to an AC outlet or to a DC power supply that uses more than 16 V. Such a connection could cause a fire or electric hazard.

DO NOT expose the transceiver to rain, snow or any liquids.

DO NOT reverse the polarities of the power supply when connecting the transceiver.

DO NOT apply an RF signal of more than 20 dBm (100 mW) to the antenna connector. This could damage the transceiver's front end.



ORDERING PARTS

Be sure to include the following four points when ordering replacement parts:

1. 10-digit order numbers
2. Component part number and name
3. Equipment model name and unit name
4. Quantity required

<SAMPLE ORDER>

2710000590 Fan MF40D-12H-001 ID-1 Chassis 2 pieces
8900010940 Cable OPC-1119 RC-24 Chassis 3 pieces

Addresses are provided on the inside back cover for your convenience.

REPAIR NOTES

1. Make sure a problem is internal before disassembling the transceiver.
2. **DO NOT** open the transceiver until the transceiver is disconnected from its power source.
3. **DO NOT** force any of the variable components. Turn them slowly and smoothly.
4. **DO NOT** short any circuits or electronic parts. An insulated turning tool **MUST** be used for all adjustments.
5. **DO NOT** keep power ON for a long time when the transceiver is defective.
6. **DO NOT** transmit power into a signal generator or a sweep generator.
7. **ALWAYS** connect a 30 dB to 40 dB attenuator between the transceiver and a deviation meter or spectrum analyzer when using such test equipment.
8. **READ** the instructions of test equipment thoroughly before connecting equipment to the transceiver.

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SECTION 1 SPECIFICATIONS

■ GENERAL

- Frequency coverage : 1240.000–1300.000 MHz
- Type of emission : FM, GMSK (Digital)
- Transmission speed (theoretical value) : Data 128 kbps
Digital voice 4.8 kbps
- Codec : AMBE (2.4 kbps)
- Number of memory channel : 105 (incl. 2 scan edges and 3 calls)
- Tuning steps : 5, 6.25, 10, 12.5, 20, 25, 50, 100 kHz
- Frequency stability : ± 2.5 ppm (-10°C to $+60^{\circ}\text{C}$)
- Operating temperature range : -10°C to $+60^{\circ}\text{C}$ (-22°F to $+140^{\circ}\text{F}$)
- Antenna connector : Type-N ($50\ \Omega$)
- Power supply requirement : 13.8 V DC $\pm 15\%$ (Negative ground)
- Current drain (at 13.8 V DC) : Transmit Less than 7 A (at 10 W)
Receive Less than 1.5 A (AF max.)
- Dimensions (projections not included) :
 - Main unit 141(W) \times 40(H) \times 165.8(D) mm; $5^{9/16}$ (W) \times $1^{9/16}$ (H) \times $6^{17/32}$ (D) in
 - Remote controller (RC-24) 150(W) \times 50(H) \times 49.5(D) mm; $5^{29/32}$ (W) \times $1^{31/32}$ (H) \times $6^{15/16}$ (D) in
- Weight (Approx.) :
 - Main unit 1.2 kg; 2 lb 10 oz
 - Remote controller (RC-24) 220 g; 7.7 oz

■ TRANSMITTER

- Output power (at 13.8 V DC) : 10/1 W
- Modulation : Variable reactance frequency modulation (FM)
Quadrature modulation (Digital)
- Maximum frequency deviation (FM) : ± 5.0 kHz
- Spurious emissions : Less than -50 dB
- Microphone connector : 8-pin modular jack ($600\ \Omega$)

■ RECEIVER

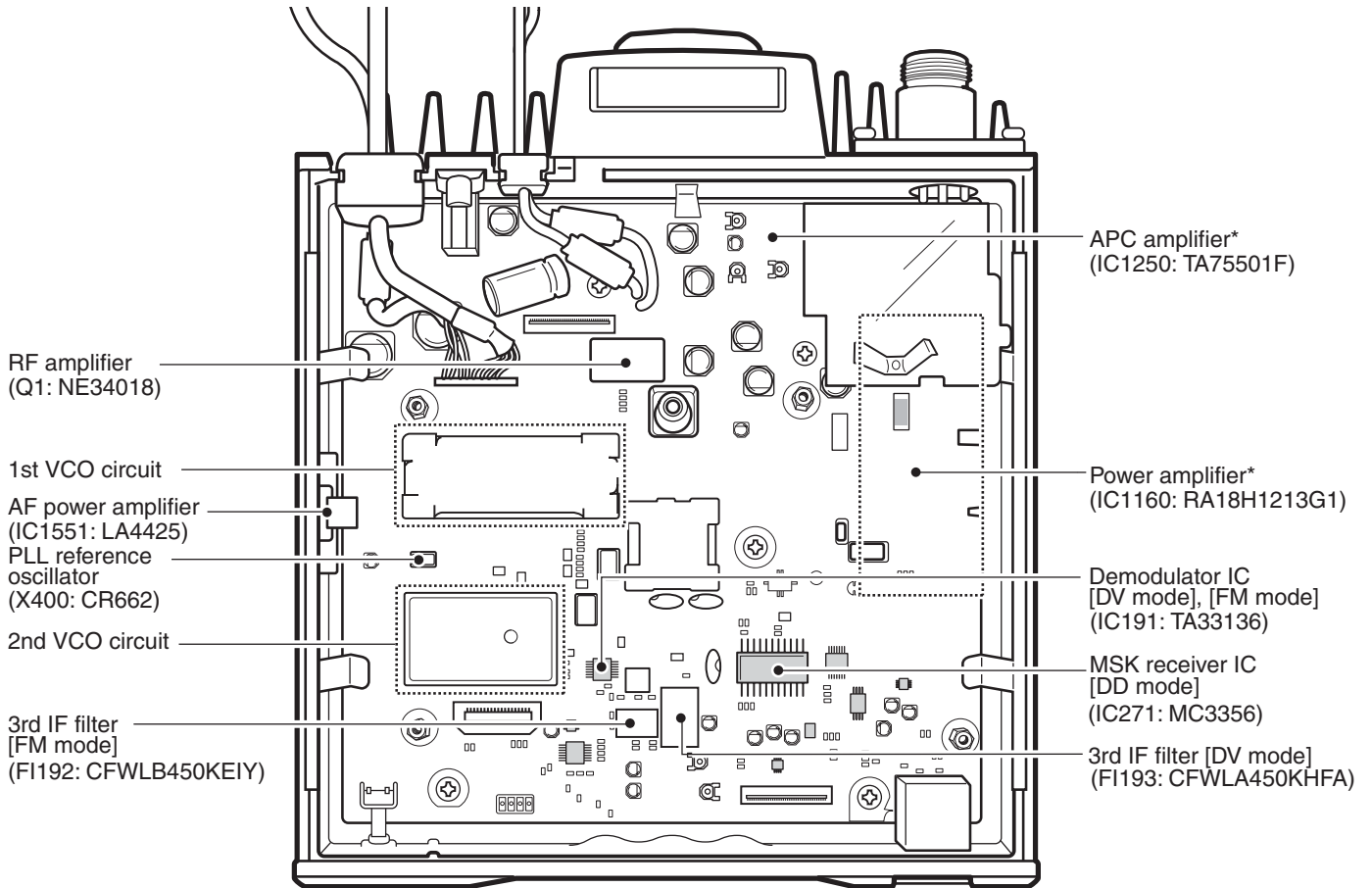
- Receive system : Triple conversion superheterodyne system (FM, DV)
Double conversion superheterodyne (DD)
- Intermediate frequencies : 1st IF: 243.95 MHz, 2nd IF: 31.05 kHz, 3rd IF: 450 kHz (FM, DV)
1st IF: 243.95 MHz, 2nd IF: 10.7 MHz (DD)
- Sensitivity : Less than $0.18\ \mu\text{V}$ (-122 dBm) at 12 dB SINAD (FM)
Less than $0.35\ \mu\text{V}$ (-116 dBm) at BER 1×10^{-2} (DV)
Less than $1.58\ \mu\text{V}$ (-103 dBm) at BER 1×10^{-2} (DD)
- Selectivity (typical) : More than 12 kHz/6dB, Less than 30 kHz/60 dB (FM)
More than 6 kHz/6dB, Less than 18 kHz/50 dB (DV)
More than 140 kHz/6dB, Less than 520 kHz/40 dB (DD)
- Spurious and image rejection : More than 50 dB
- Audio output power (at 13.8 V DC) : 2.0 W at 10% distortion with an $8\ \Omega$ load
- Squelch sensitivity (at threshold) : Less than $0.18\ \mu\text{V}$ (-122 dBm) (FM only)
- Ext. speaker connector : 2-conductor 3.5 (d) mm ($1/8$ ")/ $8\ \Omega$

All stated specifications are subject to change without notice or obligation.

SECTION 2 INSIDE VIEWS

● MAIN UNIT

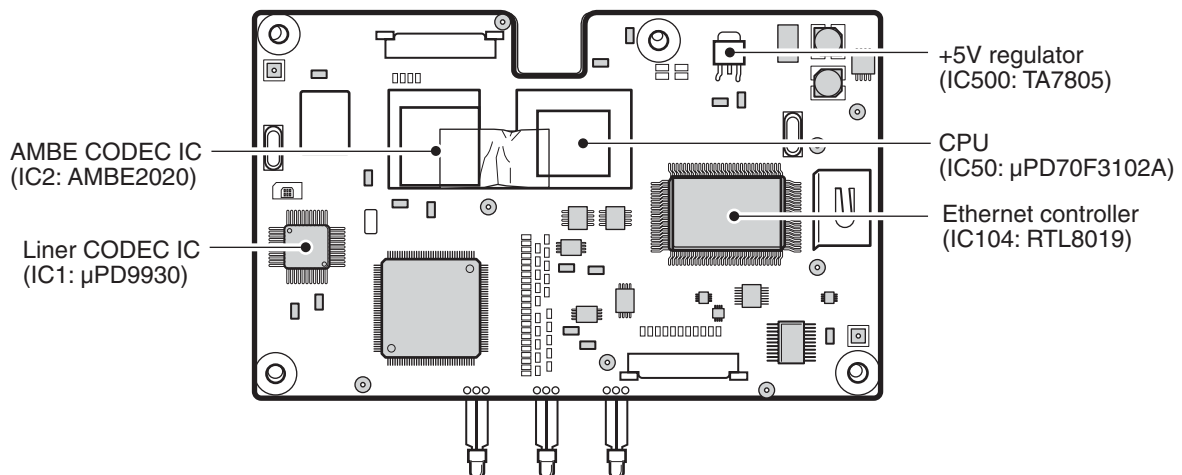
Top view



*: Located under side of this point

● LOGIC-1 UNIT

Top view

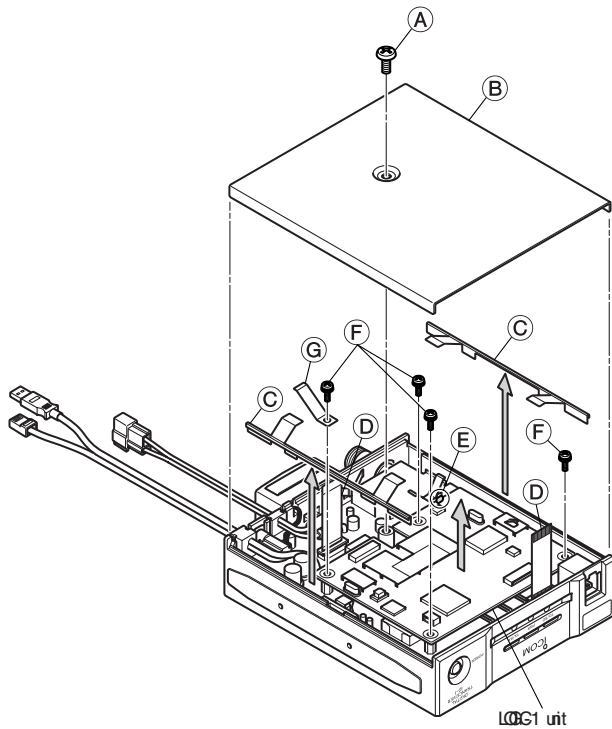


SECTION 3 DISASSEMBLY INSTRUCTIONS

3-1 ID-1

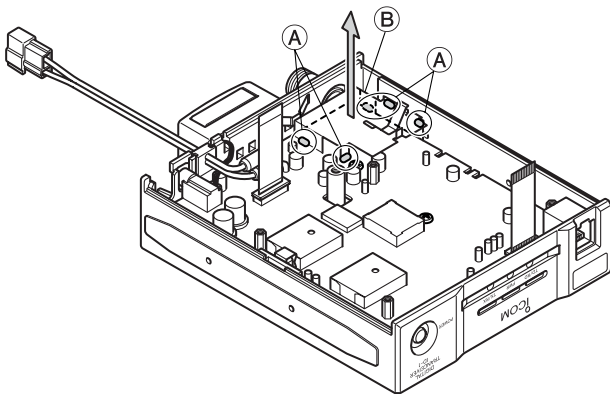
● REMOVING THE LOGIC-1 UNIT

- ① Unscrew 1 screw (A), and remove the cover (B).
- ② Remove 2 main shield plates (C).
- ③ Disconnect 2 cables (D), and unsolder 1 point (E).
- ④ Unscrew 4 screws (F), and remove the earth spring (G).
- ⑤ Take off the LOGIC-1 unit.



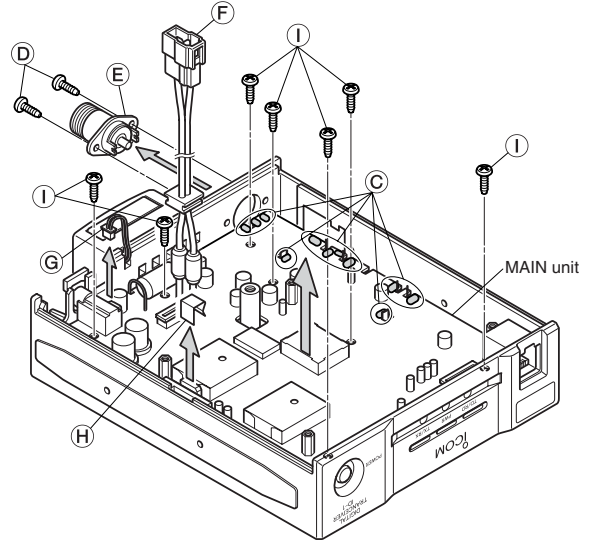
● REMOVING THE MAIN UNIT

- ① Unsolder 5 points (A), and remove the ANT plate (B).



Continue to right above.

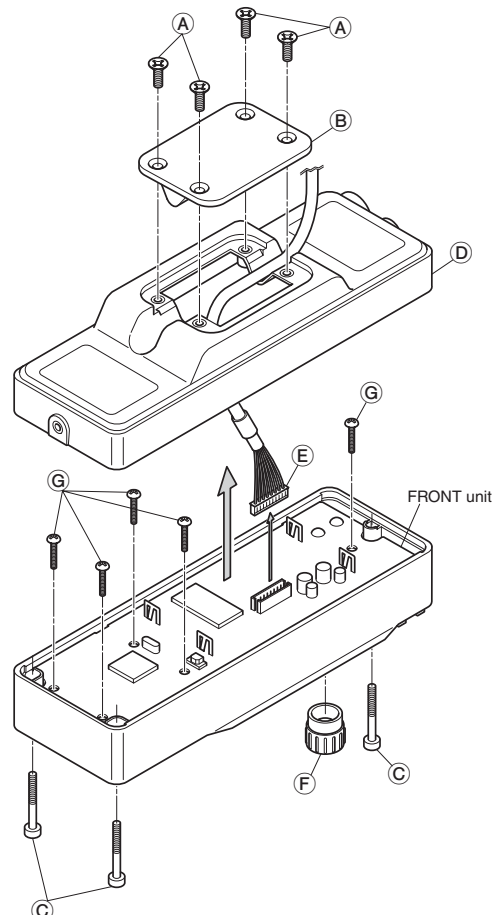
- ② Unsolder 11 points (C).
- ③ Unscrew 2 screws (D), and remove the ANT connector (E).
- ④ Take off the cable (F) from the chassis.
- ⑤ Disconnect the cable (G), and remove the TR-A clip (H).
- ⑥ Unscrew 7 screws (I), and take off the MAIN unit.



3-2 RC-24

● REMOVING THE FRONT UNIT

- ① Unscrew 4 screws (A), and remove the rear plate (B).
- ② Unscrew 3 screws (C), and remove the front panel (D).
- ③ Disconnect the cable (E), and remove the knob (F).
- ④ Unscrew 5 screws (G), and take off the FRONT unit.



SECTION 4 CIRCUIT DESCRIPTION

4-1 RECEIVER CIRCUITS

4-1-1 ANTENNA SWITCHING CIRCUIT (MAIN UNIT)

The antenna switching circuit functions as a low-pass filter while receiving and a resonator circuit while transmitting. This circuit does not allow transmit signals to enter the receiver circuits.

Received signals from the antenna connector (CHASSIS; J1) are passed through the low-pass filter which contains strip-line and C1198, and are then applied to the $\lambda/4$ type antenna switching circuit (D1160–D1162, L1162).

While receiving, no voltage is applied to D1160–D1162. Thus, the receive line and ground are disconnected and received signals are applied to the RF circuit.

4-1-2 RF CIRCUIT (MAIN UNIT)

The RF circuit amplifies signals within the range of frequency coverage and filters out-of-band signals.

The signals from the antenna switching circuit pass through the high-pass filter (L1–L4, C2–C5) and then applied to the RF amplifier (Q1). The amplified signals are passed through the bandpass filter (F11) and then applied to the another RF amplifier (Q2). The amplified signals are passed through the another bandpass filter (F12) to suppress unwanted signals.

The filtered signal is applied to the 1st mixer circuit.

4-1-3 1ST MIXER AND 1ST IF CIRCUITS (MAIN UNIT)

The 1st mixer circuit converts the received signals into fixed frequency of the 1st IF signal with the 1st LO signal. By changing the 1st LO signal, only the desired frequency passes through the bandpass filter at the next stage of the 1st mixer circuit.

The RF signals from the bandpass filter (F12) are mixed with the 1st LO signal, where come from the 1st VCO circuit, at the 1st mixer circuit (IC71) to produce a 243.95 MHz 1st IF signal. The 1st IF signal is passed through the bandpass filter (F171) to suppress unwanted signals and pass only the desired signals.

The filtered signal is applied to the 2nd IF circuit.

4-1-4 2ND MIXER AND 2ND IF CIRCUITS (MAIN UNIT)

The 2nd mixer circuit converts the 1st IF signal into the 2nd IF signal with the 2nd LO signal.

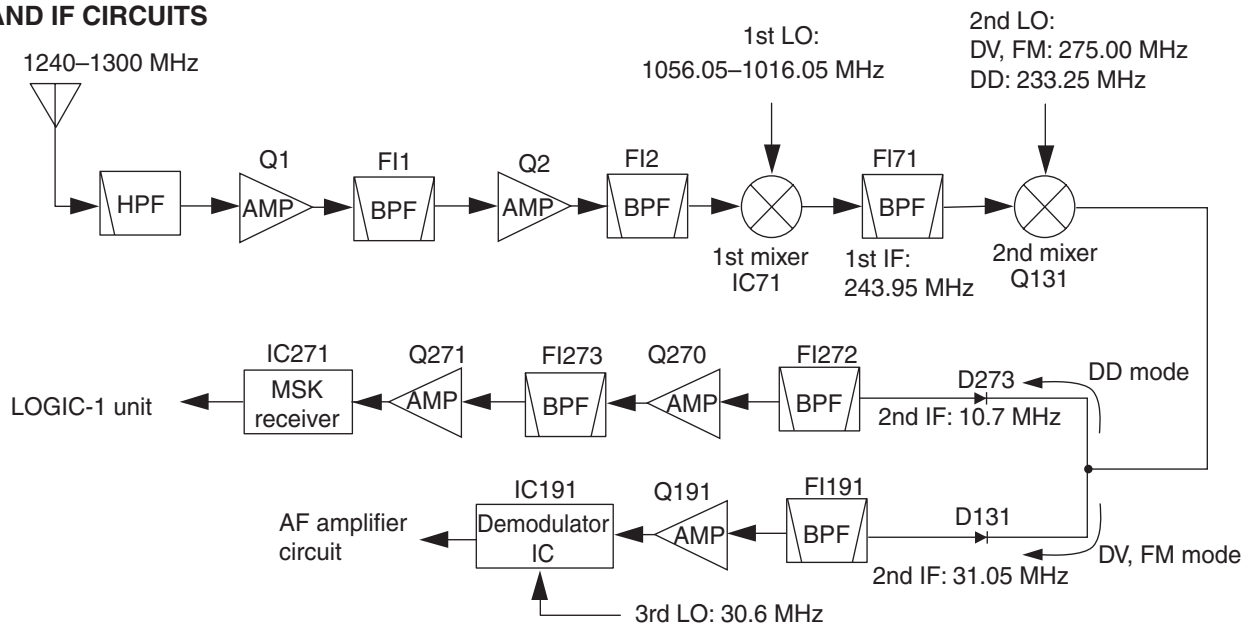
• DV/FM MODE

The filtered 1st IF signal from the bandpass filter (F171) is mixed with the 2nd LO signal (275.00 MHz), where come from 2nd VCO circuit, at the 2nd mixer circuit (Q131) to produce the 2nd IF signal (31.05 MHz). The 2nd IF signal is passed through the MCF (F1191) via the DV/FM switch (D131). The filtered signal is applied to the IF amplifier (Q191) and then applied to the 3rd mixer circuit in the demodulator IC (IC191).

• DD MODE

The filtered 1st IF signal from the bandpass filter (F171) is mixed with the 2nd LO signal (233.25 MHz), where come from the 2nd VCO circuit, at the 2nd mixer circuit (Q131) to produce the 2nd IF signal (10.7 MHz). The 2nd IF signal is passed through the bandpass filter (F1272) to remove unwanted heterodyned frequencies via the DD switch (D273). The filtered signal is amplified at the IF amplifier (Q270) and then passed through the another bandpass filter (F1273). The filtered signal is applied to the another IF amplifier (Q271) and then applied to the MSK receiver IC (IC271).

• RF AND IF CIRCUITS



4-1-5 DEMODULATOR CIRCUITS (MAIN UNIT)

• DV MODE

The demodulator IC (IC191) contains the 3rd mixer, limiter amplifier, quadrature detector, active filter and noise amplifier, etc.

The amplified signal from the IF amplifier (Q191) is applied to the 3rd mixer section of the demodulator IC (IC191, pin 16) and is then mixed with the 3rd LO signal to be converted into the 450 kHz 3rd IF signal. The 3rd IF signal from the 3rd mixer section (IC191, pin 3) passes through the ceramic filter (F1193) via the mode switches (D192, D193) to remove unwanted heterodyned frequencies. The filtered signal is amplified at the limiter amplifier section (IC191, pin 5) and then applied to the quadrature detector section (IC191, pins 10, 11) to demodulate the digital audio signals.

The 3rd LO signal (30.6 MHz) is produced at the 1st PLL circuit by doubling its reference frequency (X400: 15.3 MHz) at the doubler (Q550).

The digital audio signals from the demodulator IC (IC191, pin 9) are amplified at IC343 (pins 6, 7) and then applied to the mode switch (IC342, pins 1, 7).

The switched signals from the mode switch (IC342, pin 1) are applied to the LOGIC-1 unit via J1801 (pin 20).

• DD MODE

The MSK receiver IC (IC271) contains the limiter amplifier, quadrature detector, etc.

The amplified signal from the IF amplifier (Q271) is applied to the limiter amplifier section of the MSK receiver IC (IC271, pin 7) and then applied to the quadrature detector section (IC271, pin 11) to demodulate to the data signals.

The demodulated data signals from the MSK receiver IC (IC271, pin 13) are amplified at IC343 (pins 1, 2) and then applied to the mode switch (IC342, pins 1, 6).

The switched signals from the mode switch (IC342, pin 1) are applied to the LOGIC-1 unit via J1801 (pin 20).

• FM MODE

The same demodulator IC that is used for DV mode operation is used for FM demodulation.

The amplified signal from the IF amplifier (Q191) is applied to the 3rd mixer section of the demodulator IC (IC191, pin 16) and is then mixed with the 3rd LO signal to be converted into the 450 kHz 3rd IF signal. The 3rd IF signal from the 3rd mixer section (IC191, pin 3) passes through the ceramic filter (F1192) via the mode switches (D192, D193) to remove unwanted heterodyned frequencies. The filtered signal is amplified at the limiter amplifier section (IC191, pin 5) and then applied to the quadrature detector section (IC191, pins 10, 11) to demodulate the AF signals.

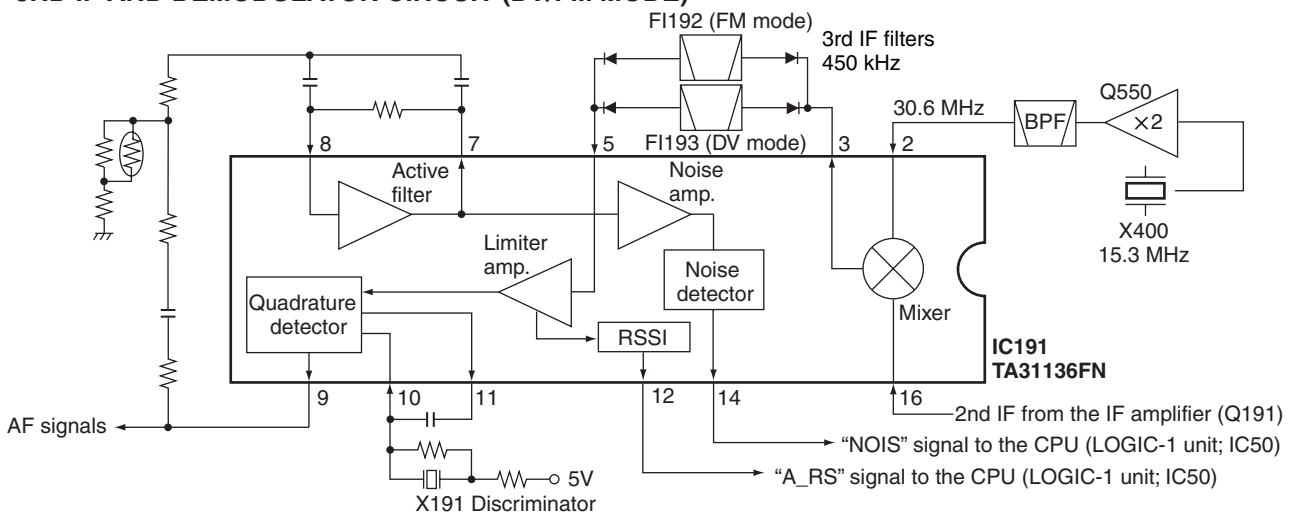
The AF signals are output from the demodulator IC (IC191, pin 9) and are then applied to the AF amplifier circuit.

4-1-6 DIGITAL CIRCUITS (LOGIC-1 UNIT)

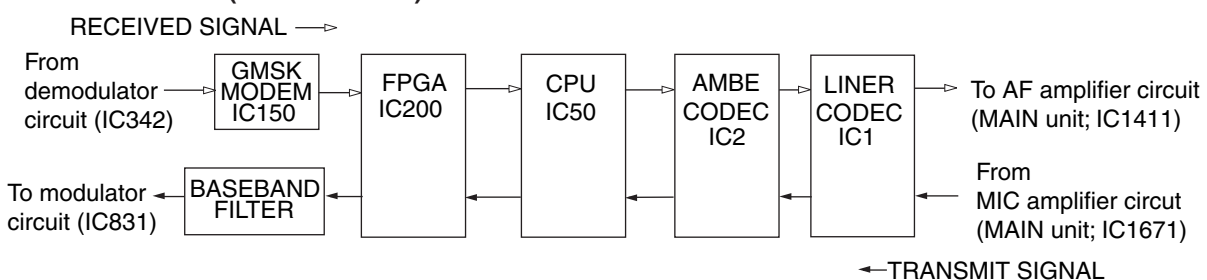
The digital circuits convert the demodulated digital audio signals into the analog audio signals and convert the demodulated data signals format for PC communication via the USB controller (for DV mode: low speed data operation) or Ethernet controller (for DD mode).

The demodulated digital audio or data signals from the mode switch (MAIN unit: IC342, pin 1) are applied to the GSMK MODEM IC (IC150, pin 11). The applied signals are synchronized with the clock signal, then the synchronized

• 3RD IF AND DEMODULATOR CIRCUIT (DV/FM MODE)



• DIGITAL CIRCUITS (LOGIC-1 UNIT)



signals are applied to the CPU (IC50) via the FPGA IC (IC200).

• DV MODE (VOICE OPERATION)

The digital audio signals from the CPU (IC50) are applied to the AMBE CODEC IC (IC2) for code expansion, and are then applied to the linear CODEC IC (IC1). The digital audio signals are converted into analog audio signals at the D/A converter section and then output from pin 34 (IC1)

The analog audio signals are applied to the mode switch (MAIN unit; IC1411, pins 1, 7) via the J101 (pin 30) as "DAF" signal.

• DD MODE/DV MODE (LOW SPEED DATA OPERATION)

While operating in DD mode, the output signals from the CPU (IC50) are applied to the connected PC via the Ethernet controller (IC104).

While operating in DV mode (low speed data operation), the output signals from the CPU (IC50) are applied to the connected PC via the USB controller (IC550).

4-1-7 AF AMPLIFIER CIRCUIT (MAIN UNIT)

The AF amplifier circuit amplifies the demodulated AF signals to a level needed to drive a speaker.

• DV MODE

The AF signals from the LOGIC-1 unit are applied to the mode switch (IC1411, pins 1, 7) and then amplified at the buffer amplifier (IC1460, pins 1, 3). The buffer amplified signals are applied to the filter switch (IC1462, pins 1, 6) to select the appropriate AF filters for DV mode and then passed through the low-pass (IC1461, pins 8, 10) and high-pass (IC1461, pins 12, 14) filters. The filtered signals are passed through the filter switch (IC1463, pins 1, 6) and are then applied to the volume controller (IC1550, pins 2, 9).

• FM MODE

The AF signals from the demodulator IC (IC191, pin 9) are applied to the mode switch (IC1411, pins 1, 6) and then applied to the buffer amplifier (IC1460, pins 1, 3). The buffer amplified signals are applied to the filter switch (IC1462, pins 1, 7) to select the appropriate AF filters for FM mode and then passed through the low-pass (IC1460, pins 6, 7, 8, 9) and high-pass (IC1460, pins 13, 14) filters. The filtered signals are passed through the filter switch (IC1463, pins 1, 7) and are then applied to the volume controller (IC1550, pins 2, 9).

The switched AF signals from the filter switch (IC1463, pin 1) are applied to the volume controller (IC1550, pins 2, 9). The level adjusted AF signals (IC1550, pin 9) are applied to the AF power amplifier (IC1551, pins 1, 4) via the AF mute switch (Q1550).

The AF mute switch is mute the AF signals while digital squelch, call sign squelch, noise squelch, tone squelch are closed, the audio level is set to minimum position or transmitting.

The power amplified AF signals from the AF power amplifier (IC1551, pin 4) are applied to the speaker that is connected to [SP] jack (J1550).

4-1-8 SQUELCH CIRCUITS (MAIN UNIT)

• DIGITAL CODE/CALL SIGN SQUELCH (DV MODE ONLY)

The digital code/call sign squelch circuit detects matched digital code/call sign and opens the squelch only when receiving a signal containing a matching digital code/call sign. When digital code/call sign squelch is in use, and a signal with a unmatched digital code/call sign is received, the digital code/call sign squelch circuit mutes the AF signals.

The detected digital audio signals from IC191 (pin 9) are applied to the CPU (LOGIC-1 unit; IC50) via the mode switch (IC342, pins 1, 7), GMSK MODEM IC (LOGIC-1 unit; IC150) and FPGA IC (LOGIC-1 unit; IC200). Then the CPU analyzes the digital code/call sign and output the AF mute signal as "RMUT" from the pin 102 to the filter switch (IC1463, pin 2) via the mute switch (LOGIC-1 unit; Q155).

• NOISE SQUELCH (FM MODE ONLY)

The noise squelch circuit cuts out AF signals when no RF signals are received. By detecting noise components in the AF signals, the squelch circuit switches the filter switch (IC1463).

Portion of the AF signals from the demodulator IC (IC191, pin 9) are applied to the active filter section in the demodulator IC (IC191, pin 8). The active filter section filters and amplifies noise components only. The amplified noise signals are converted into the pulse-type signals at the noise detector section. The detected signals output from pin 14 (IC191).

The detected signals from the demodulator IC (IC191, pin 14) are amplified at the noise amplifiers (Q192, Q193) and then applied to the noise detector (D195). The detected signals are applied to the CPU (LOGIC-1 unit; IC50, pin 32) as "NOIS" signals. Then the CPU analyzes the noise condition and outputs the AF mute signal as "RMUT" from the pin 102 to the filter switch (IC1463, pin 2) via the mute switch (LOGIC-1 unit; Q155).

• TONE SQUELCH (FM MODE ONLY)

The tone squelch circuit detects tone signals and opens the squelch only when receiving a signal containing a matching subaudible tone (CTCSS). When tone squelch is in use, and a signal with a unmatched or no subaudible tone is received, the tone squelch circuit mutes the AF signals even when noise squelch is open.

A portion of "DEAF" signals from the buffer amplifier (IC1460, pin 1) are applied to the low-pass filters (IC1461, pins 1, 2, 5, 7) to remove AF (voice) signals. The filtered signals are applied to the CTCSS decoder in the CPU (LOGIC-1 unit, IC50, pin 33) as "TONI" signals. Then the CPU analyzes the decoded tone signals and output the AF mute signal as "RMUT" from the pin 102 to the filter switch (IC1463, pin 2) via the mute switch (LOGIC-1 unit; Q155).

4-1-9 S-METER CIRCUITS (MAIN UNIT)

Some of the amplified IF signal is applied to the S-meter detector section in the demodulator IC (IC191) to be converted into DC voltage. The output signal from the demodulator IC (IC191, pin 12) is applied to the mode switch (IC341, pins 10, 11) and then applied to the CPU (LOGIC-1 unit; IC50). The CPU then outputs S-meter control signal to the RC-24 or connected PC via the USB controller (LOGIC-1 unit; IC550).

4-2 TRANSMITTER CIRCUITS

4-2-1 MICROPHONE AMPLIFIER CIRCUIT (MAIN UNIT)

The microphone amplifier circuit amplifies audio signals from the microphone to a level needed for the modulation circuit.

While connecting the microphone to ID-1, the AF signals from the microphone (J1600, pin 6) are applied to the microphone amplifier (Q1673) via the microphone mute switch (Q1670). The amplified AF signals are applied to the mode switch (IC1670, pins 1, 6, 7).

While connecting the microphone to RC-24, the AF signals from the microphone (RC24; J1) are applied to the MAIN unit (J1600, pin 6) via the buffer amplifier (RC-24; Q13).

• DV MODE

The amplified AF signals from microphone amplifier (Q1673) are amplified at the ALC amplifier (IC1672, pins 3, 5) via the mode switch (IC1670, pins 1, 7). The amplified signals are applied to the IDC amplifier (IC1671, pins 6, 7) and then passed through the splatter filter (IC1671, pins 1, 3).

The filtered signals are applied to the LOGIC-1 unit via the J1801 (pin 10).

• FM MODE

The amplified AF signals from microphone amplifier (Q1673) are passed through the mode switch (IC1670, pins 1, 6) and then applied to the IDC amplifier (IC1671, pins 6, 7). The amplified signals are passed through the splatter filter (IC1671, pins 1, 3) and mode switch (IC1673, pins 1, 6).

The CTCSS signals (CTCS) from the CPU (LOGIC-1 unit; IC50) via (LOGIC-1 unit; IC57, pin 1) are mixed with the AF signals from the IDC amplifier (IC1671, pin 7). The mixed signals are passed through the splatter filter (IC1671, pins 1, 3) and mode switch (IC1673, pins 1, 6).

The switched AF signals (IC1673, pin 6) are applied to the modulation circuit.

4-2-2 DIGITAL CIRCUITS (LOGIC-1 UNIT)

• DV MODE (VOICE OPERATION)

The AF signals from the splatter filter (MAIN unit; IC1671, pin 1) are applied to the liner CODEC IC (IC1, pin 24) to convert into digital voice data at the A/D converter section as the "DAMOD" signal. The converted digital audio signals are applied to the AMBE CODEC IC (IC2) for code compression and are then applied to the CPU (IC50).

The digital audio signals are processed at the CPU (IC50) and then applied to the FPGA IC (IC200).

• DD MODE/DV MODE (LOW SPEED DATA OPERATION)

While operating in DD mode the data signal from connected PC are applied to the Ethernet controller (IC104) and then applied to the CPU (IC50)

While operating in DV mode (low speed data operation) the data signal from connected PC are applied to the USB controller (IC550) and then applied to the CPU (IC50)

The applied data signals to the CPU (IC50) are processed and then applied to the FPGA IC (IC200).

The output signals from the CPU (IC50) are applied to the FPGA IC (IC200) to convert to the I/Q baseband signals and then output from pins 75–80, 82–87, 92–99 (IC200). The I/Q baseband signals are mixed at the resistors (R250–R293) and then pass through the baseband filters (IC300, IC301, IC302).

The filtered signals (I/Q baseband signals) are applied to the MAIN unit via J400 (pins 1, 3).

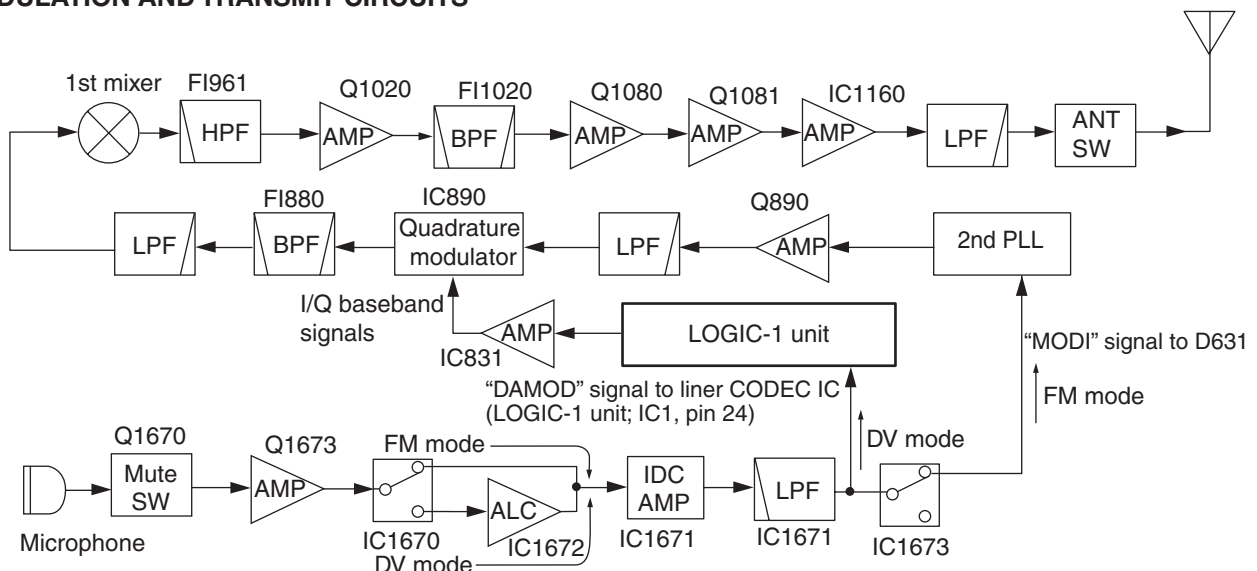
4-2-3 MODULATION CIRCUIT (MAIN UNIT)

• DV/DD MODE

The modulation circuit modulates the 2nd LO signal at the quadrature modulation circuit (IC890) using the I/Q baseband signals from the LOGIC-1 unit.

The I/Q baseband signals from the LOGIC-1 unit are amplified at the I/Q baseband amplifiers (IC832, pins 1, 2, 6, 7) and then applied to amplifier section (pins 4, 7) of the quadrature modulator IC (IC890, pins 4, 7, 14). The 2nd LO signal is applied to the quadrature modulator IC (IC890, pin 8)

• MODULATION AND TRANSMIT CIRCUITS



and then mixed with the amplified I/Q baseband signals. The modulated signal is output from pin 14.

The modulated signal (IC890, pin 14) is passed through the bandpass (F1880) and low-pass (L892, L893, C904–C908) filters and then applied to the 1st mixer circuit.

• FM MODE

The modulation circuit modulates the 2nd LO signal using the microphone audio signals.

The switched AF signals from the mode switch (IC1673, pin 6) change the reactance of varactor diode (D631) to modulate the 2nd LO signal at the 2nd VCO circuit (Q631, D630). The modulated signal from the 2nd VCO circuit is amplified at the buffer amplifiers (Q632, Q771) and is then applied to the T/R switch (D770). The switched signal is applied to the 2nd LO amplifier (Q890) and then passed through the low-pass filter (L891, C896–C898), quadrature modulator IC (IC890), bandpass filter (F1880) and low-pass filter (L892, L893, C904–C908).

The filtered signal is applied to the 1st mixer circuit.

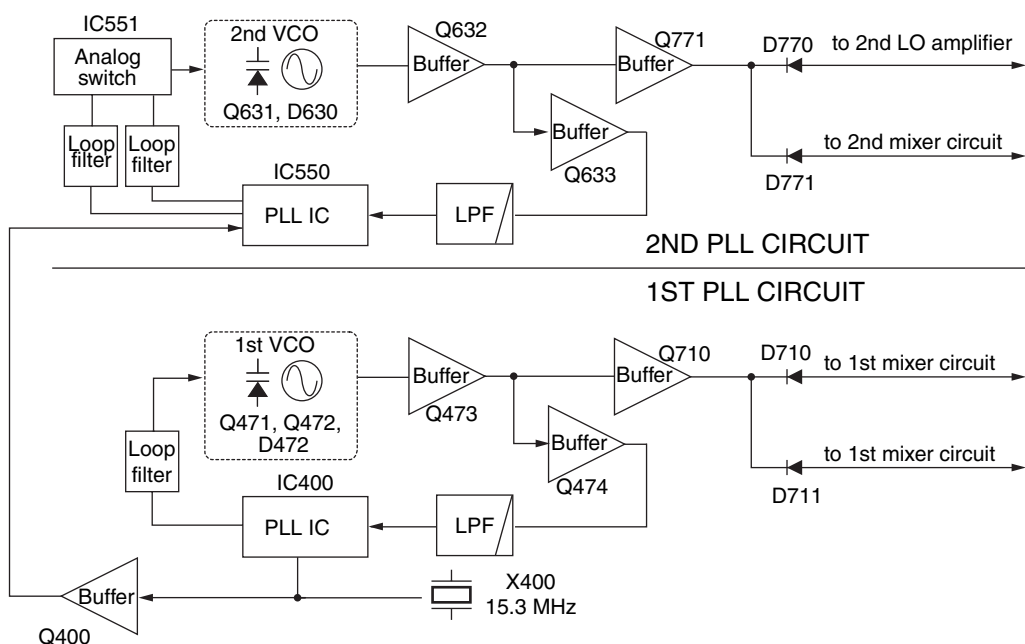
4-2-4 1ST MIXER CIRCUITS (MAIN UNIT)

The filtered signal from the low-pass filter (L892, L893, C904–C908) is mixed with the 1st LO signal, generated at the 1st VCO circuit (Q471, Q472, D472) via the buffer amplifier (Q710), at the 1st mixer circuit (IC960, pin 1, 6) to convert into the RF signal. The RF signal from the 1st mixer circuit (IC960, pin 6) is passed through the bandpass filter (F1961) and then amplified at the RF amplifier (IC1021). The amplified signal is passed through the bandpass filter (F11020) to suppress spurious components.

4-2-5 DRIVE/POWER AMPLIFIER CIRCUITS (MAIN UNIT)

The filtered RF signal from the bandpass filter (F11020) is amplified at the drive (Q1080, Q1081) and power (IC1160) amplifiers to obtain a stable 10 W of output power.

• PLL CIRCUITS



The power amplified signal from the power amplifier (IC1160, pin 4) is passed through the antenna switch (D1160), SWR detector circuit (D1166, D1170), low-pass filter which contains strip-line and C1198, and then applied to the antenna connector (CHASSIS unit: J1).

4-2-6 APC CIRCUIT (MAIN UNIT)

The APC circuit protects the driver and power amplifiers from a mismatched output load and stabilizes the output power.

The SWR detector circuit (D1166, D1170) detects the forward signals and reflection signals, and converts it into DC voltage. The output voltage is at a minimum level when the antenna impedance is matched with 50 Ω and is increased when it is mismatched.

The detected voltage is applied to the APC amplifier (IC1250, pins 3, 4) and is compared with the reference voltage which is supplied from the CPU (LOGIC-1 unit: IC50, pin 38) as "PCON" signal.

When antenna impedance is mismatched, the detected voltage exceeds the power setting voltage. The output voltage of the APC amplifiers (IC1250, IC1251) controls the bias voltage of the drive (Q1080) and power (IC1160) amplifiers to reduce the output power.

4-3 PLL CIRCUITS

4-3-1 PLL CIRCUITS (MAIN UNIT)

The PLL circuit provides stable oscillation of the 1st LO frequencies and 2nd LO frequency. The PLL output compares the phase of the divided VCO frequency to the reference frequency. The PLL output frequency is controlled by the divided ratio (N-data) of a programmable divider.

4-3-2 1ST PLL CIRCUIT (MAIN UNIT)

The 1st PLL circuit oscillates the 1st LO frequencies, and signals are applied to the 1st mixer circuit. The oscillated

signal from the 1st VCO (Q471, Q472, D471) is applied to the buffer amplifiers (Q473, Q474) and is then applied to the PLL IC (IC400, pin 6).

The PLL IC contains a prescaler, programmable counter, programmable divider and phase detector, etc.

The applied signal is divided at the prescaler and programmable counter section by the N-data ratio from the CPU (LOGIC-1 unit; IC50). The divided signal is detected on phase at the phase detector using the reference frequency and output from pin 4. The output signal is passed through the loop filter and is then applied to the 1st VCO circuit.

The oscillated signal at the 1st VCO is buffer amplified at Q473 and then passed through the low-pass (L474, L475, C488–C492) and high-pass (L47–L477, C493–C497) filters. The filtered signal is applied to the buffer amplifier (Q710) and then applied to the T/R switch (D710, D711).

The receive 1st LO signal from the T/R switch (D711) is applied to the 1st mixer circuit (IC71).

The transmit signal from the T/R switch (D710) is applied to the 1st mixer circuit (IC960).

A portion of the signal from the buffer amplifier (Q473) is fed back to the PLL IC (IC400, pin 6) via the buffer amplifier (Q474) as the comparison signal.

4-3-3 2ND PLL CIRCUIT (MAIN UNIT)

The 2nd PLL circuit oscillates the 2nd LO frequency, and the signal is applied to the 2nd mixer circuits.

The signal oscillated at the 2nd VCO circuit (Q631, D630) is amplified at the buffer amplifiers (Q632, Q633), then applied to the PLL IC (IC550, pins 2, 19). The applied signal is divided at the prescaler and programmable counter section by the N-data ratio from the CPU (LOGIC-1 unit; IC50). The divided signal is detected on phase at the phase detector using the reference frequency and output from pins 8, 13 (IC550).

While operating in DV/DD mode, the detected signal from pin 13 (IC550) is passed through the loop filter (R555–R557, C564, C567) and then applied to the 2nd VCO circuit via the mode switch (IC551, pins 1, 7).

While operating in FM mode, the detected signal from pin 8 (IC550) is passed through the loop filter (R559–R561, C571, C574) and then applied to the 2nd VCO circuit via the mode switch (IC551, pins 1, 6).

The oscillated signal at the 2nd VCO is amplified at the buffer amplifiers (Q632 Q771), and is then applied to the T/R switch (D770, D771).

The receive 2nd LO signal from the T/R switch (D771) is applied to the 2nd mixer circuit (Q131).

The transmit signal from the T/R switch (D770) is applied to the 2nd LO amplifier (Q890).

A portion of the signal from the buffer amplifier (Q632) is fed back to the PLL IC (IC550, pins 2, 19) via the buffer amplifier (Q633) and low-pass filter (L631, C653, C654) as the comparison signal.

4-4 POWER SUPPLY CIRCUITS

4-4-1 LOGIC-1 UNIT VOLTAGE LINE

Line	Description
5V	Common 5 V controlled by the +5 V regulator circuit (Q50 and Q51) using the "PWRS" signal from the CPU (IC50, pins 101).
3.3V	Common 3.3 V converted from the 5V line by the 3.3V regulator circuit (IC502).
3.2V	Common 3.2 V converted from the 5 V line by the 3.2V regulator circuit (IC4).

4-4-2 MAIN UNIT VOLTAGE LINE

Line	Description
HV	The voltage from a DC power supply.
VCC	The same voltage as the HV line which is controlled by the power switching circuit (Q23, Q24). When the power switch is pushed, the CPU outputs the "PWR" control signal to the power switching circuit to turn the circuit ON.
+9	Common 9 V converted from the HV line at the +9 CTRL circuit (IC1330). The output voltage is applied to the volume controller (IC1550), etc.
+5	Common 5 V converted from the +9V line at the 5 V regulator circuit (IC1331). The output voltage is applied to the mode switches (IC1462, IC1463), etc.
DM+5	Common 5 V converted from the +9V line at the 5 V regulator circuit (IC830). The output voltage is applied to the modulation amplifiers (IC831, IC832), etc.
T+9	Transmit 9 V controlled by the T+9 regulator circuit (Q1333, Q1334, D1331) using the "TXS" signal from the CPU (LOGIC-1 unit; IC50, pin 94). The output voltage is applied to the APC amplifier (IC1250), etc.
T+5	Transmit 5 V controlled by the T+5 regulator circuit (Q1336, D1332, D1333) using the "TXS" signal from the CPU (LOGIC-1 unit; IC50, pin 94). The output voltage is applied to the RF amplifier (IC1021), etc.
R+5	Receive 5 V controlled by the R+5 regulator circuit (Q1337) using the "RXS" signal from the CPU (LOGIC-1 unit; IC50, pin 95). The output voltage is applied to the RF amplifier (Q2) and 1st mixer (IC71), etc.
T+3	Transmit 3 V controlled by the T+3 regulator circuit (Q1342) using the "TXS" signal from the CPU (LOGIC-1 unit; IC50, pin 94). The output voltage is applied to the 1st mixer (IC960), etc.
R+3	Receive 3 V controlled by the R+3 regulator circuit (Q1343) using the "RXS" signal from the CPU (LOGIC-1 unit; IC50, pin 95). The output voltage is applied to the RF amplifier (Q1), etc.

4-5 PORT ALLOCATIONS

4-5-1 CPU (LOGIC-1 UNIT; IC50)

Pin number	Port name	Description
29	MU/D	Input port for up/down signal from the connected microphone.
32	NOIS	Input port for the noise signal from the noise detector (MAIN unit; D195).
31	RSSI	Input port for the S-meter signal from the demodulator IC (MAIN unit; IC191, pin 12).
33	TONI	Input port for CTCSS signal from the low-pass filter (MAIN unit, IC1461, pin 1).
42	TXD1	Output data signals to the USB controller (IC550, pin 24).
43	RXD1	Input port for data signals from the USB controller (IC550, pin 25) via the (IC553).
53	SDA	I/O port for data signals from/to the EEPROM (IC54, pin 5).
54	SCL	Outputs clock signal to the EEPROM (IC54, pin 6).
61	BEEP	Outputs beep audio signals.
71	RESET	Input port for reset signal from the reset IC (IC52, pin 1).
72	P2RSC	Outputs control signal to the mode switch (MAIN unit; IC551, pin 5) via the level converter (IC55).
73	P2STC	Outputs strobe signal to the 2nd PLL IC (MAIN unit; IC550, pin 3) via the level converter (IC55).
74	PDATC	Outputs the data signal to the 1st and 2nd PLL ICs (MAIN unit; IC400, pin 15, IC550, pin 5) via the level converter (IC55).
75	PSCKC	Outputs clock signal to the 1st and 2nd PLL ICs (MAIN unit; IC400, pin 14, IC550, pin 4) via the level converter (IC55).
76	P1STC	Outputs strobe signal to the 1st PLL IC (MAIN unit; IC400, pin 16) via the level converter (IC55).
77	+5AC	Outputs control signal to the 5A (Q1345) and D+5 (Q1347) regulators via the level converter (IC55). Low: While the +5 and D+5 regulators are activated.
78	W/NSC	Outputs control signal to the DV/FM filter switches (MAIN unit; D192, D193) via the level converter (IC55). High: While DV mode is selected.
79	ADSWC	Outputs control signal to the mode switches (MAIN unit; IC1411, IC1670, IC1673) via the level converter (IC55). Low: While DV mode is selected.
80	TXLED	Outputs TX LED control signal. High: During transmit.
82	RXLED	Outputs RX LED control signal. High: While receiving or squelch is opened.

Pin number	Port name	Description
85	PCON	Outputs control signal to the TX power controller (MAIN unit; Q1250).
86	ULCK	Input port for the PLL unlock signal. High: The PLL circuit is unlocked.
87	MMUT	Outputs the microphone mute signal to the mute switch (MAIN unit; Q1670). Low: While microphone audio is muted.
93	SCAN	Outputs scan control signal to the scan switch (Q400). High: While scanning.
94	TXS	Outputs the T+5, T+3 regulator circuits (MAIN unit; Q1336, Q1342) control signal. High: During transmit.
95	RXS	Outputs the R+5, R+3 regulator circuits (MAIN unit; Q1337, Q1343) control signal. High: During receive.
96	AMUT	Outputs the AF mute signal to the AF mute switch (MAIN unit; Q1550). Low: While digital code/call sign/noise/tone squelch are closed, the audio level is set to minimum position or transmitting.
102	RMUT	Outputs the SQL mute signal to the AF switch (MAIN unit; IC1463, pin 2). High: While noise or tone squelch is closed.
103	AFCSW	Outputs AFC switch (IC352, pin 5) control signal.
105	DACK2	Outputs clock signal to the D/A converter (IC57, pin 7).
106	DADAT2	Outputs the data signal to the D/A converter (IC57, pin 6).
107	DACK1	Outputs clock signal to the D/A converter (IC56, pin 7).
108	DADAT1	Outputs the data signal to the D/A converter (IC56, pin 6).
128	FSTB	Outputs strobe signal to the FPGA IC (IC200).
129	MSTRC	Outputs strobe signal to the liner CODEC IC (IC1) and FPGA IC (IC200).
130	MDATC	Outputs the data signal to the liner CODEC IC (IC1) and FPGA IC (IC200).
131	MCLKC	Outputs clock signal to the liner CODEC IC (IC1) and FPGA IC (IC200).
132	MRESC	Outputs reset signal to the liner CODEC IC (IC1) and FPGA IC (IC200).

SECTION 5 ADJUSTMENT PROCEDURES

5-1 PREPARATION

When adjusting ID-1, ADJUSTMENT SOFTWARE, JIG CABLE (see illustration on page 5-2) and OPC-1127 USB CABLE are required.

■ REQUIRED TEST EQUIPMENT

EQUIPMENT	GRADE AND RANGE	EQUIPMENT	GRADE AND RANGE
DC power supply	Output voltage : 13.8 V DC Current capacity : 10 A or more	Audio generator	Frequency range : 300–3000 Hz Measuring range : 1–500 mV
Modulation analyzer	Frequency range : DC–1500 MHz Measuring range : 0 to ±10 kHz	Attenuator	Power attenuation : 50 or 60 dB Capacity : 20 W
Frequency counter	Frequency range : 0.1–1500 MHz Frequency accuracy : ±1 ppm or better Sensitivity : 100 mV or better	Standard signal generator (SSG)	Frequency range : 0.1–1500 MHz Output level : 0.1 μV to 32 mV (–127 to –17 dBm)
Digital multimeter	Input impedance : 10 MΩ/V DC or more	AC millivoltmeter	Measuring range : 10 mV to 10 V
RF power meter	Measuring range : 1–20 W Frequency range : 1000–1500 MHz Impedance : 50 Ω SWR : Better than 1.2 : 1	Oscilloscope	Frequency rang : DC–20 MHz Measuring range : 0.01–20 V
		External speaker	Input impedance : 8 Ω Capacity : 10 W or more
Spectrum analyzer	Frequency range : At least 1500 MHz Spectrum bandwidth : 100 kHz or more	DC Ammeter	Measuring capacity : 3 A

■ SYSTEM REQUIREMENTS

- Microsoft® Windows® 98/98SE/Me/2000/XP
- USB port

■ ADJUSTMENT SOFTWARE INSTALLATION

- ① Quit all applications when Windows is running.
- ② Insert the CD into the appropriate CD drive.
- ③ Double-click the “Setup.exe” contained in the adjustment software folder in the CD drive.
- ④ The “Welcome to the InstallShield Wizard for adjustment software screen will appears.
Click [Next>].
- ⑤ The “Choose Destination Location” will appears.
Click [Next>] to install the software into the specified folder.
- ⑥ After the installation is completed, the “InstallShield Wizard Complete” will appears.
Click [Finish].
- ⑦ Eject the CD.
- ⑧ The adjustment software icon appears on the desktop screen.

■ STARTING SOFTWARE ADJUSTMENT

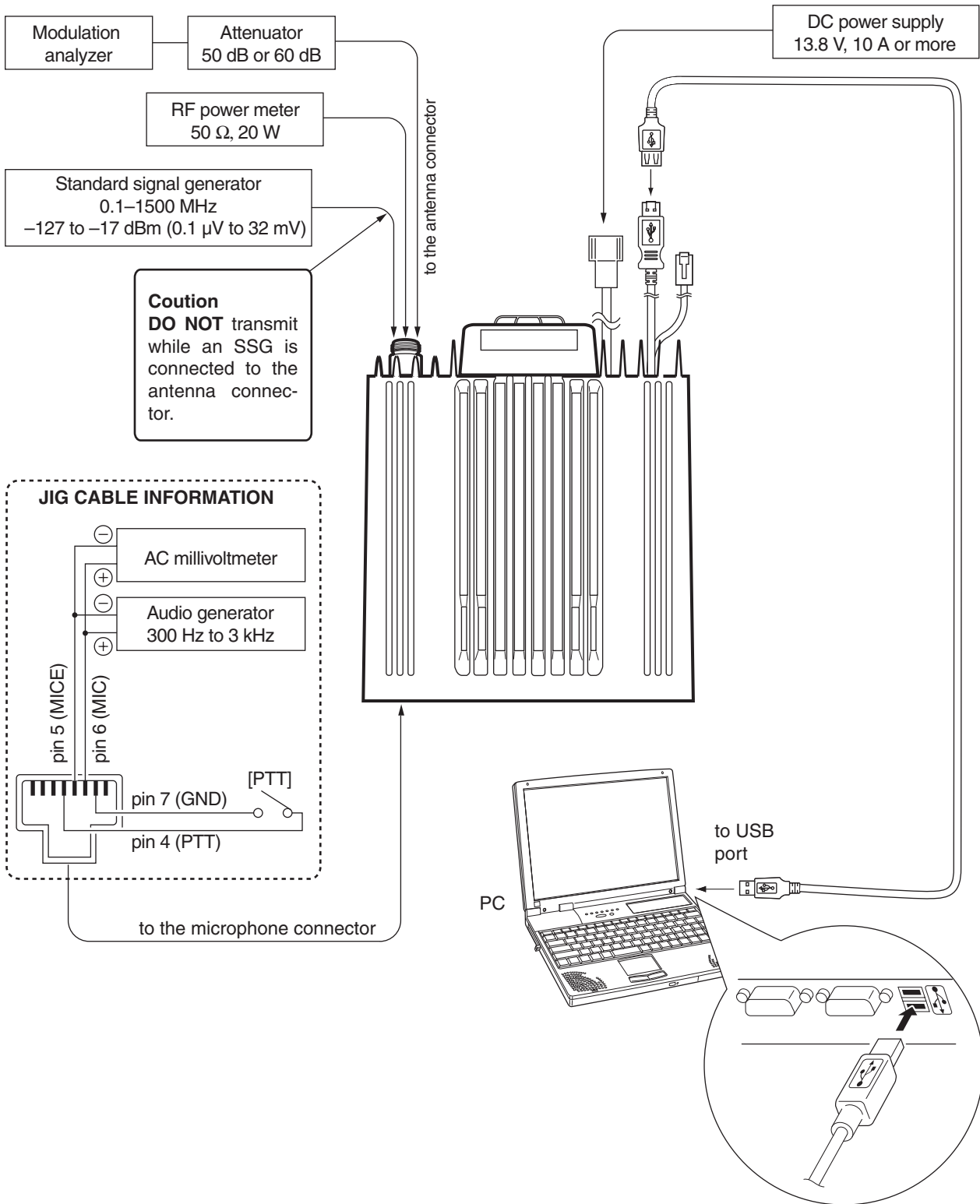
- ① Connect the transceiver and PC with the OPC-1127.
- ② Turn the transceiver power ON.
- ③ Boot up Windows, and double click the adjustment software icon on the desktop screen.
Then the control panel screen will appears.
- ④ Click [Adjustment (A)] in the menu bar and then click [Adjustment panel (F9)] in the pull down menu.
Then the adjustment screen will appears.
- ⑤ Set or modify adjustment data as desired.

■ OPERATING ON THE ADJUSTMENT MODE (CONNECTED COMPUTER KEYBOARD)

- Adjustment item selection* : [↑]/[↓]
- Specified value adjustment : [←]/[→]
- Mode selection : [M]
- PTT control : [T]
- RF power selection : [P]
- AF level control [UP] : [Q]
- AF level control [DOWN] : [W]
- Squelch level control [UP] : [A]
- Squelch level control [DOWN] : [S]
- Read the transceiver's data : [F5]
- All Default setting : [CTRL]+[D]

*When select the adjustment item, the adjustment frequency and operating mode are selected automatically.

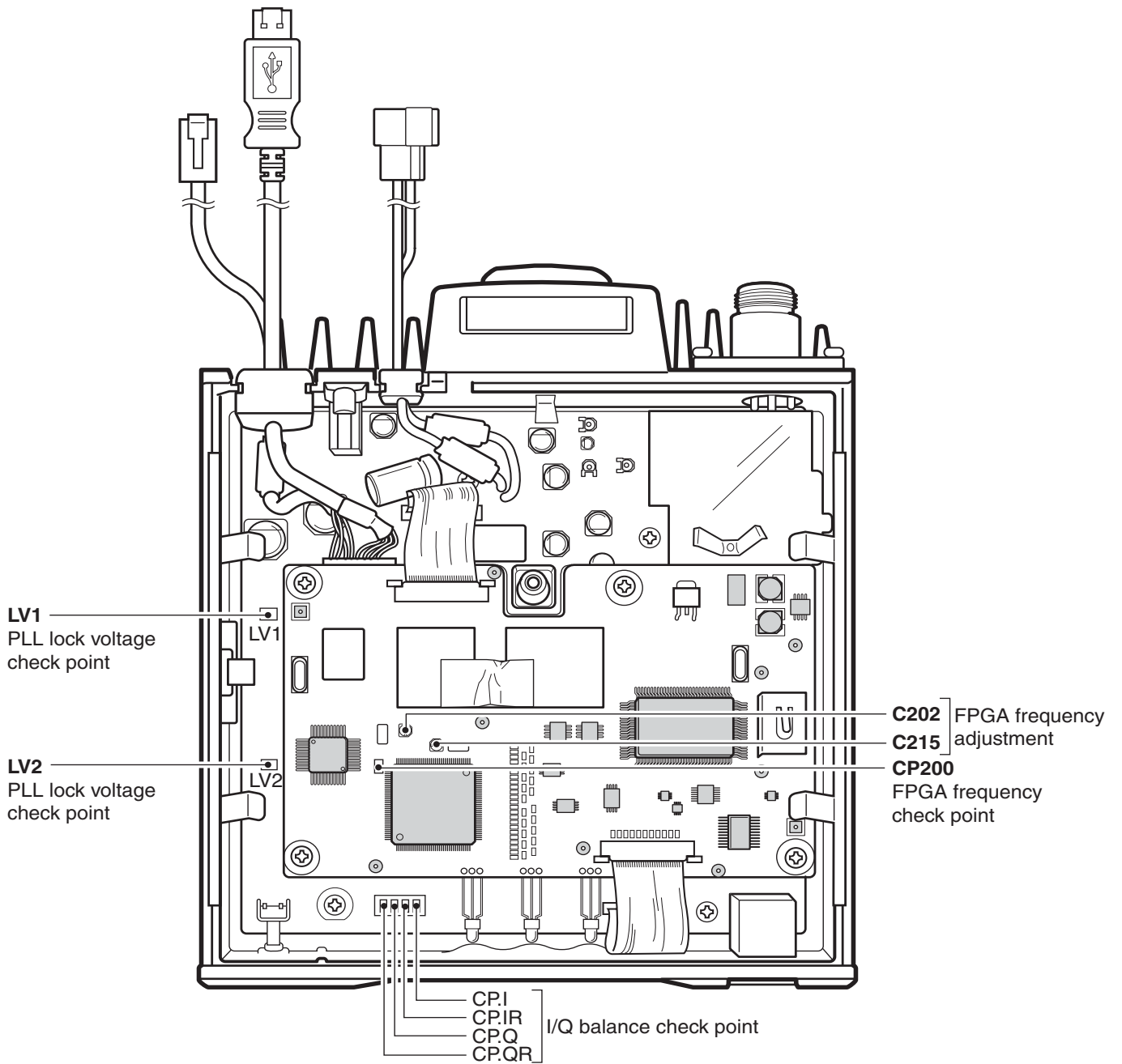
• CONNECTION



5-2 PLL AND CODEC ADJUSTMENT

ADJUSTMENT	ADJUSTMENT CONDITION	MEASUREMENT		VALUE	ADJUSTMENT			
		UNIT	LOCATION		UNIT	ADJUST		
FPGA FREQUENCY [Set FPGA frequency]	1	<ul style="list-style-type: none"> Operating freq. : 1240.00 MHz Mode : DD mode Receiving 	LOGIC-1 unit	Connect a frequency counter to the check point "CP200".	16.3840 MHz	LOGIC-1 unit	C202	
	2	<ul style="list-style-type: none"> Operating freq. : 1240.00 MHz Mode : DV mode Receiving 			9.8304 MHz			LOGIC-1 unit
PLL LOCK VOLTAGE	1	<ul style="list-style-type: none"> Operating freq. : 1240.00 MHz Mode : DV mode Connect an RF power meter or 50 Ω dummy load to the antenna connector. Receiving 	MAIN unit	Connect a digital multimeter or an oscilloscope to the check point "LV1".	More than 0.9 V	Verify		
	2	<ul style="list-style-type: none"> Operating freq. : 1300.00 MHz Receiving 			Less than 4.4 V			
	3	<ul style="list-style-type: none"> Mode : FM mode Receiving 	MAIN unit	Connect a digital multimeter or an oscilloscope to the check point "LV2".	3.1–4.0 V			
	4	<ul style="list-style-type: none"> Mode : DD mode Receiving 			2.6–3.3 V			
	5	<ul style="list-style-type: none"> Mode : FM mode Transmitting 			3.3–4.0 V			
I/Q BALANCE [FPGA D.C. voltage adjustment /DV I]	1	<ul style="list-style-type: none"> Preset "IQ Direct-current output" ON. Operating freq. : 1270.00 MHz Mode : DV mode Connect an RF power meter or 50 Ω dummy load to the antenna connector. Transmitting 	MAIN unit	Connect a digital multimeter or an oscilloscope to the check point "CP.I".	The same voltage of the check point "CP.IR".	PC screen	[FPGA D.C. voltage adjustment /DV I]	
[FPGA D.C. voltage adjustment /DV Q]	2	<ul style="list-style-type: none"> Transmitting 	MAIN unit	Connect a digital multimeter or an oscilloscope to the check point "CP.Q".	The same voltage of the check point "CP.QR".	PC screen	[FPGA D.C. voltage adjustment /DV Q]	
[FPGA D.C. voltage adjustment /DV I]	3	<ul style="list-style-type: none"> Transmitting 	Rear panel	Connect a spectrum analyzer to the antenna connector through an attenuator.	Minimum output level	PC screen	[FPGA D.C. voltage adjustment /DV I],	
[FPGA D.C. voltage adjustment /DV Q]	4	<ul style="list-style-type: none"> Repeat step 3 and step 4 several times. 						[FPGA D.C. voltage adjustment /DV Q]

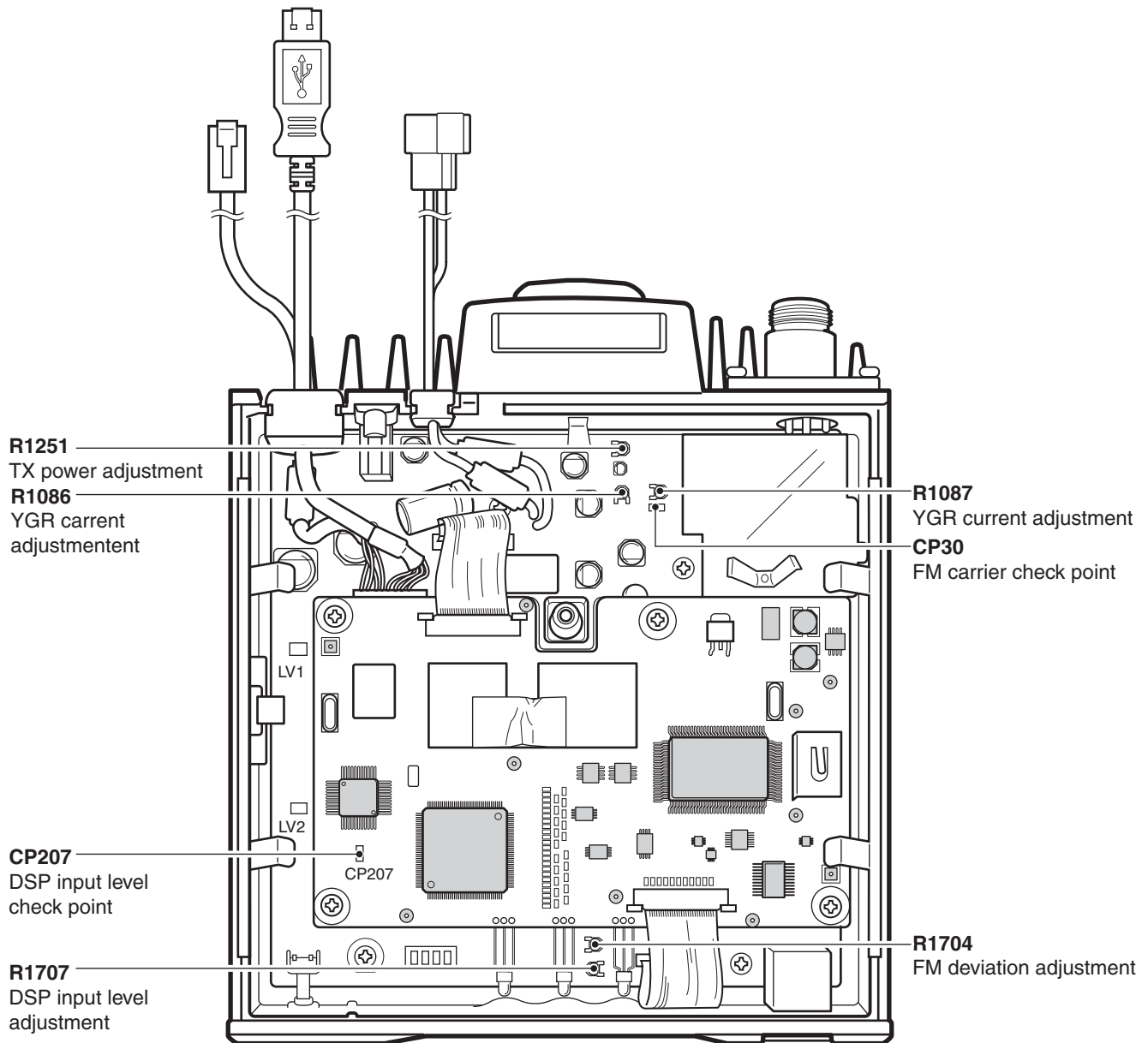
• MAIN AND LOGIC-1 UNITS



5-3 TRANSMITTER ADJUSTMENT

ADJUSTMENT	ADJUSTMENT CONDITION	MEASUREMENT		VALUE	ADJUSTMENT		
		UNIT	LOCATION		UNIT	ADJUST	
YGR CURRENT [FPGA D.C. voltage ad- justment /DV I]	1	<ul style="list-style-type: none"> • Preset R1086 and R1087 maximum counterclockwise. • Preset "IQ Direct-current output" ON. 	Rear panel	Connect an ammeter between the DC power supply and ID-1.	100 mA higher from the pre-set position.	MAIN unit	R1087
	2	<ul style="list-style-type: none"> • Operating freq. : 1300.00 MHz • Mode : DV mode • Connect an RF power meter or 50 Ω dummy load to the antenna connector. • Transmitting 			100 mA higher from step 1.	MAIN unit	R1086
REFERENCE FREQUENCY [REF Crystal adjustment]	1	<ul style="list-style-type: none"> • Operating freq. : 1300.00 MHz • Mode : FM mode • Connect an RF power meter or 50 Ω dummy load to the antenna connector. • Transmitting 	Rear panel	Loosely couple a frequency counter to the antenna connector.	1300.0000 MHz	PC screen	[REF Crystal adjustment]
FM CARRIER [FPGA D.C. voltage ad- justment /FM I]	1	<ul style="list-style-type: none"> • Operating freq. : 1300.00 MHz • Mode : FM mode • Connect an RF power meter or 50 Ω dummy load to the antenna connector. • Transmitting 	MAIN unit	Connect a digital multimeter or an oscilloscope to the check point "CP30".	The same voltage that during in DV mode (TX) at the check point "CP30".	PC screen	[FPGA D.C. voltage adjustment /FM I]
[FPGA D.C. voltage ad- justment /FM Q]	2	<ul style="list-style-type: none"> • Transmitting 			The same adjustment as step 1, if need.	PC screen	[FPGA D.C. voltage adjustment /FM Q]
OUTPUT POWER [TX output adjustment]	1	<ul style="list-style-type: none"> • Operating freq. : 1300.00 MHz • Mode : FM mode • TX power : High • Transmitting 	Rear panel	Connect an RF power meter to the antenna connector.	11 W	MAIN unit	R1251
FM DEVIATION [FM modulation adjustment]	1	<ul style="list-style-type: none"> • Operating freq. : 1270.00 MHz • Mode : FM mode • Connect an audio generator to the [MIC] connector and set as : 1.0 kHz/20 mVrms • Set a Modulation analyzer as: HPF : OFF LPF : 20 kHz De-emphasis : OFF Detector : (P-P)/2 • Transmitting 	Rear panel	Connect a modulation analyzer to the antenna connector through an attenuator.	±4.35 kHz	MAIN unit	R1704
DSP INPUT LEVEL [DSP input level adjustment]	1	<ul style="list-style-type: none"> • Operating freq. : 1270.00 MHz • Connect an audio generator to the [MIC] connector and set as : 1.0 kHz/20 mVrms • Connect an RF power meter or 50 Ω dummy load to the antenna connector. • Transmitting 	LOGIC-1 unit	Connect an oscilloscope to the check point "CP207".	750 mVp-p	MAIN unit	R1707

• MAIN AND LOGIC-1 UNITS



5-4 RECEIVER ADJUSTMENT

ADJUSTMENT ITEM	ADJUSTMENT CONDITION	OPERATION
SQUELCH LEVEL [SQL adjustment /FM thresh]	1 <ul style="list-style-type: none"> • Operating freq. : 1270.00 MHz • Mode : FM mode • Connect an SSG to the antenna connector and set as: <ul style="list-style-type: none"> Level : 0.11 μV^* (-126 dBm) Modulation : 1 kHz Deviation : 3.5 kHz • Receiving 	• Push [ENTER] on the connected computer keyboard to set to "SQL adjustment/FM thresh" level.
[SQL adjustment /FM tight]	2 <ul style="list-style-type: none"> • Set an SSG as: <ul style="list-style-type: none"> Level : 0.18 μV^* (-122 dBm) • Receiving 	• Push [ENTER] on the connected computer keyboard to set to "SQL adjustment/FM tight" level.
AFC CENTER [AFC center voltage adjustment/FM]	1 <ul style="list-style-type: none"> • Operating freq. : 1270.00 MHz • Mode : FM mode • Connect an SSG to the antenna connector and set as: <ul style="list-style-type: none"> Level : 1 mV* (-47 dBm) Modulation : OFF • Receiving 	• Push [ENTER] on the connected computer's keyboard to set to "AFC center voltage adjustment/FM" level.
[AFC center voltage adjustment /DV]	2 <ul style="list-style-type: none"> • Mode : DV mode • Receiving 	• Push [ENTER] on the connected computer keyboard to set to "AFC center voltage/DV" level.
S-METER (FM) [S-meter adjustment /FM min]	1 <ul style="list-style-type: none"> • Operating freq. : 1270.00 MHz • Mode : FM mode • Connect an SSG to the antenna connector and set as: <ul style="list-style-type: none"> Level : 0.18 μV^* (-122 dBm) Modulation : OFF • Receiving 	• Push [ENTER] on the connected computer keyboard to set to "S-meter adjustment/FM min" level.
[S-meter adjustment /FM full]	2 <ul style="list-style-type: none"> • Set an SSG as: <ul style="list-style-type: none"> Level : 5.6 μV^* (-92 dBm) • Receiving 	• Push [ENTER] on the connected computer keyboard to set to "S-meter adjustment/FM full" level.
S-METER (DV) [S-meter adjustment /DV min]	1 <ul style="list-style-type: none"> • Operating freq. : 1270.00 MHz • Mode : DV mode • Set an SSG as: <ul style="list-style-type: none"> Level : 0.18 μV^* (-122 dBm) Modulation : OFF • Receiving 	• Push [ENTER] on the connected computer keyboard to set to "S-meter adjustment/DV min" level.
[S-meter adjustment /DV full]	2 <ul style="list-style-type: none"> • Set an SSG as: <ul style="list-style-type: none"> Level : 5.6 μV^* (-92 dBm) • Receiving 	• Push [ENTER] on the connected computer keyboard to set to "S-meter adjustment/DV full" level.
S-METER (DD) [S-meter adjustment /DD min]	1 <ul style="list-style-type: none"> • Operating freq. : 1270.00 MHz • Mode : DD mode • Set an SSG as: <ul style="list-style-type: none"> Level : 1.6 μV^* (-103 dBm) Modulation : OFF • Receiving 	• Push [ENTER] on the connected computer keyboard to set to "S-meter adjustment/DD min" level.
[S-meter adjustment /DD full]	2 <ul style="list-style-type: none"> • Set an SSG as: <ul style="list-style-type: none"> Level : 5.6 μV^* (-92 dBm) • Receiving 	• Push [ENTER] on the connected computer keyboard to set to "S-meter adjustment/DD full" level.

*The output level of the standard signal generator (SSG) is indicated as the SSG's open circuit.

[LOGIC-1 UNIT]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
C443	4030011810	S.CER C1608 JB 1A 224K-T	B	71.3/18.6
C500	4510004640	S.ELE ECEV1CA470SP	B	84.4/63.5
C501	4030011600	S.CER C1608 JB 1E 104K-T	T	84.1/66.4
C502	4030011600	S.CER C1608 JB 1E 104K-T	T	86.5/67
C503	4510004640	S.ELE ECEV1CA470SP	B	96.2/63.9
C504	4030006850	S.CER C1608 JB 1H 471K-T	T	86.5/65.7
C506	4030011600	S.CER C1608 JB 1E 104K-T	T	58.6/7.5
C509	4550006250	S.TAN TEESVA 1A 106M8L	T	85.3/64
C510	4030011600	S.CER C1608 JB 1E 104K-T	T	97.4/17.8
C511	4030011600	S.CER C1608 JB 1E 104K-T	T	90.5/64.2
C512	4550006250	S.TAN TEESVA 1A 106M8L	T	88.8/64.4
C513	4510007130	S.ELE EEFCD 0J 470R	T	98.6/73.1
C514	4030006850	S.CER C1608 JB 1H 471K-T	T	109.3/75.9
C515	4510005820	S.ELE ECEV1CA101P	B	109.5/63.3
C516	4510005600	S.ELE ECEV1CS100SR	B	64.2/76
C517	4030011600	S.CER C1608 JB 1E 104K-T	T	66.9/75.3
C518	4030011600	S.CER C1608 JB 1E 104K-T	T	64.5/72.5
C519	4550006250	S.TAN TEESVA 1A 106M8L	T	65.2/69.9
C520	4550006200	S.TAN ECST0JY106R	T	71.7/75.7
C521	4550006200	S.TAN ECST0JY106R	B	69.4/64.9
C522	4550006620	S.TAN ECST0JY226R	T	96.6/65.7
C550	4030008560	S.CER C1608 CH 1H 300J-T	T	4.2/63
C551	4030008560	S.CER C1608 CH 1H 300J-T	T	4.2/48
C552	4030011600	S.CER C1608 JB 1E 104K-T	B	14.3/57.6
C553	4030011600	S.CER C1608 JB 1E 104K-T	B	15.4/53.9
C554	4030011600	S.CER C1608 JB 1E 104K-T	T	18.1/56.2
C555	4030008880	S.CER C1608 JB 1H 223K-T	T	24/61
C556	4030007070	S.CER C1608 CH 1H 330J-T	B	18.7/64.1
C557	4550006200	S.TAN ECST0JY106R	T	13/68.2
C558	4030006900	S.CER C1608 JB 1H 103K-T	T	10.1/70.3
C559	4030007090	S.CER C1608 CH 1H 470J-T	T	84/55.1
C560	4030007090	S.CER C1608 CH 1H 470J-T	B	79.5/41.3
C561	4030007090	S.CER C1608 CH 1H 470J-T	T	85.7/51.4
C562	4030007090	S.CER C1608 CH 1H 470J-T	T	88.3/52.4
C563	4030007090	S.CER C1608 CH 1H 470J-T	T	103/42
C564	4030007090	S.CER C1608 CH 1H 470J-T	T	99.3/30
C565	4030007090	S.CER C1608 CH 1H 470J-T	B	96.2/34.6
C566	4030007090	S.CER C1608 CH 1H 470J-T	T	90.6/27.8
C567	4030007090	S.CER C1608 CH 1H 470J-T	T	85.4/27.8
C568	4030007090	S.CER C1608 CH 1H 470J-T	T	85.4/26.5
C569	4030007090	S.CER C1608 CH 1H 470J-T	T	78.8/28.4
C570	4030007090	S.CER C1608 CH 1H 470J-T	T	81.7/27.8
C571	4030007090	S.CER C1608 CH 1H 470J-T	B	93.2/44.5
C572	4030007090	S.CER C1608 CH 1H 470J-T	B	90.3/47.7
C573	4030007090	S.CER C1608 CH 1H 470J-T	B	89/47.7
C574	4030007090	S.CER C1608 CH 1H 470J-T	T	78.5/55.9
C575	4030007090	S.CER C1608 CH 1H 470J-T	T	78.5/53.1
C576	4030007090	S.CER C1608 CH 1H 470J-T	T	91.2/53.1
C577	4030007090	S.CER C1608 CH 1H 470J-T	T	91.2/55.9
C578	4030007090	S.CER C1608 CH 1H 470J-T	B	12.3/49
C579	4030007090	S.CER C1608 CH 1H 470J-T	B	10.7/47
J50	6510019270	S.CNR 52365-0691	T	5.1/43.9
J100	6510021290	S.CNR S10B-ZR-SM3A-TF	B	18.7/77.2
J101	6510022820	S.CNR AXN430C530P	B	17.2/8.8
J300	6510018350	S.CNR S3B-ZR-SM3A-TF	T	13.9/12.4
J400	6510022710	S.CNR 30FLZ-SM1-TB	T	78/7.7
J401	6510022710	S.CNR 30FLZ-SM1-TB	T	35/74.4
DS100	5040002050	LED SPR-39MVWF		
DS101	5040002050	LED SPR-39MVWF		
DS102	5040002050	LED SPR-39MVWF		
T100	5920000800	TSM 20F001N <YCL>		
W1	7030003860	S.RES ERJ3GE JPW V	T	11.9/20.1
W2	7030003860	S.RES ERJ3GE JPW V	B	12.3/31.9
W50	7030003860	S.RES ERJ3GE JPW V	T	51.8/67
W51	7030003860	S.RES ERJ3GE JPW V	B	47/59.2
W52	7030003860	S.RES ERJ3GE JPW V	B	59.2/64.3
W125	7030003860	S.RES ERJ3GE JPW V	T	17.7/73.8
W126	7030003860	S.RES ERJ3GE JPW V	T	10.4/76.8
W129	7030003860	S.RES ERJ3GE JPW V	T	23.3/73.8
W200	7030003860	S.RES ERJ3GE JPW V	B	58.3/16
W213	7030003860	S.RES ERJ3GE JPW V	B	43.7/29.1
W300	7030003860	S.RES ERJ3GE JPW V	T	55.5/5.8
W310	7030003860	S.RES ERJ3GE JPW V	T	71.6/21.4
W400	7030003860	S.RES ERJ3GE JPW V	B	77.3/12.3
W401	7030003860	S.RES ERJ3GE JPW V	B	77.7/17.3
W402	7030003860	S.RES ERJ3GE JPW V	B	7.7/34.4
W403	7030003860	S.RES ERJ3GE JPW V	B	36/71.1

[LOGIC-1 UNIT]

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
IC1160	1150002190	IC RA18H1213G1-21		
J1	6510004910	CNR NR-DS-E 01		
MF1	2710000590	FAN MF40D-12H-001		
W1	8900010890	CBL OPC-1115		
W2	8900010890	CBL OPC-1115		
W3	8900011950	CBL OPC-1224		
EP1	6910000630	BEA FSRH070140RN000B		
EP20	6910011940	BEA ZCAT2436-1330A-BK-M [EUR2], [EUR3] only		
EP1160	6910000970	BEA DL-2OP 2.6-3-1.2H		
EP1162	6910000970	BEA DL-2OP 2.6-3-1.2H		

[RC-24] (Optional for some version)

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
IC1	1130009120	S.IC SED1526FOA	B	69.5/29.5
IC2	1140007890	S.IC HD64F3644H	B	111.8/20.4
IC3	1110005940	S.IC S-80842CLMCC-B63-T2	B	127.5/23.9
IC4	1130005720	S.IC TC7W04F (TE12L)	B	121/8.2
IC5	1110003390	S.IC AN8005M-(E1)	B	67.9/11.6
IC6	1110002860	S.IC TA75S393F (TE85R)	B	85.6/7.9
Q1	1530002060	S.TR 2SC4081 T106 R	B	133.6/18.1
Q2	1590000720	S.TR DTA144EUA T106	B	120.4/4
Q3	1590000680	S.TR DTC114EUA T106	B	123/2.7
Q6	1590000440	S.TR DTA143ZUA T106	B	90.4/14.6
Q7	1590000440	S.TR DTA143ZUA T106	B	86.9/20.8
Q8	1590000440	S.TR DTA143ZUA T106	B	90.4/17.1
Q9	1590000440	S.TR DTA143ZUA T106	B	90.7/19.7
Q10	1590000680	S.TR DTC114EUA T106	B	93.3/17
Q11	1590000680	S.TR DTC114EUA T106	B	93.3/19.5
Q12	1590000680	S.TR DTC114EUA T106	B	90.4/12.1
Q13	1530002060	S.TR 2SC4081 T106 R	B	34/7.1
D1	1790001280	S.DIO MA111 (TX)	B	134.1/21.7
D3	1790001280	S.DIO MA111 (TX)	B	116.2/2.4
D9	1750000130	S.DIO DA204U T106	B	132.6/10.1
D10	1790001280	S.DIO MA111 (TX)	B	126.3/3.8
D11	1790000660	S.DIO MA728 (TX)	B	126.2/2
D12	1790001280	S.DIO MA111 (TX)	B	129.8/2
D13	1790001280	S.DIO MA111 (TX)	B	114.2/8.4
X1	6050011310	S.XTL CR-717 (9.8304 MHz)	B	97.4/24.4
L1	6200001720	S.COL NL 322522T-1R0J	B	16.2/12.3
R1	7030003810	S.RES ERJ3GEYJ 125 V (1.2 MΩ)	B	90.8/40.5
R2	7310002820	S.TRI RV-158 (RH03A3AS5) 474	B	93.7/39.4
R3	7030003800	S.RES ERJ3GEYJ 105 V (1 MΩ)	B	90/38.6
R4	7030003440	S.RES ERJ3GEYJ 102 V (1 kΩ)	B	129.3/21.5
R5	7030003680	S.RES ERJ3GEYJ 104 V (100 kΩ)	B	130.5/24.7
R6	7030003760	S.RES ERJ3GEYJ 474 V (470 kΩ)	B	134/23.5
R7	7030003560	S.RES ERJ3GEYJ 103 V (10 kΩ)	B	131.7/18.1
R8	7030003720	S.RES ERJ3GEYJ 224 V (220 kΩ)	B	131.8/20.8
R9	7030003720	S.RES ERJ3GEYJ 224 V (220 kΩ)	B	133.7/20.1
R10	7030003680	S.RES ERJ3GEYJ 104 V (100 kΩ)	B	102/15.9
R11	7030003800	S.RES ERJ3GEYJ 105 V (1 MΩ)	B	100.8/22.2
R12	7030003680	S.RES ERJ3GEYJ 104 V (100 kΩ)	B	102.3/27.5
R13	7030003680	S.RES ERJ3GEYJ 104 V (100 kΩ)	B	109.8/10.5
R16	7030003680	S.RES ERJ3GEYJ 104 V (100 kΩ)	B	118.4/3.9
R17	7030003680	S.RES ERJ3GEYJ 104 V (100 kΩ)	B	123.2/4.7
R18	7030003680	S.RES ERJ3GEYJ 104 V (100 kΩ)	B	120.3/13
R19	7030003680	S.RES ERJ3GEYJ 104 V (100 kΩ)	B	120.3/11.7
R27	7030003340	S.RES ERJ3GEYJ 151 V (150 Ω)	B	84.5/23.2
R28	7030003340	S.RES ERJ3GEYJ 151 V (150 Ω)	B	87.3/23.2
R29	7030003370	S.RES ERJ3GEYJ 271 V (270 Ω)	B	85/20.9
R30	7030003440	S.RES ERJ3GEYJ 102 V (1 kΩ)	B	93.3/21.7
R31	7030003440	S.RES ERJ3GEYJ 102 V (1 kΩ)	B	93.3/23
R32	7030003390	S.RES ERJ3GEYJ 391 V (390 Ω)	B	90.6/23
R34	7030003360	S.RES ERJ3GEYJ 221 V (220 Ω)	B	88.8/19.9
R35	7030003680	S.RES ERJ3GEYJ 104 V (100 kΩ)	B	124.2/27.1
R36	7030003680	S.RES ERJ3GEYJ 104 V (100 kΩ)	B	124.2/23.2
R37	7030003680	S.RES ERJ3GEYJ 104 V (100 kΩ)	B	124.2/24.5

[RC-24] (Optional for some version)

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
R38	7030003680	S.RES ERJ3GEYJ 104 V (100 kΩ)	B	124.2/25.8
R39	7030003680	S.RES ERJ3GEYJ 104 V (100 kΩ)	B	124.2/12.8
R40	7030003680	S.RES ERJ3GEYJ 104 V (100 kΩ)	B	124.2/14.1
R41	7030003680	S.RES ERJ3GEYJ 104 V (100 kΩ)	B	124.2/15.4
R42	7030003680	S.RES ERJ3GEYJ 104 V (100 kΩ)	B	124.2/16.7
R43	7030003680	S.RES ERJ3GEYJ 104 V (100 kΩ)	B	124.2/19.3
R44	7030003680	S.RES ERJ3GEYJ 104 V (100 kΩ)	B	124.2/21.9
R45	7030003680	S.RES ERJ3GEYJ 104 V (100 kΩ)	B	124.2/20.6
R48	7030003440	S.RES ERJ3GEYJ 102 V (1 kΩ)	B	134.6/10.1
R49	7030003600	S.RES ERJ3GEYJ 223 V (22 kΩ)	B	114.3/5.3
R51	7030003640	S.RES ERJ3GEYJ 473 V (47 kΩ)	B	109.8/9.3
R52	7030003640	S.RES ERJ3GEYJ 473 V (47 kΩ)	B	11.2/36.2
R53	7030003640	S.RES ERJ3GEYJ 473 V (47 kΩ)	B	7.8/36.2
R54	7030003480	S.RES ERJ3GEYJ 222 V (2.2 kΩ)	B	129.4/3.8
R55	7030003440	S.RES ERJ3GEYJ 102 V (1 kΩ)	B	131.6/4.6
R56	7030003620	S.RES ERJ3GEYJ 333 V (33 kΩ)	B	88/7.9
R57	7030003470	S.RES ERJ3GEYJ 182 V (1.8 kΩ)	B	81.9/7.3
R58	7030003680	S.RES ERJ3GEYJ 104 V (100 kΩ)	B	83.2/7.9
R59	7030003500	S.RES ERJ3GEYJ 332 V (3.3 kΩ)	B	90.8/8.5
R60	7030003400	S.RES ERJ3GEYJ 471 V (470 Ω)	B	37.3/16.7
R61	7030003620	S.RES ERJ3GEYJ 333 V (33 kΩ)	B	32.1/7.6
R62	7030003620	S.RES ERJ3GEYJ 333 V (33 kΩ)	B	30.8/7.6
R63	7030003390	S.RES ERJ3GEYJ 391 V (390 Ω)	B	36.1/7.6
R64	7030005420	S.RES ERJ3GEYJ 202 V (2 kΩ)	B	21.6/9.5
R65	7030003500	S.RES ERJ3GEYJ 332 V (3.3 kΩ)	B	36.8/9.9
C1	4030011600	S.CER C1608 JB 1E 104K-T	B	79.2/40.5
C2	4030011600	S.CER C1608 JB 1E 104K-T	B	80.5/40.5
C3	4030011600	S.CER C1608 JB 1E 104K-T	B	81.8/40.5
C4	4030011600	S.CER C1608 JB 1E 104K-T	B	83.1/40.5
C5	4030011600	S.CER C1608 JB 1E 104K-T	B	84.4/40.5
C6	4030012600	S.CER C2012 JB 1A 105M-T	B	86.1/30.9
C7	4030012600	S.CER C2012 JB 1A 105M-T	B	82.4/31.2
C8	4030008630	S.CER C1608 JF 1H 104Z-T	B	77.4/40.5
C9	4030008660	S.CER C1608 JB 1H 102K-T	B	81.4/28.8
C10	4030009000	S.CER C2012 JB 1C 224K-T	B	130.9/23.1
C11	4030006900	S.CER C1608 JB 1H 103K-T	B	100.1/15.1
C12	4550003220	S.TAN TEESVA 1E 105M8L	B	97.4/14.8
C13	4030007030	S.CER C1608 CH 1H 150J-T	B	100.8/25.6
C14	4030007030	S.CER C1608 CH 1H 150J-T	B	100.8/19.5
C15	4030006860	S.CER C1608 JB 1H 102K-T	B	107.8/9.7
C16	4030006900	S.CER C1608 JB 1H 103K-T	B	109.8/8.1
C17	4030008630	S.CER C1608 JF 1H 104Z-T	B	119.7/28.3
C18	4030008630	S.CER C1608 JF 1H 104Z-T	B	74.5/11.5
C19	4030006850	S.CER C1608 JB 1H 471K-T	B	73.2/11.5
C20	4550006250	S.TAN TEESVA 1A 106M8L	B	71.5/12.3
C21	4550003220	S.TAN TEESVA 1E 105M8L	B	64.4/12.1
C22	4030008630	S.CER C1608 JF 1H 104Z-T	B	62.7/11.3
C23	4030006850	S.CER C1608 JB 1H 471K-T	B	61.4/11.3
C24	4030006850	S.CER C1608 JB 1H 471K-T	B	60.1/11.3
C25	4030006850	S.CER C1608 JB 1H 471K-T	B	51.9/7.6
C26	4030008630	S.CER C1608 JF 1H 104Z-T	B	117.1/5.4
C27	4030006860	S.CER C1608 JB 1H 102K-T	B	5.2/9.8
C28	4030007090	S.CER C1608 CH 1H 470J-T	B	6.5/9.8
C30	4030006860	S.CER C1608 JB 1H 102K-T	B	9.1/9.8
C32	4030007090	S.CER C1608 CH 1H 470J-T	B	92.1/4.3
C34	4030007090	S.CER C1608 CH 1H 470J-T	B	28.8/3.2
C35	4030007090	S.CER C1608 CH 1H 470J-T	B	41.9/4.2
C36	4030007090	S.CER C1608 CH 1H 470J-T	B	54.9/4.2
C37	4030007090	S.CER C1608 CH 1H 470J-T	B	67.9/4.2
C38	4030007090	S.CER C1608 CH 1H 470J-T	B	77.3/4.2
C39	4030007090	S.CER C1608 CH 1H 470J-T	B	94.1/30.2
C40	4030007090	S.CER C1608 CH 1H 470J-T	B	99.5/16.8
C41	4030007090	S.CER C1608 CH 1H 470J-T	B	110/35.9
C42	4030007090	S.CER C1608 CH 1H 470J-T	B	114.3/31.2
C43	4030007090	S.CER C1608 CH 1H 470J-T	B	116.9/31.2
C44	4030007090	S.CER C1608 CH 1H 470J-T	B	109.5/5.4
C45	4030007090	S.CER C1608 CH 1H 470J-T	B	118/36.9
C46	4030007090	S.CER C1608 CH 1H 470J-T	B	115.6/31.2
C47	4030007090	S.CER C1608 CH 1H 470J-T	B	118.2/31.2
C48	4030007090	S.CER C1608 CH 1H 470J-T	B	115.7/6.2
C49	4030007090	S.CER C1608 CH 1H 470J-T	B	128.6/36.9
C50	4030007090	S.CER C1608 CH 1H 470J-T	B	126.9/28.1
C51	4030007090	S.CER C1608 CH 1H 470J-T	B	127.2/17.6
C52	4030007090	S.CER C1608 CH 1H 470J-T	B	128.7/5.4
C53	4510004440	S.ELE ECEV1HA010SR	B	26.8/7
C54	4510004440	S.ELE ECEV1HA010SR	B	41.9/8.8
C55	4510005300	S.ELE ECEV1AA330SR	B	41.2/14.2
C56	4510005300	S.ELE ECEV1AA330SR	B	32/12.7
C57	4030006860	S.CER C1608 JB 1H 102K-T	B	21.6/7.8
C59	4030007090	S.CER C1608 CH 1H 470J-T	B	53.9/10.3
C60	4030007090	S.CER C1608 CH 1H 470J-T	B	72.1/7.8
C61	4030011600	S.CER C1608 JB 1E 104K-T	B	80.6/9.1
C62	4030007130	S.CER C1608 CH 1H 101J-T	B	85.6/5.6
C63	4030006900	S.CER C1608 JB 1H 103K-T	B	34.1/9.1
C64	4030006900	S.CER C1608 JB 1H 103K-T	B	38.4/7.4
J1	6450001470	CNR 95003-2881	T	9.7/6.1
J2	6510019420	S.CNR B8B-ZR-SM3-TF	B	53.4/16.7
J3	6510019270	S.CNR 52365-0691	B	94.5/10.5

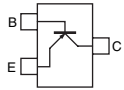
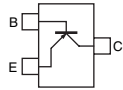
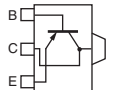
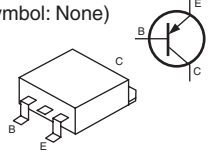
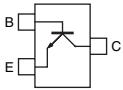
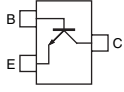
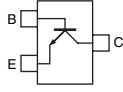
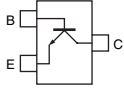
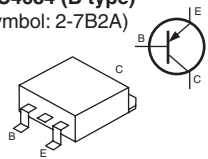
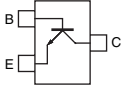
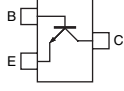
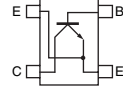
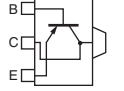
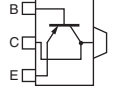
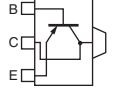
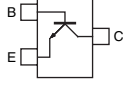
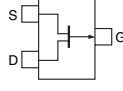
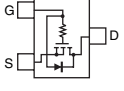
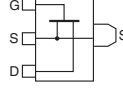
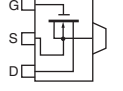
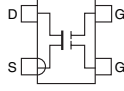
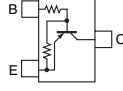
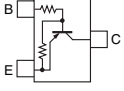
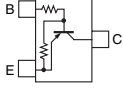
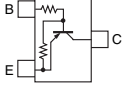
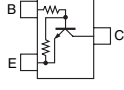
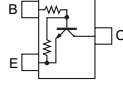
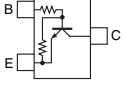
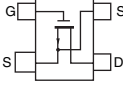
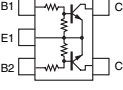
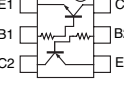
[RC-24] (Optional for some versions)

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
DS2	5040002470	S.LED FY1112H	T	31/26.4
DS3	5040002470	S.LED FY1112H	T	42.5/26.4
DS4	5040002470	S.LED FY1112H	T	54/26.4
DS5	5040002470	S.LED FY1112H	T	65.5/26.4
DS6	5040002470	S.LED FY1112H	T	77/26.4
DS7	5040002030	S.LED CL-170Y-CD-T	T	94/26.4
DS8	5040002030	S.LED CL-170Y-CD-T	T	124.7/31.6
DS10	5040002030	S.LED CL-170Y-CD-T	T	124.7/10.6
DS11	5040002030	S.LED CL-170Y-CD-T	T	113.7/31.6
DS13	5040002030	S.LED CL-170Y-CD-T	T	113.7/10.6
DS14	5040002030	S.LED CL-170Y-CD-T	T	34.5/4.2
DS15	5040002030	S.LED CL-170Y-CD-T	T	60.5/4.2
DS16	5040002030	S.LED CL-170Y-CD-T	T	86.5/4.2
S21	2250000270	ECR RH90N74E20-16F-1738	T	9.5/32.2
W3	7030000010	S.RES MCR10EZHZ JPW (000)	T	124.7/21.1
W4	7030000010	S.RES MCR10EZHZ JPW (000)	T	113.7/21.1
EP20	6910014690	S.BEA MPZ1608S221A-T	B	49.6/11
EP21	6910014690	S.BEA MPZ1608S221A-T	B	51.1/11
EP22	6910014690	S.BEA MPZ1608S221A-T	B	53.4/11.6
EP23	6910014690	S.BEA MPZ1608S221A-T	B	29.9/20
EP24	6910014690	S.BEA MPZ1608S221A-T	B	26.5/20.8
EP25	6910014690	S.BEA MPZ1608S221A-T	B	58.6/11.1
EP26	6910014690	S.BEA MPZ1608S221A-T	B	48.2/11
EP27	6910014690	S.BEA MPZ1608S221A-T	B	55.7/11


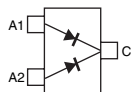
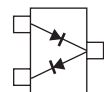


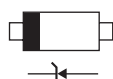

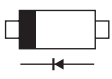
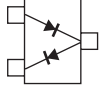
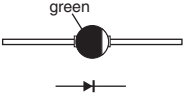
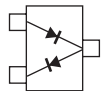
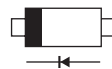



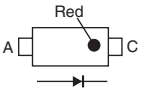




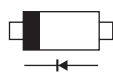
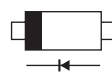
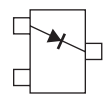
M.=Mounted side (T: Mounted on the Top side, B: Mounted on the Bottom side)
S.=Surface mount

SECTION 7 SEMI-CONDUCTOR INFORMATION

• TRANSISTORS AND FET's

2SA1362 GR (Symbol: AEG) 	2SA1586 GR (Symbol: SG) 	2SB798 DK (Symbol: DK) 	2SB934 P (Symbol: None) 	2SC4081 R (Symbol: BR) 
2SC4081 S (Symbol: BS) 	2SC4215 O (Symbol: QO) 	2SC4226 R25 (Symbol: R25) 	2SC4684 (B type) (Symbol: 2-7B2A) 	2SC5107 O (Symbol: MFO) 
2SC5195 (Symbol: 88) 	2SC5454 R54 (Symbol: R54) 	2SD999 CK (Symbol: CK) 	2SD1619 T (Symbol: DB) 	2SD1801 S (Symbol: CE) 
2SD2216J S (Symbol: Y) 	2SJ144 GR (Symbol: VG) 	2SK2036 (Symbol: KJ) 	2SK2854 (Symbol: UP) 	2SK2855 (Symbol: UT) 
3SK241 R (Symbol: DU) 	DTA114 EU (Symbol: 16) 	DTA143 TUA (Symbol: 113) 	DTA143 ZU (Symbol: 113) 	DTA144 EU (Symbol: 16) 
DTC114 EU (Symbol: 14) 	DTC143 ZU (Symbol: 123) 	DTC144 EU (Symbol: 26) 	NE34018 (Symbol: V63) 	XP1214 (Symbol: 9H) 
XP4315 (Symbol: CB) 				

• DIODES

<p>1SS355 (Symbol: A)</p> 	<p>1SS364 (Symbol: BF)</p> 	<p>1SS372 (Symbol: N9)</p> 	<p>1SV239 (Symbol: TC)</p> 	<p>1SV245 (Symbol: T3)</p> 
<p>1SV282 (Symbol: TD)</p> 	<p>1SV307 (Symbol: TX)</p> 	<p>1SV308 (Symbol: TX)</p> 	<p>DA204 U (Symbol: K)</p> 	<p>DSA3A1 (Symbol: Green)</p> 
<p>HSM88AS (Symbol: C1)</p> 	<p>HSU88TRF (Symbol: 9)</p> 	<p>MA2S077 (Symbol: S)</p> 	<p>MA2S728 (Symbol: B)</p> 	<p>MA111 (Symbol: 1B)</p> 
<p>MA4PH224 (Symbol: Red)</p> 	<p>MA728 (Symbol: 2A)</p> 	<p>MA8030 H (Symbol: 3^0)</p> 	<p>MA8033 L (Symbol: 3_3)</p> 	<p>MA8062 M (Symbol: 6-2)</p> 
<p>MA8082 M (Symbol: 8-2)</p> 	<p>MA8091 M (Symbol: 9-1)</p> 	<p>SB07-03C (Symbol: J)</p> 		

SECTION 8 MECHANICAL PARTS AND DISASSEMBLY

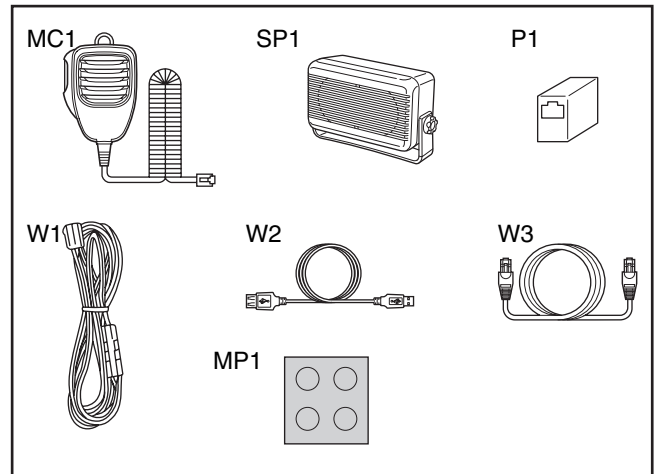
8-1 ID-1

[CHASSIS PARTS]

REF.NO.	ODER NO.	DESCRIPTION	QTY.
EP1160	6910000970	DL-20P 2.6-3-1.2H	1
EP1162	6910000970	DL-20P 2.6-3-1.2H	1
IC1160	1150002190	RA18H1213G1-21	1
J1	6510004910	NR-DS-E 01	1
MF1	2710000590	MF40D-12H-001	1
MP1	8010018711	2506 Chassis-1	1
MP2	8810008660	Screw PH BT M3x8 NI-ZU	2
MP3	8810008660	Screw PH BT M3x8 NI-ZU	2
MP4	8810008660	Screw PH BT M3x8 NI-ZU	7
MP5	8110006640	2047 Cover	1
MP6	8810008450	Screw M4x8 ZK	1
MP9	8110005751	1729 Fan Cover-1	1
MP10	8810009110	Screw M2.6x16 ZK	4
MP13	8930035230	1546 TR-A Clip	1
MP14	8510012210	2047 Main Shield Y445	2
MP15	8930043710	1562 EMER Button (A)	1
MP17	8810007130	Screw H M3x6	4
MP19	8930048350	2146 Lens	3
MP21	8930039612	Thermally Sheet (C)-2 TC100HS (10X10)	1
MP22	8930049650	Thermally Sheet (H)	2
MP23	8930053472	Thermally Sheet (R)-2 TC200HS (10X10)	3
MP24	8930055051	Thermally Sheet (V)-1 TC400HS (10X15)	1
MP26	8510014251	2506 M-Plate-1	1
MP27	8930037120	1647 M-Holder	1
MP28	8930056781	2506 YGR Plate-1 Y938A	1
MP29	8510014241	2506 ANT Plate-1	1
MP36	8310053110	2506 NAME PLATE	1
W1	8900010890	OPC-1115	1
W2	8900010890	OPC-1115	1
W3	8900011950	OPC-1224	1

[ACCESSORIES]

REF.	ORDER. NO.	DESCRIPTION	QTY.
MC1	Optional product	Microphone HM-118N	1
SP1	Optional product	Speaker SP-22	1
P1	5610000270	Connector ALA651B	1
W1	Optional product	Cable OPC-345	1
W2	8900010930	Cable OPC-1127	1
W3	8900010550	Cable OPC-1069	1
MP1	8930055180	Self-adhesive rubber feet	1



[MAIN UNIT]

REF.NO.	ODER NO.	DESCRIPTION	QTY.
MP30	8930014140	Earth Spring (D)	1
MP39	8930054521	Shield Sponge (E)-1	1
MP64	8930056580	Spacer (AD)	4
MP65	8810007130	Screw H M3x6	4
MP70	8930001170	Earth Spring (A) FX294	1
W1330	8900011960	OPC-1216	1

[LOGIC-1 UNIT]

REF.NO.	ORDER. NO.	DESCRIPTION	QTY.
MP6	8930001170	Earth Spring (A)	1

Screw abbreviations BT: Self-tapping
 NI-ZU: Nickel-zinc
 ZK : Black

8-2 RC-24

[CHASSIS PARTS]

REF.NO.	ODER NO.	DESCRIPTION	QTY.
DS1	5030002180	TSC0712-UFTDHW	1
EP2	8930048320	SRCN-2140-SP-N-W	2
MP1	8210015740	2140 Front Panel	1
MP2	8930047980	2140 LCD Holder	1
MP3	8930048290	2140 LCD Filter	1
MP4	8210015770	2140 Reflector	1
MP7	8610009840	Knob N234	1
MP9	8810008760	Screw PH BT M2x8 NI-ZU	5
MP10	8930038230	1765 Rear Seal	1
MP12	8810009060	Screw M3x6 ZK	4
MP13	8210013160	1765 Front Panel	1
MP16	8820000871	1705 Cap Screw-1	3
MP18	8310053110	2506 NAME PLATE	1
MP19	8930059370	2140 Front Key (C)	1
W1	8900010940	OPC-1119	1

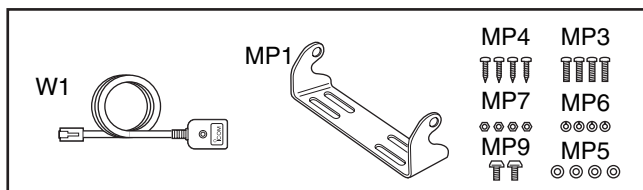
[FRONT UNIT]

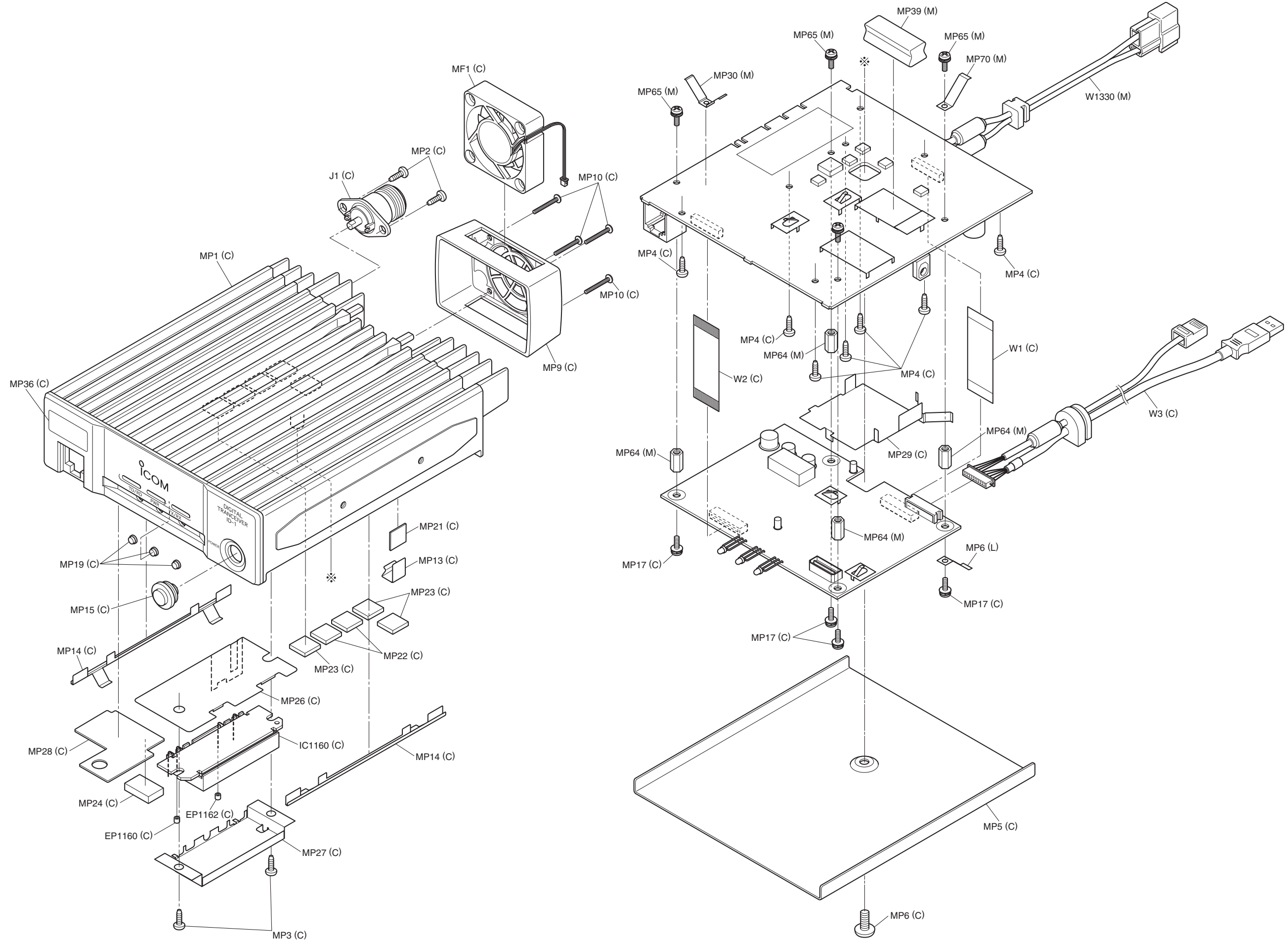
REF.NO.	ODER NO.	DESCRIPTION	QTY.
J1	6450001470	95003-2881	1
S21	2250000270	RH90N74E20-16F-1738	1

Screw abbreviations BT: Self-tapping
 NI-ZU: Nickel-zinc
 ZK : Black

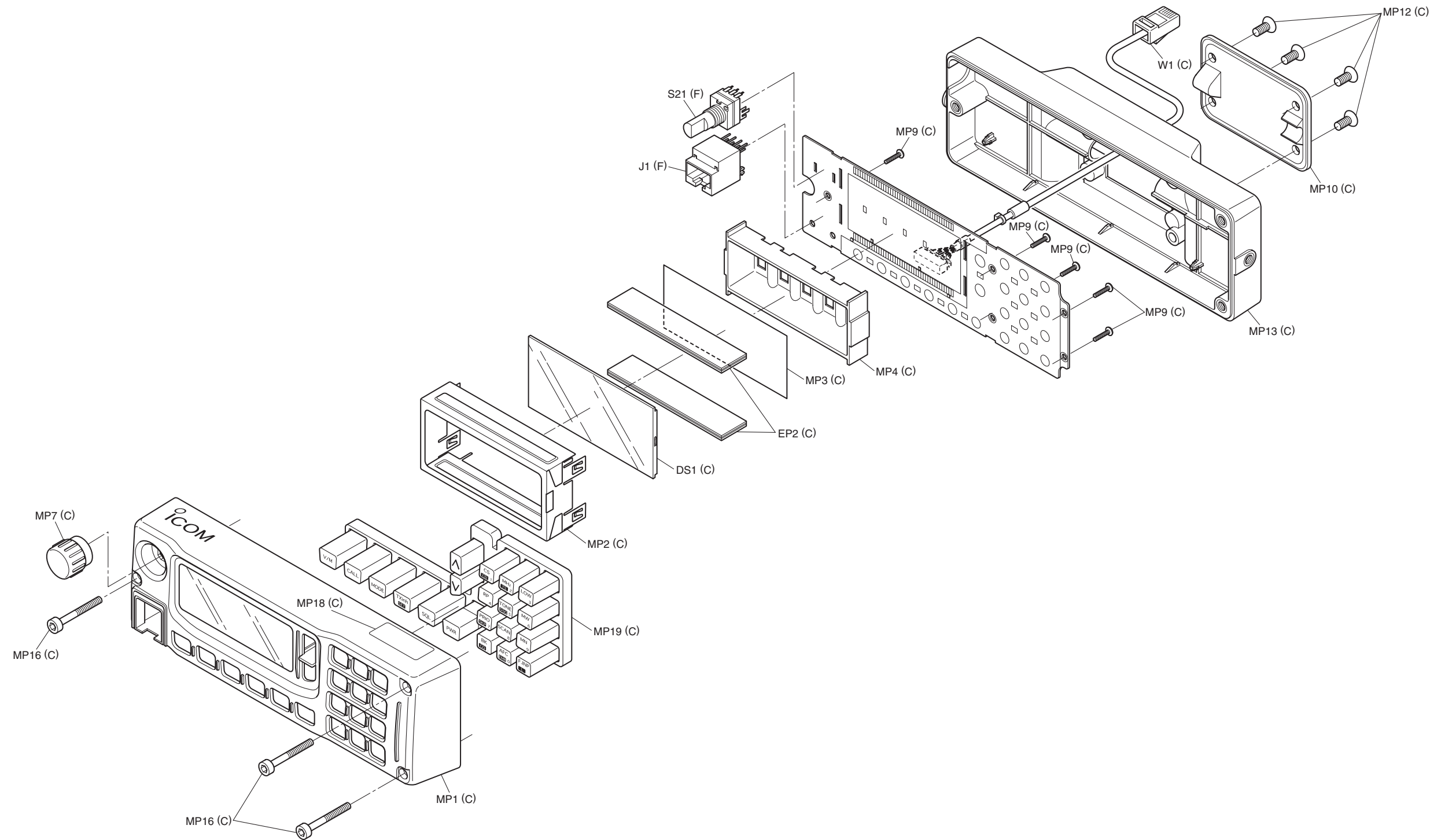
[ACCESSORIES]

REF.	ORDER. NO.	DESCRIPTION	QTY.
W1	Optional product	Cable OPC-647	1
MP1	8010016470	1765 mounting braket	1
MP3	8810000470	Screw PH M5x12(+/-)	4
MP4	8810000950	Screw AO M5x16	4
MP5	8850000150	Flat washer M5 NI BS	4
MP6	8850000390	Spring washer M5	4
MP7	8830000120	Nut M5	4
MP9	8820000910	Screw 1765 SCREW	2





• RC-24



SECTION 9 BOARD LAYOUTS

9-1 MAIN UNIT

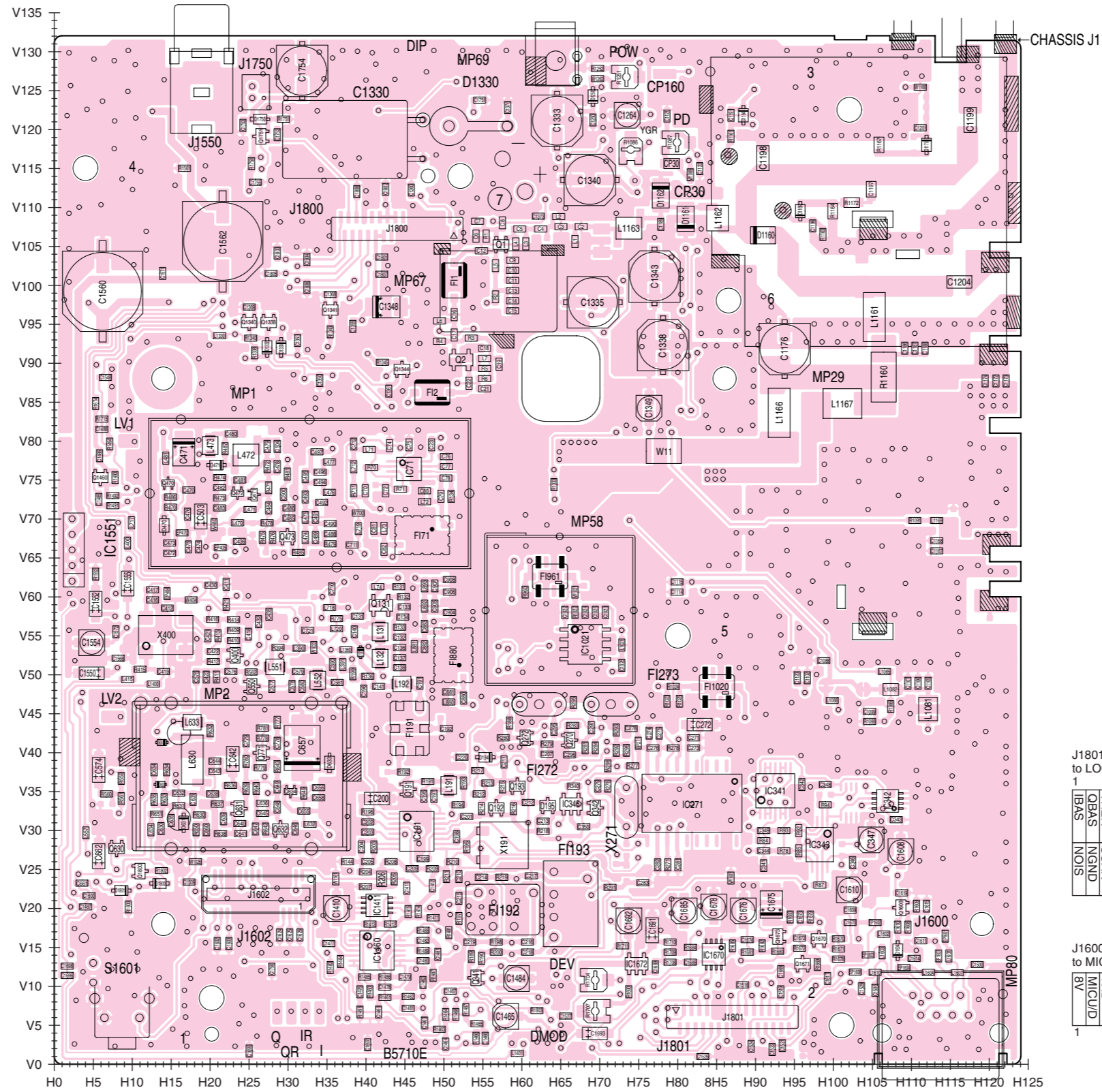
• TOP VIEW

J1800
to LOGIC-1 unit J401
30

PCON	PWR/S	1
GND	GND	
GND	GND	
GND	GND	
GND	GND	
GND	GND	
GND	GND	
GND	GND	
GND	GND	
NC	NC	
HV L	+3	
HV L	+3	
GND	GND	
GND	GND	
FXS	TXS	
FANC	VCTL	
BEEP	AMULT	

J1602
to LOGIC-1 unit J101
16

DAF	GND	30
TXSW	GND	
GND	GND	
GND	GND	
GND	GND	
GND	GND	
GND	GND	
GND	GND	
P2ST	GND	
P2RS	GND	
PDAT	GND	
PSCK	GND	
GND	GND	
UNLK	1CON	
SHIFT	POWRS	1



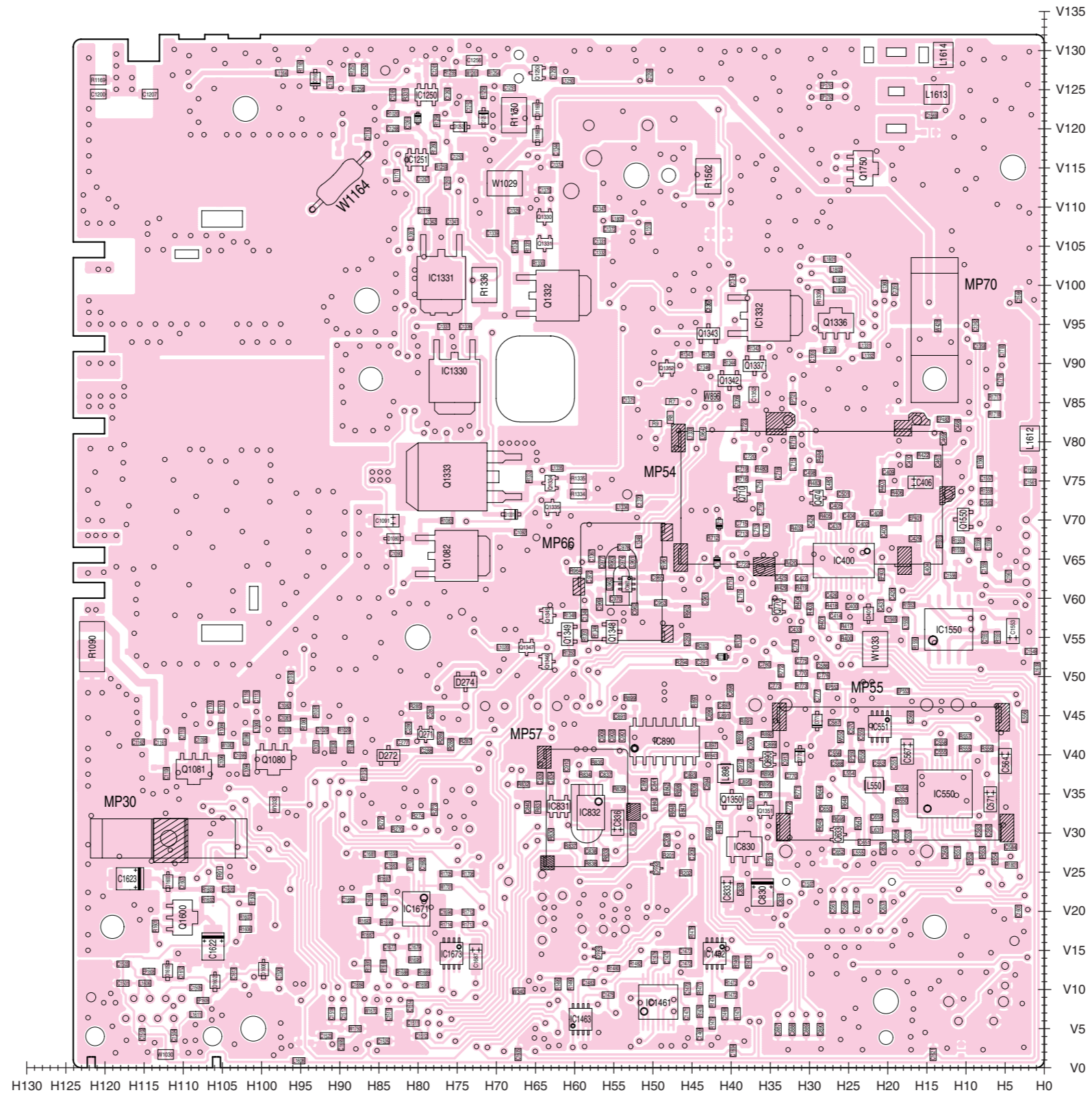
J1801
to LOGIC-1 unit J400
1

PJT	MUD	30
NC	NC	
GENV	RXD	
RSSI	TXD	
+5A	CTOS	
M/E	MIN	
MMULT	GND	
M/GND	W/S	
GND	TONI	
ADSW	DAMOD	
THE	RMULT	
SCAN	NGND	
IBAS	NOIS	

J1600
to MIC
8V

RXD	8
GND	
MIC	
MICE	
PJT	
TXD	
MICUD	
8V	

● BOTTOM VIEW



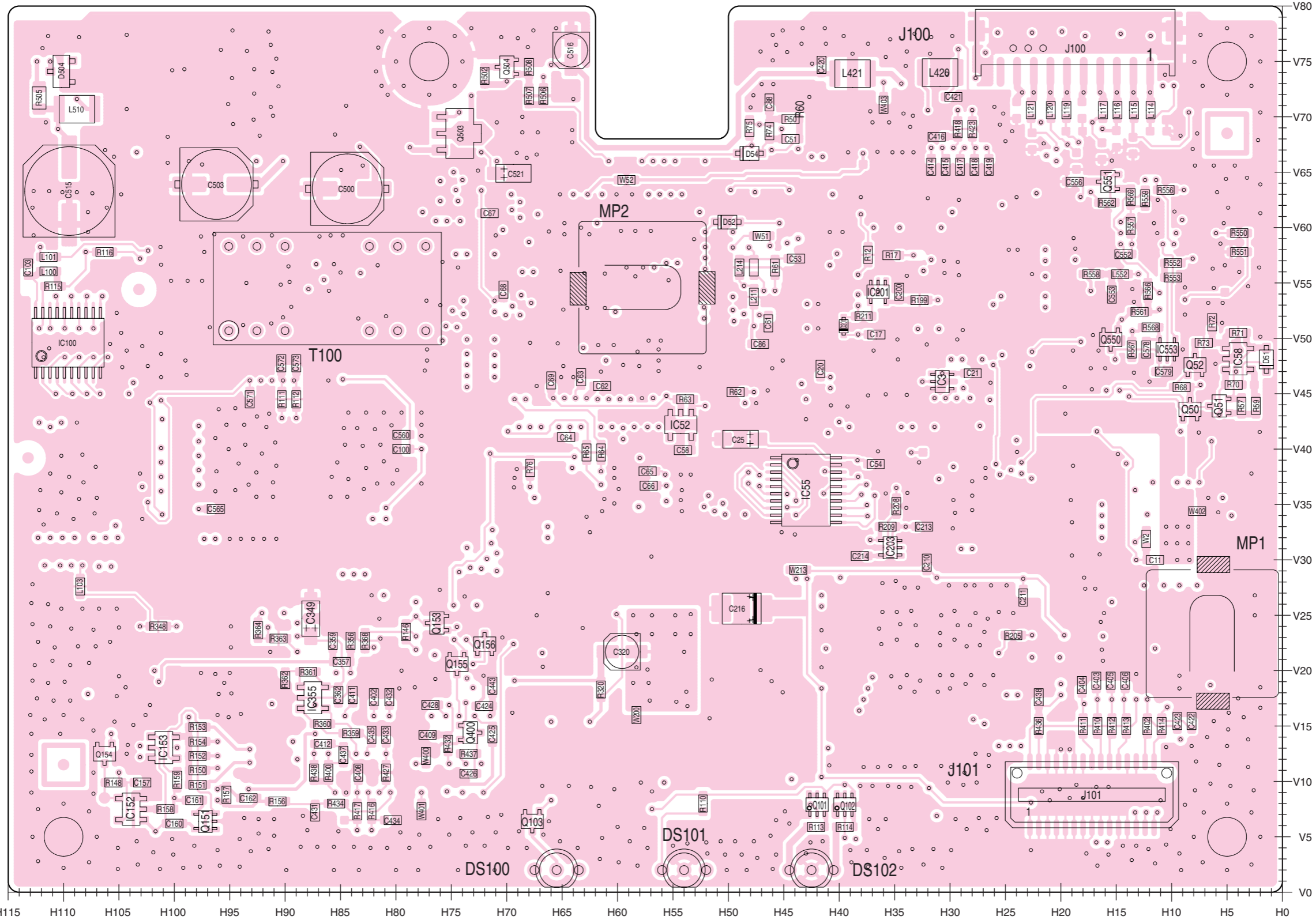
● BOTTOM VIEW

J100
to ETHERNET/USB connector

NC	10
USBGPD	
USBDM	
USBAV	
GND	
TD-	
RD+	
TD+	1

10

1

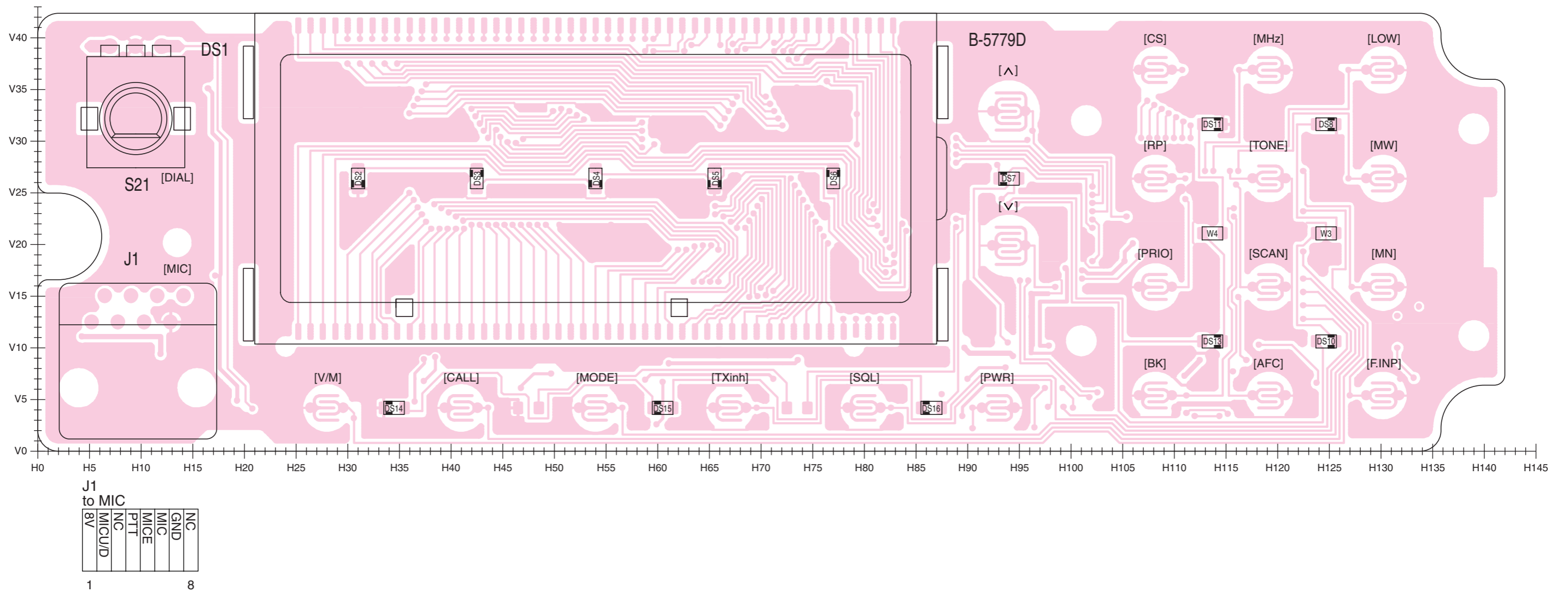


J101
to MAIN unit J1602

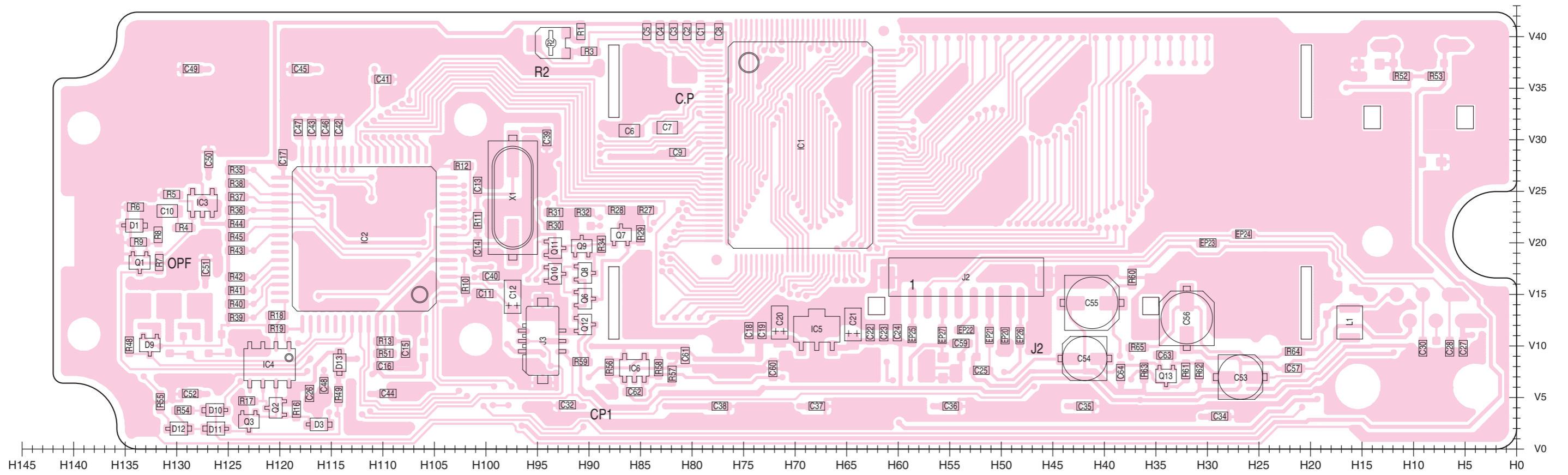
GND	1
DAF	
GND	
TXSW	
GND	
GND	
GND	
GND	
GND	
GND	
P2ST	
GND	
P2RS	
GND	
PDAT	
GND	
PCK	
GND	
GND	
P1ST	
GND	
UNLK	
POWRS	
SHIFT	30

9-3 RC-24

• TOP VIEW



• BOTTOM VIEW

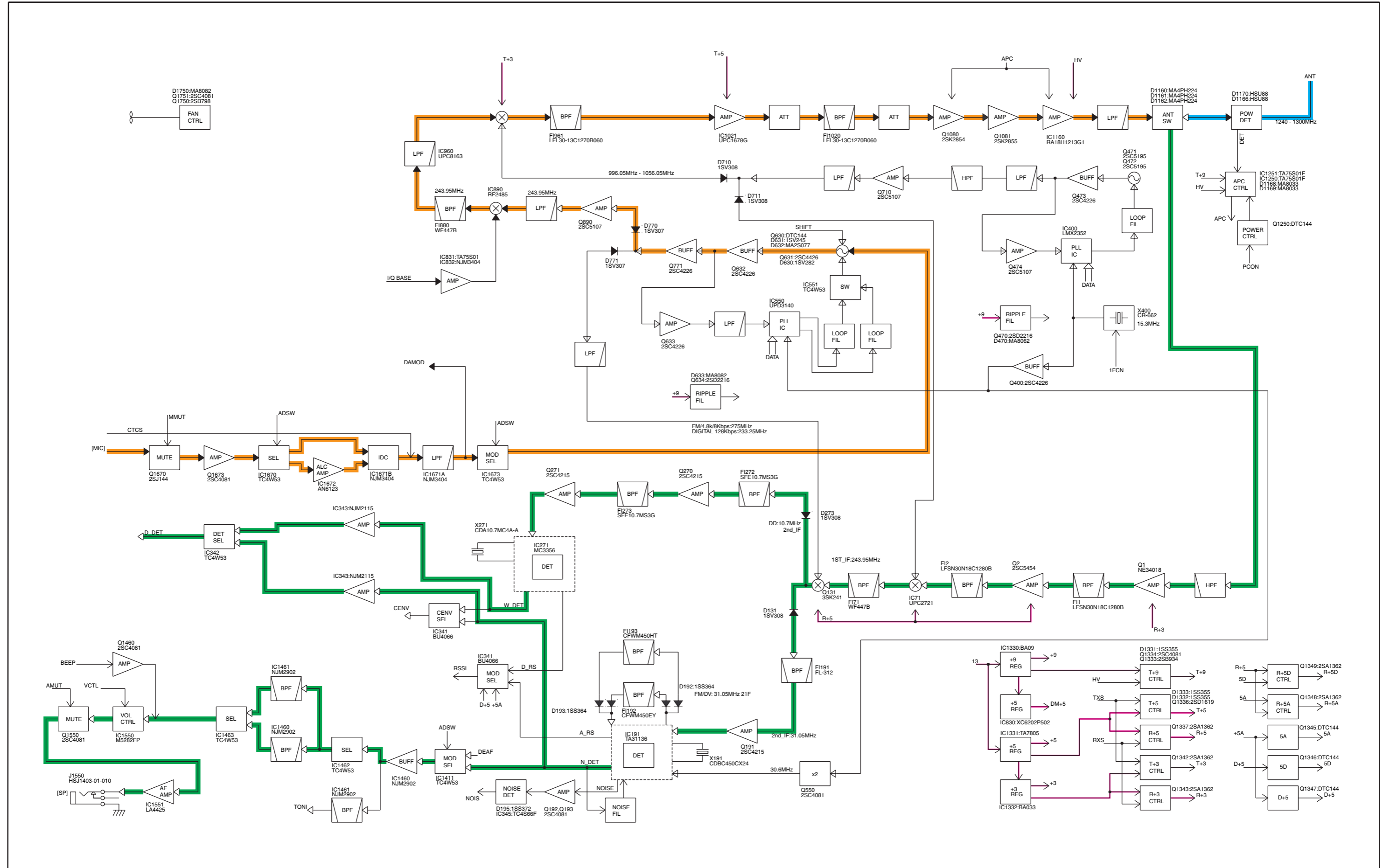


J2
to ID-1 MP80

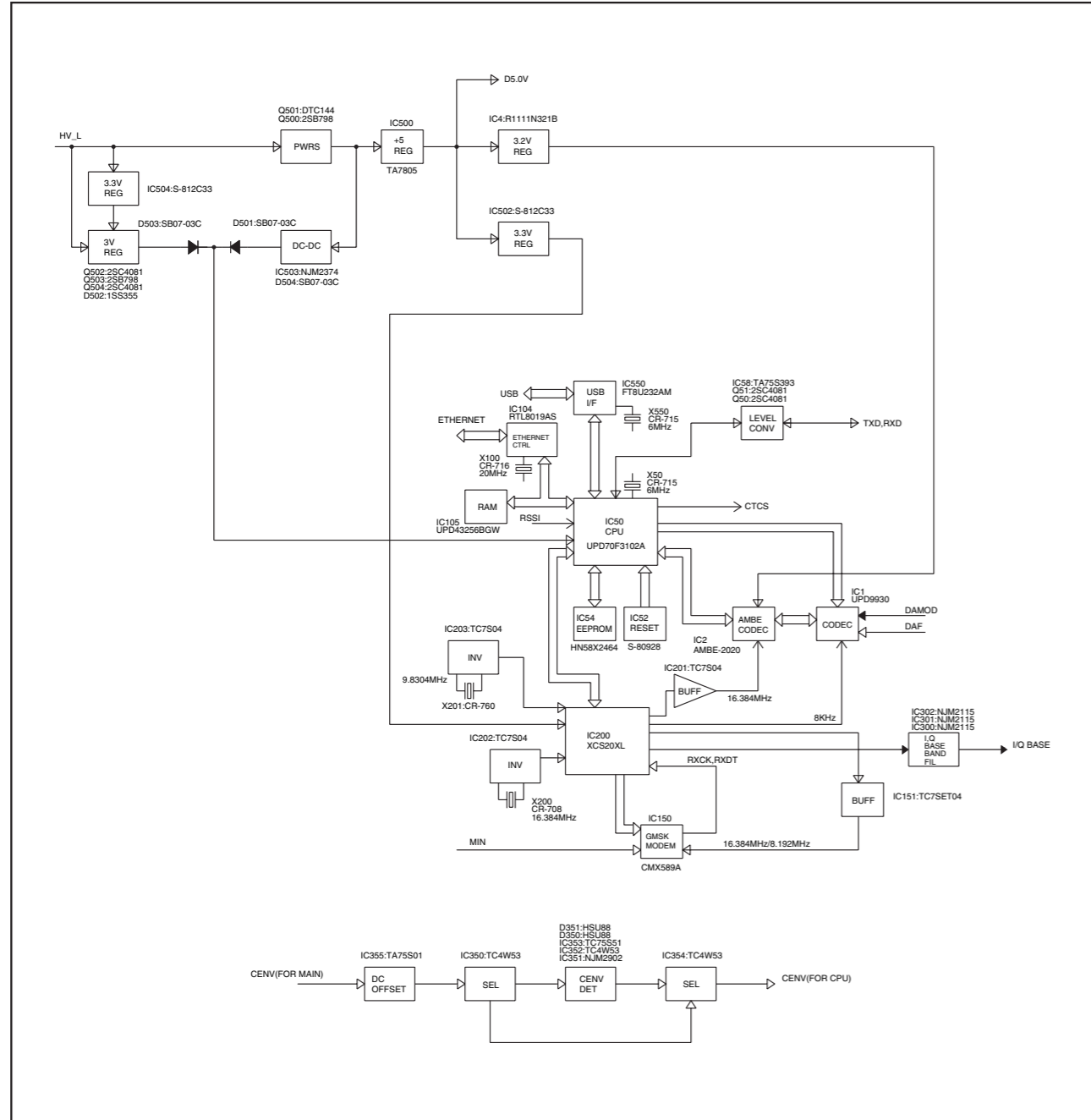
1	RXD
	GND
	MIC
	MICE
	PTT
	TXD
	MIC/D
8V	

SECTION 10 BLOCK DIAGRAM

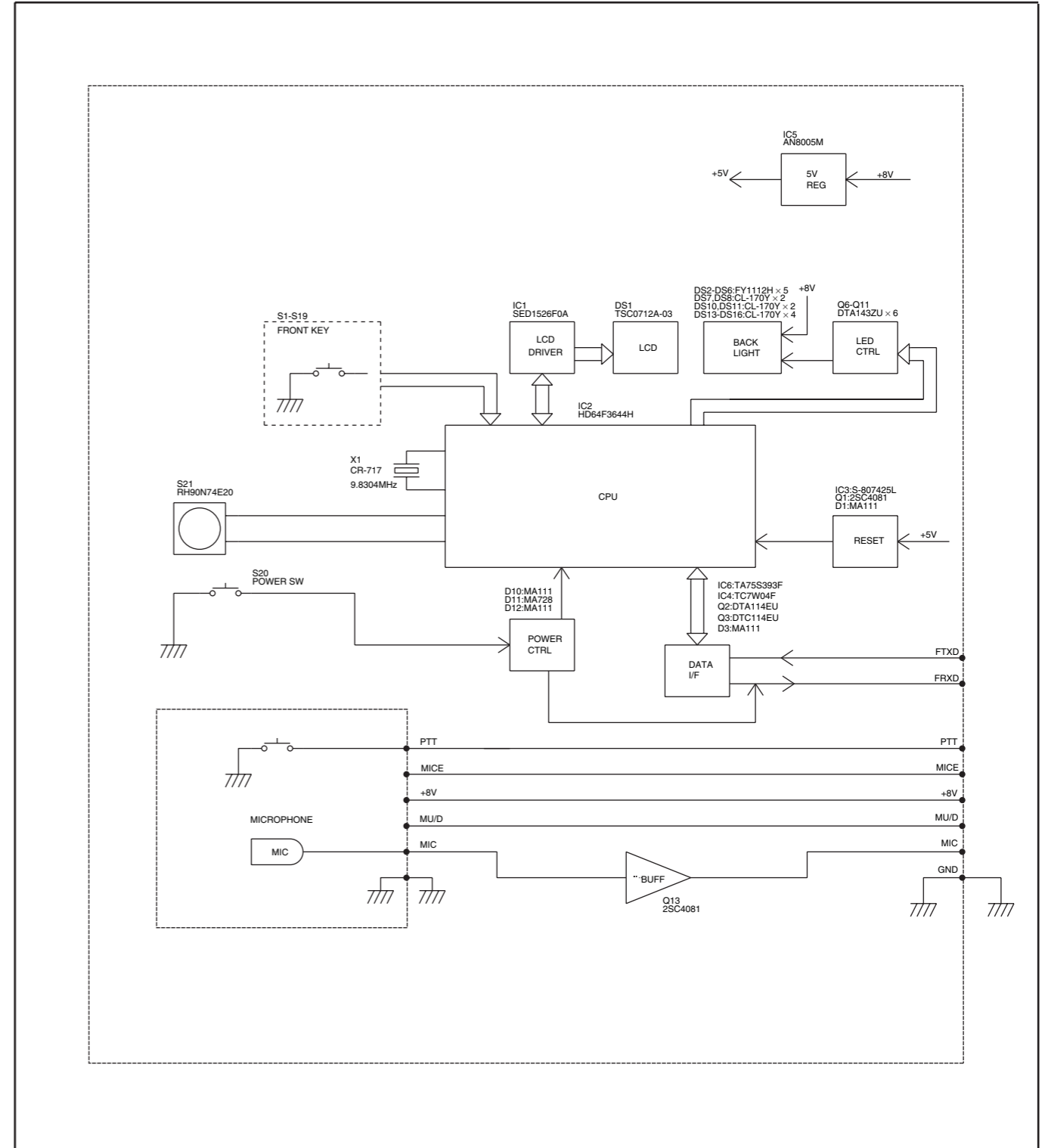
10-1 MAIN UNIT



10-2 LOGIC-1 UNIT

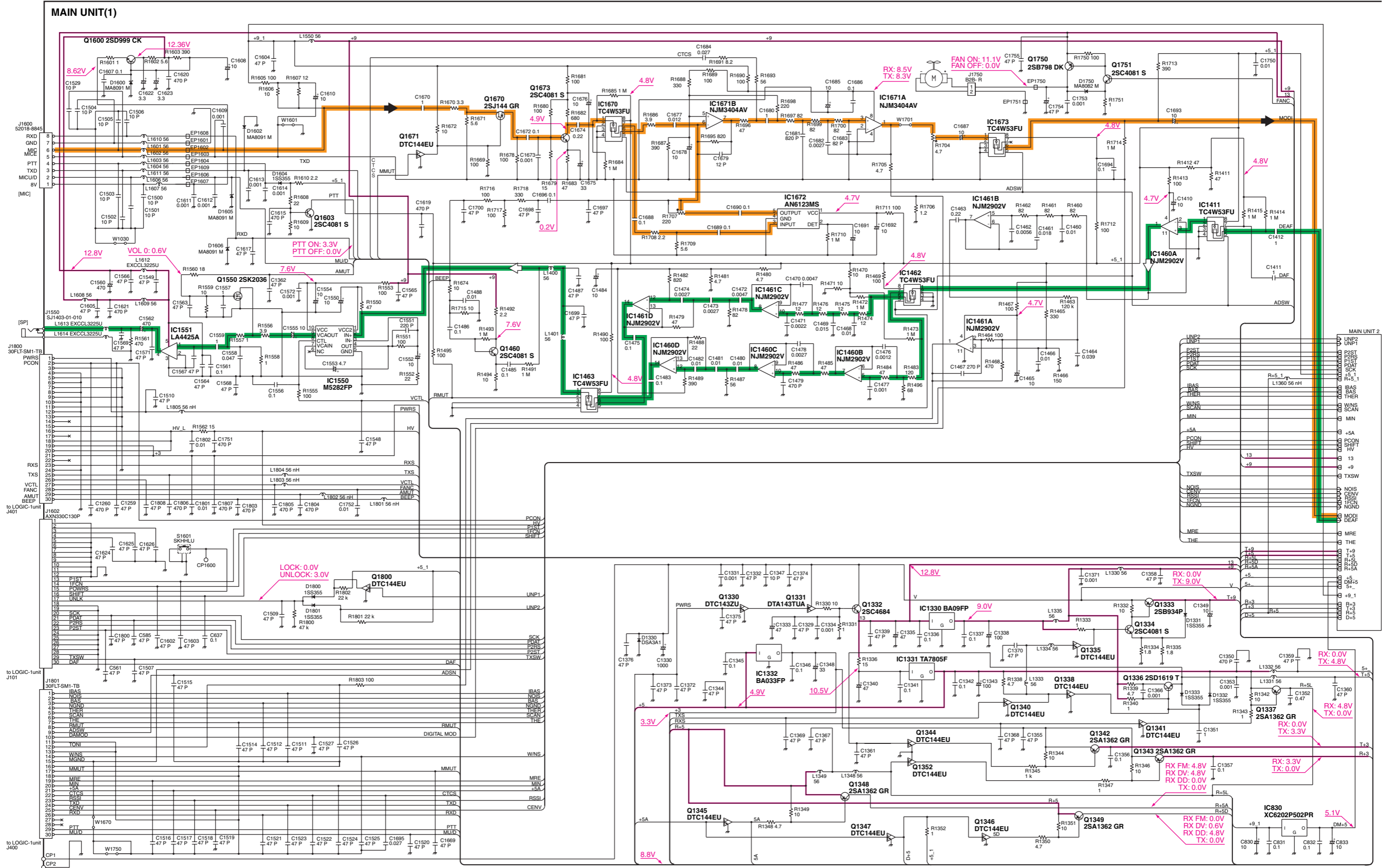


10-3 RC-24

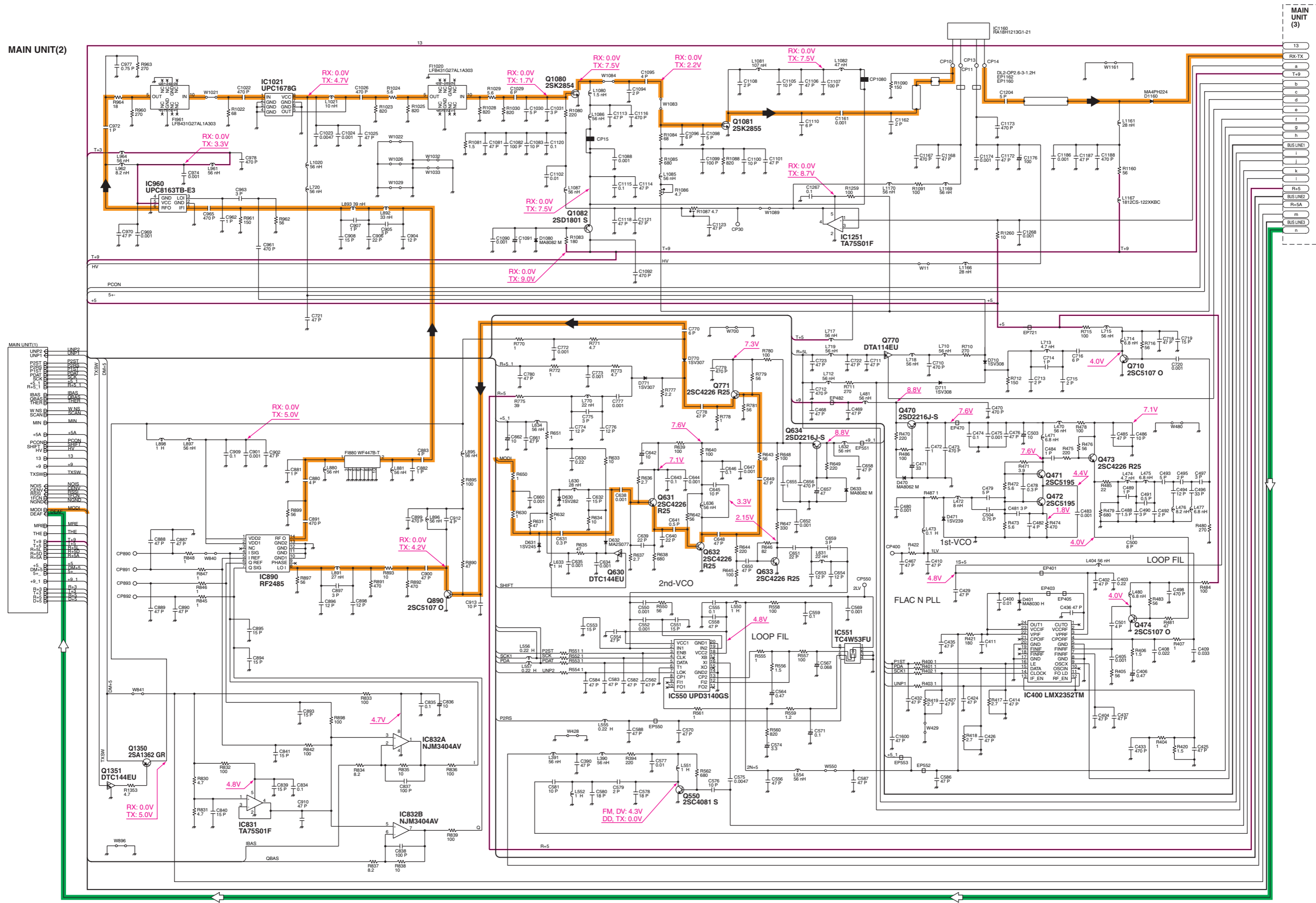


SECTION 11 VOLTAGE DIAGRAM

11-1 MAIN UNIT



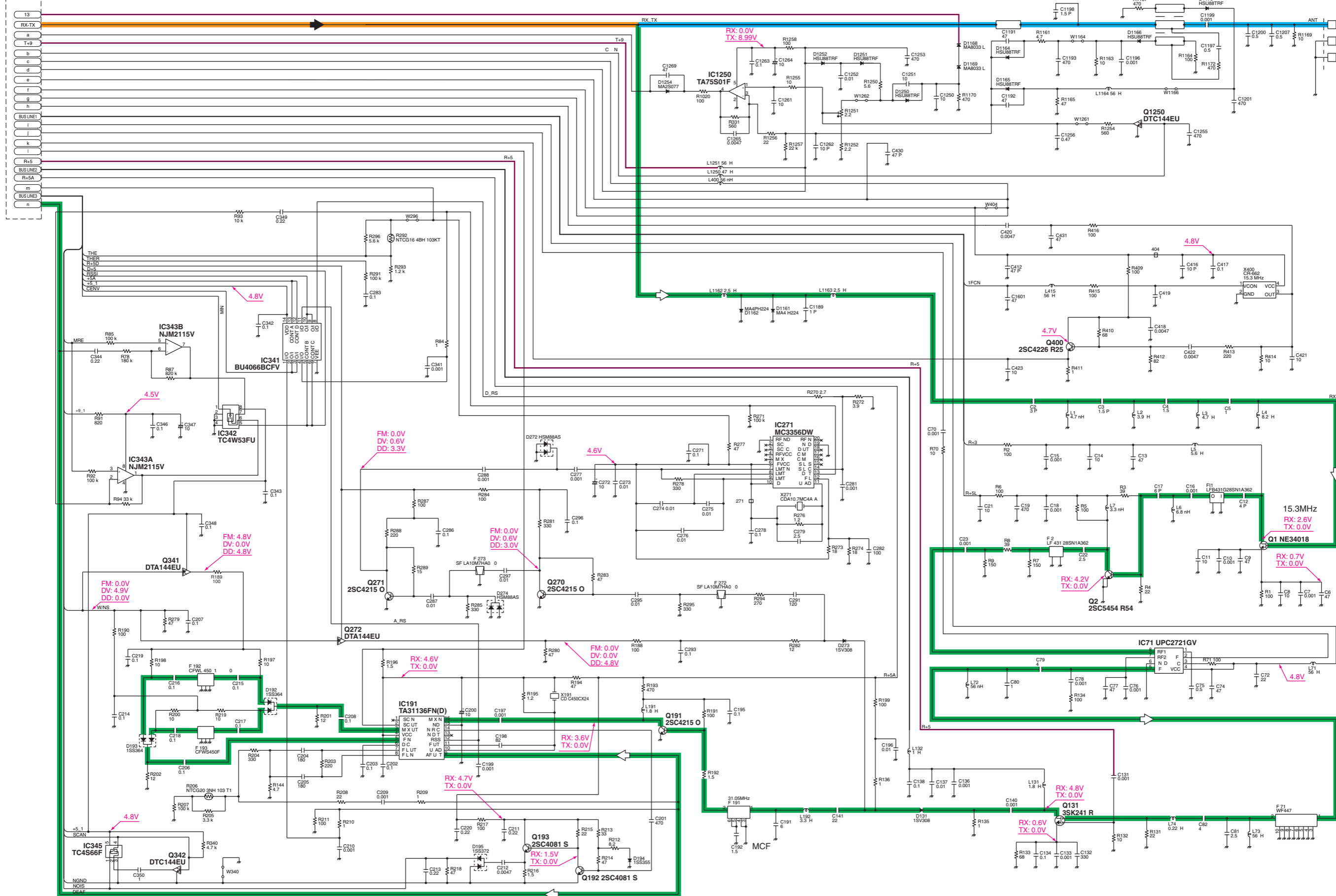
MAIN UNIT(2)



MAIN UNIT (3)

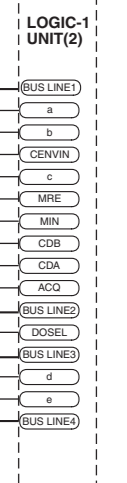
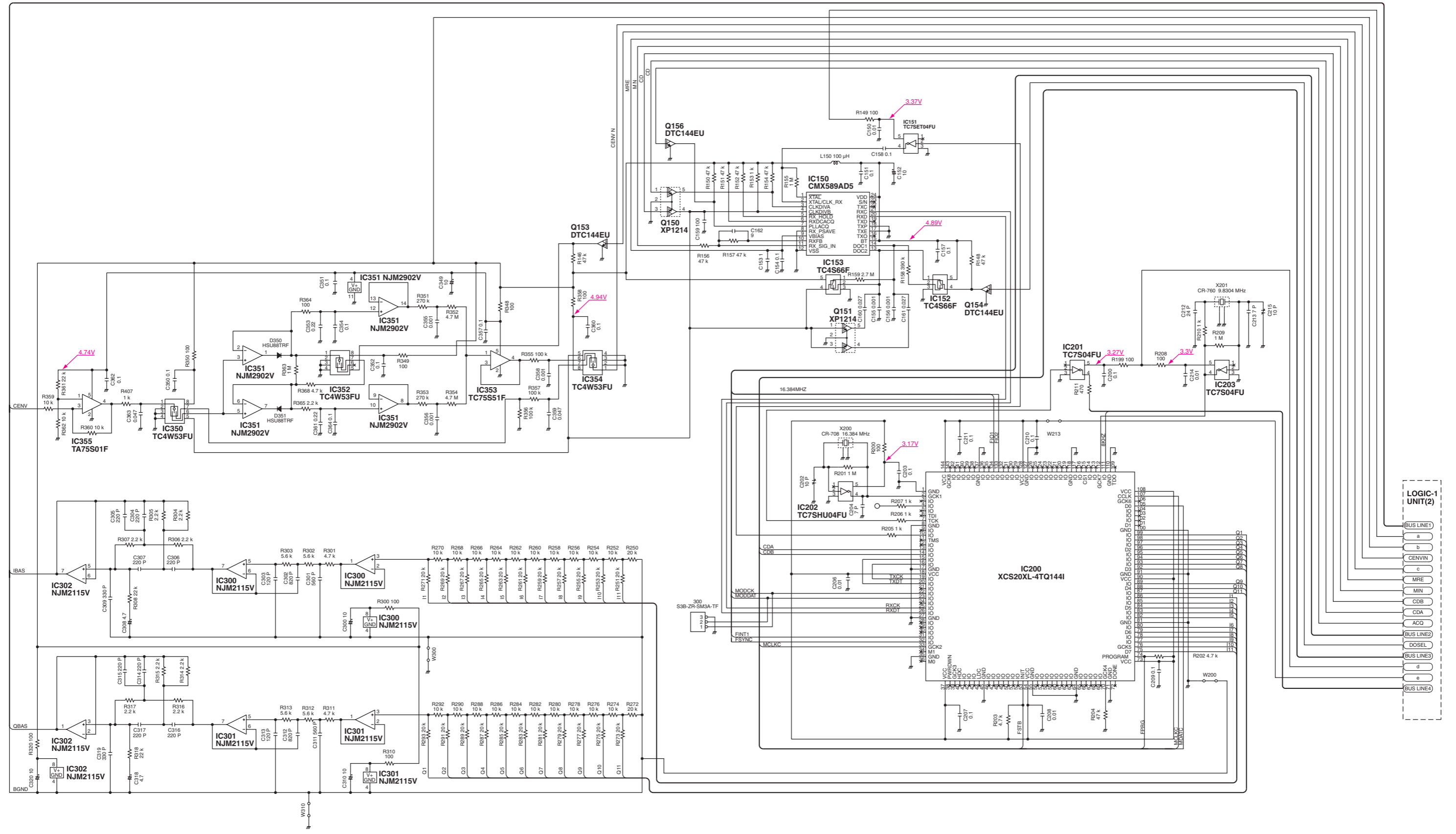
- 13 RX-TX
- a T-9
- b
- c
- d
- e
- f
- g
- h
- i
- j
- k
- l
- R-5
- BUS LINE1
- R-5A
- BUS LINE2
- m
- BUS LINE3
- n

MAIN UNIT(3)
MAIN UNIT(2)

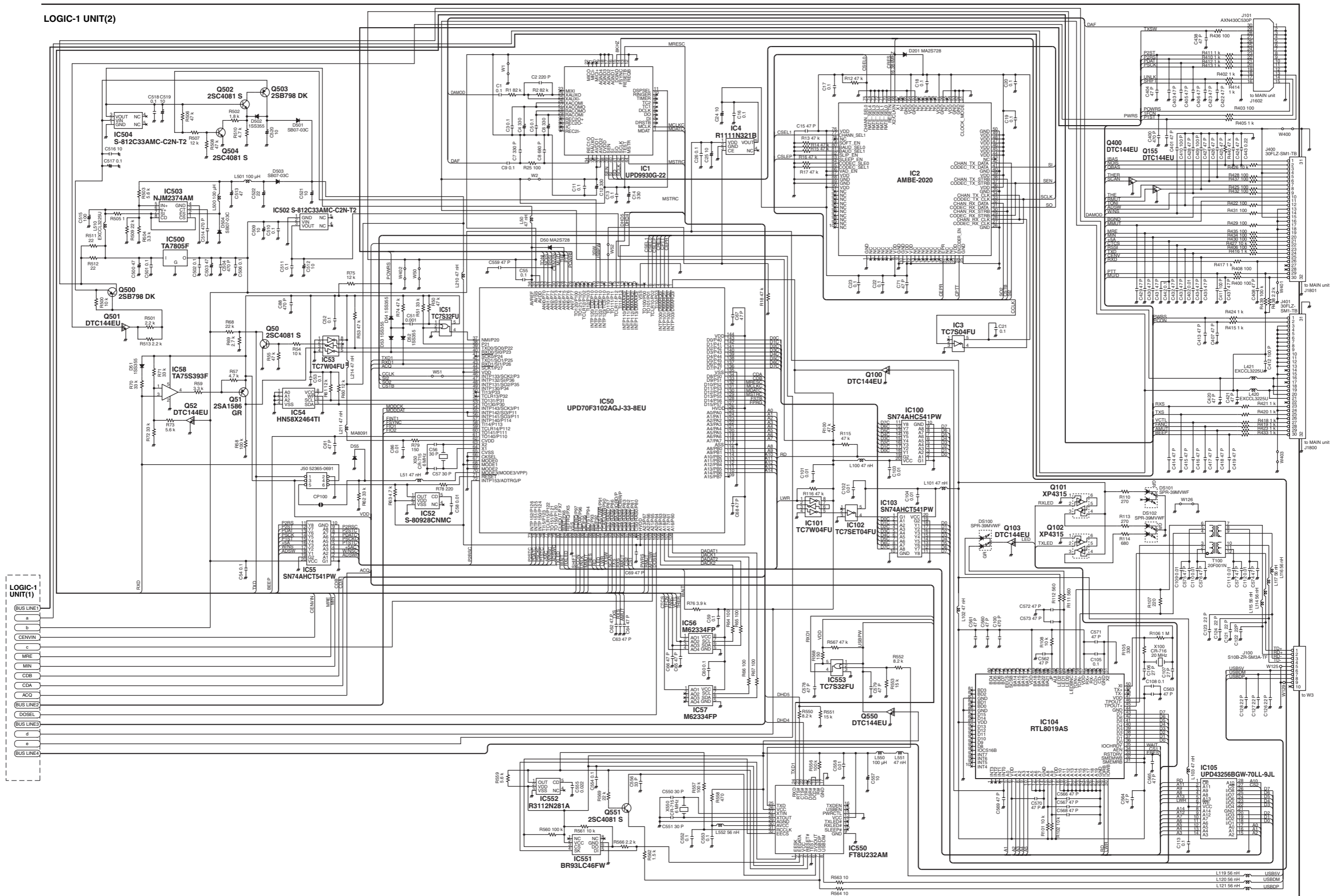


11-2 LOGIC-1 UNIT

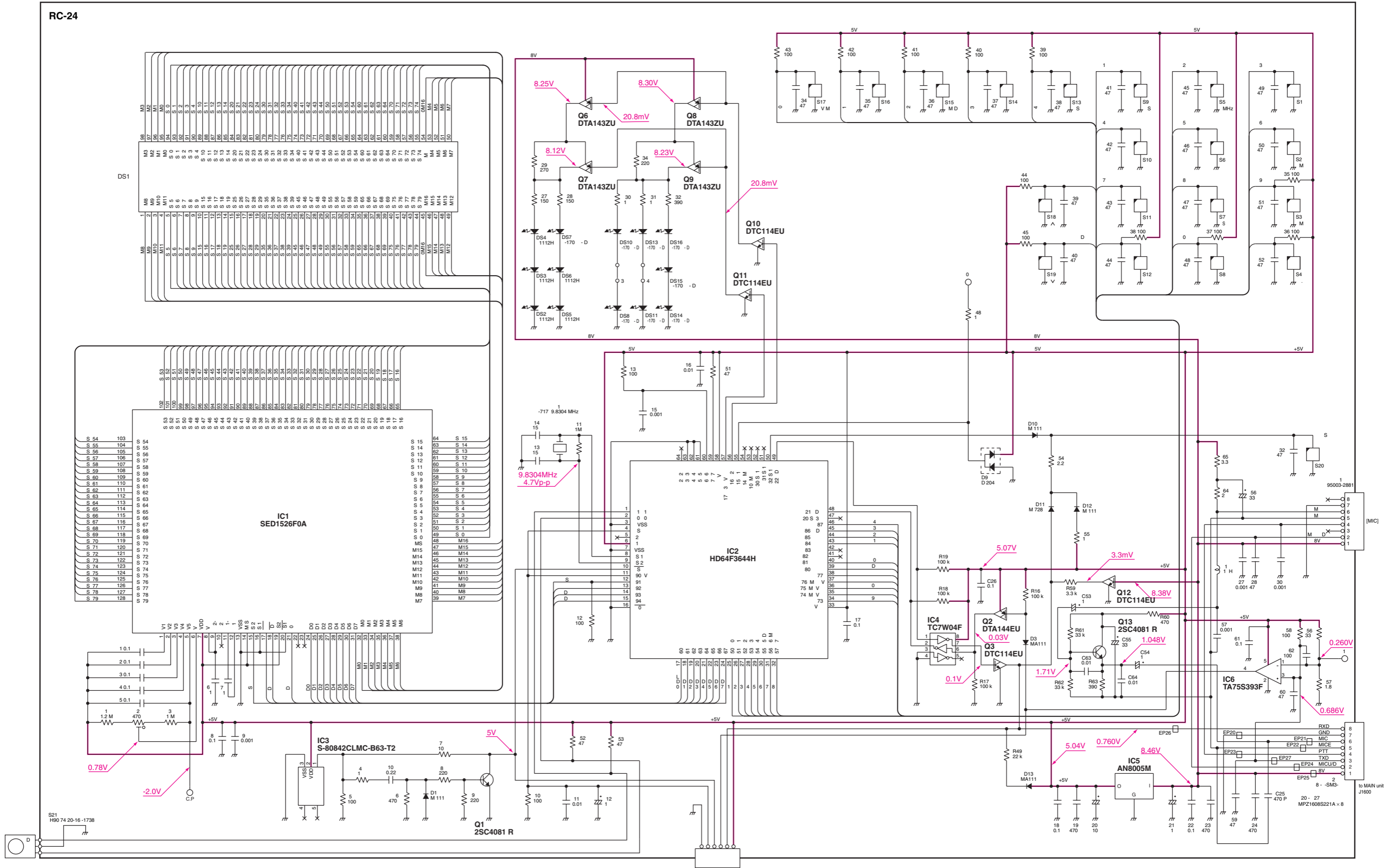
LOGIC-1 UNIT(1)



LOGIC-1 UNIT(2)



RC-24



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