

PRICE: \$30.00

DZ COMPANY · LOVELAND, COLORADO

# DZKIT

## SERVICE MANUAL



SIENNA  
HF RECEIVER/TRANSCEIVER

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## YOUR DZKIT 90-DAY FULL WARRANTY

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During your first ninety (90) days of ownership, DZ Company will replace or repair free of charge—as soon as practical—any parts which are defective, either in materials or workmanship. You can obtain parts directly from DZ Company by writing us, emailing us or telephoning us. And we'll pay shipping charges to get those parts to you—anywhere in the world.

We warrant that during the first ninety (90) days of ownership, our products, when correctly assembled, calibrated, adjusted and used in accordance with our printed instructions, will meet published specifications.

You will receive free consultation (except for the cost of your long distance phone call) on any problem you may encounter in the assembly or use of your DZKit product. Just drop us a line, email us, give us a call, or visit our website and click on "Support". That will give you access to free on-line support and a discussion group. Sorry, we cannot accept collect calls.

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THE DZ COMPANY, LLC  
LOVELAND, CO 80537

Service Manual for the

Sienna HF Transceiver



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## TABLE OF CONTENTS

Troubleshooting .....	4
Voltage, Resistance Charts .....	6
Specifications.....	10
Theory of Operation .....	11
Block Diagram.....	33
Schematics .....	34

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Sienna



## TROUBLESHOOTING

The nice thing about building your own transceiver is being able to fix it if it breaks, or to figure out why it's not working quite right as you turn it on for the first time, WITHOUT having to send it back to us for repair. But we have found that many people lack basic troubleshooting skills. So here are a few tips to help you narrow down a problem:

1. **Start by measuring the main DC voltages on every board.** Is the 5V supply really 5V? Most logic circuits can tolerate a range of 4.75 to 5.25V. If it's less than 4.75, look into the cause – disconnect all boards from the DCD board's power connectors and measure the voltage there. Is it OK? If it is, plug the other boards in one at a time to see which one is affecting the voltage. If not, troubleshoot just the DCD board.
2. **Isolate the problem to a board, and then to a section of that board.** For example, is the receiver working but not the transmitter? Since the receiver uses the same low pass filters as the transmitter, and they are located on the transmitter board, you can rule out one whole section of the transmitter board (all the low pass filter toroids and associated relays).
3. **Figure out what it can't be, to help you understand what it can be.** For example, if plugging in the transmitter makes the receiver quit working, it could be that the transmitter is loading down the shared 8-bit data bus. Or perhaps it is drawing too much power and causing the voltage to drop too low. Measure DC voltages first, to make sure that the circuits you suspect are bad are getting power.
4. **Replace unknown signals with known good ones.** For example, if the receiver doesn't work, is a signal making it all the way from the antenna jack through the antenna switch on the DCD board through the SWR meter circuit, through the tuner, through the low pass filters on the transmitter, through the T/R switch, through the band-pass filters and preamps on the RXBPF board and all the way to the RF input jack on the receiver board? Lots of circuits there! Try disconnecting the normal RF input and connect the antenna input or any other source of RF directly to the receiver board. Because Sienna has a lot of cable interconnects, you have great flexibility in separating one circuit from another.



Symptom	Possible Causes	Fix
5v Supply reads low, front panel seems locked up	C24 on DCD board	Make sure C24 is mounted the right direction, resolder it.
DCD Tray gets hot	Normal without cover on	Attach top cover. The extra heatsinking and fans will keep the tray cool
Antenna A/B relays don't switch	Unsoldered pins	Remove DCD board and check solder connections on all relays
Transmitter does not transmit	TXPVCC signal inoperative. Transformers installed backwards. Jumpers set wrong.	Make sure there is no voltage on the TxInhibit input on the Linear interface connector. Check Q13 base (should read 9.1V). Check R68, D18, R4, R5, Q16. Make sure LPTT goes low during transmit (gate of Q16). Check continuity through low pass filters. Make sure Q4 and Q5 jumpers agree with installed transistor types.
IF Filter Board fails test	Solder connections. ICs or diodes mounted backwards. Cable attached to wrong side of board. Jumpers on test board set wrong.	Inspect all solder joints. Make sure pin 1 of ICs is in square pad. Make sure 8-pin cable is attached to bottom side of board. Re-check the jumpers on the test board.
RxBPF fails test	Toroids, soldering, filters not installed, power connectors installed on wrong side of board	Measure continuity across toroids, resolder. Re-heat all solder connections. Make sure connectors are mounted right.



## VOLTAGE, RESISTANCE CHARTS

Table 1. DC Voltages on DCD/Tuner Board

Measurement point	Voltage
J10 pin 1	5.0V +/- .15V
J10 pin 2	-9.5V +/- .5V
J10 pins 3 and 5	0.0V +/- .05V (ground)
J10 pin 4	Applied voltage (11-15V)
Anode (unbanded side) of D7	0.25 * applied voltage
Cathode (banded side) of D9 and D5	2.7V
Junction of R24 and R25	0.17 * applied voltage



Table 2. DC Voltages on Receiver Board

Pin	Voltage (+/-5%)
J5 pin 1	+5.0V
J5 pin 2	-9.5V
J5 pin 4	+11 to +15V
J13 pin 4	10.0V
TP3	>4.0V
U14 pin 1	-5.0V
U13 pin 3	+5.0V
U18 pin 14	+11 to +15V
U19 pin 14	+11 to +15V
U4 pin 8	+4.5V
U4 pin 4	-9.0V
U22 pin 8	+5.0V
Q5 gate 1	+2.0V
Q5 source	+1.9V
Q5 drain	+8.6V
Q20 gate 1	+2.0V
Q20 source	+1.9V
Q20 drain	+8.7V
U25 pin 7	+10.0V
U30 pin 8	+10.0V
U30 pin 4	-5.0V
U5 pin 8	+5.0V
U9 pin 2	+9.5V
U26 pin 7	+9.9V
U7 pin 8	+5.0V
U11 pin 4	+5.0V
U11 pin 11	-5.0V



Table 3. DC Voltages on Transmitter Board

Pin	Voltage	Mode	Mode Commands	Menu setting
J18 pin 1 (right)	5.0V			
J5 pin 5 (bottom)	VCC			
U18 pin 3 (top)	10.0V			
Test Point: CWFM	9.5V	CWUSB, CWLSB, FM	md3; md7; md4;	
	9.5V	AM, USB, LSB, DIGUSB, DIGLSB	md5; md2; md1; md6; md9;	
Test Point: AM-ESSB	9.5V	AM, USB, LSB, DIGUSB, DIGLSB	md5; md2; md1; md6; md9;	ESSB on (es1;)
Test Point: SSB	9.5V	USB, LSB, DIGUSB, DI- GLSB	md2; md1; md6; md9;	ESSB off (es0;)
JP12 (top)	5.0V			
JP12 (bottom)	5.0V			
J6 pin 1 (left)	2.5V			
JP3 (top)	2.5V			
JP4 (top)	2.5V	USB, LSB, DIGUSB, DI- GLSB	md2; md1; md6; md9;	ESSB off (es0;)
U20 pin 1	2.5-3.5V	USB, LSB, DIGUSB, DI- GLSB	md2; md1; md6; md9;	ESSB off (es0;)
U20 pin 2	3.0V			
U20 pin 4	2.5V			
C162 (bottom)	1.8V	USB, LSB, DIGUSB, DI- GLSB	md2; md1; md6; md9;	ESSB off (es0;)
U17 pin 1	2.5-3.5V	As Tx drive is varied	md3; md7; md4;	Tx Drv CW/FM
U17 pin 1	2.5-3.5V	AM, USB, LSB, DIGUSB, DIGLSB	md5; md2; md1; md6; md9;	Tx Drv AM/SB
U17 pin 2	3.0V			
U17 pin 4	2.5V			
U8 pin 1	2.5-3.5V	as RF Power is varied		Tx ALC off (al0;)
U8 pin 2	3.0V			
U8 pin 3	2.5V			
U8 pin 4	2.5V			





Pin	Voltage	Mode	Mode Commands
JP7 (left)	1.4V	Transmitter keyed	
Q3 base (left pin)	1.2V	Transmitter keyed	
Q3 emitter (right pin)	0.4V	Transmitter keyed	
Q3 collector (center pin)	VCC		
R21, C9 or C133 (top)	9.5V	CWUSB, CWLSB, FM Transmitter keyed	md3; md7; md4;
Q4 collector (center pin on 2SC1969)	VCC		
Q5 collector (center pin on 2SC1969)	VCC		
R42 (top)	5.0V	Transmitter keyed	
R42 (top)	<0.7V	Transmitter keyed  (Key down in CW modes, PTT pressed in phone modes)	
D3 cathode	4.3V	Transmitter not keyed	
D3 cathode (square pad)	<0.7V	Transmitter keyed  (Key down in CW modes, PTT pressed in phone modes)	
Top right pin on K2	<0.8V	Freq < 2 MHz	fa00001800000;
Top right pin on K4	<0.8V	Freq 2-6 MHz	fa00003500000;
Top right pin on K6	<0.8V	Freq 6-12MHz	fa00007000000;
Top right pin on K8	<0.8V	Freq 12-20MHz	fa00014000000;
Top right pin on K10	<0.8V	Freq 20-30 MHz	fa00021000000;



## Specifications

**Frequency range:** 10 kHz to 30 MHz, and 50-54MHz Rcv (Specs valid 500 kHz-30 MHz)

**Modes:** SSB, CW, AM, FM, (Digital via Sedona accessory)

**FM modulation:** frequency modulated carrier with pre-emphasis, selectable deviation (2.5, 4, 5kHz)

**FM receive IF:** 455kHz, includes two 4-pole +/-10KHz ceramic filters (can be replaced with filters as narrow as +/-3KHz)

**Sensitivity:** 0.4uV for 10dB S/N (preamps off, PSB™ off)

**MDS (PSB off):** -120/-128/-132dBm (preamps: off/1/both)

**MDS (PSB on):** -125/-130/-132dBm (preamps: off/1/both)

**BDR:** >105dB at spacings greater than 1KHz, >115dB at >4KHz spacings

**Tx IMD:** 3rd order: -40dB PEP @ 10W output, -37dB @ 100W, 5th order down > 50dB

**Noise Blanker:** Variable threshold

**Freq stability:** +/-1 ppm (0-50C) after 30 minute warm-up, using included TCXO

**Displayed resolution:** 1 or 10 Hz (internal resolution is sub-Hz)

**Tuning step size:** 1, 10, 100, 1K, 10K Hz

**RIT, XIT range:** +/-16MHz, with two speeds (10 Hz, 1 kHz steps)

**Memories:** 147, including 85 programmable GP memories preset to desired bandplan, one scratchpad preset to WWV, all accessible using external keypad or PC, 5 VFOA memories per band and one VFOB memory. 10 12-character CW buffers, editable in menu, activated from external keypad. Farnsworth timing selectable from menu.

**Mic input impedance:** 150-600 Ohms, balanced and unbalanced

**IF frequencies:** 70.455 MHz, 9.0 MHz, 455 kHz

**IF Filter selection:** (see Inrad web site for filter specs) *NOTE: Most Inrad filters must be mounted on Yaesu-compatible "C" boards. If ordering directly from Inrad, be sure to specify this option.* Exceptions are the 6k Hz AM filter at the 2nd IF and the 20 kHz ceramic or 5.8kHz Collins mechanical filter at the 3rd IF.

**Broadband IF frequency output:** 455Khz and 9MHz +/-100KHz, 50 ohms

**IF Notch:** 30dB attenuation, tunable +/- 10kHz (at 455kHz IF)

**Transverter output:** Use 10w Tx output or unfiltered 30mW low level RF output on 10M

**Stereo audio output power:** 1.5W/ch (available even while using headphones)

**Linear control outputs:** QSK via high-power MOSFET, TTL band data, ALC (range 0 to -5v)

**DSP** (DSP - autonotch, variable bandwidth filters, NR, AGC) software from Silicon Pixels included with Sedona

**DC power requirements:** 2.5A receive (10-15v), 6A transmit @10W, 26A transmit @100W output (13.8-15V)

**Dimensions:** 3.5"H x 14"W x 16"D (feet located in a 12.25" x 14.0" area)

**Weight:** 10 lbs (base unit), 12 lbs with 100W amp

Specifications subject to change without notice.



# Theory of Operation

The Sienna HF transceiver is organized into five major blocks:

- DC Power conditioning (DCD board)
- Control (Controller, Front Panel and VFD boards)
- Receiver (Receiver, BPF and IF Filter boards)
- Transmitter (Transmitter, TXBPF, Tuner and 100W amplifier boards)

Refer to the Block Diagram on page 33 and the Schematics starting on page 34.

## **DC Power Conditioning: DCD board**

*Over-voltage. Under-voltage, reverse polarity and overcurrent protection*

Kit rigs sometimes fail to do some basic power conditioning on the input, making them failure-prone. The Sienna includes over- and under-voltage protection, over-current protection (fuses), and reverse polarity protection. In addition, the internal DC voltages of +5V, +9V and -9V are derived from regulators which have additional input and output protection circuitry.

Refer to the DCD board, sheet 3. The DC input from Anderson Powerpole connectors is protected from reverse polarity by diode D6. Capacitor C21 adds some protection against static discharge and shunts any high frequency energy to ground.

R26 and zener diode D9 tap a small amount of current from the input even when power is off in order to provide a 2.7V DC reference for comparator U7, an LM393. Capacitor C22 assures that any rapid changes in the input voltage will be swamped out, keeping the reference voltage stable until the input voltage drops well below normal.

R9, R10, D7 and C20 provide a voltage divider with long attack and very fast decay, setting the low trip point at about 1/3 of the input voltage. When the voltage rises above  $2.7 \times 3$  (8.4V), the output of comparator U7 (pin 1) goes high. As long as the other comparator output (pin 7) is not low, the DC voltage will be enabled. Diode D7 assures that when the voltage drops, capacitor C20 is discharged quickly.

R24, R25 and C23 form a similar divider and stabilizer to detect when the voltage is above 15V.

Resistors R11 and R12 on one comparator, and R13 and R23 on the other, add a couple of Volts of hysteresis to keep the output of the comparators from oscillating at the trip points.

If the output of either comparator goes low, transistor Q2 turns off, causing K19, a 25A automotive relay, to open, which removes power. When the comparator outputs are both high,



pullup resistor R14 assures that Q2 will be on, enabling the relay to turn on. The relay cannot actually turn on unless the on/off switch is pushed because one side of the relay coil is routed through the switch to DC power.

Fuse F1 protects the radio from overcurrent conditions. This is a 9A Resettable fuse. When it warms up enough due to overcurrent conditions, it suddenly develops a high resistance, keeping high current from flowing. As it cools, it automatically resets.

When Q2 and the on/off switch are on, DC voltage appears at pad W3, which provides power for the 100W amplifier. Since this is a high current lead, it is located as close as possible to the relay to minimize voltage drop. A short cable connects this point to the amp. When the tray is rotated up for service, an extension cable is required. This extension cable will have noticeable voltage drop when the 100W amp is in use, so performance could suffer. As a result, it should not be used except for testing.

#### *On/off switch LED*

Comparator U6 is used to detect when the DC voltage going to the regulators has dropped to a low enough level that they are about to shut down. When the voltage gets to a little over 10V, the LED inside the on/off switch is turned from green to red. This is useful when operating the radio from batteries.

#### *Regulators*

The 5V regulator, U8, is a low-drop-out regulator, which means that it does not require much more voltage going in than it generates. However, excessive voltage going in would make it run very hot, so its input voltage is dropped by pass transistor Q1 and regulator U9 from the input of 11V-15V. Both regulators have input and output protection. Q1 is mounted to the tray, and U9 is mounted to a board on the chassis bottom, providing excellent heatsinking, and the fan in the compartment in front of the tray helps keep the tray and the regulator cool during normal operation. During service, with the top open, the cooling effect of the fan is greatly reduced, but the unit has been tested for extended periods in this state with no ill effects.

U10 is a MAX765 negative voltage generator. It is a “chopper”, which turns the DC input voltage into an AC voltage which is then converted back to DC and output as a negative DC voltage. This negative voltage is used by the receiver to allow high performance dual supply op-amps to be used. RFC1 helps keep the switching transients off the line, which could induce noise into the sensitive receiver circuits.

The raw DC input is also fed to the receiver, controller and transmitter. The receiver uses the raw input voltage on the audio output amplifiers in order to allow them to handle the very high instantaneous currents (up to an amp!) needed for good speech reproduction.



### *Antenna switch, SWR meter*

The DCD board also has an antenna A/B switch and an SWR meter on it (see sheets 2 and 4 on the DCD/Tuner schematic). Relay K17 and K18 switch between main antennas A and B. The use of two relays instead of one provides better port-to-port isolation. A portion of the transmitted signal, both forward and reflected signals, is picked up by transformer T1 and fed into buffer U5. The outputs are clamped to keep the levels from exceeding 5V, and are fed to the main controller's A/D converters for measurement. C17, RV1 and RV2 are used to calibrate the meter so that the measured voltages correspond to correct power levels as measured against an external wattmeter. If no wattmeter is available, a 50 ohm dummy load allows the meter calibration to come close.

In order to handle both 10W transmitters and 100W amplifiers, the output of U5 is scaled by resistive dividers R31/R37 and R32/R36. A signal (/NOPA) from the amplifier goes high if the amplifier is present and enabled. If it is not present, R5 keeps the voltage low, forcing Q6 and Q7 to be off and removing the scaling factor. Since the resistors provide a high impedance load, the outputs of the dividers drive unity gain buffers in U11 which then present low impedance (and thus less noisy) drives to the controller. Since the op-amps are powered from the raw DC supply that is capable of reaching 15V, the outputs are protected with zener diodes and limiting resistors to make sure the controller board does not see voltages higher than 4.7V.

Control circuits are discussed in the Controller theory section.



## Control: Controller, Front Panel and VFD Boards

The main Controller board is the heart of the Sienna. An Atmel Mega644P microcontroller (U9) running at a clock frequency of 16MHz provides the main control functions, and a second Mega644P (U30) is used for Keyer, VOX/AntiVOX detection, microphone sampling in FM, keypad detection and meter backlight functions. A +/-1 PPM Temperature Compensated Crystal Oscillator (TCXO), six Direct Digital Synthesis (DDS) chips and associated bandpass filters and high bandwidth buffer/amplifiers provide a clean source of high purity, low phase noise local oscillators for the transmitter and receiver.

Refer to the Controller schematic pages, Sheets 1 through 11. While this four layer board is very dense and may look formidable, the circuitry is actually very straightforward. Sheet 1 shows the DC input conditioning. Two 3.3V regulators are used to drop the 5V down to 3.3V for the DDS chips and the buffers that drive their data and address busses. R2/C3 and R38/C46 provide decoupling for the analog 5V supply that is used for the A/D converter circuits on the microprocessors.

### *Main microprocessor*

Sheet 2 shows the main microprocessor. This processor has 64K bytes of internal program storage, 4K bytes of RAM and 2K bytes of Electrically Erasable Programmable Read-Only Memory (EEPROM). The EEPROM stores constants and lookup tables such as the filter parameters, current state of the instrument, band plans and so on. A software timer writes data to the EEPROM every 10 seconds if anything that needs to be saved has changed. Main memory and EEPROM memory can be rewritten through the SPI bus (J6), which is what is used at the factory to initially program the processor, or through the RS-232C port (pins 9 and 10 on the processor, going to U7 on Sheet 4. The ST207E converts CMOS voltages into RS-232C levels which are fed to the PC or the back panel via J4. Other RS-232C control lines (RTS, CTS) are also converted to CMOS levels by U7 and fed to the secondary microprocessor to allow handshake control and use of RTS as a CW key. RS-232C signal DTR is fed into the PTT circuitry via Q2 and Q4. Q21 allows this signal to be disabled (via control bit SERDIS), since at boot-up, the PC can pull the DTR line and we do not want it causing the rig to go into transmit mode!

U8 is a power-on reset chip providing a long reset pulse to start the processor correctly when power is first applied.

### *LTxEn, HRcvEn*

The signal that turns on (enables) the transmitter is called LTxEn. As with many signals, the “L” means it is low true (0 Volts). (“/” is also used to indicate low true signals.) This signal is generated by the main microprocessor in response to detection of a Push-To-Talk (/PTT) signal from the microphone, or by the Keyer microprocessor (PTT\_Keyer), which is responsible for VOX detection and for CW keying, or by the DTR signal on the RS-232 port. DTR can be disabled via an output port bit called SERDIS to keep RS-232 problems from holding the transmitter on. These three signals are wire-or’d together and fed into an input port as HPTT so the main microprocessor can tell when a transmitter enable signal is either being requested by the



user (the mic's /PTT) or when the Keyer is controlling it. An output port bit, PTT0, or the Keyer, via PTT\_Keyer, are used to generate LTxEn, which is fed to the 10W transmitter as well as the 100W amplifier (Sheet 7).

The Keyer microprocessor also controls when the receiver is enabled, through the signal HRcvEn. The two control signals, LTxEn and HRcvEn, are sequenced so that the receiver is muted before the transmitter turns on, and so that the transmitter has time for the RF to make it all the way through the various amplifier stages (and so that RF bleedthrough into the receiver stages also have time to propagate) before the receiver is un-muted and its AGC controls returned to normal.

Sheet 4 also shows the 5V to 3.3V level converter (U10) that drives address and data lines on the DDS chips.

#### *A-to-D (A/D) Converters*

Going back to Sheet 2, the Mega644P has eight A/D converter inputs. There is actually only one 10-bit A/D inside the chip, and it uses a multiplexer to look at one analog input at a time. The signals fed into the first seven inputs are the FM squelch, AF Gain, RF Gain, Mic Gain, Headphone Volume, RF Power and RF Processor pots that are located on the Front Panel board and fed into the Controller on J9 (Sheet 6). The eighth analog input comes from U19 on Sheet 7. This CMOS analog multiplexer selects one of eight additional voltages: Forward and Reflected Power from the DCD/Tuner board; Supply voltage, ALC/compression and Driver Current from the 10W transmitter board; Final Current from the 100W PA board, S-Meter value from the Receiver board, and the value of the IF Filter switch on the Front Panel. An interrupt routine in the microprocessor selects and samples one of these 15 voltages every time an A/D conversion completes (about every 64 microseconds).

#### *Parallel Data Bus*

Also on Sheet 2, Port C of the processor is used as an 8-bit parallel data bus for all boards. This bus is buffered by U15 to become the "XBus". Its output is enabled only when data on one of the boards needs to be changed, otherwise pull-up resistors on each board terminate the bus and keep it quiet to avoid causing unnecessary digital interference to the transmitter or receiver.

U20 is an address decoder. AS0, AS1 and AS2 (U34, Sheet 6) select one of eight data strobe pulses for the DDS chips and read/write pulses to the Keyer microprocessor.

#### *I/O Stobes, inter-processor communications and address decoding*

Port B on the microprocessor is used for I/O control. IOStrobe1 and /IOStrobe2 serve as clock pulses to output data from Port C to the various I/O chips on the Controller board. (The "/" in front means that the signal is low true, meaning that it is normally high and pulses low when active.) DispRDY and /DispCk are signals from and to the Vacuum Fluorescent Display board that are fed to the Controller board from J17 on Sheet 7. KeyerRDY is a signal from the Keyer microprocessor (U30, pin 42, Sheet 3) that tells the main processor that data is either ready on



port C or has been accepted from port C. Q12 provides a Frequency Update pulse for all DDS chips. A4 and A5 are address lines for the DDS chips.

Port D has the RS-232C data lines TXD and RXD, Rotary Pulse Generator (RPG) outputs from the two tuning dials, and additional address lines for the internal I/O ports and DDS chips.

Sheet 5 shows address decoding for the 16 data strobe lines /Strobe1 through /StrobeG. These are used to output and input (“strobe”) data on port C to and from all boards in the rig as well as various control functions on the Controller board. Sheets 5 and 6 show most of the internal ports. /Strobe1 and /Strobe2 read switch data from the Front Panel board. /Strobe2 also reads the state of the internal PTT line so that the processor knows when an external device (microphone, etc.) has activated the Push-to-Talk. /Strobe4 (Sheet6) and /Strobe7 (Sheet 5) provide outputs that directly drive LEDs inside the pushbutton switches on the Front Panel board. /Strobe6 (Sheet 5) and /Strobe5 (Sheet 6) provide 16 outputs that are used for a variety of control functions.

/Strobe8 through /StrobeG are fed to the Receiver, Transmitter and Tuner boards along with the XBus to program those boards. (See Sheet 7).

### *Serial Bus*

A serial bus is also fed to the Receiver and Transmitter boards. SCL (U13 pin 9) and SDA (U13 pin 12, as well as U12 pin 17) (Sheet 5) form a high speed I<sup>2</sup>C bus that is used to control DACs and Digitally Controlled Potentiometers (DCPs) on the Receiver and Transmitter boards. This bus is quiescent (not active) unless changes are needed, which helps avoid digital interference to sensitive receiver and transmitter circuits.

### *DDS*

Sheets 8 through 11 show the DDS chips, bandpass filters on each output, and buffer amplifiers. Normally, DDS chips only require low pass filters on their outputs. Sienna uses bandpass filters so as to provide a much more constant impedance across the frequencies they must output, which helps to keep the level constant without the need for complex AGC circuitry. These devices take five bytes (AD9851) or 6 bytes (AD9852) of digital data and convert it directly to a frequency. The 0-512mV output must be converted to +/-256mV, amplified, and filtered to remove harmonics and other spurious signals (spurs). Close in spurs are typically down at least 70dB. A +/-1PPM TCXO provides a stable, low phase-noise 30MHz reference oscillator for all six DDS's.

The TV (Transmit VFO, not television!) signal coming from the TXVFO DDS (U5) on Sheet 8 is routed to a pair of Hittite GaAsFET switches which are controlled by TXVFILT (Sheet 5, pin 2 of U13). These switches allow one of two low pass filters to be applied to the output of the TXVFO amplifier. The TXVFO covers the frequency range 12.5 to 40.4MHz, so a low pass filter tuned for, say, 41MHz, would allow harmonics from frequencies at the lower end of the range to pass through, so a dual range filter helps keep the output pure. The firmware performs the switch at a TXVFO frequency of 22MHz (operating frequency of approx 11.3MHz).





Note that a similar switch is not needed for the RXVFO, because it operates at a much higher frequency range of 70-124MHz. Any harmonics of 70MHz fall well outside the upper cutoff of the Butterworth bandpass filter (130MHz).

### *LED Backlight*

Sheet 7 shows backlighting circuitry for the meters. Q13, Q14 and Q15, along with the associated resistors, form a 3-bit binary control, allowing up to 8 brightness levels. The control lines for these MOSFETs come from the Keyer processor. High intensity LEDs D1-D4 provide plenty of light for the two meters.

### *MIC Bias*

A 9V bias for electret mics can be turned on and off via Q16 (Sheet 7). The MICBIAS control bit from U13, pin 19 on Sheet 5 is used for this.

### *Keyer microprocessor*

Sheet 3 is a diagram of the Keyer processor. The keyer speed, dot weight, dash weight and pitch pots from the Front Panel board are fed into the first four A/D inputs on port A (ADC0-3), similar to those of the main processor. A/D input 4 (the 5th input) comes from the transmitter (routed through the receiver board) and is a buffered, uncompressed version of the microphone audio, level shifted so that it idles at 2.5V with a peak-to-peak AC voltage of up to 5V. For VOX detection, the processor takes a running average of the AC voltage and computes an RMS value that is tested against a trip threshold set by a menu option. (During FM transmit, all A/D inputs are disabled except the mic, so that rapid sampling of the audio can occur, with this information passed to the main microprocessor in order to re-program the DDS chip controlling the BFO in real-time.) Similarly, the buffered and level-shifted speaker output is fed into A/D input 7 to form the AntivoX input. Another RMS calculation is done on this signal and used along with a menu item to adjust the trip point of the VOX input up or down. A/D input 5 is the external keypad input. Yaesu designed the FH-1 keypad as a set of 12 buttons with resistors in series with them such that 12 different DC voltages from 0 to 5V are produced. The firmware tests these voltages to determine which button has been pushed and sends this coded information over the internal inter-processor bus (port C on both processors, with KeyerRDY, /KeyerRd and /KeyerWr). The Keypad input from the back panel is routed to A/D input 5, which reads the 0V to 5V signal to determine which of 12 buttons was pushed.

A/D input 6 is grounded. This bit allows the processor to determine if the controller board is rev A or B. Rev A boards left this line floating (pulled high by an internal pullup inside the processor). Different code is executed depending upon whether the board uses rev A or B hardware.

Port B, bit 3 is used as a Pulse Width Modulated output signal whose frequency is determined by the Pitch pot. The output is filtered by an RLC network and routed to the Front Panel board where it goes through the Sidetone pot and back to J11 which then goes to the Receiver board's audio output stage. If no front panel is present, jumper JP2 (Sheet 7), assures that the Sidetone (at full volume) will make it to the receiver board.



The dot paddle and dash paddle inputs are filtered and fed to two edge-driven interrupt lines (port D, bits 2 and 3). The manual key input is fed to bit 0, where it is sampled continuously in the 1ms interrupt routine. Outputs from the Keyer are the PTT\_Keyer line, which is routed to the controller to allow the Keyer to control the PTT line, and the Key line, which is routed to the transmitter.

The Keyer processor also has its own SPI bus for programming and a power-on reset chip. This processor is not programmable by the user. Any changes to its internal firmware must be done either by the factory or in the field through the use of an inexpensive Atmel programmer board (STK500).

### *Display board*

The VFD board is a Noritake GU256x64C-3900 model that is programmed with ASCII control command sequences. It connects to port C as just another I/O device. DispRDY and /DispCk signals provide the handshaking. Jumper JP1 on the Keyer processor tells the main controller if a front panel is present. One of the effects of this is to cause the display routines to be ignored if no front panel is present.

### **Receiver: BPF, Receiver and IF Filter Boards**

Refer to the block diagram on page 33 and to the schematics on pages xxx-xxx.

### *Antenna to bandpass filters*

RF from the main antenna ports (A and B) passes through low pass filters and a transmit/receive (T/R) PIN diode switch on the transmitter or 100W amplifier boards. From there, the signal enters the antenna input (J2) on the RXBPF board (See RXBPF schematic, Sheet 2). Relay K6 selects either this input or one from the Receive Antenna input (J3) after the latter is passed through a 55MHz low pass filter. The Receive Antenna does not pass through band-specific low pass filters or a T/R switch as does the main antenna, which reduces the loss, but also exposes it to potential intermodulation distortion (intermod) from strong shortwave stations. If you experience intermod when using the receive antenna, we recommend use of an external bandpass filter such as those made by Array Solutions. RFC1 is a 1mH choke that routes low frequencies to ground, reducing hum from power lines.

### *High-pass and bandpass filters, attenuator1, input overload protection, PSB<sup>TM</sup>*

The selected signal is then fed through a high-pass filter located between relays K6 and K7. If selected, this filter reduces the chance of intermod from strong AM broadcast stations. A menu option allows the filter to be enable or disabled on a VFO memory basis. The signal then passes through a 10dB attenuator which can also be switched out. Pressing the front panel Pre2/Atten button activates this attenuator unless preamp1 is on. The output of the attenuator is clamped by diodes D1 and D2 to prevent large input signals from damaging the rest of the circuitry. It is then coupled to two outputs via transformer T3, which can be disabled. One output is passed to the back panel for connection to a secondary receiver. The other is connected to point "A" on



the schematic, which is the bus that all eleven bandpass filters are connected to, each controlled by a pair of GaAsFET switches, with each filter handling a different segment of the HF spectrum. In addition, one pair of GaAsFETs (U14/U15 on Sheet 7 of the RXBPF board) is allocated as a bypass. This circuit represents the DZKit exclusive Passive Signal Boost (PSB)<sup>TM</sup>. By skipping the BPFs, any associated front-end loss is eliminated at the expense of a potential increase in intermod, and an increase in the noise floor, since more spectrum is allowed in. However, on a fading band, that extra 5dB of “gain” (actually “lack of loss”) can spell the difference between hearing and not hearing a weak signal. PSB is not intended to be used except under such conditions. We do not recommend that you leave it enabled permanently even though signals will sound stronger.

### *Preamps, attenuator*

The selected bandpass filter’s output is point “B”. Referring to Sheet 9 on the RXBPF board, B is routed directly to the first preamp (Q4 and associated circuitry) and to relay K4, where it can be fed to the RF output without preamps. The first preamp’s output can be switched on by relay K1 and appears at point R2, which feeds preamp2 (Q4 and associated parts) and relay K5. If K5 is disabled, so is K2, and thus Q4 has no power and provides only a weak load for preamp1. If K2 and K5 are enabled, preamp1 is fed into preamp2 and then out to the RF output.

The preamps are low noise 2N5109 bipolar transistors set up for a power gain of 10dB each and coupled via broadband toroid transformers T1 and T2.

### *Receiver first IF*

The RF output of the RXBPF board feeds into the Roofing filter board. It is applied directly to a Minicircuits ADE-1MH diode ring mixer (U1). Local oscillator LO1 from the controller, which is the VFO, is set to the displayed receive frequency plus 70.455MHz and fed into the LO port. The output, consisting of sum and difference frequencies and a number of other mixing products, is fed into an 85 to 50 ohm LC T-filter to remove reflections from the following splitter, a Minicircuits ADP-2-1. One output drives an Inrad 4.5KHz bandpass filter at 70.455MHz and the other is fed back to the receiver board unfiltered for use with the FM receive and IF output circuitry.

The output of the bandpass filter is amplified by Q5, a dual-gate MOSFET with about 20dB of power gain. The second gate of Q5 is derived from the AGC circuitry on Sheet 6, buffered and inverted by U1 to provide a nominal 4V on gate 2, decreasing to 2V under full AGC action and reducing the gain accordingly. The source is biased at 1.2V, so the 4V on gate 2 represents 2.8V of gain enhancement. When the control voltage goes down to 2V in response to a strong signal detected by the 3rd IF, the differential of 0.8V reduces the gain to its minimum level.

The output of Q5 feeds a Darlington transistor configuration, which provides high input impedance and low output impedance, necessary to successfully drive the next RF mixer. Resistors R101 and R126 set Q5’s load impedance to about 1.3K ohms to provide a moderately high impedance load for the amplifier, whose nominal output impedance is about 200 ohms, while biasing the Darlington stage at a reasonable level. This preserves the power gain while allowing the



stage to drive the low impedance (50 ohm) mixer load.

### *Receiver second IF*

The 70.455MHz 1st IF output of the Darlington driver feeds U8, a TUF-3 mixer, along with LO2 from the controller set to 61.455Mhz (+/-, depending on filters in use and desired side-band). The difference product of about 9MHz is used for the 2nd IF, allowing a wide variety of Inrad crystal filters to be used. Transformer T4 boosts the 50 ohm output impedance of the mixer up to 1800 ohms while providing a factor of 6 voltage gain. The signal is fed into another amplifier (Q20, Sheet 3) that is identical to that of the previous stage. R54 and C51 decouple the buffered AGC voltage from the first stage.

### *Noise Blanker*

The amplified 9MHz output of Q20 drives another Darlington buffer which then drives the noise blanker circuitry on Sheet 4. The noise blanker is placed ahead of the crystal filters so that it can detect broadband noise pulses (limited only by the roofing filter). The noise blanker is a simple 9MHz bandpass filter with an input and output impedance of about 120 ohms having a group delay of several microseconds, long enough for the IF amplifier, U12, to detect a signal and generate a blanking pulse just as the signal arrives at NBOUT. Three pulse widths are allowed using control bits NBPWA and NBPWB that are latched into U2 (Sheet 1). The NBOn-Off bit enables or disables the noise blanker by controlling whether power is applied to the detection circuit. When unpowered, the gating transistor, Q7, is always off. A DAC output, NBThr, provides a variable trip point. Since FM and the Noise Blanker are not used at the same time, NBThr is used for both circuits.

Since there is about 11dB of loss in the noise blanker, and up to 15dB of additional loss in the crystal filters and associated resistive pads, the output of the noise blanker is boosted by high bandwidth amplifier U25, an Analog Devices AD8000 op-amp in a gain of 5.7 configuration. The op-amp has high input impedance, allowing resistors R150 and R151 to set the input impedance to a value that matches the output impedance of the noise blanker, while providing enough gain to offset the loss in the noise blanker and crystal filters and a low output impedance capable of driving the crystal filters.

### *Crystal Filters*

The crystal filters are plugged into 4 slots on the IF Filter board. Up to four filters can be installed on the IF Filter board at the 9MHz IF frequency. The first one is an Inrad 2311 6KHz filter. This provides enough bandwidth for AM reception. The standard filter is a 4-pole 2.4KHz Inrad model, providing good bandwidth for SSB and CW reception. All filters are switched via 1N914 diodes, and impedance matched on input and output via Minicircuits transformers and resistive pads (attenuators). These pads serve several purposes. A portion of the pad is used to provide DC biasing for the diodes. They also serve to isolate the stages from each other and to help prevent downstream amplifier byproducts from feeding back into previous amplifiers, which would cause distortion. Finally, the presence of pads allows the attenuation to be



tweaked so that the loss through the IF Filter board is about the same regardless of the loss characteristics of the various filters.

The crystal filters have various input/output impedances. The Inrad 2311 is about 400 ohms, whereas the others are 200 ohms, so an additional matching transformer is required as well as a different value pad.

The IF Filter board is designed to accommodate the filters (except the 2311) on Yaesu-compatible plug-in boards. A cutout in the bottom chassis provides access to these plug-in boards.

The Meter select bits MtrSlktA and B determine whether the S-meter or the FM receiver output is routed to the Rx Meter. Since MtrSlktB is high in FM mode, it is used as a disable control for the IF Filters. It also turns on Q9 and Q10 (IF Filters Sheets 2 and 3) in order to provide a termination on the output side. Although the FM receiver follows a separate RF path that does not involve any of the circuitry discussed so far, the IF amplifiers do remain on, and this circuit helps keep them well-behaved during FM reception.

#### *Receiver third IF, IF Notch*

The filtered signal is brought back to the Receiver board via coaxial cable and immediately fed into an NXP SA612 Gilbert Cell mixer. This active mixer has about 10-12dB of low-noise gain and low input voltage requirements on the local oscillator (LO3). However, its input and output impedance is 1800 ohms, so a step up transformer is required on the input. The output is fed into the notch filter (bottom of Sheet 5 on the Receiver) whose input impedance, set by resistors R85 and R88, is 1800 ohms. The third LO is set to 9.455MHz, so the primary mixing products are at about 18.455MHz, easily rejected by the notch filter even when turned off, and 455kHz. The notch filter consists of input differential amp consisting of Q29 and Q30. The output of Q30 is fed into a tuned circuit consisting of L17 and varactor D5. Voltages NotchV and LNotch control the capacitance of D5 to allow tuning, Depth of the notch is controlled by parallel filter consisting of C190 and C191 and the resistor stack between them. The output of the notch filter (Q36 emitter) is coupled to the IF Filter board's 455kHz crystal and/or Collins mechanical filters via step-down transformer T3. The filters further reject the 18.455MHz sum product and other secondary mixing products, passing only the 455kHz signal.

#### *AGC*

The 455kHz filtered signal is brought back to the Receiver board via coaxial cable, where the 50 ohm impedance is transformed by T8 (Receiver board, Sheet 5) to 1800 ohms to drive the main IF amplifier (U9). This is the venerable MC1350, used in IF amplifiers in radio and TV for decades. Although no longer made by Motorola, it is still available from others. This amplifier has up to 50dB of power gain, and 60dB of AGC dynamic range. The AGC input on pin 5 provides logarithmic AGC action that is linearized by Q28 and U33, acting as an anti-log amplifier so that the S-meter receives linear steps from about S7 to 45 dB over S9. S-meter accuracy below S7 gradually gets worse as it approaches S0 because the AGC range of the MC1350 is not wide enough to handle the range that would be required. S0 = -127dBm, and 45 over S9 is



–28dBm, encompassing a 99dB range!

The output of U9 is buffered by Q15 and fed to the final mixer. The emitter side of Q15 drives the AGC circuitry. As discussed earlier, Q6 provides a variable gain amplifier that is used to set the overall loop gain during receiver calibration. The output of Q6 drives a 10dB voltage gain amplifier with a frequency response optimized for 455KHz operation, whose output is rectified to produce a 0 to 76mV AGC control voltage (the cathode of D7). The output of D7 feeds a very long time constant filter (R70, C37) of about 1 second. This is the “IF-derived attack” of the AGC. Since this must drive an op-amp (U27 pin 3), the impedance must be low enough that the input offset and input bias current of the op-amp do not add a DC offset to the small AGC voltage. U27 (pins 1,2,3) multiplies the AGC voltage by 17 in a non-inverting configuration, resulting in a 0-1.3V output swing. The other half of U27 level shifts the 0-1.3V signal to 3.75-5.1V which becomes the AGC voltage that is fed into U9. U10 provides the necessary negative output that sets the differential amplifier offset. U10 receives its input from output “C” of a serially programmed D/A converter (U23, sheet 8). A calibration step involves setting this voltage so that the quiescent, no-signal AGC voltage is 3.45V.

The AGC output is level shifted back to 0.8 to 2.1V via U27 (pins 5,6,7). Since this is a logarithmic signal, it is linearized by passing it through a temperature compensated antilog amplifier consisting of U33 (pins 1,2,3), Q28 and associated parts. The output is buffered and scaled by U33 (pins 5,6,7) and fed into a CMOS switch that selects either the S-meter signal (for all modes except FM) and the FM relative signal strength output RSSI. The selected signal drives the Rx meter.

An AGCOff bit is used to short out the 0-76mV AGC control voltage, forcing the AGC voltage to stay at 3.81V and running the IF amplifier open loop at maximum gain.

For SSB mode, the AGCSlow control bit is set high, turning off Q3 and removing R77 from the circuit. This increases the time constant to about 500ms.

### *Muting and de-sense*

When operating in Full Break-in mode, in which you want to hear the receiver between dots in CW mode, it is necessary to keep the transmitter from saturating the receiver’s amplifiers so that recovery time is fast.

Keeping the transmitter out of the receiver’s input amplifiers requires shielding, which is accomplished by separating them into different compartments, and isolating them via solid state Transmit/Receive switching. But that’s not really enough. The AGC circuitry must be forced into maximum attenuation mode too. This is done by forcing the RFG DAC to maximum, thus setting the AGC to 7V whenever the PTT line is active. This is done in the firmware. However, the Sienna also has a full duplex mode, in which the Receiver is meant to be left on during transmission. This is commonly used when operating satellites. Since external transverters are often used for this, the transmit and receive frequencies are different, and there is less chance for transmitter bleed-through into the receiver. Thus, if full duplex is selected, the forced 7V AGC condition is not done.



It takes a few milliseconds for transmitter signals to make it all the way through the receiver, so an additional signal from the controller, HRFGE<sub>n</sub>, forces the AGC to maximum during transmissions, and is sequenced by the Keyer processor along with the LTxE<sub>n</sub> and HRcvE<sub>n</sub> lines. This is one thing that enables high speed QSK (full break-in) operation.

There's one other thing that must be done during non-full-duplex transmit. The receiver cannot help but pick up a little of the transmitted signal, and we do not usually want to hear that in the speakers. Therefore the audio output must be muted during transmit. This is done by Q34 (Sheet 8). The various audio outputs (from the AM detector, SSB/CW detector and FM detector) are amplified by U4 (pins 1,2,3) and fed into P-channel JFET Q34. R100 provides a load, while C127 makes the AC voltage on the gate follow the source, providing a 0V gate-source voltage that keeps the transistor turned on. As long as the HRcvE<sub>n</sub> line is high (meaning the transmitter is off), the drain of Q31 will be low, allowing the AC waveform to keep Q34 on. As soon as HRcvE<sub>n</sub> goes low (and we're not in full duplex), Q31 goes high, forcing Q34 to pinch off. The time constant formed by C127 and R102 assures that the drain-source junction pinches off slowly, which eliminates an audible click that occurs when an audio signal is switched off abruptly.

Once the audio signal makes it through Q34, it is fed to the back panel and to Line Out after being attenuated. The signal is quite strong at this point and must be attenuated so as not to overdrive a PC sound card. In addition, an output impedance of about 600 ohms is desirable. This is done via R44 and R136.

#### *Audio mixer*

Audio signals from the Receiver, Sidetone from the Controller, Line In audio from an external source are then fed into a TDA7418 parametric equalizer which allows them to be muted or equalized and routed to separate amplifiers.

#### *Volume controls*

The output of one speaker channel is buffered and level shifted by Q16 to provide an AntiVOX output that is then fed into an A/D converter in the Controller's Keyer microprocessor.

U11 is used to drive the headphones, and one additional pole of frequency rolloff is provided. The speaker audio is amplified by U18 and U19 to provide 1.5W of stereo with high drive capability. Since the speakers have good audio frequency response up to 20KHz and there's only one pole on the amplifiers, the audio response has a fair amount of treble. This helps maintain good frequency response when Line In audio is played through the speakers.

#### *FM*

FM receive is accomplished via an FM receiver chip, the NXP SA615 (Sheet 3). This chip requires a local oscillator and a wideband input signal. To accomplish this, LO3, at 9.455MHz, is split into two paths (Sheet 5). One path drives the mixer that it used for AM/CW/SSB (U5) and it is also fed into pin 4 (FMOSC) of the SA615. The input signal is fed in at 9MHz, which pro-



vides a 455KHz difference frequency on the output. This 9MHz signal is derived from the 70.455MHz first IF by routing it through a 70.7MHz low pass filter (to remove sum products from the U6 mixer), and another Gilbert cell mixer, U22, which provides 10dB of gain too. LO3, at 61.455MHz, combines with the 70.455MHz IF to provide a final difference frequency of 9MHz. The output is bandpass filtered by a 500KHz bandwidth filter and fed into the SA615.

The mixer output of the SA615 is a wideband signal at 455KHz. That signal is split into two paths by transformer T2. One side of the transformer passes this output through a low pass active filter which also adds some gain and transforms the impedance from 1800 to 50 ohms via R107 and then feeds it to the IF Output connector on the back panel. The other side of the transformer passes through a 20KHz ceramic filter and back into the SA615 for detection. A squelch input is provided by output B of DAC U23 (Sheet 8), whose level is set by the FM squelch control on the front panel. Comparator U29 compares this voltage with that of the RSSI (relative signal strength indicator) output of the SA615 to provide the squelch signal. The detected audio output is fed to the audio amplifier stages by R30 (Sheet 8).

### *Detectors*

Sheet 7 shows the AM, CW and SSB detectors. AM, CW and SSB are present at the XFO1 signal. AM is routed through diode D16 and D19 when control signal ModeAM is high. The AM signal is then given one last boost by U26 before being detected by the half-wave rectifier formed by D6. R22 and C15 filter the high mixing products out, leaving only audio. R196, R197 and D15 form a biasing circuit to bias D6 exactly at its diode voltage (about 0.6V). This allows small signals to be detected, since they do not need to overcome the diode drop.

CW and SSB signals are routed to the product detector/BFO (U7) after passing one final 20KHz ceramic bandpass filter to clean up any remaining mixing products. U7 is another Gilbert cell mixer with >10dB of gain. LO4 is set to 455KHz (+/-, depending on the pitch and/or sideband that's desired).

### *Metering*

CMOS switch U17 (Sheet 7) selects either the S-meter or the FM relative signal strength indicator (RSSI). The output of DAC U23 (TxMeter) drives the Tx analog meter. TxMeter is a calculated value and depends on the meter function that is selected (SWR, Forward Power, PA Volts, etc.).







## **Transmitter: Transmitter, TxBPF and 100W PA boards**

Refer to the block diagram on page 33 and schematics starting on page 75

The transmitter in the Sienna is completely separate from the receiver. They do not share local oscillators or bandpass filters as is the case in most transceivers. This allows the transmitter and receiver to be operated at the same time, i.e. in full duplex, a useful mode for satellite operations in particular, where you need to be able to listen to your downlinked signal while transmitting. It's also useful if you should want to transmit audio code practice on AM, or re-transmit receiver audio on a different frequency. It can also be used to monitor your transmitted signal.

### *Microphone and Line Processing*

Balanced microphones can be used with Sienna. The balanced lines are fed into U6, a precision preamp with programmable gain. The gain is set by a digital pot in U14. For most low output microphones, the default setting provides very high gain. High output mics can also be used, in which case the gain can be reduced by changing the resistance via a menu option. The preamp output and the unbalanced line input from the phono connector on the rear panel are mixed by U9 (pins 12,13,14), a precision, low distortion, rail-to-rail op-amp, to provide three outputs—one for the balanced modulator, one for the PC's line input, and one for FM and VOX detection. The VOX/FM path includes a pre-emphasis circuit, which is simply a high pass filter. FM receivers employ “de-emphasis”, or low pass filtering, which cancels out the effect of the pre-emphasis. U9 (pins 5,6,7) mix the input from the receiver board (RxLine) with the external Line In signal. This output becomes the “Line” signal.

The output of the balanced preamp goes to jumper JP12, allowing it to be tested without the load of the subsequent amplifiers, and allowing for a future audio equalizer to be inserted.

### *Line/Mic selection*

U19 is a low distortion CMOS switch that allows either the Line or Mic outputs to drive the balanced modulator. Note that for digital modes, there are two ways for the signal to get into the transmitter—via the unbalanced Line In connector on the transmitter board's phono connector, or via “RxLine”. When the internal PC is used, its sound card output appears on this line.

### *Balanced Modulator and CW keying*

The selected input is fed into the balanced modulator (U7). Pot RV1 is used in a calibration step to null the carrier in SSB modes. In AM, the balance is removed by turning on Q22, allowing the carrier to feed through. The local oscillator, TXBFO, runs at about 11.98 MHz. Thus the first IF is 11.98 MHz +/- audio frequencies.

In CW and FM modes, the LO is switched to Q21. The keying circuit (Q19, Q23) waveshapes the keying signal via low pass filter consisting of C9 and R20 and applies it to the drain of Q21. The waveshaped CW signal then appears at the source of Q21. Diodes D12 and D13 and capacitor C130 keep the RF from bleeding through to the subsequent stages when the transistor is off.



In FM mode, the key is turned on and TXBFO is frequency modulated based on the amplitude of the sampled microphone input.

### *SSB/AM filtering*

The transformer-coupled (T6) DSB signal from U7 (107A and 107B) is applied to two 7-element variable bandwidth Cohn-style crystal filters, one for SSB use, with a 2.5 kHz bandwidth, and one for AM use, with a 5 kHz bandwidth. For SSB use, the LO is shifted above or below the crystal filter's bandwidth to pick off just the desired sideband.

### *RF Speech Processor/Buffer/Drive*

The output of the SSB filter is and fed (FO1) into variable gain amplifier U20. If the processor is off, a fixed gain is used. This gain setting is adjustable in a menu option. It should be set so that the clipping diodes D1 and D2 do not appreciably clip the signal. If the RF speech processor is enabled (SSB mode only), the Processor Level pot is allowed to control the gain of the amplifier. The processor level control on the front panel (or its corresponding RS-232 control command) causes output "D" of DAC U5 (Sheet 6) to be changed from 2.5V to 3.5V as the control is moved from 0 to full scale. This changes the gain of this amplifier by up to 30dB, resulting in a strong signal that is clipped by Schottky diodes D1 and D2. Transformer T2 samples the signal level at the point at which the RF signal enters the clipper. Diode D6 rectifies it and R80 and C131 filter it to produce a DC voltage, CMPR, that is fed into a buffer op-amp (U4, Sheet 9), where it is protected against overvoltage and fed to an A/D converter on the Controller board. The clipped signal is fed into a five element crystal filter (back on Sheet 3), which removes the high order mixing products caused by the clipping. This results in an RF compression of up to 15dB. The output is fed to the drive control via a Darlington transistor, Q37, which allows the high crystal filter impedance to be matched while providing low impedance drive for the subsequent stage.

IF CW or FM are in use, the waveshaped signal CWRF is fed through a wide crystal filter to remove harmonic content and provide some additional CW waveshaping, and then through Darlington transistor buffer Q30. Q27, Q30 and Q37 cannot all be on at the same time, so the appropriate one is powered by control voltages CWFM, AM-ESSB and SSB. The resulting output of CW, FM, AM, ESSB or SSB appears at FO2 and drives another variable gain amplifier, called the Drive, providing a strong signal, MTX, for TUF-3 mixer U10.

If the processor is off, the effective filtering of the 7th order filter followed by the 5th order filter provides essentially 12th order filtering, resulting in excellent unwanted sideband and carrier suppression.

### *VFO, Bandpass filters*

The VFO is fed into TUF-3 mixer U10 (Sheet 5) along with the selected SSB, CW, AM or FM (carrier) signal. The difference product is bandpass filtered by the TXBPF board located at J13. This board is identical to the ones used on the RXBPF board for the receiver discussed earlier. The only difference is that the TXBPF board selects the band based on 4 bits of band data from



U1 (Sheet 8). This band data is compatible with that used by Yaesu's linear amplifiers. The TXBPF board also has an 11.98MHz notch filter on it to reject any remnants of the local oscillator.

### *Voltage Controlled Amplifier, ALC*

The bandpass filtered signal from J13 is next fed into another NXP SA603 voltage controlled amplifier (U8). The FGAIN (fixed gain drive) control voltage (Sheet 6) provides the 3.9V to 4.9V required to change the gain of this amplifier over a 30dB range.

K13 (Sheet 9) selects either the internal 0-4.1V ALC control voltage from output A of DAC U5 (Sheet 6) or an external ALC voltage from an external amplifier. The 0 to -4.1V voltage provided by most amplifiers is inverted first by U11 (Pins 5,6,7). The selected ALC voltage is then passed through differential amplifier U11 (pins 1,2,3) where it is conditioned, resulting in the 3.9V to 4.9V control voltage for U17. This amplifier (U17) along with the drive amplifier (U8) and the RF Proc amplifier (U20) are the sole sources of adjustable transmitter power gain.

### *Driver*

The 1mW output of U8 is amplified by U23 by about 22 and then transformer coupled to the power amps. Sheet 6 shows the power amplifier stages. Q3 amplifies the signal up to 1 Watt, which is then coupled into the paralleled final amplifiers consisting of Q4 and Q5. Q4 and Q5's bias point is changed from Class B (for CW and FM modes) to Class AB for SSB and AM modes. This is done by Q6 and Q12, "Class" (U2 pin 12) is the control bit that turns Q8 on and off. When the transmitter is off (output of Q16, HTxEn, low), Q13 is off, so TXPVCC is at a low voltage that is insufficient to bias Q3, keeping any low level RF from feeding through. When Q13 turns on (TXPVCC = 8.4V), Q3 receives bias, allowing the RF to pass to the finals.

### *10 Watt PA*

The 1W output of the driver is fed into Q4 and Q5, which are out of phase with each other by 180 degrees thanks to toroid transformer T3. The outputs are recombined by T5 to produce the final 10 Watt output signal. Transformer T4 serves as the DC collector inductor for both transistors. A portion of the output signal is sampled by one-turn windings on the secondary of T5 and fed back to the inputs to provide some automatic level control.

A protection circuit consisting of U13 and Q26 guarantees that if anything—static charges, glitches, software errors, etc.—removes drive from any of the relays that connect the 10W output to the low pass filters, the TXPVCC signal that enables the transmitter will be removed. Since the relays take up to 15 ms to switch, the solid state circuitry causes the RF drive to be removed before the relays actually open. This protects the finals from the high voltage flyback pulse generated by T5 when its load is removed.



### *T/R switch and low pass filters*

The 10W output from T5 is fed into one of five low pass filters shown on Sheet 7. If the 100W amplifier is not installed, the bandpass filters are also tapped at the 10W signal point and fed through a transmit/receive PIN diode switch network consisting of diodes D3 and D7, chokes RFC1 and RFC2, and output coupling capacitors C80 and C113. Resistors R40 and R42 bias the PIN diodes at half the supply voltage when enabled by Q1. The low pass filtered receive signal is then passed to the RXBPF board's "Main Antenna" input. Of course, if the rig is used in full duplex mode, this path cannot be used and the receive antenna input is automatically selected to avoid feeding high power RF into the receiver.

The low pass filters are 7-element Elliptical LC filters.

Control logic is shown on Sheet 8 and consists of 8-bit registers that produce the control bits already discussed.

### *100W amplifier*

If the 100W amplifier is installed, the T/R switching is done on this board instead of the transmitter, so the RF cable going to the BPF board is removed from the transmitter (J8) and reconnected to the 100W amp (J6). Similarly, the transmitter output is re-routed from J5 on the DCD/Tuner board to the 10W RF input (J5) on the 100W amp, and the antenna output of the 100W amp (J2) is routed to the DCD/Tuner board's antenna jack (J4).

### *Fan control*

Sheet 1 shows decoding logic, fan control and the high power supply switching. A voltage divider consisting of thermistor TH1, which touches the heatsink, and R28 produces a nominal (cool heatsink) voltage of about 1.09V. The reference input to the comparator is set to 2.88V. As the heatsink gets hot, the thermistor's resistance goes down, increasing the voltage. Capacitor C69 stabilizes the voltage. Once the voltage rises to 2.88V, the comparator's output turns off (open), and current then flows through R31 and the base-emitter junction of Q10, turning on Q10. This shorts out R32 and causes maximum current to flow through the two fans. Resistors R29 and R30 provide hysteresis, which keeps the comparator from oscillating at the trip point. When the fans and/or lack of transmitting reduces the temperature enough, the comparator trips the other direction and restores the fans to idle (low speed).

### *T/R switching*

Unregulated DC input voltage at J5 pins 3, 4 and 5 provides the high current to the final amplifier transistors, and this voltage is not switched. It is present at all times. The amplifier's T/R switch is switched via signal TXPVCC.



### *Amp bypass*

Sheet 2 is the heart of the 100W amplifier. A 10 Watt input signal can either be fed to the amplifier or it can be switched directly to the T/R switch via relays K1 and K2. If the amp is bypassed, the BON signal (derived from the PAON bit before the relay driver on Sheet 1) will stay low, assuring that the amplifier is biased off by U3/Q7. When the amp is enabled, PAON goes high, switching the 10W input signal to the 100W amp and making BON go high, which enables the bias circuit and sets the amplifier for Class B operation. This provides more efficiency than a Class AB amplifier, allowing for higher power out. Class C is usually used in CW modes, but the conservatively rated parts can easily operate in Class B while still providing over 100W out.

### *Drive reduction at higher frequencies*

R17, R18 and C9 form an equalization network to reduce the drive requirement on higher bands. T1 couples the signal into the amplifier.

### *Final current measurement*

U3, R19, R20, Q5 and R21 form a current measurement circuit. When current flows through sense resistor R19, a small voltage is developed across it. Since it is a .005 ohm resistor, a 20A current would result in a 100mV drop. This is small enough not to impact the voltage delivered to the final transistors. The higher voltage side of R19 also appears at R20. Op-amp U3 sees the lower voltage on pin 2, and since an input at the negative terminal also appears at the positive terminal while also providing a high impedance load, the net effect is to mirror the voltage of the sense resistor across R20. Using the previous example, 100mV across the 100 ohm R20 causes 1mA to flow through it. Since the op-amp's + input is also high impedance, that same current must flow through Q5, developing a voltage across R21. (There's also base-emitter current flowing through R21, but it is equal to the collector current divided by the beta of the transistor, and thus can be ignored). 1mA through the 3.16K R21 is 3.16V. Thus, a 20A current flowing to the final transistors is converted to 3.16V for measurement by the microprocessor. The output of Q5 is fed into a series resistor and 5.1V Zener diode to keep the voltage going to the microprocessor from spiking above the microprocessor's rating.

### *The amplifier*

The amplifier transistors are operated in push-pull. A positive swing on the AC input signal on the secondary of T1 is amplified by Q8 but not by Q9. When the AC waveform goes negative, the situation is reversed and Q9 amplifies while Q8 is off. The two halves of the signal are re-assembled by transformer T2. The center tap of T2, which is at AC ground by virtue of C6 and C25, feeds the DC supply to the collectors. T2 has a 4:1 turns ratio, so the approximately 24Vp-p maximum swing on the primary appears as 96Vp-p on the secondary. Since transformers do not affect power transfer appreciably (except for some minor losses), the 100Wrms signal that is developed by the primary ( $24V_{p-p} = 8.5V_{rms}$ ;  $8.5V * 20A = 170W$  input power; the efficiency is about 60%, which results in about 100Wrms) is also seen at the secondary. With a secondary voltage of 96Vp-p (34Vrms), and with a power level of 100W, the AC current flowing in



the secondary is thus about 3 Amps rms.

#### *T/R switch*

When the LTxEEn signal is active, the TXPVCC voltage is enabled, and current flows through R23, RFC5, D3, RFC6 and R24, biasing D3 at about 6V and allowing the AC waveform to pass through it via PIN diode action. D3 is large to be able to handle the high AC current. When the amplifier is not transmitting, the signal appearing at the antenna input is routed through the low-pass filters to the receiver (C21, D5, D13 and C22 on Sheet 4). Since this path must be disabled during transmit, and since high voltage appears at the Xcv point, a circuit consisting of U4 and surrounding parts creates a low current, 100V backbias voltage that keeps D5 and D13 turned off. When PTT is removed, Q1 turns off the backbias circuit and Q2 quickly shunts the voltage to ground, which also allows the normal diode biasing to work, turning on PIN diodes D5 and D13 and passing the signal to the receiver. In order to enable high speed QSK, this solid state T/R switching occurs within 1ms of removal of the PTT signal.

#### *Low pass filters*

The Xcv output signal is then routed to the low pass filters consisting of L1-L12, K4-K13, and the silver mica capacitors. Control signals from U1 and U2 select one bank of these filters depending on band. The output of the filters is fed to the antenna output.

#### *Amp enable*

When the rig is placed in “power save” mode, it is undesirable for any accidental transmitter enable signal to turn on the transmitter and amp. The amplifier uses one control bit to drive Q12, which keeps the TXPVCC signal from going high.







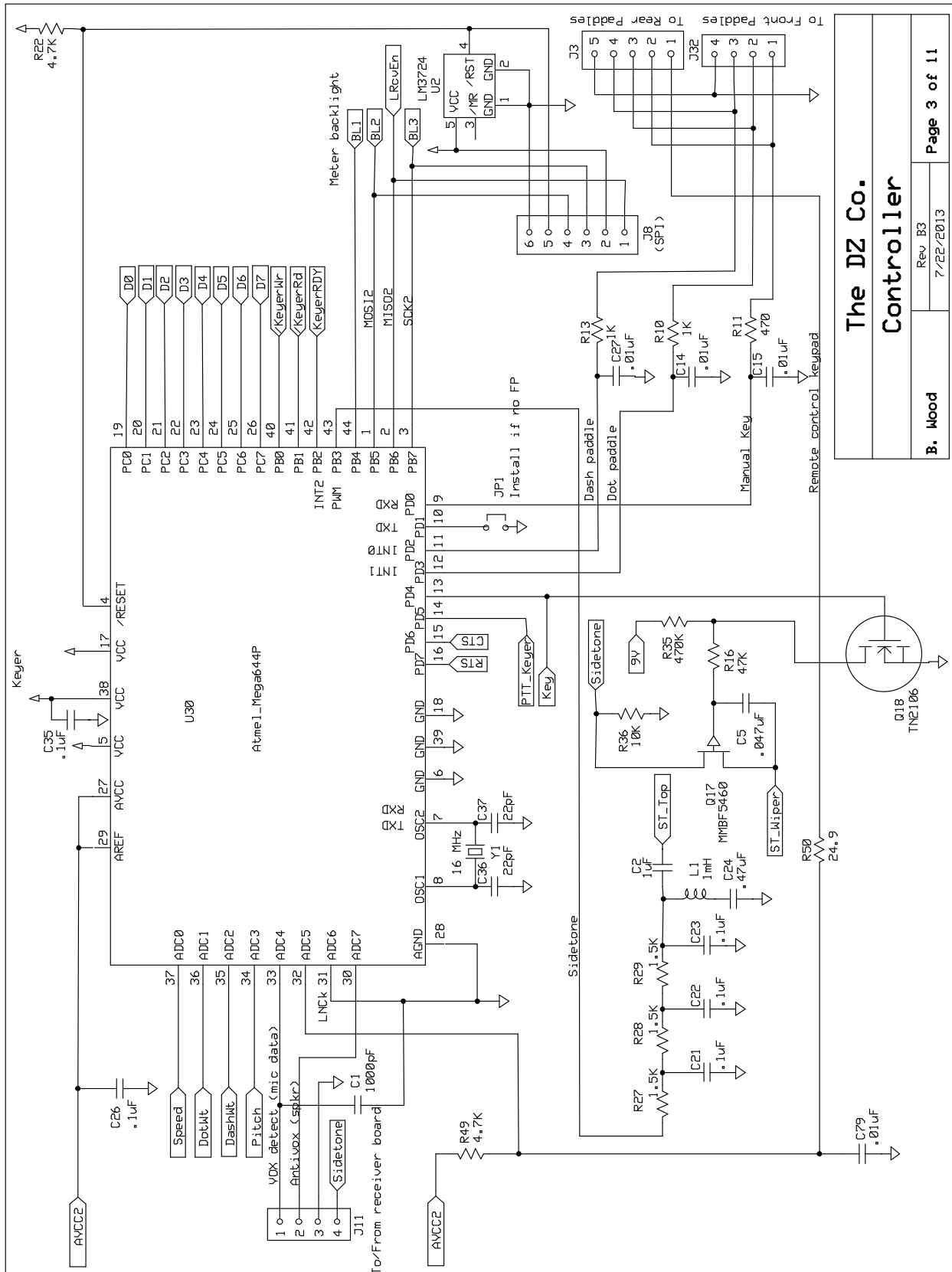
Insert block diagram page here



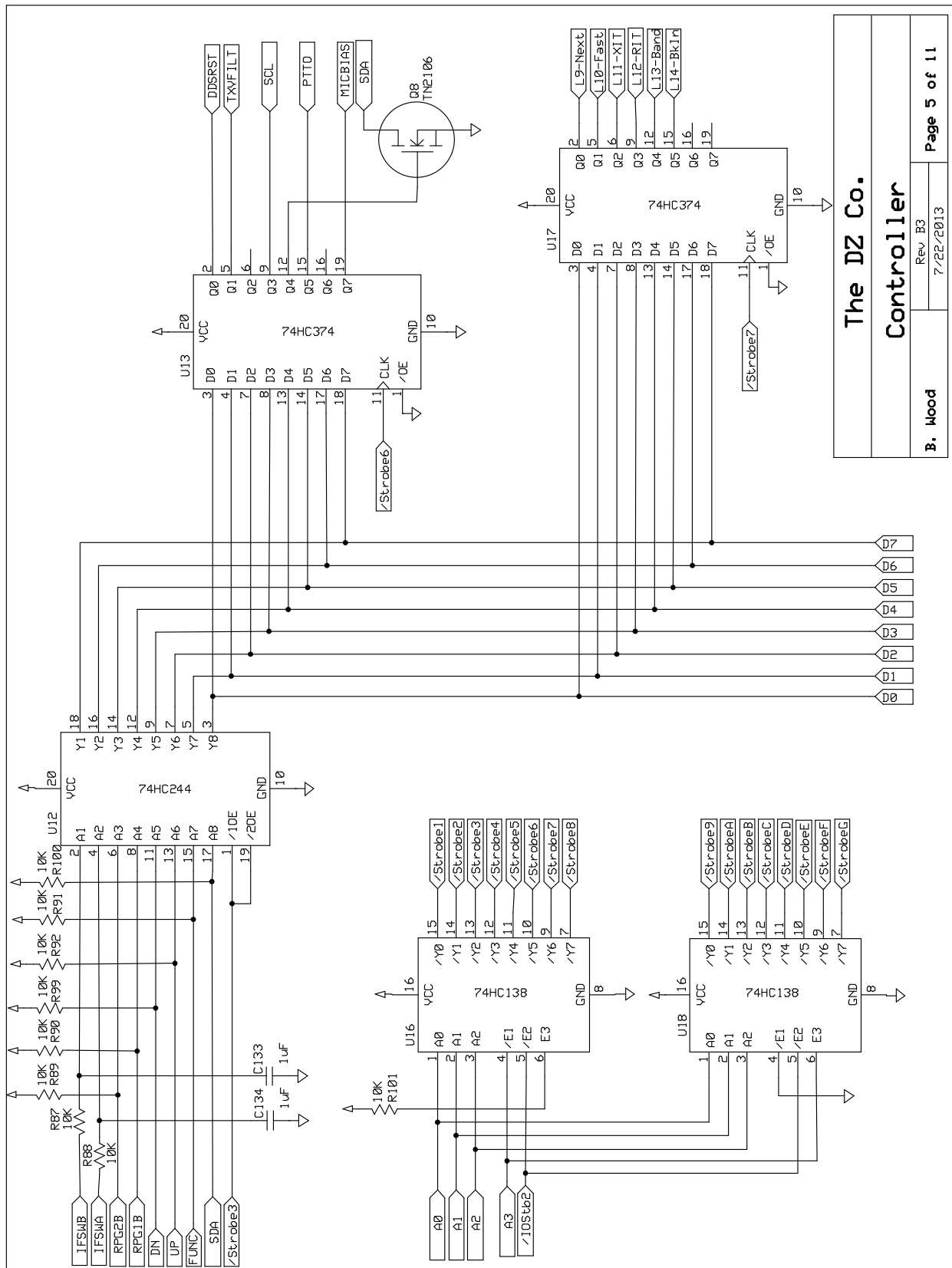
# Schematics



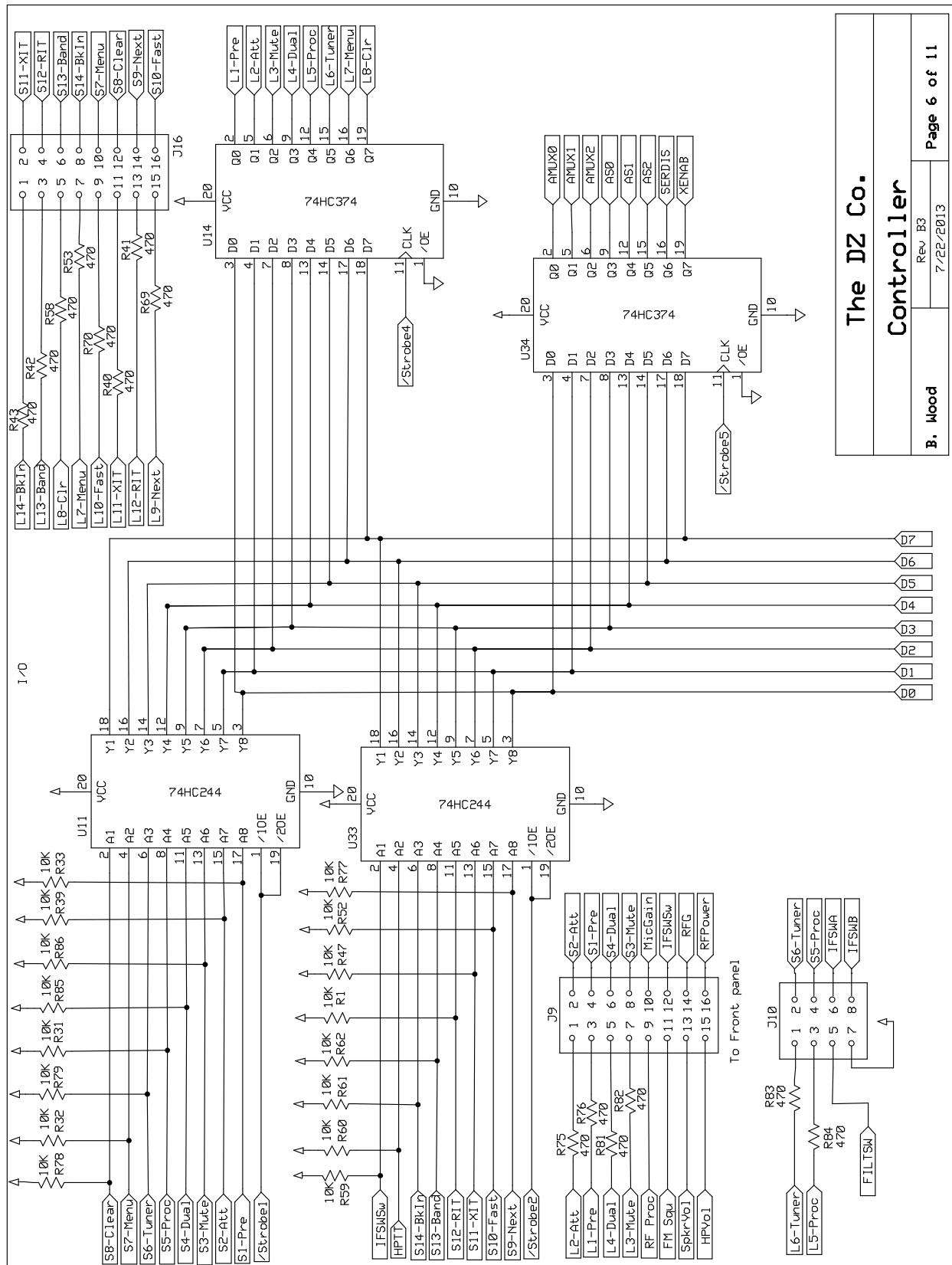






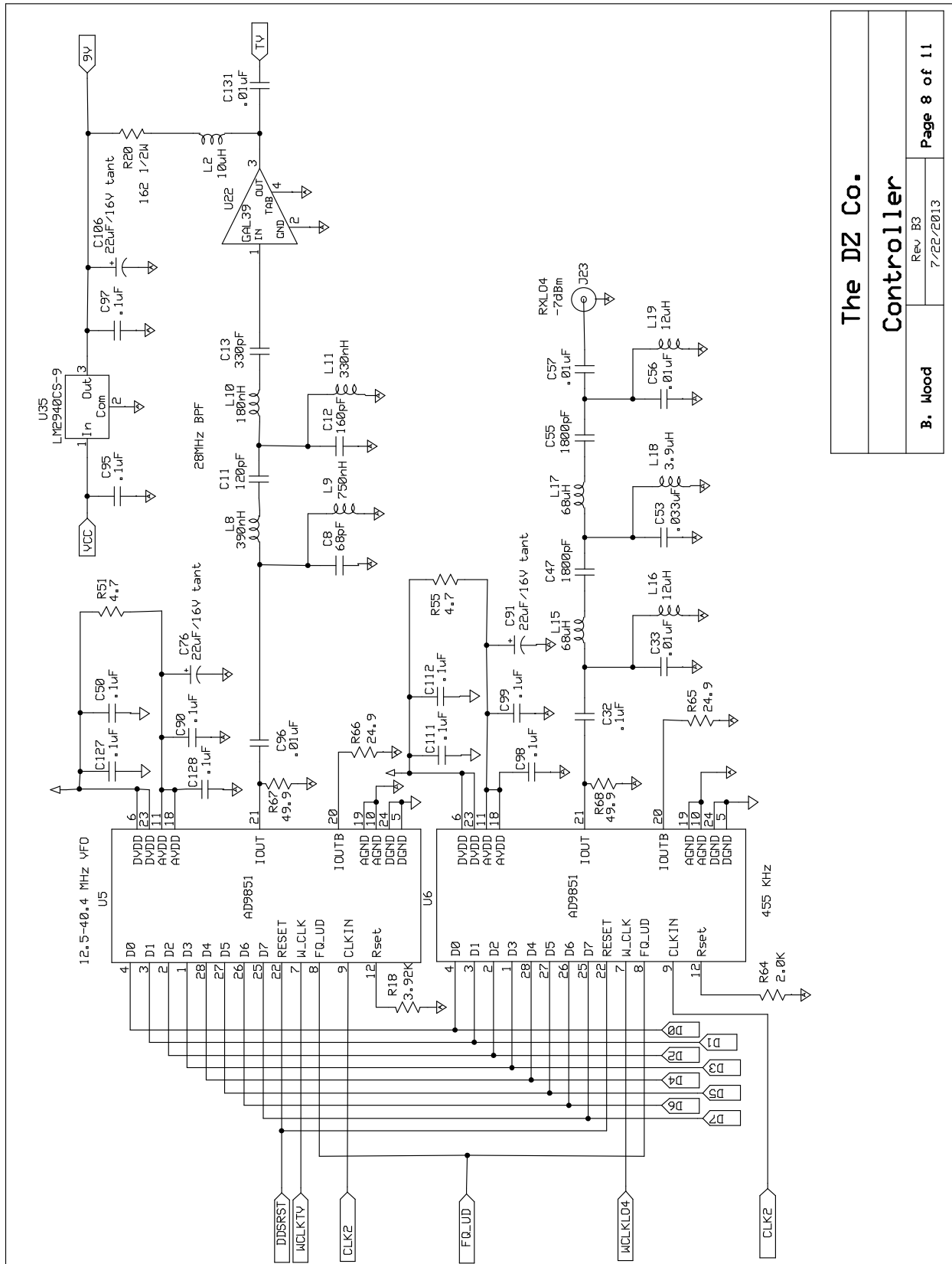


<b>The DZ Co.</b>		Rev. B3
		7/22/2013
<b>B. Hood</b>	<b>Page 5 of 11</b>	



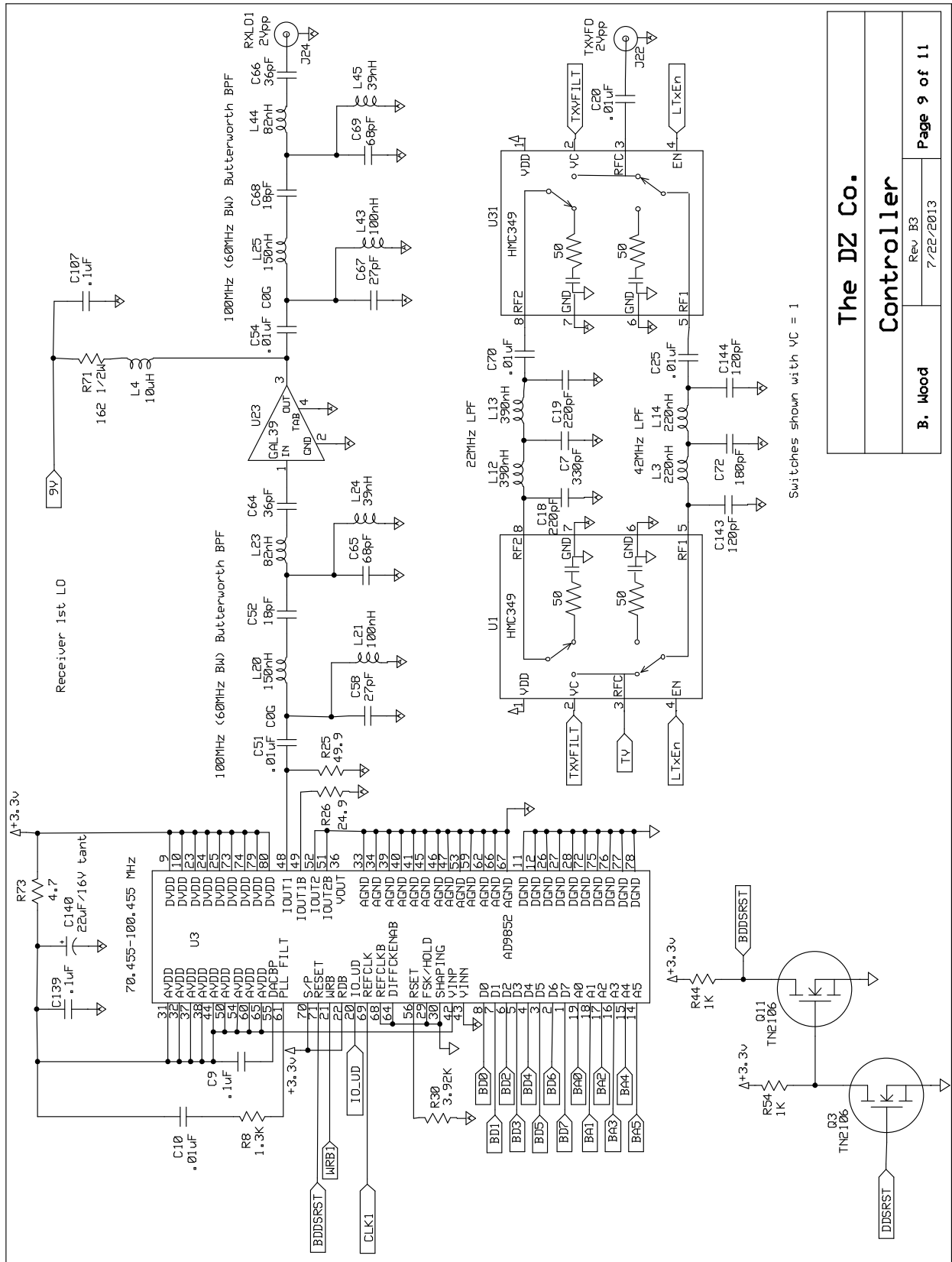






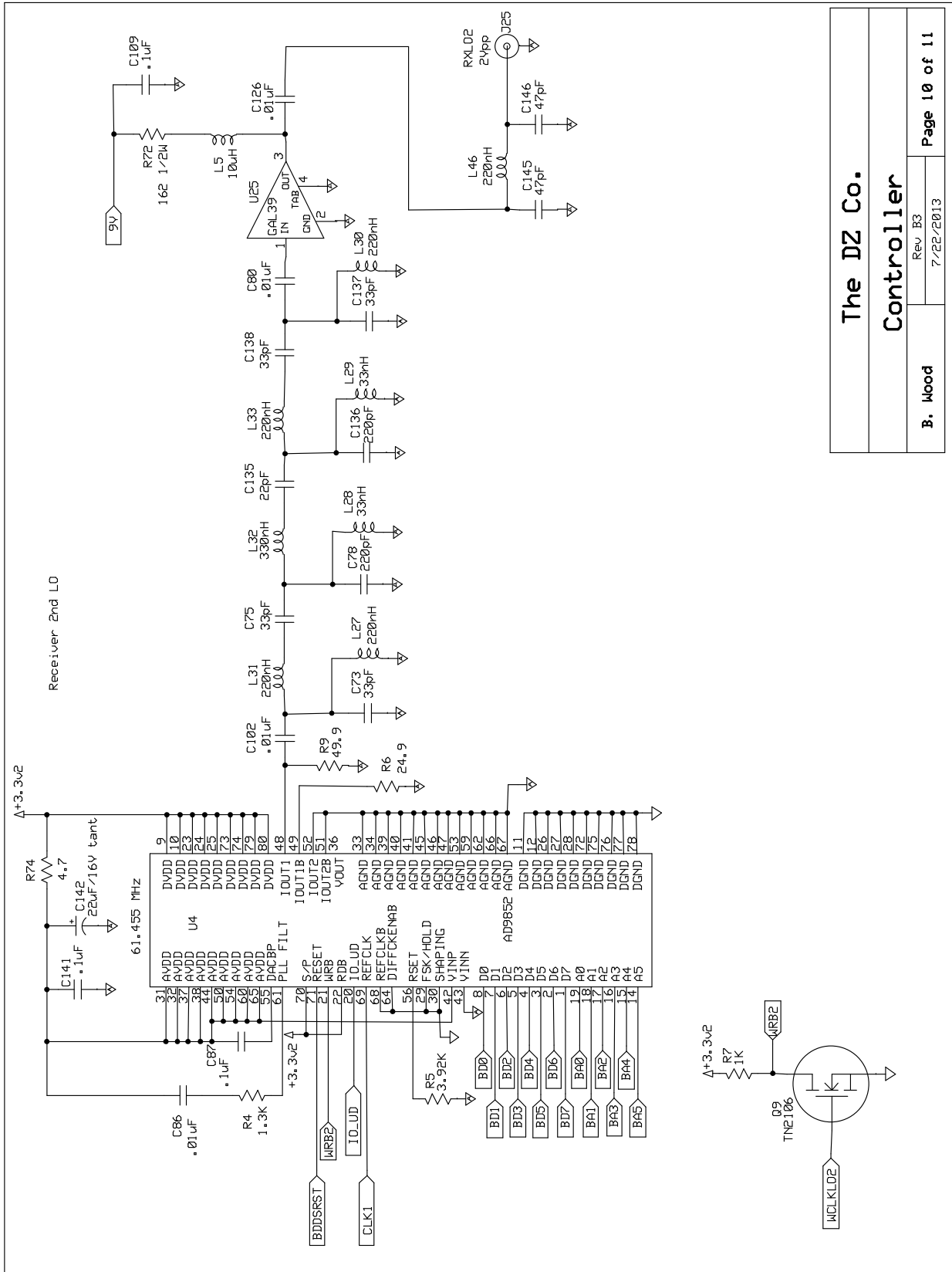
The DZ Co.  
Controller

B. Wood Rev B3 7/22/2013 Page 8 of 11



Switches shown with VC = 1

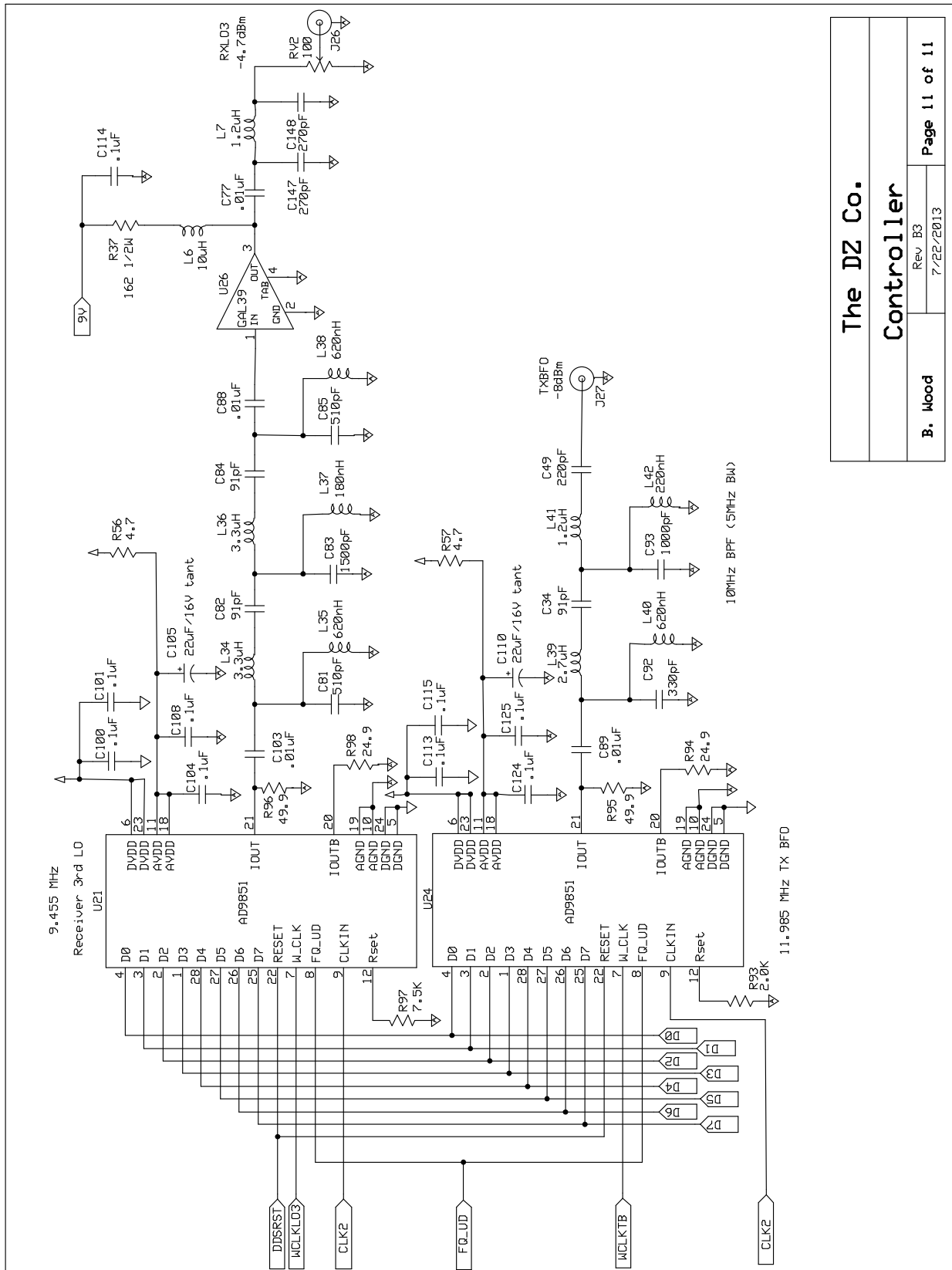
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<b>Controller</b>	
<b>B. Wood</b>	Rev B3 7/22/2013
<b>Page 9 of 11</b>	



The DZ Co.  
Controller

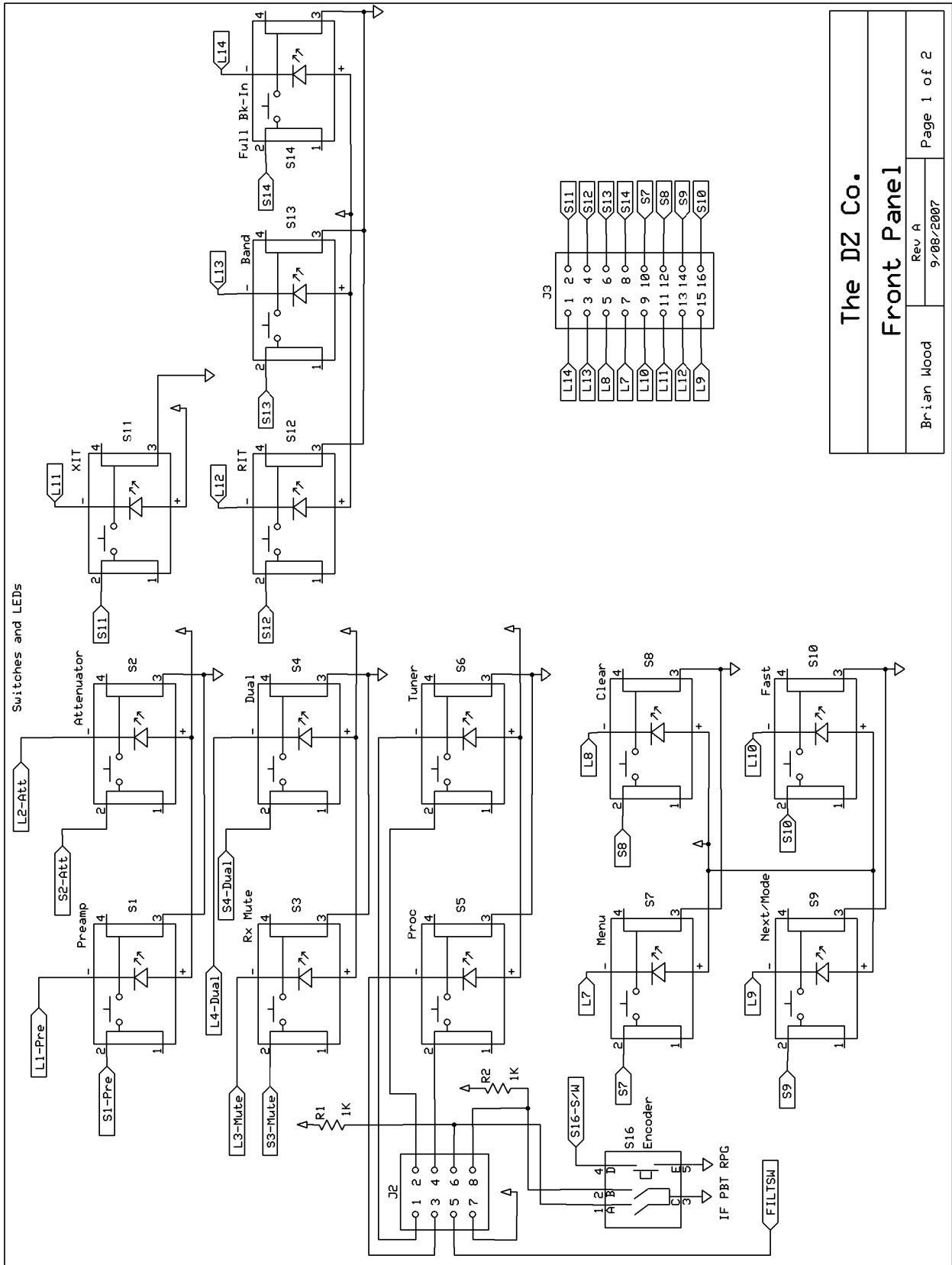
B. Wood	Rev B3 7/22/2013
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Page 10 of 11

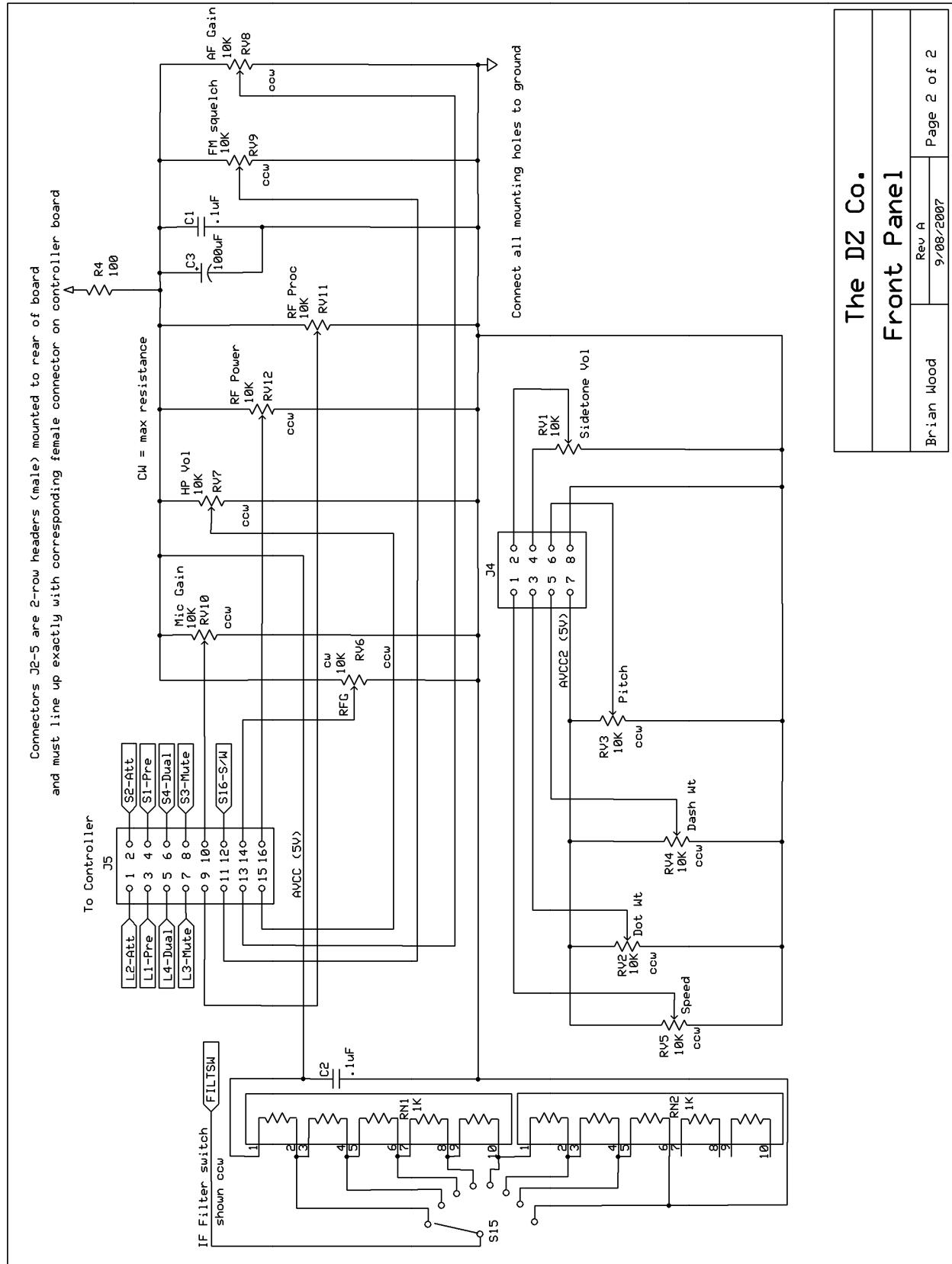


<b>The DZ Co.</b>	
<b>Controller</b>	
Rev B3	Page 11 of 11
7/22/2013	

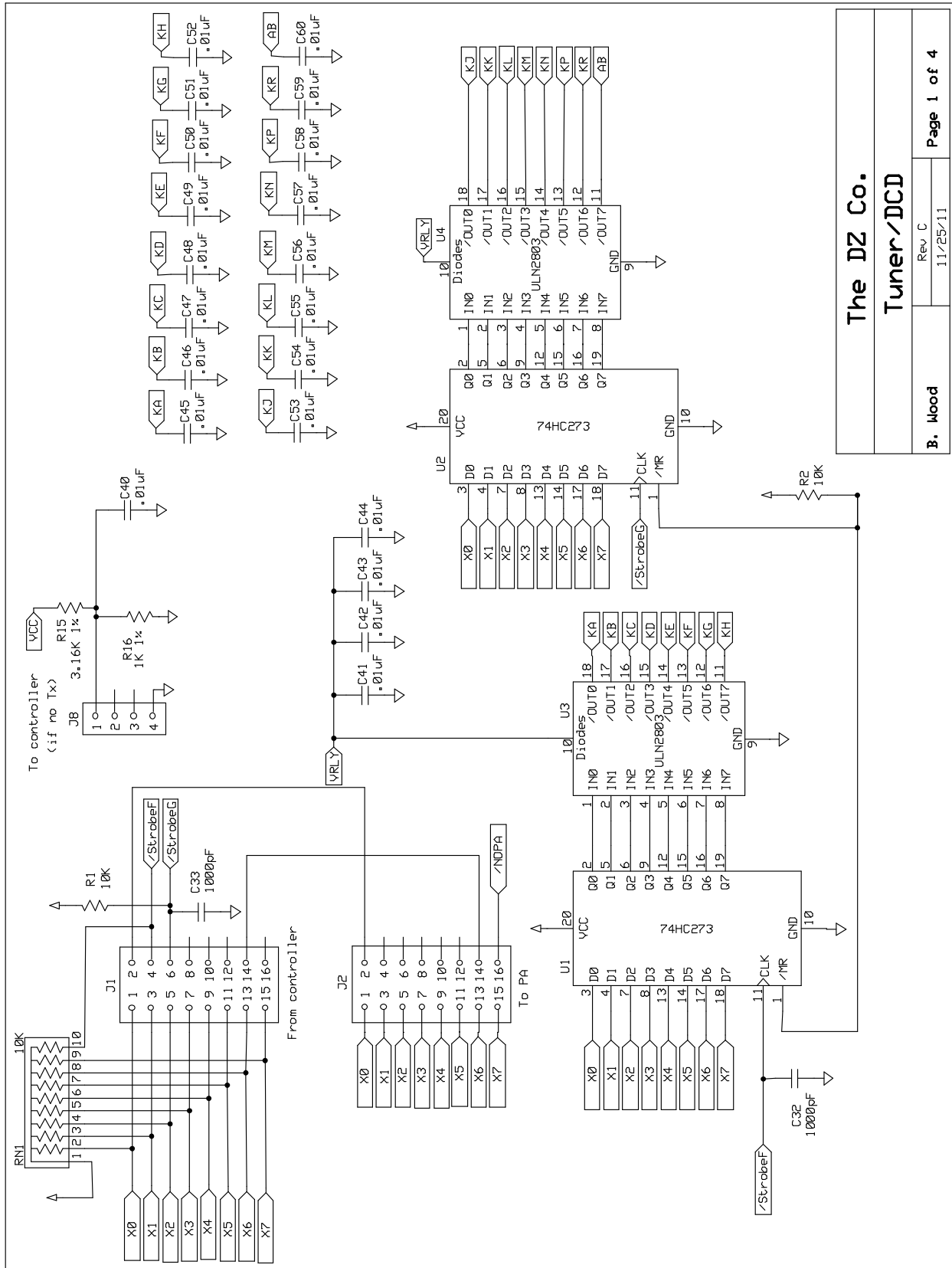
**B. Hood**



The DZ Co.  
Front Panel  
Rev A  
9/08/2007  
Page 1 of 2  
Brian Wood



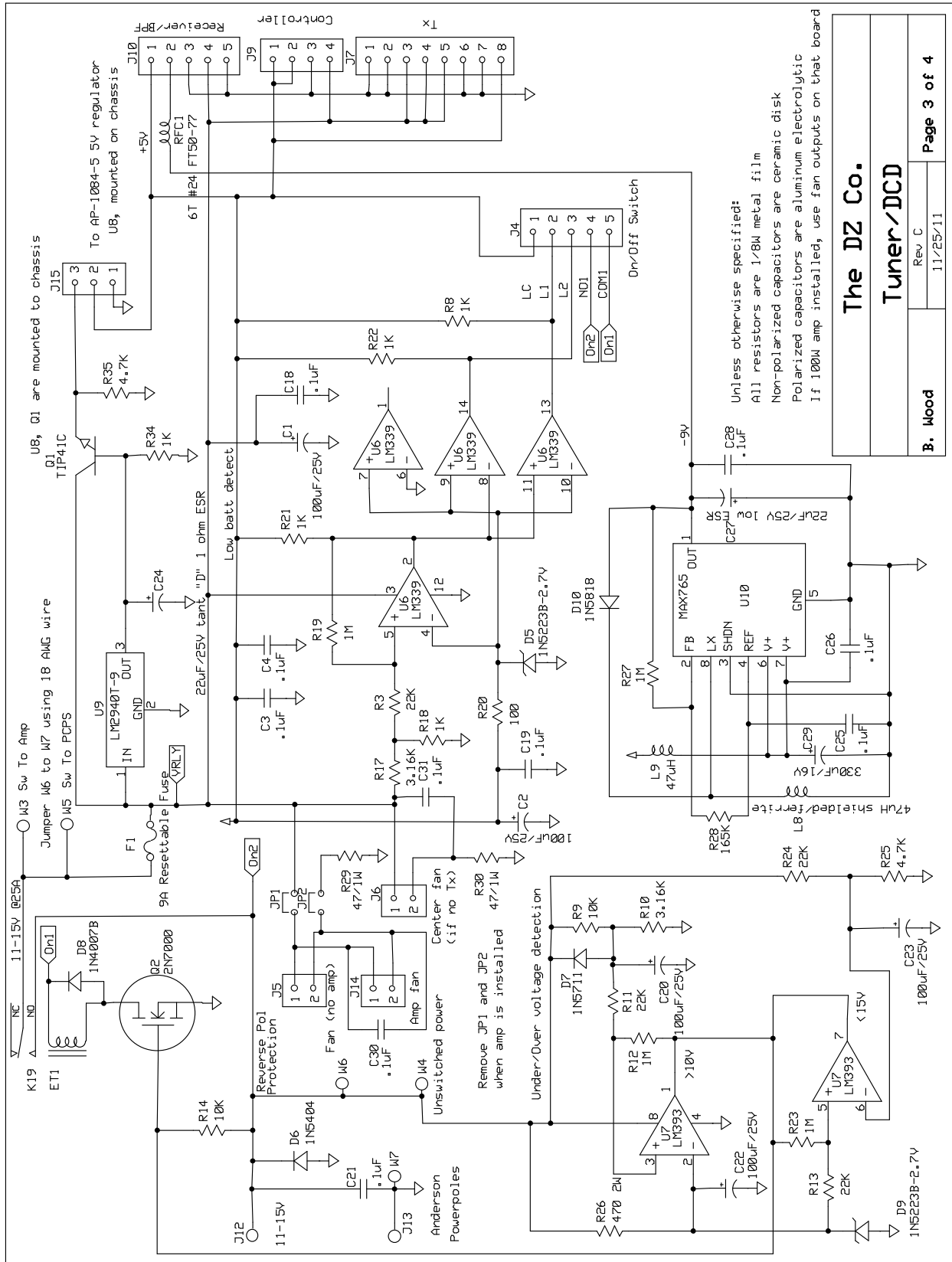
The DZ Co. Front Panel		Rev A
		9/08/2007
Brian Wood		Page 2 of 2

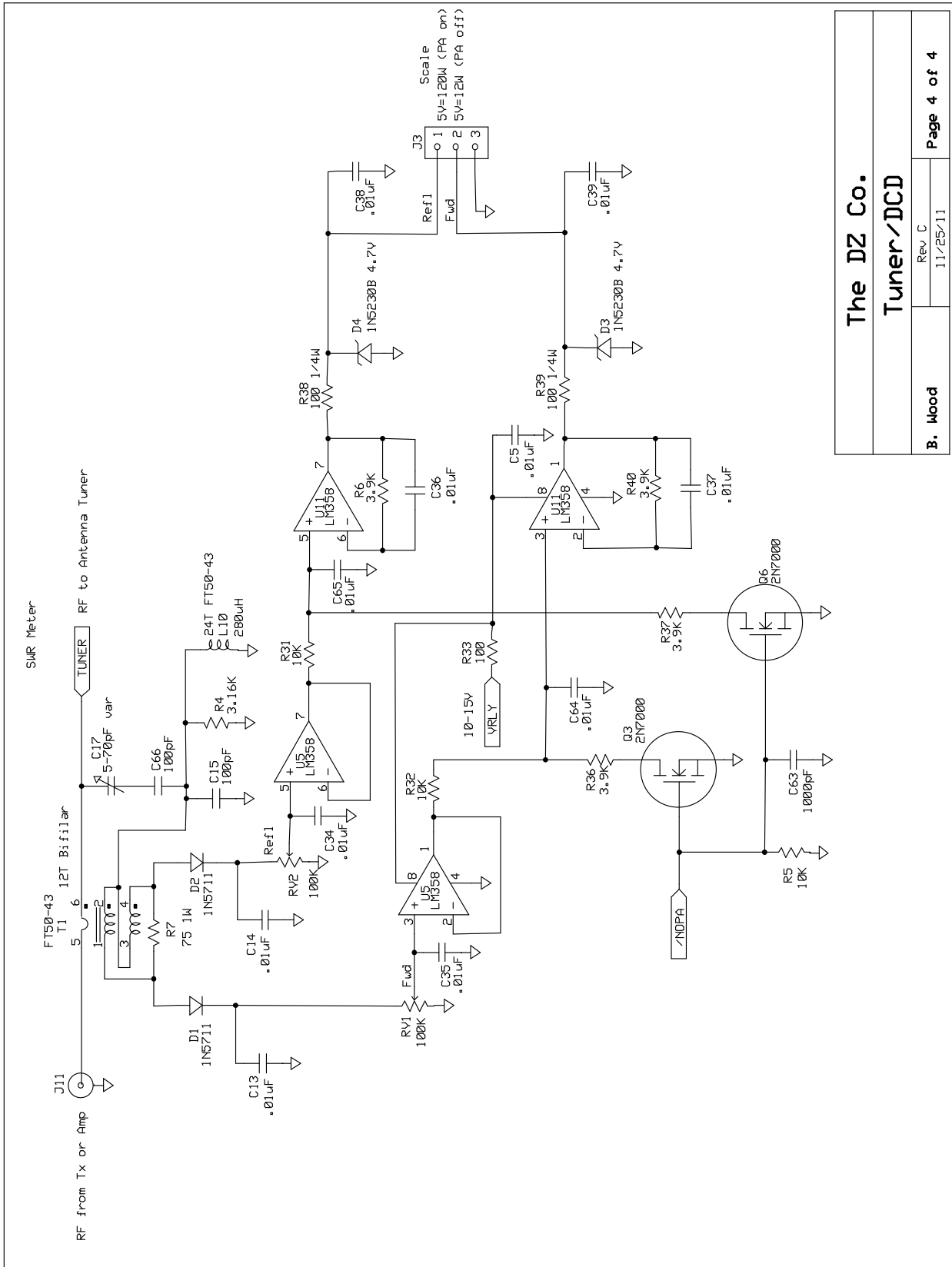


The DZ Co.  
Tuner/DCD  
Rev. C  
11/25/11  
B. Wood  
Page 1 of 4







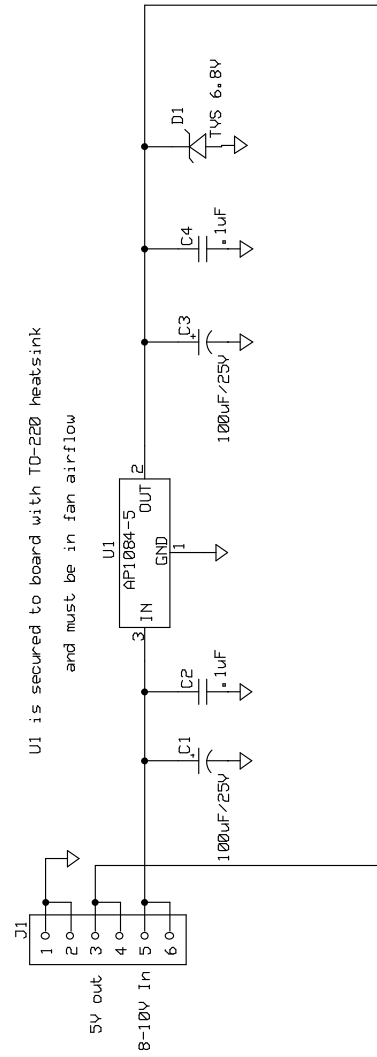


The DZ Co.  
Tuner/DCD

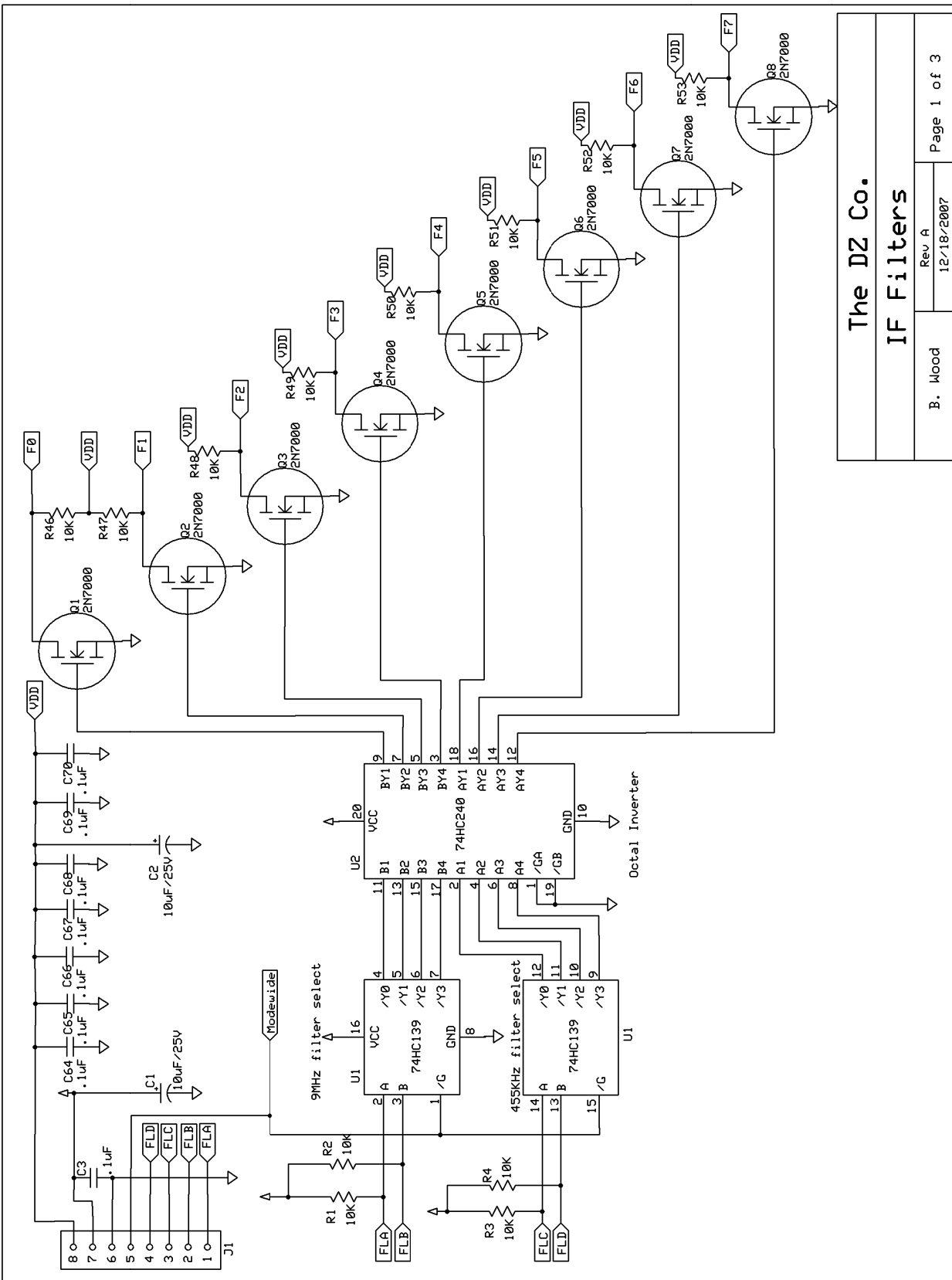
Rev. C  
11/25/11

B. Hood

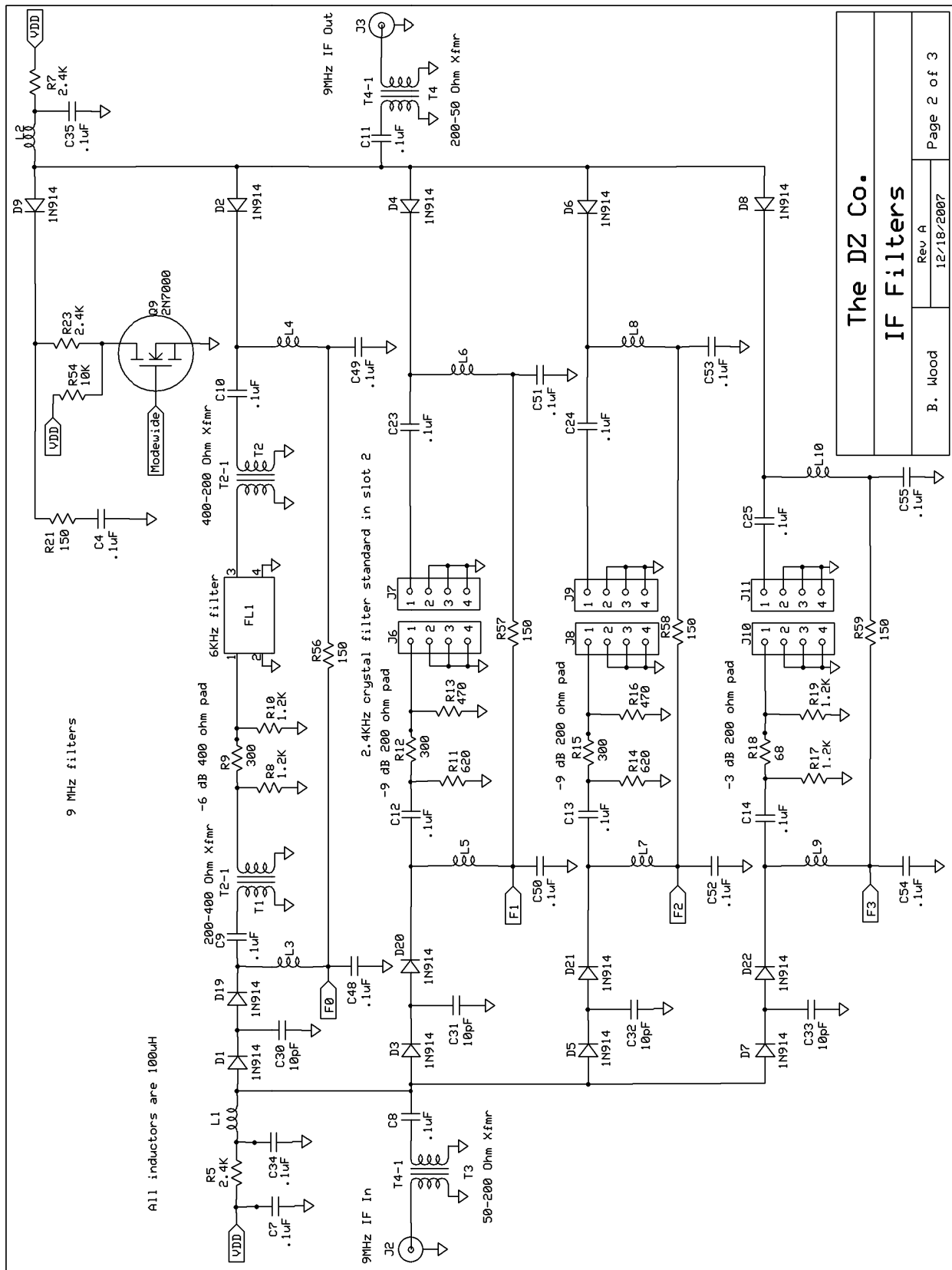
Page 4 of 4

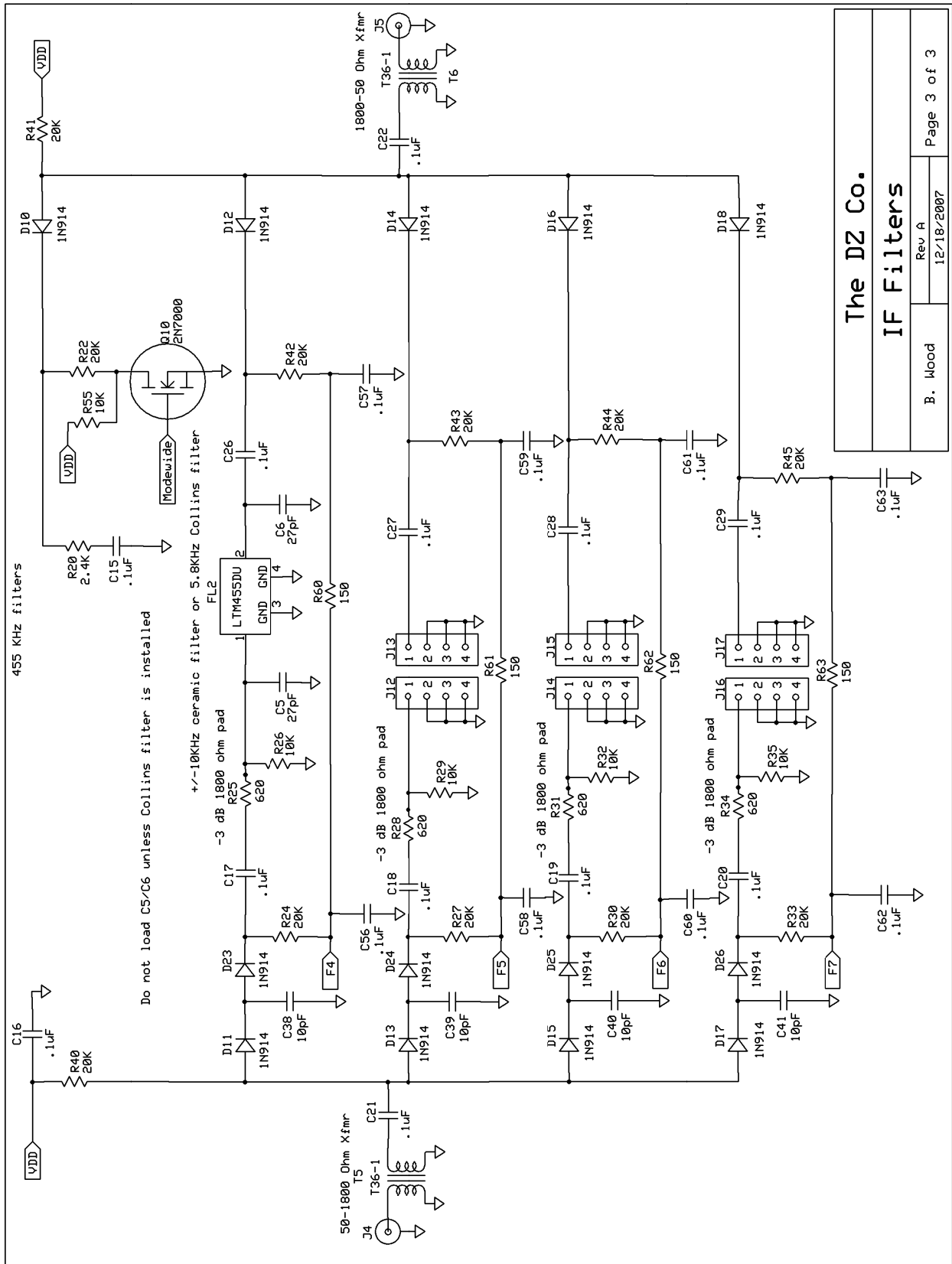


<b>The DZ Company, LLC</b>	
<b>5V regulator</b>	
Rev A	Page 1 of 1
7/31/2013	
<b>B. Wood</b>	



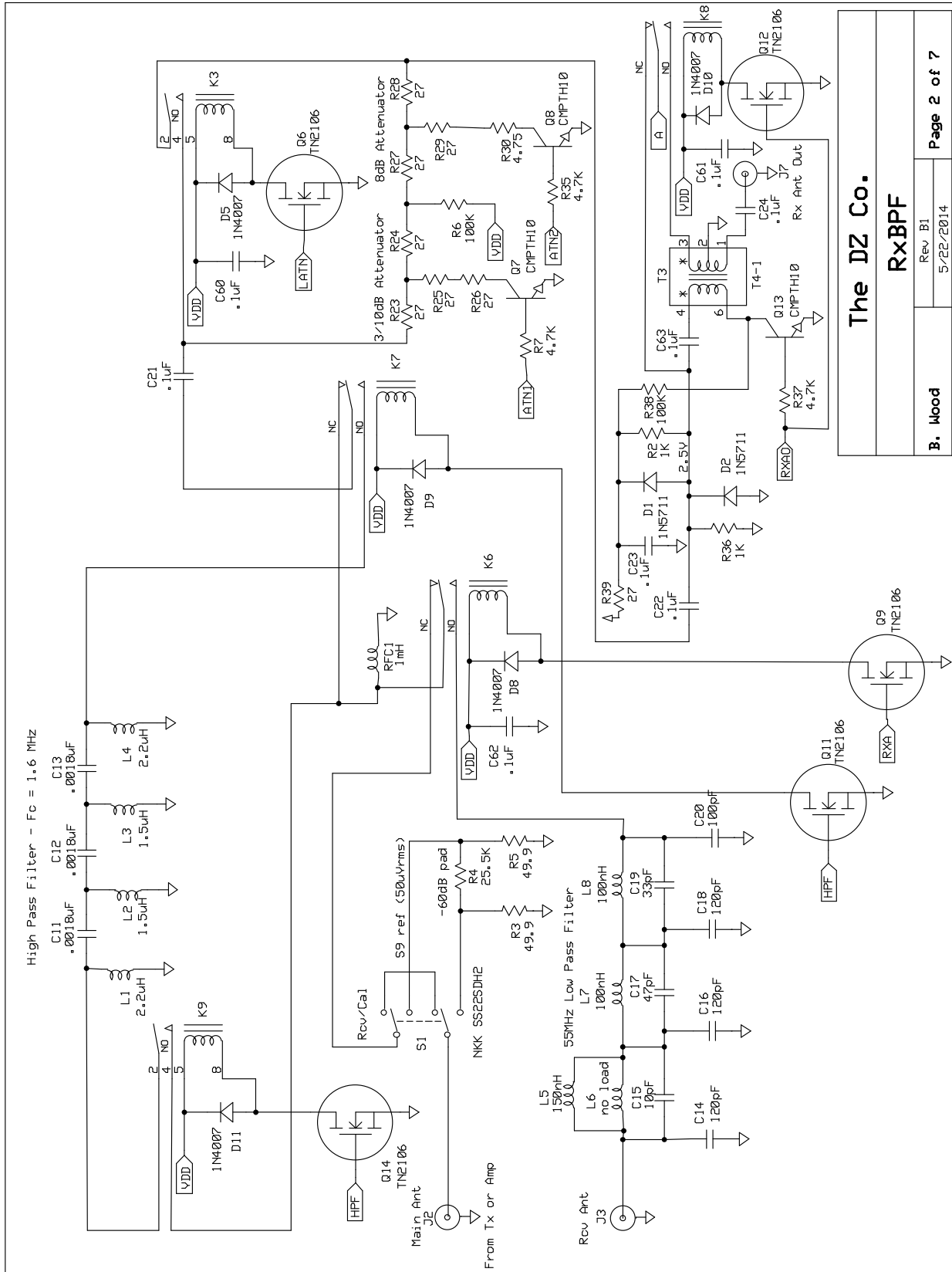
The DZ Co.  
IF Filters  
B. Hood  
Rev A  
12/18/2007  
Page 1 of 3





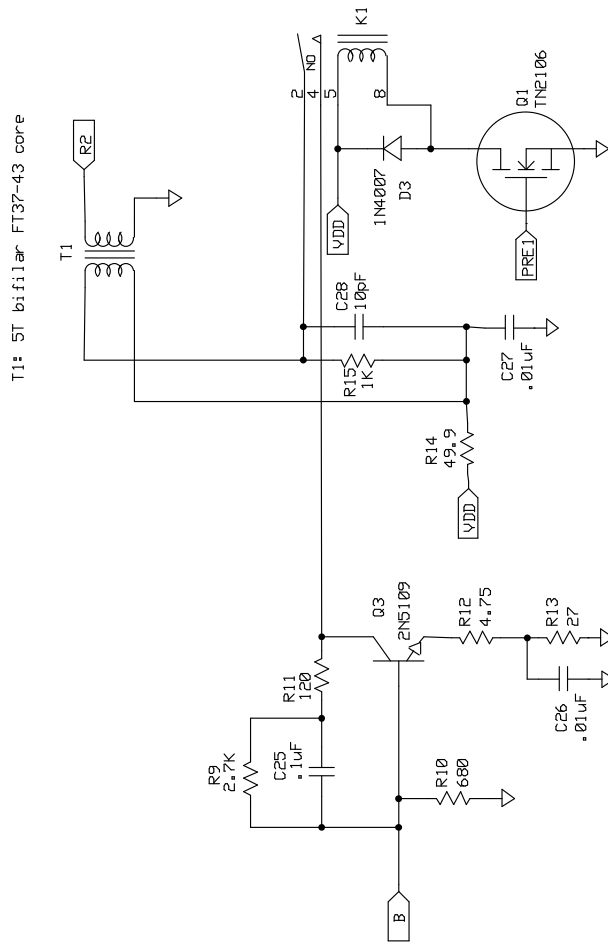




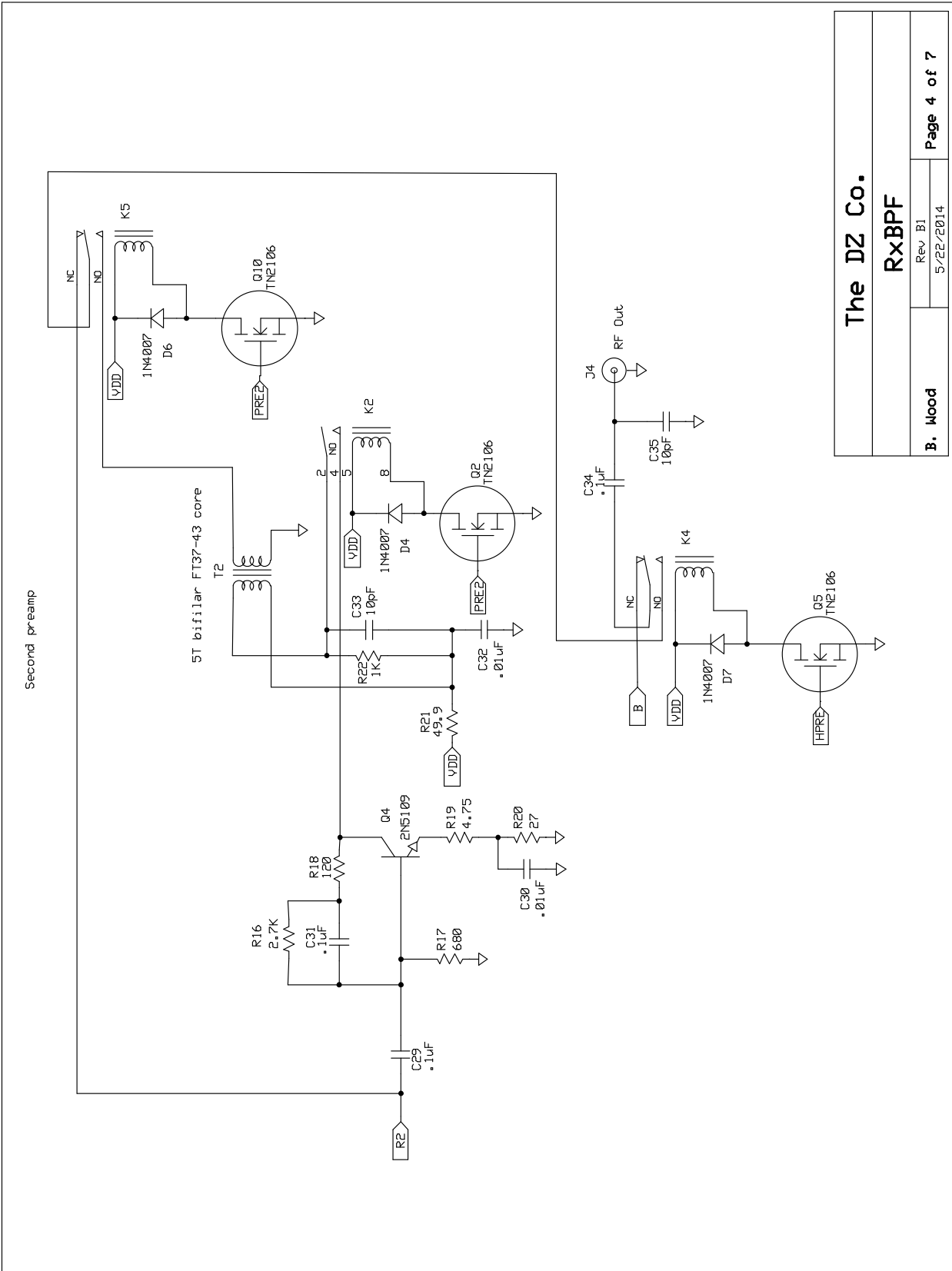




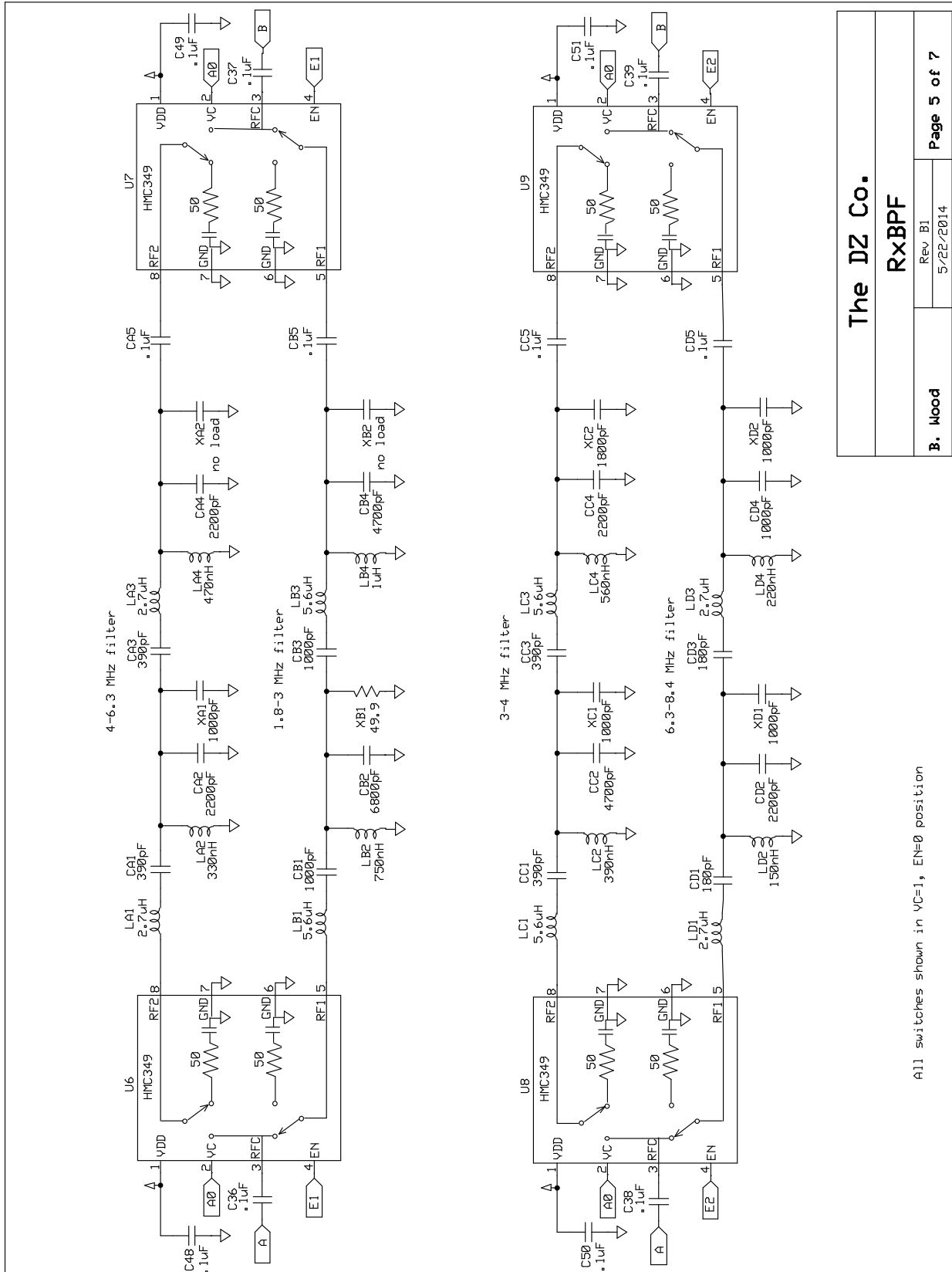
First preamp



The DZ Co.	
RxBPF	
B. blood	Rev. B1 5/22/2014
Page 3 of 7	

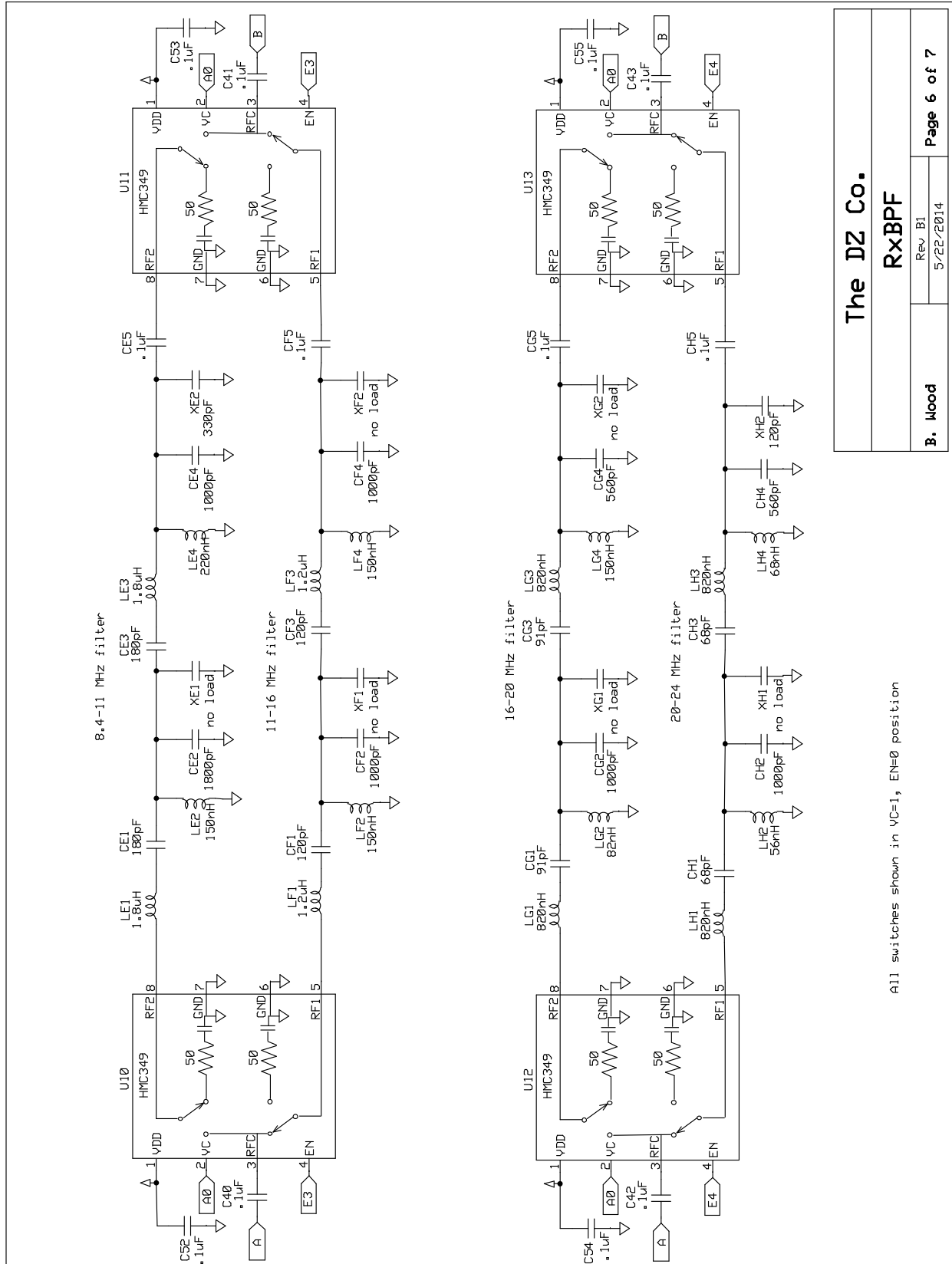


The DZ Co.  
RxBPF  
Rev. B1  
5/22/2014  
B. Mood  
Page 4 of 7



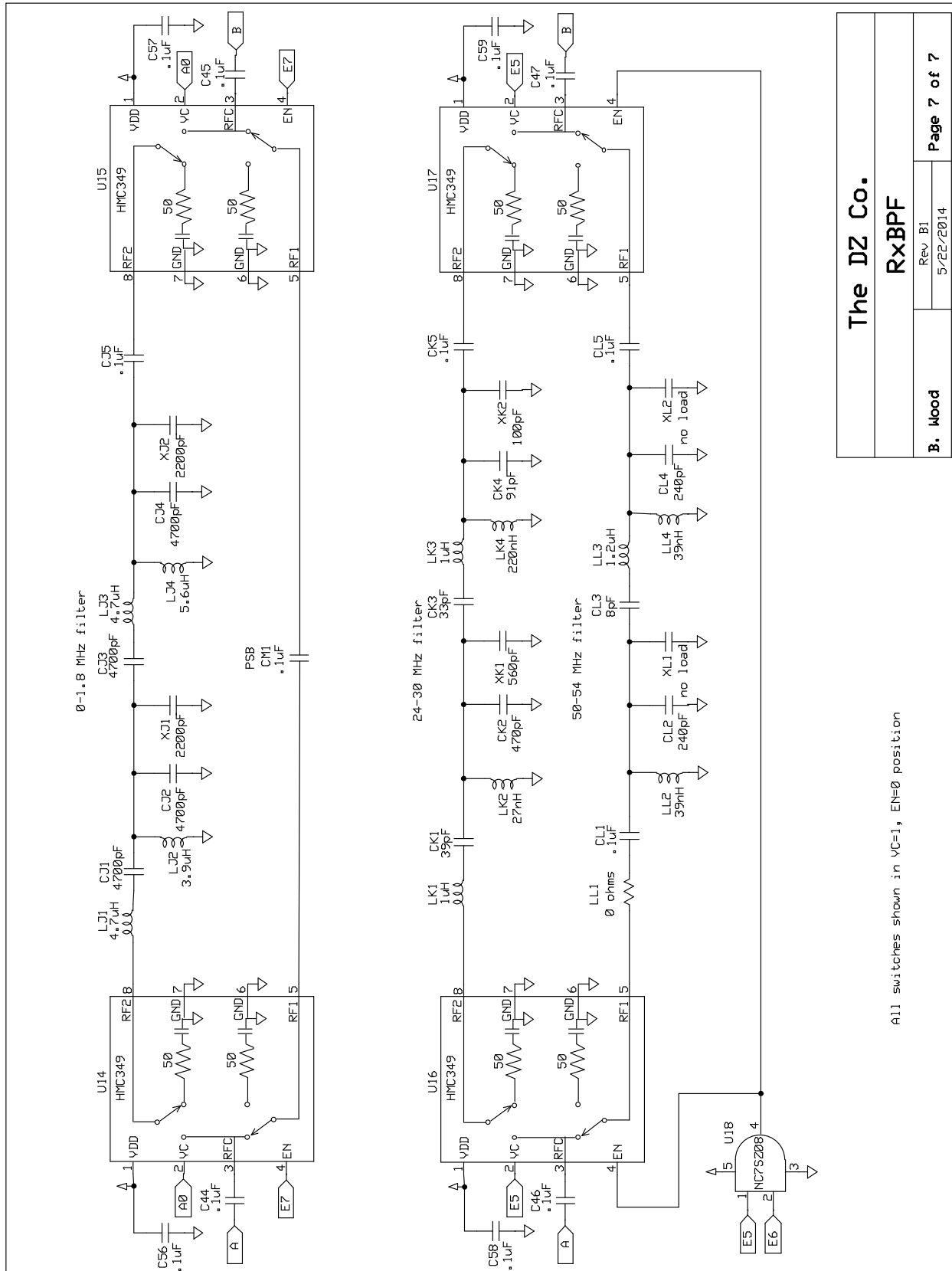
All switches shown in VC=1, EN=0 position

The DZ Co.		Rev B1	
		5/22/2014	
B. Hood		Page 5 of 7	



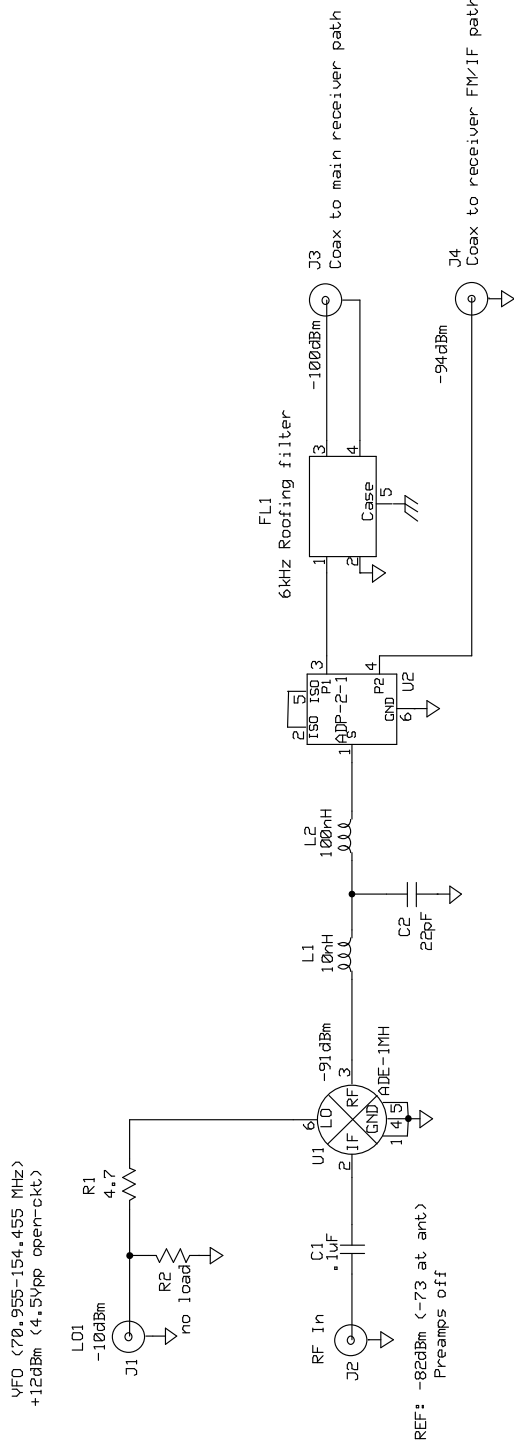
The DZ Co.  
RxBPF  
Rev. B1  
5/22/2014  
B. Mood  
Page 6 of 7

All switches shown in VC=1, EN=0 position



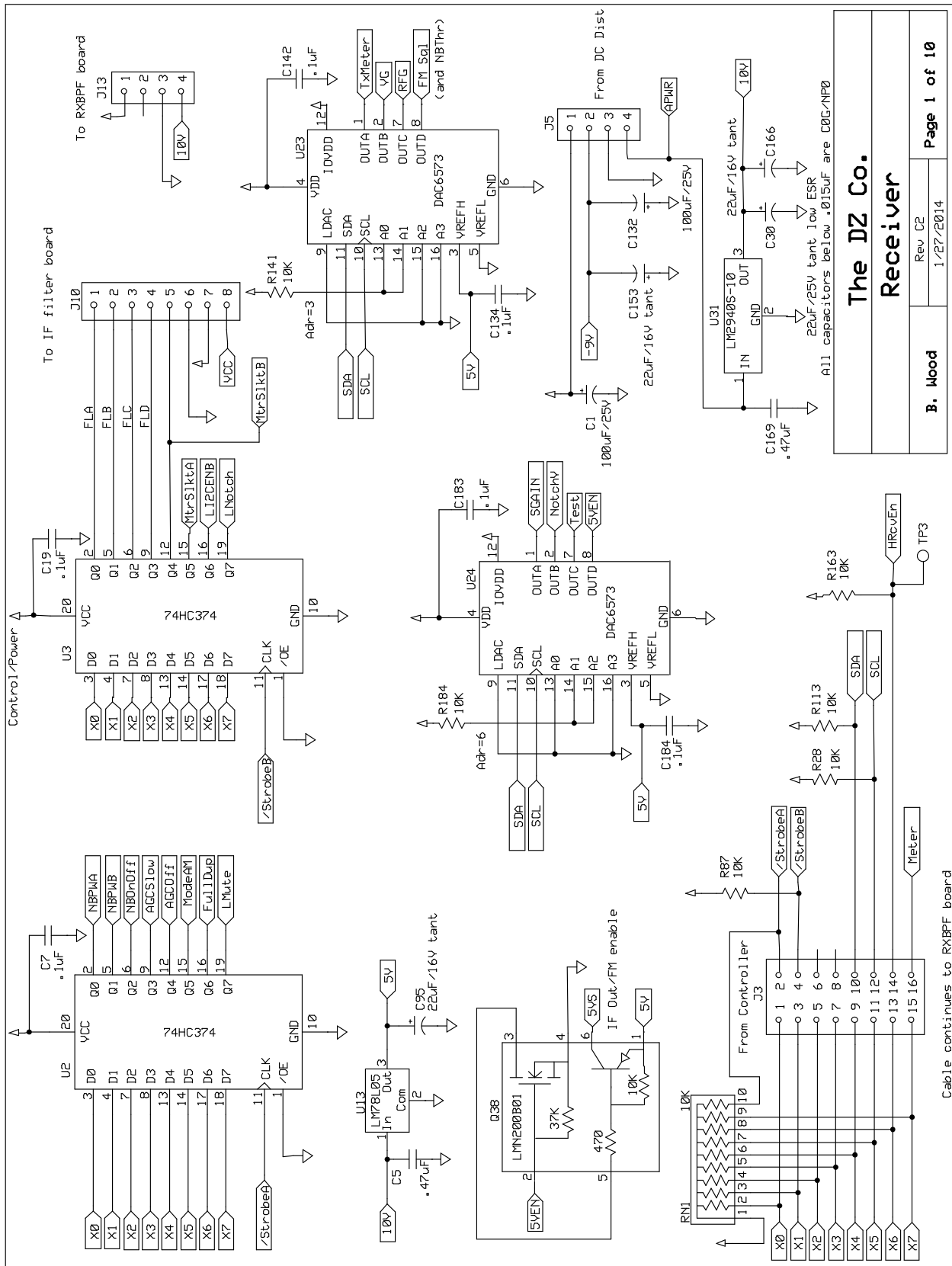
<b>The DZ Co.</b>			
		<b>RxBPF</b>	
<b>B. Wood</b>	Rev B1	<b>Page 7 of 7</b>	
	5/22/2014		

All switches shown in VC=1, EN=0 position

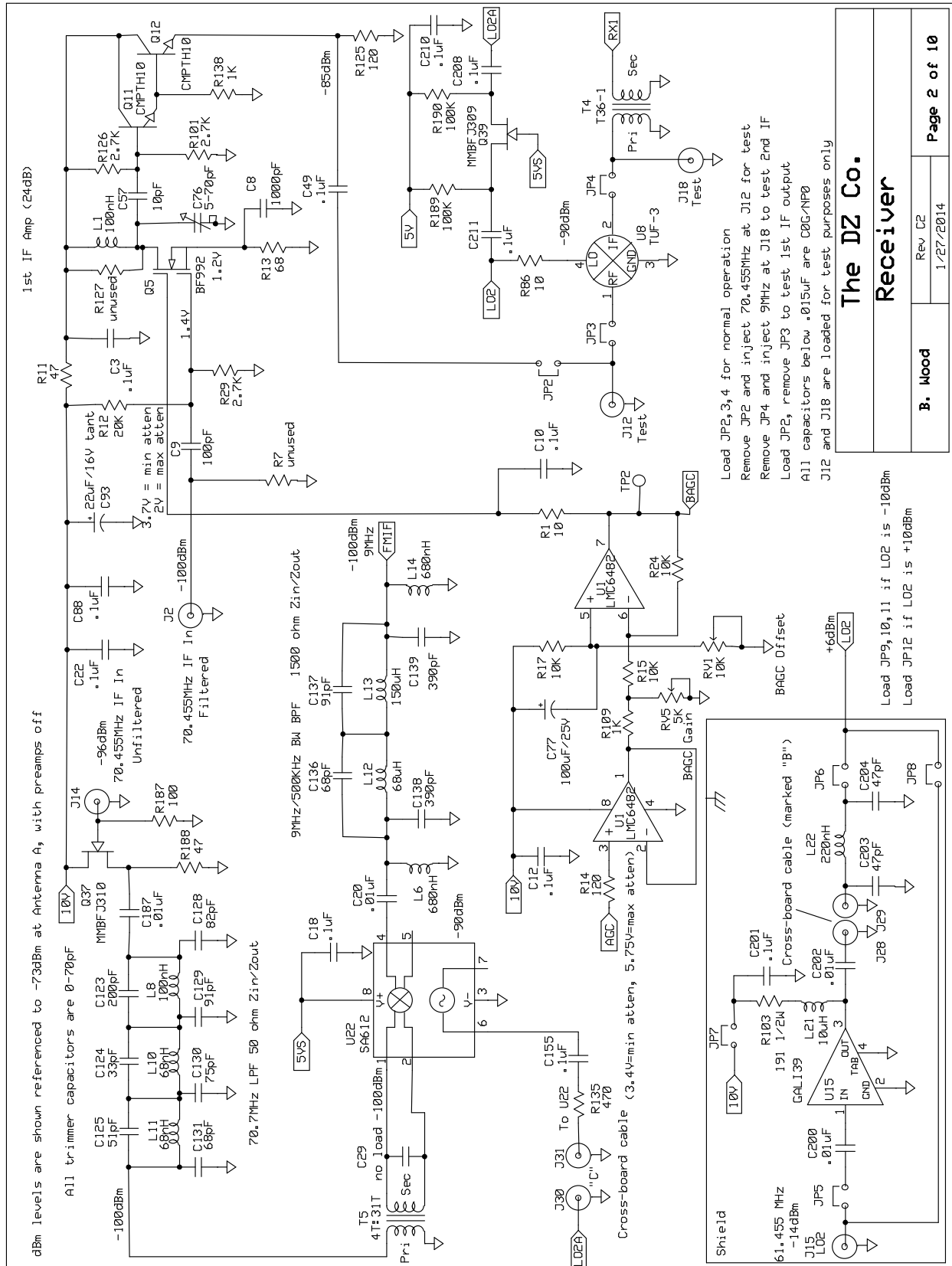


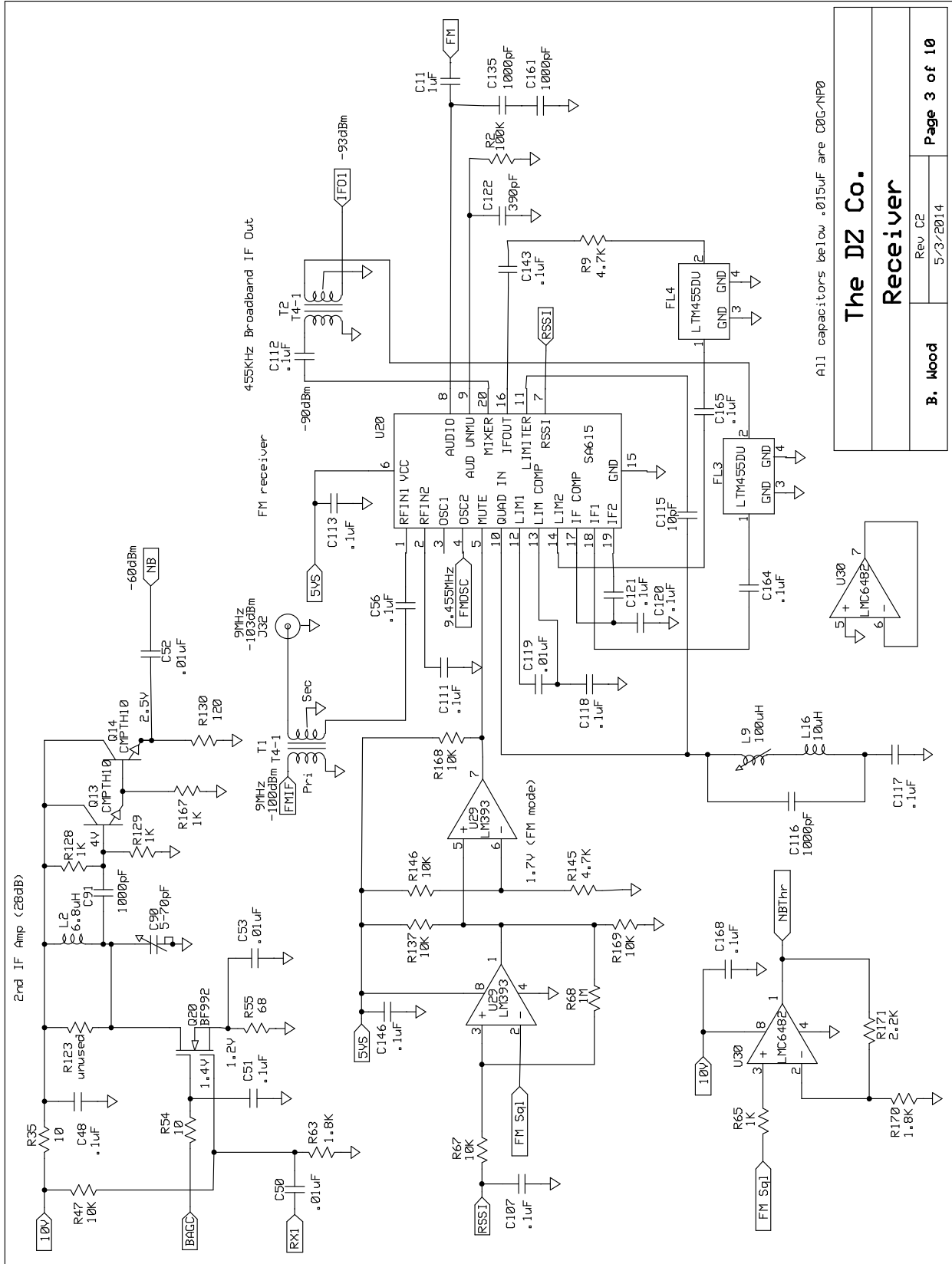
Note: Laird 205F shield is placed over U1 and T1, soldered to mixer ground  
Case of FL1 is connected to chassis via crushable conductive material

<b>The DZ Company, LLC</b>	
<b>1st mixer/filter</b>	
<b>B. Wood</b>	Rev A3 9/28/2014
Page 1 of 1	









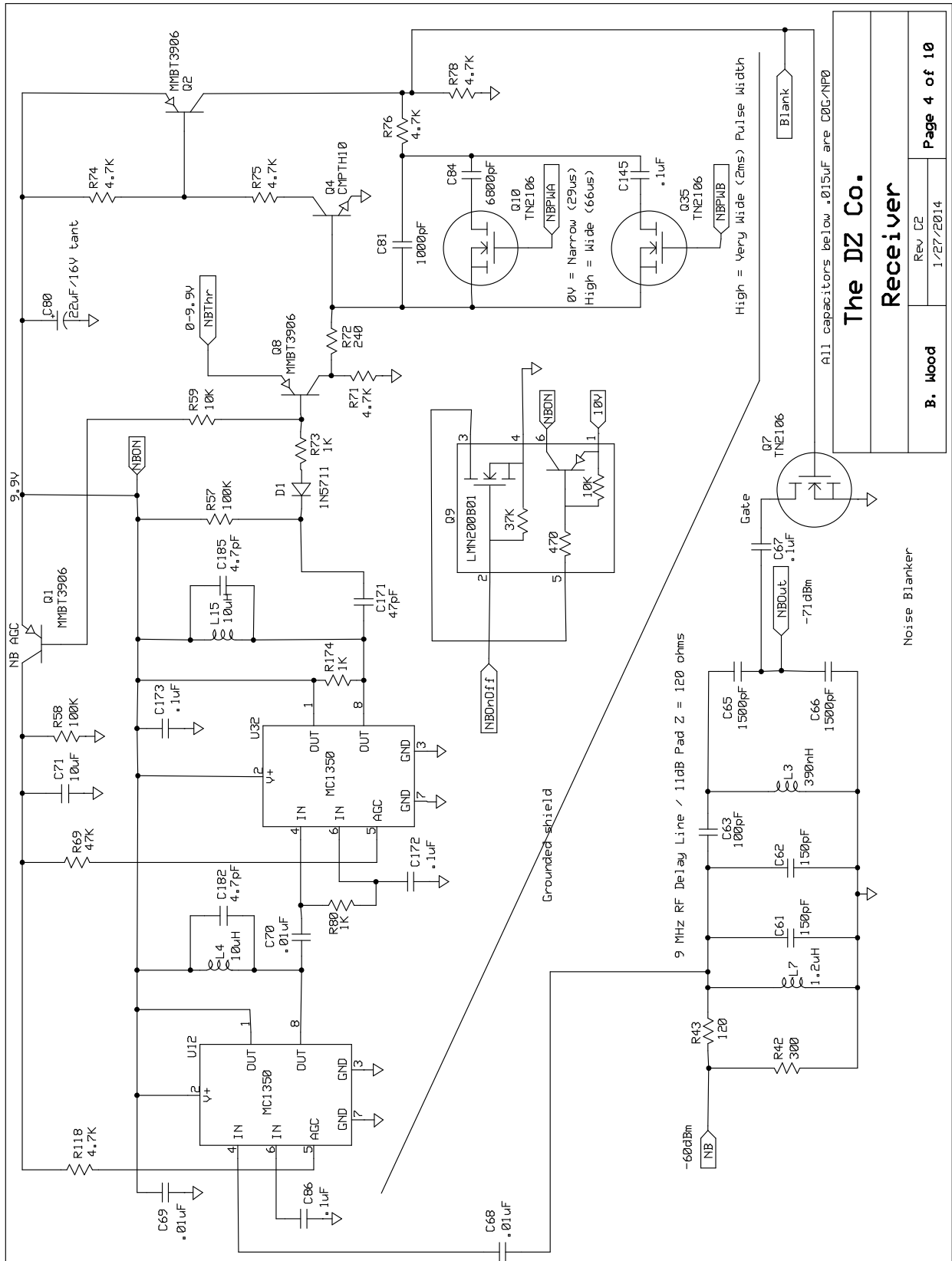
All capacitors below .015uF are C0G/NP0

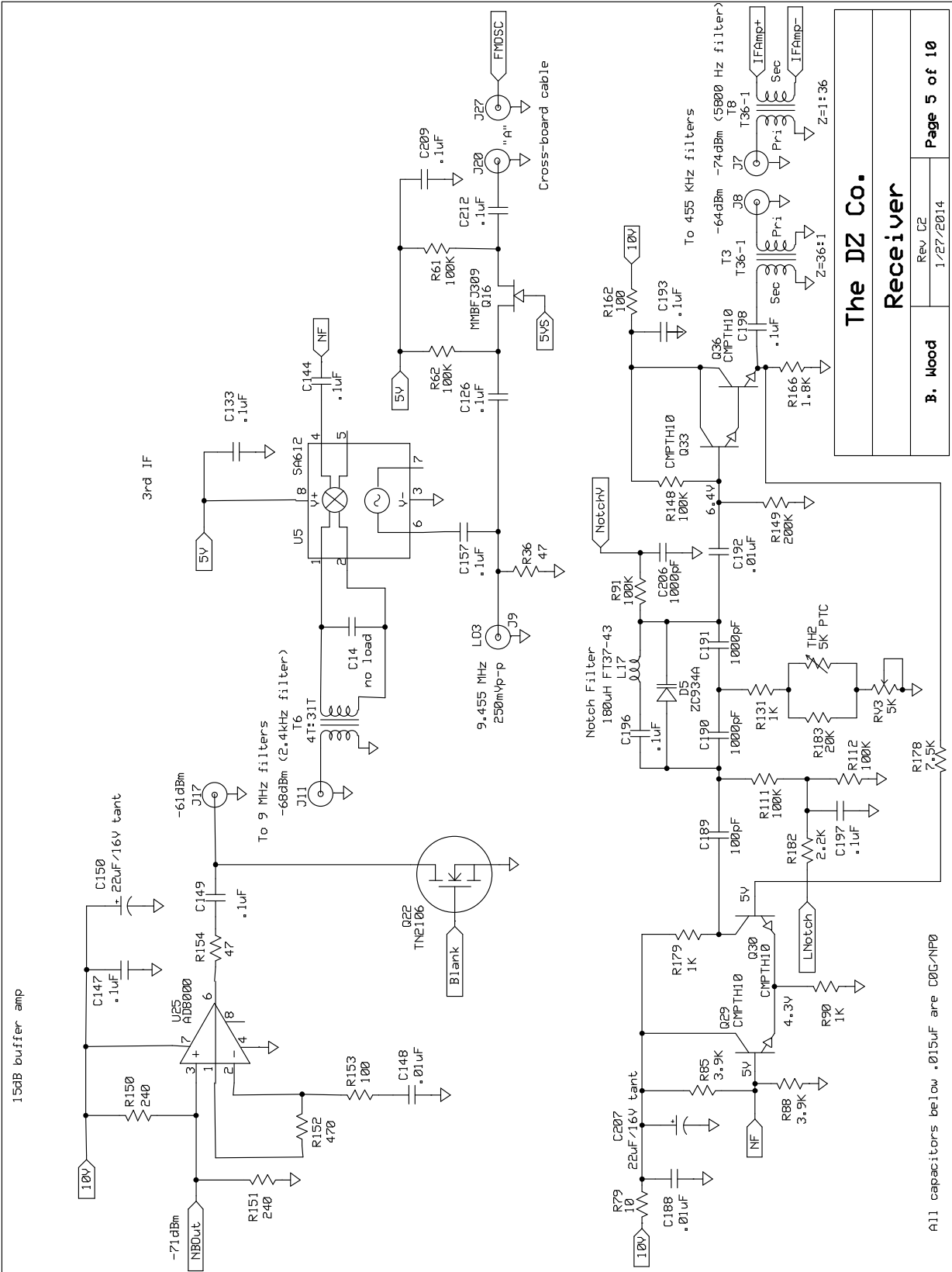
# The DZ Co. Receiver

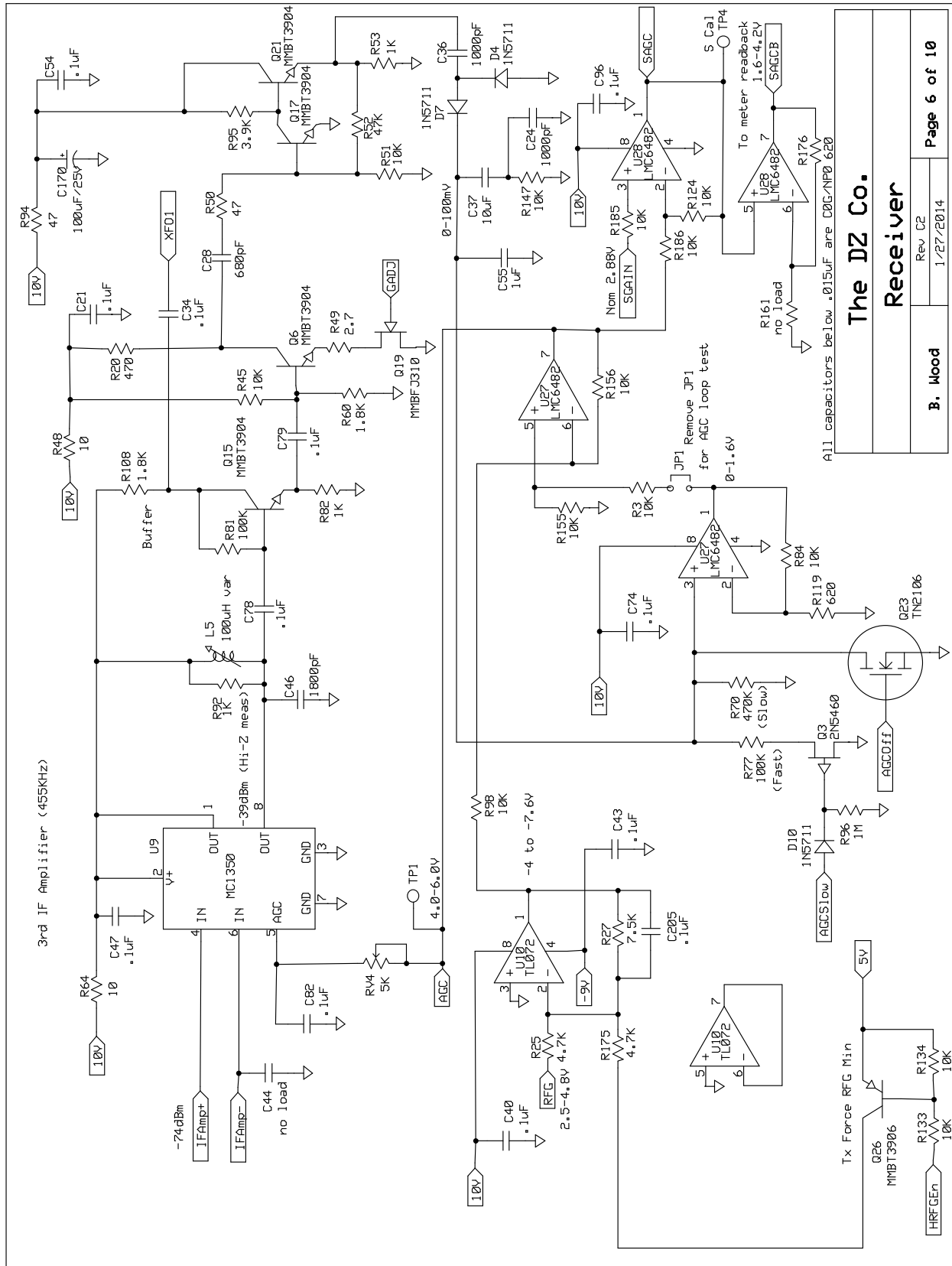
Rev C2  
5/3/2014

B. Wood

Page 3 of 10



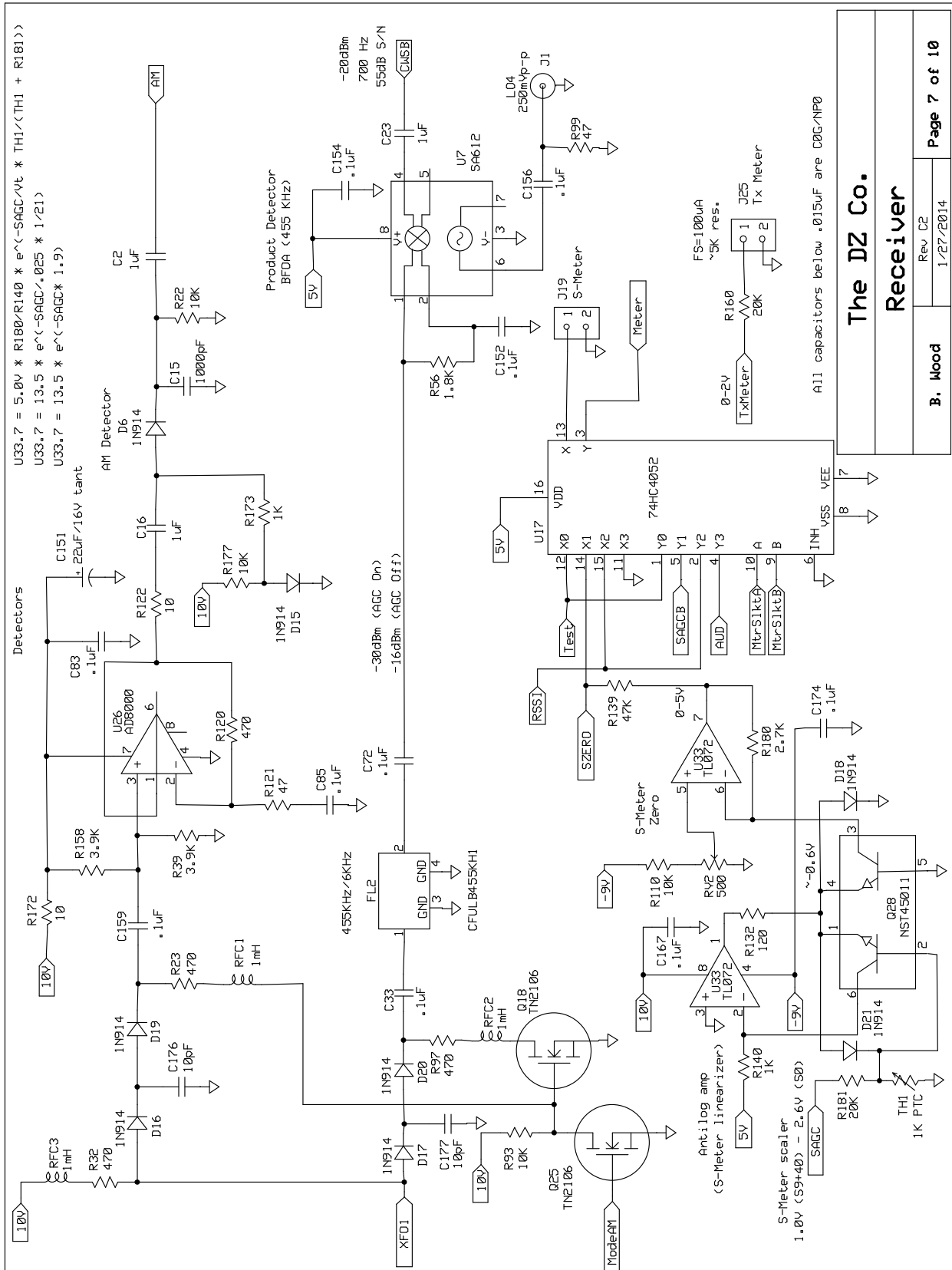


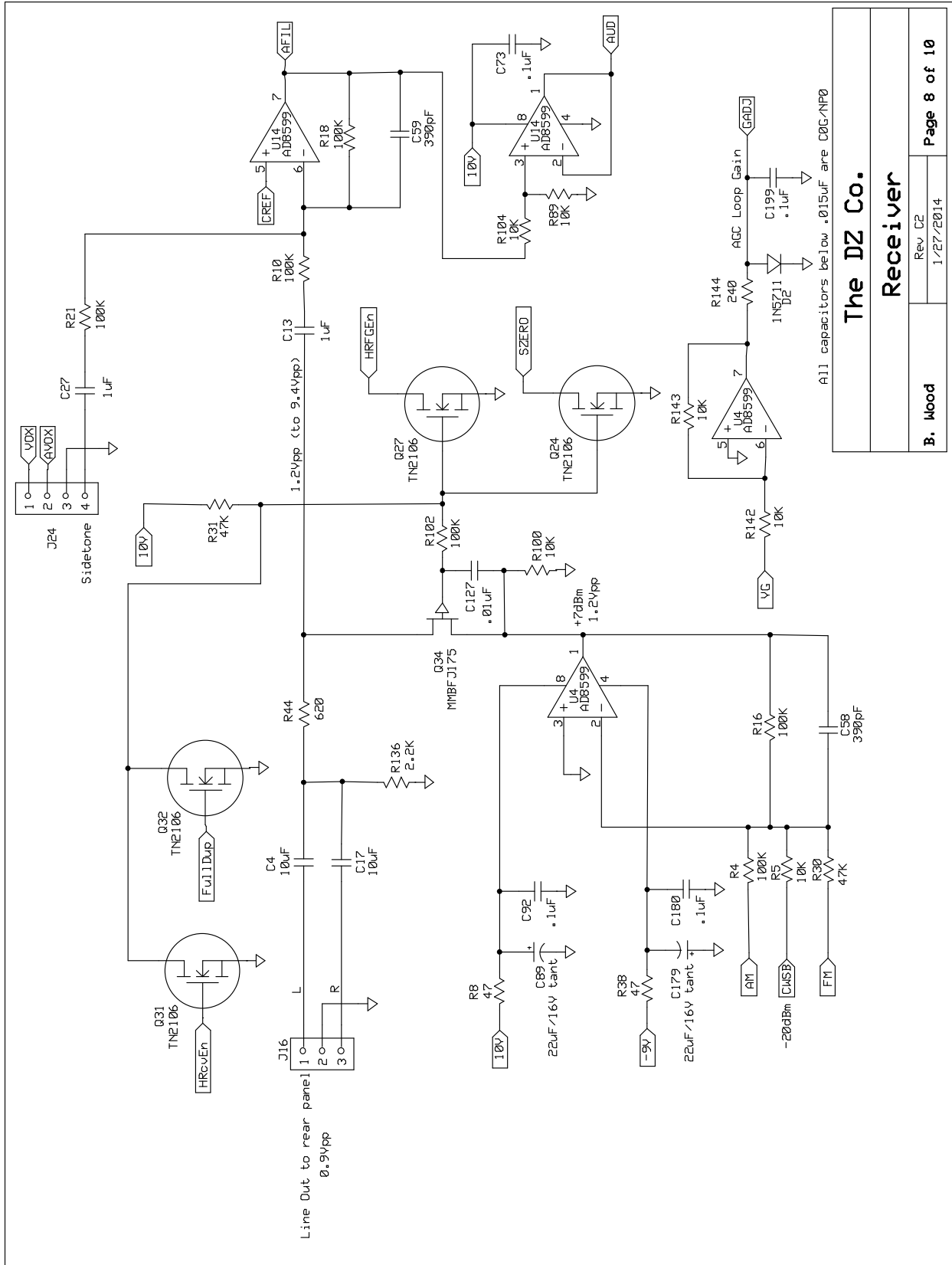


All capacitors below .015uF are C0G/NP0 620

The DZ Co. Receiver

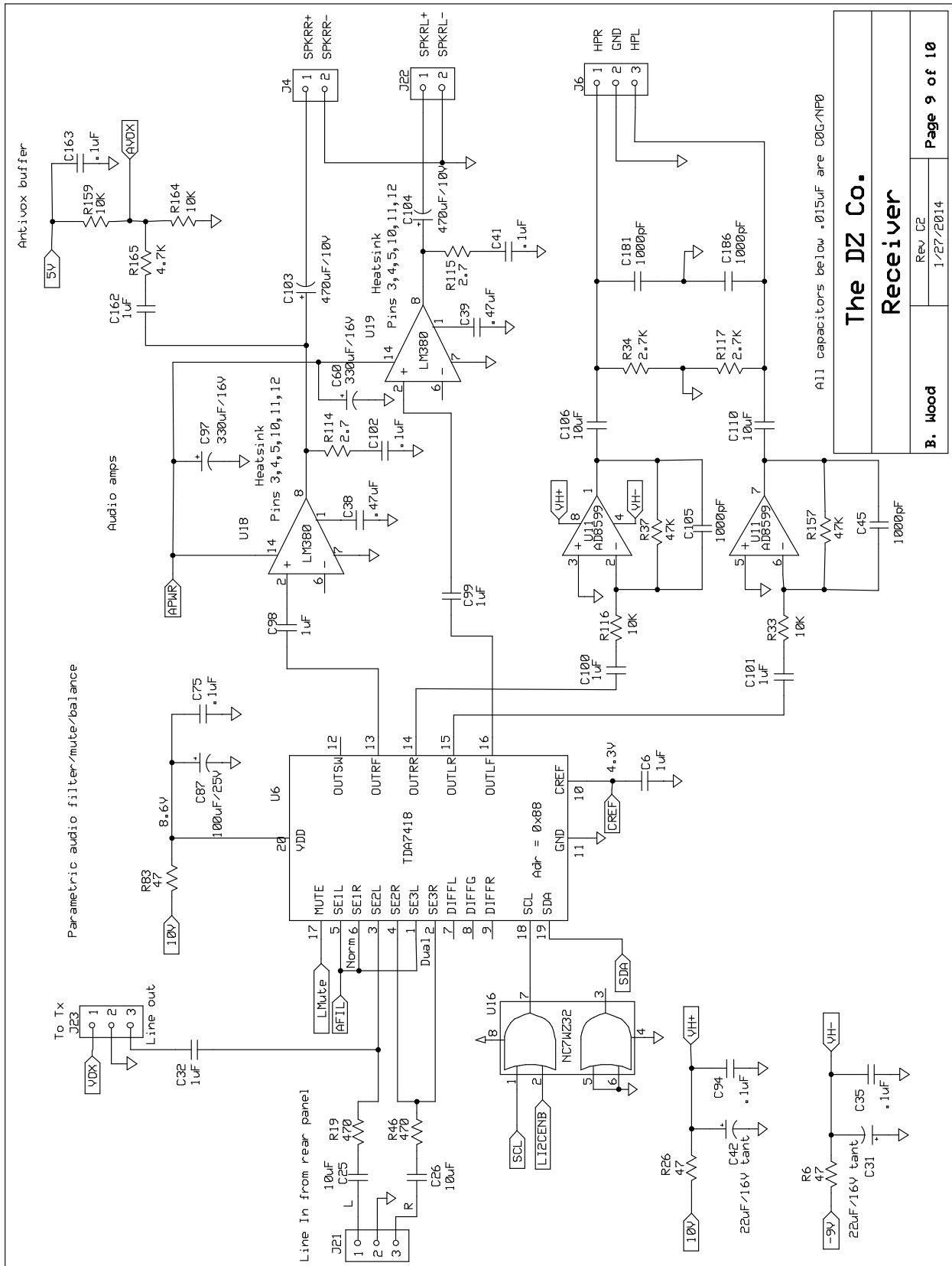
B. Wood	Rev C2	Page 6 of 10
	1/27/2014	





**The DZ Co.**  
**Receiver**  
Rev C2  
1/27/2014  
**Page 8 of 10**

**B. blood**



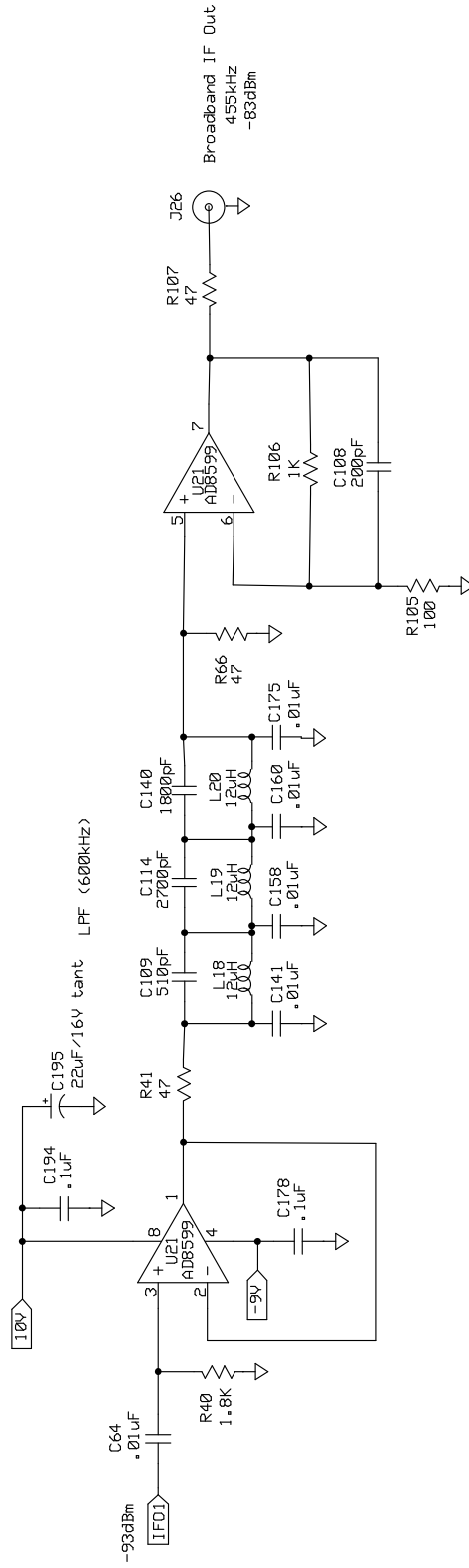
**The DZ Co.**  
**Receiver**

**B. Blood**  
REV C2  
1/27/2014  
**Page 9 of 10**



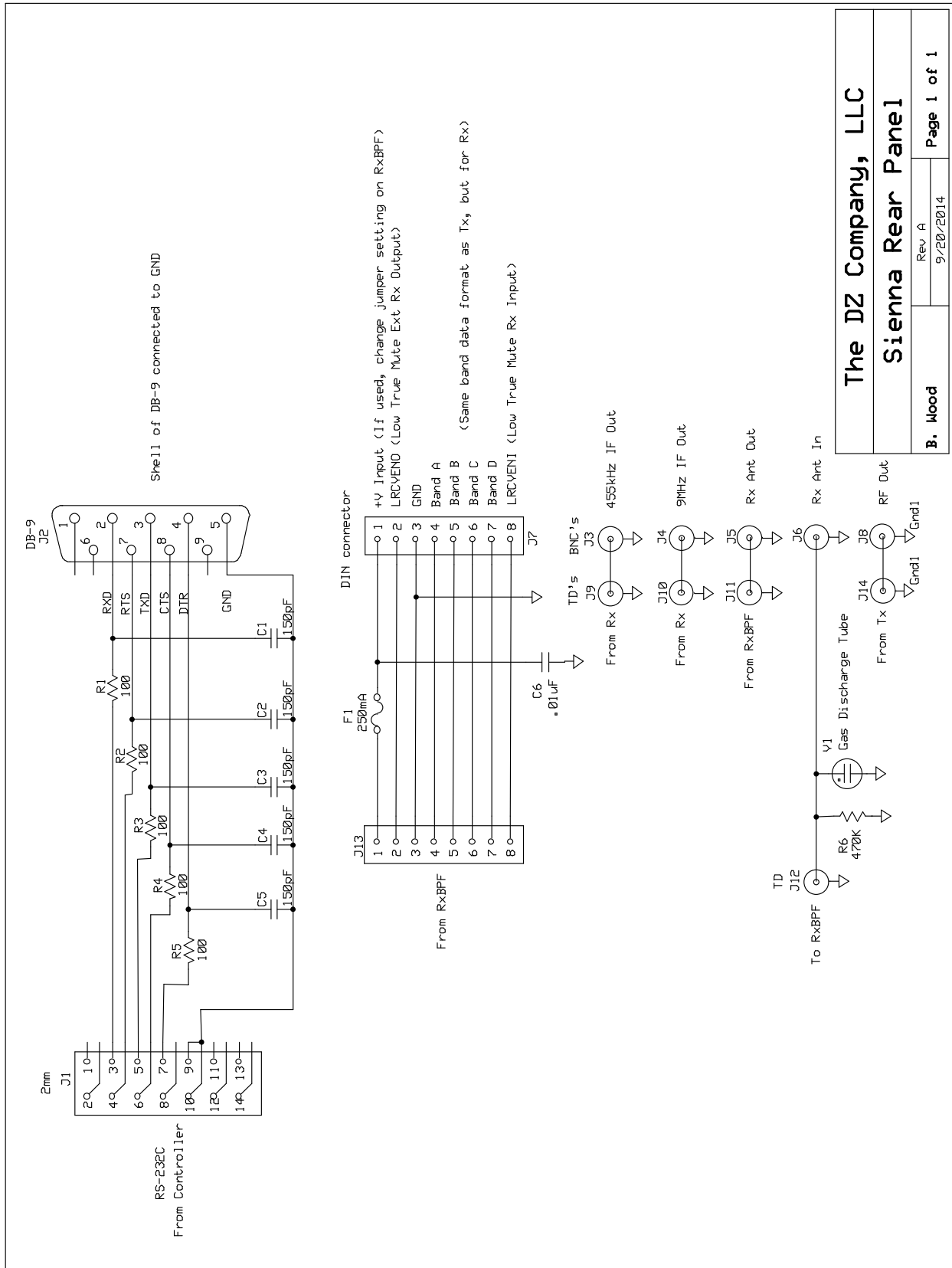


IF Output amp/filter



All capacitors below .015uF are 00G/NP0

<b>The DZ Co.</b>		Rev. C2
		5/3/2014
<b>B. Wood</b>	<b>Page 10 of 10</b>	



The DZ Company, LLC

Sienna Rear Panel

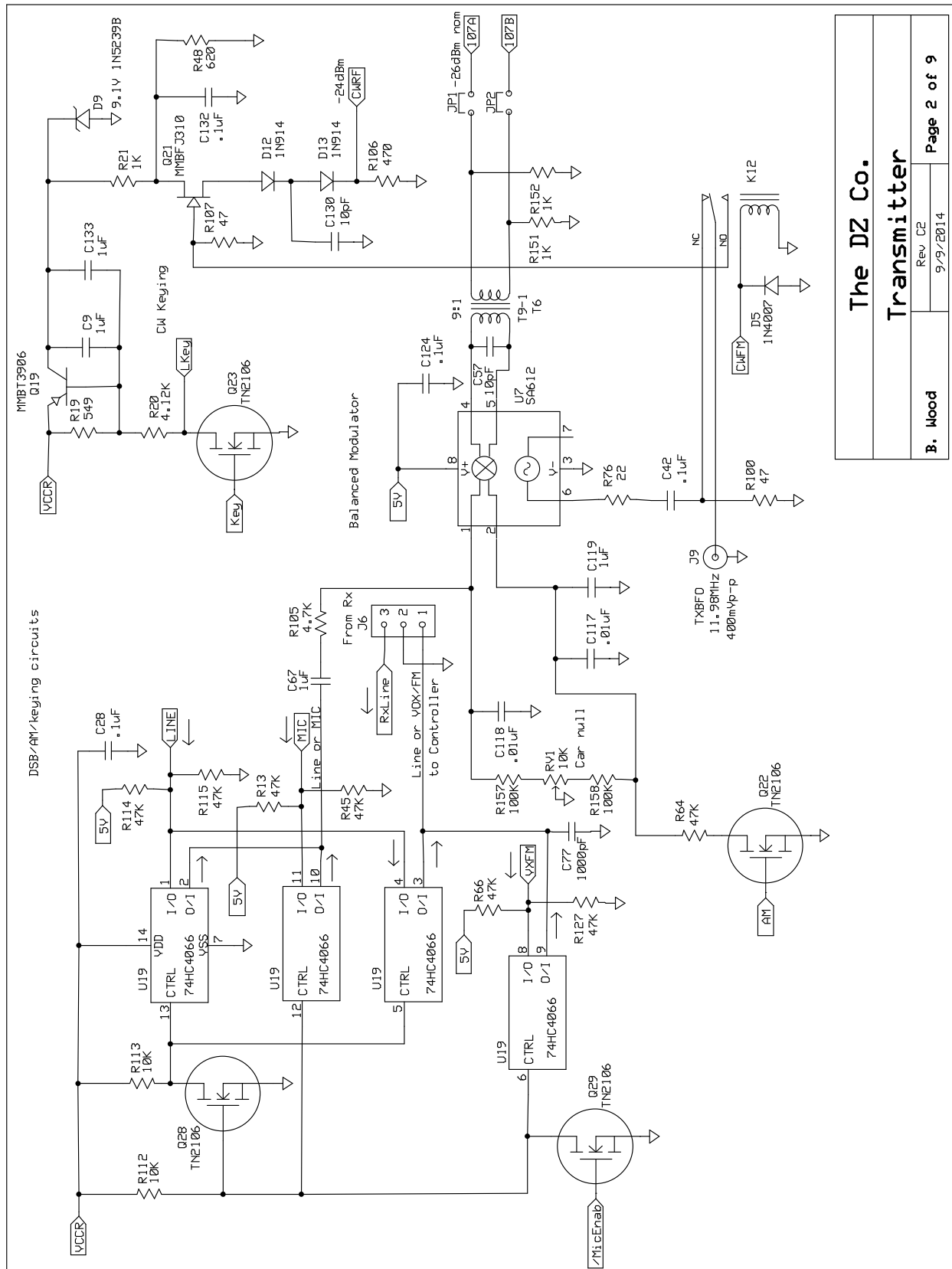
Rev A

9/20/2014

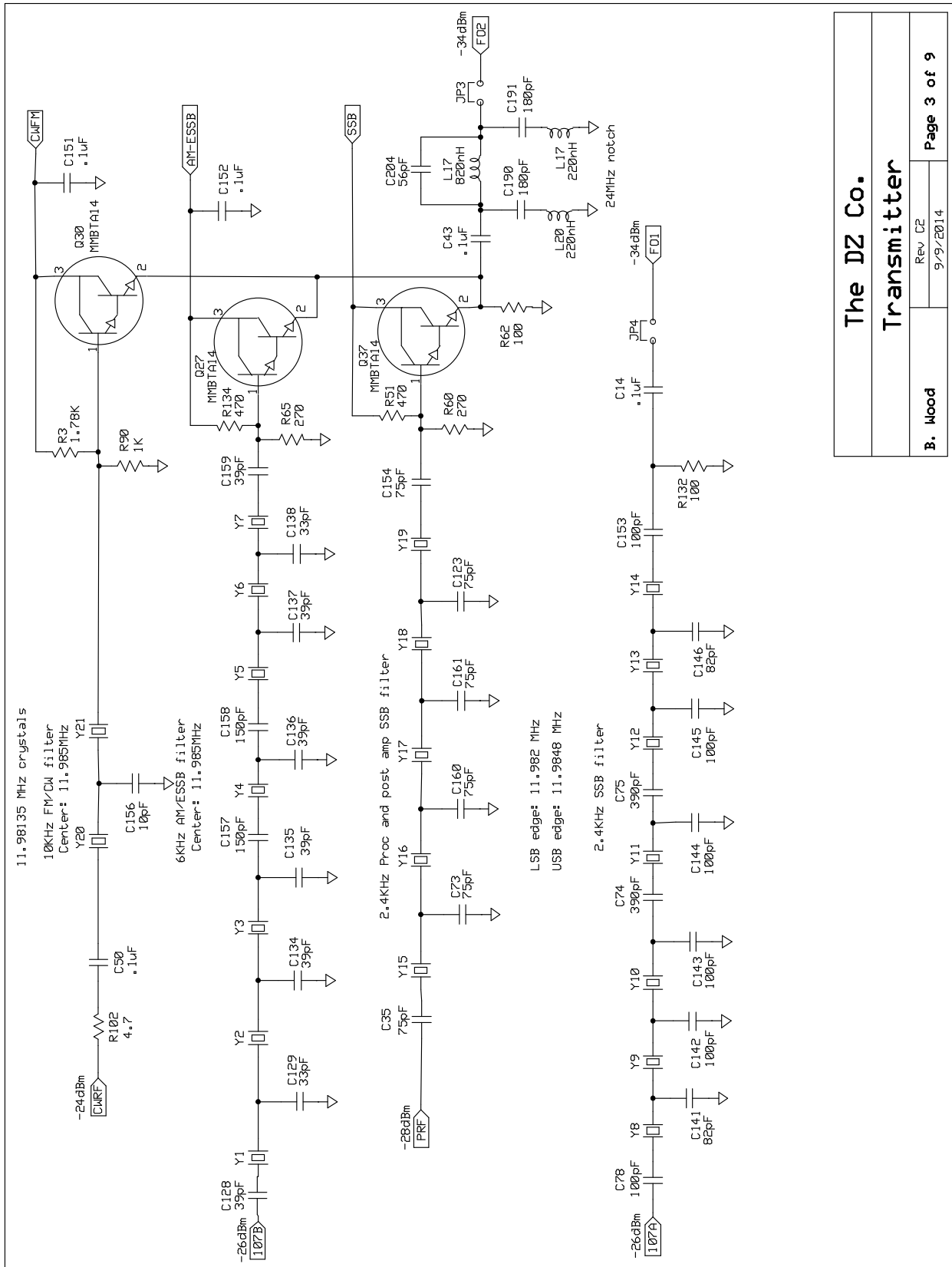
B. Wood

Page 1 of 1





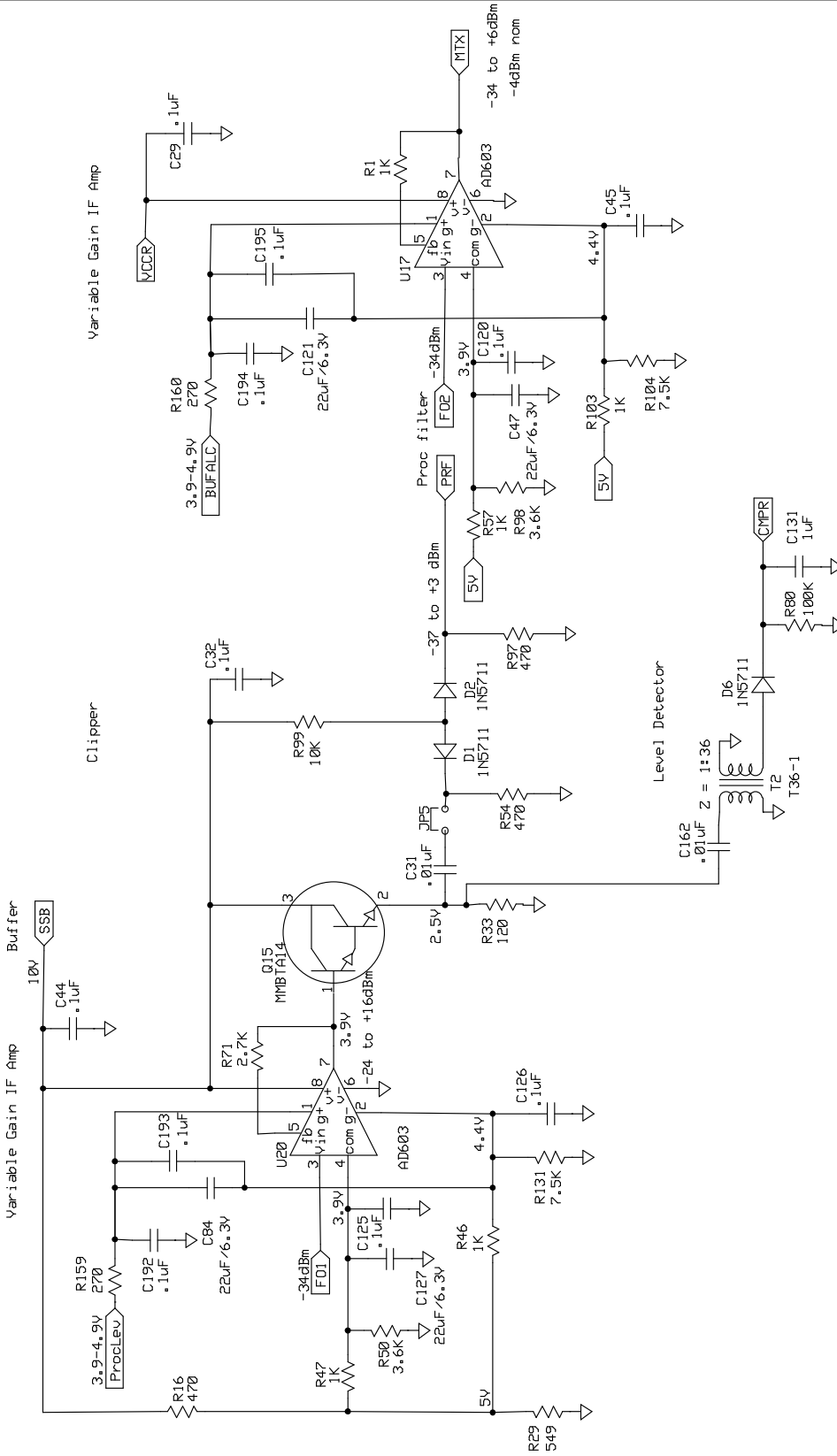
**The DZ Co.**  
**Transmitter**  
Rev C2  
9/9/2014  
Page 2 of 9  
B. Wood



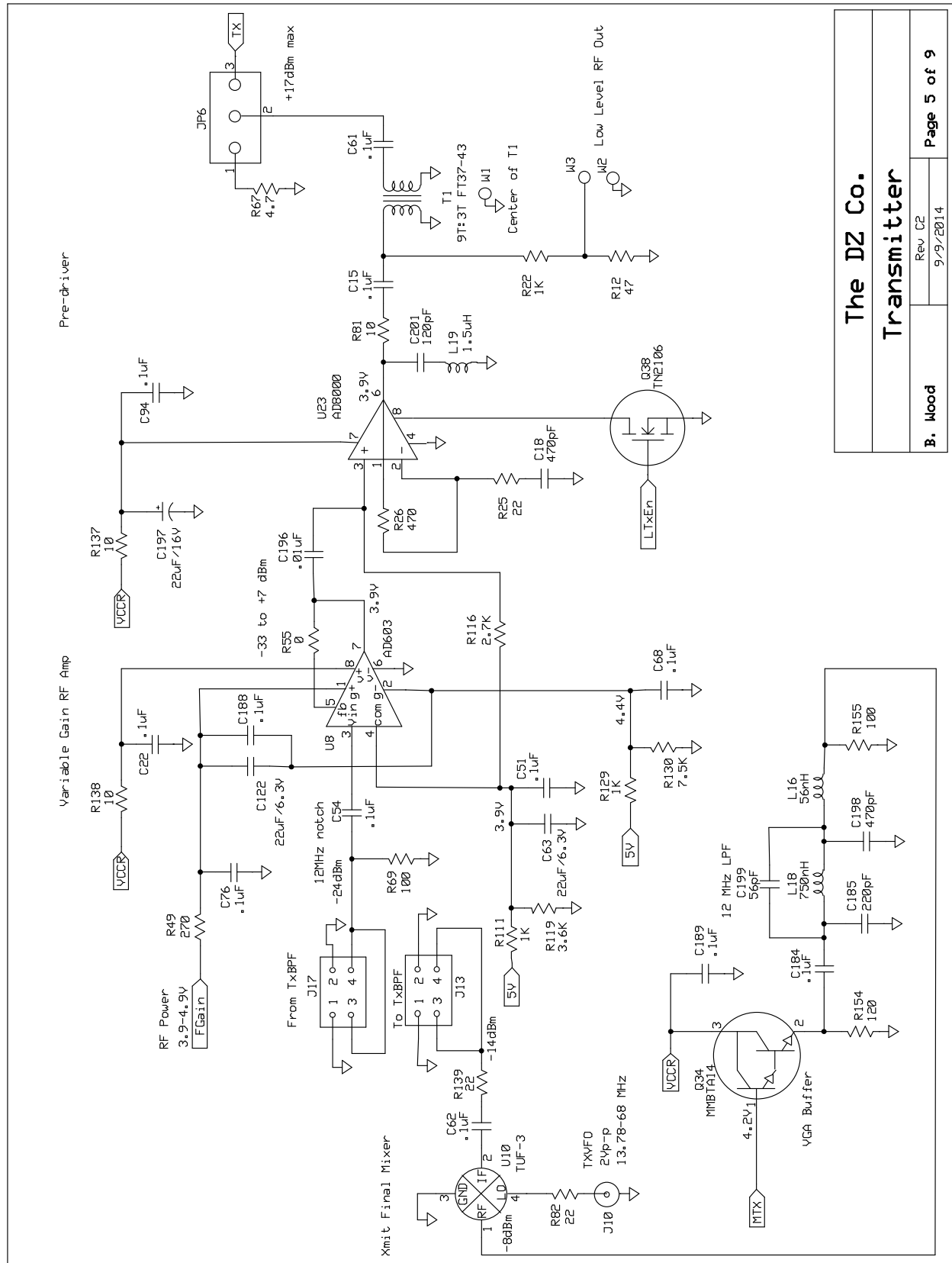
**The DZ Co.**  
**Transmitter**  
Rev C2  
9/9/2014  
**B. Wood**  
Page 3 of 9



RF Speech processor / SSB preamp



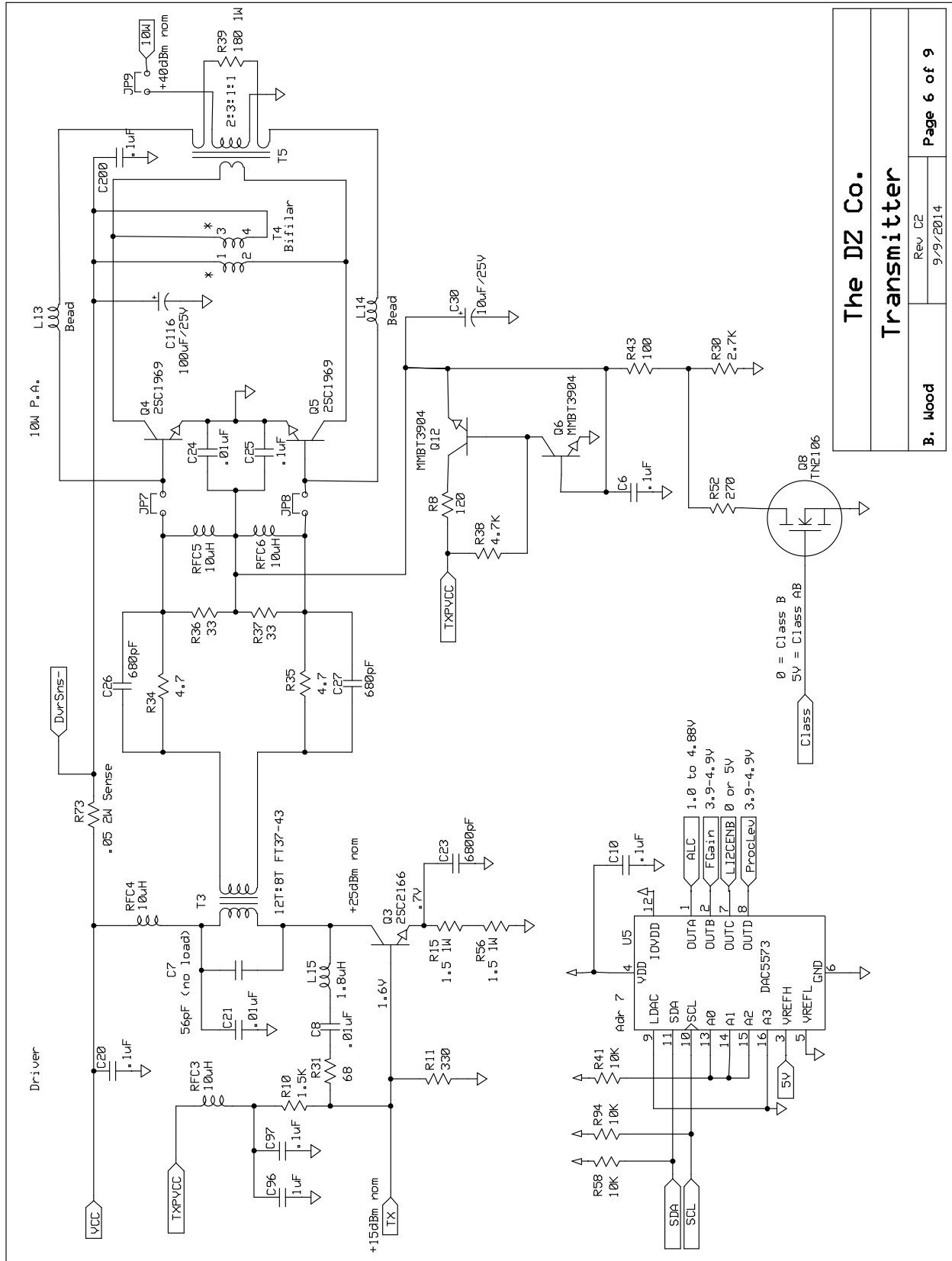
The DZ Co.  
Transmitter  
Rev C2  
9/9/2014  
Page 4 of 9  
B. Wood



**The DZ Co.**  
**Transmitter**

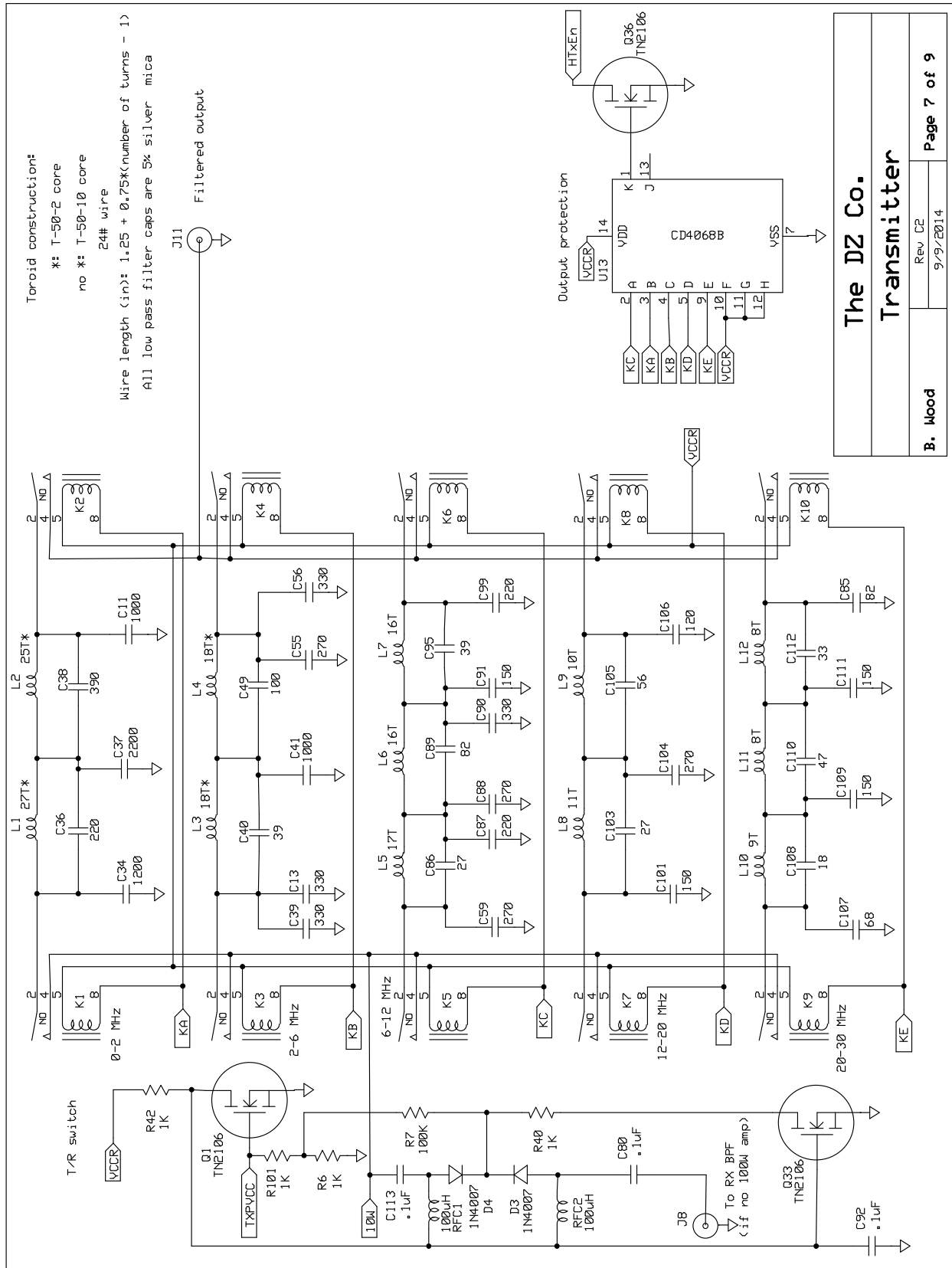
Rev C2	Page 5 of 9
9/9/2014	

**B. Blood**

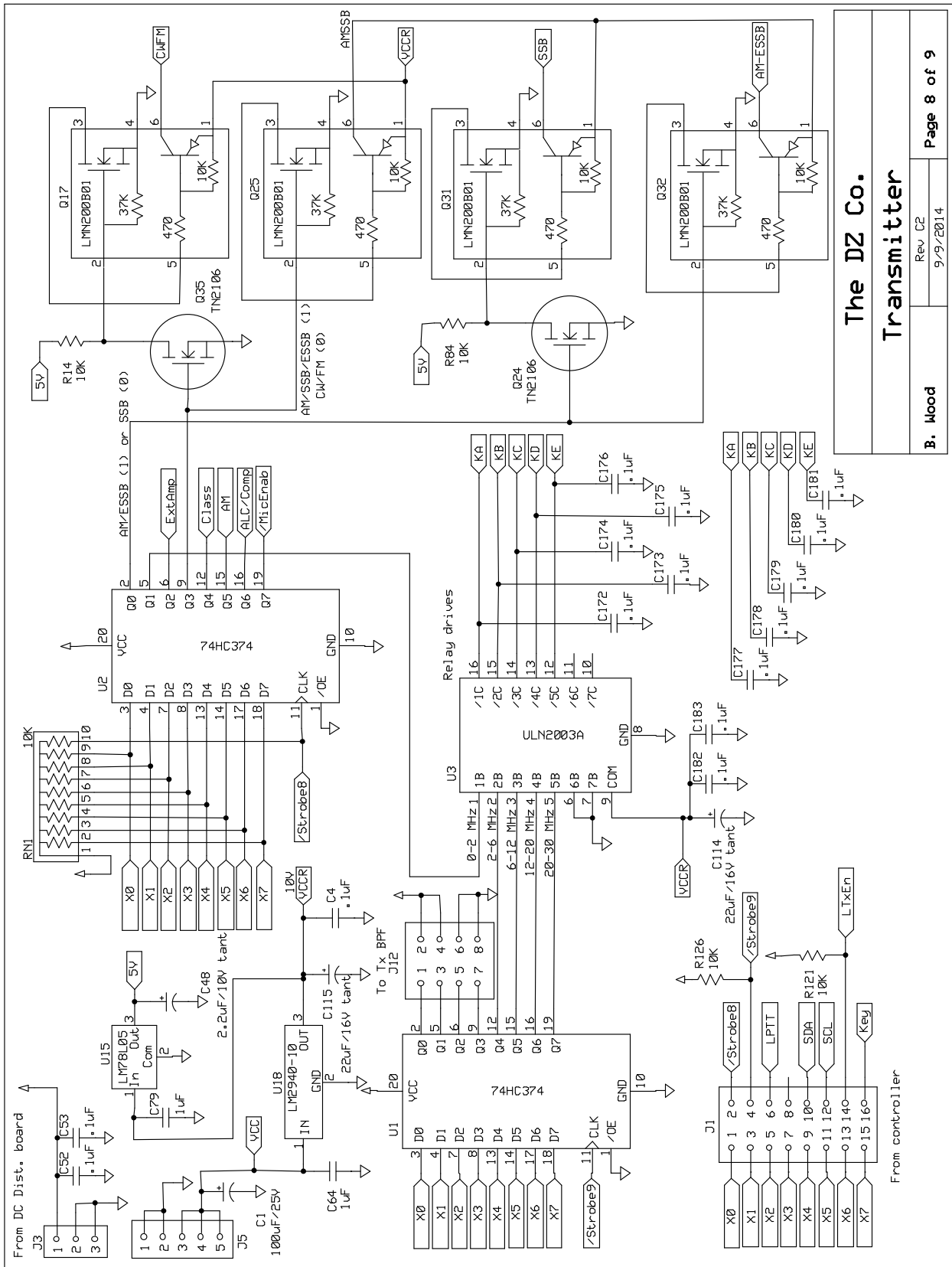


<b>The DZ Co.</b>	
<b>Transmitter</b>	
Rev C2	9/9/2014
<b>B. Blood</b>	
<b>Page 6 of 9</b>	

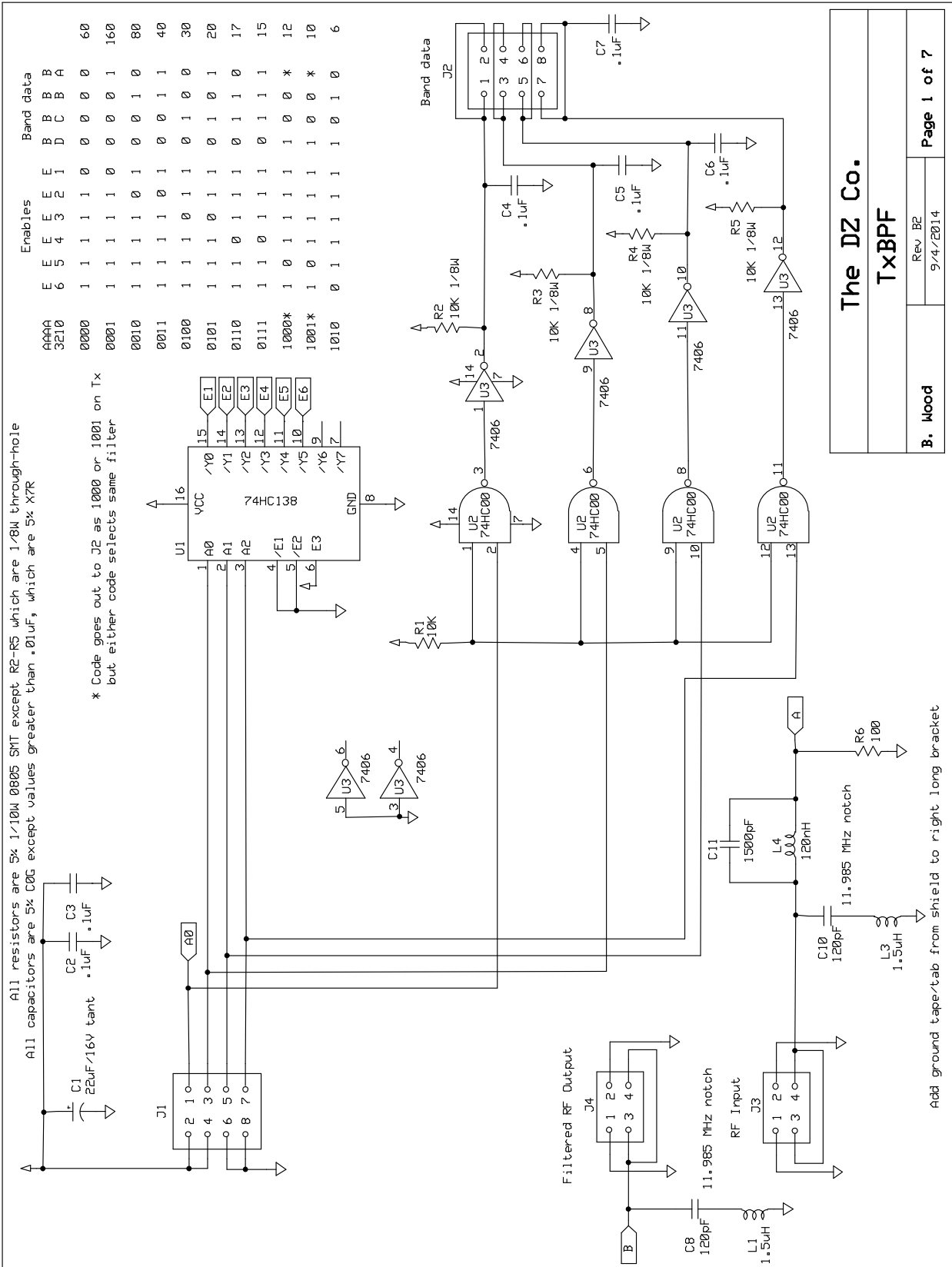




**The DZ Co.**  
**Transmitter**  
 Rev C2  
 9/9/2014  
**B. Mood**  
 Page 7 of 9

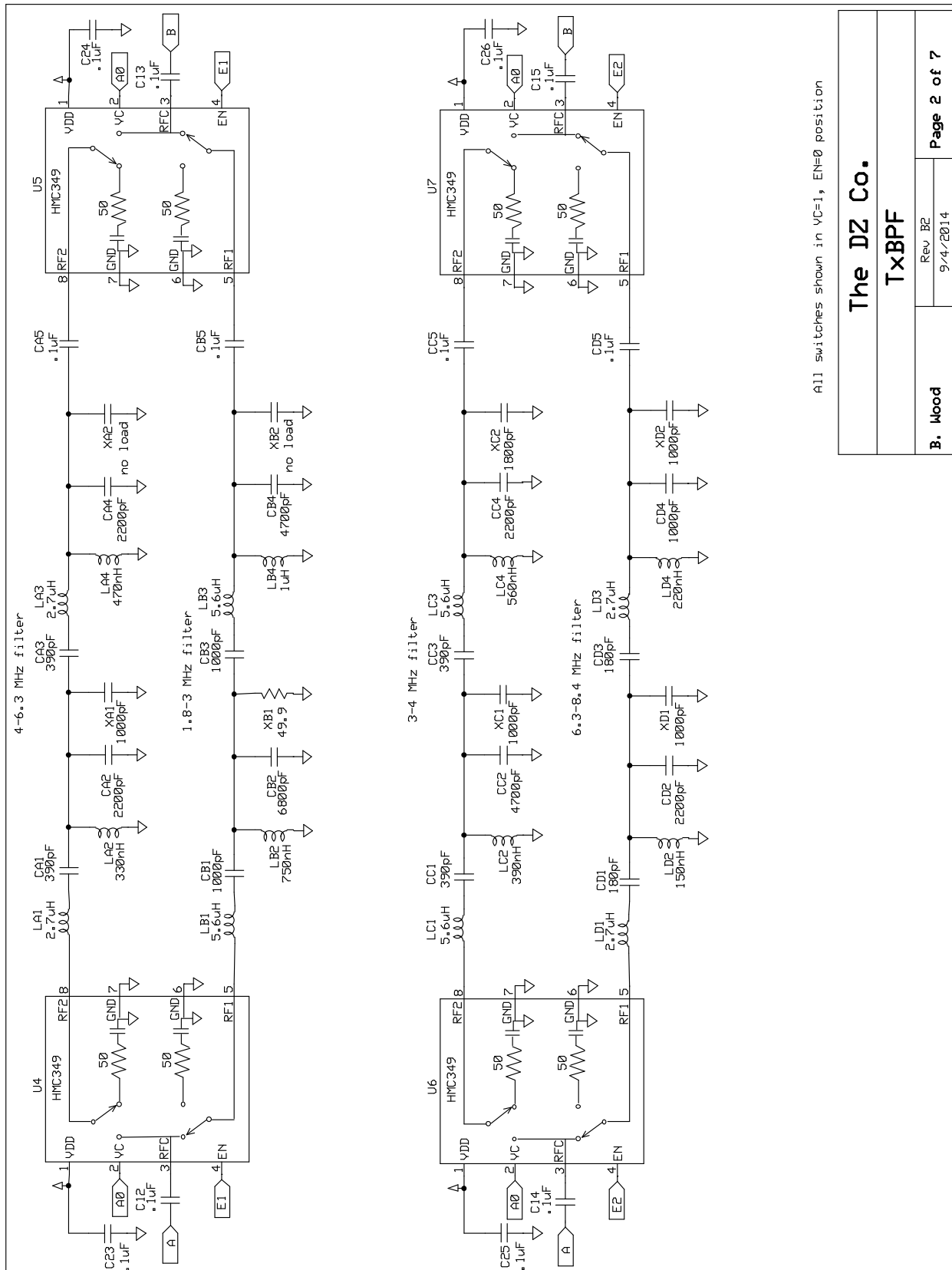






The DZ Co.  
 Tx BPF  
 Rev B2  
 9/4/2014  
 B. Mood  
 Page 1 of 7

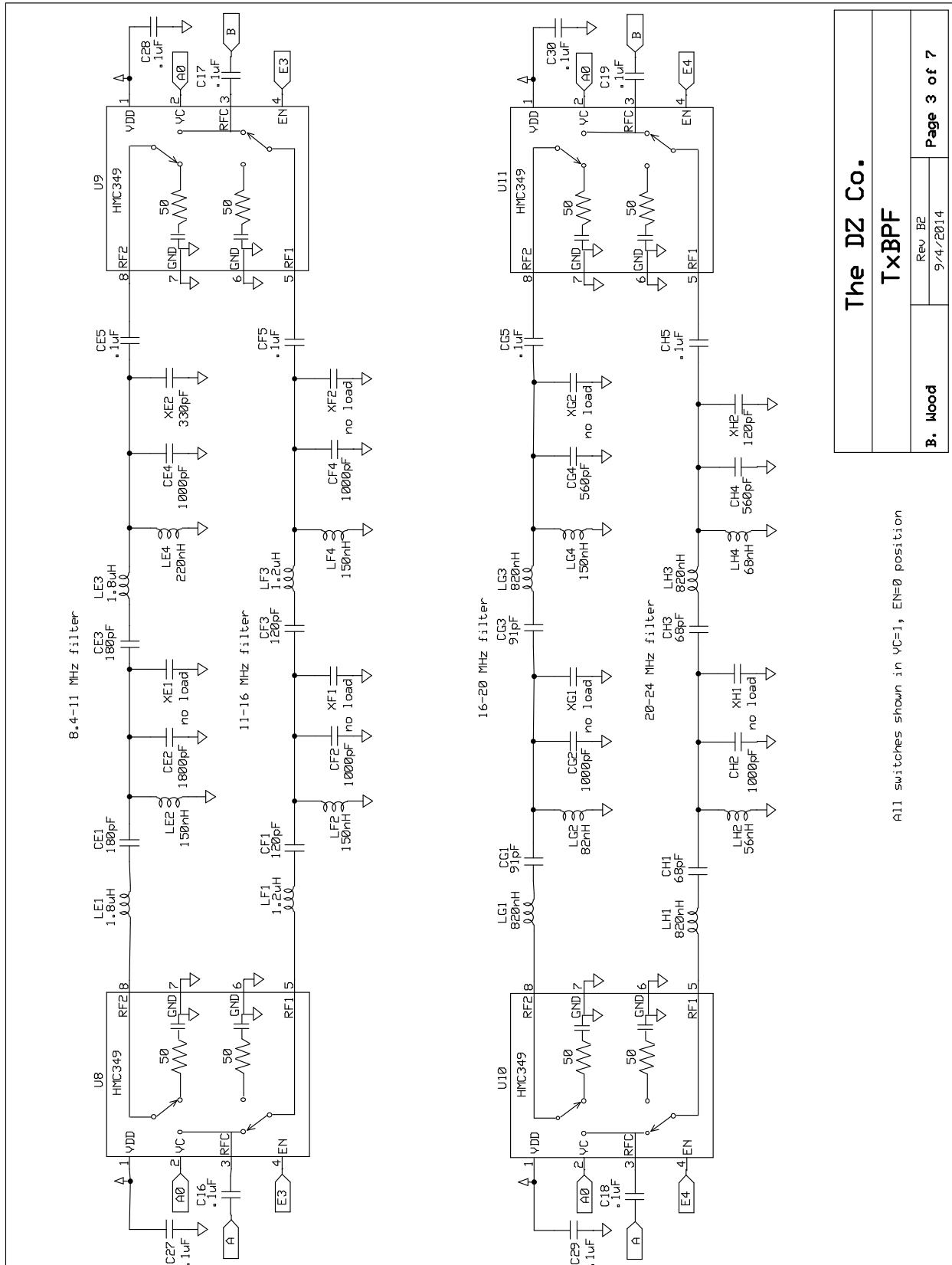
Add ground tape/tab from shield to right long bracket



All switches shown in VC=1, EN=0 position

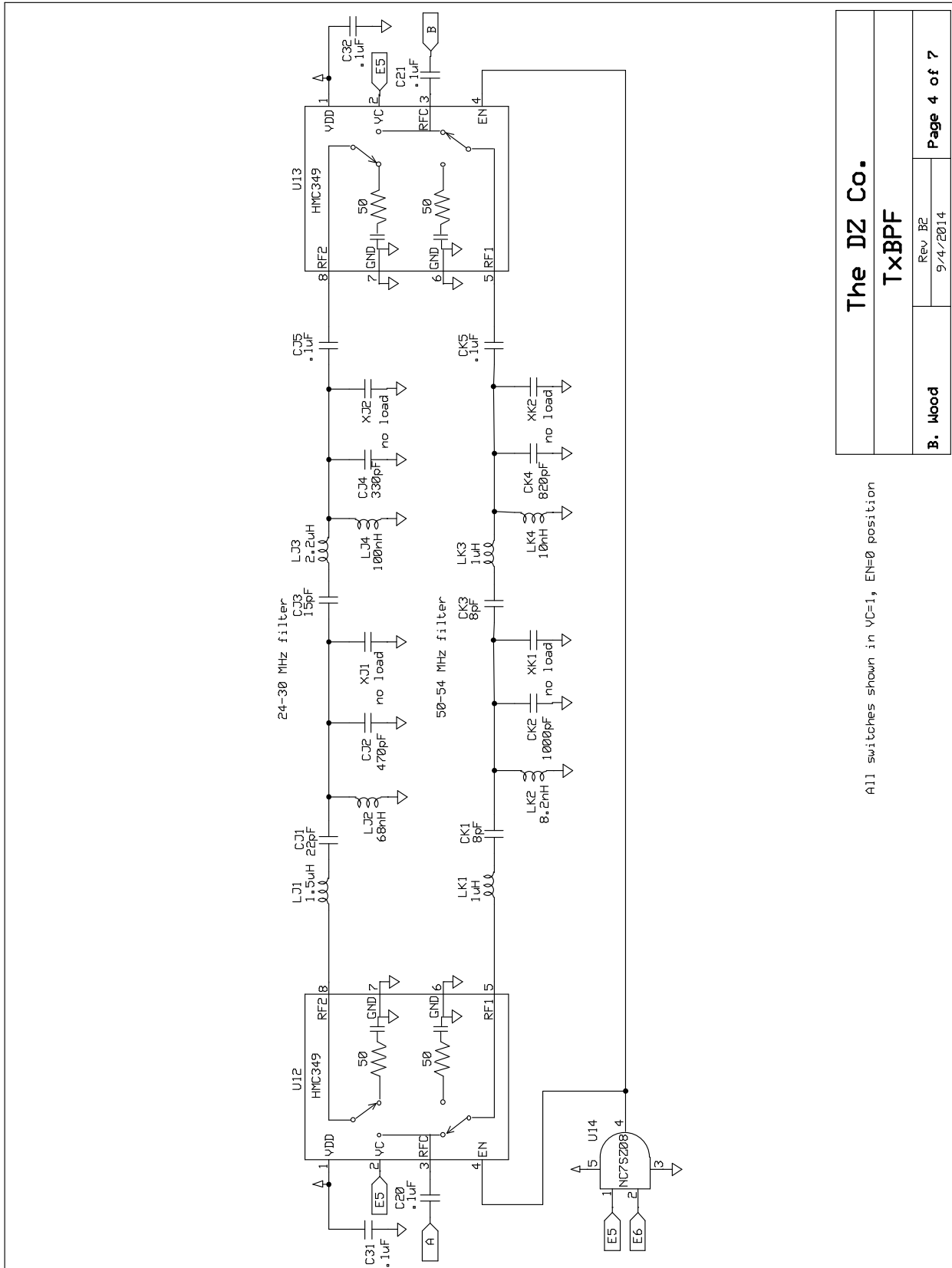
<b>The DZ Co.</b>	
<b>TxBPF</b>	
Rev B2	Page 2 of 7
9/4/2014	

B. Wood



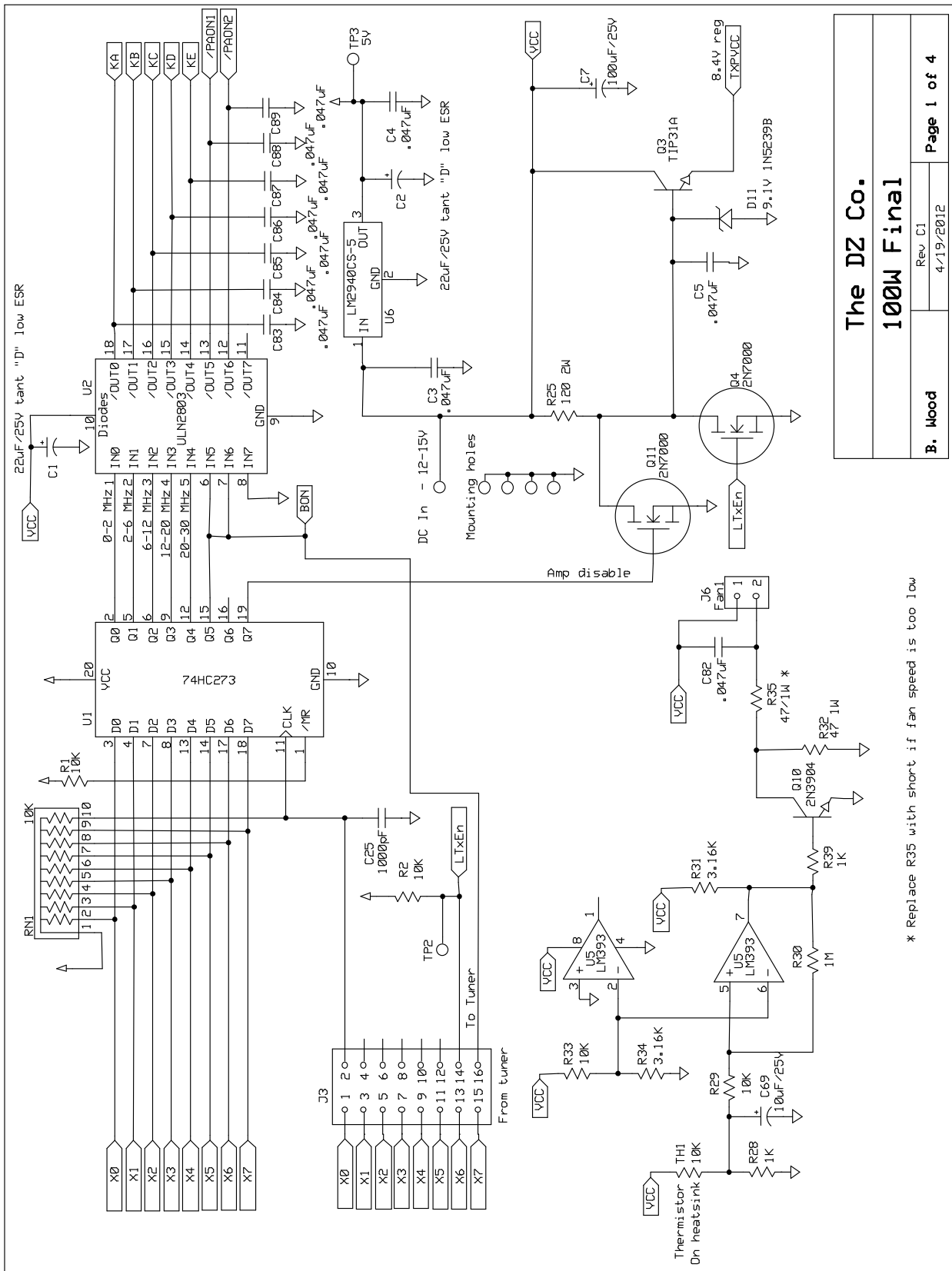
All switches shown in VC=1, EN=0 position

**The DZ Co.**  
**TxBPF**  
 Rev. B2  
 9/4/2014



<b>The DZ Co.</b>	
<b>TxBPF</b>	
Rev. BE	9/4/2014
<b>B. Hood</b>	<b>Page 4 of 7</b>

All switches shown in VC=1, EN=0 position

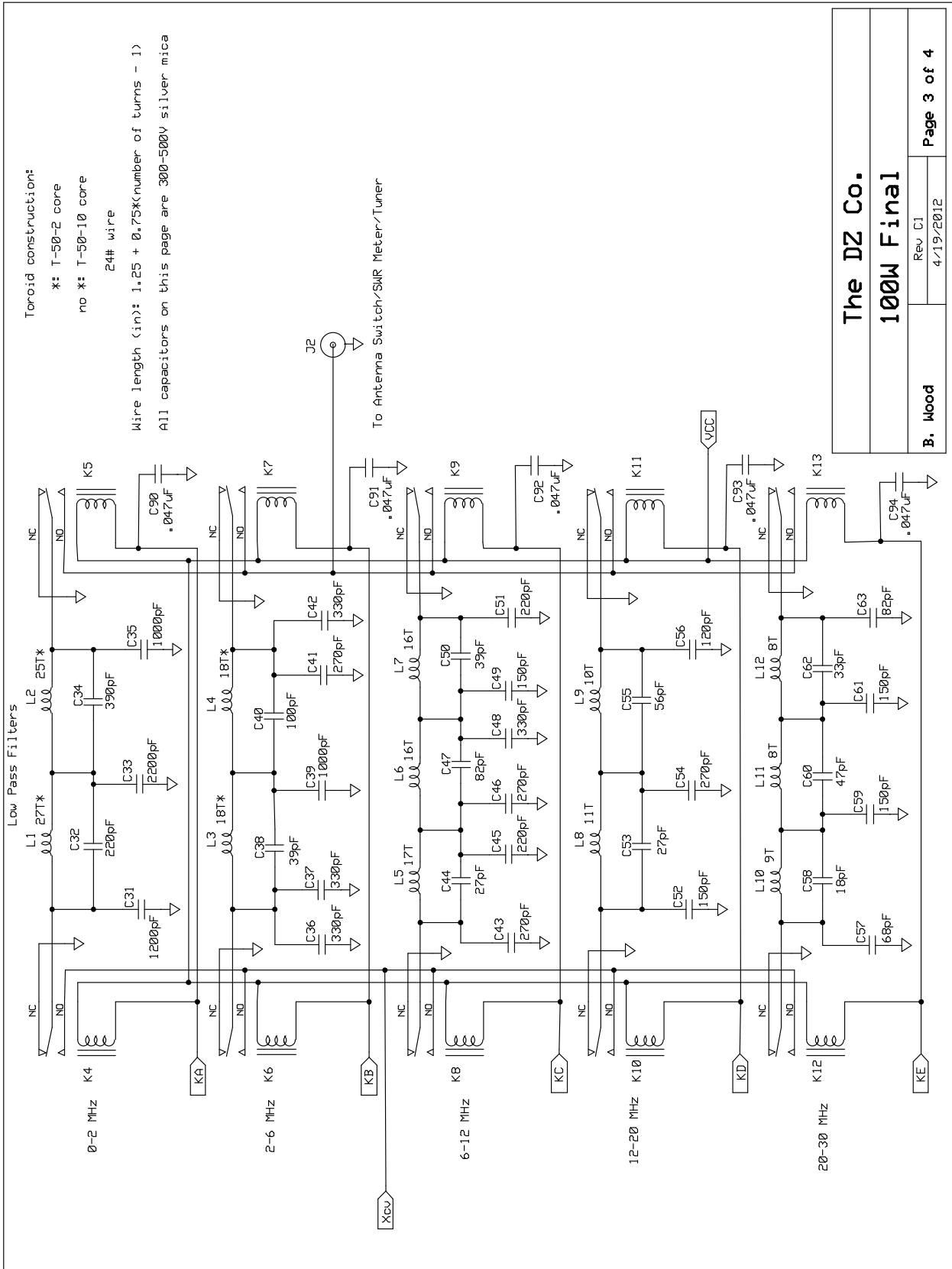


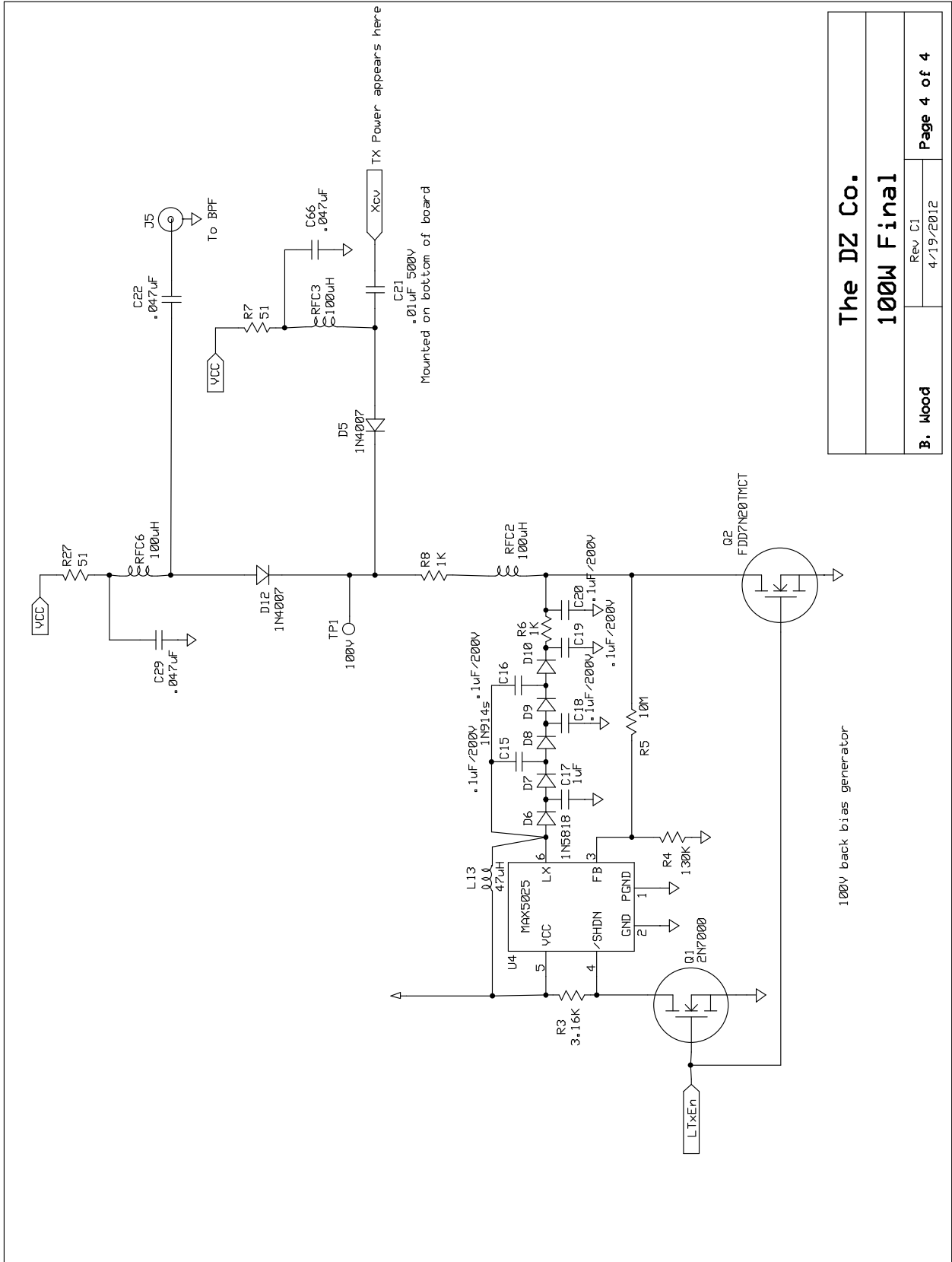
**The DZ Co.**  
**100W Final**  
Rev C1  
4/19/2012  
**B. Hood** Page 1 of 4

\* Replace R35 with short if fan speed is too low









<b>The DZ Co.</b>		Rev C1	Page 4 of 4
<b>100W Final</b>			
<b>B. Blood</b>			









# DZ COMPANY

LOVELAND, COLORADO

*UNIQUE ELECTRONIC EQUIPMENT IN KIT FORM*