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LE FORTY2, EMETTEUR-RECEPTEUR BLU COMPLET POUR LE 40M

Le Forty2 est basé sur le concept simple du Forty. De nouvelles fonctionnalités ont été ajoutées dont: un microcontrôleur gérant différentes fonctionnalités, comme un synthétiseur de fréquence, un affichage LCD, une bande passante BF ajustable, un compresseur de modulation, un RIT avec possibilité de trafic en Split, etc…
La puissance BF a été augmentée de façon à avoir une écoute confortable sur haut-parleur, même en ambiance bruyante. Bref, le Forty a évolué vers une station à part entière, et facile à exploiter dans toutes les circonstances.
La bande des 40 mètres a été choisie pour plusieurs raisons. Elle est pratiquement ouverte à toutes les heures de la journée et ceci toute l'année, on y contacte de nombreuses stations de l'hexagone, et elle aura prochainement un regain d'intérêt, lors de son extension programmée.

DESCRIPTION:
Il est utile de faire une mise au point avant toute description. Il n'est pas question ici de réaliser une émetteur-récepteur aux performances exceptionnelles rivalisant avec les stations commerciales les plus chères. Le Forty2 a été conçu pour pouvoir être réalisé facilement, avec des composants bon marché et disponibles à ce jour. Sa mise au point doit être simple, avec des outils courants. En plus, il est très agréable à utiliser, principalement à cause de son faible bruit à la réception, et à son filtre de bande très efficace sur les QRM (brouillages).

Caractéristiques principales (mesurées sur les prototypes):

Récepteur simple changement de fréquence (FI 4,9152 MHz) :
- sensibilité < 0,8 µV
- sélectivité 800 Hz à 4 KHz, par filtre du 8ème ordre, programmable.
- IP3 à +5dBm (signaux espacés de 20 KHz)
- réjection fréquence image > 50 dB
- atténuateur HF commutable et ajustable de – 3 à – 36 dB
- dynamique CAG 65 dB (globale + de 80 dB)
- puissance BF 2,5 watts sur 8 ohms

Emetteur:
- puissance HF 4 à 5 watts efficaces sur 50 ohms
- suppression harmoniques > 45dB (h2) et > 55dB (h3)
- IMD (2 tons) > 20dB
- taux de compression ajustable de 1/1 à 12/1
- réjection porteuse résiduelle > 35dB

Synthétiseur:
- couverture 2 ,085 à 2,385 MHz (7,000 à 7,300 MHz)
- pas de 10 – 1 – 0,1 KHz
- RIT (Split) sur toute la couverture (pas de 100 Hz)
- mémorisation décalage en fréquence suivant fréquence centrale des filtres à quartz
- mémorisation fréquence et modes à l'extinction

Consommations sous 13,8 volts :
- réception 150 mA en moyenne
- émission 1000 mA maximum

Le Forty2, pour bien séparer les fonctions, est réalisé en trois sous-ensembles :
- l'émetteur-récepteur,
- le synthétiseur avec les filtres BF et l'amplificateur BF,
- la face avant avec l'afficheur et le bar graphe.

Schéma synoptique :

Détails récepteur (schéma « board 1 », schéma « board 2b », et partie schéma « board 2a »):
Le signal issu de l'antenne, transitant par le filtre passe-bas de l'émetteur puis par le relais émission réception, est appliqué sur un filtre passe-bande à trois cellules. Le premier filtre accordé L3-CA1 est un filtre série. Puis deux filtres accordés parallèles L4-C4 et L5-C6, à très faible couplage (C5). Q1 est un transistor de commutation rapide (intégrant les résistances de base), commandé par le micro contrôleur 16F84, et permettant la mise à la masse de la résistance ajustable P1. Celle-ci règle le niveau d'atténuation d'entrée. IC1 (SA612) est un circuit oscillateur mélangeur à gain, qui mélange le signal utile d'entrée avec le signal issu du VCO du synthétiseur.

Les produits du mélange sont filtrés par le filtre à 4 quartz en échelle (X1 à X4), et ne subsiste que la fréquence de 4,9152 MHz. La bande passante de ce filtre est réglée à 4 KHz environ (à –6dB). L'ondulation de ce filtre est extrêmement faible. Q2 est un simple amplificateur FI, pour compenser la perte en insertion du filtre à quartz. IC2 (oscillateur mélangeur à gain SA612) est le détecteur de produit, c'est-à-dire qu'il mélange la FI (fréquence intermédiaire) à la fréquence du quartz X5, pour restituer la basse fréquence audible (BF). CA2 permet un ajustement précis de la fréquence de l'oscillateur à quartz (BFO) afin de centrer correctement le spectre BF utile par rapport au filtre à quartz. La tension d'alimentation des circuits IC1 et IC2 est fixée à 6,2 volts par la diode zener D1. La BF, issue de la sortie symétrique de IC2, est appliquée à l'entrée symétrique du préamplificateur BF (IC3-LM386). C19 sert à éliminer les résidus HF, C20 et C21 isolent les deux circuits en tension.
Le schéma du préamplificateur BF est très simple. C22 règle le gain de IC3 à sa valeur maximale (46 dB). Cette amplification est nécessaire pour avoir une tension de CAG (contrôle automatique de gain) conséquente. Le CAG est très simple mais néanmoins efficace. Voyons son fonctionnement : la tension continue interne, présente aux broches 1 et 2 des SA612, est normalement de 1,4 volts. Si on diminue cette tension, par une action extérieure, le gain des SA612 diminue également, allant jusqu'à une atténuation très forte. Pour générer cette tension de contrôle de gain, on prélève une partie du signal BF en sortie de IC3, on la redresse (D2), on règle la constantes de temps de retombée (C26, R8), et on applique cette tension continue au transistor Q3. Ce dernier joue le rôle de résistance variable entre les broches 1 et 2 de IC2 et la masse. R9 est une résistance de limitation. On a donc un pont diviseur variable constitué de la résistance interne à IC2 et de R9. La tension varie de 1,4 volts (sans signal) à 0,6 volts (signal maximum). Celle-ci est appliquée sur IC1 et également sur IC2, augmentant ainsi la dynamique de CAG, avec une légère différence de tension sur IC1 (R10) pour ne pas trop atténuer les signaux faibles. La self L6 sert à égaliser les tensions continues sur les broches 1 et 2 de IC2, tout en évitant à la HF d'être court-circuitée à la masse par C15.
La résistance ajustable P3 sert à ajuster le niveau BF pour ne pas saturer le circuit passe-bas IC16 (schéma « board 2b »). Trop de gain amènerait un taux de distorsion trop élevé. Le circuit (MAX293) utilisé ici est un filtre passe-bas à capacités commutées, elliptique, du 8ème ordre, avec d'excellentes performances. En effet, quel confort d'écoute quand on peut quasiment éliminer les signaux aigus de stations trop près de la fréquence écoutée. Ceci en BLU, mais aussi et surtout en CW, où ne persiste plus que la station écoutée, et ceci avec très peu de souffle. En plus, quelle que soit la largeur de bande choisie, il n'y a aucune déformation du signal, ni aucun son de cloche, comme dans la plupart des filtres. On peut comparer facilement la réception avec celle d'un récepteur équipé d'un filtre DSP BF. Le réglage de la bande passante se fait par variation de la capacité à la borne 1 de IC16, ce qui fait varier la fréquence de l'oscillateur interne du MAX293 déterminant la valeur de la bande passante. On aurait pu y placer une diode varicap avec une grande variation de capacité, style BB112, mais la solution adoptée ici est la commande par le microcontrôleur 16F84. Le microcontrôleur envoie ses instructions à IC12 (4094 sur schéma « board 2a »), lequel sélectionne les condensateurs adéquats C86 à C92 (mise à la masse par les transistors de commutation Q9 à Q15). L'alimentation de IC16 (6 volts) se fait au travers du régulateur IC15. La BF filtrée, disponible sur la broche 5 de IC16, est dirigée d'une part vers l'amplificateur de S'mètre(H9-1), après avoir été redressée par les diodes au germanium D14 et D15 et le niveau réglé par P9, d'autre part vers le potentiomètre de volume (Pot1).
L'amplificateur BF final (IC17) utilise un circuit LM380N, capable de délivrer plus de 2 watts sous 12 volts. Le signal est dirigé sur un connecteur pour haut-parleur externe (H13). Si rien n'est branché sur le connecteur externe, le haut-parleur interne est automatiquement mis en service (H12).

Détails émetteur (schéma « board 1 ») :

Le signal issu du microphone (de préférence un modèle dynamique basse impédance) est appliqué à l'entrée 4 de IC5. Le condensateur de découplage C31 est utile lors de l'utilisation d'un microphone haute impédance, et contre les retours HF. Le SSM2165-1 est un préamplificateur BF faible bruit, incorporant un compresseur de modulation et un réducteur de bruit ambiant. Le taux de compression est ajustable avec un rapport de 1/1 (sans compression) à 15/1. Le réglage se fait par variation de la résistance sur la broche 6 du circuit. 0 ohm correspond à un rapport de 1/1 et 250 Kohms à un rapport de 15/1. Sur notre circuit se trouve une résistance ajustable de 200 Kohms (P4). On peut donc faire varier le taux de 1/1 à 1/12. Mais il est inutile de dépasser 1/8, suffisamment efficace sans aucune distorsion. Le circuit fonctionnant exclusivement sous 5 volts, il a été ajouté un régulateur de tension (IC4).
P5 ajuste le niveau du signal avant injection sur la broche 1 de IC6 (SA612). C127 évite le déréglage du modulateur équilibré en fonction de la position de P5. IC6 est monté en modulateur équilibré, avec gain, générant le signal HF en DSB (double bande latérale avec réduction de porteuse) sur la broche 4. La fréquence de ce signal est déterminée par le quartz X6 de 4,9152 MHz. CA3 permet d'ajuster finement la fréquence du signal d'émission par rapport à celle de réception. P6 permet d'ajuster au maximum de réjection de porteuse. La bande latérale indésirable est supprimée par le filtre à 4 quartz faisant suite à IC6. Le signal du VCO (issu du synthétiseur), dont le niveau est ajusté par P2, est mélangé dans IC7 (SA612) au signal BLU issu du filtre à quartz. Seule la fréquence utile dans la bande des 40m est filtrée en sorties 4 et 5 de IC7 par le circuit résonant

parallèle L7-C48. La tension d'alimentation des circuits IC6 et IC7 est fixée à 6,2 volts par la diode zener D5. Les trois étages d'amplification amènent le signal utile à une puissance de près de 5 watts HF. L'étage Q4 est un amplificateur sélectif, alors que les deux étages suivants sont à large bande. Le transistor de puissance Q6 ayant entrée et sortie à très basse impédance, l'utilisation de transformateurs abaisseur (L9) et élévateur (L11) d'impédance a été adoptée pour un transfert d'énergie maximum. La diode D6 et la résistance R22 fixent, au travers de la self d'isolement HF L10, la tension de polarisation de base du transistor Q6 à 0,7 volts pour un fonctionnement de cet étage en classe AB linéaire. Une partie infime de la HF est prélevée (C61, P7) et redressée (D7) pour l'indicateur de puissance. La sortie vers l'antenne se fait au travers du filtre passe-bas C3-L2-C2-L1-C1, afin de rejeter au maximum les harmoniques indésirables.

Détails synthétiseur (schéma « board 2a ») :

Deux circuits intégrés bon marché sont utilisés dans ce montage. Le circuit MC145170 est un synthétiseur à commande série, et le PIC 16F84 est un microcontrôleur programmable pilotant le synthétiseur, l'afficheur LCD, et quelques fonctions annexes. L'association de ces circuits ainsi qu'un bon programme permettent de réaliser des merveilles.
Les caractéristiques du synthétiseur sont intéressantes:
- synthétiseur à une seule boucle de phase aux pas de 100 Hz, 1 KHz et 10 KHz sélectionnables.
- RIT couvrant la totalité de la bande ce qui permet en plus de travailler en « split ».
- lecture de la fréquence sur un afficheur LCD 1 ligne de 16 caractères.
- correction de la fréquence d'affichage suivant la fréquence centrale du filtre à quartz utilisé, et ceci par programmation accessible à l'utilisateur à la mise sous tension.

Le VCO fonctionne sur une fréquence relativement élevée (conjointement avec un filtre de boucle à comparateur de phase), pour avoir des temps de verrouillage courts. Ce VCO est suivi d'un diviseur par dix pour fournir la fréquence utile.
Voyons le schéma de principe:
Nous nous limiterons à une description simple. L'ensemble est géré par le microcontrôleur IC8 (PIC 16F84), dont le programme a été spécialement écrit pour cette application. IC8 est synchronisé à 4 MHz par X11, C80, C81. L'ensemble R34, R35, C82 et D12 forme le circuit de "reset".
La sélection de la fréquence se fait à l'aide d'un encodeur classique, sur les bits RB0 (interruption) et RB1. R36-C84 et R37-C83 forment un circuit anti-rebond.
Le bit RB6 reçoit les commandes de sélection de "pas" (100 Hz, 1 KHz ou 10 KHz) et de mise en service de l'atténuateur, le bit RB7 la sélection du mode "RIT" et des valeurs de filtres, et le bit RA2 la détection "PTT" (passage en émission). L'anti-rebond de ces commandes est géré par le programme.
IC9 (MC145170-2) est un circuit synthétiseur à commande série. IC8 envoie sous forme série les ordres à IC9 via les bits RA1 (vers Data), RB2 (vers Clock) et RA4 (vers Enable). A noter que par manque de bits, il a fallu multiplexer RB2 (par Q8) avec l'affichage.
En même temps IC8 envoie les ordres à l'afficheur LCD en mode 4 bits. Les bits RB2 à RB5 fournissent les datas, le bit RA1 la sélection commande ou données, et RA0 la validation. Les bits RA3, RB3 et RB4 permettent de commander IC12 (registre à décalage 8 bits 4094), pour la commutation des condensateurs du filtre passe bas BF, et pour la commande atténuateur.
R30 limite le courant pour le rétro éclairage. P8 permet de régler le contraste et C78 découple l'alimentation de l'afficheur LCD. Les résistances R31 à R33, R38, R39 et R41 sont des résistances de "pull up" (maintien au niveau haut).
La fréquence de référence du synthétiseur est de 12 MHz (X12, C95, C96 et CA5). CA5 affine la fréquence de référence. C93 et C94 découplent IC9 et la diode Led D13 permet de visualiser le verrouillage du synthétiseur.
IC11 (TL071) compare la phase des signaux issus en R et V de IC9 et fournit la tension de commande nécessaire au VCO. R45 à R50 , C97 à C99 et C101 constituent les éléments du filtre de boucle. Le filtre passe-bas (R51, R52 et C102, C103) élimine tout résidu de bruit indésirable.
Le VCO est architecturé autour du transistor FET faible bruit Q7. L12, CA4 et les diodes varicap D8-D9 déterminent la fréquence d'oscillation. D10 maintient un niveau d'oscillation constant. La diode zener D11 détermine et régule la tension d'alimentation de l'oscillateur et du comparateur de phase. Une partie du signal prélevée sur le "drain" de Q7 est injectée en 4 de IC9 (mesure de la fréquence par le synthétiseur). Sur la "source" de Q7 est prélevé le signal qui sera divisé par dix dans IC10 (diviseur sinus MC12080). A la sortie de ce circuit se trouve la fréquence utile, dont les harmoniques ont été réduites par le filtre passe-bas L13, C70, C71. IC13 et IC14 sont des régulateurs de tensions.

Détails face avant (schéma « board 3 ») :

Le circuit de la face avant ne comporte que peu d'éléments. Il sert de support à l'afficheur LCD avec ses condensateurs de découplage (C118 et C119). Y sont également fixés les boutons poussoirs et l'encodeur rotatif. C123 et C124 sont des condensateurs anti rebonds.

IC18 (LM3914) est un circuit de commande de rampe de diodes Led. Le nombre de diodes allumées est fonction de la valeur de la tension sur la broche 5. En ôtant le cavalier sur S3, il n'y a qu'une diode à la fois qui s'allume, cela permet de moins consommer de courant. IC20 est un régulateur de tension, le 4094 fonctionnant sous 5 volts.

MONTAGE:
Les platines doivent être montées avec grand soin si l'on veut que l'appareil fonctionne du premier coup. Les circuits imprimés ont été réalisés de façon à avoir le meilleur plan de masse possible, essentiel en montages HF. De ce fait, les espaces entre pistes et masse sont très restreints, et, si vous réalisez vous-même le circuit, l'utilisation d'un fer à souder à température régulée et à panne ultra fine est indispensable, sinon gare aux faux contacts. Même remarque pour les composants CMS. Sinon, l'ARTRA fournit les circuits imprimés avec vernis épargne, évitant les courts-circuits lors du soudage. En plus, les composants CMS y sont soudés d'avance.
Bien vérifier les composants et leurs emplacements. Souder au plus court. Les selfs à bobiner seront réalisées suivant les schémas. Ne pas oublier les straps sur la platine du synthétiseur. Les liaisons avec l'afficheur et les commandes en face avant se feront avec du petit câble plat, c'est plus propre. Les liaisons BF et HF se feront avec du petit câble blindé. Le condensateur C125 est à souder directement sur la prise micro. Voir le schéma d'interconnections.
Ne pas oublier le radiateur de Q6, le transistor dégageant pas mal de chaleur. Idem pour la graisse silicone entre le transistor et le radiateur, ainsi qu'entre la diode D6 et le radiateur. D6 assure ainsi la protection thermique de Q6, en évitant l'emballement de ce dernier.
Des trous sont prévus sur le circuit pour relier les filtres à quartz à la masse. Mais ceci n'est pas indispensable. Les pattes 1 (émetteurs) des transistors Q9 à Q15 doivent être reliées entre elles par un fil de masse. Cette façon de procéder simplifie l'implantation de ces composants.
Il est également préférable de faire arriver les fils de liaisons entre les platines, côté soudure. Cela fait plus propre.
L'afficheur doit être rapproché au maximum du circuit imprimé (les pattes noires de l'afficheur reposant contre le circuit). Pour cette raison, les condensateurs C118 et C119 sont soudés côté cuivre de la platine de face avant. Pot1 est simplement vissé sur la platine, les fils étant reliés directement sur les pattes du potentiomètre. La prise micro et l'interrupteur marche arrêt sont fixés directement sur le boîtier, comme d'ailleurs les connecteurs antenne, audio et alimentation.
Les platines sont prévues pour être facilement intégrées dans le boîtier L640, disponible chez Dahms Electronic. La fixation est très simple et fonctionnelle (en cas de modifications ultérieures). La platine synthétiseur (board 2) se fixe sur les rails par des entretoises de 10mm de long, au plus près de la face arrière. La platine émetteur récepteur (board 1) se fixe sur la platine synthétiseur au moyen d'entretoises de 10mm de long. Les faces cuivrées tournées l'une vers l'autre (voir photos). Et les fils et câbles de raccordement seront placés entre les deux platines. La platine face avant se fixe tout naturellement sur la face avant du boîtier.
Il est fortement recommandé de se servir du schéma d'interconnections pour raccorder les différentes platines

REGLAGES:
Appareils nécessaires au réglage :
- charge fictive 50 ohms / 10 watts
- wattmètre, tos'mètre
- contrôleur universel
- fréquencemètre 30 MHz
- oscilloscope 40 MHz
- générateur HF (pas indispensable)

Avant toute mise sous tension, vérifier la valeur de tous les composants en place. Ne pas confondre les selfs moulées avec les résistances, et bien faire attention au code de repérage des condensateurs. Rechercher les faux contacts et les oublis de soudage.
Dans un premier temps, ne pas placer les circuits intégrés dans leur support. Brancher éventuellement une charge de 50 ohms / 10 watts dans la prise antenne.
Mettre sous tension et vérifier la présence des tensions continues régulées aux bornes des diodes zener et des régulateurs. Les valeurs sont indiquées sur les schémas dans les petites cases rectangulaires, et ne doivent pas être supérieures ou inférieures de plus de 5 % aux valeurs inscrites. Eteindre et mettre en place les circuits intégrés.

Réglage récepteur :
Prérégler P1, P3 et CA1 à mi-course, CA2 à un quart de la capacité totale.
Mettre sous tension. Après le temps d'initialisation, régler l'affichage sur 7.070.0. La valeur du pas se règle par appuis successifs sur le bouton poussoir « step ». Par un appui prolongé sur « filter » on affiche la valeur du filtre

en service. Le changement de valeur se fait au moyen de l'encodeur rotatif. Sélectionner 2.4 KHz. Valider par un appui bref sur « filter ».
Pot1 à mi-course, il doit y avoir du souffle dans le haut-parleur. Vérifier que l'atténuateur est hors service et régler CA1, L4 et L5 pour avoir le maximum de souffle. Reprendre ce réglage plusieurs fois pour avoir un maximum franc et unique. Parfaire éventuellement par la suite, soit au générateur HF, soit sur la réception d'une station faible.
La valeur de la résistance ajustable P1 détermine le niveau d'atténuation HF. Moins de résistance augmente l'atténuation. L'atténuateur est mis en service par un appui prolongé sur « attn ». La mise hors service se fait de la même façon. A régler le soir lorsque les signaux perturbateurs sont très puissants.
Le réglage du BFO (CA2) pour décoder la bande latérale inférieure (LSB), est fonction de la valeur de la fréquence de résonance des quartz. Et celle-ci est variable suivant les fabricants. C'est pourquoi il est impératif de prendre tous les quartz, X1 à X10, de la même série, du même fabricant. Pour le réglage de CA2, procéder comme suit : placer CA2 au maximum de valeur (CA2 fermé). Mesurer la fréquence d'oscillation sur la broche 7 de IC2. Noter cette fréquence. Ajouter la valeur de 1,8 KHz, et régler CA2 jusqu'à lire cette dernière valeur sur le fréquencemètre. Exemple : CA2 au maximum de valeur, fréquence affichée 4915,410 KHz. 4915,410 + 1,8 = 4917,210 KHz. Donc faire varier CA2 jusqu'à lire 4917,210 KHz sur le fréquencemètre. Pour les puristes, quelques compléments d'information : Pourquoi ajouter 1,8 KHz ? Ceci est la valeur centrale corrigée, de la largeur initiale du filtre à quartz. Pourquoi corrigée puisque la largeur calculée du filtre est de 4 KHz, et que cette valeur centrale devrait être de 2 KHz ? Le quartz résonne sur sa fréquence de résonance série avec une capacité en série de 30 pF. Comme CA2 (fermé au maximum) n'est que de 22 pF, les 200 Hz manquants correspondent aux 8 pF manquants.
Vérification du bon fonctionnement du CAG (contrôle automatique de gain) : Sans signal à l'entrée du récepteur, les tensions sur les broches 2 de IC1 et IC2 doivent être de 1,40 volts. Injecter un signal de 50 µV à l'entrée, la tension sur 2 de IC1 doit être voisine de 1,02 volts, et la tension sur 2 de IC2 doit être voisine de 0,88 volts. Les valeurs ne sont pas très critiques, il est par contre impératif que ces valeurs diminuent quand le niveau du signal à l'entrée augmente.
Vérifier le récepteur en branchant une antenne, et régler P3 pour qu'il n'y ait pas de distorsion sur les signaux audibles (normalement à mi course).
Réinjecter un signal de 50 µV à l'entrée, régler P9 pour allumer le bar graphe jusqu'à la huitième diode, correspondant à S9. Si le cavalier S3 est en place sur la platine face avant, toutes les diodes Led jusqu'à la valeur maximum s'allument. S3 ôté, seule la diode Led de la valeur maximale s'allume. Ce qui peut être utile lors de l'utilisation sur batterie.

Réglage du synthétiseur :
Le synthétiseur, s'il a correctement été monté, doit fonctionner dès la mise sous tension. Vérifier la Led D13. Si elle clignote, le synthétiseur n'est pas verrouillé. Régler CA4 jusqu'à avoir un éclat fixe de D6 (utiliser un tournevis non métallique). Pour être plus précis, avec un voltmètre branché en sortie 6 de IC11, régler CA4 pour avoir 2,53 volts pour une fréquence affichée 7.070.0. Passer en limite haute de la bande (7,300 MHz), puis basse (7,000 MHz) et vérifier que le synthétiseur reste vérouillé. Dans le cas contraire reprendre légèrement le réglage de CA4.
Il faut également vérifier l'exactitude de la fréquence affichée. Il faut comparer avec un autre récepteur étalonné, à affichage précis de la fréquence. Si la différence est inférieure à 100 Hz, l'ajustage précis se fait avec le condensateur ajustable CA5. Si la différence est supérieure à 100 Hz, il va falloir configurer IC8 pour lui indiquer la valeur de la correction. Pour ce faire, éteindre l'appareil puis le rallumer en appuyant simultanément sur le bouton poussoir « RIT ». L'afficheur LCD affiche « Shift +00.0 K ». A ce stade il faut rentrer la valeur du décalage en fréquence notée entre l'affichage du synthétiseur et celle du récepteur de référence. A l'aide de l'encodeur afficher ce décalage (au pas de 100 Hz). En appuyant sur le bouton poussoir «step » on choisit entre un décalage positif ou négatif. La mémorisation de la valeur choisie se fait en appuyant sur le bouton poussoir « RIT ». Faire des essais en comparant avec le récepteur étalon ou un générateur HF. Le décalage restera en mémoire et sera actif à chaque mise sous tension. Terminer en corrigeant avec CA5 pour être pile sur la bonne fréquence. C'est plus facile à faire qu'à expliquer.

Réglage de l'émetteur :
Le réglage de l'émetteur demande un peu plus d'attention.
Préréglages : P2, P4 et P5 au minimum (à fond dans le sens contraire des aiguilles d'une montre), P6 à mi course
Cavalier sur S1 et pas de cavalier sur S2, ce qui permet d'alimenter la totalité du récepteur en passant en émission, sans alimenter pour autant l'étage de puissance émission.
Brancher une charge fictive 50 ohms / 10 watts. Insérer un wattmètre tos'mètre.
Oscilloscope branché sur la broche 6 de IC7, régler P2 de façon à avoir un signal de 200 à 220mV crête à crête, valeur maximum admise par le SA612 pour ne pas générer de distorsions en sortie.

Appuyer sur la pédale du microphone. En agissant sur CA3, on entend le signal de la porteuse émission. Ajuster CA3 au battement nul entendu dans le récepteur du Forty2. En augmentant le gain micro avec P5, on s'entend parler. Attention à bien faire ce réglage pour ne pas être décalé en émission par rapport au correspondant. L'idéal est de mesurer la fréquence sur la broche 7 de IC6 et de régler CA3 sur la même fréquence que précédemment avec CA2 (4917,210 KHz dans notre exemple).
Enlever le cavalier placé sur S1 et le placer sur S2 (position du cavalier en fonctionnement normal).
P5 à fond dans le sens contraire des aiguilles d'une montre (gain micro à zéro), P6 à mi-course. Appuyer sur la pédale du microphone. Oscilloscope branché en parallèle sur la sortie antenne, visualiser le signal de résidu de porteuse. Régler P6 au minimum de signal. Sans relâcher la pédale du microphone, prérégler L7 et L8 au maximum de signal.
Augmenter la valeur de P5 tout en sifflant dans le microphone. Le signal doit augmenter sur le wattmètre jusqu'à atteindre une valeur maximum entre 3 et 5 watts HF. Ne pas trop pousser ce réglage, la qualité de la modulation en dépend. Si l'aiguille du wattmètre dévie jusqu'à 5 watts sur un coup de sifflet, elle ne doit pas dépasser 2 watts en parlant normalement. Pas de crainte, la puissance crête est bien de 5 watts !
Le transistor Q6 est un transistor HF à grand gain. Ceci est intéressant pour pouvoir sortir 5 watts avec un minimum d'étages d'amplification, mais peut aussi amener ce transistor à auto-osciller. Si tel est le cas, placer un condensateur de 10 nF en série avec une résistance de 1 K entre base et collecteur de Q6, câblés sous le circuit et au plus court. Au contraire, si le montage d'origine n'auto-oscille pas, on peut essayer de remplacer R23 et R24 par des straps, ce qui permettra de sortir le maximum de puissance HF (comme sur mes prototypes).
Pour le réglage du compresseur de modulation, la meilleure position se trouve entre un quart et un tiers de la valeur de P4. A chacun de faire ses essais, mais attention à ne pas trop pousser !
Le bar graphe permet aussi d'afficher la puissance de sortie relative en émission. Régler P7 pour la déviation correspondant à celle du wattmètre de référence.

Bonne réalisation et bon trafic avec le Forty 2 !

Pour nous contacter : artra68@aol.com
Notre site : www.artra-qrp.com

LISTE DES COMPOSANTS:

Platine émetteur-récepteur (board 1)

R23, R24 : 1,5 ohms (brun-vert-or)
R6 : 10 ohms (brun-noir-noir)
R21, R11 : 47 ohms (jaune-violet-noir)
R1, R20 : 100 ohms (brun-noir-brun)
R5, R15, R18 : 470 ohms (jaune-violet-brun)
R2, R4, R9, R10, R19, R22 : 1 K (brun-noir-rouge)
R17, R61 : 4,7 K (jaune-violet-rouge)
R7 : 6,8 K (bleu-gris-rouge)
R12 : 22 K (rouge-rouge-orange)
R16 : 33 K (orange-orange-orange)
R8 : 47 K (jaune-violet-orange)
R13, R14 : 220 K (rouge-rouge-jaune)
R3 : 510 K (vert-brun-jaune)
P3 : mini ajustable à plat 1 K
P1, P2, P5 : mini ajustable à plat 4,7 K
P7 : mini ajustable à plat 22 K
P6 : mini ajustable à plat 50 K
P4 : mini ajustable à plat 220 K
C61 : 1,5 pF (1p5)
C5 : 2,2 pF (2p2)
C11, C13, C42, C44 : 27 pF (270 ou 27p)
C12, C43 : 47 pF (470 ou 47p)
C9, C17, C18, C40, C41, C53 : 100 pF (101)
C4, C6, C48, C50 : 150 pF (151)
C1, C3 : 470 pF (471)

C2, C31, C33, C49 : 1 nF (102)
C7, C10, C14, C45, C47, C52, C55, C57, C127 : 10 nF (103)
C126 : 47nF (473)
C8, C15, C16, C19, C20, C21, C23, C24, C28, C29, C30, C36, C38, C39, C46, C51, C54, C59, C60 : 100 nF (104)
C37 : 220 nF (224)
C56 : 2,2 µF tantale
C26, C35 : 2,2 µF chimique radial
C22, C58 : 10 µF tantale
C32, C34 : 22 µF chimique radial
C25 : 47 µF chimique radial
C27 : 100 µF chimique radial
CA2, CA3 : 22 pF ajustable vert 7mm
CA1 : 80 pF ajustable rouge 10mm
IC1, IC2, IC6, IC7 : SA612 ou NE612
IC3 : LM386
IC4 : 78L05
IC5 : SSM2165-1 (CMS)
Q1 : DTC114
Q2 : BC548C
Q3 : 2SC1841
Q4 : 2N2222A
Q5 : 2SC2053
Q6 : 2SC1971 avec radiateur adapté (plus graisse silicone)
D1, D5 : zener 6,2v
D2, D3, D4 : 1N4148
D6 : 1N4007
D7 : 1N60
X1 à X10 : quartz 4915 KHz
L1, L2 : 13 spires fil émaillé 0,5mm sur tore T50-2
L3 : self moulée 15 µH axiale (brun-vert-noir)
L6 : self moulée 100 µH axiale (brun-noir-brun)
L4, L5, L7, L8 : selfs Néosid 5164
L9 : 5 spires deux fils émaillés 0,5mm en parallèle sur ferrite 2 trous BN43-202
L10 : self de choc VK200 entièrement bobinée avec sorties radiales
L11 : 10 spires deux fils émaillés 0,5mm torsadés sur tore FT50-43
RL1 : relais 12 volts 2RT
Cinq supports DIL8 (tulipe)
Deux supports cavaliers et un cavalier

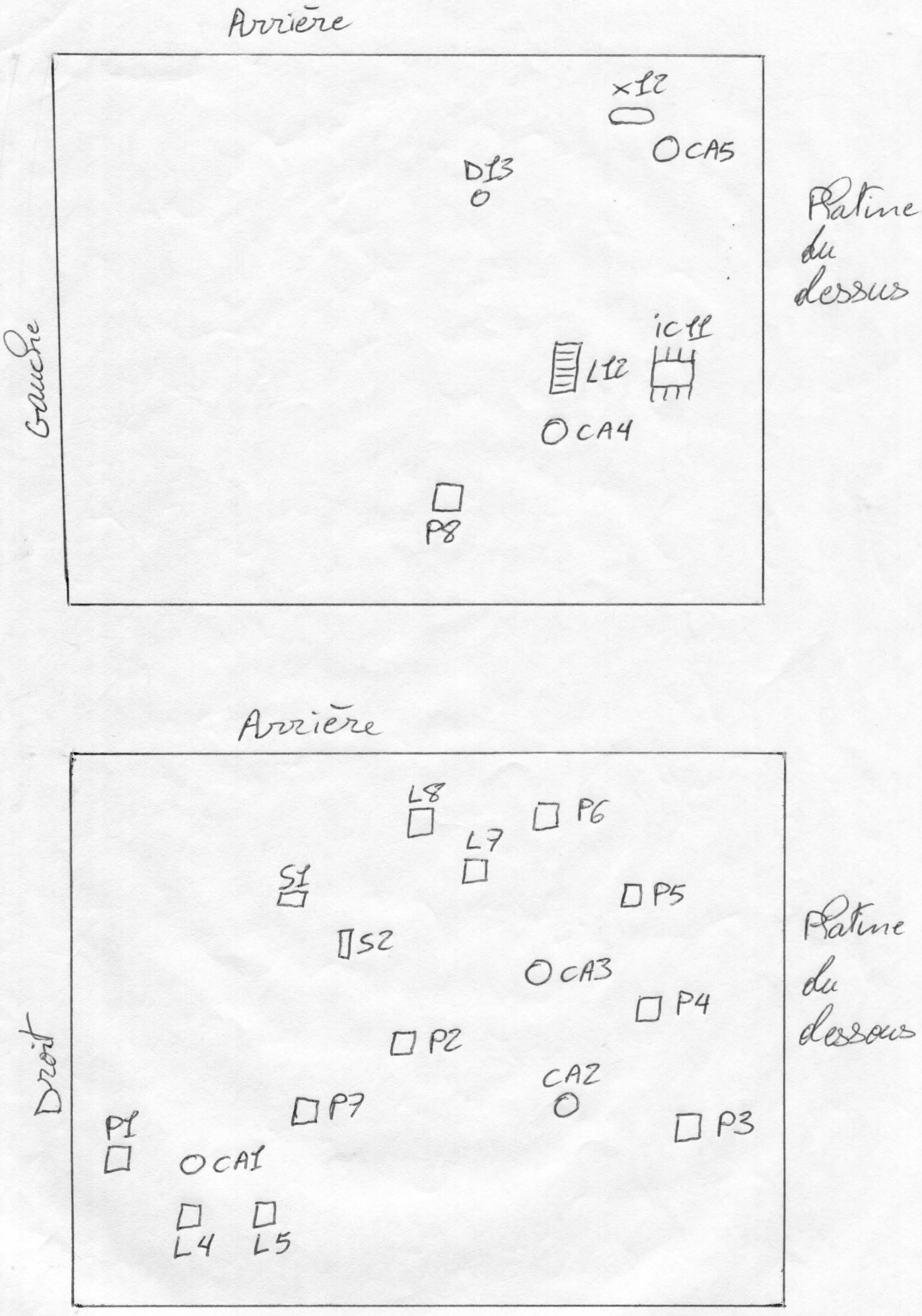
Platine synthétiseur et filtres BF (board 2)

R59 : 10 ohms (brun-noir-noir)
R30 : 15 ohms (brun-vert-noir)
R54 : 100 ohms (brun-noir-brun)
R28 : 220 ohms (rouge-rouge-brun)
R26, R27 : 330 ohms (orange-orange-brun)
R35 : 470 ohms (jaune-violet-brun)
R44 : 560 ohms (vert-bleu-brun)
R29 : 820 ohms (gris-rouge-brun)
R36, R37, R51, R52 : 1 K (brun-noir-rouge)
R41 : 2,2 K (rouge-rouge-rouge)
R31, R32, R33, R34, R38, R39, R40, R42, R55, R56, R57, R58 : 10 K (brun-noir-orange)
R53 : 12 K (brun-rouge-orange)
R49, R50 : 47 K (jaune-violet-orange)
R45, R46, R47, R48 : 56 K (vert-bleu-orange)
R25 : 100 K (brun-noir-jaune)
R43 : 1 M (brun-noir-vert)
P8 : mini ajustable à plat 10 K
P9 : mini ajustable à plat 470 K

C67 : 3,3 pF (3p3 ou 339)
C63, C64 : 33 pF (330)
C86, C95 : 47 pF (470)
C80, C81, C96 : 56 pF (560)
C87 : 82p (820)
C62, C66 : 100 pF (101)
C88 : 120p (121) + 15p (150)
C89 : 150p (151)
C70 : 180 pF (181)
C90 : 220 pF (221)
C91 : 390 pF (391)
C71 : 470 pF (471)
C92 : 680 pF (681)
C68, C109 : 1 nF (102)
C72 : 2,2 nF (222)
C93, C114 : 10 nF (103)
C97, C98 : 15 nF (153)
C65, C69, C73, C74, C75, C77, C79, C82, C83, C84, C85, C105, C106, C107, C108, C113, C116 : 100 nF (104)
C99, C101 : 220 nF (224)
C110 : 330 nF (334)
C104, C111 : 680 nF (684)
C102, C103 : 1 µF non polarisé
C112 : 1 µF chimique radial
C115 : 4,7 µF chimique radial
C76, C78, C94, C100 : 47 µF chimique radial
C117 : 220 µF chimique radial
CA4, CA5 : ajustable 10 pF
IC8 : PIC 16F84 programmé
IC9 : MC145170-2
IC10 : MC12080
IC11 : TL071
IC12 : 4094
IC13 : 78L05
IC14 : 78M05 (CMS)
IC15 : 78L06
IC16 : MAX293
IC17 : LM380-14
Q7 : 2SK937
Q8 : 2SA933
Q9 à Q15 : DTC114
D8, D9 : 11EQS04
D10, D12 : 1N4148
D11 : zener 10v
D13 : Led 3mm
D14, D15 : 1N60
X11 : quartz 4,000 MHz
X12 : quartz 12,000 MHz
L12 : 15 spires fil émaillé 0,5mm sur tore T37-6
L13 : self moulée 15 µH (brun-vert-noir)
Deux supports DIL8 (tulipe)
Un support DIL14 (tulipe)
Deux supports DIL16 (tulipe)
Un support DIL18 (tulipe)
Fichier hexa pour 16F84 téléchargeable sur nos sites

Platine face avant (board 3)

R60 : 3,3 K (orange-orange-rouge)
C119, C120, C122, C123, C124 : 100 nF céramique multicouche (104)
C121 : 47 µF chimique radial
C118 : 100 µF chimique radial
IC18 : LM3914
IC19 : bar graphe 10 Led
IC20 : 78M05 (CMS)
Pot1 : potentiomètre logarithmique 10KB
Pb1, Pb2 : boutons poussoirs 2 circuits pour circuit imprimé type D6
Un encodeur rotatif pour circuit imprimé
Un afficheur LCD 1 ligne de 16 caractères LTN114 (CMC116L01)
Un support cavalier et un cavalier.


Arrière
Gauche
Platine du dessus
L12
IC11
CA5
D13
CA4
P8
Arrière
Droit
Platine du dessous
L8
P6
L7
S1
P5
S2
CA3
P4
P2
CA2
P7
P1
P3
CA1
L4
L5

Forta 2 réglages de maintenance.

CA1 + L4 + L5 = filtre passe-bande réception HF (platine du dessous).

CA2 = BFO (platine du dessous). Réglage très pointu.

CA3 = calage de la fréquence d'émission (platine du dessous). Réglage très pointu.

CA4 = VCO, fonctionne avec la LED D6 à l'intérieur (platine du dessus).

CA5 = correspondance de l'affichage de fréquence avec la fréquence réelle, avec la fonction Shift (platine du dessus), près du quartz 12 MHz du MC145170.

IC11 = TL071 (réglage synthétiseur). Platine du dessus.

LED intérieur D13 = vérouillage VCO (platine du dessus).

P1 = atténuateur HF en réception (platine du dessus).

P2 = puissance HF de sortie VCO. NE PAS TOUCHER sinon réglage (platine du dessous).

P3 = CAG, pré-réglé à mis course (platine du dessous).

P4 = compresseur de modulation (platine du dessous).

P5 = gain microphone (platine du dessous).

P6 = réjection de porteuse LSB (platine du dessous). Réglage très pointu mais facile à faire.

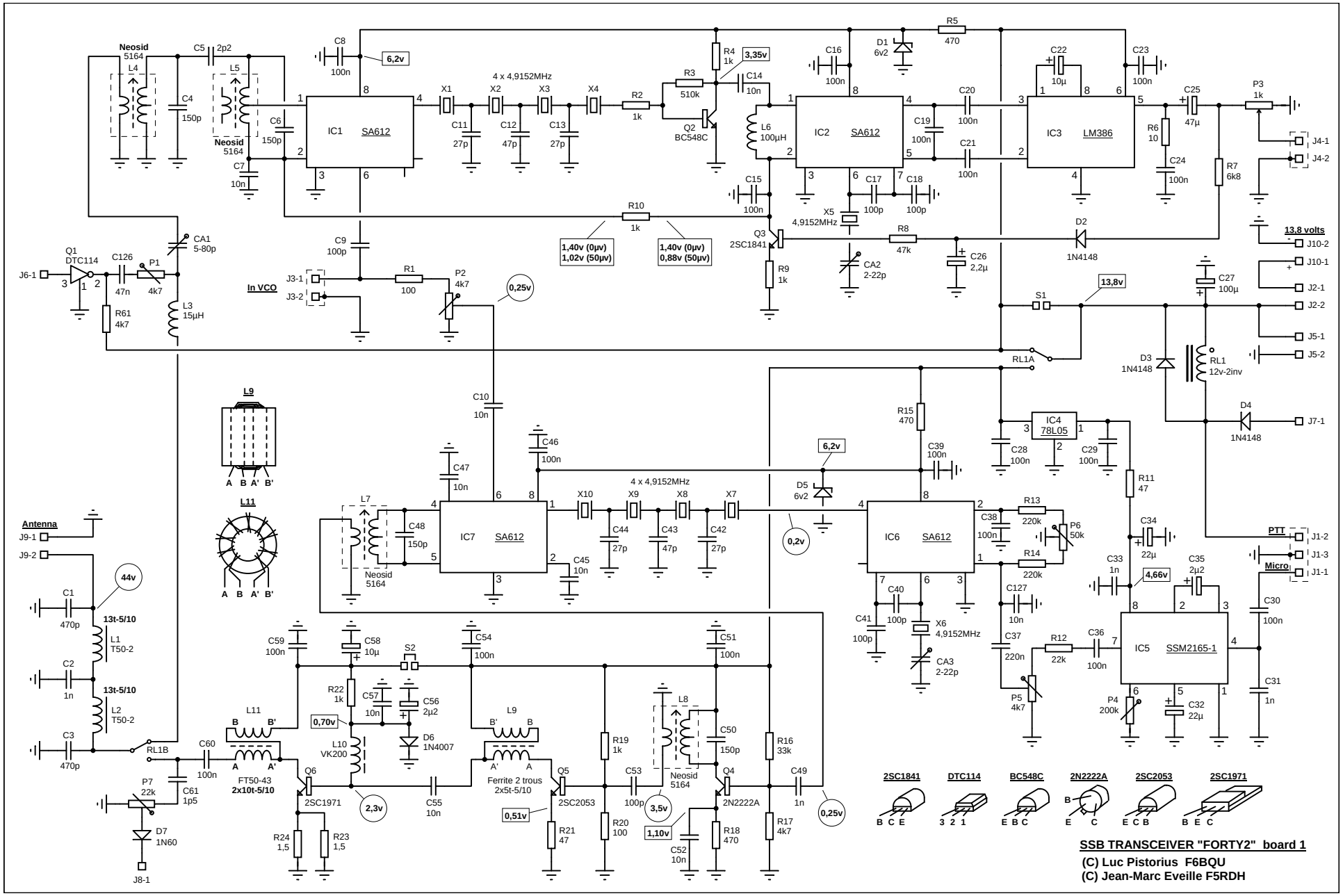
P7 = Wattmètre (platine du dessous, coté PA).

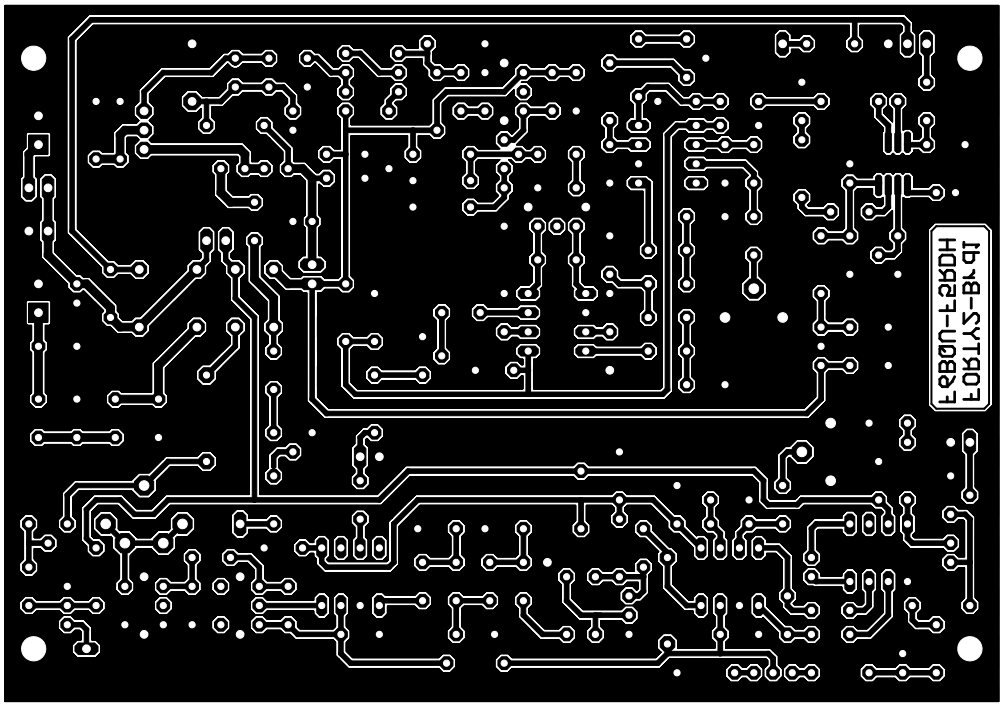
P8 = contrast de l'affichage (platine du dessus).

P9 = S-mètre (platine du dessus).

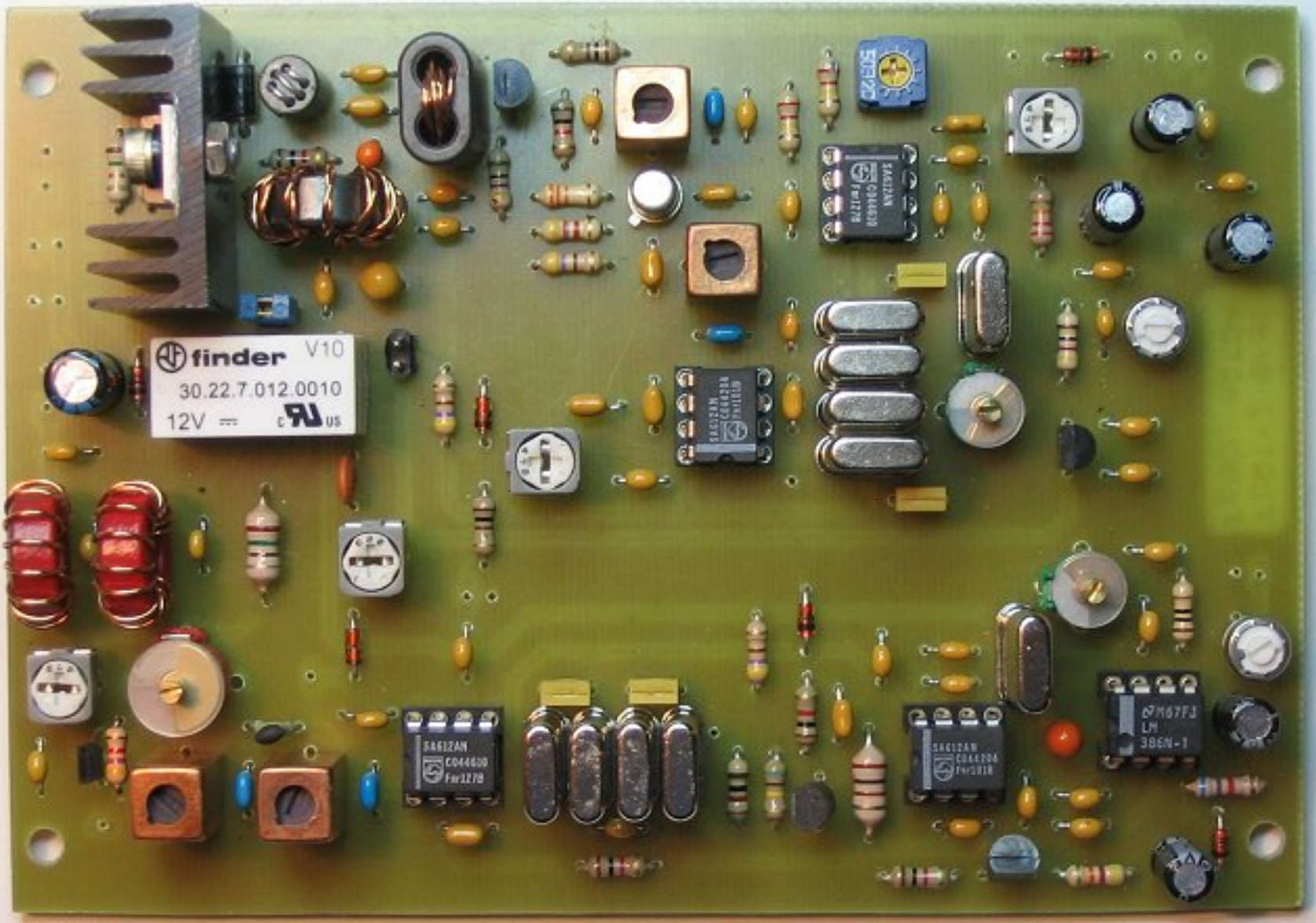
S1 + S2 = cavalier de réglage émission, S2 position normale (platine du dessous).

S3 = cavalier, fonctionnement du S-mètre (façade avant).

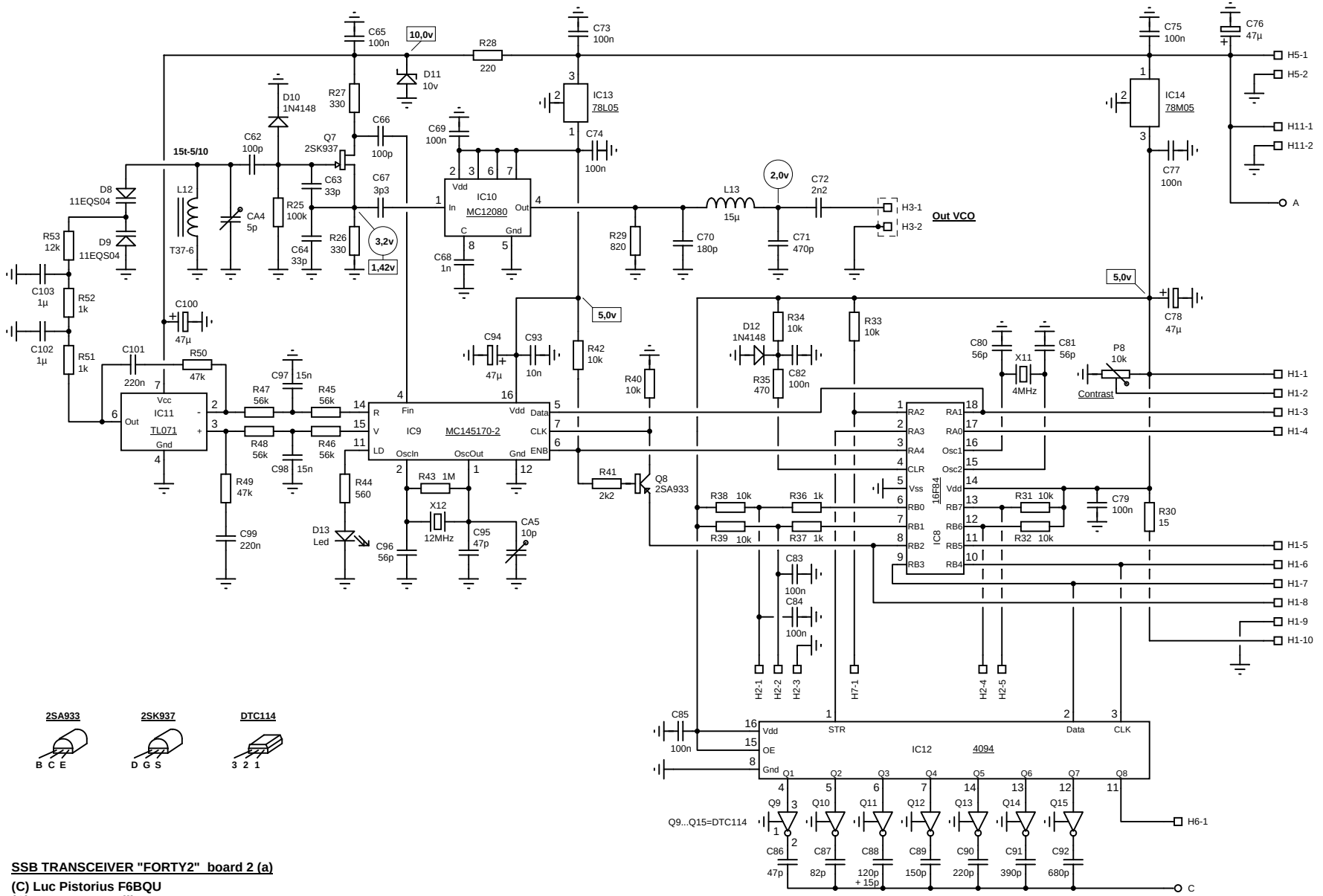

Neosid 5164
L4
C5 2p2
L5
C4 150p
C6 150p
C7 10n
C8 100n
6,2v
IC1 SA612
4 x 4,9152MHz
X1 X2 X3 X4
C11 27p
C12 47p
C13 27p
R2 1k
R3 510k
R4 1k
3,35v
C14 10n
Q2 BC548C
L6 100µH
C15 100n
C16 100n
D1 6v2
R5 470
IC2 SA612
C19 100n
C20 100n
C21 100n
C17 100p
C18 100p
X5 4,9152MHz
CA2 2-22p
R8 47k
C26 2,2µ
Q3 2SC1841
R9 1k
R10 1k
1,40v (0µv) 1,02v (50µv)
1,40v (0µv) 0,88v (50µv)
D2 1N4148
C22 10µ
C23 100n
IC3 LM386
C25 47µ
P3 1k
R6 10
C24 100n
R7 6k8
J4-1
J4-2
13,8 volts
J10-2
J10-1
J2-1
J2-2
J5-1
J5-2
C27 100µ
S1
13,8v
RL1A
D3 1N4148
RL1 12v-2inv
D4 1N4148
J7-1
Q1 DTC114
J6-1
C126 47n
P1 4k7
CA1 5-80p
L3 15µH
R61 4k7
C9 100p
In VCO
J3-1
J3-2
R1 100
P2 4k7
0,25v
L9
A B A' B'
L11
A B A' B'
C10 10n
C46 100n
C47 10n
L7
C48 150p
Neosid 5164
IC7 SA612
4 x 4,9152MHz
X10 X9 X8 X7
C44 27p
C43 47p
C42 27p
C45 10n
6,2v
D5 6v2
0,2v
R15 470
C39 100n
IC6 SA612
C38 100n
R13 220k
P6 50k
R14 220k
C40 100p
C41 100p
X6 4,9152MHz
CA3 2-22p
C127 10n
C37 220n
P5 4k7
R12 22k
C36 100n
IC4 78L05
C28 100n
C29 100n
R11 47
C34 22µ
C33 1n
4,66v
IC5 SSM2165-1
C35 2µ2
C30 100n
C31 1n
C32 22µ
P4 200k
PTT
Micro
J1-2
J1-3
J1-1
Antenna
J9-1
J9-2
44v
C1 470p
13t-5/10
L1 T50-2
C2 1n
13t-5/10
L2 T50-2
C3 470p
RL1B
C60 100n
P7 22k
C61 1p5
D7 1N60
J8-1
FT50-43
2x10t-5/10
C59 100n
C58 10µ
S2
C54 100n
C51 100n
R22 1k
C57 10n
C56 2µ2
0,70v
D6 1N4007
L10 VK200
Ferrite 2 trous 2x5t-5/10
L8
C50 150p
Neosid 5164
R19 1k
C53 100p
R16 33k
C49 1n
Q6 2SC1971
2,3v
C55 10n
Q5 2SC2053
0,51v
R21 47
R20 100
3,5v
1,10v
C52 10n
Q4 2N2222A
R18 470
R17 4k7
0,25v
R24 1,5
R23 1,5
2SC1841
DTC114
BC548C
2N2222A
2SC2053
2SC1971
B C E
3 2 1
E B C
E C
E C B
B E C
SSB TRANSCEIVER "FORTY2" board 1
(C) Luc Pistorius F6BQU
(C) Jean-Marc Eveille F5RDH


FORTY2-BRD
LEAD-FREE

F6BQU-F5RDH
FORTY2-Brd1

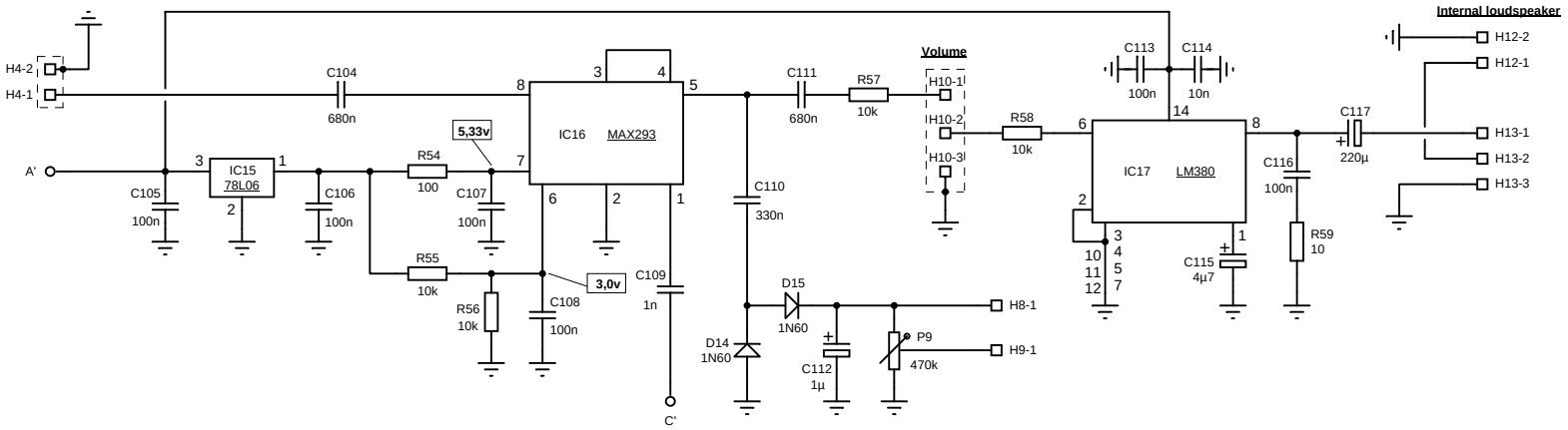


Forty2 - board 1

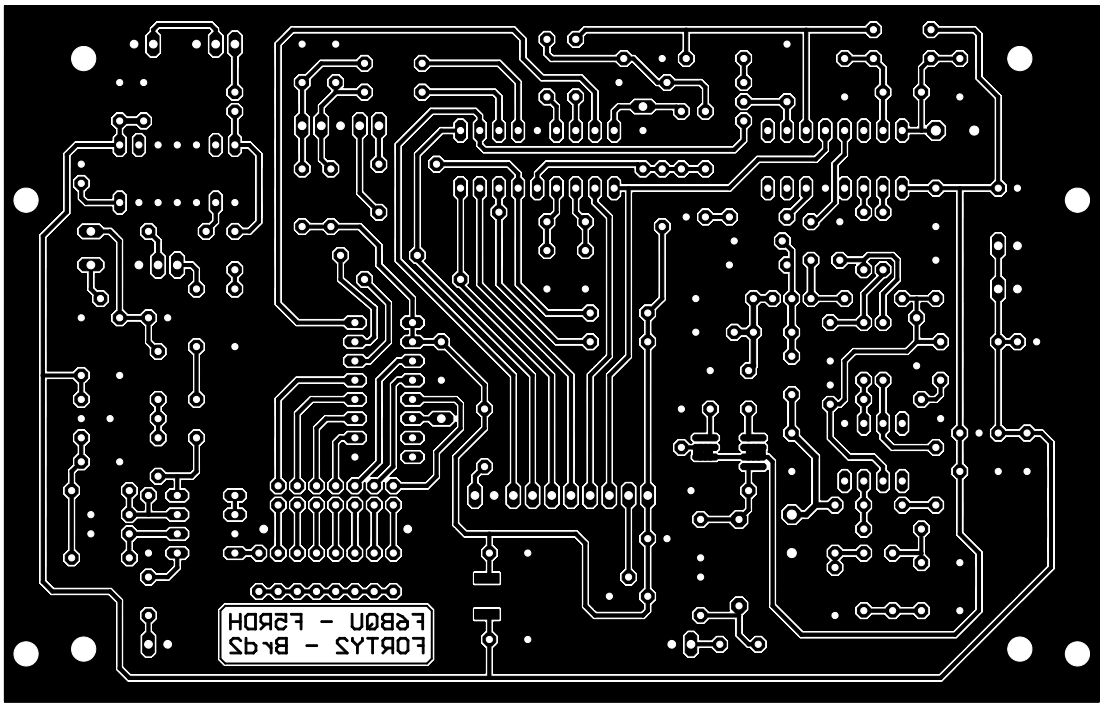


SSB TRANSCEIVER "FORTY2" board 2 (a)

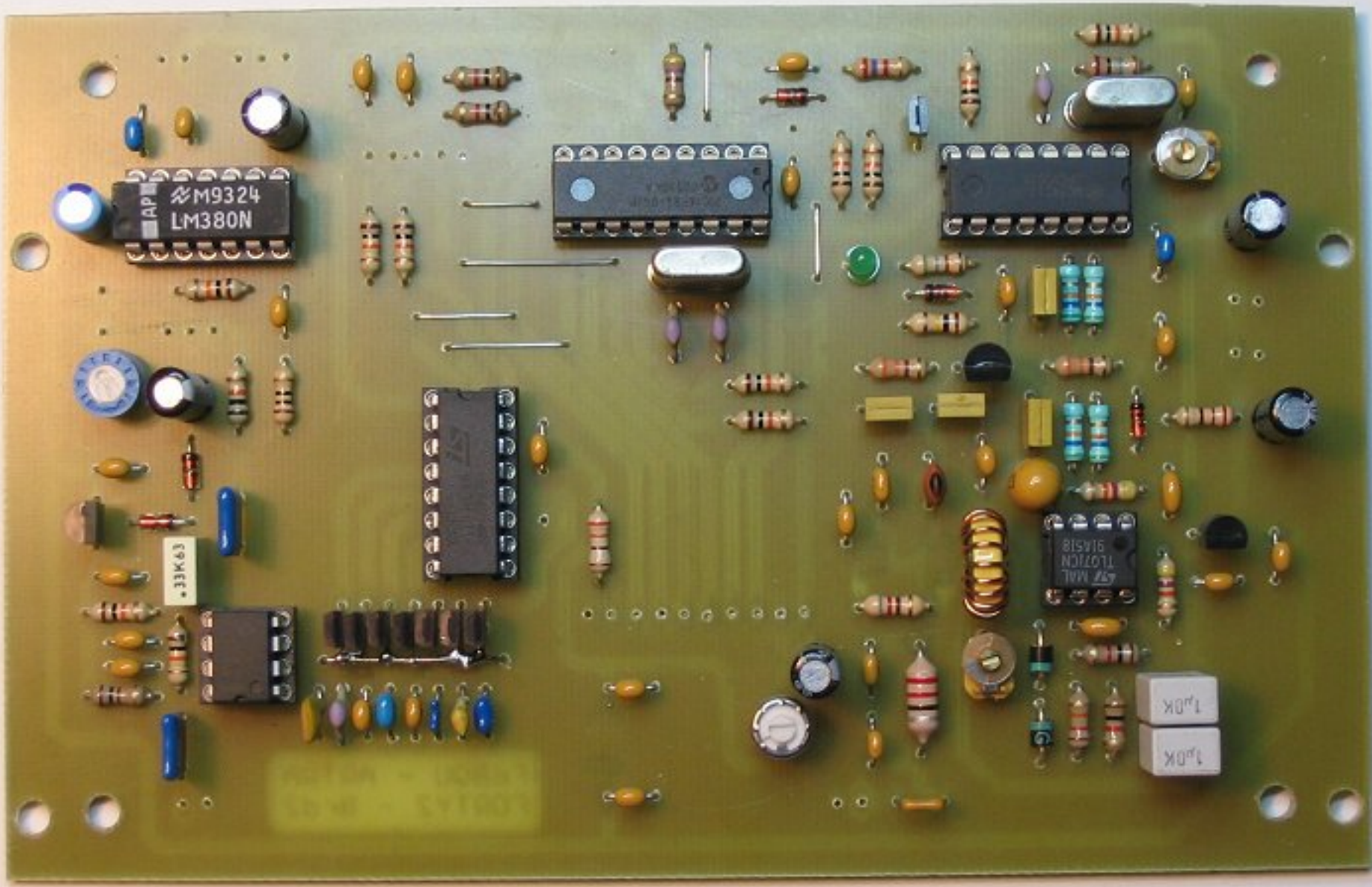
(C) Luc Pistorius F6BQU
(C) Jean-Marc Eveille F5RDH



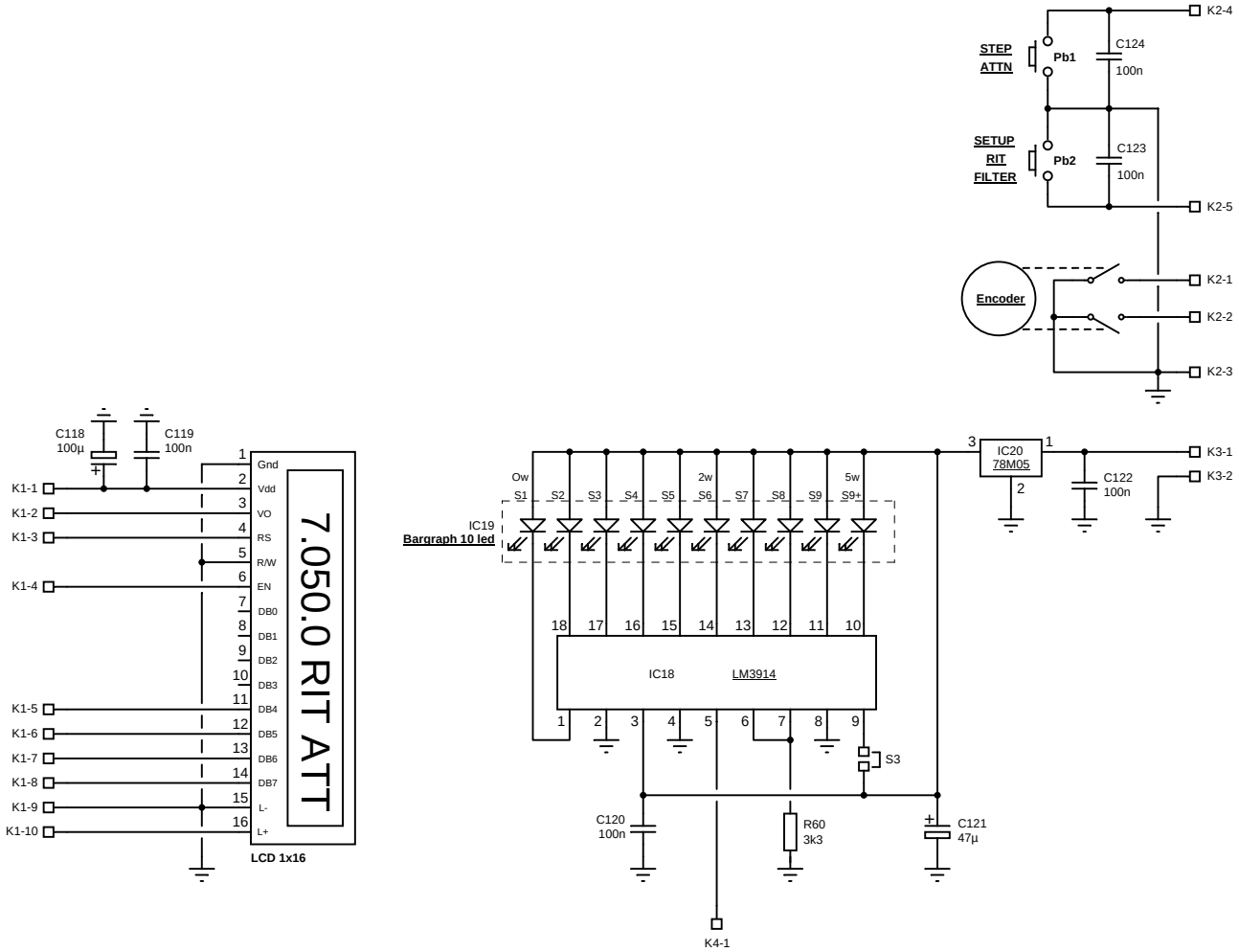
SSB TRANSCEIVER "FORTY2" board 2 (b)


F68DU - F5RDH
FORTY2 - Br4Z

H12
NF
C117
C114
C113
C115
IC17
H8
H9
H10
R58
C116
C112
P9
R57
R59
C105
D15
D14
IC15
C111
C110
C106
R55
C108
C107
R54
R56
IC16
C109
C104
H4
H2
R36
R37
C84
C83
R38
R39
Q9...Q15
C86
C87
C88
C89
C90
C91
C92
IC12
C85
H6
R30
H1
C77
IC14
C75
C78
P8
R35
C82
D12
H7
IC8
C79
R33
R34
X11
C81
C80
R31
R32
Q8
R41
R40
R42
R43
X12
C96
C95
IC9
CA5
C94
D13
R44
D10
R25
C66
C97
R45
R46
C93
H5
H11
Q7
R26
R27
C65
C64
C63
D11
R28
C98
R48
R47
C76
C68
C67
C62
C100
C69
IC10
L12
R49
C99
IC13
C73
IC11
C74
R50
R29
C101
D8
R51
C70
L13
CA4
C102
D9
R53
R52
C71
C103
H3
C72
F6BQU - F5RDH
FORTY2 -SYBrd2

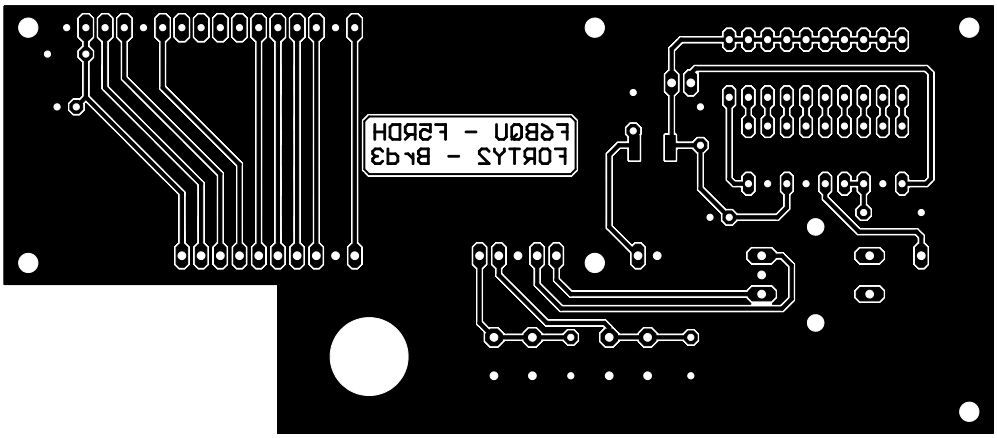


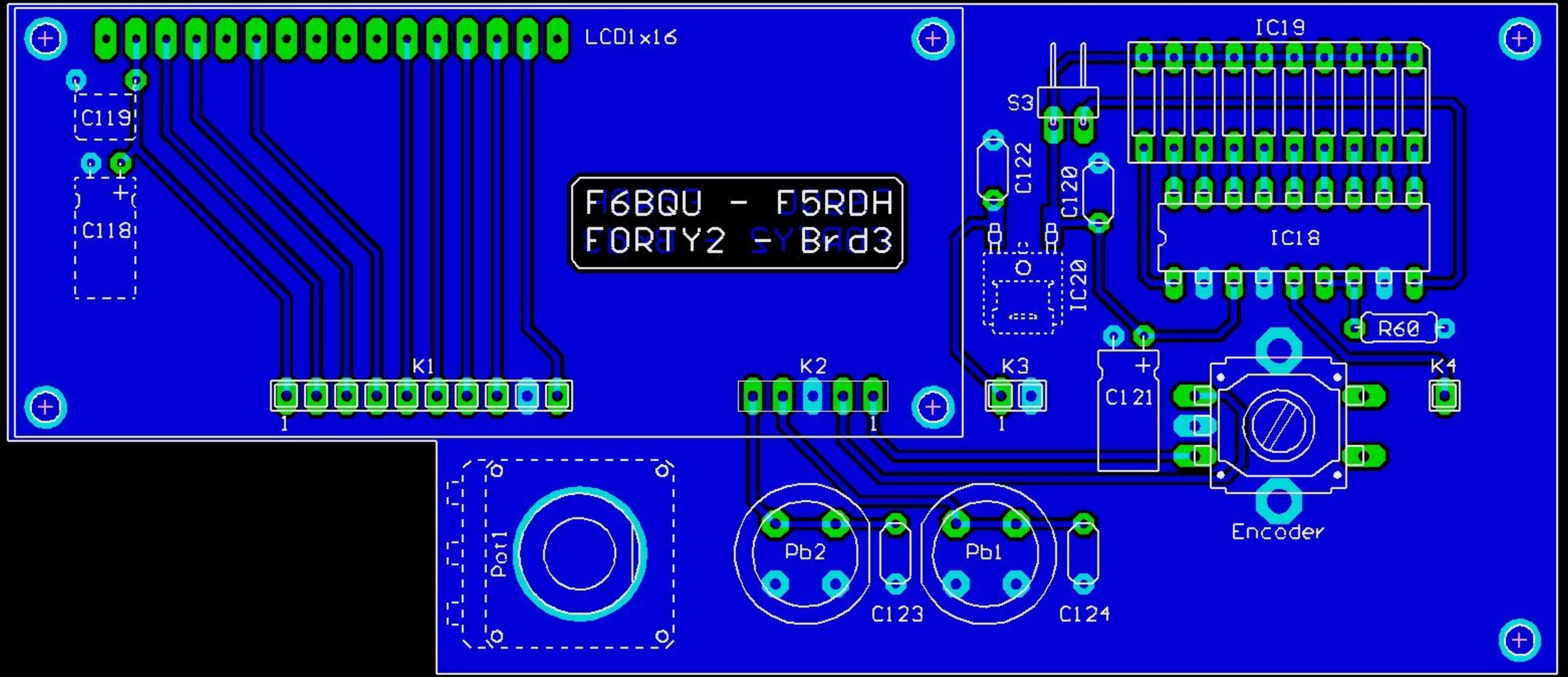
Forty2 - board 2

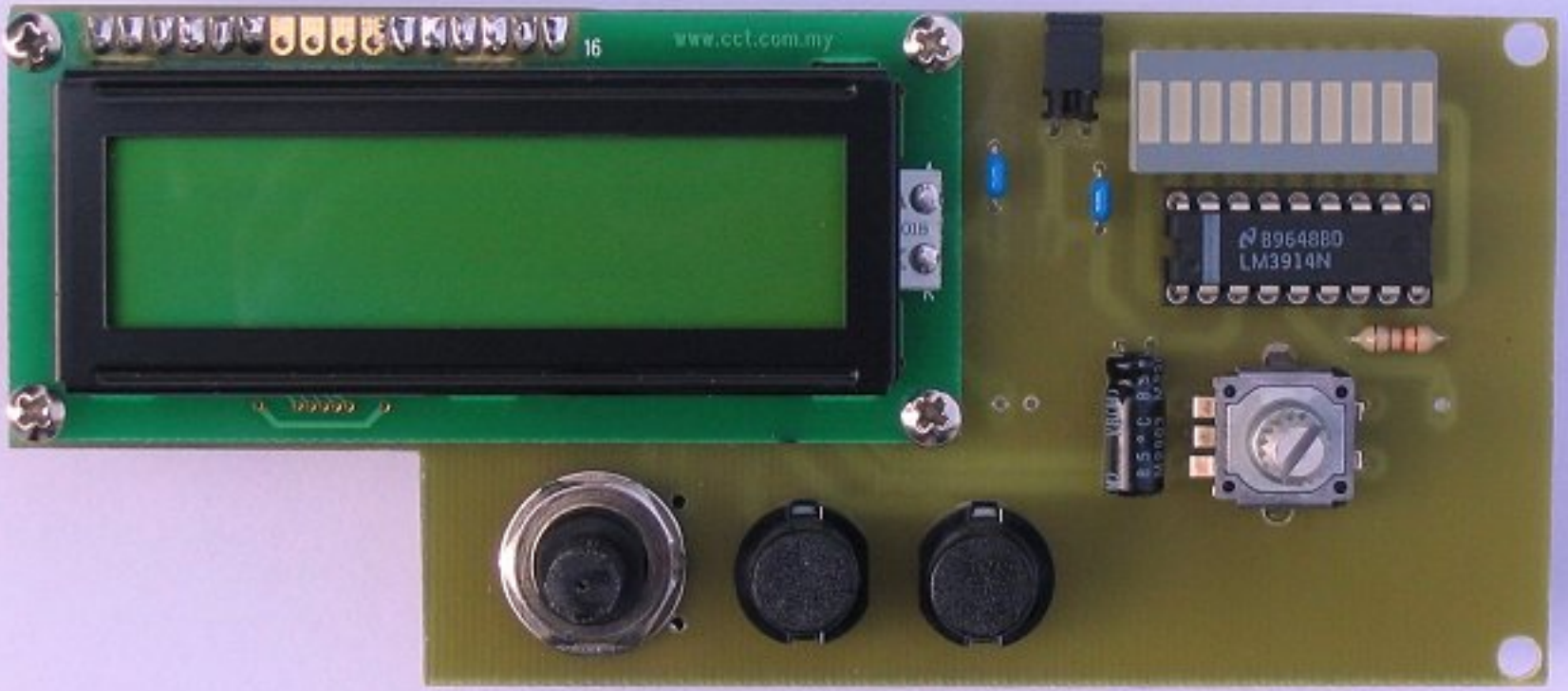


SSB TRANSCEIVER "FORTY2" board 3

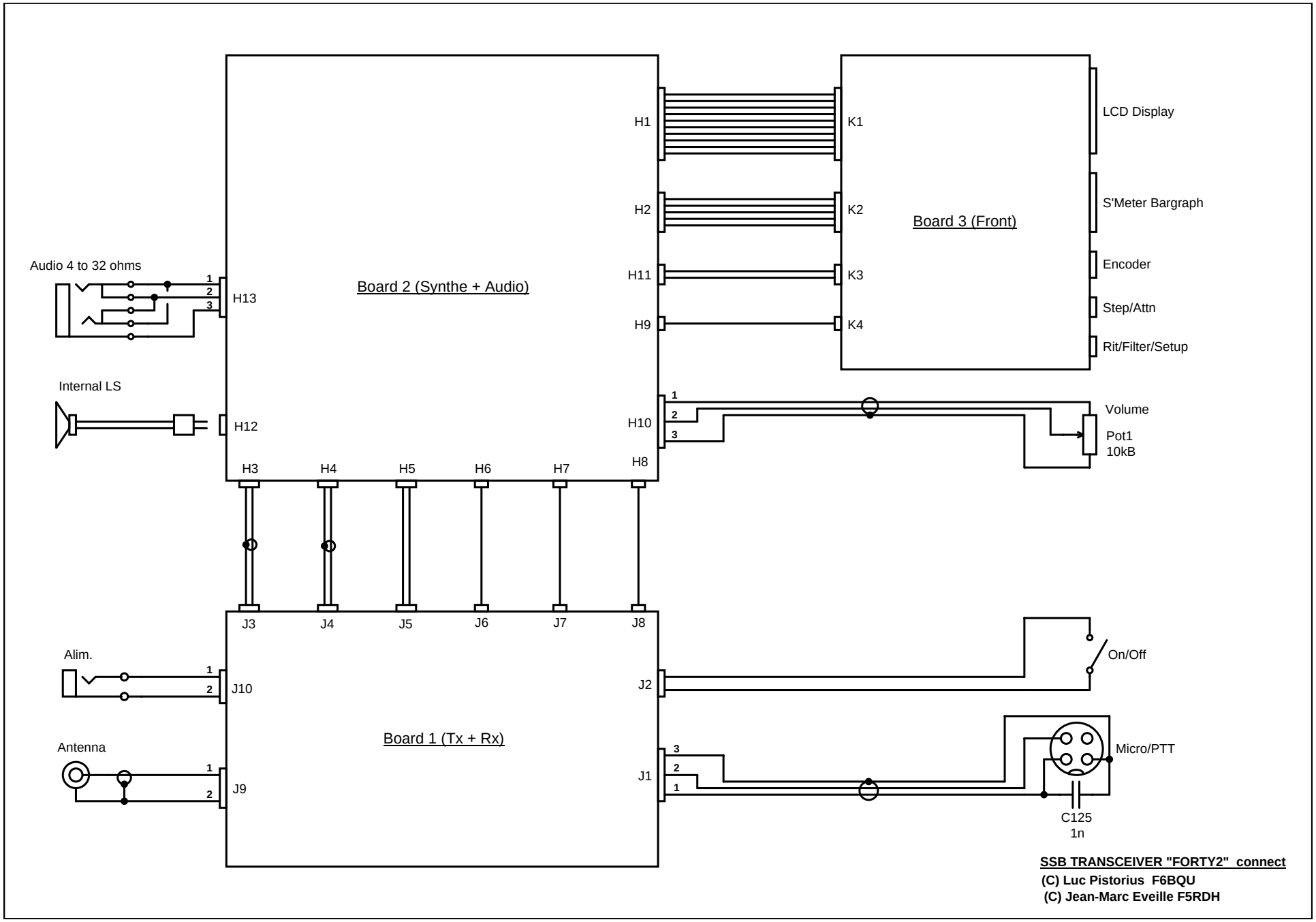
(C) Luc Pistorius F6BQU
(C) Jean-Marc Eveille F5RDH

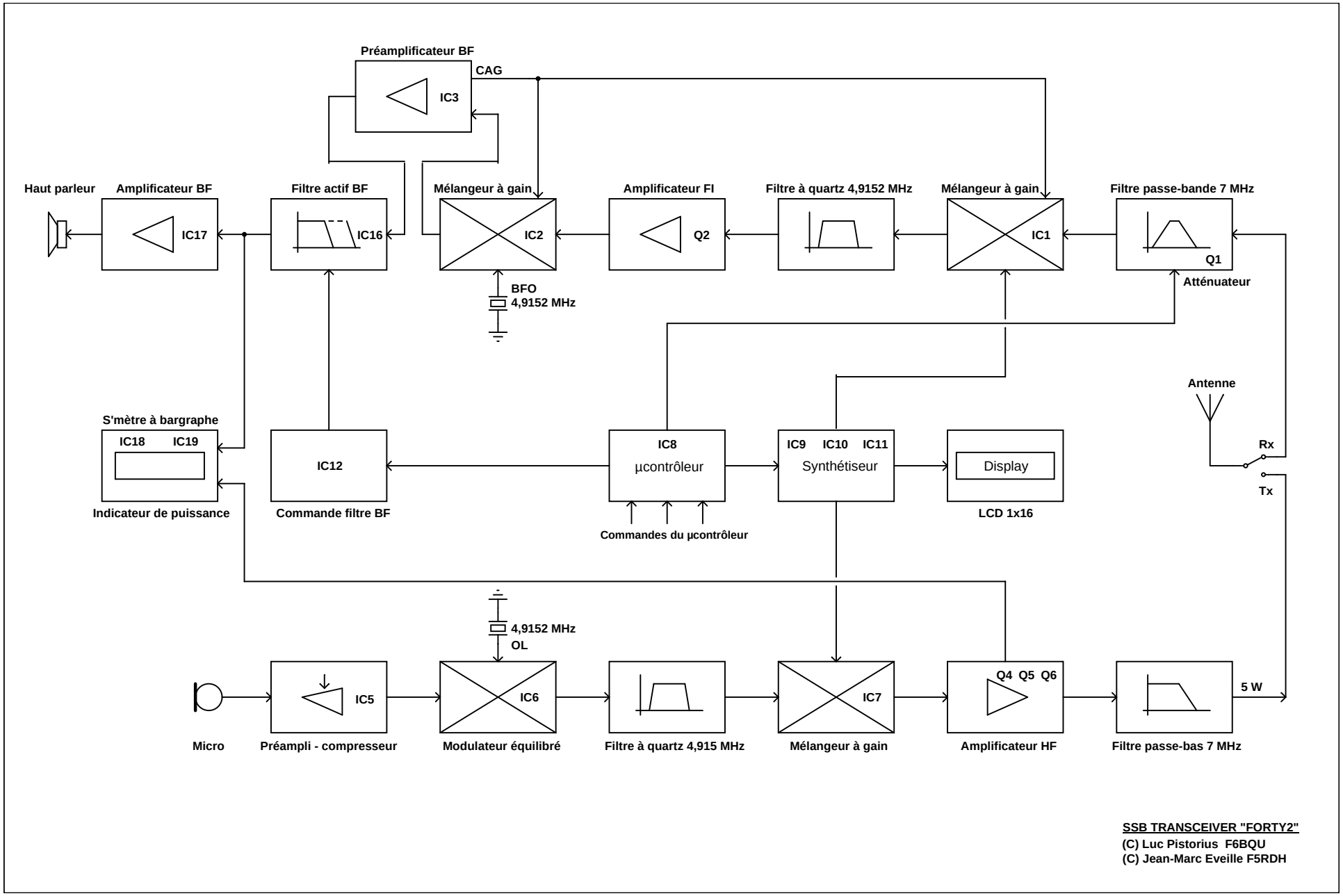

F6B0U - F5RDH
FORTY2 - Brd3


LCD1x16
C119
C118
F6BQU - F5RDH
FORTY2 - Brd3
K1
K2
K3
K4
S3
IC19
IC18
IC20
C122
C120
C121
R60
Encoder
Pb2
Pb1
C123
C124
Pot1



Forty2 - board 3


Board 2 (Synthe + Audio)
Board 3 (Front)
Board 1 (Tx + Rx)
H1
H2
H11
H9
H10
H8
H3
H4
H5
H6
H7
H13
H12
K1
K2
K3
K4
LCD Display
S'Meter Bargraph
Encoder
Step/Attn
Rit/Filter/Setup
Audio 4 to 32 ohms
Internal LS
Volume
Pot1
10kB
J3
J4
J5
J6
J7
J8
J2
J1
J10
J9
Alim.
Antenna
On/Off
Micro/PTT
C125
1n
SSB TRANSCEIVER "FORTY2" connect
(C) Luc Pistorius F6BQU
(C) Jean-Marc Eveille F5RDH


Préamplificateur BF
IC3
CAG
Haut parleur
Amplificateur BF
IC17
Filtre actif BF
IC16
Mélangeur à gain
IC2
Amplificateur FI
Q2
Filtre à quartz 4,9152 MHz
Mélangeur à gain
IC1
Filtre passe-bande 7 MHz
Q1
Atténuateur
BFO
4,9152 MHz
Antenne
Rx
Tx
S'mètre à bargraphe
IC18
IC19
Indicateur de puissance
IC12
Commande filtre BF
IC8
µcontrôleur
Commandes du µcontrôleur
IC9
IC10
IC11
Synthétiseur
Display
LCD 1x16
4,9152 MHz
OL
Micro
IC5
Préampli - compresseur
IC6
Modulateur équilibré
Filtre à quartz 4,915 MHz
IC7
Mélangeur à gain
Q4
Q5
Q6
Amplificateur HF
Filtre passe-bas 7 MHz
5 W
SSB TRANSCEIVER "FORTY2"
(C) Luc Pistorius F6BQU
(C) Jean-Marc Eveille F5RDH


F5RDH
VOLUME
ON
OFF
RIT
FILTER
STEP
ATT
FORTY II


ANTENNE
13,8V

MITSUBISHI RF POWER TRANSISTOR

2SC1971

NPN EPITAXIAL PLANAR TYPE

DESCRIPTION

2SC1971 is a silicon NPN epitaxial planar type transistor designed for RF power amplifiers on VHF band mobile radio applications.

FEATURES

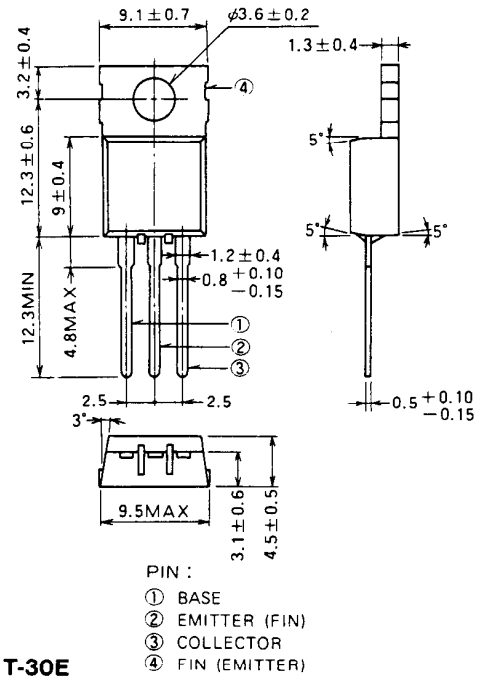
- High power gain: $G_{pe} \geqq 10dB$
  @V_{CC} = 13.5V, P_O = 6W, f = 175MHz
- Emitter ballasted construction, gold metallization for high reliability and good performances.
- TO-220 package similar is combinient for mounting.
- Ability of withstanding more than 20:1 load VSWR when operated at V_{CC} = 15.2V, P_O = 6W, f = 175MHz.

APPLICATION

4 to 5 watts output power amplifiers in VHF band applications.

OUTLINE DRAWING

Dimensions in mm



PIN :
① BASE
② EMITTER (FIN)
③ COLLECTOR
④ FIN (EMITTER)

T-30E

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CBO}	Collector to base voltage		35	V
V_{EBO}	Emitter to base voltage		4	V
V_{CEO}	Collector to emitter voltage	$R_{BE} = \infty$	17	V
I_C	Collector current		2	A
P_C	Collector dissipation	T_a = 25°C	1.5	W
		T_C = 25°C	12.5	W
T_j	Junction temperature		150	°C
T_{stg}	Storage temperature		−55 to 150	°C
R_{th-a}	Thermal resistance	Junction to ambient	83	°C/W
R_{th-c}		Junction to case	10	°C/W

Note. Above parameters are guaranteed independently.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

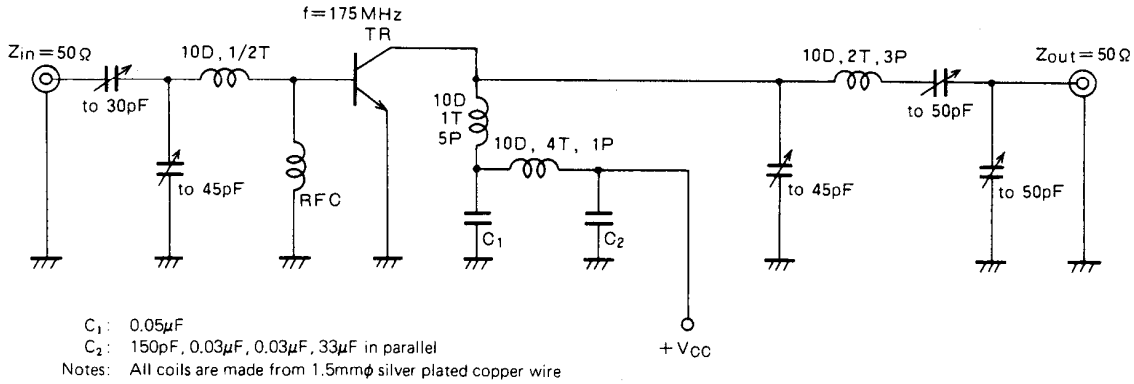
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{(BR)EBO}$	Emitter to base breakdown voltage	I_E = 5mA, I_C = 0	4			V
$V_{(BR)CBO}$	Collector to base breakdown voltage	I_C = 10mA, I_E = 0	35			V
$V_{(BR)CEO}$	Collector to emitter breakdown voltage	I_C = 50mA, $R_{BE} = \infty$	17			V
I_{CBO}	Collector cutoff current	V_{CB} = 25V, I_E = 0			500	μA
I_{EBO}	Emitter cutoff current	V_{EB} = 3V, I_C = 0			500	μA
h_{FE}	DC forward current gain *	V_{CE} = 10V, I_C = 0.1A	10	50	180	—
* P_O	Output power	V_{CC} = 13.5V, P_{in} = 0.6W, f = 175MHz	6	7		W
η_C	Collector efficiency		60	70		%

Note. * Pulse test, P_W = 150μs, duty = 5%.
Above parameters, ratings, limits and conditions are subject to change.

NOV. '97

MITSUBISHI ELECTRIC

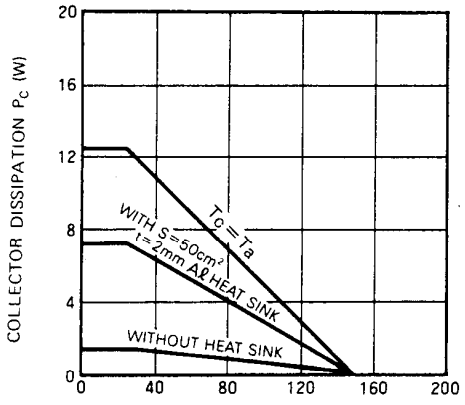
TEST CIRCUIT



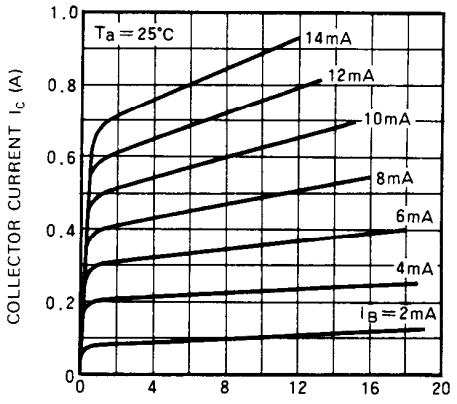
C_1: 0.05μF
C_2: 150pF, 0.03μF, 0.03μF, 33μF in parallel
Notes: All coils are made from 1.5mmφ silver plated copper wire
Coil dimensions in milli-meter
D: Inner diameter of coil
T: Turn number of coil
P: Pitch of coil

TYPICAL PERFORMANCE DATA

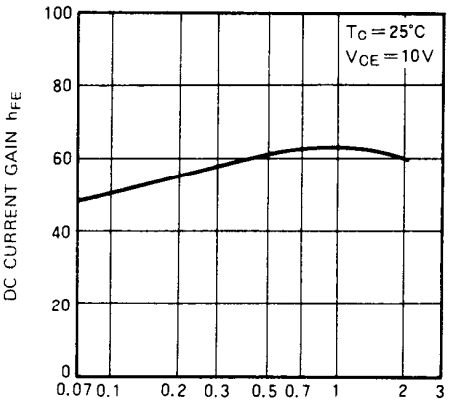
COLLECTOR DISSIPATION VS. AMBIENT TEMPERATURE



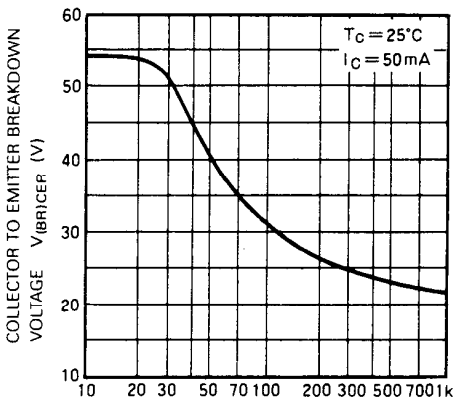
COLLECTOR CURRENT VS. COLLECTOR TO EMITTER VOLTAGE



DC CURRENT GAIN VS. COLLECTOR CURRENT

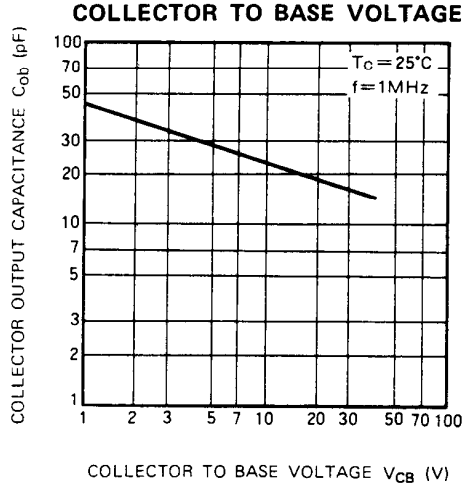


COLLECTOR TO EMITTER BREAKDOWN VOLTAGE VS. BASE TO EMITTER RESISTANCE

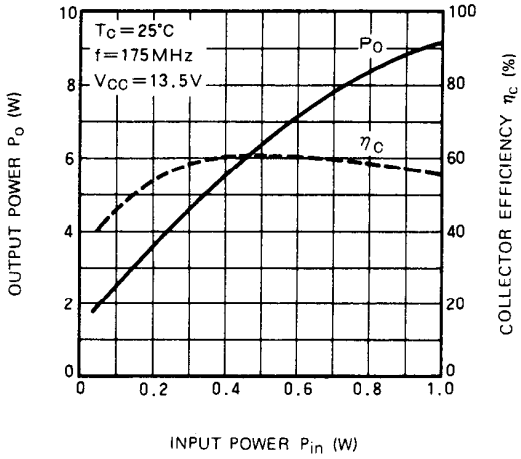


NPN EPITAXIAL PLANAR TYPE

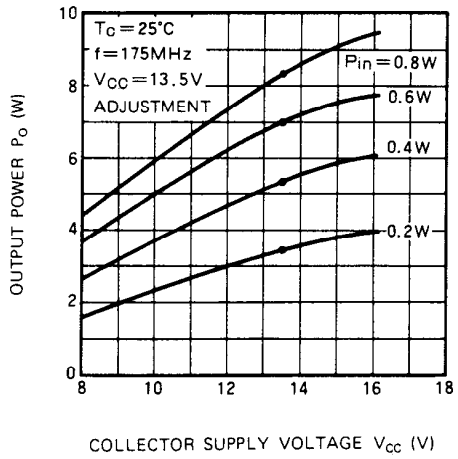
COLLECTOR OUTPUT CAPACITANCE VS. COLLECTOR TO BASE VOLTAGE



OUTPUT POWER, COLLECTOR EFFICIENCY VS. INPUT POWER



OUTPUT POWER VS. COLLECTOR SUPPLY VOLTAGE



MITSUBISHI ELECTRIC

National Semiconductor

August 2000

LM380
2.5W Audio Power Amplifier

General Description

The LM380 is a power audio amplifier for consumer applications. In order to hold system cost to a minimum, gain is internally fixed at 34 dB. A unique input stage allows ground referenced input signals. The output automatically self-centers to one-half the supply voltage.

The output is short circuit proof with internal thermal limiting. The package outline is standard dual-in-line. The LM380N uses a copper lead frame. The center three pins on either side comprise a heat sink. This makes the device easy to use in standard PC layouts.

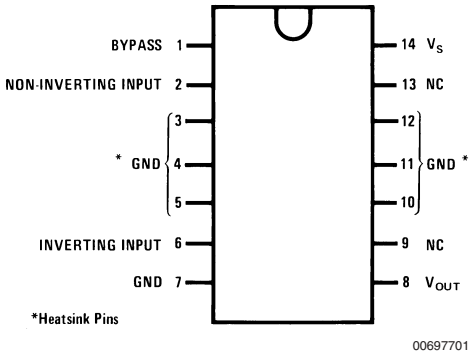
Uses include simple phonograph amplifiers, intercoms, line drivers, teaching machine outputs, alarms, ultrasonic drivers, TV sound systems, AM-FM radio, small servo drivers, power converters, etc.

A selected part for more power on higher supply voltages is available as the LM384. For more information see AN-69.

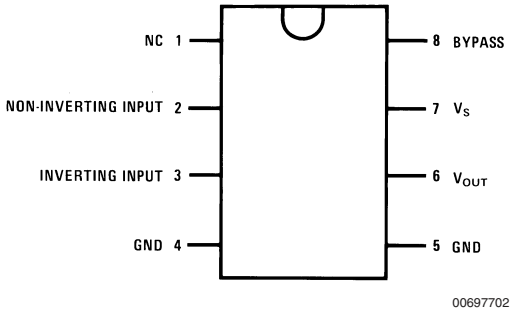
Features

- Wide supply voltage range: 10V-22V
- Low quiescent power drain: 0.13W (V_S= 18V)
- Voltage gain fixed at 50
- High peak current capability: 1.3A
- Input referenced to GND
- High input impedance: 150kΩ
- Low distortion
- Quiescent output voltage is at one-half of the supply voltage
- Standard dual-in-line package

Connection Diagrams (Dual-In-Line Packages, Top View)



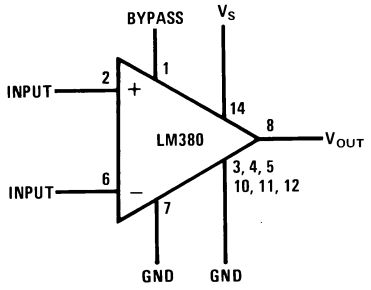
Order Number LM380N
See NS Package Number N14A



Order Number LM380N-8
See NS Package Number N08E

Block and Schematic Diagrams

LM380N



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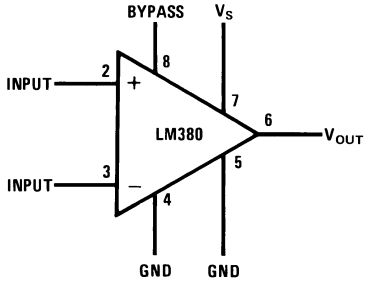
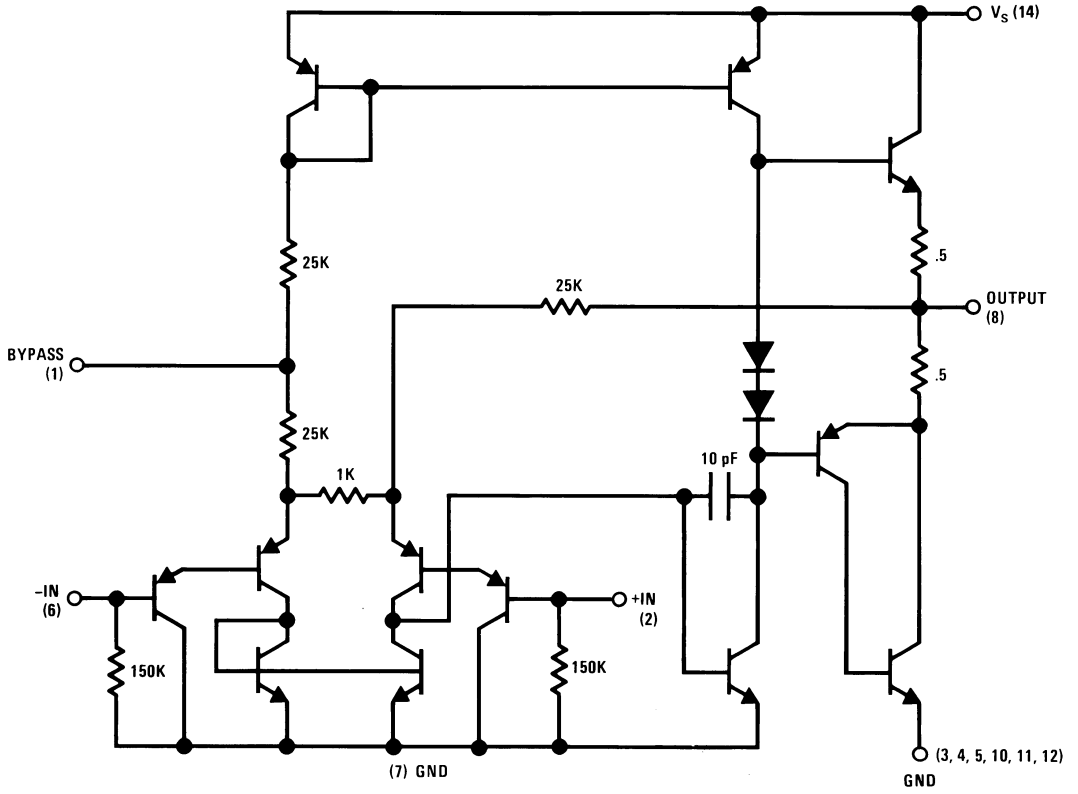
LM380N-8



00697704



00697705

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	22V
Peak Current	1.3A
Package Dissipation 14-Pin DIP (Note 7)	8.3W
Package Dissipation 8-Pin DIP (Note 7)	1.67W
Input Voltage	±0.5V
Storage Temperature	−65˚C to +150˚C
Operating Temperature	0˚C to +70˚C
Junction Temperature	+150˚C
Lead Temperature (Soldering, 10 sec.)	+260˚C
ESD rating to be determined	
Thermal Resistance	
θ_{JC} (14-Pin DIP)	30˚C/W
θ_{JC} (8-Pin DIP)	37˚C/W
θ_{JA} (14-Pin DIP)	79˚C/W
θ_{JA} (8-Pin DIP)	107˚C/W

Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$P_{OUT(RMS)}$	Output Power	R_L = 8Ω, THD = 3% (Notes 4, 5)	2.5			W
A_V	Gain		40	50	60	V/V
V_{OUT}	Output Voltage Swing	R_L = 8Ω		14		V_{p-p}
Z_{IN}	Input Resistance			150k		Ω
THD	Total Harmonic Distortion	(Notes 5, 6)		0.2		%
PSRR	Power Supply Rejection Ratio	(Note 3)		38		dB
V_S	Supply Voltage		10		22	V
BW	Bandwidth	P_{OUT} = 2W, R_L = 8Ω		100k		Hz
I_Q	Quiescent Supply Current			7	25	mA
V_{OUTQ}	Quiescent Output Voltage		8	9.0	10	V
I_{BIAS}	Bias Current	Inputs Floating		100		nA
I_{SC}	Short Circuit Current			1.3		A

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: V_S = 18V and T_A = 25˚C unless otherwise specified.

Note 3: Rejection ratio referred to the output with C_{BYPASS} = 5 µF.

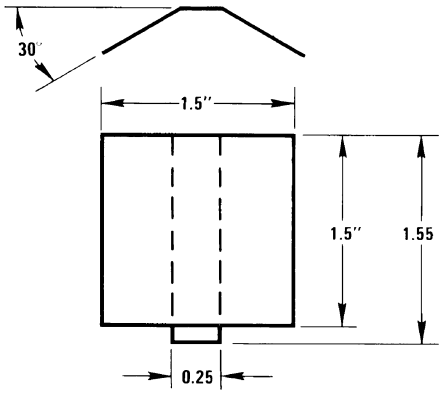
Note 4: With device Pins 3, 4, 5, 10, 11, 12 soldered into a 1/16" epoxy glass board with 2 ounce copper foil with a minimum surface of 6 square inches.

Note 5: C_{BYPASS} = 0.47 µfd on Pin 1.

Note 6: The maximum junction temperature of the LM380 is 150˚C.

Note 7: The package is to be derated at 15˚C/W junction to heat sink pins for 14-pin pkg; 75˚C/W for 8-pin.

Heat Sink Dimensions

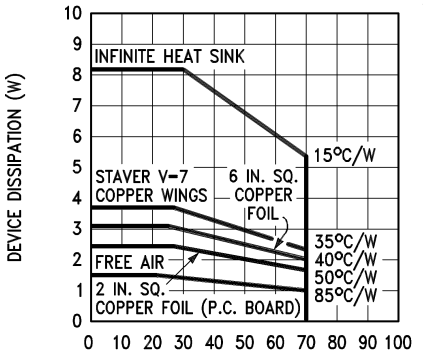


00697706

Staver Heat Sink #V-7
Staver Company
41 Saxon Ave.
P.O. Drawer H
Bayshore, NY 11706
Tel: (516) 666-8000
Copper Wings
2 Required
Soldered to
Pins 3, 4, 5,
10, 11, 12
Thickness 0.04
Inches

Typical Performance Characteristics

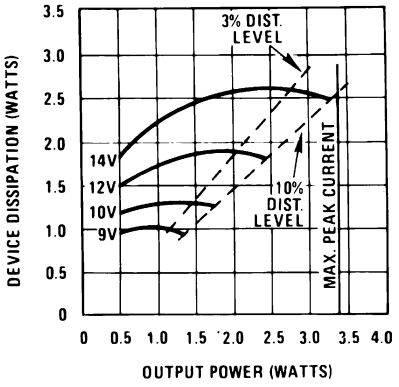
Maximum Device Dissipation vs Ambient Temperature



Note: 2 oz. copper foil, single-sided PC board.

00697712

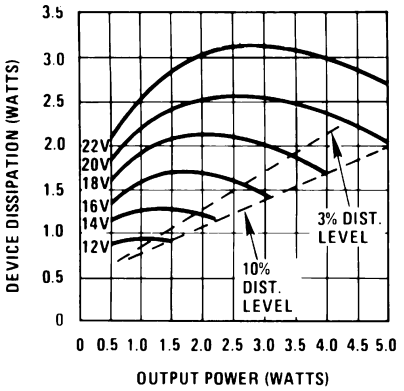
Device Dissipation vs Output Power—4Ω Load



00697713

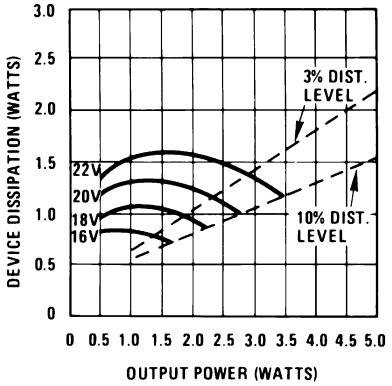
Typical Performance Characteristics (Continued)

Device Dissipation vs Output Power—8Ω Load



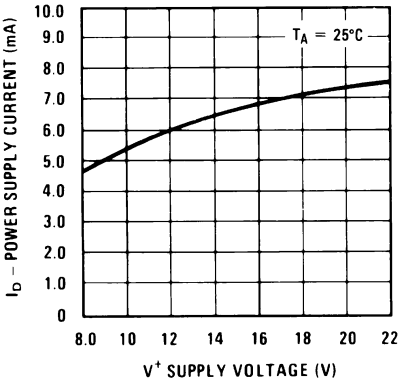
00697714

Device Dissipation vs Output Power—16Ω Load



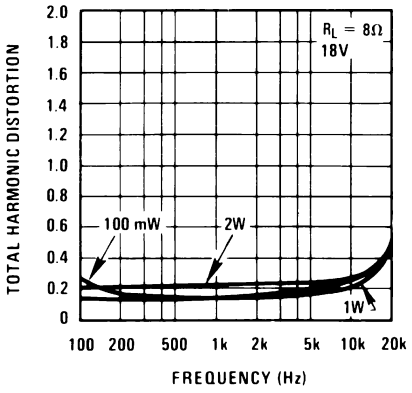
00697715

Power Supply Current vs Supply Voltage



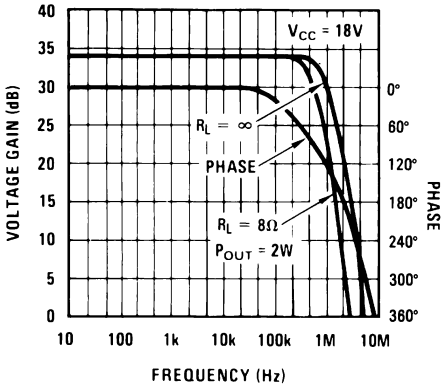
00697716

Total Harmonic Distortion vs Frequency



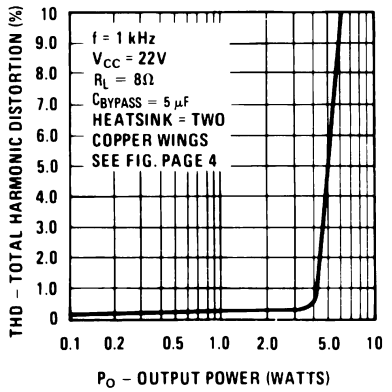
00697717

Output Voltage Gain and Phase vs Frequency



00697718

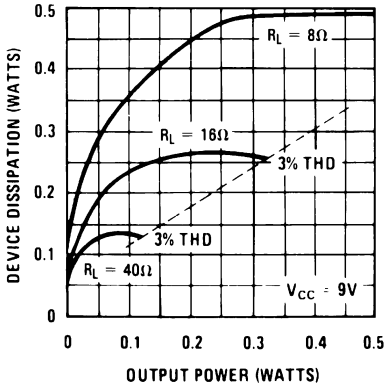
Total Harmonic Distortion vs Output Power



00697719

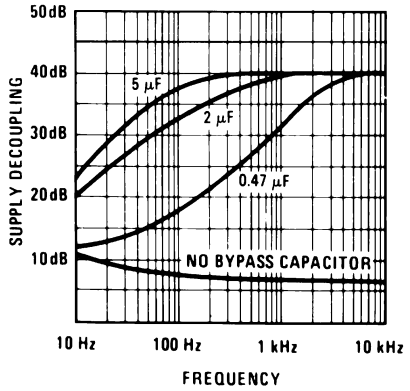
Typical Performance Characteristics (Continued)

Device Dissipation vs Output Power



00697720

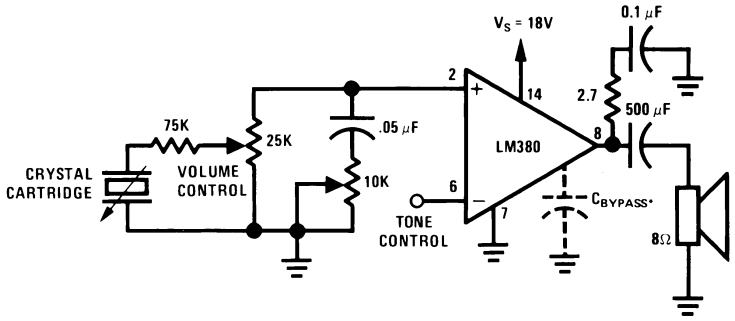
Supply Decoupling vs Frequency



00697721

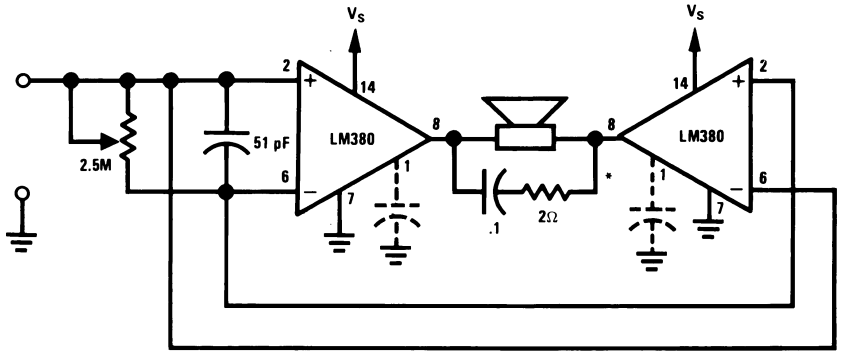
Typical Applications

Phono Amplifier



00697708

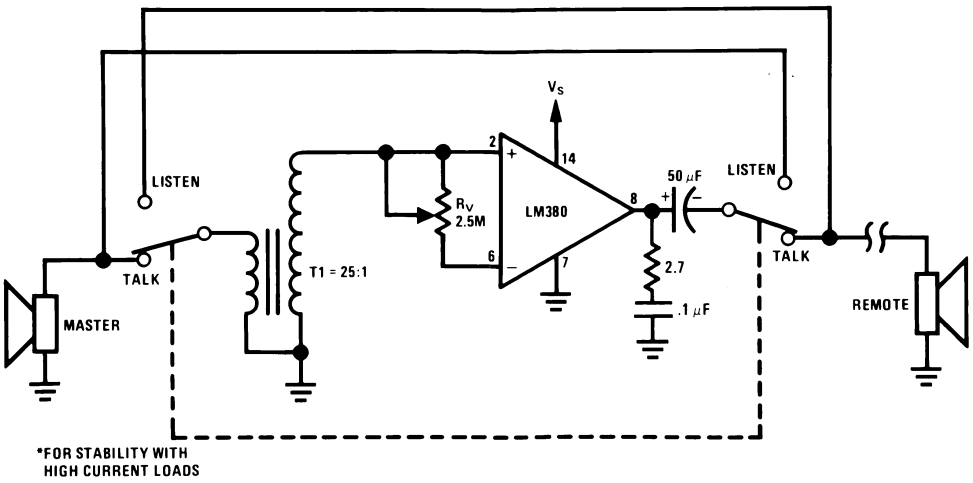
Bridge Amplifier



00697709

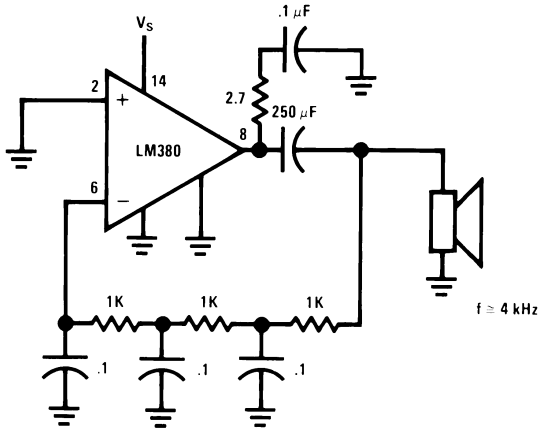
Typical Applications (Continued)

Intercom



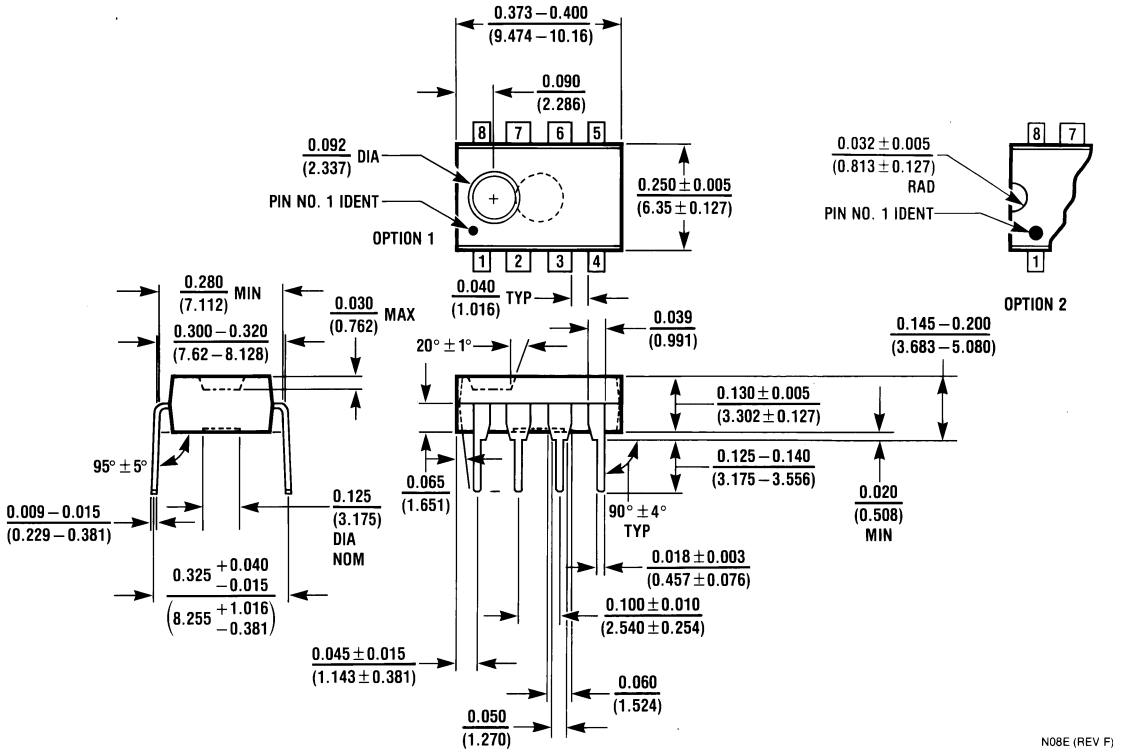
00697710

Phase Shift Oscillator

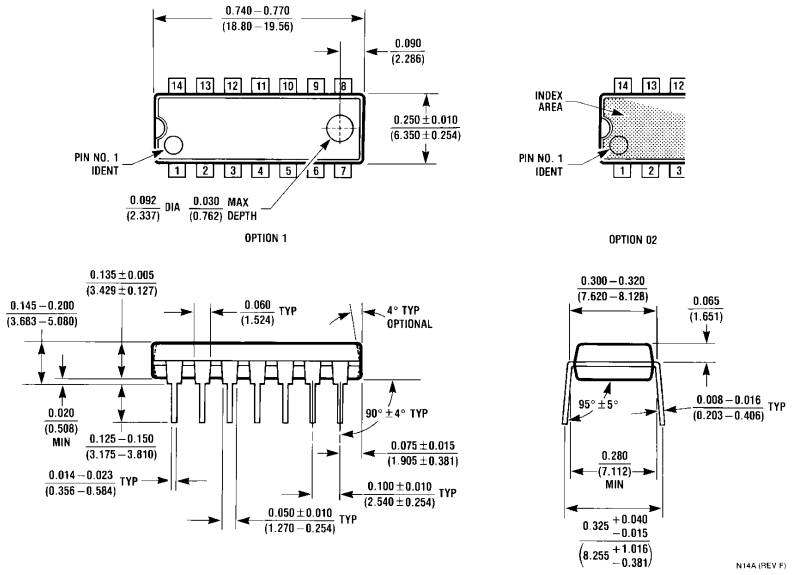


00697711

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Order Number LM380N-8
NS Package Number N08E



Molded Dual-In-Line Package (N)
Order Number LM380N
NS Package Number N14A

Notes

National Semiconductor
Americas Customer
Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

www.national.com

National Semiconductor
Europe Customer Support Center
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Support Center
Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560

National Semiconductor

August 2000

LM386
Low Voltage Audio Power Amplifier

General Description

The LM386 is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value from 20 to 200.

The inputs are ground referenced while the output automatically biases to one-half the supply voltage. The quiescent power drain is only 24 milliwatts when operating from a 6 volt supply, making the LM386 ideal for battery operation.

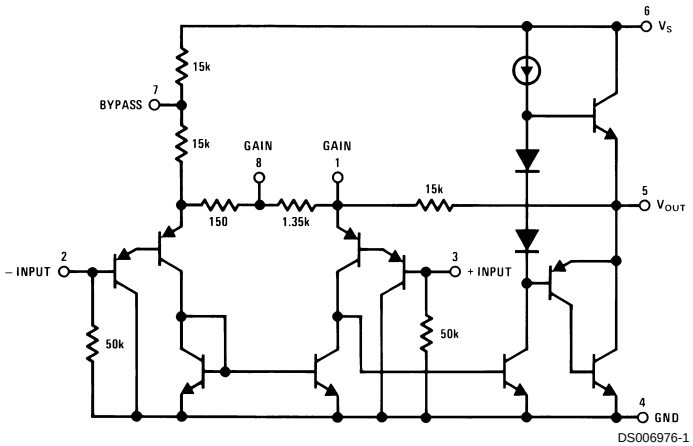
Features

- Battery operation
- Minimum external parts
- Wide supply voltage range: 4V–12V or 5V–18V
- Low quiescent current drain: 4mA
- Voltage gains from 20 to 200
- Ground referenced input
- Self-centering output quiescent voltage
- Low distortion: 0.2% (A_V = 20, V_S = 6V, R_L = 8Ω, P_O = 125mW, f = 1kHz)
- Available in 8 pin MSOP package

Applications

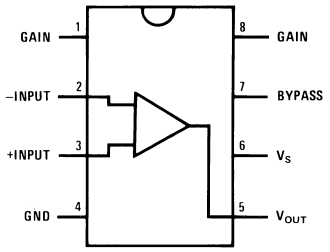
- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

Equivalent Schematic and Connection Diagrams



DS006976-1

**Small Outline,
Molded Mini Small Outline,
and Dual-In-Line Packages**



DS006976-2

**Top View
Order Number LM386M-1,
LM386MM-1, LM386N-1,
LM386N-3 or LM386N-4
See NS Package Number
M08A, MUA08A or N08E**

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
(LM386N-1, -3, LM386M-1)	15V
Supply Voltage (LM386N-4)	22V
Package Dissipation (Note 3)	
(LM386N)	1.25W
(LM386M)	0.73W
(LM386MM-1)	0.595W
Input Voltage	±0.4V
Storage Temperature	−65˚C to +150˚C
Operating Temperature	0˚C to +70˚C
Junction Temperature	+150˚C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec)	+260˚C
Small Outline Package	
(SOIC and MSOP)	
Vapor Phase (60 sec)	+215˚C
Infrared (15 sec)	+220˚C

See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.

Thermal Resistance	
θ_{JC} (DIP)	37˚C/W
θ_{JA} (DIP)	107˚C/W
θ_{JC} (SO Package)	35˚C/W
θ_{JA} (SO Package)	172˚C/W
θ_{JA} (MSOP)	210˚C/W
θ_{JC} (MSOP)	56˚C/W

Electrical Characteristics (Notes 1, 2)

T_A = 25˚C

Parameter	Conditions	Min	Typ	Max	Units
Operating Supply Voltage (V_S)					
LM386N-1, -3, LM386M-1, LM386MM-1		4		12	V
LM386N-4		5		18	V
Quiescent Current (I_Q)	V_S = 6V, V_{IN} = 0		4	8	mA
Output Power (P_{OUT})					
LM386N-1, LM386M-1, LM386MM-1	V_S = 6V, R_L = 8Ω, THD = 10%	250	325		mW
LM386N-3	V_S = 9V, R_L = 8Ω, THD = 10%	500	700		mW
LM386N-4	V_S = 16V, R_L = 32Ω, THD = 10%	700	1000		mW
Voltage Gain (A_V)	V_S = 6V, f = 1 kHz		26		dB
	10 µF from Pin 1 to 8		46		dB
Bandwidth (BW)	V_S = 6V, Pins 1 and 8 Open		300		kHz
Total Harmonic Distortion (THD)	V_S = 6V, R_L = 8Ω, P_{OUT} = 125 mW		0.2		%
	f = 1 kHz, Pins 1 and 8 Open				
Power Supply Rejection Ratio (PSRR)	V_S = 6V, f = 1 kHz, C_{BYPASS} = 10 µF		50		dB
	Pins 1 and 8 Open, Referred to Output				
Input Resistance (R_{IN})			50		kΩ
Input Bias Current (I_{BIAS})	V_S = 6V, Pins 2 and 3 Open		250		nA

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operation in ambient temperatures above 25˚C, the device must be derated based on a 150˚C maximum junction temperature and 1) a thermal resistance of 107˚C/W junction to ambient for the dual-in-line package and 2) a thermal resistance of 170˚C/W for the small outline package.

Application Hints

GAIN CONTROL

To make the LM386 a more versatile amplifier, two pins (1 and 8) are provided for gain control. With pins 1 and 8 open the 1.35 kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pin 1 to 8, bypassing the 1.35 kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 1 to ground.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 1 to 5 (paralleling the internal 15 kΩ resistor). For 6 dB effective bass boost: R ≃ 15 kΩ, the lowest value for good stable operation is R = 10 kΩ if pin 8 is open. If pins 1 and 8 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9.

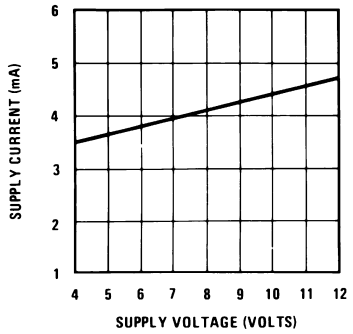
INPUT BIASING

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM386 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

When using the LM386 with higher gains (bypassing the 1.35 kΩ resistor between pins 1 and 8) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1 µF capacitor or a short to ground depending on the dc source resistance on the driven input.

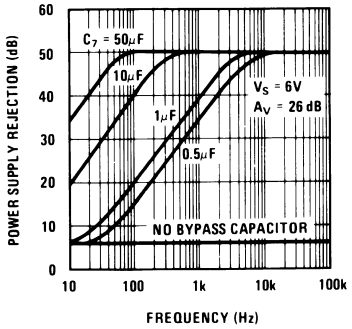
Typical Performance Characteristics

Quiescent Supply Current vs Supply Voltage



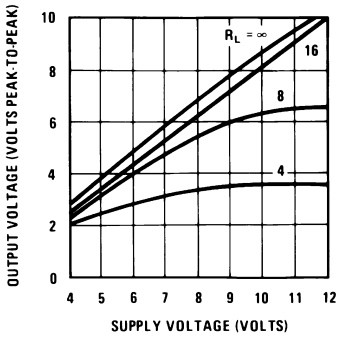
DS006976-5

Power Supply Rejection Ratio (Referred to the Output) vs Frequency



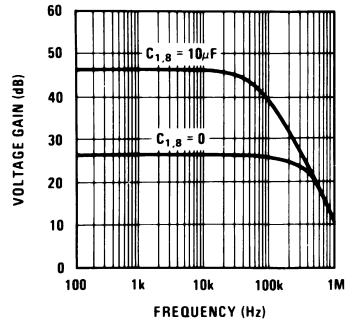
DS006976-12

Peak-to-Peak Output Voltage Swing vs Supply Voltage



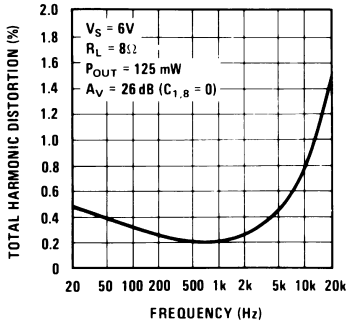
DS006976-13

Voltage Gain vs Frequency



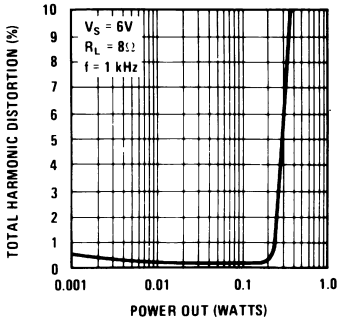
DS006976-14

Distortion vs Frequency



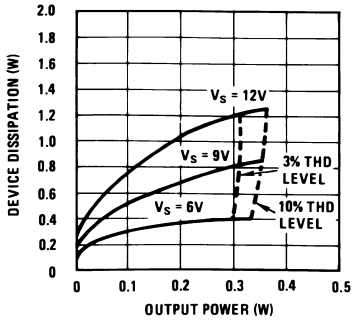
DS006976-15

Distortion vs Output Power



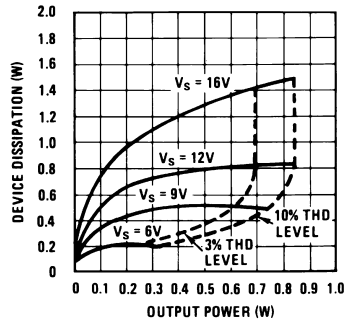
DS006976-16

Device Dissipation vs Output Power—4Ω Load



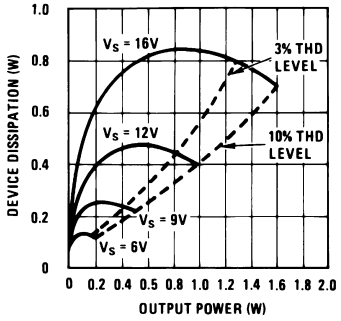
DS006976-17

Device Dissipation vs Output Power—8Ω Load



DS006976-18

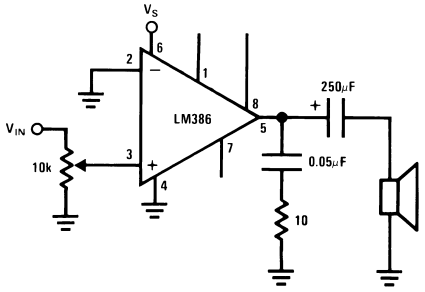
Device Dissipation vs Output Power—16Ω Load



DS006976-19

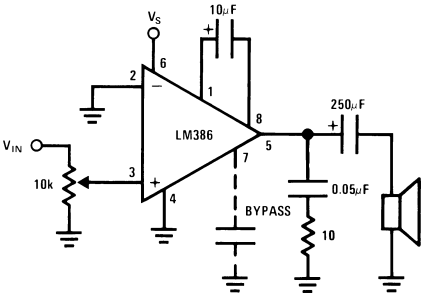
Typical Applications

Amplifier with Gain = 20
Minimum Parts



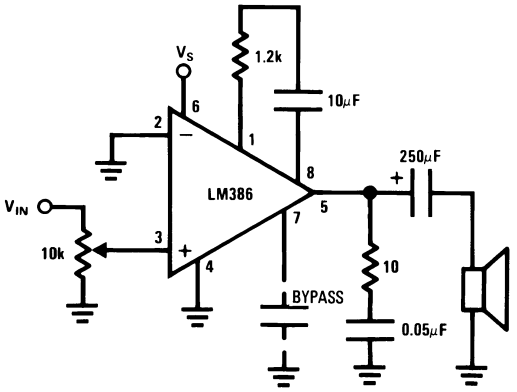
DS006976-3

Amplifier with Gain = 200



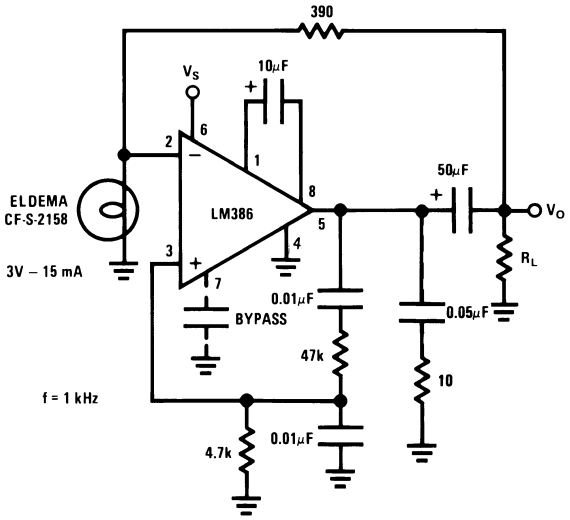
DS006976-4

Amplifier with Gain = 50



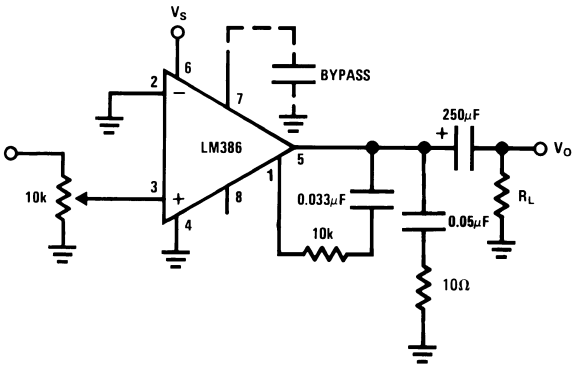
DS006976-6

Low Distortion Power Wienbridge Oscillator



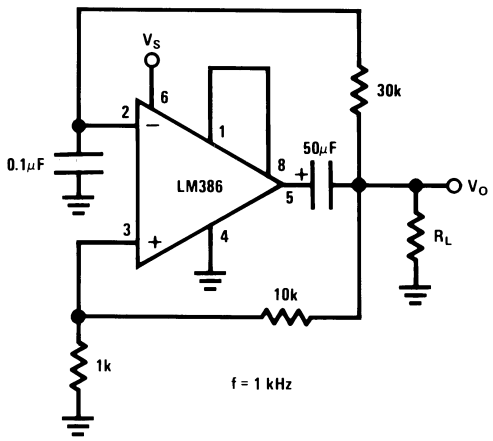
DS006976-7

Amplifier with Bass Boost



DS006976-8

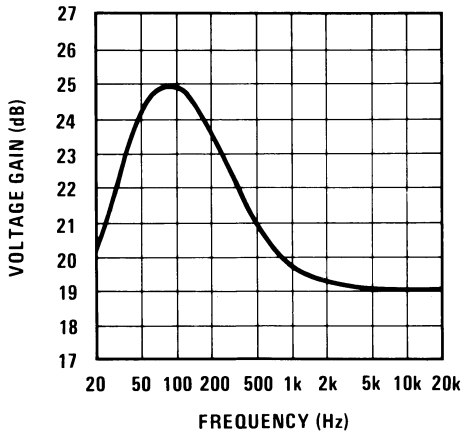
Square Wave Oscillator



DS006976-9

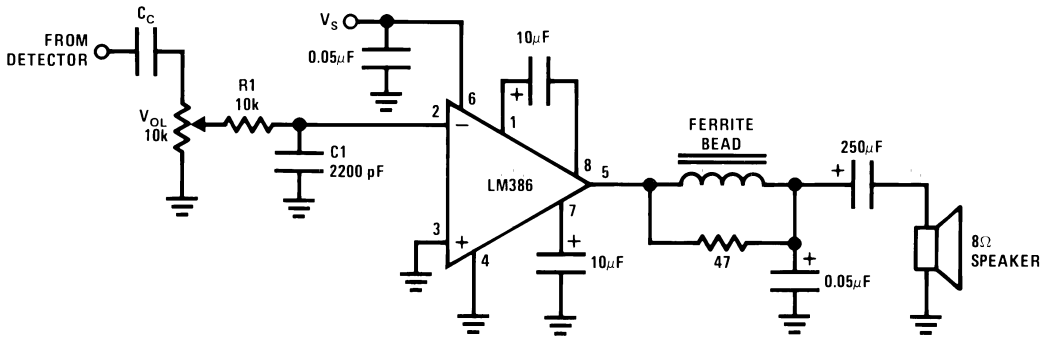
Typical Applications (Continued)

Frequency Response with Bass Boost



DS006976-10

AM Radio Power Amplifier



DS006976-11

Note 4: Twist Supply lead and supply ground very tightly.

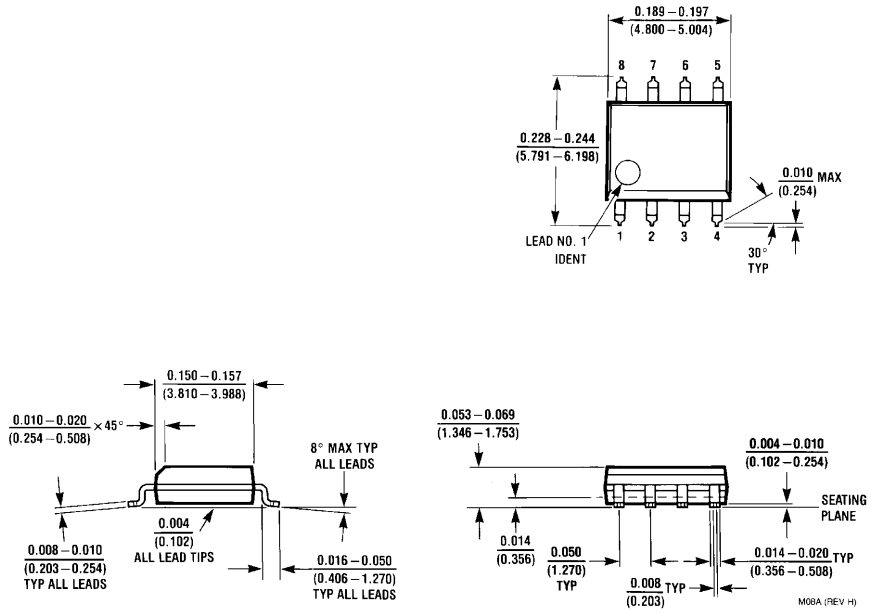
Note 5: Twist speaker lead and ground very tightly.

Note 6: Ferrite bead in Ferroxcube K5-001-001/3B with 3 turns of wire.

Note 7: R1C1 band limits input signals.

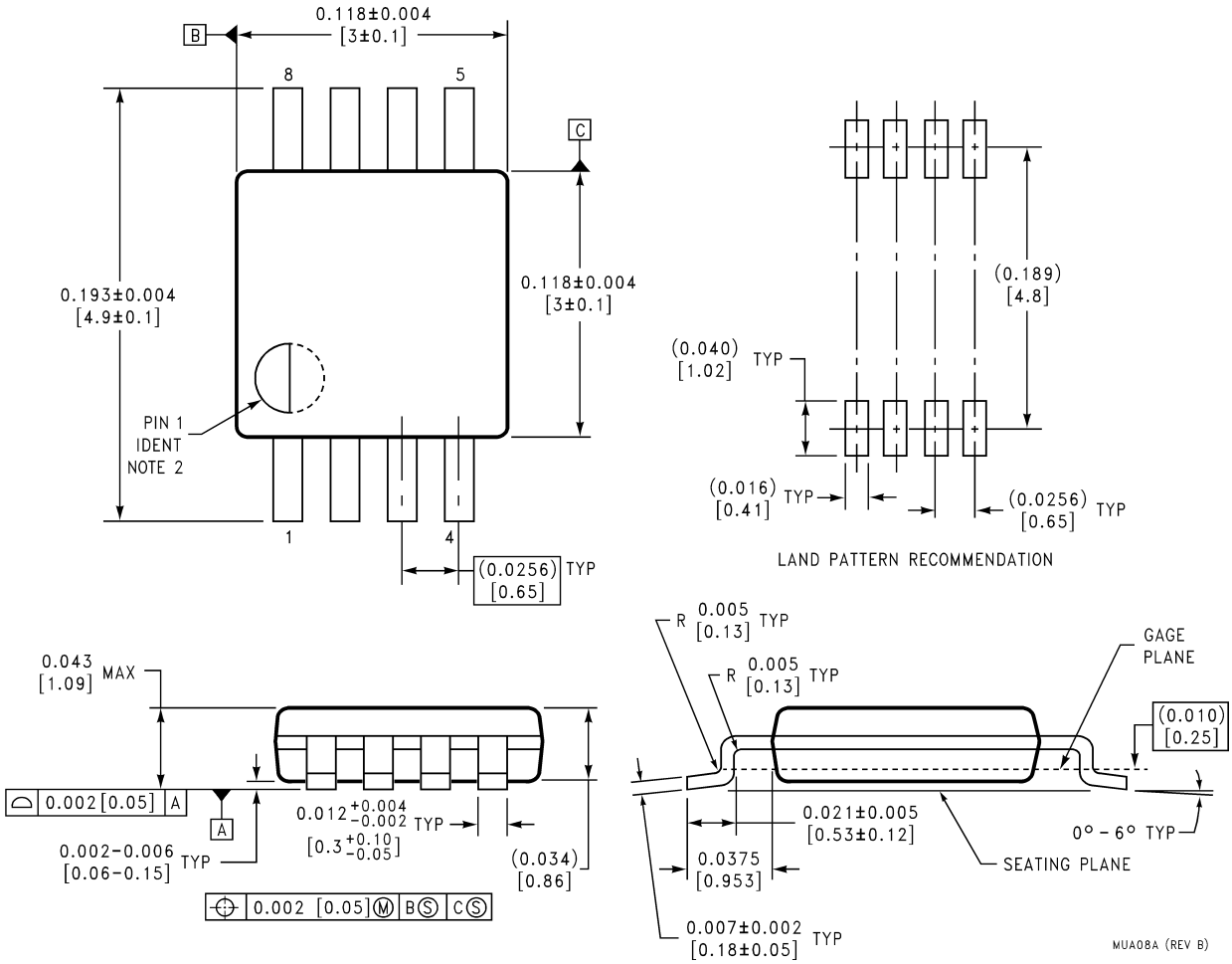
Note 8: All components must be spaced very closely to IC.

Physical Dimensions inches (millimeters) unless otherwise noted



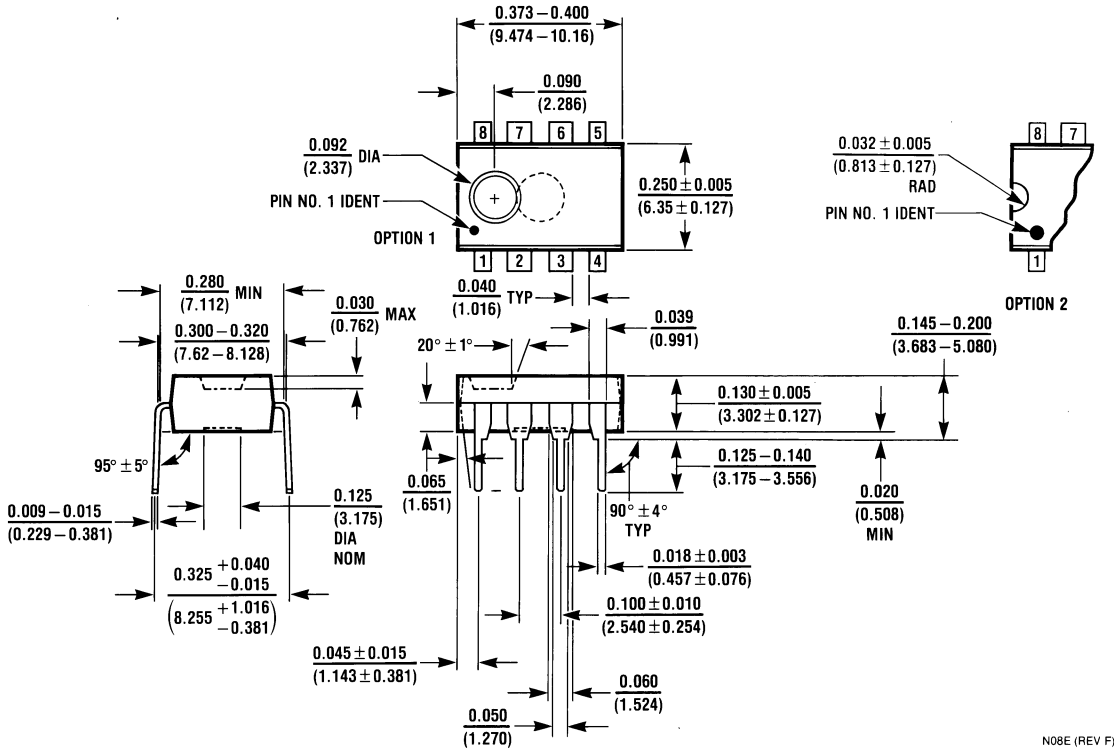
SO Package (M)
Order Number LM386M-1
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



8-Lead (0.118” Wide) Molded Mini Small Outline Package
Order Number LM386MM-1
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Dual-In-Line Package (N)
Order Number LM386N-1, LM386N-3 or LM386N-4
NS Package Number N08E

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National Semiconductor

January 2000

LM3914
Dot/Bar Display Driver

General Description

The LM3914 is a monolithic integrated circuit that senses analog voltage levels and drives 10 LEDs, providing a linear analog display. A single pin changes the display from a moving dot to a bar graph. Current drive to the LEDs is regulated and programmable, eliminating the need for resistors. This feature is one that allows operation of the whole system from less than 3V.

The circuit contains its own adjustable reference and accurate 10-step voltage divider. The low-bias-current input buffer accepts signals down to ground, or V^-, yet needs no protection against inputs of 35V above or below ground. The buffer drives 10 individual comparators referenced to the precision divider. Indication non-linearity can thus be held typically to ½%, even over a wide temperature range.

Versatility was designed into the LM3914 so that controller, visual alarm, and expanded scale functions are easily added on to the display system. The circuit can drive LEDs of many colors, or low-current incandescent lamps. Many LM3914s can be "chained" to form displays of 20 to over 100 segments. Both ends of the voltage divider are externally available so that 2 drivers can be made into a zero-center meter.

The LM3914 is very easy to apply as an analog meter circuit. A 1.2V full-scale meter requires only 1 resistor and a single 3V to 15V supply in addition to the 10 display LEDs. If the 1 resistor is a pot, it becomes the LED brightness control. The simplified block diagram illustrates this extremely simple external circuitry.

When in the dot mode, there is a small amount of overlap or "fade" (about 1 mV) between segments. This assures that at no time will all LEDs be "OFF", and thus any ambiguous display is avoided. Various novel displays are possible.

Much of the display flexibility derives from the fact that all outputs are individual, DC regulated currents. Various effects can be achieved by modulating these currents. The individual outputs can drive a transistor as well as a LED at the same time, so controller functions including "staging" control can be performed. The LM3914 can also act as a programmer, or sequencer.

The LM3914 is rated for operation from 0˚C to +70˚C. The LM3914N-1 is available in an 18-lead molded (N) package.

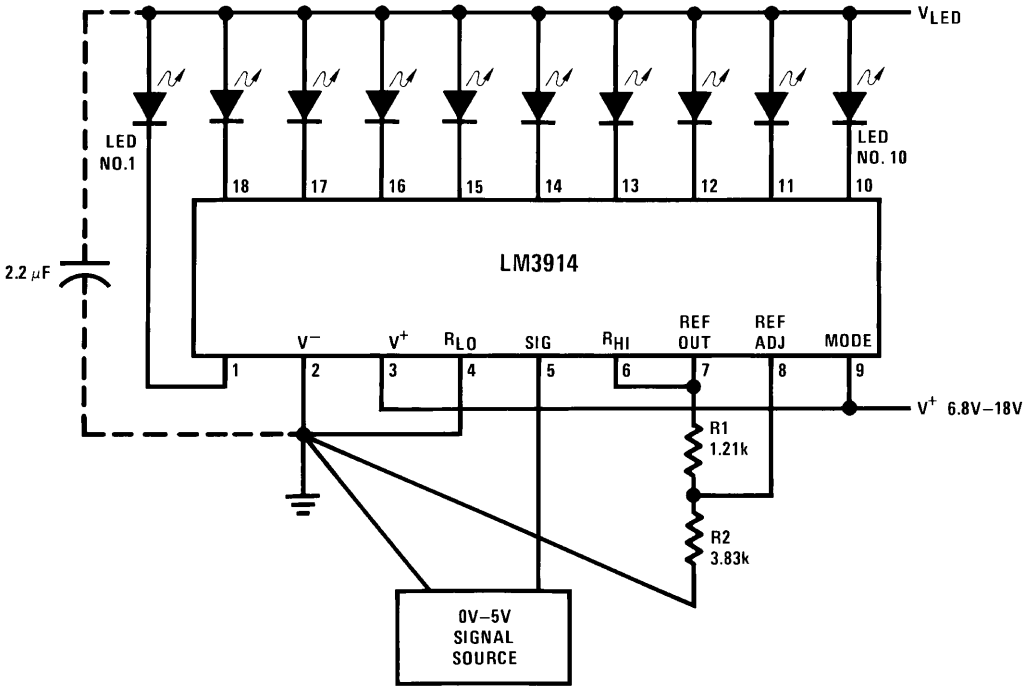
The following typical application illustrates adjusting of the reference to a desired value, and proper grounding for accurate operation, and avoiding oscillations.

Features

- Drives LEDs, LCDs or vacuum fluorescents
- Bar or dot display mode externally selectable by user
- Expandable to displays of 100 steps
- Internal voltage reference from 1.2V to 12V
- Operates with single supply of less than 3V
- Inputs operate down to ground
- Output current programmable from 2 mA to 30 mA
- No multiplex switching or interaction between outputs
- Input withstands ±35V without damage or false outputs
- LED driver outputs are current regulated, open-collectors
- Outputs can interface with TTL or CMOS logic
- The internal 10-step divider is floating and can be referenced to a wide range of voltages

Typical Applications

0V to 5V Bar Graph Meter



DS007970-1

$$\text{Ref Out V} = 1.25\left(1 + \frac{R2}{R1}\right)$$

$$I_{LED} \cong \frac{12.5}{R1}$$

Note: Grounding method is typical of *all* uses. The 2.2 µF tantalum or 10 µF aluminum electrolytic capacitor is needed if leads to the LED supply are 6" or longer.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Dissipation (Note 6)	
Molded DIP (N)	1365 mW
Supply Voltage	25V
Voltage on Output Drivers	25V
Input Signal Overvoltage (Note 4)	±35V
Divider Voltage	−100 mV to V^+
Reference Load Current	10 mA
Storage Temperature Range	−55˚C to +150˚C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260˚C
Plastic Chip Carrier Package	
Vapor Phase (60 seconds)	215˚C
Infrared (15 seconds)	220˚C

See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.

Electrical Characteristics (Notes 2, 4)

Parameter	Conditions (Note 2)		Min	Typ	Max	Units
COMPARATOR						
Offset Voltage, Buffer and First Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, I_{LED} = 1 mA			3	10	mV
Offset Voltage, Buffer and Any Other Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, I_{LED} = 1 mA			3	15	mV
Gain ($\Delta I_{LED}/\Delta V_{IN}$)	$I_{L(REF)}$ = 2 mA, I_{LED} = 10 mA		3	8		mA/mV
Input Bias Current (at Pin 5)	$0V \le V_{IN} \le V^+ - 1.5V$			25	100	nA
Input Signal Overvoltage	No Change in Display		−35		35	V
VOLTAGE-DIVIDER						
Divider Resistance	Total, Pin 6 to 4		8	12	17	kΩ
Accuracy	(Note 3)			0.5	2	%
VOLTAGE REFERENCE						
Output Voltage	$0.1 mA \le I_{L(REF)} \le 4 mA$, $V^+ = V_{LED}$ = 5V		1.2	1.28	1.34	V
Line Regulation	$3V \le V^+ \le 18V$			0.01	0.03	%/V
Load Regulation	$0.1 mA \le I_{L(REF)} \le 4 mA$, $V^+ = V_{LED}$ = 5V			0.4	2	%
Output Voltage Change with Temperature	$0˚C \le T_A \le +70˚C$, $I_{L(REF)}$ = 1 mA, V^+ = 5V			1		%
Adjust Pin Current				75	120	µA
OUTPUT DRIVERS						
LED Current	$V^+ = V_{LED}$ = 5V, $I_{L(REF)}$ = 1 mA		7	10	13	mA
LED Current Difference (Between Largest and Smallest LED Currents)	V_{LED} = 5V	I_{LED} = 2 mA		0.12	0.4	mA
		I_{LED} = 20 mA		1.2	3	
LED Current Regulation	$2V \le V_{LED} \le 17V$	I_{LED} = 2 mA		0.1	0.25	mA
		I_{LED} = 20 mA		1	3	
Dropout Voltage	$I_{LED(ON)}$ = 20 mA, V_{LED} = 5V, ΔI_{LED} = 2 mA				1.5	V
Saturation Voltage	I_{LED} = 2.0 mA, $I_{L(REF)}$ = 0.4 mA			0.15	0.4	V
Output Leakage, Each Collector	(Bar Mode) (Note 5)			0.1	10	µA
Output Leakage	(Dot Mode) (Note 5)	Pins 10–18		0.1	10	µA
		Pin 1	60	150	450	µA
SUPPLY CURRENT						
Standby Supply Current (All Outputs Off)	V^+ = 5V, $I_{L(REF)}$ = 0.2 mA			2.4	4.2	mA
	V^+ = 20V, $I_{L(REF)}$ = 1.0 mA			6.1	9.2	mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Electrical Characteristics (Notes 2, 4) (Continued)

Note 2: Unless otherwise stated, all specifications apply with the following conditions:

$3\ V_{DC} \le V^+ \le 20\ V_{DC}$ V_{REF}, V_{RHI}, $V_{RLO} \le (V^+ - 1.5V)$

$3\ V_{DC} \le V_{LED} \le V^+$ $0V \le V_{IN} \le V^+ - 1.5V$

$-0.015V \le V_{RLO} \le 12\ V_{DC}$ $T_A = +25^\circ C$, $I_{L(REF)} = 0.2$ mA, $V_{LED} = 3.0V$, pin 9 connected to pin 3 (Bar Mode).

$-0.015V \le V_{RHI} \le 12\ V_{DC}$

For higher power dissipations, pulse testing is used.

Note 3: Accuracy is measured referred to +10.000 V_{DC} at pin 6, with 0.000 V_{DC} at pin 4. At lower full-scale voltages, buffer and comparator offset voltage may add significant error.

Note 4: Pin 5 input current must be limited to ±3 mA. The addition of a 39k resistor in series with pin 5 allows ±100V signals without damage.

Note 5: Bar mode results when pin 9 is within 20 mV of V^+. Dot mode results when pin 9 is pulled at least 200 mV below V^+ or left open circuit. LED No. 10 (pin 10 output current) is disabled if pin 9 is pulled 0.9V or more below V_{LED}.

Note 6: The maximum junction temperature of the LM3914 is 100˚C. Devices must be derated for operation at elevated temperatures. Junction to ambient thermal resistance is 55˚C/W for the molded DIP (N package).

Definition of Terms

Accuracy: The difference between the observed threshold voltage and the ideal threshold voltage for each comparator. Specified and tested with 10V across the internal voltage divider so that resistor ratio matching error predominates over comparator offset voltage.

Adjust Pin Current: Current flowing out of the reference adjust pin when the reference amplifier is in the linear region.

Comparator Gain: The ratio of the change in output current (I_{LED}) to the change in input voltage (V_{IN}) required to produce it for a comparator in the linear region.

Dropout Voltage: The voltage measured at the current source outputs required to make the output current fall by 10%.

Input Bias Current: Current flowing out of the signal input when the input buffer is in the linear region.

LED Current Regulation: The change in output current over the specified range of LED supply voltage (V_{LED}) as measured at the current source outputs. As the forward voltage of an LED does not change significantly with a small change in forward current, this is equivalent to changing the voltage at the LED anodes by the same amount.

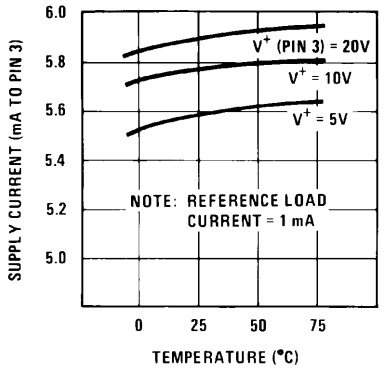
Line Regulation: The average change in reference output voltage over the specified range of supply voltage (V^+).

Load Regulation: The change in reference output voltage (V_{REF}) over the specified range of load current ($I_{L(REF)}$).

Offset Voltage: The differential input voltage which must be applied to each comparator to bias the output in the linear region. Most significant error when the voltage across the internal voltage divider is small. Specified and tested with pin 6 voltage (V_{RHI}) equal to pin 4 voltage (V_{RLO}).

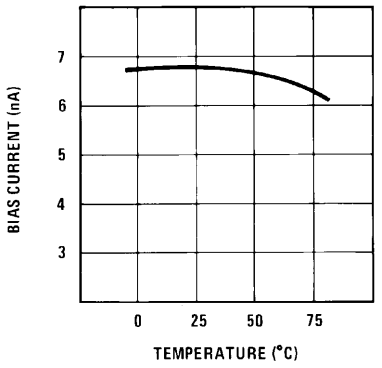
Typical Performance Characteristics

Supply Current vs Temperature



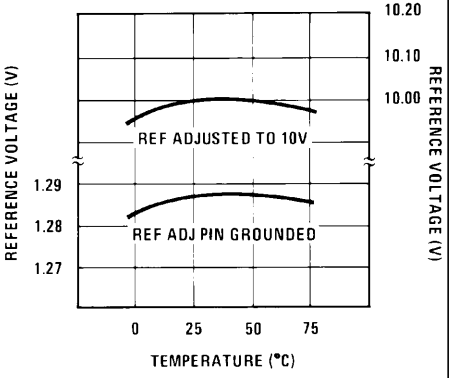
DS007970-2

Operating Input Bias Current vs Temperature



DS007970-20

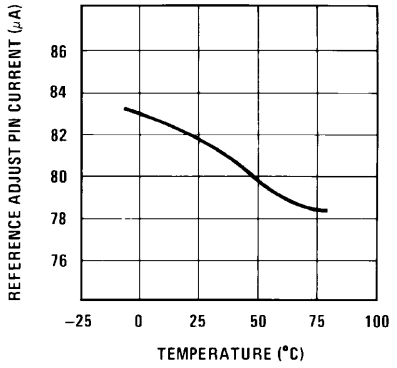
Reference Voltage vs Temperature



DS007970-21

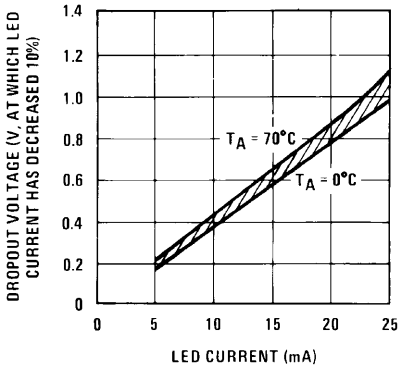
Typical Performance Characteristics (Continued)

Reference Adjust Pin Current vs Temperature



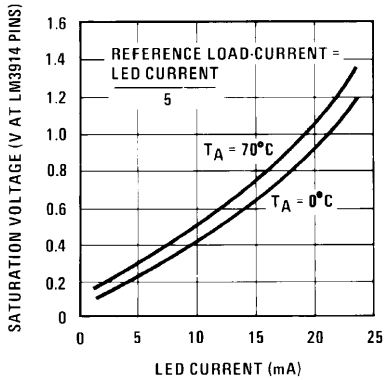
DS007970-22

LED Current-Regulation Dropout



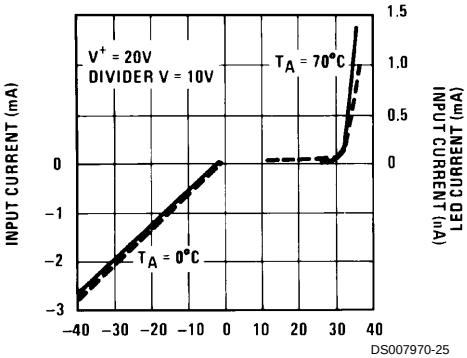
DS007970-23

LED Driver Saturation Voltage



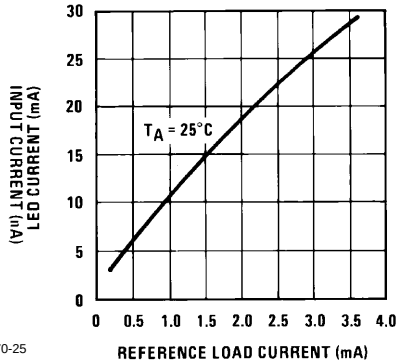
DS007970-24

Input Current Beyond Signal Range (Pin 5)



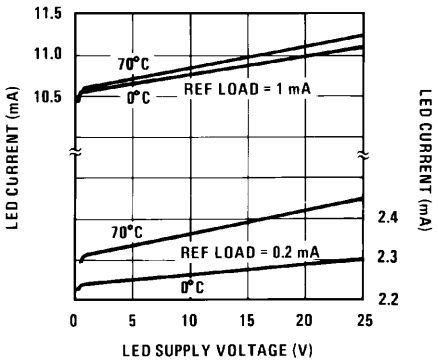
DS007970-25

LED Current vs Reference Loading



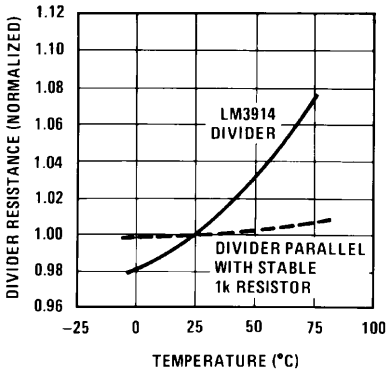
DS007970-26

LED Driver Current Regulation



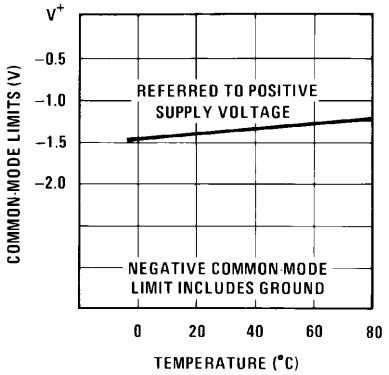
DS007970-27

Total Divider Resistance vs Temperature



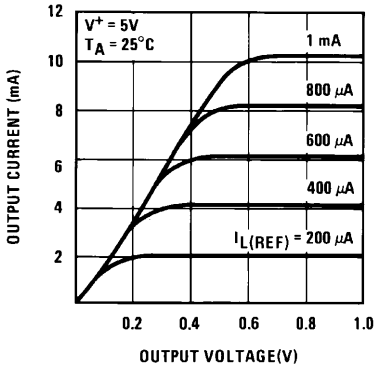
DS007970-28

Common-Mode Limits



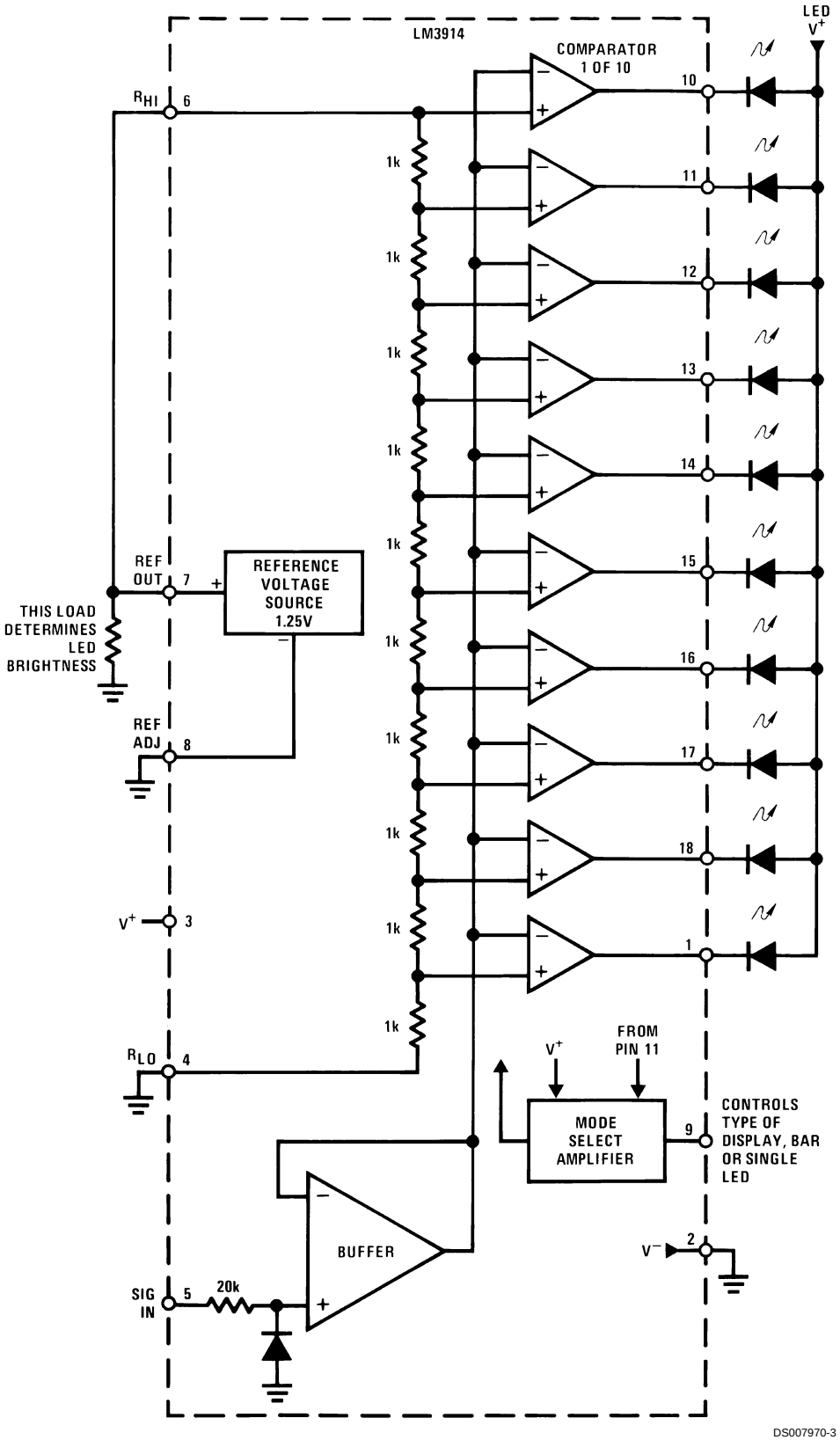
DS007970-29

Output Characteristics



DS007970-30

Block Diagram (Showing Simplest Application)



Functional Description

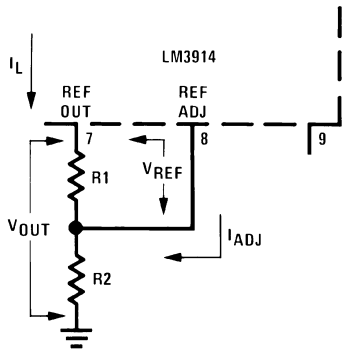
The simplifed LM3914 block diagram is to give the general idea of the circuit's operation. A high input impedance buffer operates with signals from ground to 12V, and is protected against reverse and overvoltage signals. The signal is then applied to a series of 10 comparators; each of which is biased to a different comparison level by the resistor string.

In the example illustrated, the resistor string is connected to the internal 1.25V reference voltage. In this case, for each 125 mV that the input signal increases, a comparator will switch on another indicating LED. This resistor divider can be connected between any 2 voltages, providing that they are 1.5V below V^+ and no less than V^-. If an expanded scale meter display is desired, the total divider voltage can be as little as 200 mV. Expanded-scale meter displays are more accurate and the segments light uniformly only if bar mode is used. At 50 mV or more per step, dot mode is usable.

INTERNAL VOLTAGE REFERENCE

The reference is designed to be adjustable and develops a nominal 1.25V between the REF OUT (pin 7) and REF ADJ (pin 8) terminals. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2 giving an output voltage of:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R_2$$



DS007970-4

Since the 120 µA current (max) from the adjust terminal represents an error term, the reference was designed to minimize changes of this current with V^+ and load changes.

CURRENT PROGRAMMING

A feature not completely illustrated by the block diagram is the LED brightness control. The current drawn out of the reference voltage pin (pin 7) determines LED current. Approximately 10 times this current will be drawn through each lighted LED, and this current will be relatively constant despite supply voltage and temperature changes. Current drawn by the internal 10-resistor divider, as well as by the external current and voltage-setting divider should be included in calculating LED drive current. The ability to modulate LED brightness with time, or in proportion to input voltage and other signals can lead to a number of novel displays or ways of indicating input overvoltages, alarms, etc.

MODE PIN USE

Pin 9, the Mode Select input controls chaining of multiple LM3914s, and controls bar or dot mode operation. The following tabulation shows the basic ways of using this input. Other more complex uses will be illustrated in the applications.

Bar Graph Display: Wire Mode Select (pin 9) *directly* to pin 3 (V^+ pin).

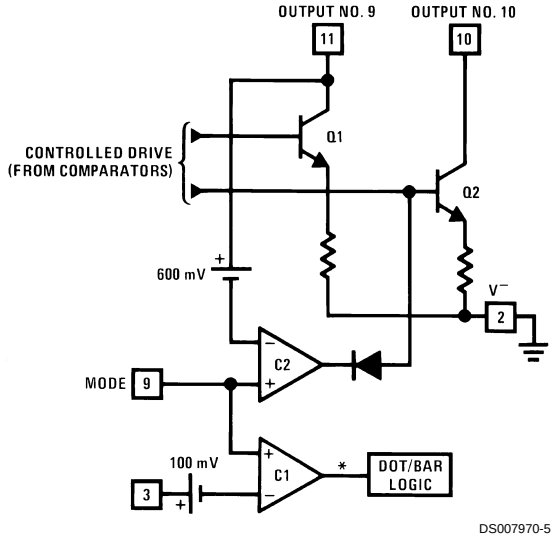
Dot Display, Single LM3914 Driver: Leave the Mode Select pin open circuit.

Dot Display, 20 or More LEDs: Connect pin 9 of the *first* driver in the series (i.e., the one with the lowest input voltage comparison points) to pin 1 of the next higher LM3914 driver. Continue connecting pin 9 of lower input drivers to pin 1 of higher input drivers for 30, 40, or more LED displays. The last LM3914 driver in the chain will have pin 9 wired to pin 11. All previous drivers should have a 20k resistor in parallel with LED No. 9 (pin 11 to V_{LED}).

Mode Pin Functional Description

This pin actually performs two functions. Refer to the simplified block diagram below.

Block Diagram of Mode Pin Description



DS007970-5

*High for bar

DOT OR BAR MODE SELECTION

The voltage at pin 9 is sensed by comparator C1, nominally referenced to (V^+ − 100 mV). The chip is in bar mode when pin 9 is above this level; otherwise it's in dot mode. The comparator is designed so that pin 9 can be left open circuit for dot mode.

Taking into account comparator gain and variation in the 100 mV reference level, pin 9 should be no more than 20 mV below V^+ for bar mode and more than 200 mV below V^+ (or open circuit) for dot mode. In most applications, pin 9 is either open (dot mode) or tied to V^+ (bar mode). In bar mode, pin 9 should be connected directly to pin 3. Large currents drawn from the power supply (LED current, for example) should not share this path so that large IR drops are avoided.

DOT MODE CARRY

In order for the display to make sense when multiple LM3914s are cascaded in dot mode, special circuitry has been included to shut off LED No. 10 of the first device when

Mode Pin Functional Description

(Continued)

LED No. 1 of the second device comes on. The connection for cascading in dot mode has already been described and is depicted below.

As long as the input signal voltage is below the threshold of the second LM3914, LED No. 11 is off. Pin 9 of LM3914 No. 1 thus sees effectively an open circuit so the chip is in dot mode. As soon as the input voltage reaches the threshold of LED No. 11, pin 9 of LM3914 No. 1 is pulled an LED drop (1.5V or more) below V_{LED}. This condition is sensed by comparator C2, referenced 600 mV below V_{LED}. This forces the output of C2 low, which shuts off output transistor Q2, extinguishing LED No. 10.

V_{LED} is sensed via the 20k resistor connected to pin 11. The very small current (less than 100 µA) that is diverted from LED No. 9 does not noticeably affect its intensity.

An auxiliary current source at pin 1 keeps at least 100 µA flowing through LED No. 11 even if the input voltage rises high enough to extinguish the LED. This ensures that pin 9 of LM3914 No. 1 is held low enough to force LED No. 10 off when *any* higher LED is illuminated. While 100 µA does not normally produce significant LED illumination, it may be noticeable when using high-efficiency LEDs in a dark environment. If this is bothersome, the simple cure is to shunt LED No. 11 with a 10k resistor. The 1V IR drop is more than the 900 mV worst case required to hold off LED No. 10 yet small enough that LED No. 11 does not conduct significantly.

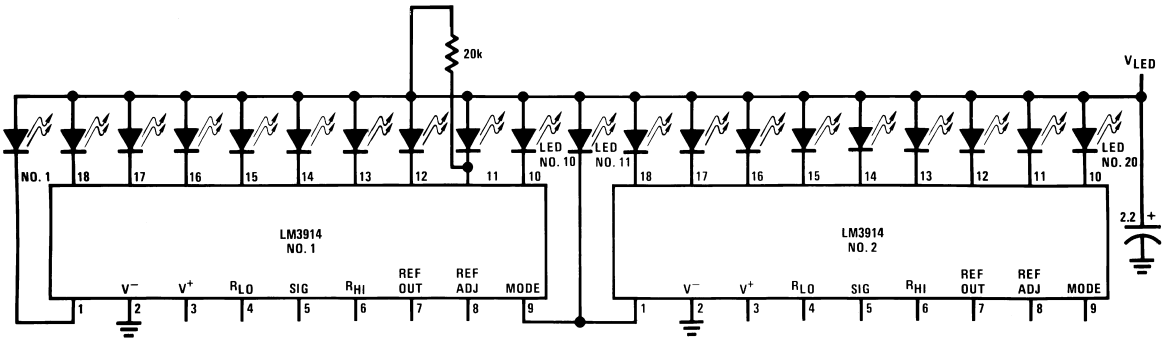
OTHER DEVICE CHARACTERISTICS

The LM3914 is relatively low-powered itself, and since any number of LEDs can be powered from about 3V, it is a very efficient display driver. Typical standby supply current (all LEDs OFF) is 1.6 mA (2.5 mA max). However, any reference loading adds 4 times that current drain to the V^+ (pin 3) supply input. For example, an LM3914 with a 1 mA reference pin load (1.3k), would supply almost 10 mA to every LED while drawing only 10 mA from its V^+ pin supply. At full-scale, the IC is typically drawing less than 10% of the current supplied to the display.

The display driver does not have built-in hysteresis so that the display does not jump instantly from one LED to the next. Under rapidly changing signal conditions, this cuts down high frequency noise and often an annoying flicker. An "overlap" is built in so that at no time between segments are all LEDs completely OFF in the dot mode. Generally 1 LED fades in while the other fades out over a mV or more of range (Note 3). The change may be much more rapid between LED No. 10 of one device and LED No. 1 of a *second* device "chained" to the first.

The LM3914 features individually current regulated LED driver transistors. Further internal circuitry detects when any driver transistor goes into saturation, and prevents other circuitry from drawing excess current. This results in the ability of the LM3914 to drive and regulate LEDs powered from a pulsating DC power source, i.e., largely unfiltered. (Due to possible oscillations at low voltages a nominal bypass capacitor consisting of a 2.2 µF solid tantalum connected from the pulsating LED supply to pin 2 of the LM3914 is recommended.) This ability to operate with low or fluctuating voltages also allows the display driver to interface with logic circuitry, opto-coupled solid-state relays, and low-current incandescent lamps.

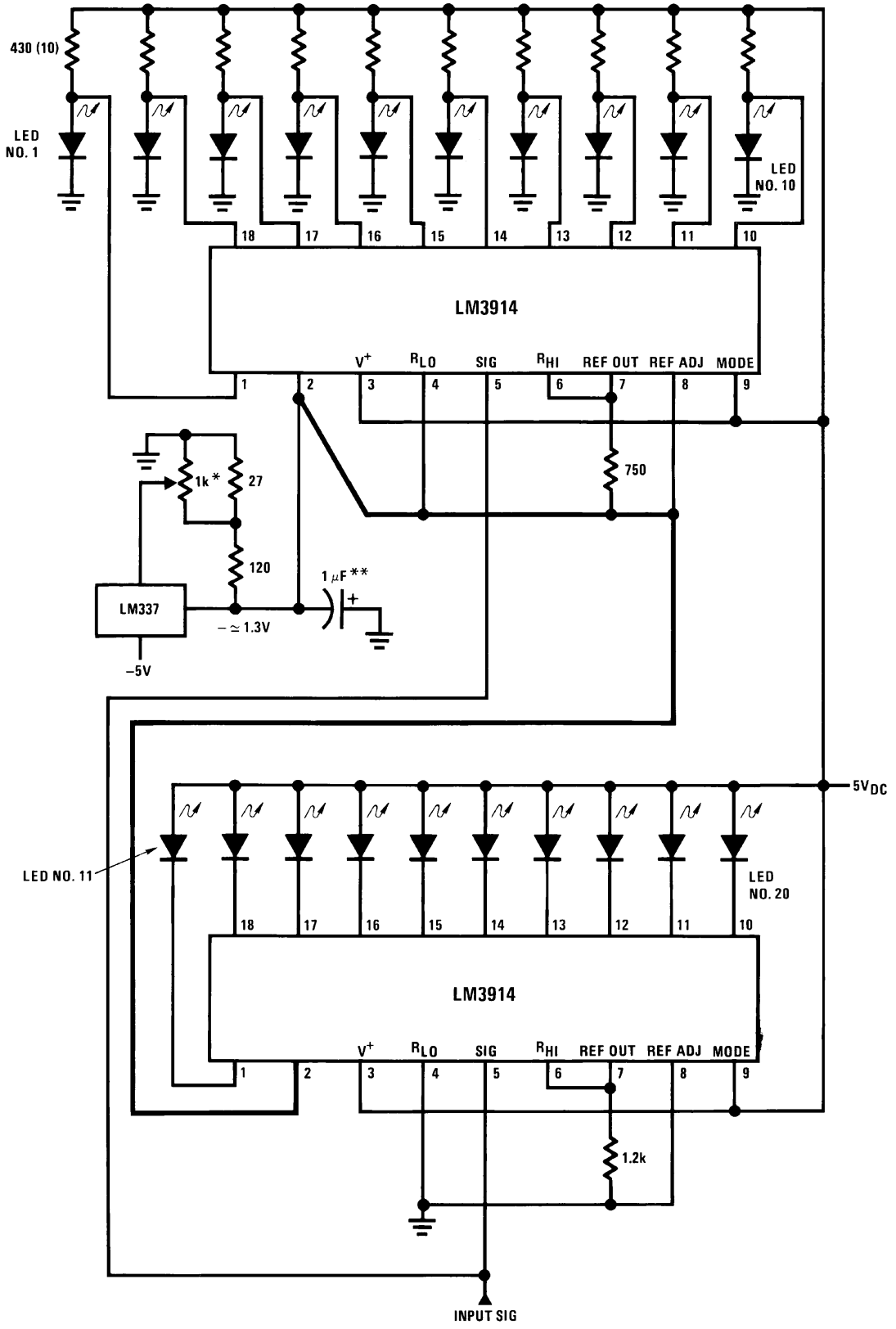
Cascading LM3914s in Dot Mode



DS007970-6

Typical Applications

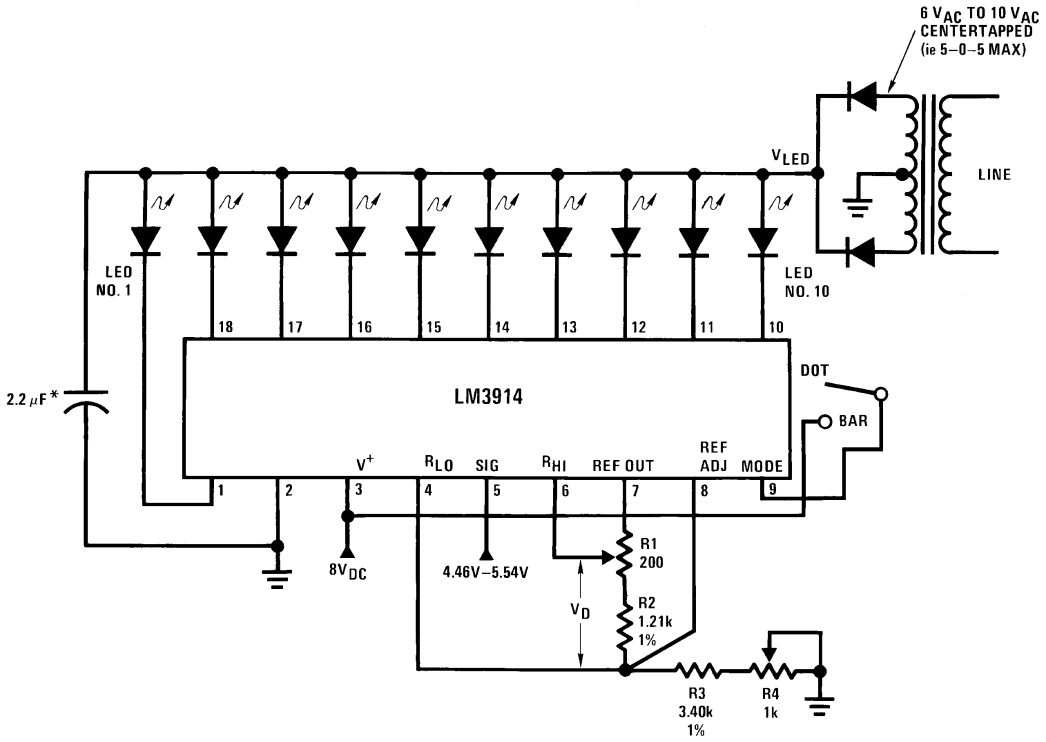
Zero-Center Meter, 20-Segment



DS007970-7

Typical Applications (Continued)

Expanded Scale Meter, Dot or Bar



DS007970-8

*This application illustrates that the LED supply needs practically no filtering

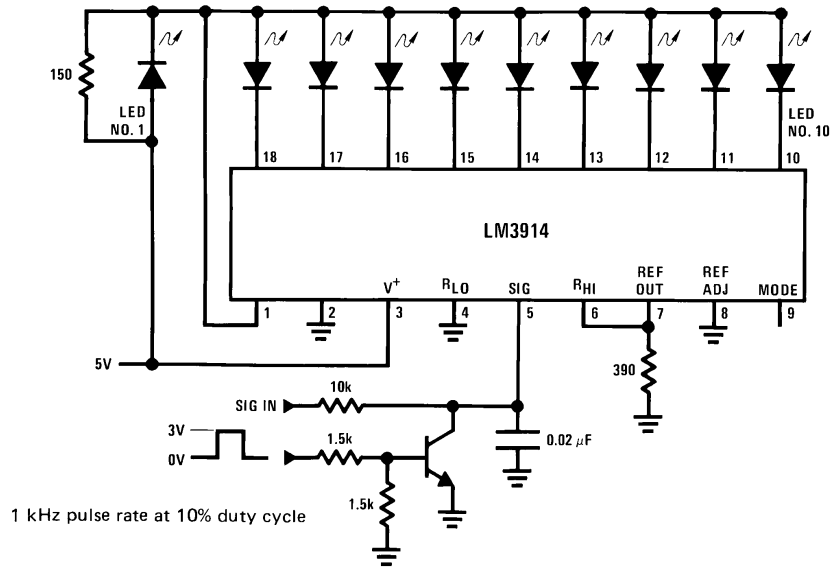
Calibration: With a precision meter between pins 4 and 6 adjust R1 for voltage V_D of 1.20V. Apply 4.94V to pin 5, and adjust R4 until LED No. 5 just lights. The adjustments are non-interacting.

Application Example:
Grading 5V Regulators

Highest No. LED on	Color	$V_{OUT(MIN)}$
10	Red	5.54
9	Red	5.42
8	Yellow	5.30
7	Green	5.18
6	Green	5.06
5V		
5	Green	4.94
4	Green	4.82
3	Yellow	4.7
2	Red	4.58
1	Red	4.46

Typical Applications (Continued)

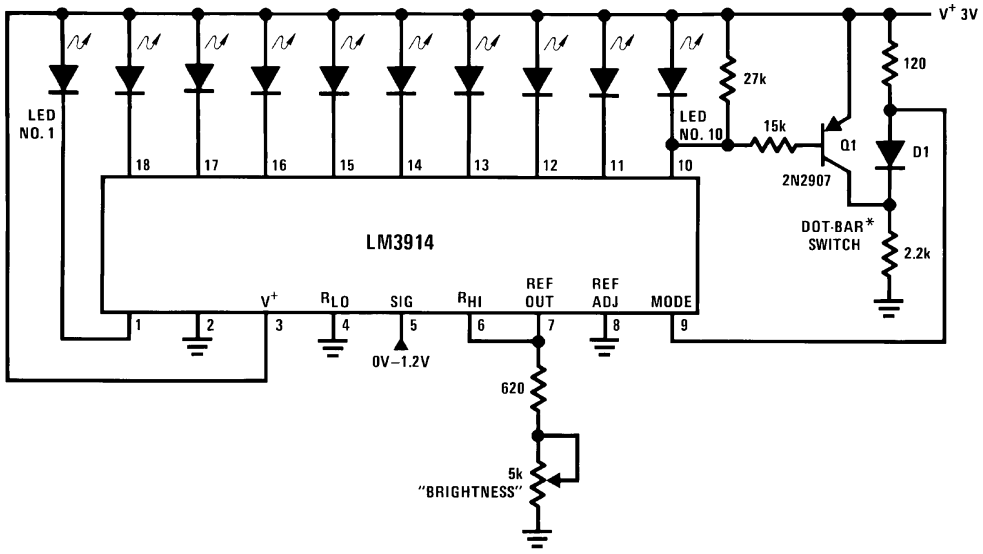
"Exclamation Point" Display



DS007970-9

LEDs light up as illustrated with the upper lit LED indicating the actual input voltage. The display appears to increase resolution and provides an analog indication of overrange.

Indicator and Alarm, Full-Scale Changes Display from Dot to Bar

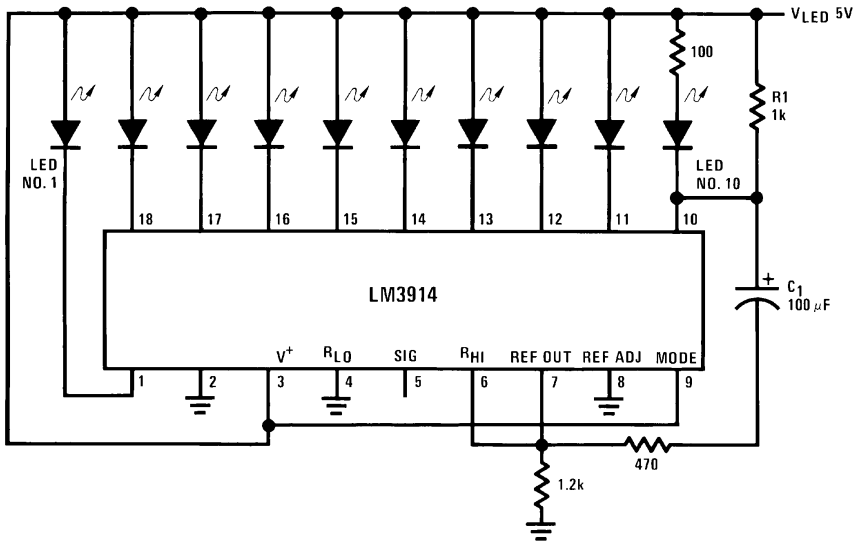


DS007970-10

*The input to the Dot-Bar Switch may be taken from cathodes of other LEDs. Display will change to bar as soon as the LED so selected begins to light.

Typical Applications (Continued)

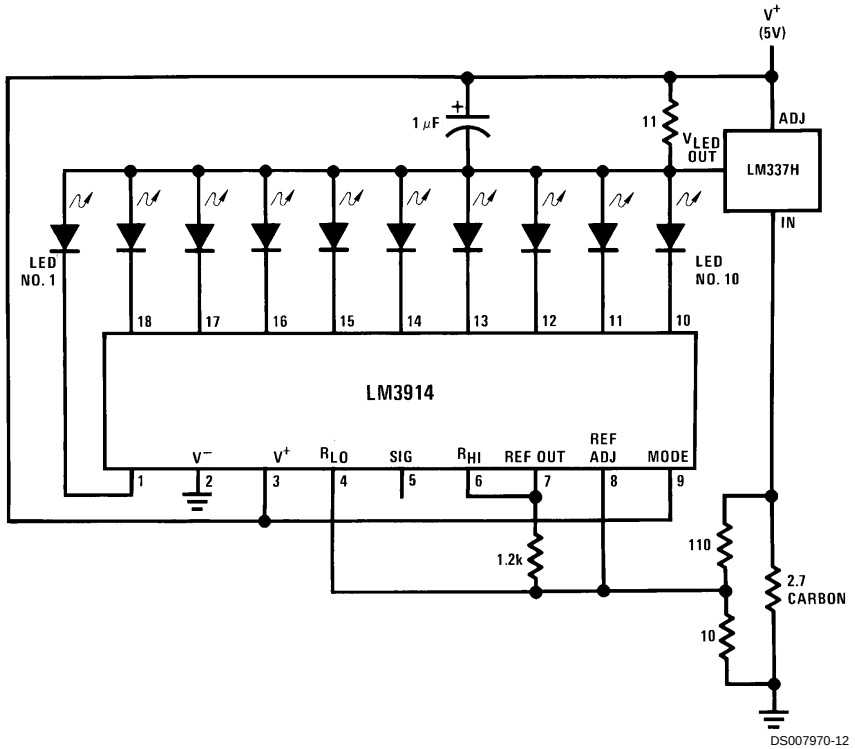
Bar Display with Alarm Flasher



DS007970-11

Full-scale causes the full bar display to flash. If the junction of R1 and C1 is connected to a different LED cathode, the display will flash when that LED lights, and at any higher input signal.

Adding Hysteresis (Single Supply, Bar Mode Only)

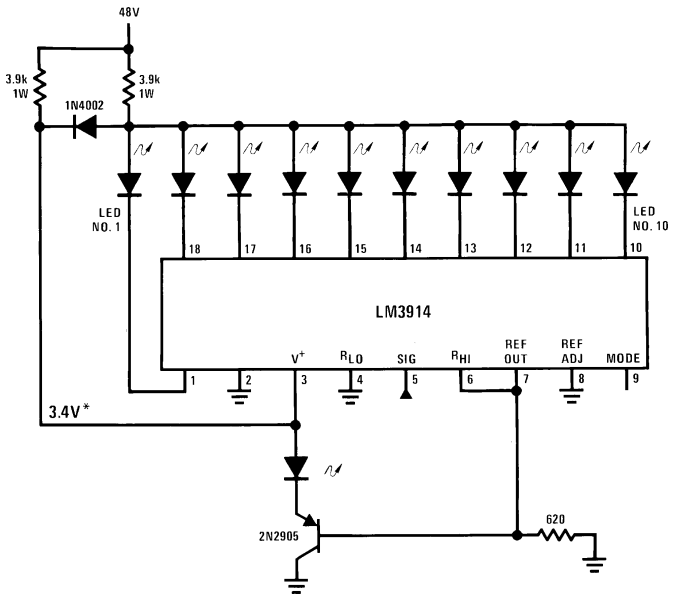


DS007970-12

Hysteresis is 0.5 mV to 1 mV

Typical Applications (Continued)

Operating with a High Voltage Supply (Dot Mode Only)

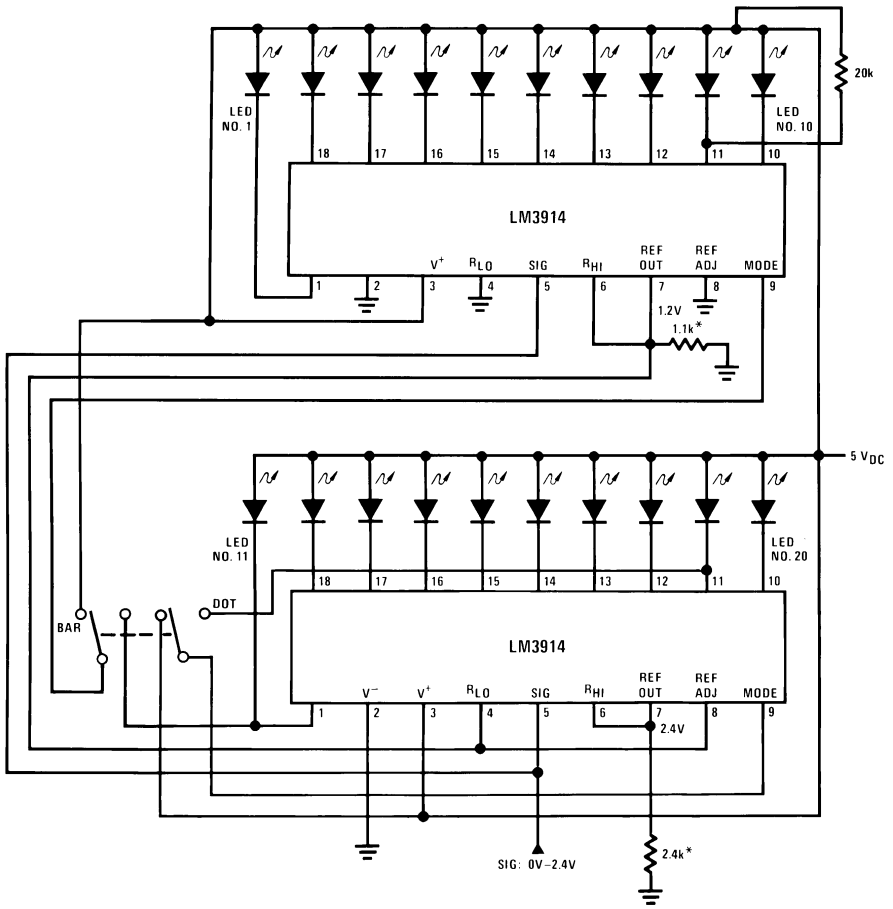


DS007970-13

The LED currents are approximately 10 mA, and the LM3914 outputs operate in saturation for minimum dissipation.
*This point is partially regulated and decreases in voltage with temperature. Voltage requirements of the LM3914 also decrease with temperature.

Typical Applications (Continued)

20-Segment Meter with Mode Switch



DS007970-14

*The exact wiring arrangement of this schematic shows the need for Mode Select (pin 9) to sense the V^+ voltage exactly as it appears on pin 3.
Programs LEDs to 10 mA

Application Hints

Three of the most commonly needed precautions for using the LM3914 are shown in the first typical application drawing showing a 0V–5V bar graph meter. The most difficult problem occurs when large LED currents are being drawn, especially in bar graph mode. These currents flowing out of the ground pin cause voltage drops in external wiring, and thus errors and oscillations. Bringing the return wires from signal sources, reference ground and bottom of the resistor string (as illustrated) to a single point very near pin 2 is the best solution.

Long wires from V_{LED} to LED anode common can cause oscillations. Depending on the severity of the problem 0.05 µF to 2.2 µF decoupling capacitors from LED anode common to pin 2 will damp the circuit. If LED anode line wiring is inaccessible, often similar decoupling from pin 1 to pin 2 will be sufficient.

If LED turn ON seems slow (bar mode) or several LEDs light (dot mode), oscillation or excessive noise is usually the problem. In cases where proper wiring and bypassing fail to stop oscillations, V^+ voltage at pin 3 is usually below suggested limits. Expanded scale meter applications may have one or both ends of the internal voltage divider terminated at relatively high value resistors. These high-impedance ends should be bypassed to pin 2 with at least a 0.001 µF capacitor, or up to 0.1 µF in noisy environments.

Power dissipation, especially in bar mode should be given consideration. For example, with a 5V supply and all LEDs programmed to 20 mA the driver will dissipate over 600 mW. In this case a 7.5Ω resistor in series with the LED supply will cut device heating in half. The negative end of the resistor should be bypassed with a 2.2 µF solid tantalum capacitor to pin 2 of the LM3914.

Turning OFF of most of the internal current sources is accomplished by pulling positive on the reference with a current source or resistance supplying 100 µA or so. Alternately, the input signal can be gated OFF with a transistor switch.

Other special features and applications characteristics will be illustrated in the following applications schematics. Notes have been added in many cases, attempting to cover any special procedures or unusual characteristics of these applications. A special section called “Application Tips for the LM3914 Adjustable Reference” has been included with these schematics.

Application Hints (Continued)

APPLICATION TIPS FOR THE LM3914 ADJUSTABLE REFERENCE

GREATLY EXPANDED SCALE (BAR MODE ONLY)

Placing the LM3914 internal resistor divider in parallel with a section (≅230Ω) of a stable, low resistance divider greatly reduces voltage changes due to IC resistor value changes with temperature. Voltage V_1 should be trimmed to 1.1V first by use of R2. Then the voltage V_2 across the IC divider string can be adjusted to 200 mV, using R5 without affecting V_1. LED current will be approximately 10 mA.

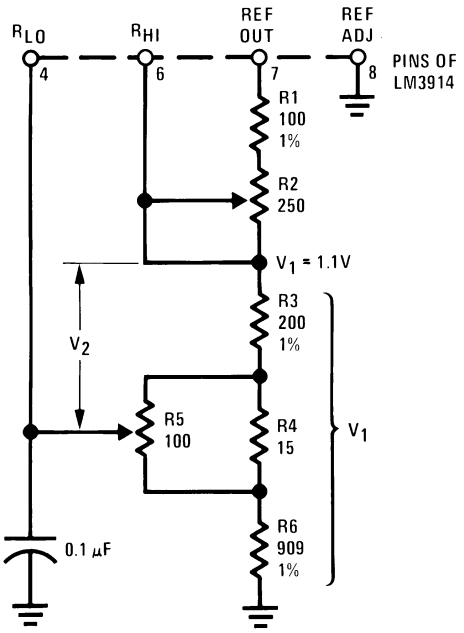
NON-INTERACTING ADJUSTMENTS FOR EXPANDED SCALE METER (4.5V to 5V, Bar *or* Dot Mode)

This arrangement allows independent adjustment of LED brightness regardless of meter span and zero adjustments.

First, V_1 is adjusted to 5V, using R2. Then the span (voltage across R4) can be adjusted to exactly 0.5V using R6 without affecting the previous adjustment.

R9 programs LED currents within a range of 2.2 mA to 20 mA after the above settings are made.

Greatly Expanded Scale (Bar Mode Only)



DS007970-15

ADJUSTING LINEARITY OF SEVERAL STACKED DIVIDERS

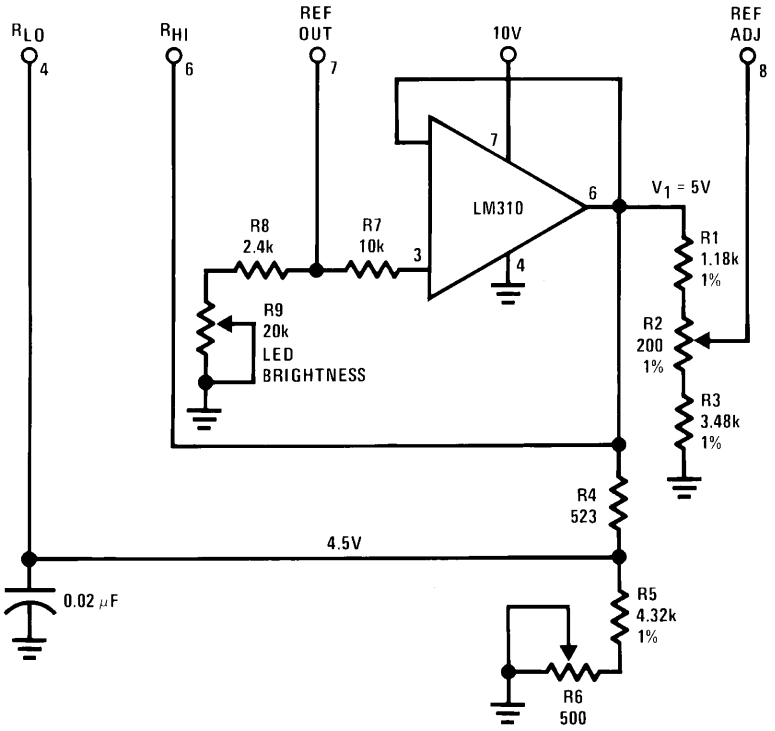
Three internal voltage dividers are shown connected in series to provide a 30-step display. If the resulting analog meter is to be accurate and linear the voltage on each divider must be adjusted, preferably without affecting any other adjustments. To do this, adjust R2 first, so that the voltage across R5 is exactly 1V. Then the voltages across R3 and R4 can be independently adjusted by shunting each with selected resistors of 6 kΩ or higher resistance. This is possible because the reference of LM3914 No. 3 is acting as a constant current source.

The references associated with LM3914s No. 1 and No. 2 should have their Ref Adj pins (pin 8) wired to ground, and their Ref Outputs loaded by a 620Ω resistor to ground. This makes available similar 20 mA current outputs to all the LEDs in the system.

If an independent LED brightness control is desired (as in the previous application), a unity gain buffer, such as the LM310, should be placed between pin 7 and R1, similar to the previous application.

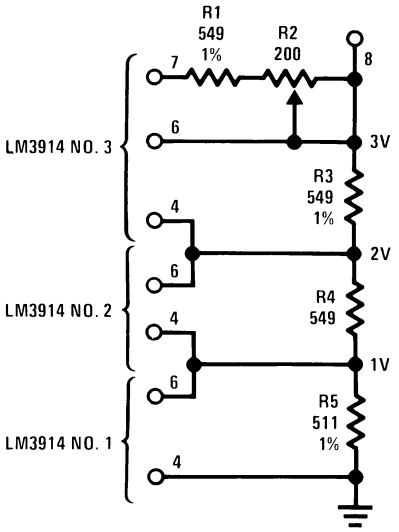
Application Hints (Continued)

Non-Interacting Adjustments for Expanded Scale Meter (4.5V to 5V, Bar *or* Dot Mode)



DS007970-16

Adjusting Linearity of Several Stacked Dividers



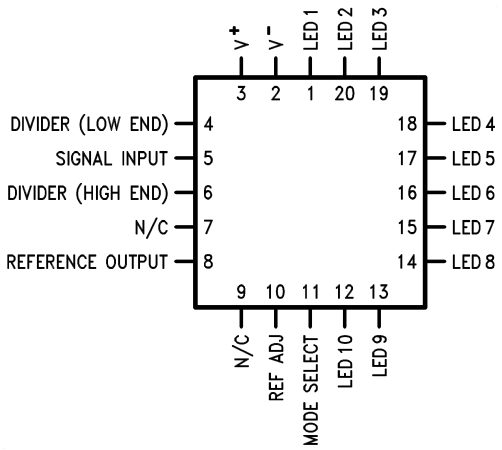
DS007970-17

Other Applications

- "Slow" — fade bar or dot display (doubles resolution)
- 20-step meter with single pot brightness control
- 10-step (or multiples) programmer
- Multi-step or "staging" controller
- Combined controller and process deviation meter
- Direction and rate indicator (to add to DVMs)
- Exclamation point display for power saving
- Graduations can be added to dot displays. Dimly light every other LED using a resistor to ground
- Electronic "meter-relay" — display could be circle or semi-circle
- Moving "hole" display — indicator LED is dark, rest of bar lit
- Drives vacuum-fluorescent and LCDs using added passive parts

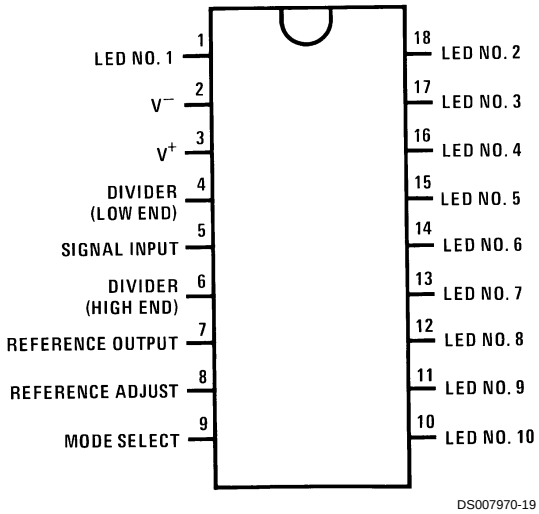
Connection Diagrams

Plastic Chip Carrier Package



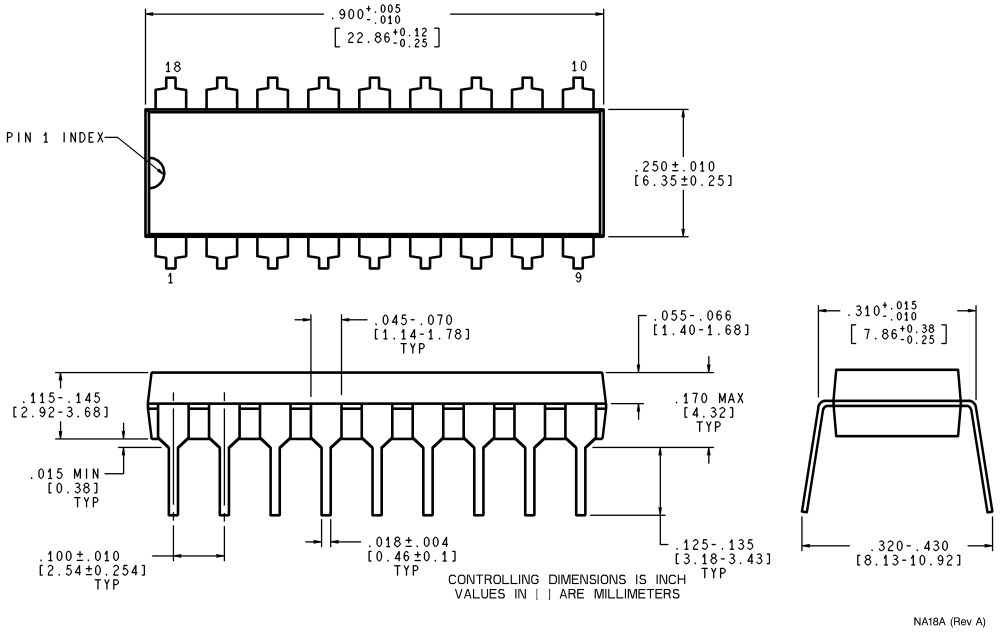
Top View
Order Number LM3914V
See NS Package Number V20A

Dual-in-Line Package



Top View
Order Number LM3914N-1
See NS Package Number NA18A
Order Number LM3914N *
See NS Package Number N18A
*** Discontinued, Life Time Buy date 12/20/99**

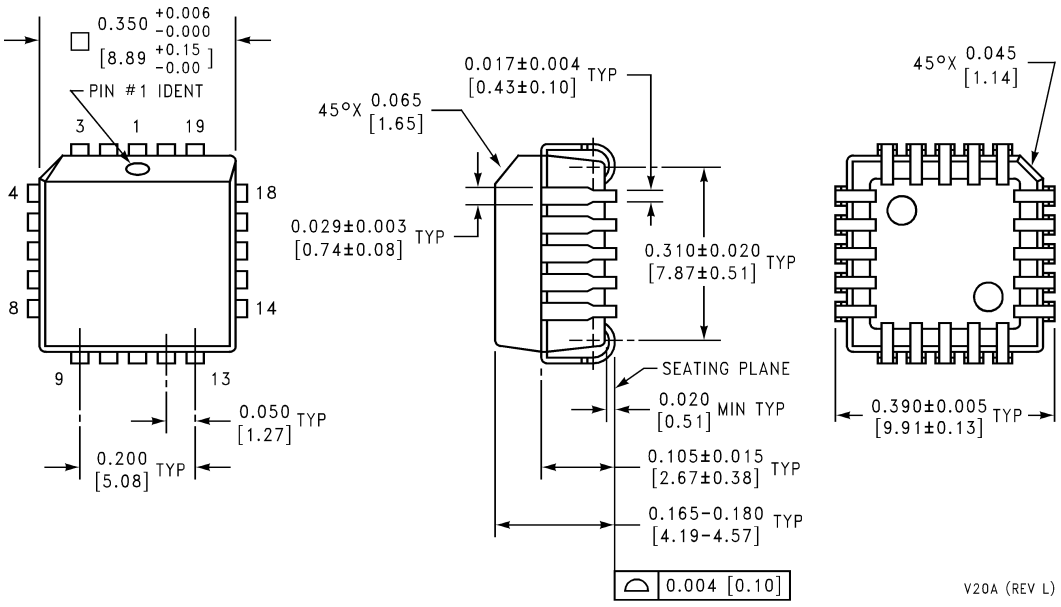
Physical Dimensions inches (millimeters) unless otherwise noted



Note: Unless otherwise specified.

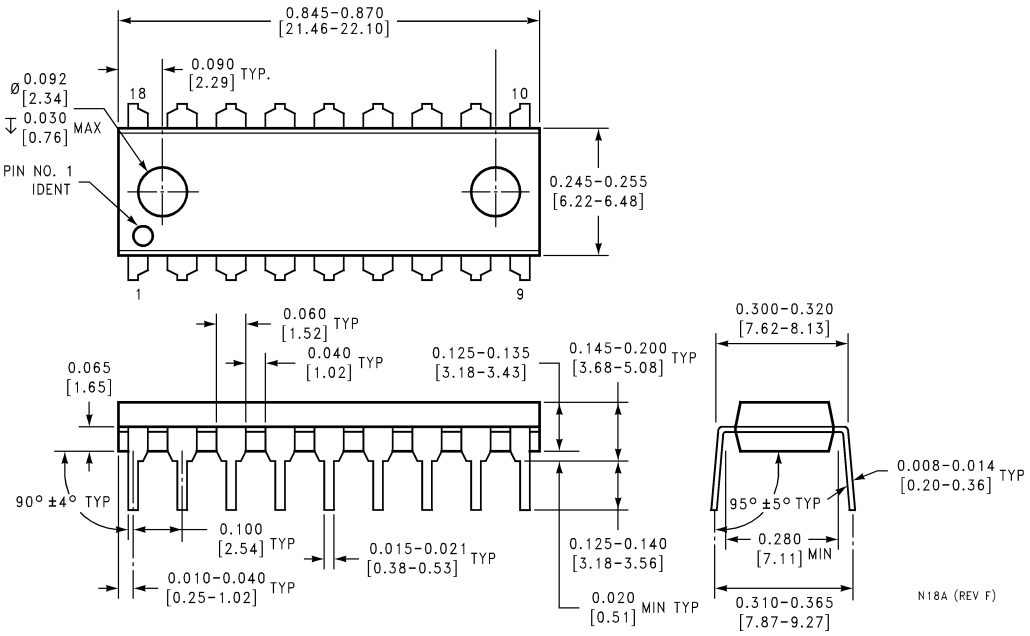
1. Standard Lead Finish:
   200 microinches /5.08 micrometer minimum
   lead/tin 37/63 or 15/85 on alloy 42 or equivalent or copper
2. Reference JEDEC registration MS-001, Variation AC, dated May 1993.

Dual-In-Line Package (N)
Order Number LM3914N-1
NS Package Number NA18A



Plastic Chip Carrier Package (V)
Order Number LM3914V
NS Package Number V20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Dual-In-Line Package (N)
Order Number LM3914N *
NS Package Number N18A
*** Discontinued, Life Time Buy date 12/20/99**

LIFE SUPPORT POLICY

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19-0020; Rev 0; 6/92

MAXIM

8th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

General Description

The MAX293/MAX294/MAX297 are easy-to-use, 8th-order, lowpass, elliptic, switched-capacitor filters that can be set up with corner frequencies from 0.1Hz to 25kHz (MAX293/MAX294) or from 0.1Hz to 50kHz (MAX297).

The MAX293/MAX297's 1.5 transition ratio provides sharp rolloff and -80dB of stopband rejection. The MAX294's 1.2 transition ratio provides the steepest rolloff and -58dB of stopband rejection. All three filters have fixed responses, so the design task is limited to selecting the clock frequency that controls the filter's corner frequency.

An external capacitor is used to generate a clock using the internal oscillator, or an external clock signal can be used. An uncommitted op amp (noninverting input grounded) is provided for building a continuous-time lowpass filter for post-filtering or anti-aliasing. Steep rolloff and high order make these filters ideal for anti-aliasing applications that require maximum bandwidth, and for communication applications that require filtering signals in close proximity within the frequency domain.

The MAX293/MAX294/MAX297 are available in 8-pin DIP and 16-pin wide SO packages, delivering aggressive performance from a tiny area.

Applications

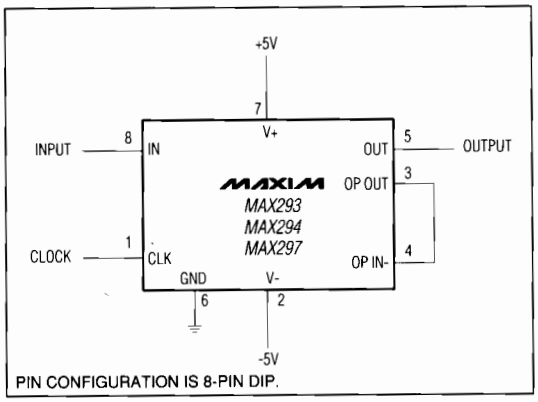
Data-Acquisition Systems

Anti-Aliasing

DAC Post-Filtering

Voice/Data Signal Filtering

Typical Operating Circuit



PIN CONFIGURATION IS 8-PIN DIP.

Features

- ♦ **8th-Order Lowpass Elliptic Filters**
- ♦ **Clock-Tunable Corner-Frequency Range:**
  0.1Hz to 25kHz (MAX293/MAX294)
  0.1Hz to 50kHz (MAX297)
- ♦ **No External Resistors or Capacitors Required**
- ♦ **Internal or External Clock**
- ♦ **Clock to Corner Frequency Ratio:**
  100:1 (MAX293/294)
  50:1 (MAX297)
- ♦ **Operate with a Single +5V Supply or Dual ±5V Supplies**
- ♦ **Uncommitted Op Amp for Anti-Aliasing or Clock-Noise Filtering**
- ♦ **8-Pin DIP and 16-Pin Wide SO Packages**

Ordering Information

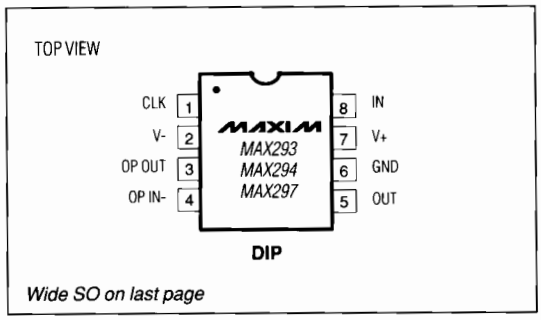
PART	TEMP. RANGE	PIN-PACKAGE
MAX293CPA	0°C to +70°C	8 Plastic DIP
MAX293CWE	0°C to +70°C	16 Wide SO
MAX293C/D	0°C to +70°C	Dice*
MAX293EPA	-40°C to +85°C	8 Plastic DIP
MAX293EWE	-40°C to +85°C	16 Wide SO
MAX293MJA	-55°C to +125°C	8 CERDIP**
MAX294CPA	0°C to +70°C	8 Plastic DIP
MAX294CWE	0°C to +70°C	16 Wide SO
MAX294C/D	0°C to +70°C	Dice*

Ordering Information continued on last page.

* *Contact factory for dice specifications.*

** *Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations



Wide SO on last page

8th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to V-) 12V
Input Voltage at Any Pin ..... (V- - 0.3V) ≤ V_{IN} ≤ (V+ + 0.3V)
Continuous Power Dissipation
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ...727mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) ...762mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX29_C_ ..... 0°C to +70°C
MAX29_E_ ..... -40°C to +85°C
MAX29_MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, filter output measured at OUT pin, 20kΩ load resistor to ground at OUT, f_{CLK} = 100kHz (MAX293/MAX294) or f_{CLK} = 50kHz (MAX297) T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
FILTER CHARACTERISTICS						
Corner-Frequency Range	MAX293/MAX294			0.1-25k		Hz
	MAX297			0.1-50k		
Clock to Corner Frequency Ratio	MAX293/MAX294			100:1		
	MAX297			50:1		
Clock to Corner Frequency Tempco	MAX293			8		ppm/°C
	MAX294			7		
	MAX297			4		
Insertion Gain Relative to DC Gain (Note 1)	MAX293	$f_{IN} = 0.381F_O$	0.12	-0.10	-0.17	dB
		$f_{IN} = 0.594F_O$	0.12	0.02	-0.17	
		$f_{IN} = 0.759F_O$	0.12	-0.11	-0.17	
		$f_{IN} = 0.866F_O$	0.12	-0.03	-0.17	
		$f_{IN} = 0.939F_O$	0.12	-0.11	-0.17	
		$f_{IN} = 0.993F_O$	0.12	0.04	-0.17	
		$f_{IN} = 1.000F_O$	0.12	0.01	-0.17	
		$f_{IN} = 1.500F_O$	-75	-78		
		$f_{IN} = 1.610F_O$	-80	-87		
		$f_{IN} = 2.020F_O$	-80	-84		
		$f_{IN} = 4.020F_O$	-80	-84		
	MAX294	$f_{IN} = 0.425F_O$	0.10	-0.11	-0.17	
		$f_{IN} = 0.644F_O$	0.10	0.02	-0.17	
		$f_{IN} = 0.802F_O$	0.10	-0.10	-0.17	
		$f_{IN} = 0.895F_O$	0.10	-0.03	-0.17	
		$f_{IN} = 0.946F_O$	0.10	-0.07	-0.17	
		$f_{IN} = 0.994F_O$	0.26	0.16	-0.17	
		$f_{IN} = 1.000F_O$	0.26	0.13	-0.17	
		$f_{IN} = 1.200F_O$	-51	-54		
		$f_{IN} = 1.270F_O$	-57	-62		
		$f_{IN} = 1.530F_O$	-57	-60		
		$f_{IN} = 2.840F_O$	-57	-60		

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5V, V- = -5V, filter output measured at OUT pin, 20kΩ load resistor to ground at OUT, f_{CLK} = 100kHz (MAX293/MAX294) or f_{CLK} = 50kHz (MAX297) T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Insertion Gain Relative to DC Gain (Note 1) (continued)	MAX297	f_{IN} = 0.377F_O	0.10	-0.11	-0.17	dB
		f_{IN} = 0.591F_O	0.10	0.03	-0.17	
		f_{IN} = 0.754F_O	0.10	-0.12	-0.17	
		f_{IN} = 0.873F_O	0.10	0.02	-0.17	
		f_{IN} = 0.944F_O	0.10	-0.07	-0.17	
		f_{IN} = 0.996F_O	0.20	0.11	-0.17	
		f_{IN} = 1.000F_O	0.20	0.10	-0.17	
		f_{IN} = 1.500F_O	-75	-79		
		f_{IN} = 1.610F_O	-80	-87		
		f_{IN} = 2.020F_O	-80	-84		
		f_{IN} = 4.000F_O	-80	-85		
Passband Ripple	MAX293			0.15		dB
	MAX294			0.27		
	MAX297			0.23		
Output DC Swing			±4			V
Output Offset Voltage	IN = GND			±150	±400	mV
DC Insertion Gain with Output Offset Removed			-0.15	±0.01	0.15	dB
Total Harmonic Distortion plus Noise	T_A = +25°C	MAX293		-71		dB
		MAX294		-69		
		MAX297		-77		
Clock Feedthrough	T_A = +25°C			5.0		mVp-p
Output Drive Capability			20	10		kΩ
CLOCK						
Internal Oscillator Frequency	C_{OSC} = 1000pF		29	35	43	kHz
Internal Oscillator Current Source/Sink	V_{CLK} = 0V or 5V			±70	±120	µA
Clock Input (Note 2) High			4.0			V
Low					1.0	
UNCOMMITTED OP AMP						
Input Offset Voltage				±10	±50	mV
Output Drive Capability			20	10		kΩ
Output DC Swing			±4			V
Gain-Bandwidth Product				4		MHz
POWER REQUIREMENTS						
Supply Voltage Dual Supply			±2.375		±5.5	V
Single Supply	V- = 0V, GND = V+/2		4.75		11.0	
Supply Current	V+ = 5V, V- = -5V, V_{CLK} = 0V to 5V			15.0	22.0	mA
	V+ = 2.375V, V- = -2.375V, V_{CLK} = -2V to 2V			7.0	12.0	

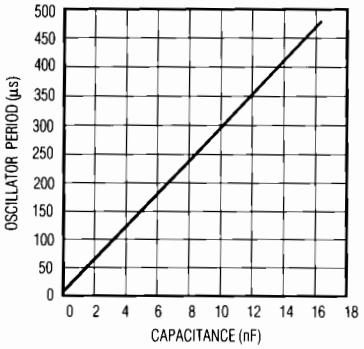
Note 1: Test frequencies selected at ripple peaks and troughs.
Note 2: Guaranteed by design.

8th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

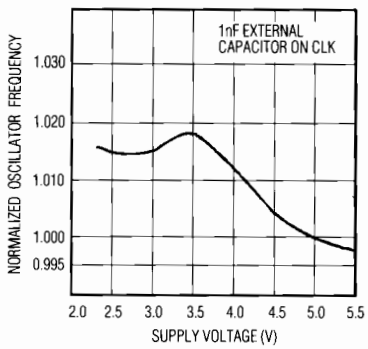
Typical Operating Characteristics

(V+ = 5V, V- = -5V, f_{CLK} = 100kHz (MAX293/MAX294) or f_{CLK} = 50kHz (MAX297), T_A = +25°C, unless otherwise noted.)

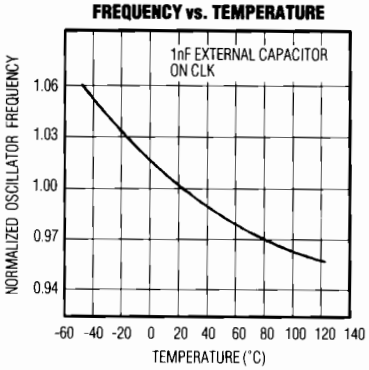
INTERNAL OSCILLATOR PERIOD vs. CAPACITANCE VALUE



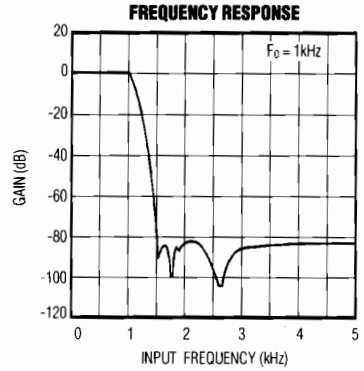
NORMALIZED INTERNAL OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



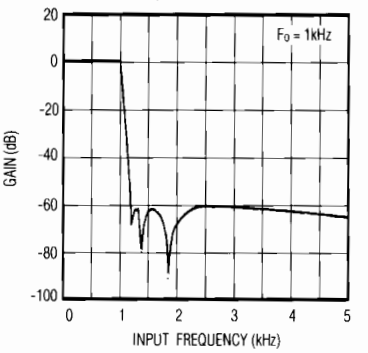
NORMALIZED INTERNAL OSCILLATOR FREQUENCY vs. TEMPERATURE



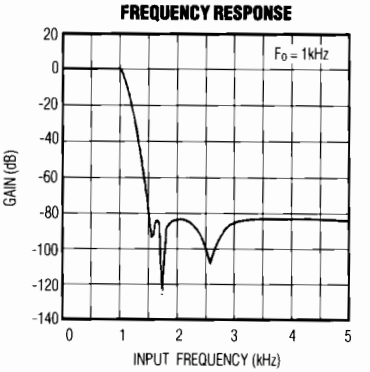
MAX293 FREQUENCY RESPONSE



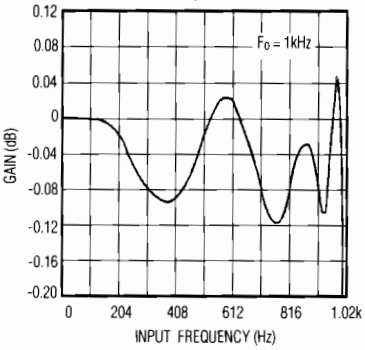
MAX294 FREQUENCY RESPONSE



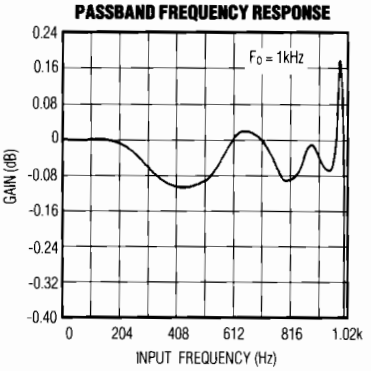
MAX297 FREQUENCY RESPONSE



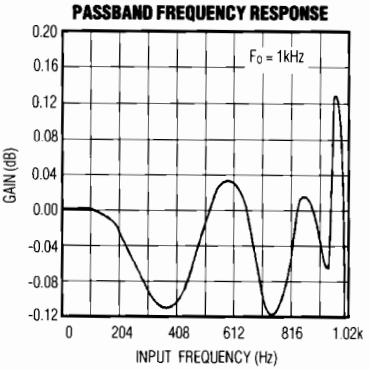
MAX293 PASSBAND FREQUENCY RESPONSE



MAX294 PASSBAND FREQUENCY RESPONSE



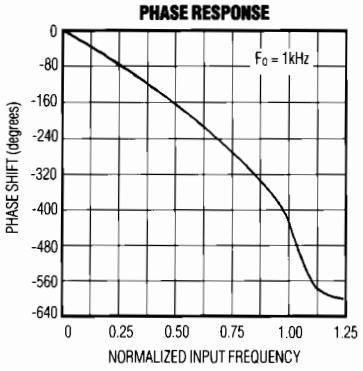
MAX297 PASSBAND FREQUENCY RESPONSE



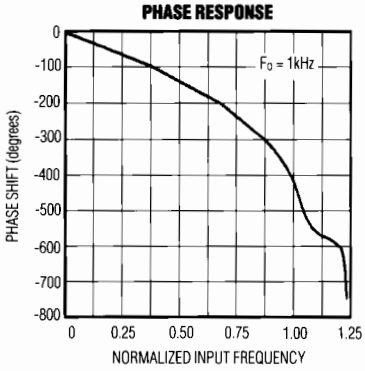
Typical Operating Characteristics (continued)

(V+ = 5V, V- = -5V, f_{CLK} = 100kHz (MAX293/MAX294) or f_{CLK} = 50kHz (MAX297), T_A = +25°C, unless otherwise noted.)

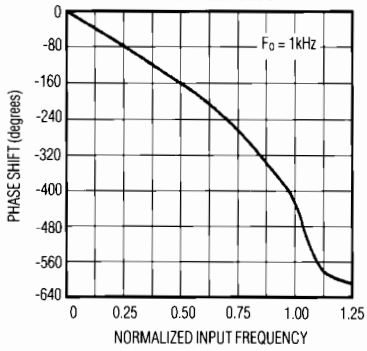
MAX293 PHASE RESPONSE



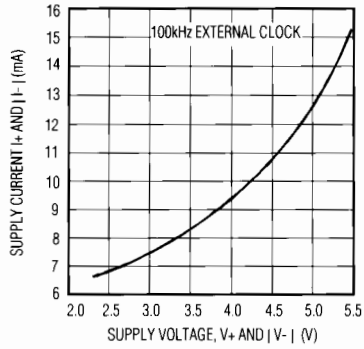
MAX294 PHASE RESPONSE



MAX297 PHASE RESPONSE



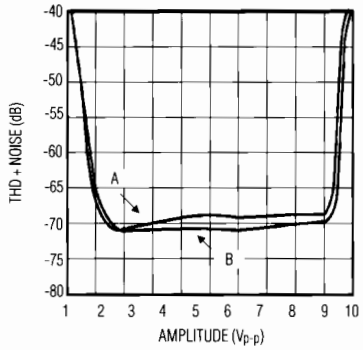
SUPPLY CURRENT vs. SUPPLY VOLTAGE



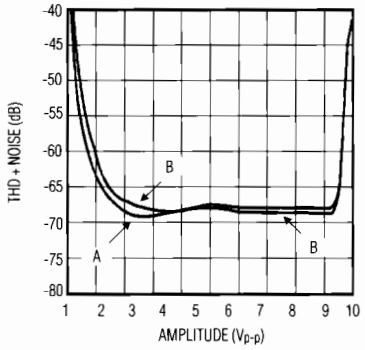
LABEL	f_{CLK} (Hz)	F_O (kHz)	INPUT FREQ. (Hz)	MEASUREMENT BANDWIDTH (kHz)
A	200k	2	200	30
B	1M	10	1k	80
C	200k	4	400	30
D	1M	20	2k	80

(V+ = 5V, V- = -5V, R_{LOAD} = 20kΩ, T_A = +25°C, unless otherwise noted.)

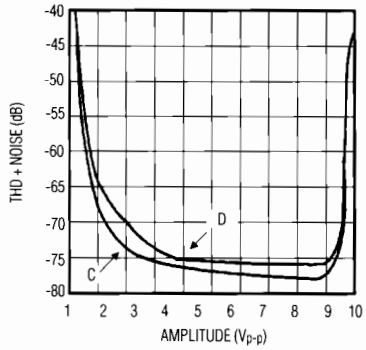
MAX293 THD + NOISE vs. INPUT SIGNAL AMPLITUDE



MAX294 THD + NOISE vs. INPUT SIGNAL AMPLITUDE



MAX297 THD + NOISE vs. INPUT SIGNAL AMPLITUDE



8th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

Pin Description

PIN		NAME	FUNCTION
8-PIN DIP	16-PIN SO		
	1,2,7,8,9, 10,15,16	N.C.	No Connect—not internally connected
1	3	CLK	Clock Input—use internal or external clock.
2	4	V-	Negative Supply pin. Dual supplies: -2.375V to -5.5V. Single supply: V- = 0V.
3	5	OP OUT	Uncommitted Op-Amp Output
4	6	OP IN-	Inverting Input to the uncommitted op amp. The noninverting op amp is internally tied to GND.
5	11	OUT	Filter Output
6	12	GND	Ground. In single-supply operation, GND must be biased to the mid-supply voltage level.
7	13	V+	Positive Supply pin. Dual supplies: +2.375V to +5.5V. Single supply: +4.75V to +11.0V.
8	14	IN	Filter Input

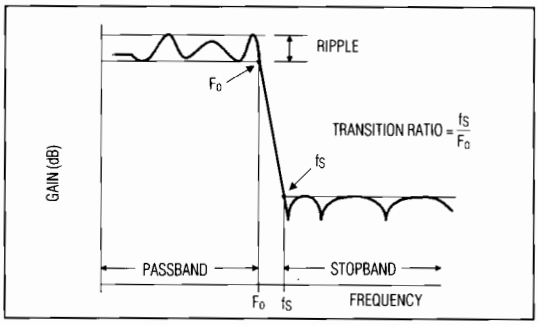


Figure 1. Elliptic Filter Response

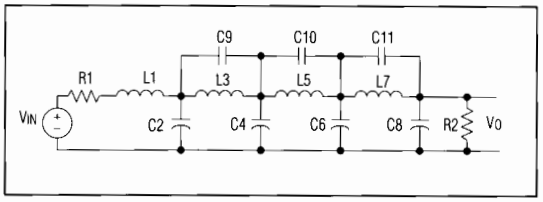


Figure 2. 8th-Order Ladder Filter Network

Detailed Description

The MAX293/MAX294/MAX297 8th-order (eight-pole), elliptic, switched-capacitor, lowpass filters provide the steepest possible rolloff with frequency of the four common filter types (Butterworth, Bessel, Chebyshev, elliptic). The high Q value of the poles near the passband edge combined with stopband zeros allows for the sharp attenuation characteristic of elliptic filters. The MAX293/MAX297 have a 1.5 transition ratio and typically -78dB and -79dB of stopband rejection, respectively; the MAX294 has a 1.2 transition ratio (providing the steepest rolloff) and typically -58dB of stopband rejection.

Passband Ripple and Corner Frequency

The MAX293/MAX294 operate with a 100:1 clock to corner frequency ratio and a 25kHz maximum corner frequency, with corner frequency defined as the point where the filter output attenuation falls just below the passband ripple (Figure 1). The passband ripple is typically 0.15dB (MAX293) and 0.27dB (MAX294). The MAX297 operates with a 50:1 clock to corner frequency ratio and a 50kHz maximum corner frequency. Its passband ripple is typically 0.23dB.

Transition Ratio and Stopband Response

In the frequency domain, the first transmission zero causes the filter's amplitude to drop to a minimum level. Beyond this zero, the response rises as the frequency increases until the next transmission zero. Several repetitions of this response create the filter's stopband comb shape (Figure 1). The stopband begins at f_S. At frequencies above f_S, the filter's gain does not exceed the gain at f_S. The transition ratio is defined as the ratio of the stopband frequency to the corner frequency.

Background Information

Most switched-capacitor filters are designed with biquadratic sections. Each section implements two filtering poles, and the sections can be cascaded to produce higher-order filters. The advantage to this approach is ease of design. However, this type of design is highly sensitive to component variations if any section's Q is high.

An alternative approach is to emulate a passive network using switched-capacitor integrators with summing and scaling. The passive network can be synthesized using CAD programs, or can be found in many filter books. Figure 2 shows the basic ladder filter structure.

A switched-capacitor filter that emulates a passive ladder filter retains many of its advantages. The filter's component sensitivity is low when compared to a cascaded biquad design because each component affects the entire filter shape, not just one pole pair. That is, a mismatched component in a biquad design will have a concentrated error on its respective poles, while the

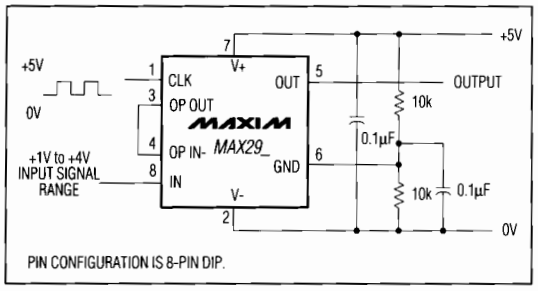


Figure 3. +5V Single-Supply Operation

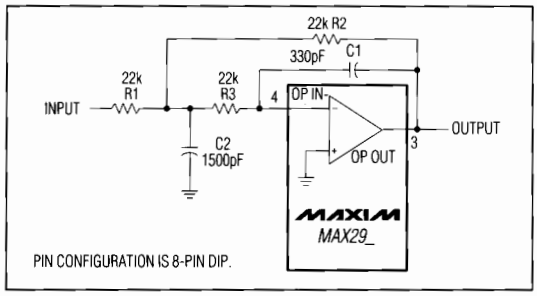


Figure 4. Uncommitted Op Amp Configured as a 2nd-Order Butterworth Lowpass Filter (F_o = 10kHz)

same mismatch in a ladder filter design will spread its error over all poles.

Clock-Signal Requirements

The MAX293/MAX294/MAX297 maximum recommended clock frequency is 2.5MHz, producing a cutoff frequency of 25kHz for the MAX293/MAX294 and 50kHz for the MAX297. The CLK pin can be driven by an external clock or by the internal oscillator with an external capacitor. For external clock applications, the clock circuitry has been designed to interface with +5V CMOS logic. Drive the CLK pin with a CMOS gate powered from 0V and +5V when using either a single supply or dual ±5V supplies. Varying the rate of an external clock will dynamically adjust the filter's corner frequency.

When using the internal oscillator, the capacitance (C_{OSC}) on the CLK pin determines the oscillator frequency:

$$f_{OSC(kHz)} = \frac{10^5}{3C_{OSC(pF)}}$$

The stray capacitance at CLK should be minimized, since it will affect the internal oscillator frequency.

Applications Information

Power Supplies

The MAX293/MAX294/MAX297 operate from either dual or single power supplies. The dual-supply voltage range is ±2.375V to ±5.5V (0.1µF bypass capacitors from each supply to GND are recommended). When using a single supply, tie the V- pin to ground and bias the GND pin to the mid-supply point using a resistor-divider network, as shown in Figure 3.

Input-Signal Amplitude Range

The ideal input-signal range is determined by observing at what voltage level the signal-to-noise plus distortion (SINAD) ratio is maximized for a given corner frequency. The *Typical Operating Characteristics* show the MAX293/MAX294/MAX297 THD + Noise response as the input signal's peak-to-peak amplitude is varied.

Uncommitted Op Amp

The uncommitted op amp has its noninverting input connected to the GND pin, and can be used to build a 1st- or 2nd-order continuous-time lowpass filter. This filter is intended for anti-aliasing applications preceding the switched-capacitor filter, but it can be used as a post-filter to reduce clock noise. Figure 4 shows one of many filters that can be built with this op amp: a 2nd-order Butterworth filter with a 10kHz corner frequency and an input impedance greater than 22kΩ. Table 1 gives alternative component values for different corner frequencies of the same Butterworth filter.

Table 1. Component Values for Figure 4's Filter

Corner Freq. (Hz)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	C1 (F)	C2 (F)
100k	10	10	10	68p	330p
50k	20	20	20	68p	330p
25k	20	20	20	150p	680p
10k	22	22	22	330p	1.5n
1k	22	22	22	3.3p	15n
100	22	22	22	33n	150n
10	22	22	22	330n	1.5µ

NOTE: Some approximations have been made in selecting preferred component values.

The passband error caused by a 2nd-order Butterworth can be calculated using the formula:

$$\text{Gain error} = -10\log\left[1 + \left(\frac{f}{f_c}\right)^4\right] \text{ dB}$$

8th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

As the passband ripple of the MAX293/MAX294/MAX297 elliptic filters is of the order of ±0.1dB, it is normally appropriate to keep the passband errors of any anti-aliasing filter at or below this level. This is achieved by choosing the corner frequency of Figure 4's Butterworth filter (f_{cB}) to be higher than the corner frequency of the elliptic switched-capacitor filter (f_{cE}) by a factor of 2.5 or more. A factor of 5 or more is recommended to avoid problems with component tolerances, i.e. $f_{cB} > (5)(f_{cE})$.

When using the uncommitted op amp as a post-filter to reduce clock noise, keep the filter's input impedance above 20kΩ to avoid excessive loading of the switched-capacitor filter. Note that the op amp experiences some clock feedthrough, so it is generally more useful for anti-aliasing than for clock-noise attenuation.

DAC Post-Filtering

When using the MAX293/MAX294/MAX297 for DAC post-filtering, synchronize the DAC and the filter clocks. If clocks are not synchronized, beat frequencies will alias into the desired passband. The DAC's clock should be generated by dividing down the switched-capacitor filter's clock.

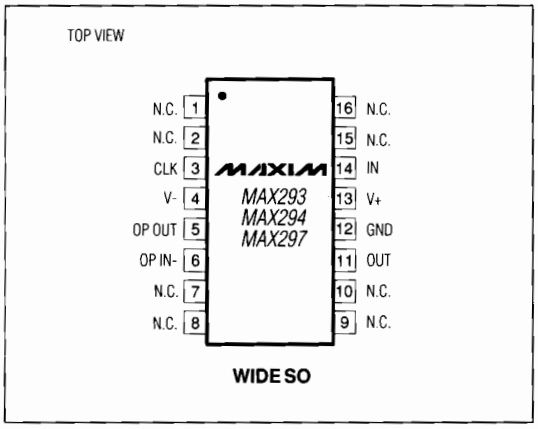
Harmonic Distortion

Harmonic distortion arises from nonlinearities within the filter. These nonlinearities generate harmonics when a pure sine wave is applied to the filter input. Table 2 lists typical harmonic distortion values for the MAX293/MAX294/MAX297 with a 1kHz 5Vp-p sine wave input signal, a 1MHz clock frequency, and a 20kΩ load.

Table 2. Typical Harmonic Distortion (dB)

FILTER	HARMONIC			
	2nd	3rd	4th	5th
MAX293	70	90	88	92
MAX294	67	90	92	94
MAX297	84	89	93	99

Pin Configurations (continued)



Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX294EPA	-40°C to +85°C	8 Plastic DIP
MAX294EWE	-40°C to +85°C	16 Wide SO
MAX294MJA	-55°C to +125°C	8 CERDIP**
MAX297CPA	0°C to +70°C	8 Plastic DIP
MAX297CWE	0°C to +70°C	16 Wide SO
MAX297C/D	0°C to +70°C	Dice*
MAX297EPA	-40°C to +85°C	8 Plastic DIP
MAX297EWE	-40°C to +85°C	16 Wide SO
MAX297MJA	-55°C to +125°C	8 CERDIP**

** Contact factory for dice specifications.*
*** Contact factory for availability and processing to MIL-STD-883.*

Order this document by MC145170–2/D

MOTOROLA
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MC145170-2

PLL Frequency Synthesizer with Serial Interface

The new MC145170–2 is pin–for–pin compatible with the MC145170–1. A comparison of the two parts is shown in the table below. The MC145170–2 is recommended for new designs and has a more robust power–on reset (POR) circuit that is more responsive to momentary power supply interruptions. The two devices are actually the same chip with mask options for the POR circuit. The more robust POR circuit draws approximately 20 μA additional supply current. Note that the maximum specification of 100 μA quiescent supply current has not changed.

The MC145170–2 is a single–chip synthesizer capable of direct usage in the MF, HF, and VHF bands. A special architecture makes this PLL easy to program. Either a bit– or byte–oriented format may be used. Due to the patented BitGrabber™ registers, no address/steering bits are required for *random access* of the three registers. Thus, tuning can be accomplished via a 2–byte serial transfer to the 16–bit N register.

The device features fully programmable R and N counters, an amplifier at the f_{in} pin, on–chip support of an external crystal, a programmable reference output, and both single– and double–ended phase detectors with linear transfer functions (no dead zones). A configuration (C) register allows the part to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing noise and interference.

In order to reduce lock times and prevent erroneous data from being loaded into the counters, a patented jam–load feature is included. Whenever a new divide ratio is loaded into the N register, both the N and R counters are jam–loaded with their respective values and begin counting down together. The phase detectors are also initialized during the jam load.

- Operating Voltage Range: 2.7 to 5.5 V
- Maximum Operating Frequency:
  185 MHz @ V_{in} = 500 mVpp, 4.5 V Minimum Supply
  100 MHz @ V_{in} = 500 mVpp, 3.0 V Minimum Supply
- Operating Supply Current:
  0.6 mA @ 3.0 V, 30 MHz
  1.5 mA @ 3.0 V, 100 MHz
  3.0 mA @ 5.0 V, 50 MHz
  5.8 mA @ 5.0 V, 185 MHz
- Operating Temperature Range: –40 to 85°C
- R Counter Division Range: 1 and 5 to 32,767
- N Counter Division Range: 40 to 65,535
- Direct Interface to Motorola SPI Serial Data Port
- See Application Notes AN1207/D and AN1671/D
- See web site *mot–sps.com* for MC145170 control software. Select in order, Products, Wireless Semiconductor, Download, then PLL Demo Software. Choose PLLGEN.EXE.

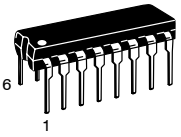
BitGrabber is a trademark of Motorola Inc.

COMPARISION OF THE PLL FREQUENCY SYNTHESIZERS

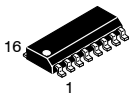
Parameter	MC145170–2	MC145170–1
Minimum Supply Voltage	2.7 V	2.5 V
Maximum Input Current, f_{in}	150 μA	120 μA
Dynamic Characteristics, f_{in} (Figure 23)	Unchanged	–
Power–On Reset Circuit	Improved	–

CMOS PLL FREQUENCY SYNTHESIZER WITH SERIAL INTERFACE

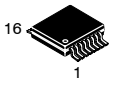
SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 648

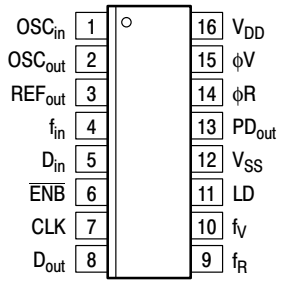


D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SOG–16)



DT SUFFIX
PLASTIC PACKAGE
CASE 948C
(TSSOP–16)

PIN CONNECTIONS

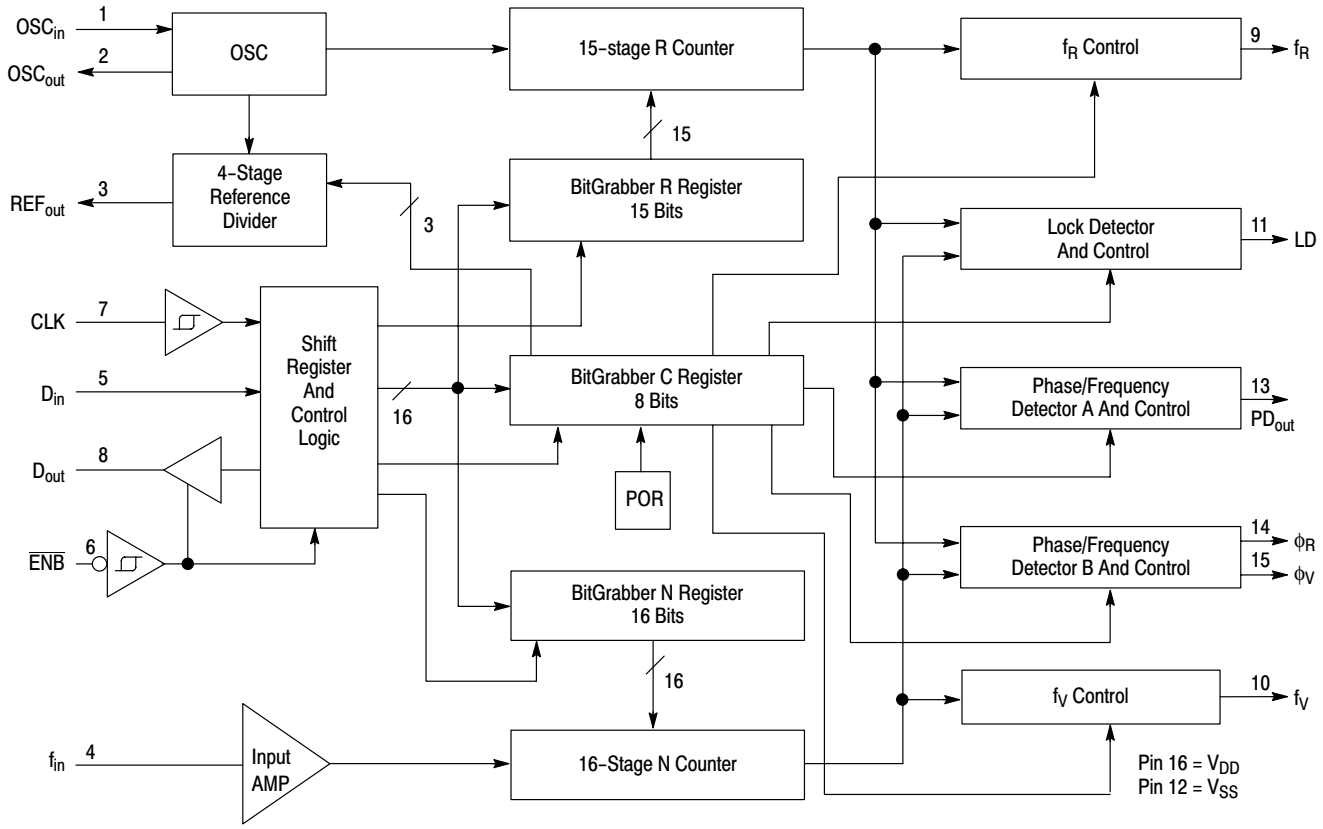


(Top View)

ORDERING INFORMATION

Device	Operating Temp Range	Package
MC145170P2	T_A = –40 to 85°C	Plastic DIP
MC145170D2		SOG–16
MC145170DT2		TSSOP–16

BLOCK DIAGRAM



This device contains 4,800 active transistors.

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 5.5	V
DC Input Voltage	V_{in}	–0.5 to V_{DD} + 0.5	V
DC Output Voltage	V_{out}	–0.5 to V_{DD} + 0.5	V
DC Input Current, per Pin	I_{in}	±10	mA
DC Output Current, per Pin	I_{out}	±20	mA
DC Supply Current, V_{DD} and V_{SS} Pins	I_{DD}	±30	mA
Power Dissipation, per Package	P_D	300	mW
Storage Temperature	T_{stg}	–65 to 150	°C
Lead Temperature, 1 mm from Case for 10 seconds	T_L	260	°C

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.
2. ESD data available upon request.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A = –40 to 85°C)

Parameter	Test Condition	Symbol	V_{DD} V	Guaranteed Limit	Unit
Power Supply Voltage Range		V_{DD}	–	2.7 to 5.5	V
Maximum Low–Level Input Voltage [Note 1] (D_{in}, CLK, $\overline{ENB}$, f_{in})	dc Coupling to f_{in}	V_{IL}	2.7 4.5 5.5	0.54 1.35 1.65	V
Minimum High–Level Input Voltage [Note 1] (D_{in}, CLK, $\overline{ENB}$, f_{in})	dc Coupling to f_{in}	V_{IH}	2.7 4.5 5.5	2.16 3.15 3.85	V
Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)		V_{Hys}	2.7 5.5	0.15 0.20	V
Maximum Low–Level Output Voltage (Any Output)	I_{out} = 20 μA	V_{OL}	2.7 5.5	0.1 0.1	V
Minimum High–Level Output Voltage (Any Output)	I_{out} = – 20 μA	V_{OH}	2.7 5.5	2.6 5.4	V
Minimum Low–Level Output Current (PD_{out}, REF_{out}, f_R, f_V, LD, ϕ_R, ϕ_V)	V_{out} = 0.3 V V_{out} = 0.4 V V_{out} = 0.5 V	I_{OL}	2.7 4.5 5.5	0.12 0.36 0.36	mA
Minimum High–Level Output Current (PD_{out}, REF_{out}, f_R, f_V, LD, ϕ_R, ϕ_V)	V_{out} = 2.4 V V_{out} = 4.1 V V_{out} = 5.0 V	I_{OH}	2.7 4.5 5.5	–0.12 –0.36 –0.36	mA
Minimum Low–Level Output Current (D_{out})	V_{out} = 0.4 V	I_{OL}	4.5	1.6	mA
Minimum High–Level Output Current (D_{out})	V_{out} = 4.1 V	I_{OH}	4.5	–1.6	mA
Maximum Input Leakage Current (D_{in}, CLK, $\overline{ENB}$, OSC_{in})	V_{in} = V_{DD} or V_{SS}	I_{in}	5.5	±1.0	μA
Maximum Input Current (f_{in})	V_{in} = V_{DD} or V_{SS}	I_{in}	5.5	±150	μA
Maximum Output Leakage Current (PD_{out})	V_{in} = V_{DD} or V_{SS}, Output in High–Impedance State	I_{OZ}	5.5	±100	nA
(D_{out})			5.5	±5.0	μA
Maximum Quiescent Supply Current	V_{in} = V_{DD} or V_{SS}; Outputs Open; Excluding f_{in} Amp Input Current Component	I_{DD}	5.5	100	μA
Maximum Operating Supply Current	f_{in} = 500 mVpp; OSC_{in} = 1.0 MHz @ 1.0 Vpp; LD, f_R, f_V, REF_{out} = Inactive and No Connect; OSC_{out}, ϕ_V, ϕ_R, PD_{out} = No Connect; D_{in}, ENB, CLK = V_{DD} or V_{SS}	I_{dd}	–	[Note 2]	mA

NOTES: 1. When dc coupling to the OSC_{in} pin is used, the pin must be driven rail–to–rail. In this case, OSC_{out} should be floated.
2. The nominal values at 3.0 V are 0.6 mA @ 30 MHz, and 1.5 mA @ 100 MHz. The nominal values at 5.0 V are 3.0 mA @ 50 MHz, and 5.8 mA @ 185 MHz. These are not guaranteed limits.

AC INTERFACE CHARACTERISTICS (T_A = –40 to 85°C, C_L = 50 pF, Input $t_r = t_f$ = 10 ns, unless otherwise noted.)

Parameter	Symbol	Figure No.	V_{DD} V	Guaranteed Limit	Unit
Serial Data Clock Frequency (Note: Refer to Clock t_w Below)	f_{clk}	1	2.7 4.5 5.5	dc to 3.0 dc to 4.0 dc to 4.0	MHz
Maximum Propagation Delay, CLK to D_{out}	t_{PLH}, t_{PHL}	1, 5	2.7 4.5 5.5	150 85 85	ns
Maximum Disable Time, D_{out} Active to High Impedance	t_{PLZ}, t_{PHZ}	2, 6	2.7 4.5 5.5	300 200 200	ns
Access Time, D_{out} High Impedance to Active	t_{PZL}, t_{PZH}	2, 6	2.7 4.5 5.5	0 to 200 0 to 100 0 to 100	ns
Maximum Output Transition Time, D_{out} CL = 50 pF	t_{TLH}, t_{THL}	1, 5	2.7 4.5 5.5	150 50 50	ns
CL = 200 pF		1, 5	2.7 4.5 5.5	900 150 150	ns
Maximum Input Capacitance – D_{in}, $\overline{ENB}$, CLK	C_{in}		–	10	pF
Maximum Output Capacitance – D_{out}	C_{out}		–	10	pF

TIMING REQUIREMENTS (T_A = –40 to 85°C, Input $t_r = t_f$ = 10 ns, unless otherwise noted.)

Parameter	Symbol	Figure No.	V_{DD} V	Guaranteed Limit	Unit
Minimum Setup and Hold Times, D_{in} vs CLK	t_{su}, t_h	3	2.7 4.5 5.5	55 40 40	ns
Minimum Setup, Hold, and Recovery Times, $\overline{ENB}$ vs CLK	t_{su}, t_h, t_{rec}	4	2.7 4.5 5.5	135 100 100	ns
Minimum Inactive–High Pulse Width, $\overline{ENB}$	$t_{w(H)}$	4	2.7 4.5 5.5	400 300 300	ns
Minimum Pulse Width, CLK	t_w	1	2.7 4.5 5.5	166 125 125	ns
Maximum Input Rise and Fall Times, CLK	t_r, t_f	1	2.7 4.5 5.5	100 100 100	µs

SWITCHING WAVEFORMS

Figure 1.

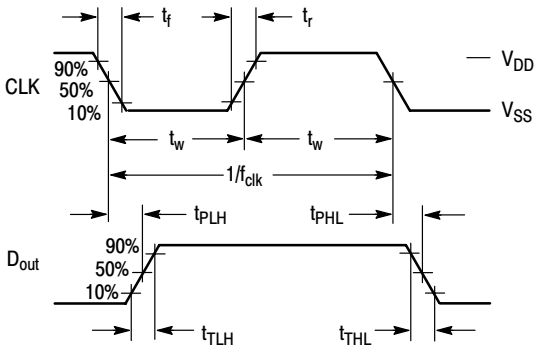


Figure 2.

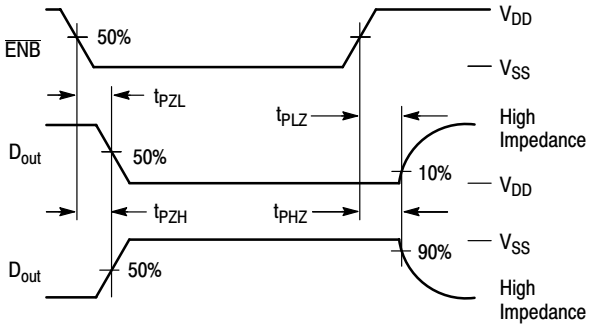


Figure 3.

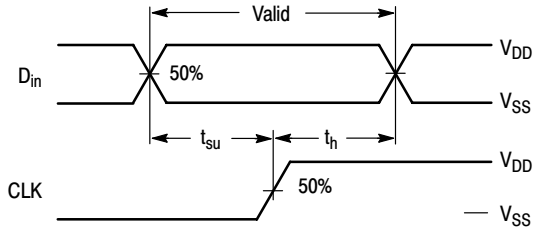


Figure 4.

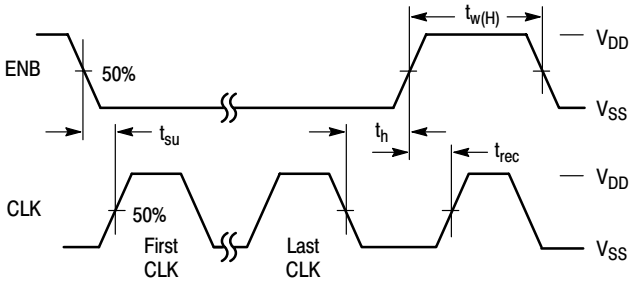
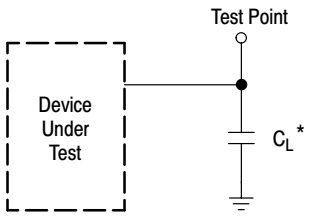
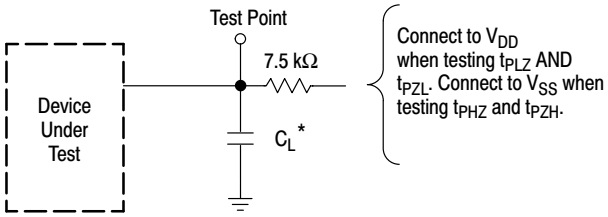


Figure 5. Test Circuit



* Includes all probe and fixture capacitance.

Figure 6. Test Circuit



* Includes all probe and fixture capacitance.

LOOP SPECIFICATIONS (T_A = –40 to 85°C)

Parameter	Test Condition	Symbol	Figure No.	V_{DD} V	Guaranteed Range Min	Guaranteed Range Max	Unit
Input Frequency, f_{in} [Note}	V_{in} ≥ 500 mVpp Sine Wave, N Counter Set to Divide Ratio Such that f_V ≤ 2.0 MHz	f	7	2.7 3.0 4.5 5.5	5.0 5.0 25 45	80 100 185 185	MHz
Input Frequency, OSC_{in} Externally Driven with ac–coupled Signal	V_{in} ≥ 1.0 V_{pp} Sine Wave, OSC_{out} = No Connect, R Counter Set to Divide Ratio Such that f_R ≤ 2 MHz	f	8a	2.7 3.0 4.5 5.5	1.0* 1.0* 1.0* 1.0*	22 25 30 35	MHz
Crystal Frequency, OSC_{in} and OSC_{out}	C1 ≤ 30 pF C2 ≤ 30 pF Includes Stray Capacitance	f_{XTAL}	9	2.7 3.0 4.5 5.5	2.0 2.0 2.0 2.0	12 12 15 15	MHz
Output Frequency, REF_{out}	C_L = 30 pF	f_{out}	10, 12	2.7 4.5 5.5	dc dc dc	– 10 10	MHz
Operating Frequency of the Phase Detectors		f		2.7 4.5 5.5	dc dc dc	– 2.0 2.0	MHz
Output Pulse Width, ϕ_R, ϕ_V, and LD	f_R in Phase with f_V C_L = 50 pF	t_w	11, 12	2.7 4.5 5.5	– 20 16	– 100 90	ns
Output Transition Times, ϕ_R, ϕ_V, LD, f_R, and f_V	C_L = 50 pF	t_{TLH}, t_{THL}	11, 12	2.7 4.5 5.5	– – –	– 65 60	ns
Input Capacitance f_{in} OSC_{in}		C_{in}	– –	– –	– –	7.0 7.0	pF

* IF lower frequency is desired, use wave shaping or higher amplitude sinusoidal signal in ac–coupled case. Also, see Figure 22 for dc coupling.

Figure 7. Test Circuit, f_{in}

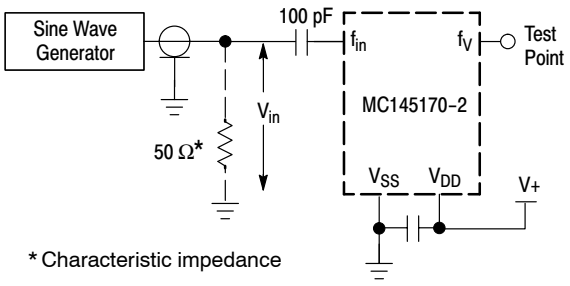


Figure 8.

Figure 8a. Test Circuit, OSC Circuit Externally Driven [Note]

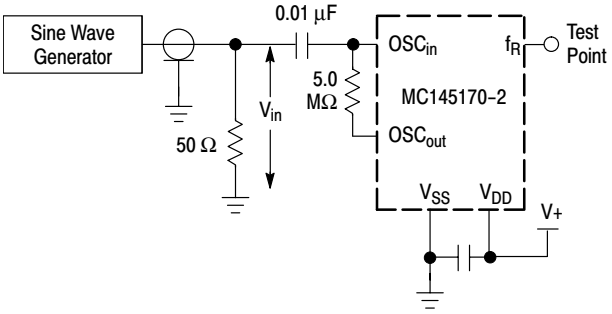


Figure 8b. Circuit to Eliminate Self–Oscillation, OSC Circuit Externally Driven [Note]

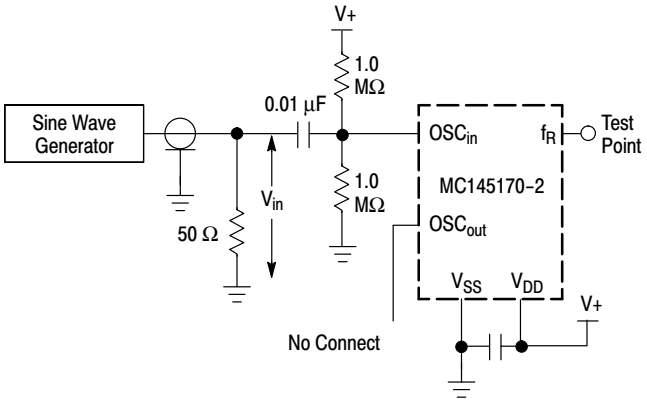


Figure 9. Test Circuit, OSC Circuit with Crystal

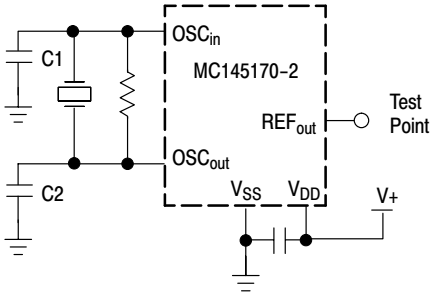


Figure 10. Switching Waveform

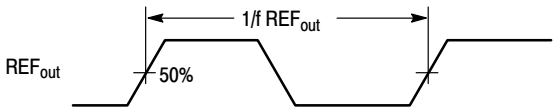


Figure 11. Switching Waveform

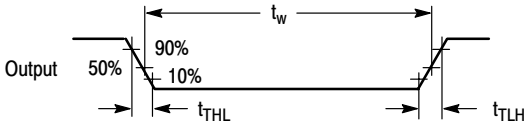
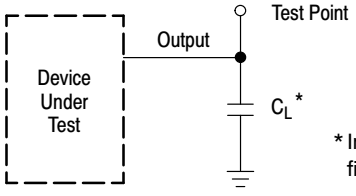


Figure 12. Test Load Circuit



NOTE: Use the circuit of Figure 8b to eliminate self–oscillation of the OSC_{in} pin when the MC145170–2 has power applied with no external signal applied at V_{in}. (Self–oscillation is not harmful to the MC145170–2 and does not damage the IC.)

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

D_{in}

Serial Data Input (Pin 5)

The bit stream begins with the most significant bit (MSB) and is shifted in on the low–to–high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the N register, or 3 bytes (24 bits) to access the R register. Additionally, the R register can be accessed with a 15–bit transfer (see Table 1). An optional pattern which resets the device is shown in Figure 13. The values in the C, N, and R registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{ENB}$.

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided (i.e., the registers may be accessed in any sequence). Data is retained in the registers over a supply range of 2.7 to 5.5 V. The formats are shown in Figures 13, 14, 15, and 16.

D_{in} typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull–up resistor of 1 to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst–case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1. Register Access

(MSBs are shifted in first, C0, N0, and R0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
9 to 13	See Figure 13	(Reset)
8	C Register	C7, C6, C5, . . ., C0
16	N Register	N15, N14, N13, . . ., N0
15 or 24	R Register	R14, R13, R12, . . ., R0
Other Values ≤ 32	None	
Values > 32	See Figures 24 — 31	

CLK

Serial Data Clock Input (Pin 7)

Low–to–high transitions on Clock shift bits available at D_{in}, while high–to–low transitions shift bits from D_{out}. The chip's 16–1/2–stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Four to eight clock cycles followed by five clock cycles are needed to reset the device; this is optional. Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the N register. Either 15 or 24 cycles can be used to access the R register (see Table 1 and Figures 13, 14, 15, and 16). For cascaded devices, see Figures 24 to 31.

CLK typically switches near 50% of V_{DD} and has a Schmitt–triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D_{in}** for more information.

NOTE

To guarantee proper operation of the power–on reset (POR) circuit, the CLK pin must be held at the potential of either the V_{SS} or V_{DD} pin during power up. That is, the CLK input should not be floated or toggled while the V_{DD} pin is ramping from 0 to at least 2.7 V. If control of the CLK pin is not practical during power up, the initialization sequence shown in Figure 13 must be used.

$\overline{ENB}$

Active–Low Enable Input (Pin 6)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{ENB}$ is in an inactive high state, shifting is inhibited, D_{out} is forced to the high–impedance state, and the port is held in the initialized state. To transfer data to the device, $\overline{ENB}$ (which must start inactive high) is taken low, a serial transfer is made via D_{in} and CLK, and $\overline{ENB}$ is taken back high. The low–to–high transition on $\overline{ENB}$ transfers data to the C, N, or R register depending on the data stream length per Table 1.

NOTE

Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{ENB}$ is high and CLK is low.

This input is also Schmitt–triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D_{in}** for more information.

D_{out}

Three–State Serial Data Output (Pin 8)

Data is transferred out of the 16–1/2–stage shift register through D_{out} on the high–to–low transition of CLK. This output is a No Connect, unless used in one of the manners discussed below.

D_{out} could be fed back to an MCU/MPU to perform a wrap–around test of serial data. This could be part of a system check conducted at power up to test the integrity of the system's processor, PC board traces, solder joints, etc.

The pin could be monitored at an in–line QA test during board manufacturing.

Finally, D_{out} facilitates troubleshooting a system and permits cascading devices.

REFERENCE PINS

OSC_{in}/OSC_{out}

Reference Oscillator Input/Output (Pins 1, 2)

These pins form a reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate values as recommended by the crystal supplier are connected from each pin to ground (up to a maximum of 30 pF each, including stray capacitance). An external feedback resistor of 1.0 to 5.0 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The required connections for the components are shown in Figure 9.

If desired, an external clock source can be ac coupled to OSC_{in}. A 0.01 μF coupling capacitor is used for measurement purposes and is the minimum size

recommended for applications. An external feedback resistor of approximately 5 MΩ is required across the OSC_{in} and OSC_{out} pins in the ac–coupled case (see Figure 8a or alternate circuit 8b). *OSC_{out} is an internal node on the device and should not be used to drive any loads* (i.e., OSC_{out} is unbuffered). However, the buffered REF_{out} is available to drive external loads.

The external signal level must be at least 1 V p–p; the maximum frequencies are given in the **Loop Specifications** table. These maximum frequencies apply for R Counter divide ratios as indicated in the table. For very small ratios, the maximum frequency is limited to the divide ratio times 2 MHz. (Reason: the phase/frequency detectors are limited to a maximum input frequency of 2 MHz.)

If an external source is available which swings virtually rail–to–rail (V_{DD} to V_{SS}), then dc coupling can be used. In the dc–coupled case, no external feedback resistor is needed. OSC_{out} must be a No Connect to avoid loading an internal node on the device, as noted above. *For frequencies below 1 MHz, dc coupling must be used.* The R counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the OSC_{in} pin. See Figure 22.

Each rising edge on the OSC_{in} pin causes the R counter to decrement by one.

REF_{out}
Reference Frequency Output (Pin 3)

This output is the buffered output of the crystal–generated reference frequency or externally provided reference source. This output may be enabled, disabled, or scaled via bits in the C register (see Figure 14).

REF_{out} can be used to drive a microprocessor clock input, thereby saving a crystal. Upon power up, the on–chip power–on–initialize circuit forces REF_{out} to the OSC_{in} divided–by–8 mode.

REF_{out} is capable of operation to 10 MHz; see the **Loop Specifications** table. Therefore, divide values for the reference divider are restricted to two or higher for OSC_{in} frequencies above 10 MHz.

If unused, the pin should be floated and should be disabled via the C register to minimize dynamic power consumption and electromagnetic interference (EMI).

COUNTER OUTPUT PINS

f_R
R Counter Output (Pin 9)

This signal is the buffered output of the 15–stage R counter. f_R can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f_R signal can be used to verify the R counter's divide ratio. This ratio extends from 5 to 32,767 and is determined by the binary value loaded into the R register. Also, direct access to the phase detector via the OSC_{in} pin is allowed by choosing a divide value of 1 (see Figure 15). The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f_R must not exceed 2 MHz.

When activated, the f_R signal appears as normally low and pulses high. The pulse width is 4.5 cycles of the OSC_{in} pin signal, except when a divide ratio of 1 is selected. When 1 is selected, the OSC_{in} signal is buffered and appears at the f_R pin.

f_V
N Counter Output (Pin 10)

This signal is the buffered output of the 16–stage N counter. f_V can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f_V signal can be used to verify the N counter's divide ratio. This ratio extends from 40 to 65,535 and is determined by the binary value loaded into the N register. The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f_V must not exceed 2 MHz.

When activated, the f_V signal appears as normally low and pulses high.

LOOP PINS

f_{in}
Frequency Input (Pin 4)

This pin is a frequency input from the VCO. This pin feeds the on–chip amplifier which drives the N counter. This signal is normally sourced from an external voltage–controlled oscillator (VCO), and is ac–coupled into f_{in}. A 100 pF coupling capacitor is used for measurement purposes and is the minimum size recommended for applications (see Figure 7). The frequency capability of this input is dependent on the supply voltage as listed in the **Loop Specifications** table. For small divide ratios, the maximum frequency is limited to the divide ratio times 2 MHz. (Reason: the phase/frequency detectors are limited to a maximum frequency of 2 MHz.)

For signals which swing from at least the V_{IL} to V_{IH} levels listed in the **Electrical Characteristics** table, dc coupling may be used. Also, for low frequency signals (less than the minimum frequencies shown in the **Loop Specifications** table), dc coupling is a requirement. The N counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the f_{in} pin. See Figure 22.

Each rising edge on the f_{in} pin causes the N counter to decrement by 1.

PD_{out}
Single–Ended Phase/Frequency Detector Output (Pin 13)

This is a three–state output for use as a loop error signal when combined with an external low–pass filter. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 14)

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: negative pulses from high impedance

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: positive pulses from high impedance

Frequency and Phase of $f_V = f_R$: essentially high–impedance state; voltage at pin determined by loop filter

POL bit (C7) = high

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: positive pulses from high impedance

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: negative pulses from high impedance

Frequency and Phase of $f_V = f_R$: essentially high–impedance state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to the high–impedance state by utilization of the disable feature in the C register (patented).

ϕ_R and ϕ_V
Double–Ended Phase/Frequency Detector Outputs (Pins 14, 15)

These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 14)

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C7) = high

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via the C register (patented).

LD
Lock Detector Output (Pin 11)

This output is essentially at a high level with narrow low–going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies (see Figure 17).

This output can be enabled and disabled via the C register (patented). Upon power up, on–chip initialization circuitry disables LD to a static low logic level to prevent a false "lock" signal. If unused, LD should be disabled and left open.

POWER SUPPLY

V_{DD}
Most Positive Supply Potential (Pin 16)

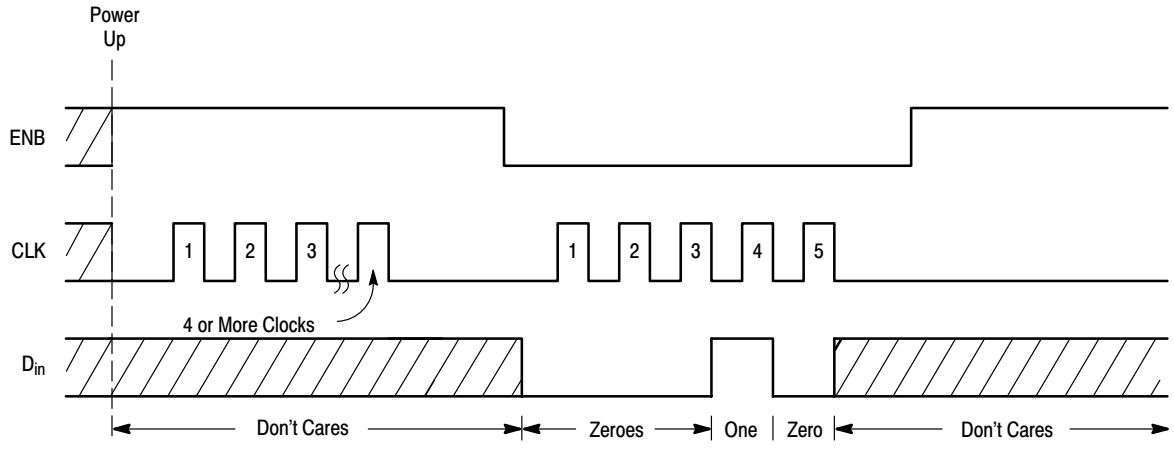
This pin may range from 2.7 to 5.5 V with respect to V_{SS}.

For optimum performance, V_{DD} should be bypassed to V_{SS} using low–inductance capacitor(s) mounted very close to the device. Lead lengths on the capacitor(s) should be minimized. (The very fast switching speed of the device causes current spikes on the power leads.)

V_{SS}
Most Negative Supply Potential (Pin 12)

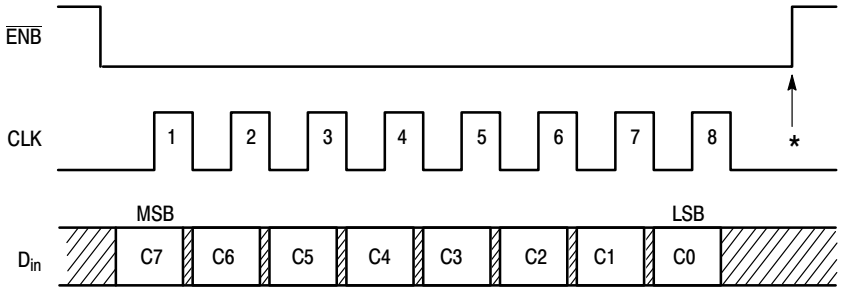
This pin is usually ground. For measurement purposes, the V_{SS} pin is tied to a ground plane.

Figure 13. Reset Sequence



NOTE: This initialization sequence is usually not necessary because the on–chip power–on reset circuit performs the initialization function. However, this initialization sequence must be used immediately after power up if control of the CLK pin is not possible. That is, if CLK (Pin 7) toggles or floats upon power up, use the above sequence to reset the device. Also, use this sequence if power is momentarily interrupted such that the supply voltage to the device is reduced to below 2.7 V, but not down to at least 1 V (for example, the supply drops down to 2 V). This is necessary because the on–chip power–on reset is only activated when the supply ramps up from a voltage below approximately 1.0 V.

Figure 14. C Register Access and Format (8 Clock Cycles are Used)



* At this point, the new byte is transferred to the C register and stored. No other registers are affected.

C7 — POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts PD_{out} and interchanges the ϕ_R function with ϕ_V as depicted in Figure 17. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6 — PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high–impedance state. This bit is cleared low at power up.

C5 — LDE: Enables the lock detector output when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

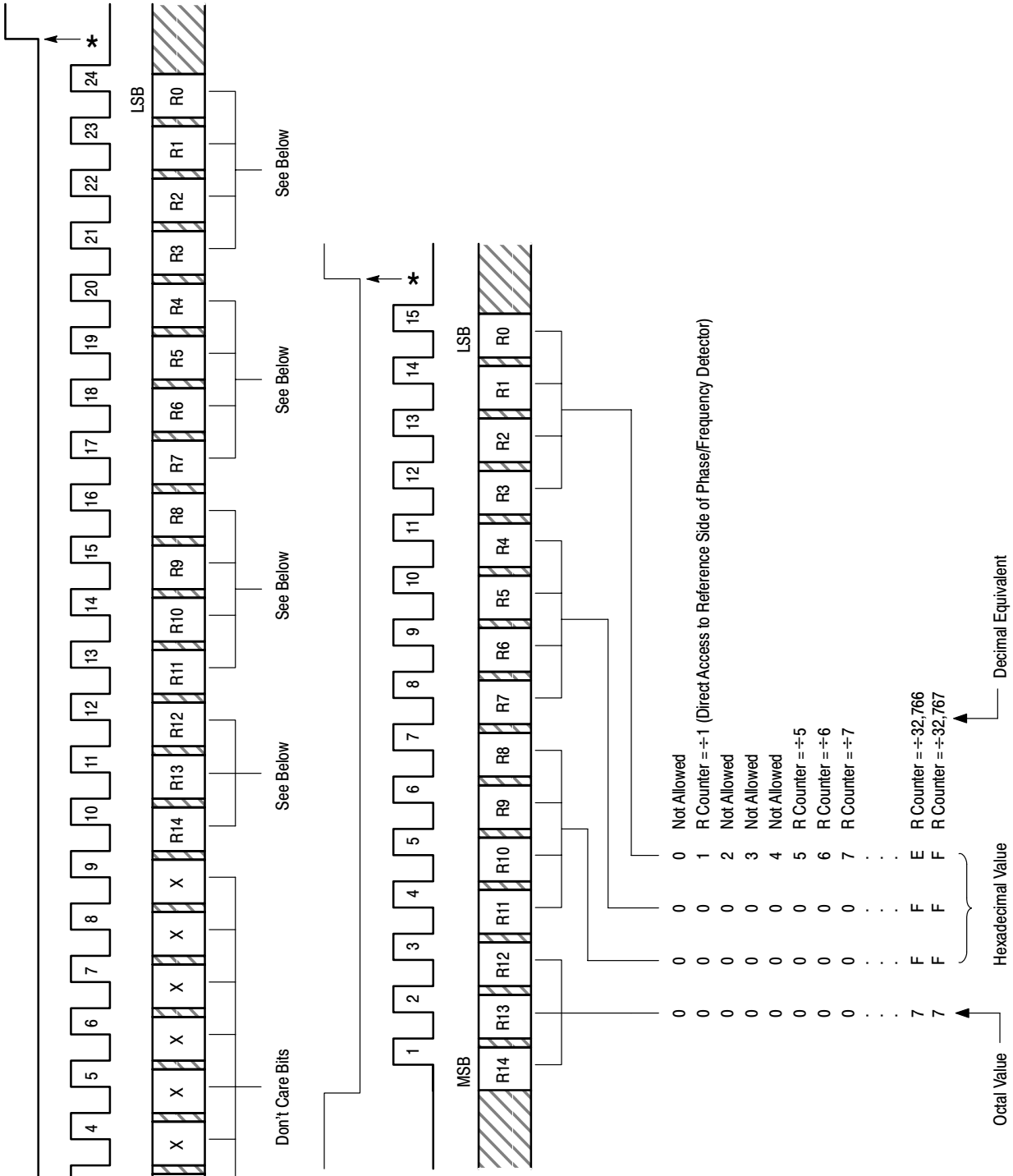
C4 – C2, OSC2 – OSC0: Reference output controls which determine the REF_{out} characteristics as shown below. Upon power up, the bits are initialized such that $OSC_{in}/8$ is selected.

C4	C3	C2	REF_{out} Frequency
0	0	0	dc (Static Low)
0	0	1	OSC_{in}
0	1	0	$OSC_{in}/2$
0	1	1	$OSC_{in}/4$
1	0	0	$OSC_{in}/8$ (POR Default)
1	0	1	$OSC_{in}/16$
1	1	0	$OSC_{in}/8$
1	1	1	$OSC_{in}/16$

C1 — f_VE: Enables the f_V output when set high. When cleared low, the f_V output is forced to a static low level. The bit is cleared low upon power up.

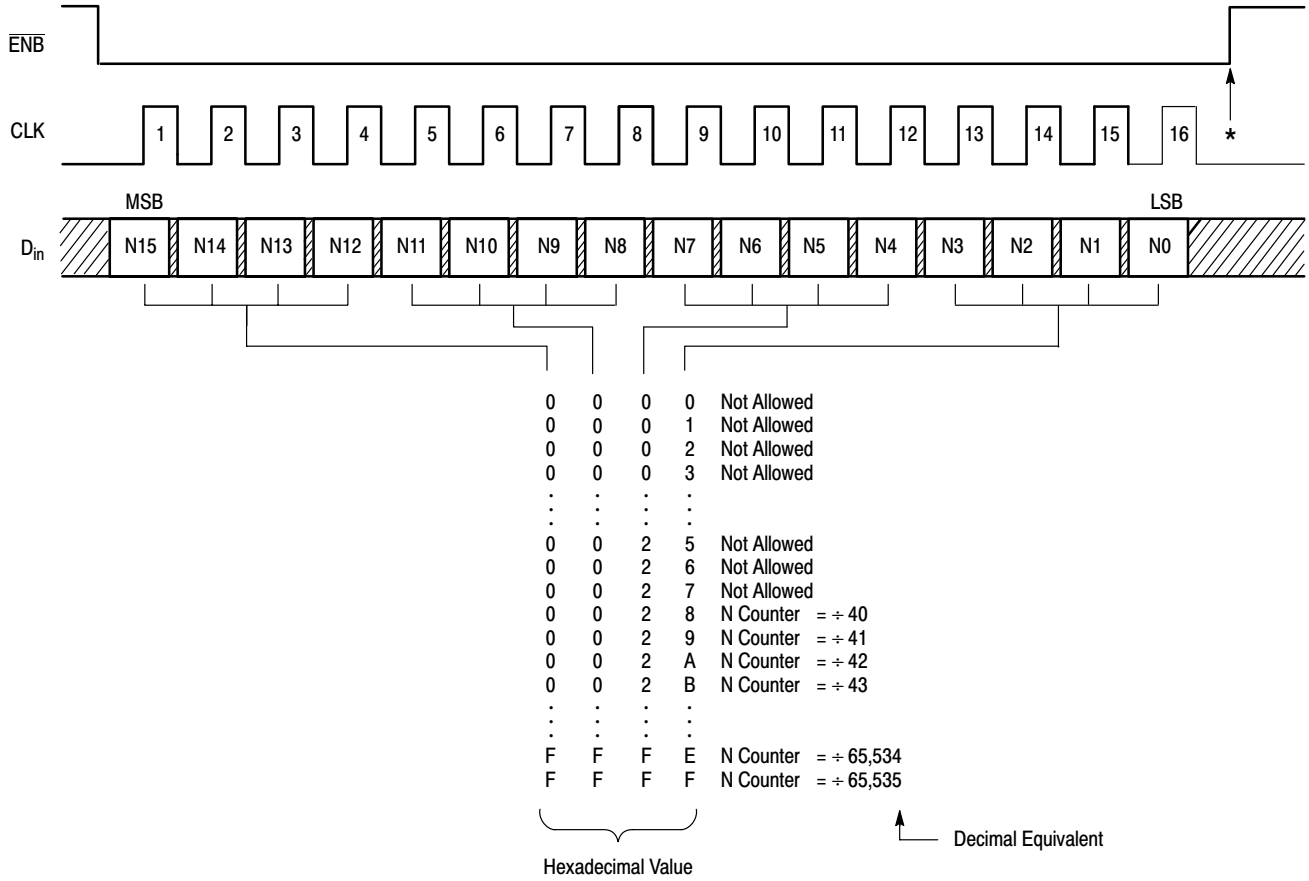
C0 — f_RE: Enables the f_R output when set high. When cleared low, the f_R output is forced to a static low level. The bit is cleared low upon power up.

Figure 15. R Register Access and Formats (Either 24 or 15 Clock Cycles Can Be Used)



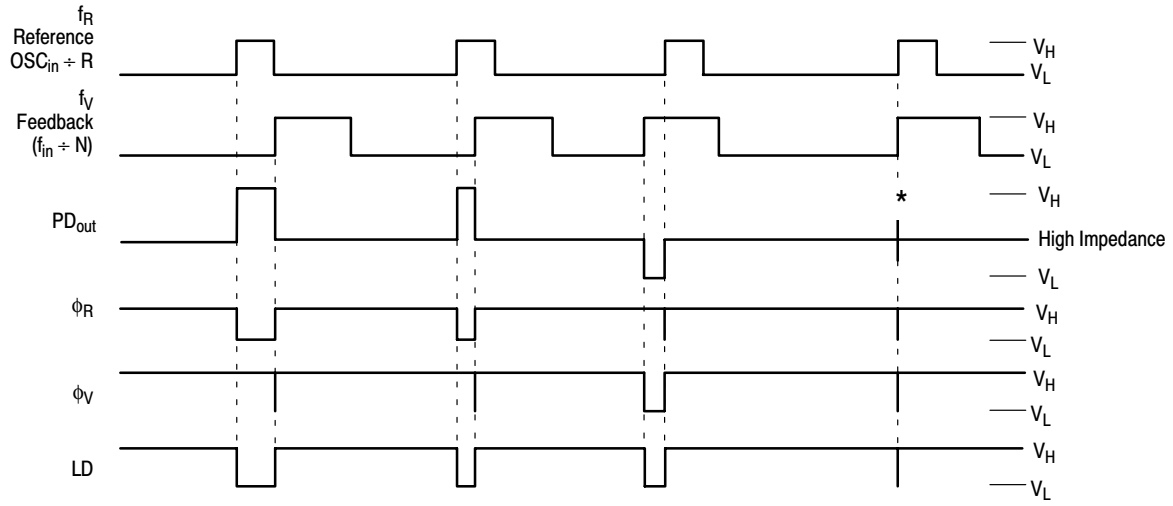
* At this point, the new data is transferred to the R register and stored. No other registers are affected.

Figure 16. N Register Access and Format (16 Clock Cycles Are Used)



* At this point, the two new bytes are transferred to the N register and stored. No other registers are affected. In addition, the N and R counters are jam–loaded and begin counting down together.

Figure 17. Phase/Frequency Detectors and Lock Detector Output Waveforms



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, both the sinking and sourcing output FETs are turned on for a very short interval.

NOTE: The PD_{out} generates error pulses during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor. PD_{out}, ϕ_R, and ϕ_V are shown with the polarity bit (POL) = low; see Figure 14 for POL.

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to OSC_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used (see Figures 8a and 8b).

For additional information about TCXOs, visit *motorola.com* on the world wide web.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 18.

The crystal should be specified for a loading capacitance (C_L) which does not exceed 20 pF when used at the highest operating frequencies listed in the **Loop Specifications** table. Larger C_L values are possible for lower frequencies. Assuming R1 = 0 Ω, the shunt load capacitance (C_L) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \times C2}{C1 + C2}$$

where

C_{in} = 5.0 pF (see Figure 19)
C_{out} = 6.0 pF (see Figure 19)
C_a = 1.0 pF (see Figure 19)
C1 and C2 = external capacitors (see Figure 18)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes 0 in the above expression for C_L.

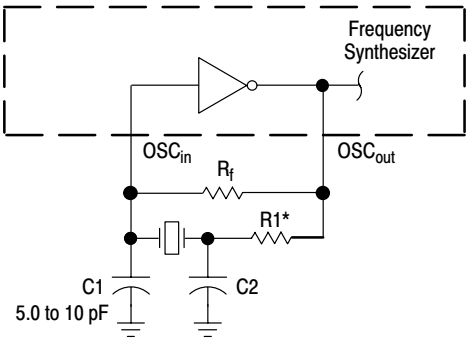
A good design practice is to pick a small value for C1, such as 5 to 10 pF. Next, C2 is calculated. C1 < C2 results in a more robust circuit for start–up and is more tolerant of crystal parameter variations.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 20. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 18 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency at the REF_{out} pin (OSC_{out} is not used because loading impacts the oscillator). The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 2).

Figure 18. Pierce Crystal Oscillator Circuit



* May be needed in certain cases. See text.

Figure 19. Parasitic Capacitances of the Amplifier and C_{stray}

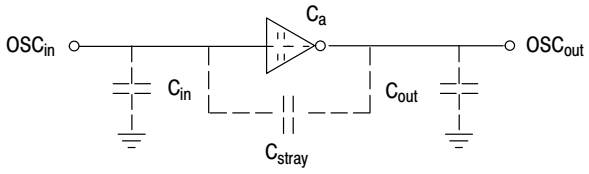
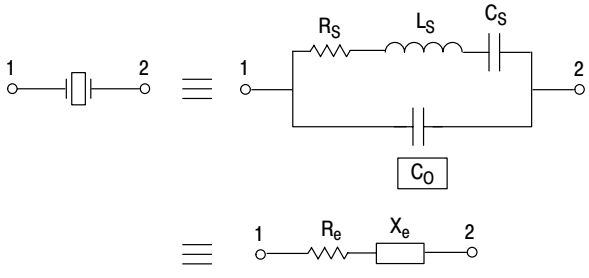


Figure 20. Equivalent Crystal Networks



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, “The Piezoelectric Crystal Unit–Definitions and Method of Measurement”, *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, “Quartz Crystals for Frequency Control”, *Electro–Technology*, June 1969.

P. J. Ottowitz, “A Guide to Crystal Selection”, *Electronic Design*, May 1966.

D. Babin, “Designing Crystal Oscillators”, *Machine Design*, March 7, 1985.

D. Babin, “Guidelines for Crystal Oscillator Design”, *Machine Design*, April 25, 1985.

See web site *mot–sps.com* for MC145170–2 control software. Select in order, Products, Wireless Semiconductor, Download, then PLL Demo Software. Choose PLLGEN.EXE.

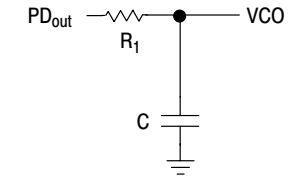
Table 2. Partial List of Crystal Manufacturers

CTS Corp.
United States Crystal Corp.
Crystek Crystal
Statek Corp.
Fox Electronics

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

PHASE–LOCKED LOOP — LOW PASS FILTER DESIGN

(A)

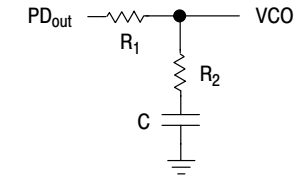


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC + 1}$$

(B)

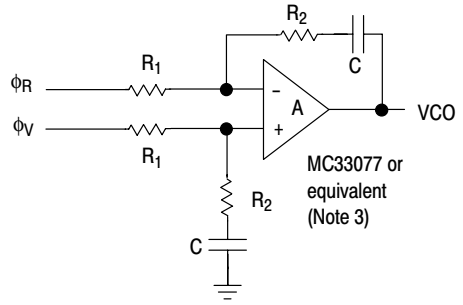


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\,\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}} \right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)sC + 1}$$

(C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

Assuming Gain A Is Very Large, Then:

$$F(s) = \frac{R_2sC + 1}{R_1sC}$$

NOTES:

1. For (C), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.
2. The ϕR and ϕV outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp.
3. For the latest information on MC33077 or equivalent, see the Motorola Analog IC web site at *http://www.mot–sps.com/analog*.

DEFINITIONS:

N = Total Division Ratio in Feedback Loop
K_ϕ (Phase Detector Gain) = $V_{DD}/ 4\pi$ volts per radian for PD_{out}
K_ϕ (Phase Detector Gain) = $V_{DD}/2\pi$ volts per radian for ϕ_V and ϕ_R

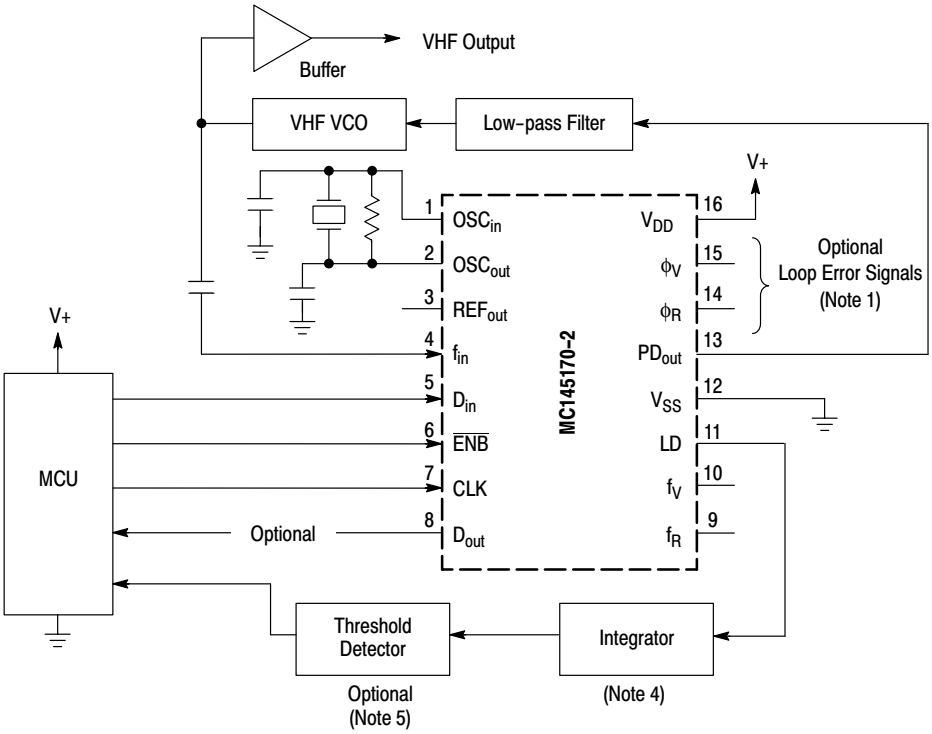
$$K_{VCO}\ (\text{VCO Gain}) = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R–related VCO sidebands.

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley–Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley–Interscience, 1980.
Blanchard, Alain, *Phase–Locked Loops: Application to Coherent Receiver Design.* New York, Wiley–Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley–Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice–Hall, 1983.
Berlin, Howard M., *Design of Phase–Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.
Seidman, Arthur H., *Integrated Circuits Applications Handbook*, Chapter 17, pp. 538–586. New York, John Wiley & Sons.
Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN*. March 5, 1980.
AN535, Phase–Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.
AR254, Phase–Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.
AN1207, The MC145170 in Basic HF and VHF Oscillators, Motorola Semiconductor Products, Inc., 1992.
AN1671, MC145170 PSpice Modeling Kit, Motorola Semiconductor Products, Inc., 1998.

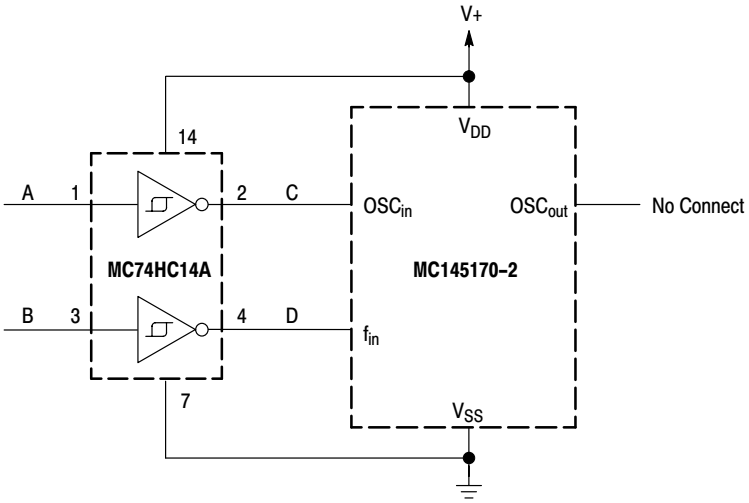
Figure 21. Example Application



NOTES:

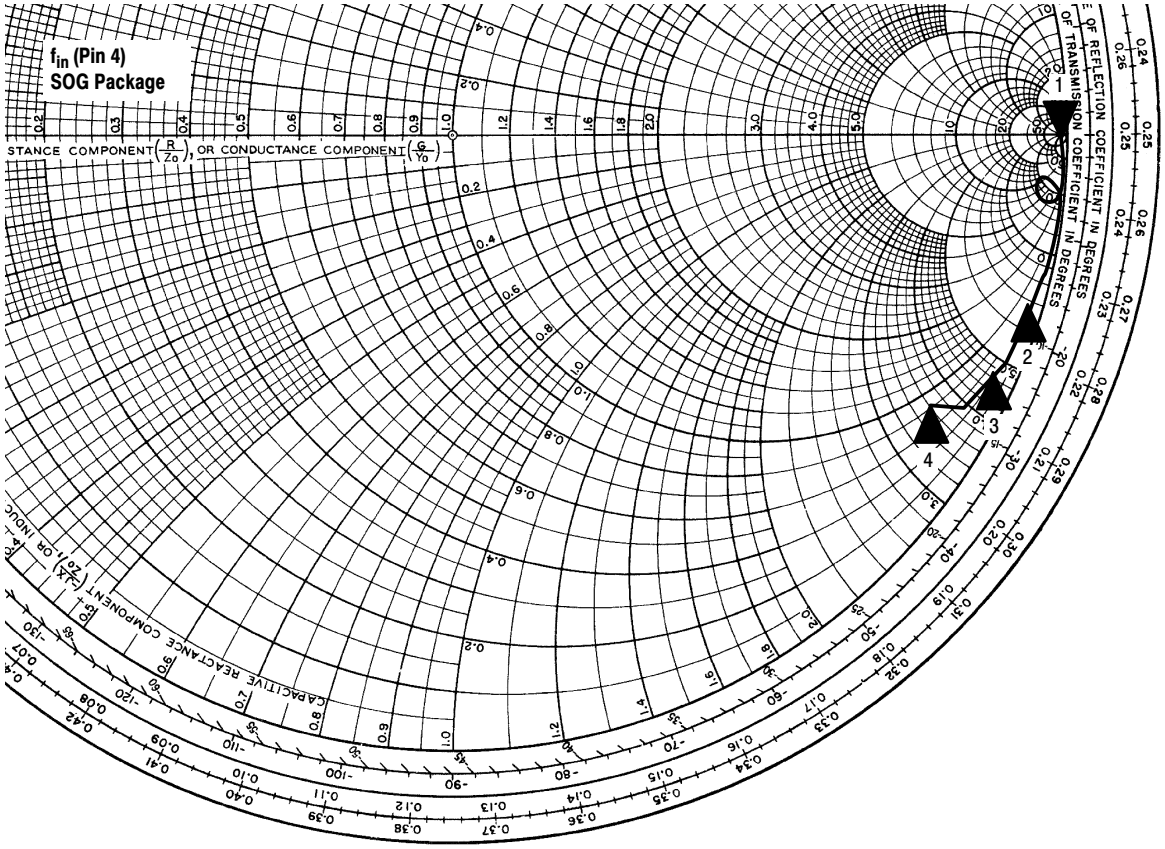
1. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.
2. For optimum performance, bypass the V_{DD} pin to V_{SS} (GND) with one or more low–inductance capacitors.
3. The R counter is programmed for a divide value = OSC_{in}/f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by f_R = N, where N is the divide value of the N counter.
4. May be an R–C low–pass filter.
5. May be a bipolar transistor.

Figure 22. Low Frequency Operation Using dc Coupling



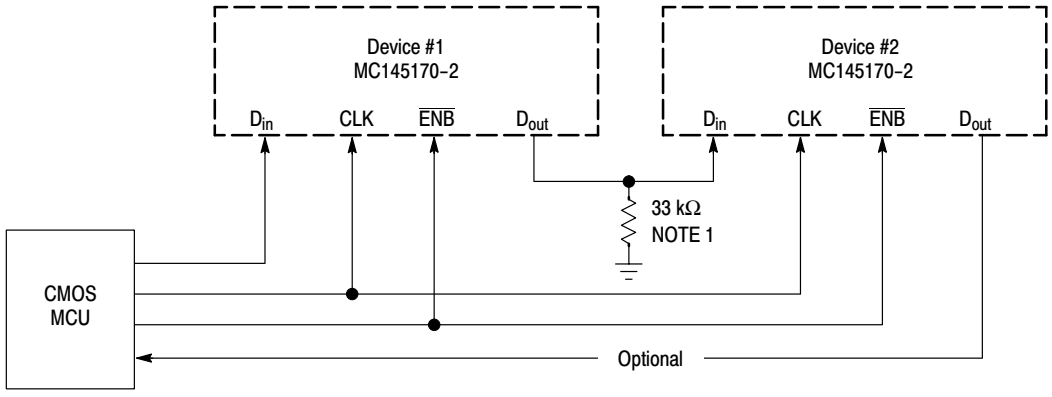
NOTE: The signals at Points A and B may be low–frequency sinusoidal or square waves with slow edge rates or noisy signal edges. At Points C and D, the signals are cleaned up, have sharp edge rates, and rail–to–rail signal swings. With signals as described at Points C and D, the MC145170–2 is guaranteed to operate down to a frequency as low as dc.
Refer to the MC74HC14A data sheet for input switching levels and hysteresis voltage range.

Figure 23. Input Impedance at f_{in} — Series Format (R + jX) (5.0 MHz to 185 MHz)



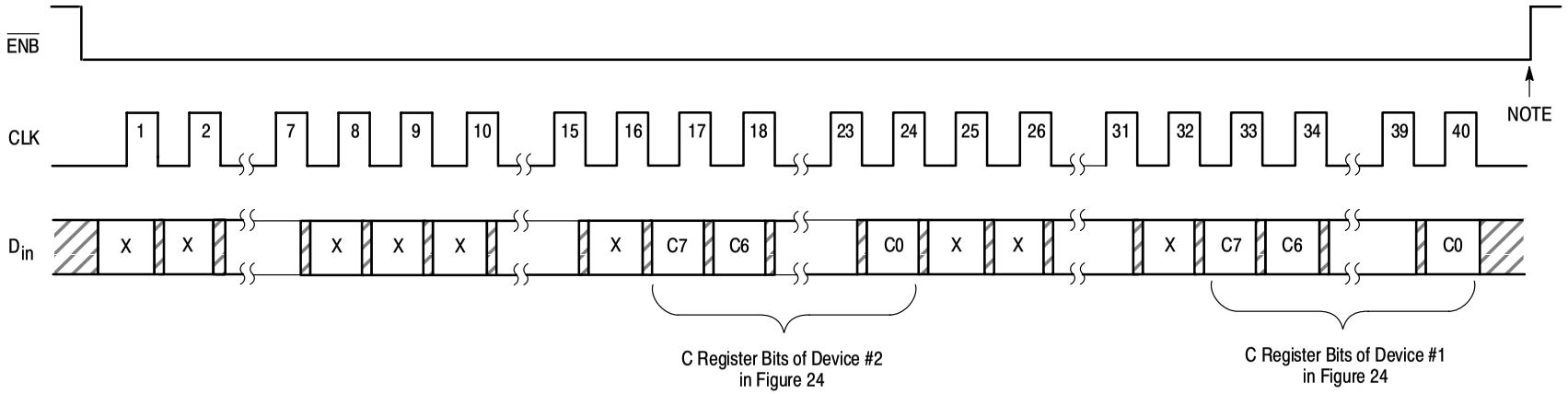
Marker	Frequency (MHz)	Resistance (Ω)	Reactance (Ω)	Capacitance (pF)
1	5	2390	– 5900	5.39
2	100	39.2	– 347	4.58
3	150	25.8	– 237	4.48
4	185	42.6	– 180	4.79

Figure 24. Cascading Two MC145170–2 Devices



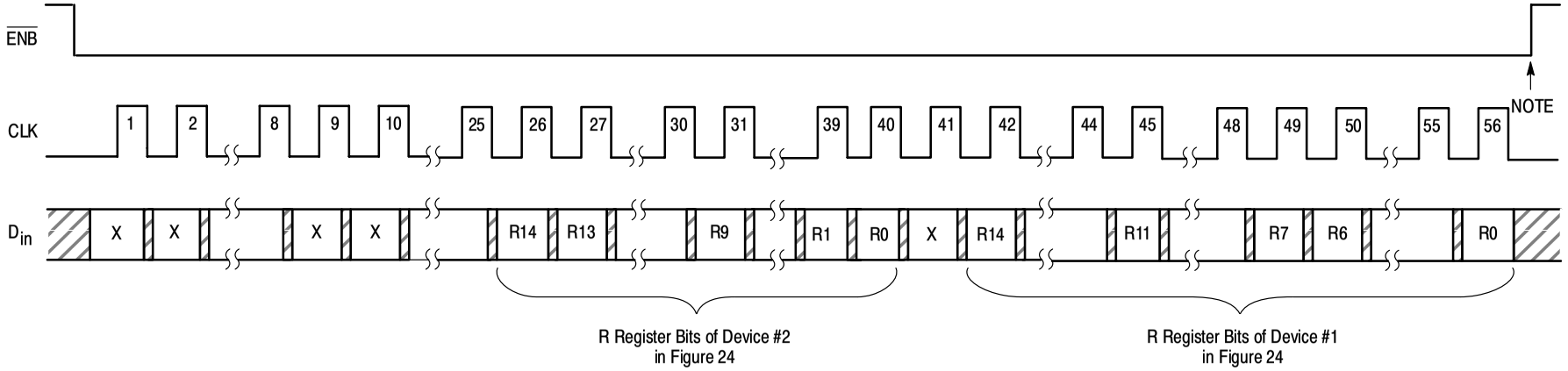
NOTES:
1. The 33 kΩ resistor is needed to prevent the D_{in} pin from floating. (The D_{out} pin is a three–state output.)
2. See related Figures 25, 26, and 27.

Figure 25. Accessing the C Registers of Two Cascaded MC145170–2 Devices



NOTE: At this point, the new data is transferred to the C registers of both devices and stored. No other registers are affected.

Figure 26. Accessing the R Registers of Two Cascaded MC145170–2 Devices



NOTE: At this point, the new data is transferred to the R registers of both devices and stored. No other registers are affected.

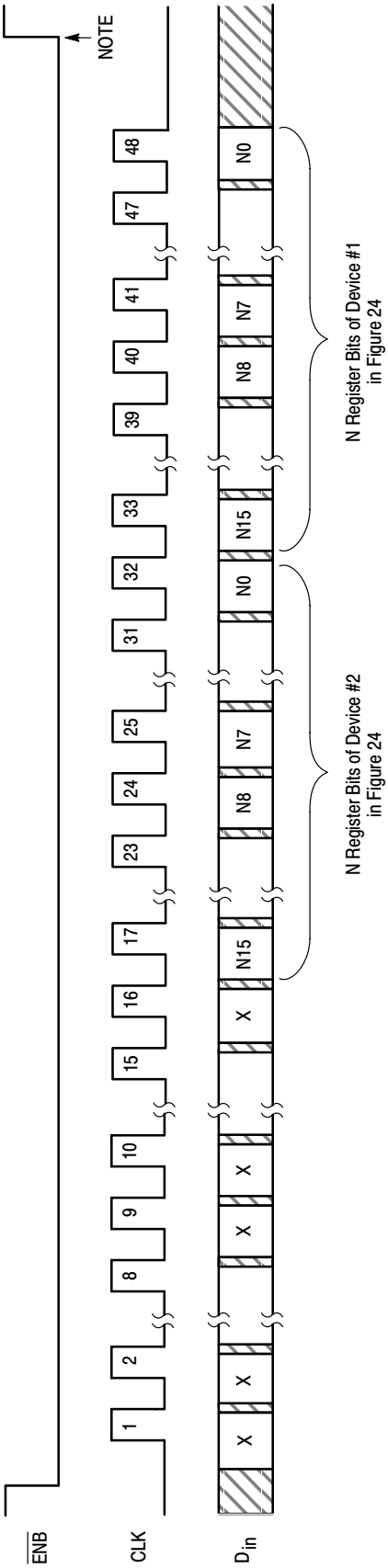
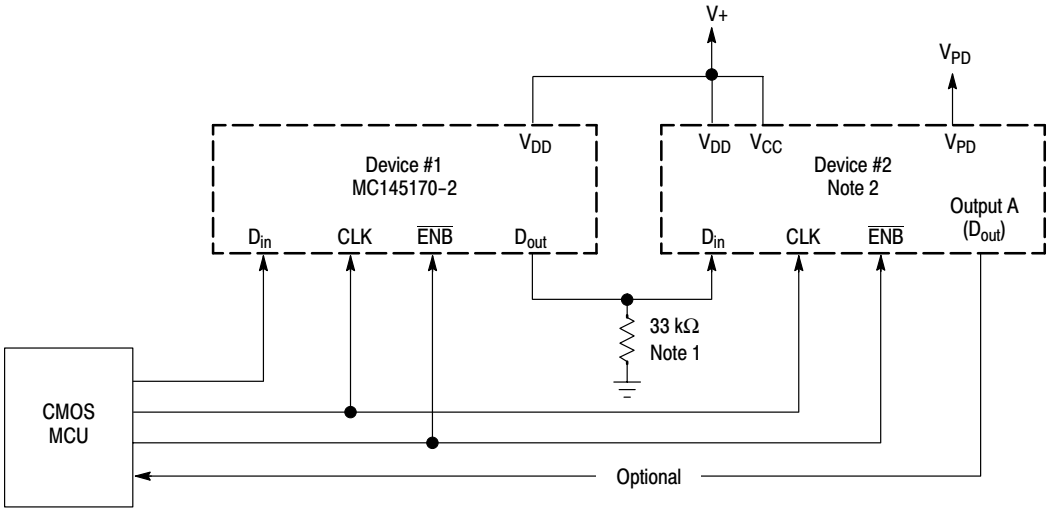


Figure 27. Accessing the N Registers of Two Cascaded MC145170–2 Devices

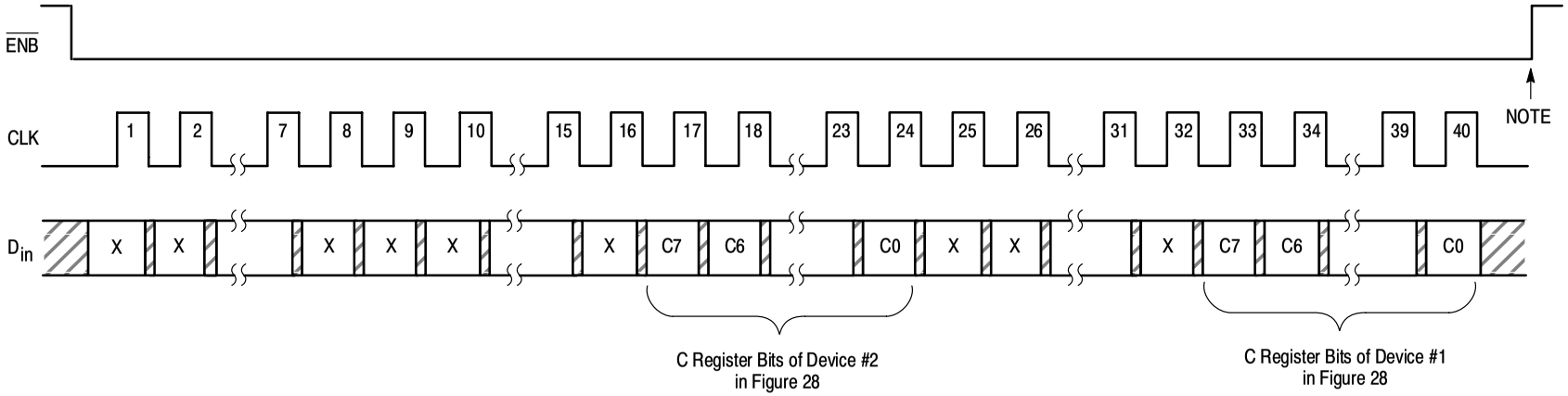
NOTE: At this point, the new data is transferred to the N registers of both devices and stored. No other registers are affected.

Figure 28. Cascading Two Different Device Types



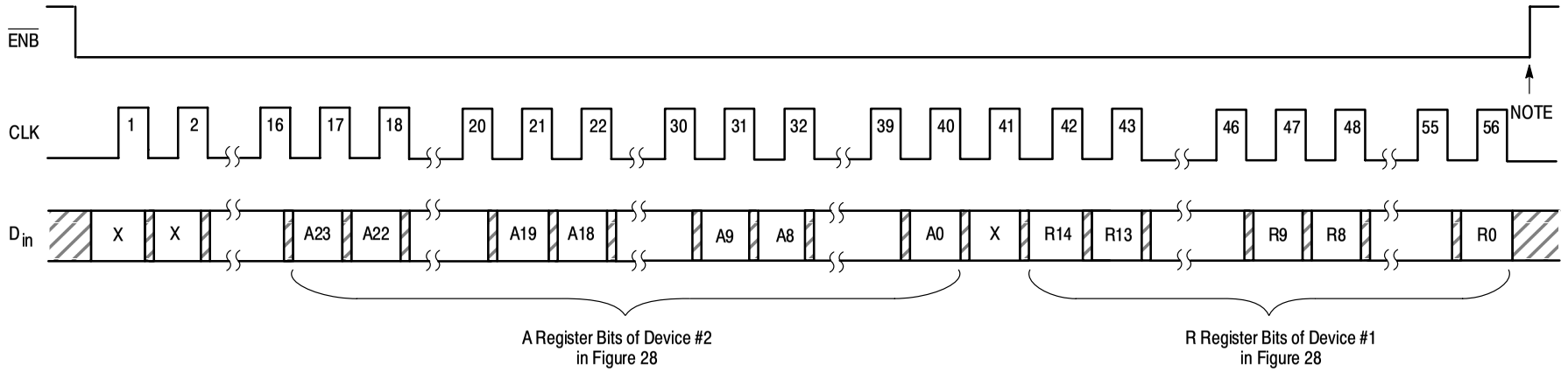
NOTES:
1. The 33 kΩ resistor is needed to prevent the D_{in} pin from floating. (The D_{out} pin is a three–state output.)
2. This PLL Frequency Synthesizer may be a MC145190, MC145191, MC145192, MC145200, or MC145201.
3. See related Figures 29, 30, and 31.

Figure 29. Accessing the C Registers of Two Different Device Types



NOTE: At this point, the new data is transferred to the C registers of both devices and stored. No other registers are affected.

Figure 30. Accessing the A and R Registers of Two Different Device Types



NOTE: At this point, the new data is transferred to the A register of Device #2 and R register of Device #1 and stored. No other registers are affected.

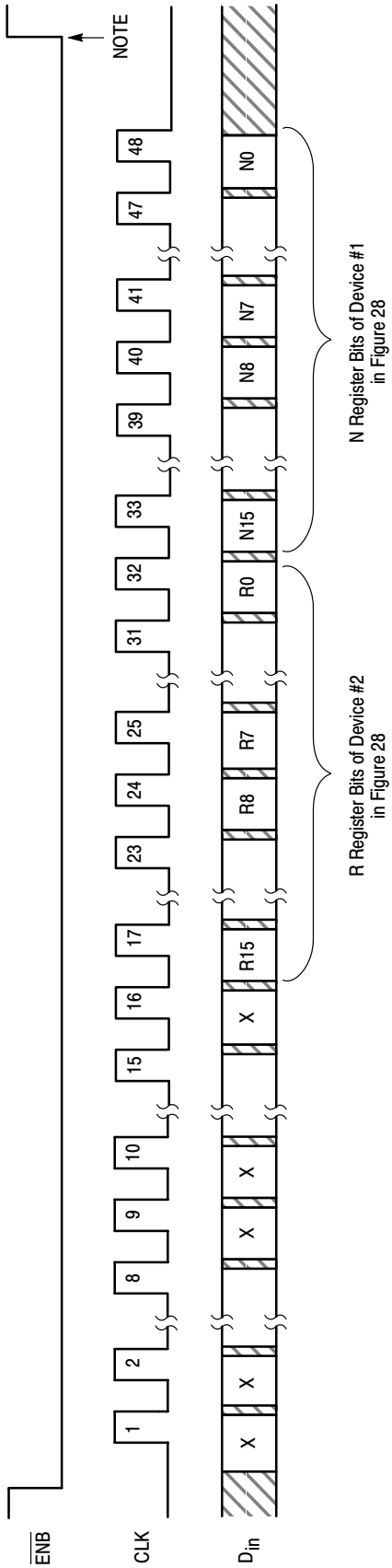
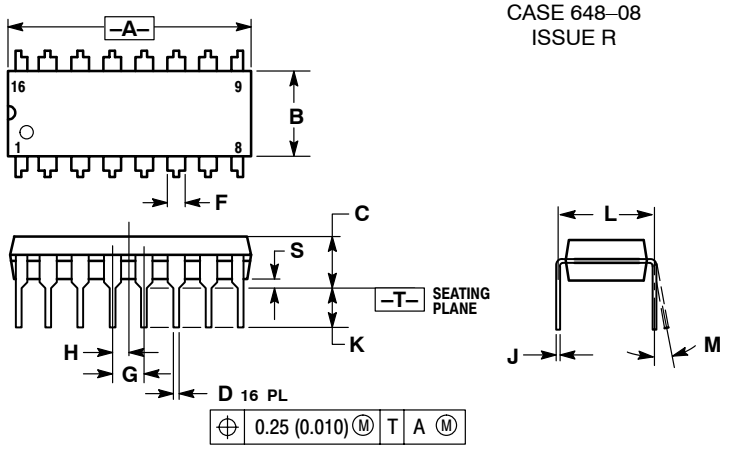


Figure 31. Accessing the R and N Registers of Two Different Device Types

NOTE: At this point, the new data is transferred to the R register of Device #2 and N register of Device #1 and stored. No other registers are affected.

OUTLINE DIMENSIONS

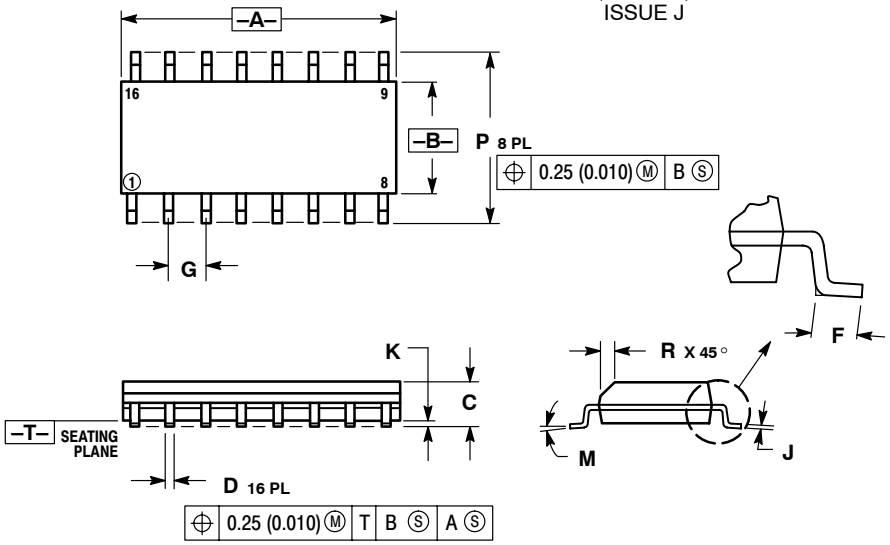
P SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

D SUFFIX
PLASTIC PACKAGE
CASE 751B–05
(SOG–16)
ISSUE J

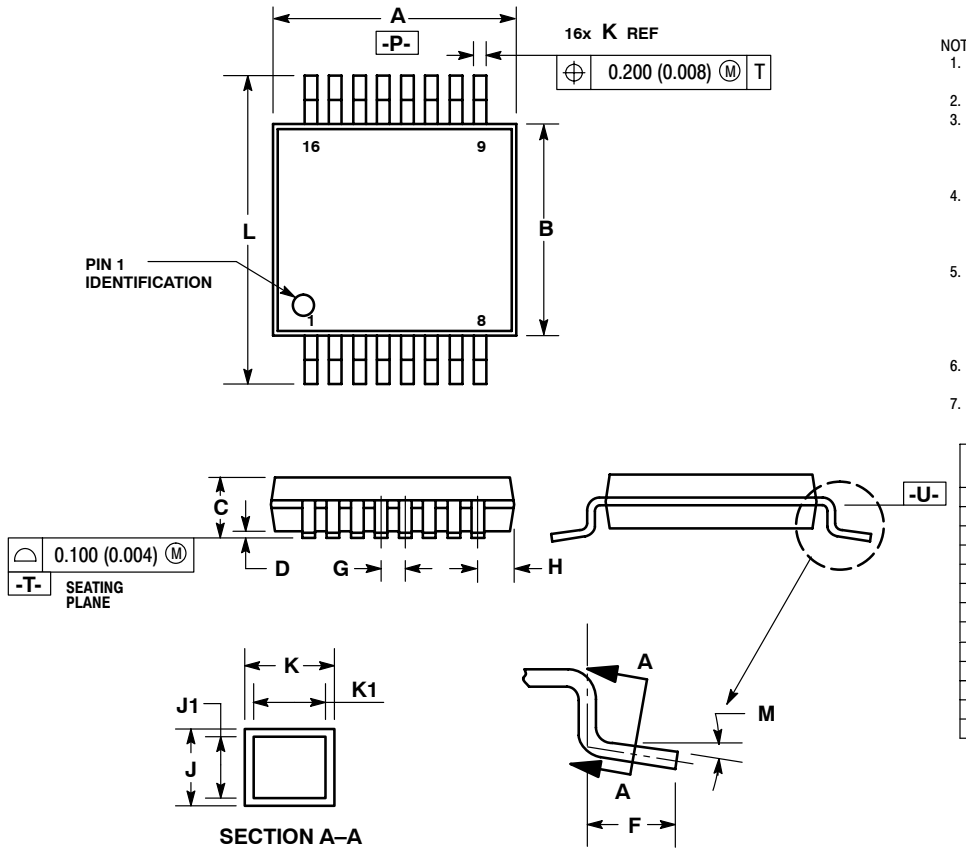


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

OUTLINE DIMENSIONS

DT SUFFIX
PLASTIC PACKAGE
CASE 948C–03
(TSSOP–16)
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -U-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	5.10	---	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0047
D	0.05	0.25	0.002	0.010
F	0.45	0.55	0.018	0.022
G	0.65 BSC		0.026 BSC	
H	0.22	0.23	0.009	0.010
J	0.09	0.24	0.004	0.009
J1	0.09	0.18	0.004	0.007
K	0.16	0.32	0.006	0.013
K1	0.16	0.26	0.006	0.010
L	6.30	6.50	0.248	0.256
M	0°	10°	0°	10°

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P.O. Box 5405, Denver, Colorado 80217. 1–303–675–2140 or 1–800–441–2447

Technical Information Center: 1–800–521–6274

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center, 3–20–1, Minami–Azabu. Minato–ku, Tokyo 106–8573 Japan. 81–3–3440–3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2, Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong. 852–26668334

HOME PAGE: http://www.motorola.com/semiconductors/

DATA SHEET

SA612A
Double-balanced mixer and oscillator

Product specification
Replaces data of September 17, 1990
IC17 Data Handbook

1997 Nov 07

PHILIPS

Double-balanced mixer and oscillator SA612A

DESCRIPTION

The SA612A is a low-power VHF monolithic double-balanced mixer with on-board oscillator and voltage regulator. It is intended for low cost, low power communication systems with signal frequencies to 500MHz and local oscillator frequencies as high as 200MHz. The mixer is a “Gilbert cell” multiplier configuration which provides gain of 14dB or more at 45MHz.

The oscillator can be configured for a crystal, a tuned tank operation, or as a buffer for an external L.O. Noise figure at 45MHz is typically below 6dB and makes the device well suited for high performance cordless phone/cellular radio. The low power consumption makes the SA612A excellent for battery operated equipment. Networking and other communications products can benefit from very low radiated energy levels within systems. The SA612A is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface mounted miniature package).

FEATURES

- Low current consumption
- Low cost
- Operation to 500MHz
- Low radiated energy
- Low external parts count; suitable for crystal/ceramic filter
- Excellent sensitivity, gain, and noise figure

PIN CONFIGURATION

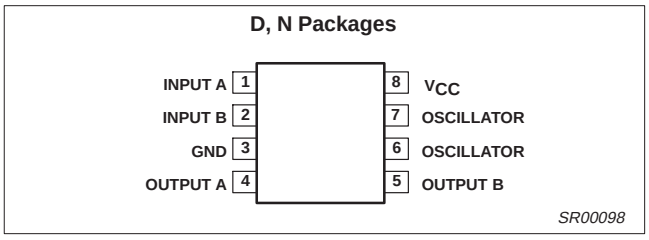


Figure 1. Pin Configuration

APPLICATIONS

- Cordless telephone
- Portable radio
- VHF transceivers
- RF data links
- Sonabuoys
- Communications receivers
- Broadband LANs
- HF and VHF frequency conversion
- Cellular radio mixer/oscillator

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Plastic (DIP)	-40 to +85°C	SA612AN	SOT97-1
8-Pin Plastic Small Outline (SO) package (Surface-Mount)	-40 to +85°C	SA612AD	SOT96-1

BLOCK DIAGRAM

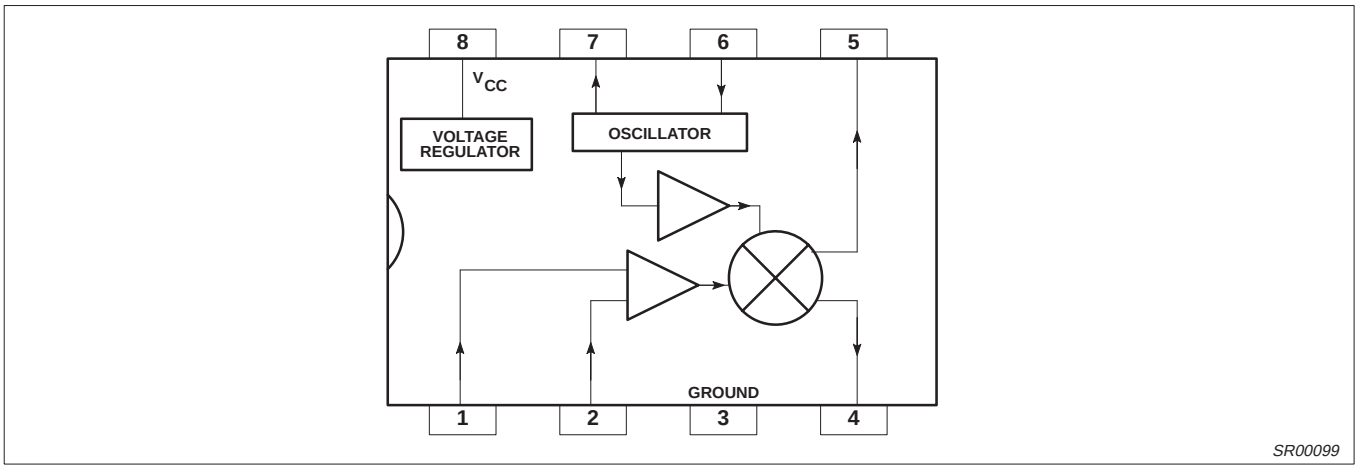


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature	-65 to +150	°C
T_A	Operating ambient temperature range SA612A	-40 to +85	°C

AC/DC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_{CC} = 6V, Figure 3

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	3.0	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figured at 45MHz			5.0		dB
	Third-order intercept point at 45MHz	RF_{IN}=-45dBm		-13		dBm
	Conversion gain at 45MHz		14	17		dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3		pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

DESCRIPTION OF OPERATION

The SA612A is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The SA612A is designed for optimum low power performance. When used with the SA614A as a 45MHz cordless phone/cellular radio 2nd IF and demodulator, the SA612A is capable of receiving -119dBm signals with a 12dB S/N ratio. Third-order intercept is typically -15dBm (that's approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small-signal or signal-to-noise issues not critical, the input to the SA612A should be appropriately scaled.

TEST CONFIGURATION

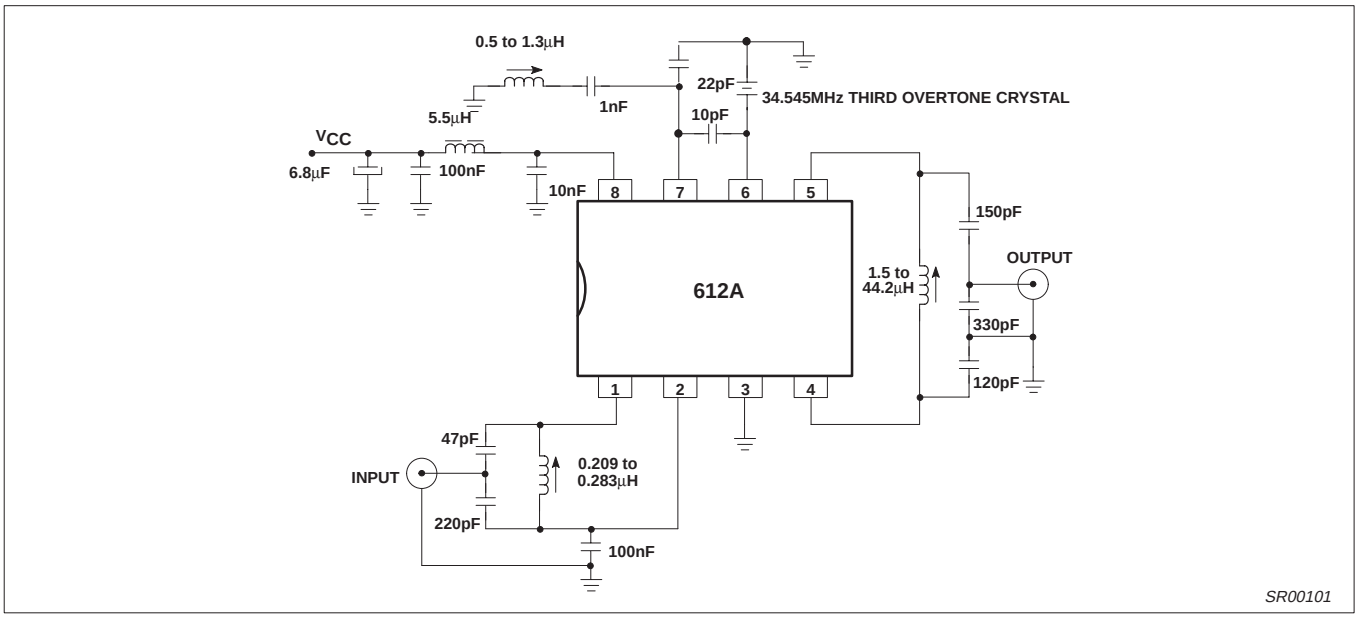


Figure 3. Test Configuration

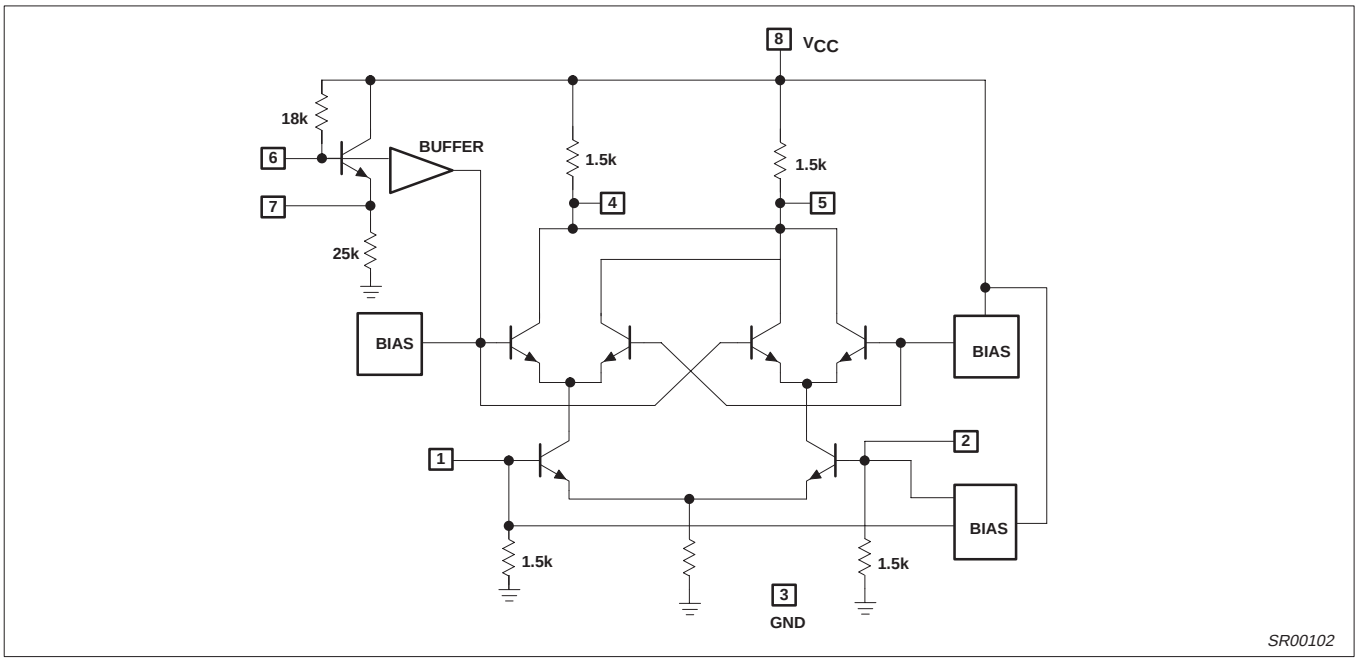


Figure 4. Equivalent Circuit

Besides excellent low power performance well into VHF, the SA612A is designed to be flexible. The input, output, and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedance is approximately 1.5k || 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 5 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 6 shows three single-ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank “Q” and required drive levels. The higher the Q of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required L.O. is beyond oscillation limits, or the system calls for an external L.O., the external signal can be injected at Pin 6 through a DC blocking capacitor. External L.O. should be 200mV$_{P-P}$ minimum to 300mV$_{P-P}$ maximum.

Figure 7 shows several proven oscillator circuits. Figure 7a is appropriate for cordless phones/cellular radio. In this circuit a third overtone parallel-mode crystal with approximately 5pF load capacitance should be specified. Capacitor C3 and inductor L1 act as a fundamental trap. In fundamental mode oscillation the trap is omitted.

Figure 8 shows a Colpitts varacter tuned tank oscillator suitable for synthesizer-controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar circuits provide the simple solution for non-critical applications. The resistive divider in the emitter-follower circuit should be chosen to provide the minimum input signal which will assume correct system operation.

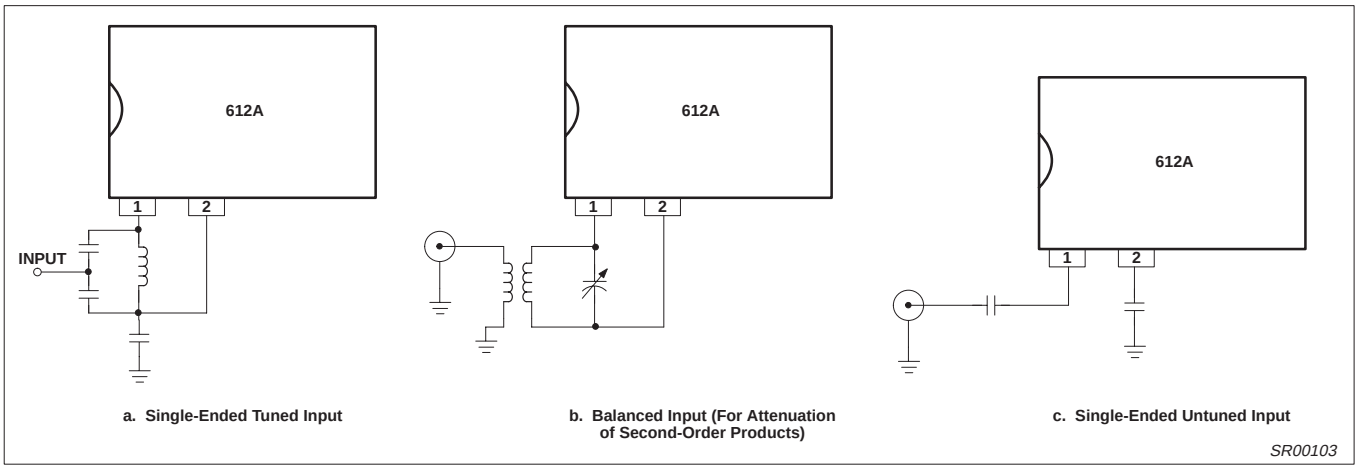


Figure 5. Input Configuration

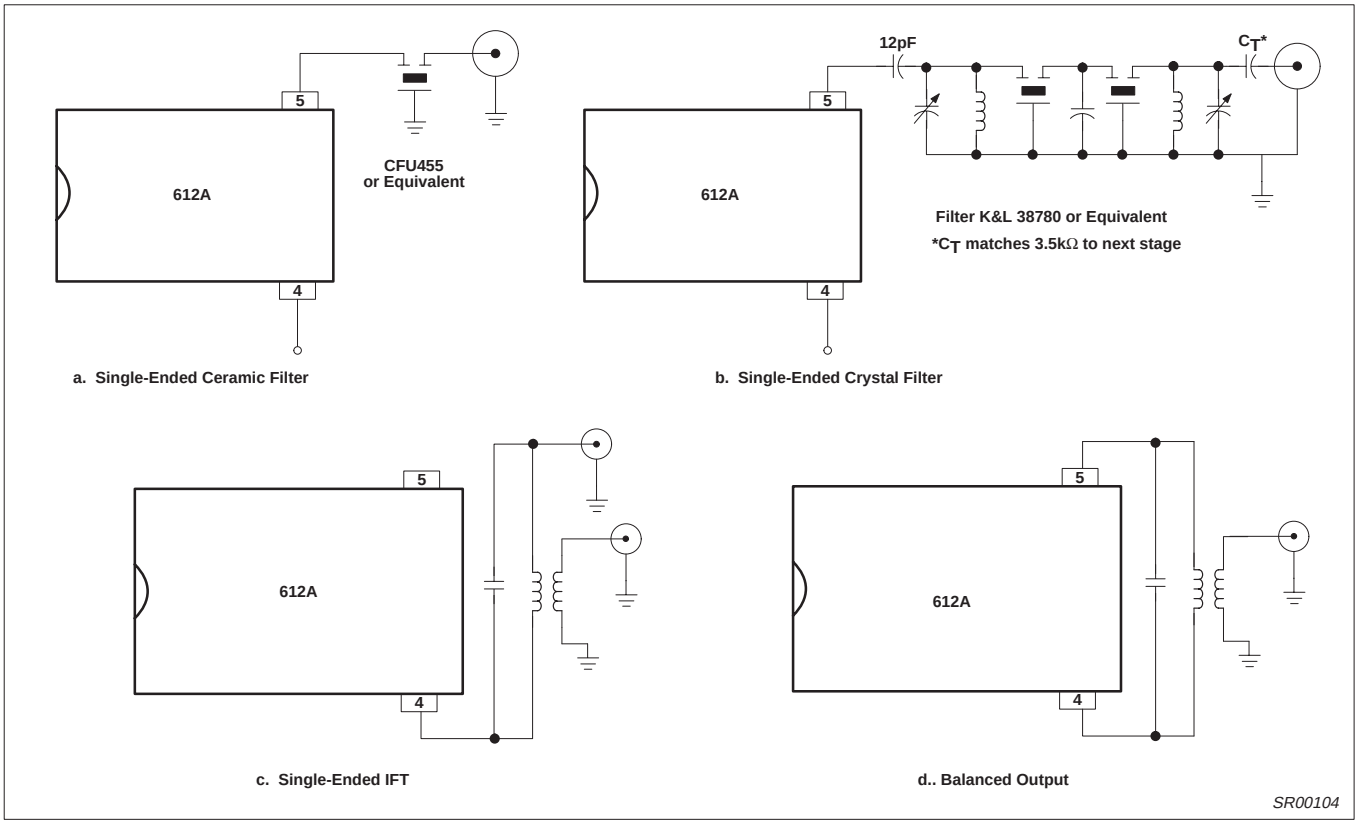


Figure 6. Output Configuration

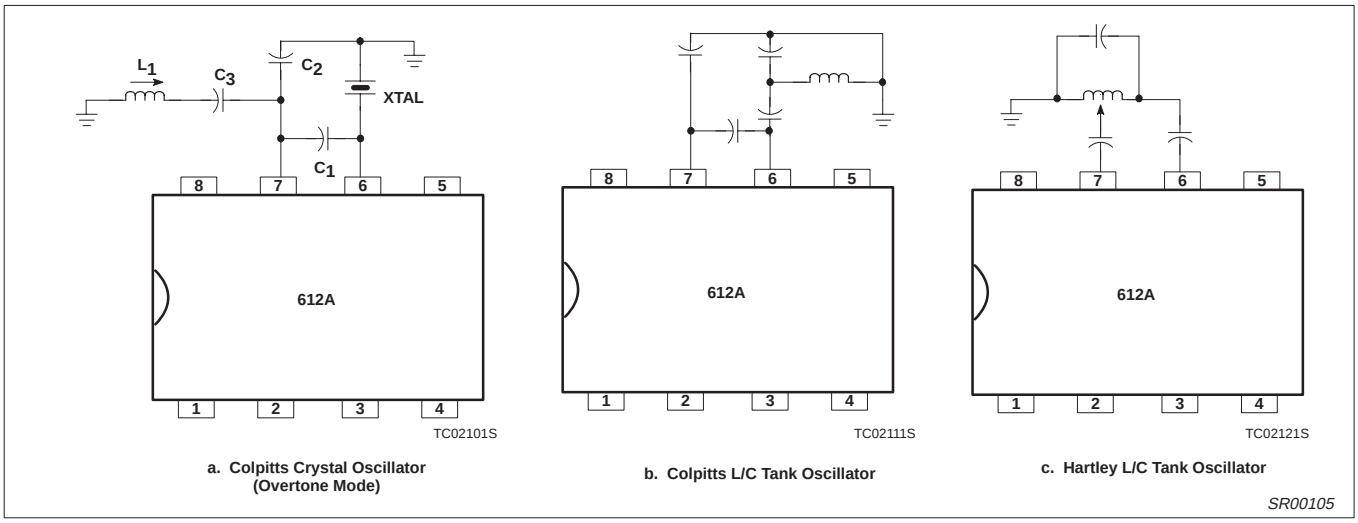


Figure 7. Oscillator Circuits

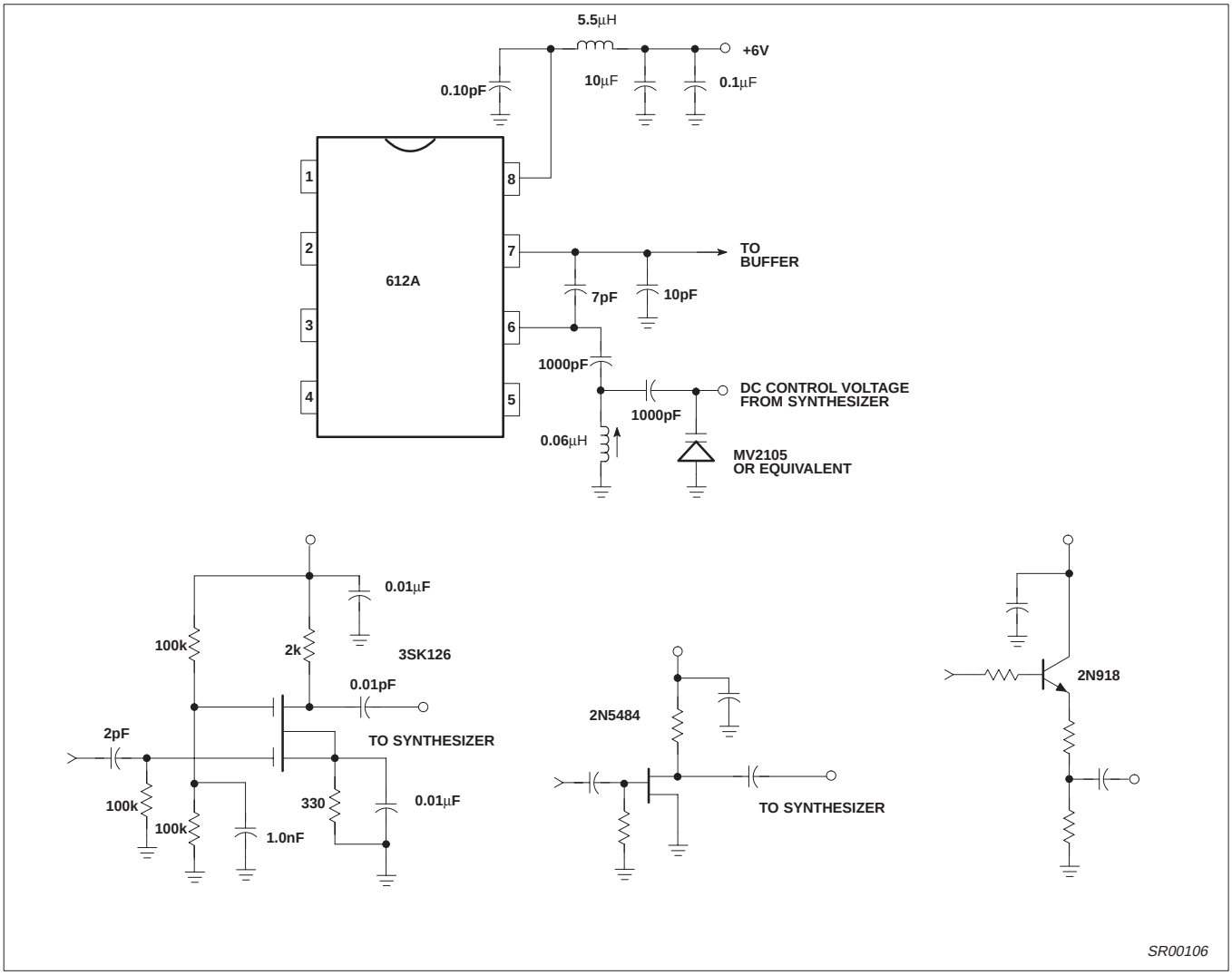


Figure 8. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

TEST CONFIGURATION

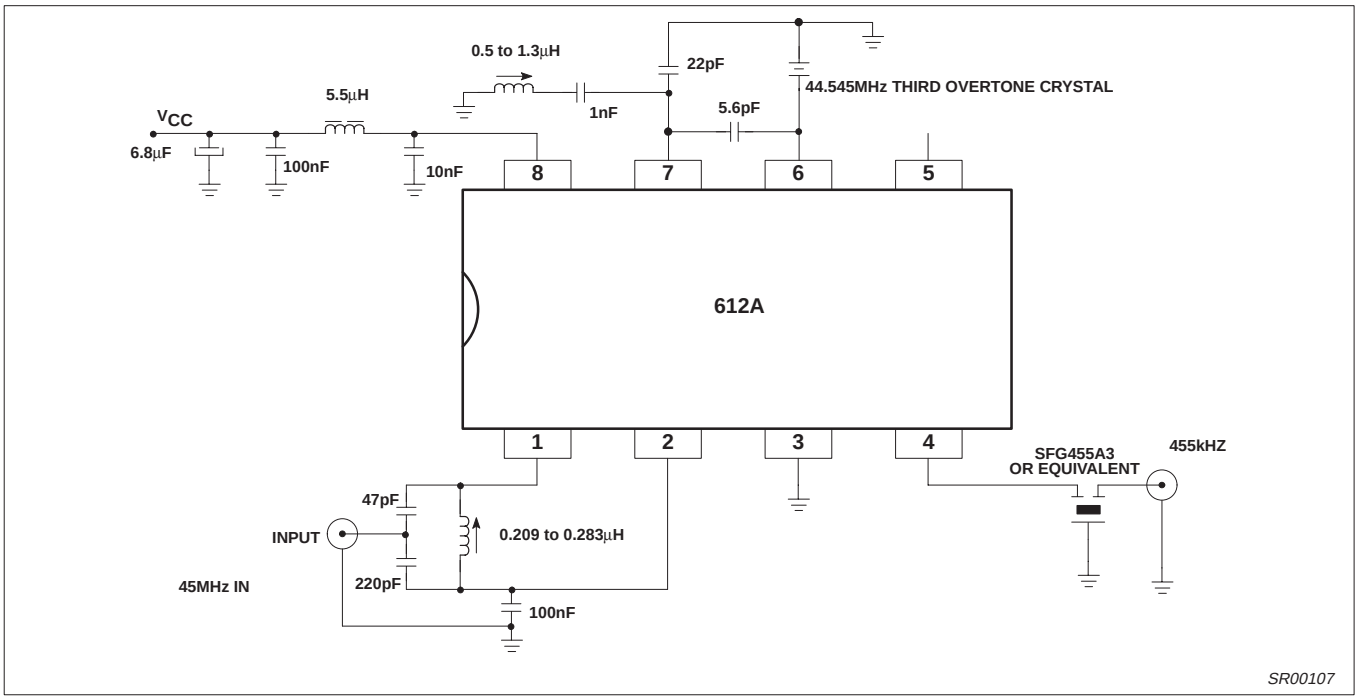


Figure 9. Typical Application for Cordless/Cellular Radio

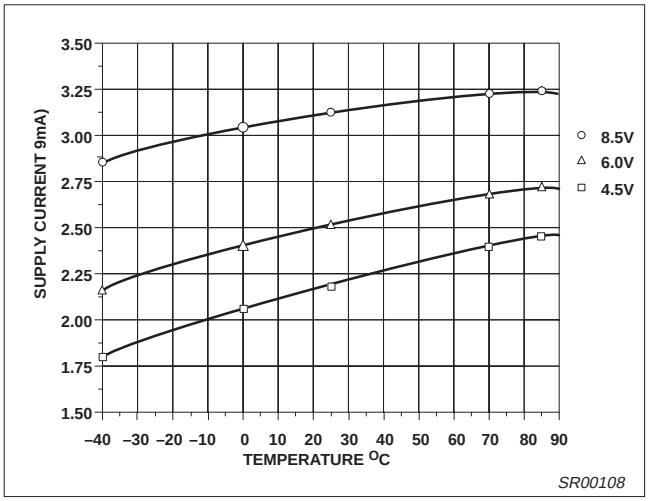


Figure 10. I_{CC} vs Supply Voltage

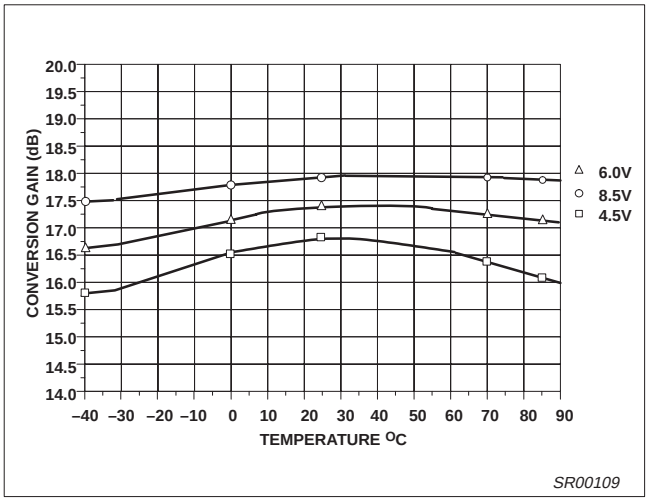


Figure 11. Conversion Gain vs Supply Voltage

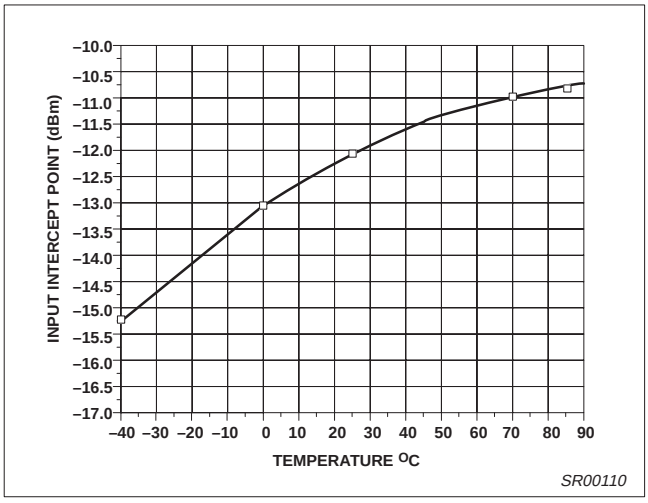


Figure 12. Third-Order Intercept Point

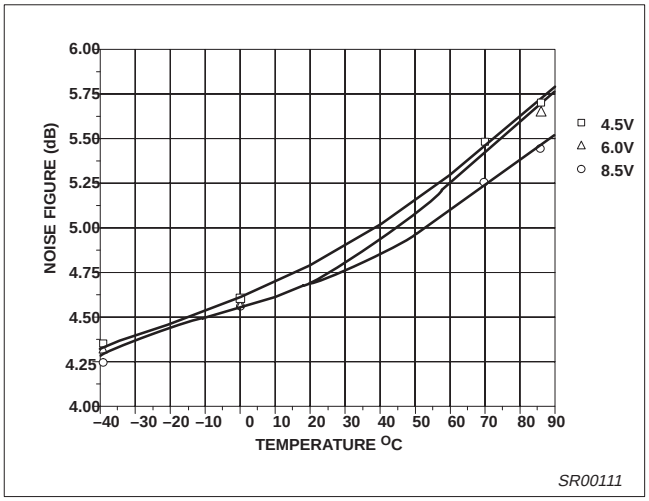


Figure 13. Noise Figure

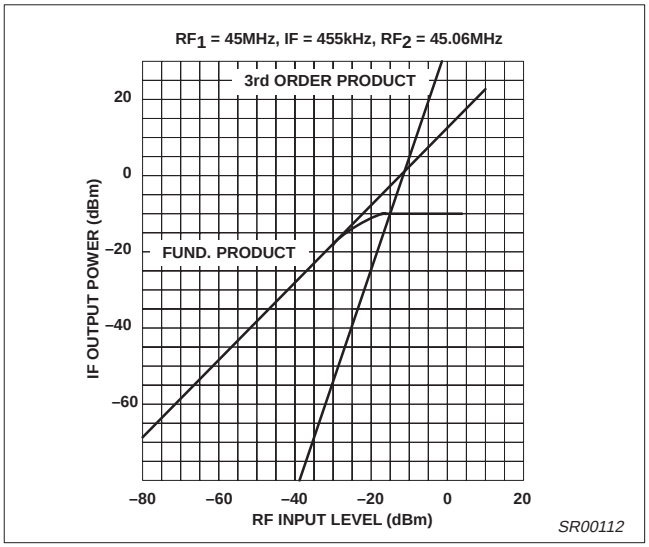


Figure 14. Third-Order Intercept and Compression

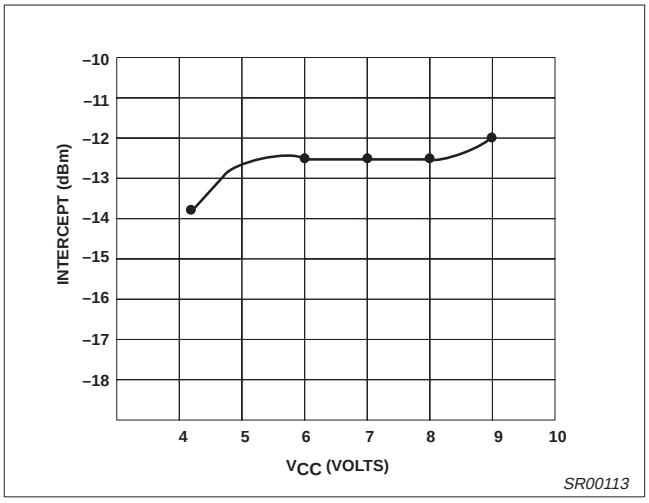
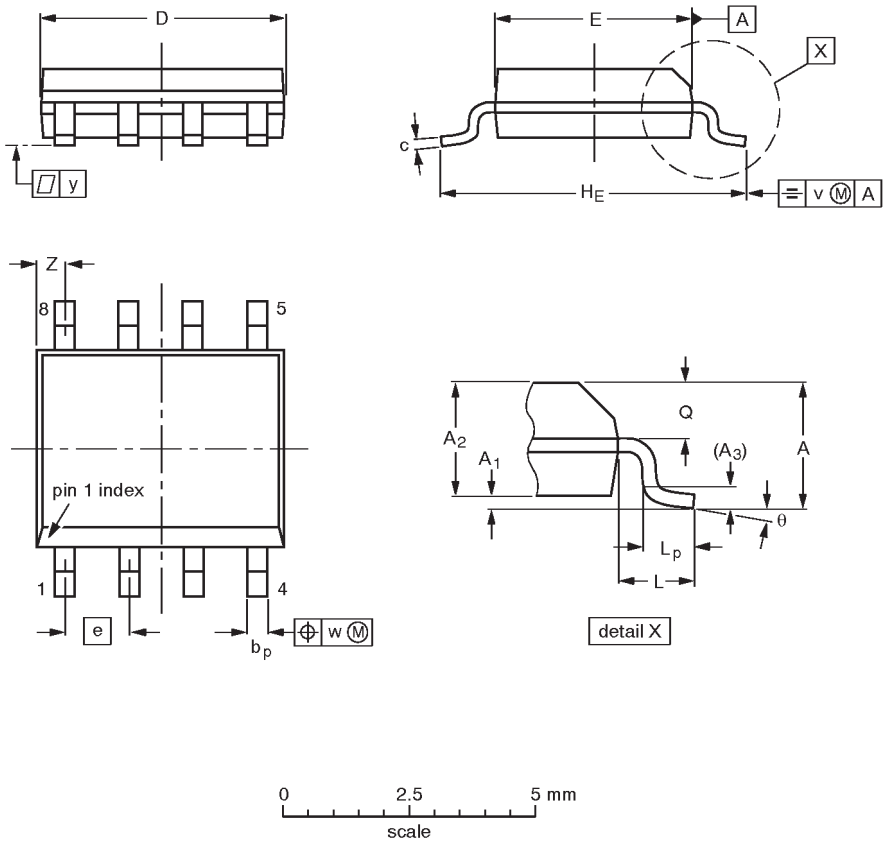


Figure 15. Input Third-Order Intermod Point vs V_{CC}

SO8: plastic small outline package; 8 leads; body width 3.9mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

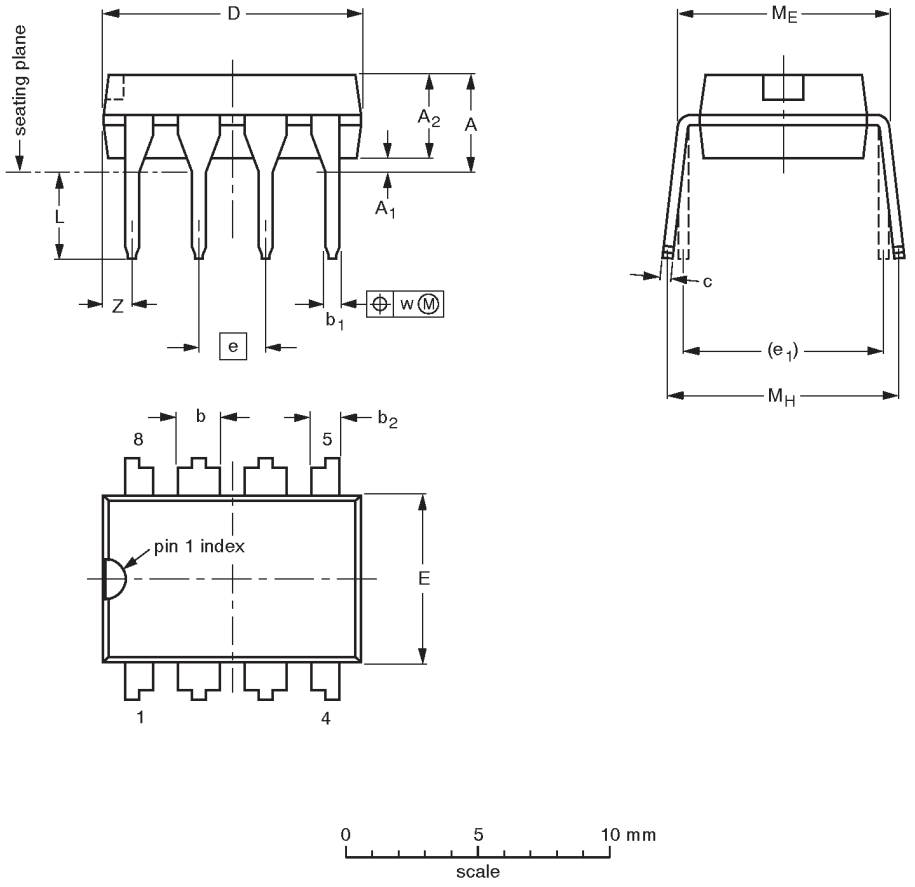
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.20 0.19	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~92-11-17~~ 95-02-04

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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Let's make things better.

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PHILIPS

Microphone Preamplifier with Variable Compression and Noise Gating

SSM2165*

FEATURES

Complete Microphone Conditioner in an 8-Lead Package
Single +5 V Operation
Preset Noise Gate Threshold
Compression Ratio Set by External Resistor
Automatic Limiting Feature Prevents ADC Overload
Adjustable Release Time
Low Noise and Distortion
20 kHz Bandwidth (±1 dB)
Low Cost

APPLICATIONS

Microphone Preamplifier/Processor
Computer Sound Cards
Public Address/Paging Systems
Communication Headsets
Telephone Conferencing
Guitar Sustain Effects Generator
Computerized Voice Recognition
Surveillance Systems
Karaoke and DJ Mixers

GENERAL DESCRIPTION

The SSM2165 is a complete and flexible solution for conditioning microphone inputs in computer audio systems. It is also excellent for improving vocal clarity in communications and public address systems. A low noise voltage controlled amplifier (VCA) provides a gain that is dynamically adjusted by a control loop to maintain a set compression characteristic. The compression ratio is set by a single resistor and can be varied from 1:1 to over 15:1 relative to the fixed rotation point. Signals above the rotation point are limited to prevent overload and to eliminate "popping." A downward expander (noise gate) prevents amplification of noise or hum. This results in optimized signal levels prior to digitization, thereby eliminating the need for additional gain or attenuation in the digital domain that could add noise or impair accuracy of speech recognition algorithms. The flexibility of setting the compression ratio and the time constant of the level detector, coupled with two values of rotation point, make the SSM2165 easy to integrate in a wide variety of microphone conditioning applications.

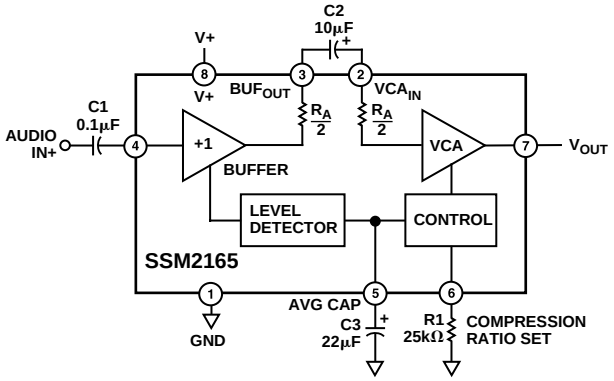
The SSM2165 is an ideal companion product for audio codecs used in computer systems, such as the AD1845 and AD1847. The device is available in 8-lead SOIC and P-DIP packages, and guaranteed for operation over the extended industrial temperature range of –40°C to +85°C. As shown in Figure 1a, the SSM2165-1 has a rotation point of –25.7 dBu (40 mV)[1], a VCA gain of 18 dB, and gives –7.7 dBu (320 mV) before limiting. As shown in Figure 1b, the SSM2165-2 has a rotation point of –17.8 dBu (100 mV),

*Patents pending.

[1]All signals are in rms volts or dBu (0 dBu = 0.775 V rms).

REV. A

FUNCTIONAL BLOCK DIAGRAM



a VCA gain of 8 dB and gives –9.8 dBu (250 mV) before limiting. Both have a noise gate threshold of –64 dBu (500 µV), below which downward expansion reduces the gain with a ratio of approximately 1:3. That is, a –3 dB reduction of output signal occurs with a –1 dB reduction of input signal. For applications requiring adjustable noise gate threshold, VCA gain up to 18 dB, and adjustable rotation point, please refer to the SSM2166.

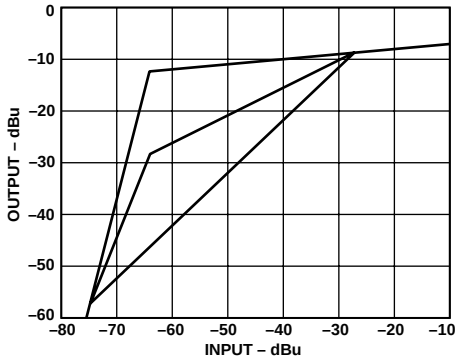


Figure 1a. SSM2165-1 Compression and Gating Characteristics

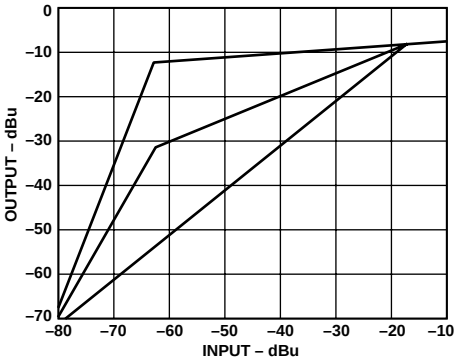


Figure 1b. SSM2165-2 Compression and Gating Characteristics

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

SSM2165–SPECIFICATIONS (V+ = +5 V, f = 1 kHz, R_L = 100 kΩ, R_{COMP} = 0 Ω, T_A = +25°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
AUDIO SIGNAL PATH						
Voltage Noise Density	e_n	15:1 Compression, V_{IN} = GND		17		nV/√Hz[2]
Noise		20 kHz Bandwidth, V_{IN} = GND		–109		dBu[1]
Total Harmonic Distortion	THD+N					
SSM2165-1		2nd and 3rd Harmonics, V_{IN} = –30 dBu		0.2	0.5	%
SSM2165-2		2nd and 3rd Harmonics, V_{IN} = –20 dBu		0.2	0.5	%
		22 kHz Low-Pass Filter				
Input Impedance	Z_{IN}			180		kΩ
Output Impedance	Z_{OUT}			75		Ω
Load Drive		Resistive	5			kΩ
		Capacitive			2	nF
Input Voltage Range		1% THD		1		V rms
Output Voltage Range		1% THD		1.4		V rms
Gain Bandwidth Product		1:1 Compression				
SSM2165-1		VCA G = 18 dB		300		kHz
SSM2165-2		VCA G = 8 dB		100		kHz
CONTROL SECTION						
VCA Dynamic Gain Range				40		dB
VCA Fixed Gain						
SSM2165-1				18		dB
SSM2165-2				8		dB
Rotation Point						
SSM2165-1				40		mV rms
SSM2165-2				100		mV rms
Compression Ratio, Min				1:1		
Compression Ratio, Max				15:1		
Control Feedthrough		15:1 Compression		±5		mV
POWER SUPPLY						
Supply Voltage Range	V_S		4.5		5.5	V
Supply Current	I_{SY}			7.5	10	mA
Quiescent Output Voltage Level				2.2		V
Power Supply Rejection Ratio[2]	PSRR			50		dB

NOTES
[1]0 dBu = 0.775 V rms.
[2]Referred to input.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . +10 V
Audio Input Voltage . . . . . Supply Voltage
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature (T_J) . . . . . +150°C
Lead Temperature (Soldering, 60 sec) . . . . . +300°C

ESD RATINGS

883 (Human Body) Model . . . . . 2.0 kV

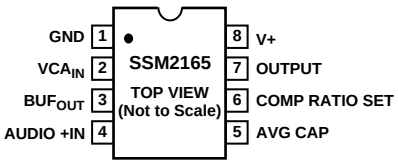
THERMAL CHARACTERISTICS

Thermal Resistance
8-Lead Plastic DIP
θ_{JA} . . . . . 103°C/W
θ_{JC} . . . . . 43°C/W
8-Lead SOIC
θ_{JA} . . . . . 158°C/W
θ_{JC} . . . . . 43°C/W

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
SSM2165-1P	–40°C to +85°C	Plastic DIP	N-8
SSM2165-2P	–40°C to +85°C	Plastic DIP	N-8
SSM2165-1S	–40°C to +85°C	Narrow SOIC	SO-8
SSM2165-2S	–40°C to +85°C	Narrow SOIC	SO-8

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin #	Mnemonic	Function
1	GND	Ground
2	VCA_{IN}	VCA Input Pin. A typical connection is a 1 µF–10 µF capacitor from the buffer output pin (Pin 3) to this pin.
3	BUF_{OUT}	Input Buffer Amplifier Output Pin. Must not be loaded by capacitance to ground.
4	AUDIO +IN	Input Audio Signal. The input signal should be ac-coupled (0.1 µF typical) into this pin.
5	AVG CAP	Detector Averaging Capacitor. A capacitor, 2.2 µF–22 µF, to ground from this pin is the averaging capacitor for the detector circuit.
6	COMP RATIO SET	Compression Ratio Set Pin. A resistor to ground from this pin sets the compression ratio as shown in Figure 1.
7	OUTPUT	Output Signal.
8	V+	Positive Supply, +5 V Nominal.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the SSM2165 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

SSM2165–Typical Performance Characteristics

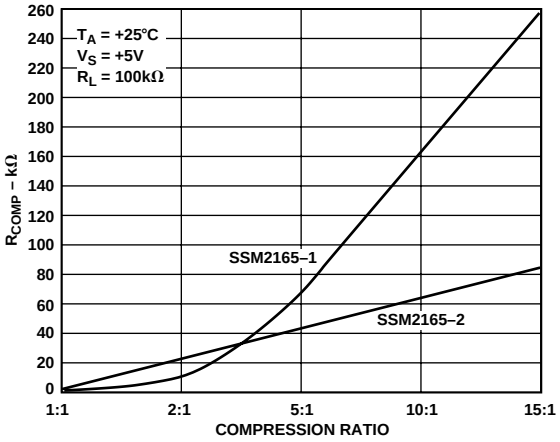


Figure 2. Compression Ratio vs. R_{COMP}

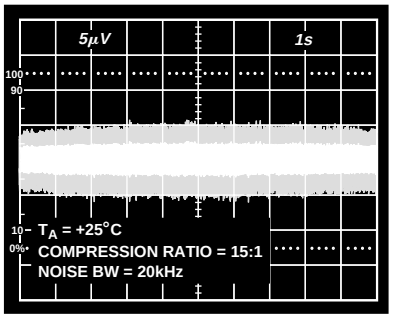


Figure 5. Wideband Output Noise

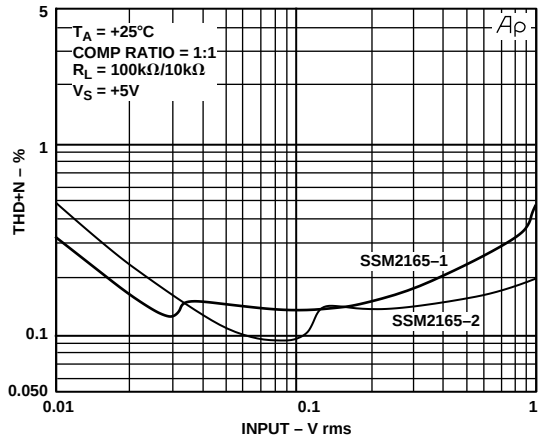


Figure 3. THD + N (%) vs. Input (V rms)

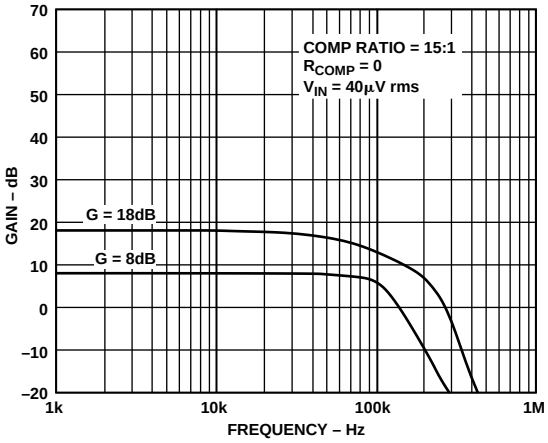


Figure 6. GBW Curves vs. VCA Gain

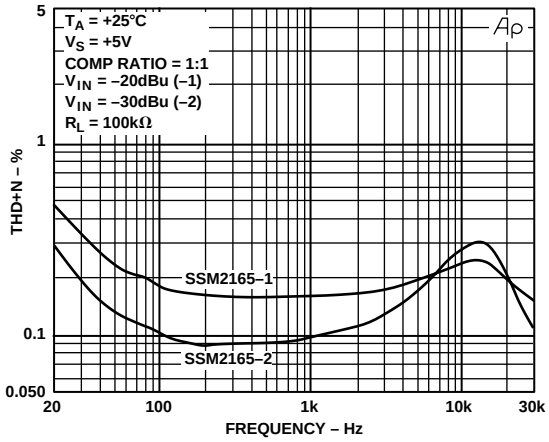


Figure 4. THD + N (%) vs. Frequency (Hz)

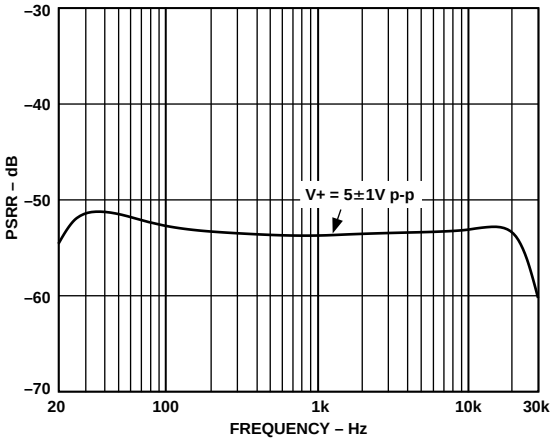


Figure 7. PSRR vs. Frequency, Referred to Input

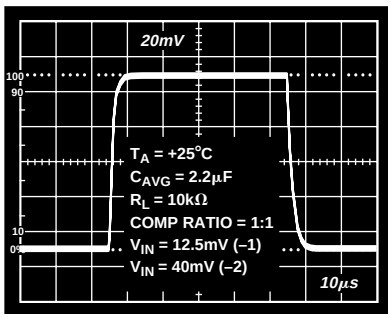


Figure 8. Small Signal Transient Response

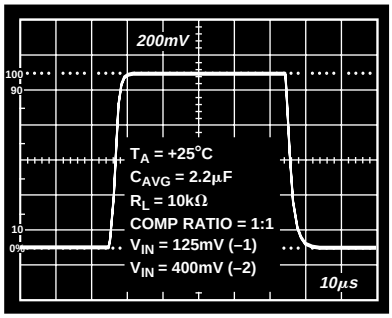


Figure 9. Large Signal Transient Response

APPLICATIONS INFORMATION

The SSM2165 is a complete microphone signal conditioning system in a single integrated circuit. Designed primarily for voiceband applications, this integrated circuit provides amplification, rms detection, limiting, variable compression, and downward expansion. The internal rms detector has a time constant set by an external capacitor. An integral voltage-controlled amplifier (VCA) provides up to 40 dB of gain in the signal path with approximately 30 kHz bandwidth. The device operates on a single +5 V supply, accepts input signals up to 1 V[1], and produces output signal levels at limiting of 320 mV and 250 mV for the SSM2165-1 and SSM2165-2 respectively, into loads > 5 kΩ.

The SSM2165 contains an input buffer and automatic gain control (AGC) circuit for audio and voice band signals. Circuit operation is optimized by providing user-adjustable compression ratio and time constant. A downward expansion (noise gating) feature reduces background and circuit noise below 500 μV. The rotation point determines the output signal levels before limiting (referred to the input), and is 40 mV for the SSM2165-1 and 100 mV for the SSM2165-2.

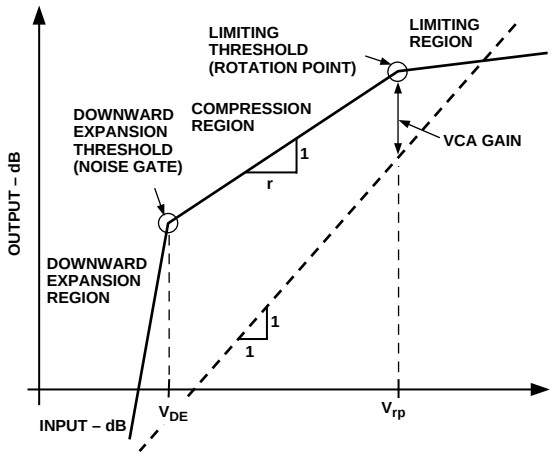


Figure 10. General Input/Output Characteristics of the SSM2165

[1]All signals are in rms volts or dBu (0 dBu = 0.775 V rms).

THEORY OF OPERATION

Figure 10 illustrates the general transfer characteristic for the SSM2165 where the output level in dBu is plotted as a function of the input level in dBu (0 dBu = 0.775 V rms). For input signals in the range of V_{DE} (Downward Expansion) to V_{RP} (Rotation Point) an "r" dB change in the input level causes a 1 dB change in the output level. Here, "r" is defined as the "compression ratio." The compression ratio may be varied from 1:1 (no compression) to over 15:1 via a single resistor, R_{COMP}. Input signals above V_{RP} are compressed with a fixed compression ratio of approximately 10:1. This region of operation is the "limiting region." Varying the compression ratio has no effect on the limiting region. The breakpoint between the compression region and the limiting region is referred to as the "limiting threshold" or "rotation point," and is different for the SSM2165-1 and SSM2165-2, see Table I.

Table I. Characteristics vs. Dash Number

SSM2165	Rotation Point	Gain	Output*
–1	40 mV (–25.7 dBu)	18 dB	320 mV (–6 dBu)
–2	100 mV (–17.7 dBu)	8 dB	250 mV (–8 dBu)

*At limiting.

The term "rotation point" derives from the observation that the straight line in the compression region "rotates" about this point on the input/output characteristic as the compression ratio is changed.

When the compression is set to 2:1, a –2 dB change of the input signal level in the compression region causes –1 dB change of the output level. Likewise, at 10:1 compression, a –10 dB change of the input signal level in the compression region causes a –1 dB change in the output level. The gain of the system with an input signal level of V_{RP} is fixed regardless of the compression ratio, and is different for the SSM2165-1 and SSM2165-2 (see Figures 1a and 1b). The "nominal gain" of the system is 18 dB for the SSM2165-1, and 8 dB for the SSM2165-2. System gain is measured at V_{RP} and is ($V_{OUT} - V_{IN}$) in dB.

Input signals below V_{DE} are downward expanded at a ratio of approximately 1:3. As a result, the gain of the system is small for very small input signal levels below V_{DE}, even though it may be quite large for input signals above V_{DE}. The downward expansion threshold, V_{DE}, is fixed at 500 μV (–64 dBu) for both dash versions.

The SSM2165 Signal Path

Figure 11 illustrates the block diagram of the SSM2165. The audio input signal is processed by the unity gain input buffer and then by the VCA. The buffer presents an input impedance of approximately 180 kΩ to the source. A dc voltage of approximately 1.5 V is present at AUDIO +IN (Pin 4), requiring the use of a blocking capacitor (C1) for ground-referenced sources. A 0.1 µF capacitor is a good choice for most audio applications. The buffer is designed to drive only the low impedance input of the VCA, and must not be loaded by capacitance to ground. The VCA is a low distortion, variable-gain amplifier whose gain is set by the internal control circuitry. The input to the VCA is a virtual ground in series with 500 Ω. An external blocking capacitor (C2) must be used between the buffer's output and the VCA input. The desired low frequency response and the total of 1 kΩ impedance between amplifiers determines the value of this capacitor. For music applications, 10 µF will give high pass f_C = 16 Hz. For voice/communications applications, 1 µF will give f_C = 160 Hz. An aluminum electrolytic capacitor is an economical choice. The VCA amplifies the input signal current flowing through C6 and converts this current to a voltage at the SSM2165's output (Pin 7). The net gain from input to output can be as high as 40 dB for high compression ratios and depending on the gain set by the control circuitry. The output impedance of the SSM2165 is typically less than 75 Ω, and the external load on Pin 7 should be >5 kΩ. The nominal output dc voltage of the device is approximately 2.2 V. Use a dc blocking capacitor for grounded loads.

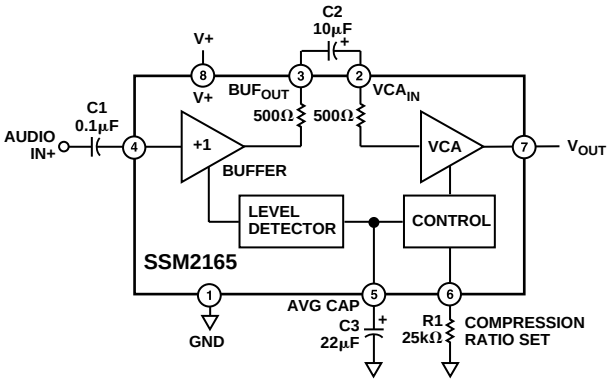


Figure 11. Functional Block Diagram and Typical Voice Application

The bandwidth of the SSM2165 is quite wide at all gain settings. The upper –3 dB point is approximately 300 kHz. The GBW plots are shown in Figure 6. While the noise of the input buffer is fixed, the input referred noise of the VCA is a function of gain. The VCA input noise is designed to be a minimum when the gain is at a maximum, thereby optimizing the usable dynamic range of the part. A photograph of the SSM2165's wideband peak-to-peak output noise is illustrated in Figure 5.

The Level Detector

The SSM2165 incorporates a full-wave rectifier and a patent-pending, true rms level detector circuit whose averaging time constant is set by an external capacitor connected to the AVG CAP pin (Pin 5). Capacitor values from 18 µF to 22 µF have been found to be more appropriate in voiceband applications, where capacitors on the low end of the range seem more appropriate for music program material. For optimal low frequency operation of the level detector down to 10 Hz, the value of the capacitor should be around 22 µF. Some experimentation with larger values for the AVG CAP may be necessary to reduce the effects of excessive low frequency ambient background noise. The value of the averaging capacitor affects sound quality: too small a value for this capacitor may cause a "pumping effect" for some signals, while too large a value can result in slow response times to signal dynamics. Electrolytic capacitors are recommended here for lowest cost.

The rms detector filter time constant is approximately given by 10 × C_{AVG} milliseconds where C_{AVG} is in µF. This time constant controls both the steady-state averaging in the rms detector as well as the release time for compression, that is, the time it takes for the system gain to react when a large input is followed by a small signal. The attack time, the time it takes for the gain to be reduced when a small signal is followed by a large signal, is mainly controlled by internal circuitry that speeds up the attack for large level changes, and controlled partly by the AVG CAP value. This limits overload time to under 1 ms in most cases.

The performance of the rms level detector is illustrated in Figure 12 for C_{AVG} = 2.2 µF and Figure 13 for C_{AVG} = 22 µF. In each of these photographs, the input signal to the SSM2165 (not shown) is a series of tone bursts in 6 successive 10 dB steps. The tone bursts range from –66 dBu (0.5 mV rms) to –6 dBu (0.5 V rms). As illustrated in the photographs, the attack time of the rms level detector is dependent only on C_{AVG}, but the release times are linear ramps whose decay times are dependent on both for C_{AVG} and the input signal step size. The rate of release is approximately 240 dB/s for a C_{AVG} = 2.2 µF, and 12 dB/s for a C_{AVG} of 22 µF.

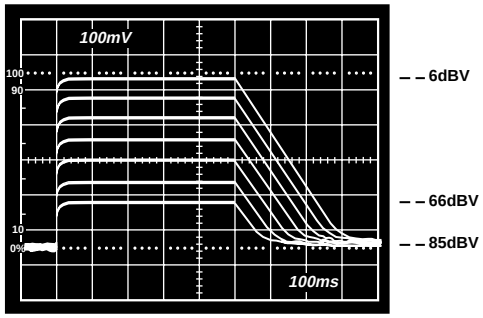


Figure 12. RMS Level Detector Performance with C_{AVG} = 2.2 µF

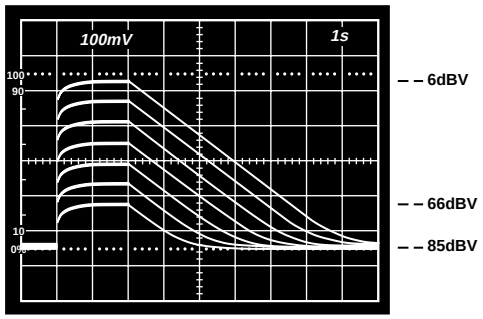


Figure 13. RMS Level Detector Performance with C_{AVG} = 22 µF

Control Circuitry
The output of the rms level detector is a signal proportional to the log of the true rms value of the buffer output with an added dc offset. The control circuitry subtracts a dc voltage from this signal, scales it, and sends the result to the VCA to control the gain. The VCA's gain control is logarithmic: a linear change in control signal causes a dB change in gain. It is this control law that allows linear processing of the log rms signal to provide the flat compression characteristic on the input/output characteristic shown in Figure 10.

Compression Ratio
Changing the scaling of the control signal fed to the VCA causes a change in the circuit's compression ratio, "r." This effect is shown in Figure 14. The compression ratio can be set by connecting a resistor between the COMP RATIO pin (Pin 6) and GND. Lowering RCOMP gives smaller compression ratios as indicated in Figure 2, with values of about 5 kΩ or less resulting in a compression ratio of 1:1. AGC performance is achieved with compression ratios between 2:1 and 15:1, and is dependent on the application. A 200 kΩ potentiometer may be used to allow this parameter to be adjusted.

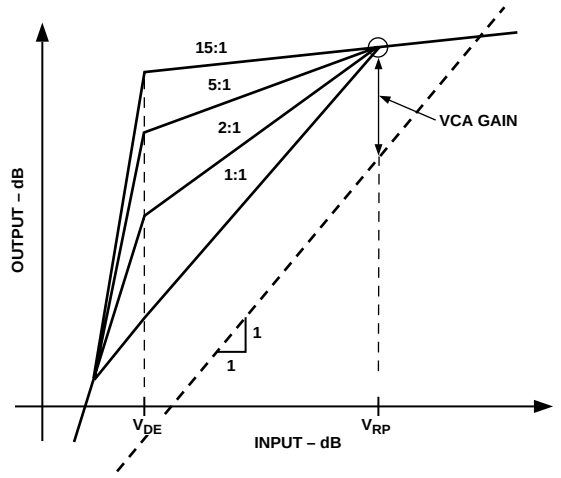


Figure 14. Effect of Varying the Compression Ratio

Rotation Point
An internal dc reference voltage in the control circuitry sets the rotation point. The rotation point determines the output level above which limiting occurs. That is, in the limiting region, a 10 dB change of input results in a 1 dB change of output. The rotation point is set to 40 mV (–26 dBu) for the SSM2165-1 and 100 mV (–18 dBu) for the SSM2165-2. In the SSM2165, limiting is compression at a fixed compression ratio of approximately 15:1. The fixed gain in the VCA is 18 dB for the SSM2165-1 and 8 dB for the SSM2165-2. The output signals at limiting are, therefore, 320 mV and 250 mV respectively. These are summarized in Table I.

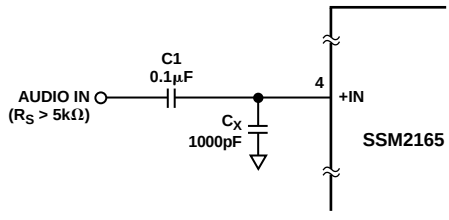
Maximum Output
Since limiting occurs for signals larger than the rotation point ($V_{IN} > V_{RP}$), the rotation point effectively sets the maximum output signal level. The application will determine which version of the SSM2165 should be selected. The output level should match the maximum input allowed by the following stage. Occasional larger signal transients will then be attenuated by the action of the limiter.

Downward Expansion Threshold
The downward expansion threshold, or noise gate, is determined by a reference voltage internal to the control circuitry. The noise gate threshold is 500 μV for both versions of the SSM2165. Users requiring some other noise gate should consider using the SSM2166. High volume users may wish to consider a custom version of the SSM2165 with other noise gate thresholds or rotation points.

Power-On/Power-Off Settling Time
Cycling the power supply to the SSM2165 will result in quick settling times: the off-on settling time of the SSM2165 is less than 200 ms, while the on-off settling time is less than 1 ms. Note that transients may appear at the output of the device during power up and power down. A clickless mute function is available on the SSM2166 only.

PC Board Layout Considerations
Since the SSM2165 is capable of wide bandwidth operation at high gain, special care must be exercised in the layout of the PC board which contains the IC and its associated components. The following applications hints should be considered and/or followed:

1. In some high system gain applications, the shielding of input wires to minimize possible feedback from the output of the SSM2165 back to the input circuit may be necessary.
2. A single-point ("star") ground implementation is recommended in addition to maintaining short lead lengths and PC board runs. In systems where an analog ground and a digital ground are available, the SSM2165 and its surrounding circuitry should be connected to the analog ground. Wire-wrap board connections and grounding implementations are to be explicitly avoided.
3. The internal buffer of the SSM2165 was designed to drive only the input of the internal VCA and its own feedback network. Stray capacitive loading to ground from either Pin 3 or Pin 2 in excess of 5 pF to 10 pF can cause excessive phase shift and can lead to circuit instability.
4. When using high impedance sources, it can be advantageous to shunt the source with a capacitor to ground at the input pin of the IC (Pin 4) to lower the source impedance at high frequencies, as shown in Figure 15. A capacitor with a value of 1000 pF is a good starting value and sets a low pass corner at 31 kHz for 5 kΩ sources.



NOTE: ADDITIONAL CIRCUIT DETAILS OMITTED FOR CLARITY.

Figure 15. Circuit Configuration for Use with High Impedance Signal Sources

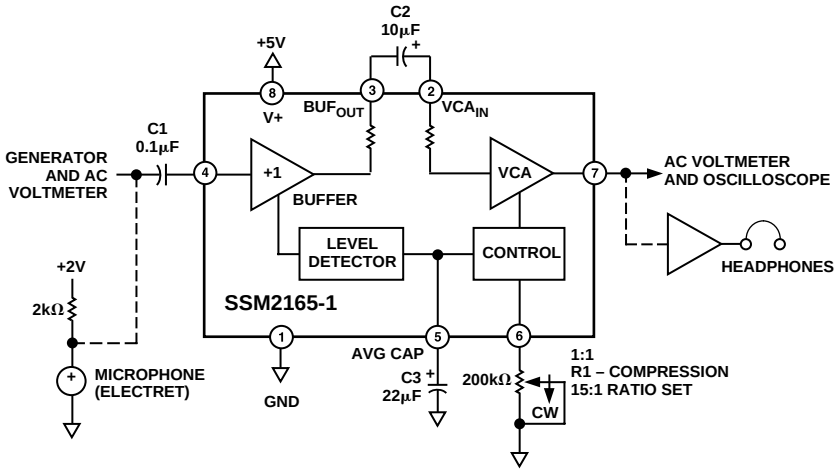


Figure 16. Electret Microphone Preamp Example

Compression Adjustment—A Practical Example

To illustrate how to set the compression ratio of the SSM2165, we will take a practical example. The SSM2165 will be used interface an electret-type microphone to a post-amplifier, as shown in Figure 16. The signal from the microphone was measured under actual conditions to vary from 2 mV to 30 mV. The post-amplifier requires no more than 350 mV at its input. We will therefore choose the SSM2165-1, whose "rotation" point is 40 mV and whose VCA fixed gain is 18 dB (×8), thus giving 320 mV at limiting. From prior listening experience, we will use a 2:1 compression ratio. The noise gate threshold of the SSM2165-1 will operate when the input signal falls below 500 µV. These objectives are summarized in Table II. The transfer characteristic we will implement is illustrated in Figure 18.

Table II. Objective Specification of Example

Input Range	2 mV–30 mV
Output Range	To 350 mV
Limiting Level	320 mV
Compression	2:1
Gain	18 dB
Noise Gate	500 µV

Test Equipment Setup

The recommended equipment and configuration is shown in Figure 17. A low noise audio generator with a smooth output adjustment range of 100 µV to 25 mV is a suitable signal source. The output voltmeter should go up to 2 volts. The oscilloscope is used to verify that the output is sinusoidal, that no clipping is occurring in the buffer, and to observe the limiting and noise gating "knees."

Breadboard Considerations

When building your breadboard, keep the leads to Pins 2 and 3 as short as possible. Use a central analog ground and decouple power supply connections adequately.

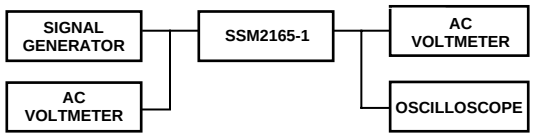


Figure 17. Test Equipment Setup

STEP 1. Initialize Potentiometer

With power off, preset R1—Compression Ratio potentiometer to zero ohms.

STEP 2. Check Setup

With power on, adjust the generator for an input level of 50 mV (–24 dBu), 1 kHz. The output meter should indicate approximately 350 mV (–6.9 dBu). If not, check your setup.

STEP 3. Find the Rotation Point

Set the input level to 50 mV (–24 dBu), and observe the output on the oscilloscope. The output will be in the limiting range of operation. Slowly reduce the input signal level until the output level just begins to stop limiting and follows the input down. Increase the input so that the output is 320 mV (–7.7 dBu). You have located the knee of the rotation point.

STEP 4. Adjust the Compression Ratio

With the input set as in Step 3, note the exact value of the input signal level just below the knee (around 40 mV (–26 dBu)). Next, reduce the input to 1/4 the value noted, (around 10 mV (–38 dBu)), for a change of –12 dB. Next, increase the R_{COMP} potentiometer resistance so the output is 160 mV (–13.7 dBu) for an output change of –6 dB. You have now set the compression, which is the ratio of input change to output change, in dB, to 2:1.

STEP 5. Confirm the Noise Gate Threshold

Set the input to 1 mV, and observe the output on the oscilloscope. A 20 dB pad between generator and input may facilitate this measurement. Reduce the input gradually until the output falls off more rapidly. This point is the noise gate threshold, and should be approximately 500 µV (–64 dBu). The noise gate threshold on the SSM2165 is fixed at 500 µV, a practical value for many microphones. Should you require a different noise gate threshold, consider using the SSM2166.

STEP 6. Listen

At this time, you may replace the signal generator with a properly powered electret microphone and listen to the results through a set of headphones. The microphone's internal FET usually requires around +2 V through a 2 kΩ resistor; this varies with the manufacturer. Experiment with the compression ratio value and averaging capacitor size. More compression will keep the output steady over a wider range of microphone-to-source distance. Varying the averaging capacitor, C_{AVG}, changes the

rms detector averaging time, and the decay time of the gate. Both compression ratio and decay time are usually determined by critical listening to the intended audio input.

STEP 7. Record Values

With the power removed from the test fixture, measure and record the values of the R_{COMP} and C_{AVG}.

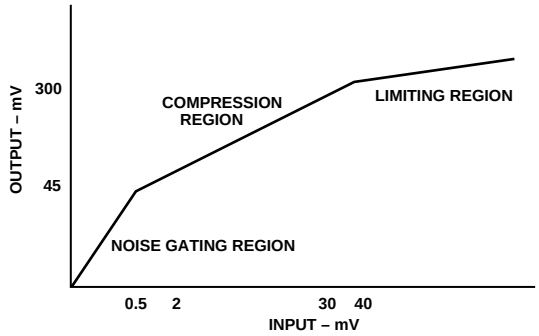


Figure 18. Transfer Characteristic

SUMMARY

We have implemented the transfer characteristic of Figure 18. For inputs below the 500 μV noise gate threshold, circuit and background noise will be downward expanded (gain-reduced) at a ratio of approximately 1:3. That is, a –1 dB change in the noise will result in –3 dB decrease at the output. Above threshold, the signal will increase at a rate of 1 dB for each 2 dB input increase, until the rotation point is reached at an input of approximately 40 mV. In the limiting region, the compression ratio increases to approximately 15:1. That is, a 15 dB increase in input will produce a 1 dB increase at the output, so there will be little further increase for higher level inputs.

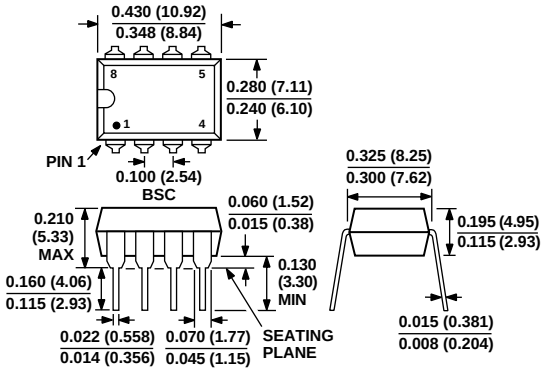
Other Versions

The SSM2165 is an 8-lead version of the 14-lead SSM2166 which is recommended for applications requiring more versatility. The SSM2166 allows selection of noise gate threshold and rotation point, and allows the buffer to provide up to 20 dB of gain. Power-down and mute functions are also built in. Customized versions of the SSM2165 are available for large volume users. The wide dynamic range of the SSM2165 makes it useful in many applications other than microphone signal conditioning such as a sustain generator for guitars. For further information, contact your Analog Devices representative.

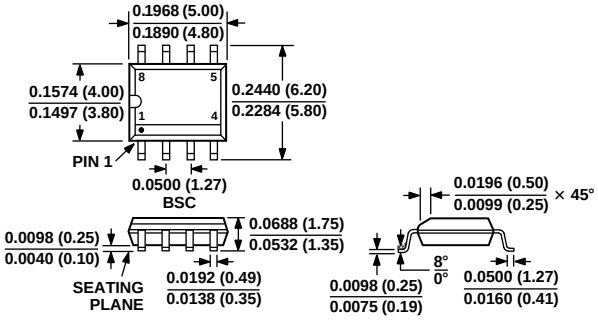
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Plastic DIP
(N-8)



8-Lead Narrow-Body SOIC
(SO-8)



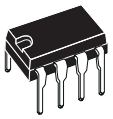
C2178a–0–6/99

PRINTED IN U.S.A.

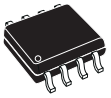
TL071
TL071A - TL071B

LOW NOISE J-FET SINGLE OPERATIONAL AMPLIFIERS

- WIDE COMMON-MODE (UP TO V_{CC}^+) AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- LOW NOISE e_n = 15nV/√Hz (typ)
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J–FET INPUT STAGE
- LOW HARMONIC DISTORTION : 0.01% (typ)
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 16V/µs (typ)



N
DIP8
(Plastic Package)



D
SO8
(Plastic Micropackage)

DESCRIPTION

The TL071, TL071A and TL071B are high speed J–FET input single operational amplifiers incorporating well matched, high voltage J–FET and bipolar transistors in a monolithic integrated circuit.

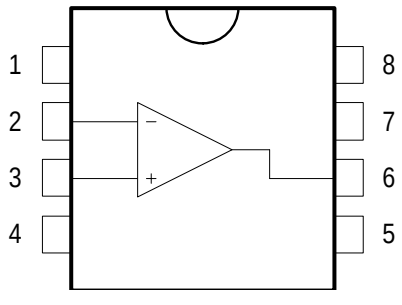
The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

ORDER CODE

Part Number	Temperature Range	Package	
		N	D
TL071M/AM/BM	-55°C, +125°C	•	•
TL071I/AI/BI	-40°C, +105°C	•	•
TL071C/AC/BC	0°C, +70°C	•	•
Example : TL071CN			

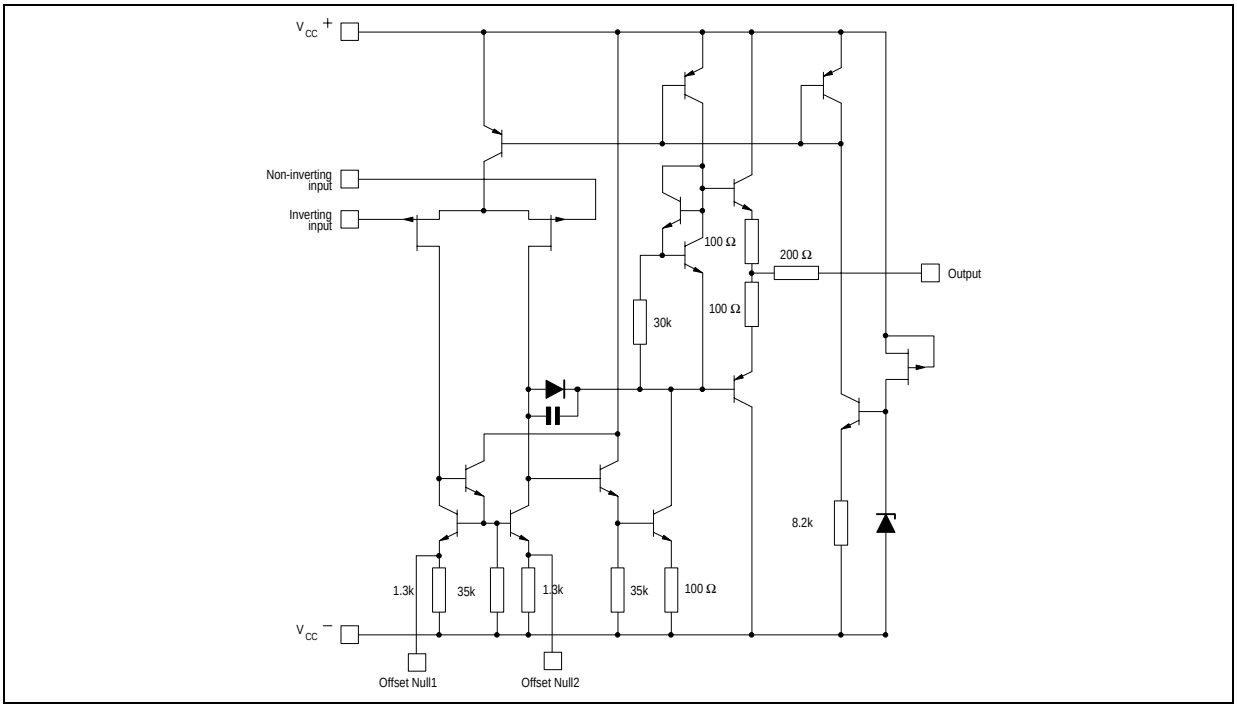
N = Dual in Line Package (DIP)
D = Small Outline Package (SO) - also available in Tape & Reel (DT)

PIN CONNECTIONS (top view)

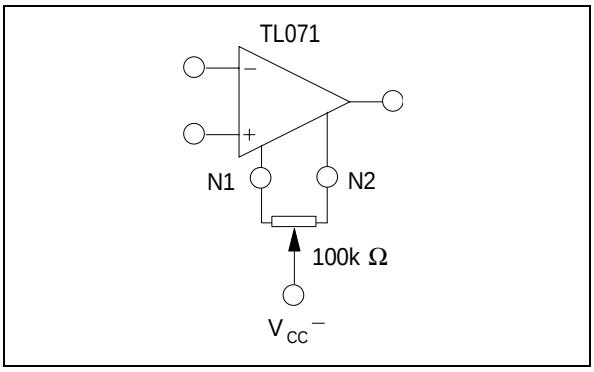


1 - Offset null 1
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-
5 - Offset null 2
6 - Output
7 - V_{CC}^+
8 - N.C.

SCHEMATIC DIAGRAM



INPUT OFFSET VOLTAGE NULL CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	TL071M, AM, BM	TL071I, AI, BI	TL071C, AC, BC	Unit
V_{CC}	Supply voltage - note 1)	±18			V
V_i	Input Voltage - note 2)	±15			V
V_{id}	Differential Input Voltage - note 3)	±30			V
P_{tot}	Power Dissipation	680			mW
	Output Short-circuit Duration - note 4)	Infinite			
T_{oper}	Operating Free-air Temperature Range	-55 to +125	-40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range	-65 to +150			°C

1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
3. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded

ELECTRICAL CHARACTERISTICS

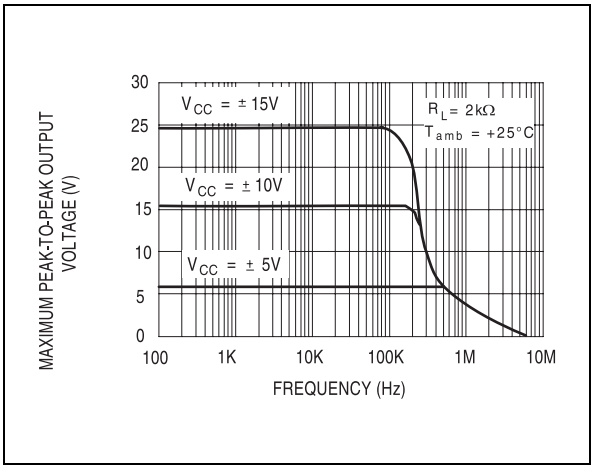
V_{CC} = ±15V, T_{amb} = +25°C (unless otherwise specified)

Symbol	Parameter		TL071I,M,AC,AI,AM, BC,BI,BM			TL071C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage (R_S = 50Ω) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$	TL071 TL071A TL071B TL071 TL071A TL071B		3 3 1	10 6 3 13 7 5		3	10 13	mV
DV_{io}	Input Offset Voltage Drift			10			10		µV/°C
I_{io}	Input Offset Current T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$			5	100 4		5	100 10	pA nA
I_{ib}	Input Bias Current -note 1) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$			20	200 20		20	200 20	pA nA
A_{vd}	Large Signal Voltage Gain (R_L = 2kΩ, V_o = ±10V) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		50 25	200		25 15	200		V/mV
SVR	Supply Voltage Rejection Ratio (R_S = 50Ω) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		80 80	86		70 70	86		dB
I_{CC}	Supply Current, no load T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$			1.4	2.5 2.5		1.4	2.5 2.5	mA
V_{icm}	Input Common Mode Voltage Range		±11	+15 -12		±11	+15 -12		V
CMR	Common Mode Rejection Ratio (R_S = 50Ω) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		80 80	86		70 70	86		dB
I_{os}	Output Short-circuit Current T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		10 10	40	60 60	10 10	40	60 60	mA
$\pm V_{opp}$	Output Voltage Swing T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$	RL = 2kΩ RL = 10kΩ RL = 2kΩ RL = 10kΩ	10 12 10 12	12 13.5		10 12 10 12	12 13.5		V
SR	Slew Rate (T_{amb} = +25°C) V_{in} = 10V, R_L = 2kΩ, C_L = 100pF, unity gain		8	16		8	16		V/µs
t_r	Rise Time (T_{amb} = +25°C) V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, unity gain			0.1			0.1		µs
K_{ov}	Overshoot (T_{amb} = +25°C) V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, unity gain			10			10		%
GBP	Gain Bandwidth Product (T_{amb} = +25°C) V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF, f= 100kHz		2.5	4		2.5	4		MHz
R_i	Input Resistance			10^{12}			10^{12}		Ω

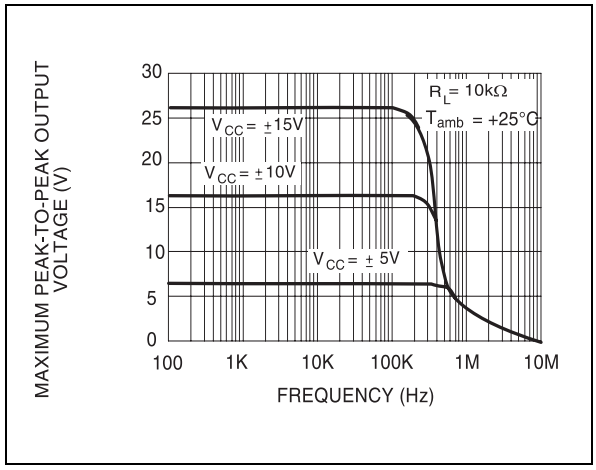
Symbol	Parameter	TL071I,M,AC,AI,AM, BC,BI,BM			TL071C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
THD	Total Harmonic Distortion (T_{amb} = +25°C, f= 1kHz, R_L = 2kΩ,C_L = 100pF, A_v = 20dB, V_o = $2V_{pp}$)		0.01			0.01		%
e_n	Equivalent Input Noise Voltage R_S = 100Ω, f = 1KHz		15			15		$\frac{nV}{\sqrt{Hz}}$
∅m	Phase Margin		45			45		degrees

1. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature.

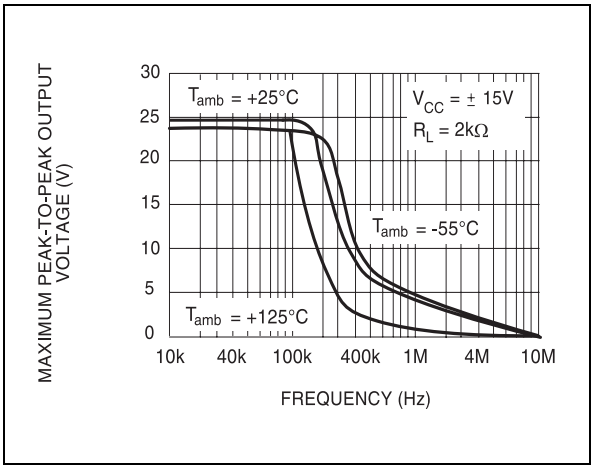
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus FREQUENCY



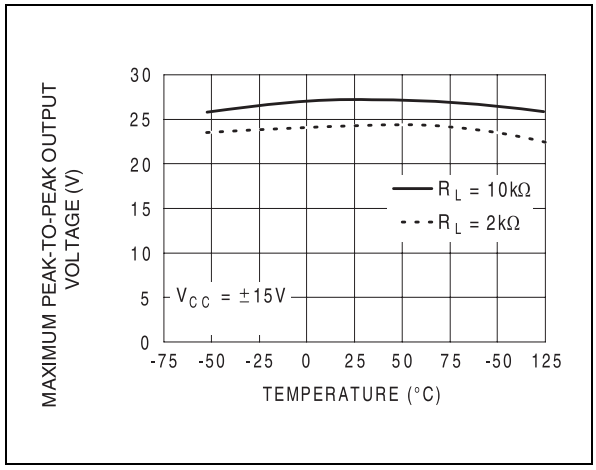
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus FREQUENCY



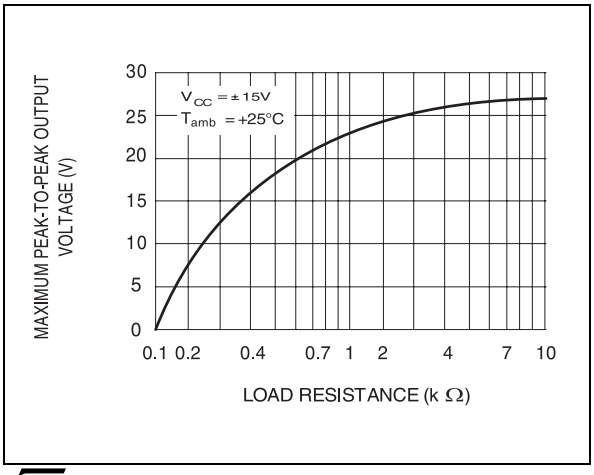
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus FREQUENCY



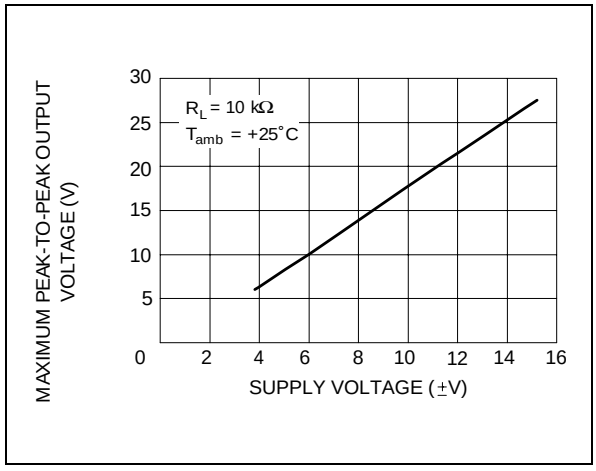
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus FREE AIR TEMP.



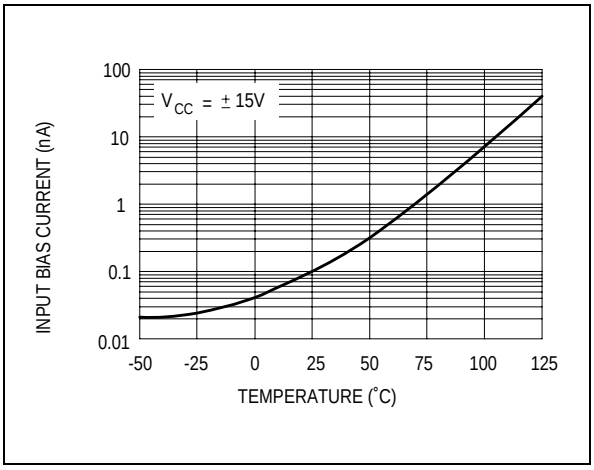
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus LOAD RESISTANCE



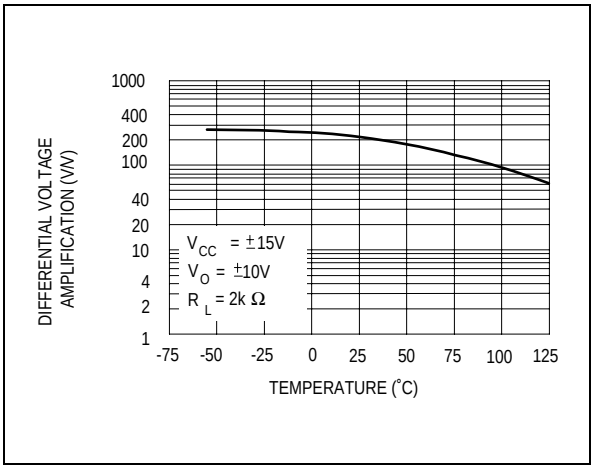
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus SUPPLY VOLTAGE



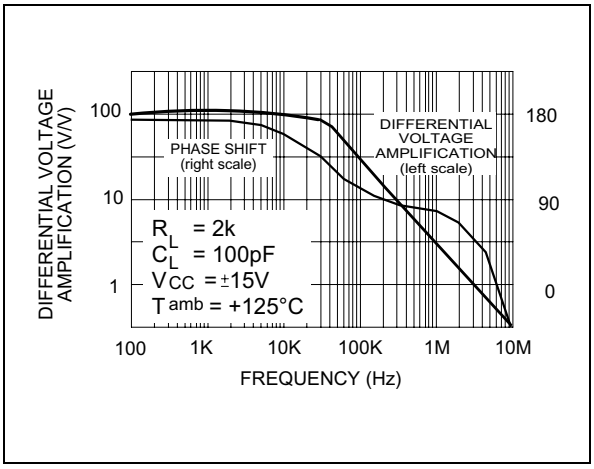
INPUT BIAS CURRENT versus FREE AIR TEMPERATURE



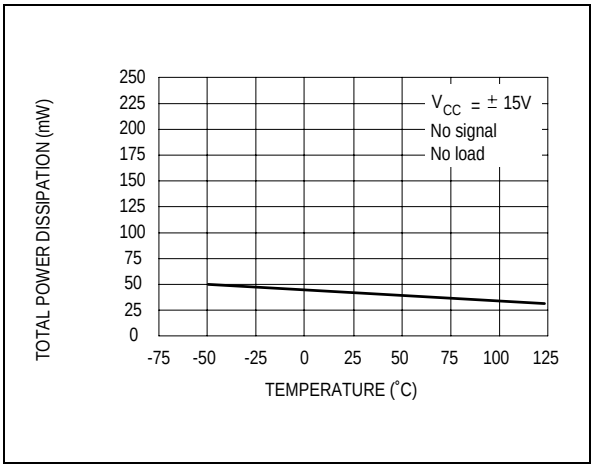
LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION versus FREE AIR TEMP.



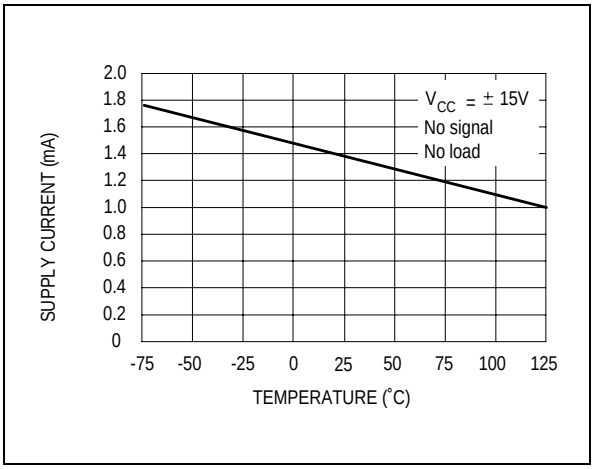
LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT versus FREQUENCY



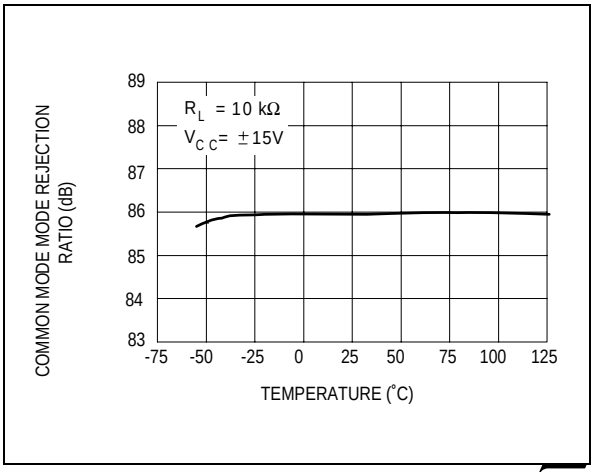
TOTAL POWER DISSIPATION versus FREE AIR TEMPERATURE



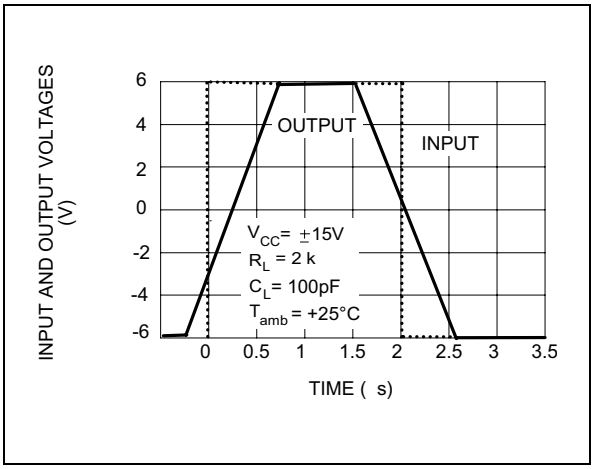
SUPPLY CURRENT PER AMPLIFIER versus FREE AIR TEMPERATURE



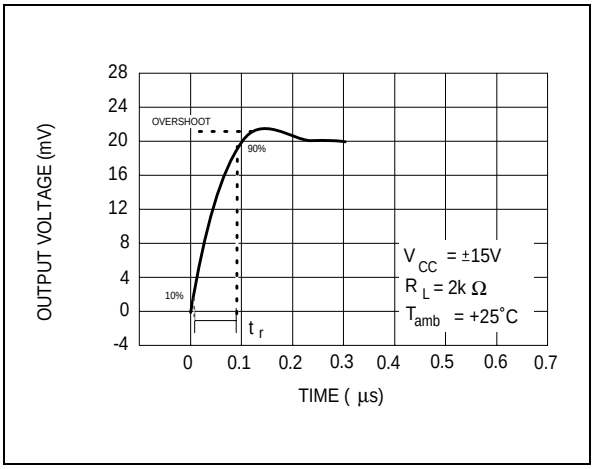
COMMON MODE REJECTION RATIO versus FREE AIR TEMPERATURE



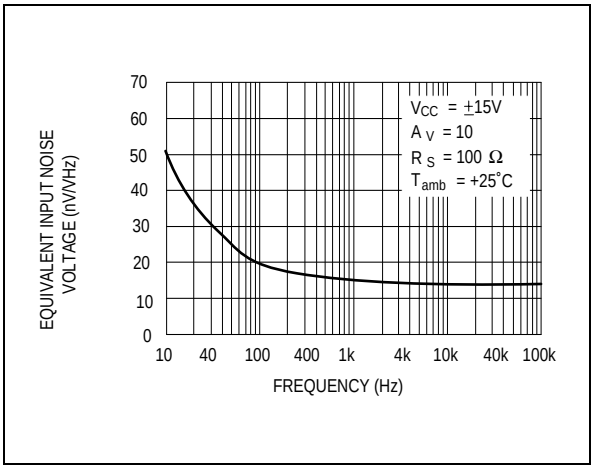
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



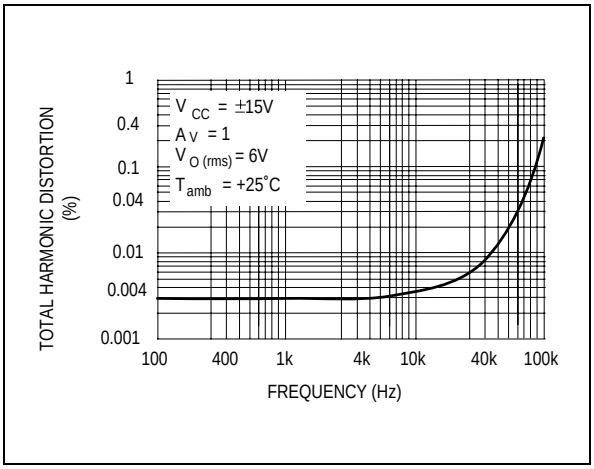
OUTPUT VOLTAGE versus ELAPSED TIME



EQUIVALENT INPUT NOISE VOLTAGE versus FREQUENCY



TOTAL HARMONIC DISTORTION versus FREQUENCY



PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage Follower

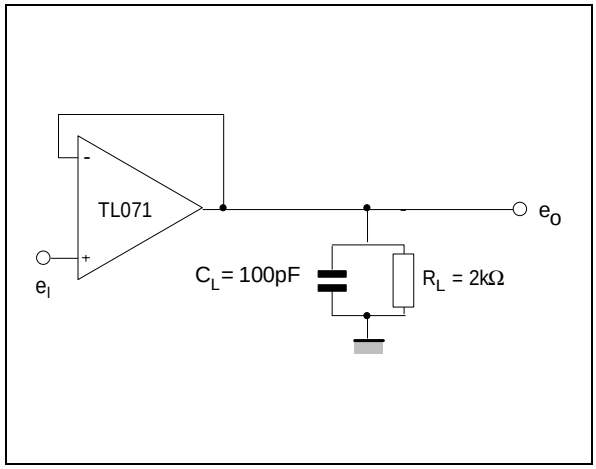
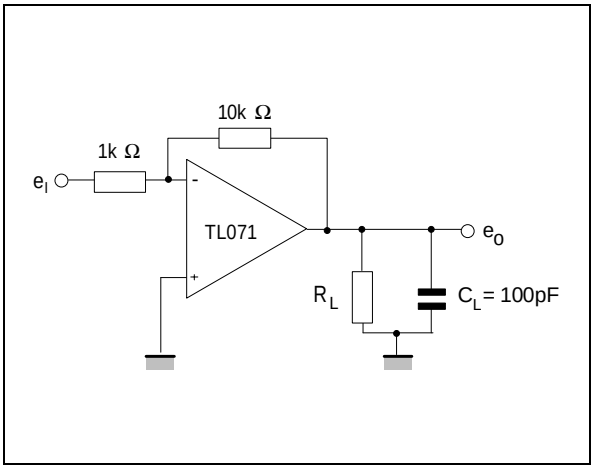
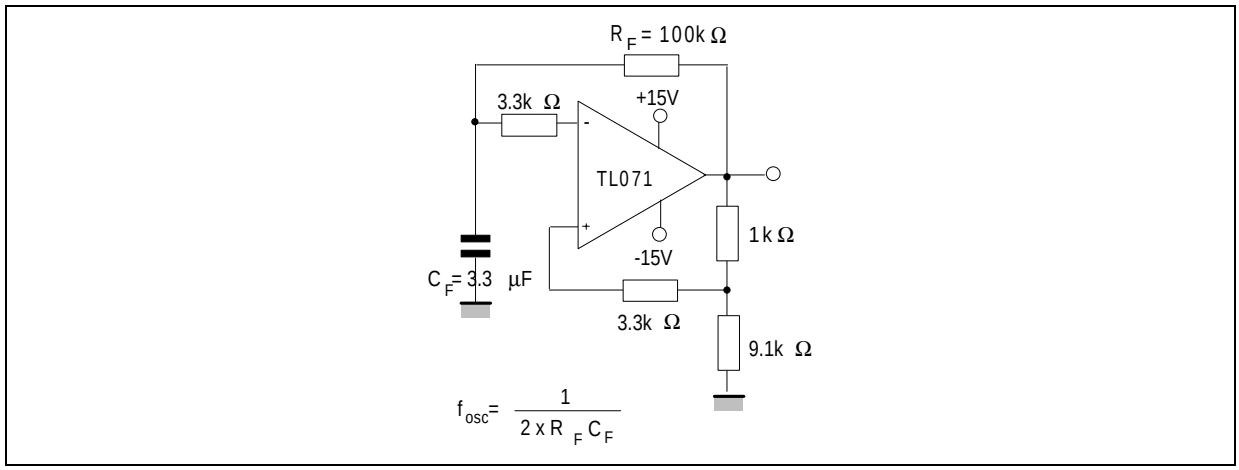


Figure 2 : Gain-of-10 Inverting Amplifier

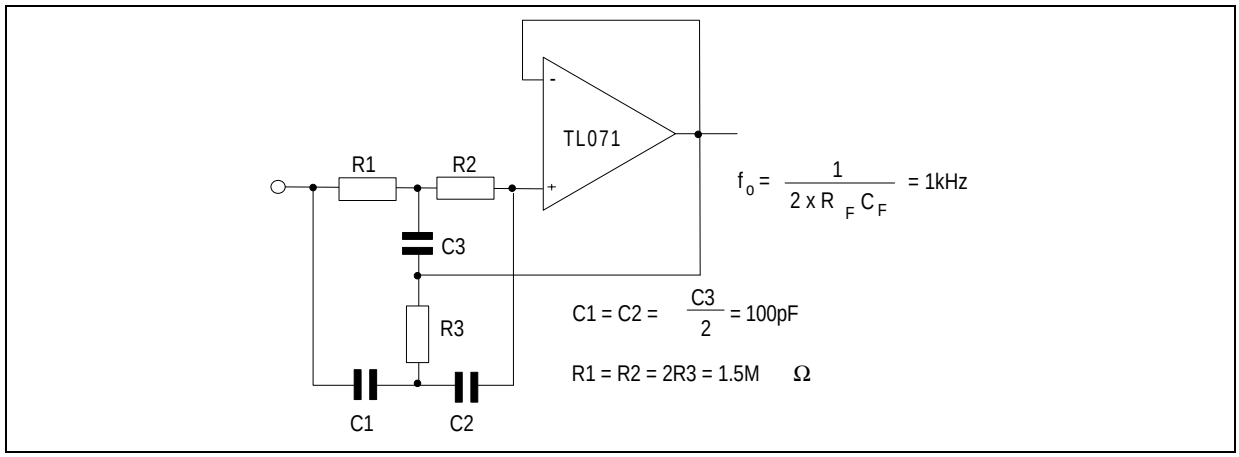


TYPICAL APPLICATIONS

(0.5Hz) SQUARE WAVE OSCILLATOR

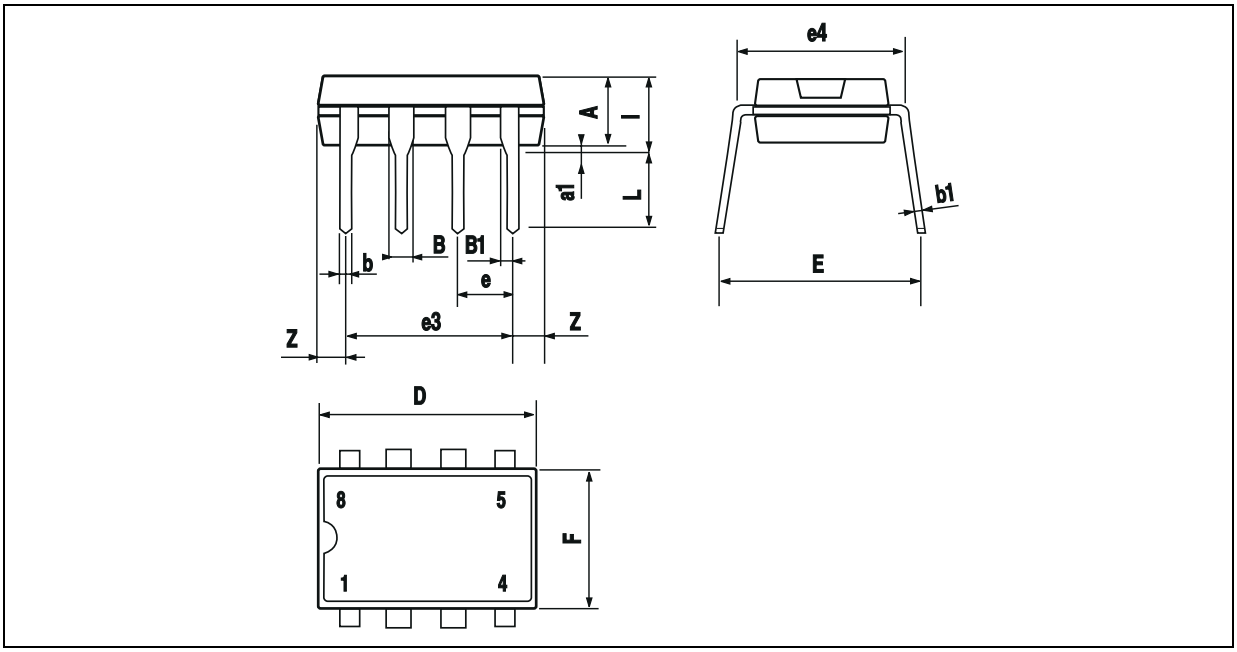


HIGH Q NOTCH FILTER



PACKAGE MECHANICAL DATA

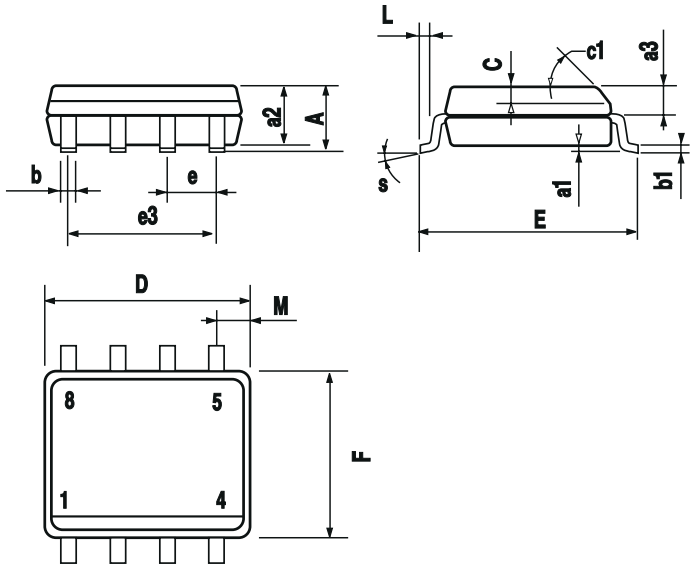
8 PINS - PLASTIC DIP



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC MICROPACKAGE (SO)



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					