# a true-frequency digital readout
## for the HW-101

## Try this simple mod
## for more precise tuning

**If you've ever operated an HW-101,** you know how frustrating it can be to try to tune it to a specific frequency; the main tuning dial simply isn't precise enough. In an effort to solve the problem, I decided to add a digital readout to my rig.

I didn't really want to *build* one; I just wanted to find an old SB-650 Digital Frequency Display, the Heathkit readout designed to accompany its HW- and SB- series equipment. But I couldn't find one for sale locally, and Heath had long ago sold out its final inventory. I decided to go ahead on my own. I tried to get a copy of the SB-650 manual, but Heath had no more.

Why this seeming obsession with the SB-650? In order to develop a reading from an HW-101, all three transceiver oscillators must be sampled and multiplexed into the counter section in proper sequence. The counting circuitry itself is more or less standard, but the multiplexing circuit is the key to success. I knew that Heath's circuit worked, and the gating and logic tables I came up with looked too unwieldy to be correct.
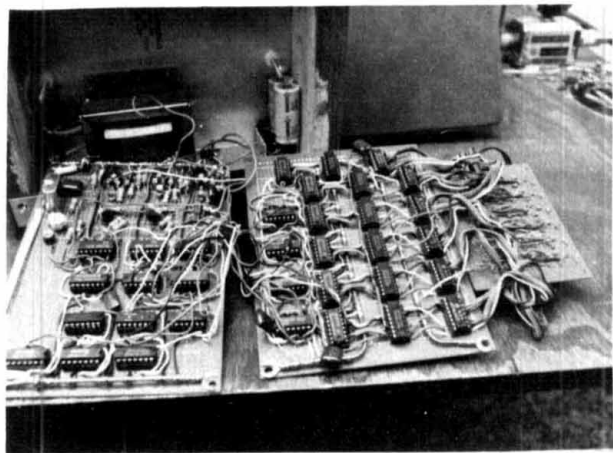


Photo A. The top, bottom, and digit boards (left to right), are shown interconnected and ready for mounting.

Although Heath couldn't provide a manual, the company did supply several schematics of the multiplexing and time chain circuitry. The multiplexing used in my readout more or less duplicates the Heath circuit.

### theory of operation

A transceiver digital readout is basically a frequency counter preceded by processing circuits that allow proper sampling of the circuits in the transceiver that determine the final operating frequency. In the HW-101 the operating frequency is determined by heterodyne action among three oscillators. The heterodyne oscillator is a high-frequency oscillator, while the carrier and VFO oscillators are relatively low in frequency. Both the carrier and VFO frequencies are essentially *subtracted* from the higher-frequency heterodyne oscillator frequency to establish the operating frequency. The processing circuitry of the readout first enters the highest frequency into the counters, then subtracts, one at a time, the other two oscillator frequencies from it. The true operating frequency is then presented to the digital display through the latches. (Although the "addition" and "subtraction" mixing takes place in different stages of the transceiver for Transmit than for Receive, the same oscillators ultimately perform the same job. Thus by tapping the oscillator outputs, the readout is accurate to within 100 Hz ± clock error, and reads the same frequency in either send or receive mode.)

### system flow

In the transceiver, samples of the three oscillators are connected by coax to phono jacks added to the back of the transceiver chassis. These are connected by 36-inch phono cables to three input phono jacks on the back of the readout chassis. (See **fig. 1** for transceiver sampling hookups.)

Each jack connects to an input stage consisting of a 40673 MOSFET preamp and a 2SC945 (or 276-2016) pulse-shaper circuit. After passing through buffer gates in U1 and being divided by four in frequency in flip-flop

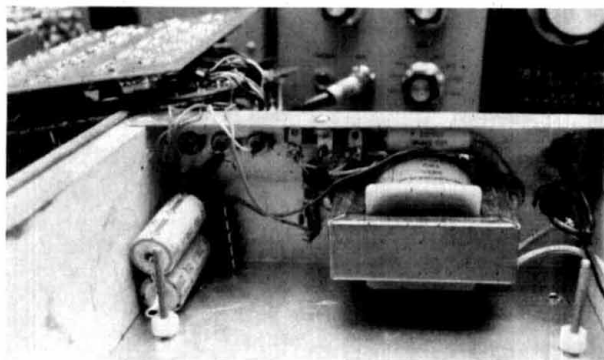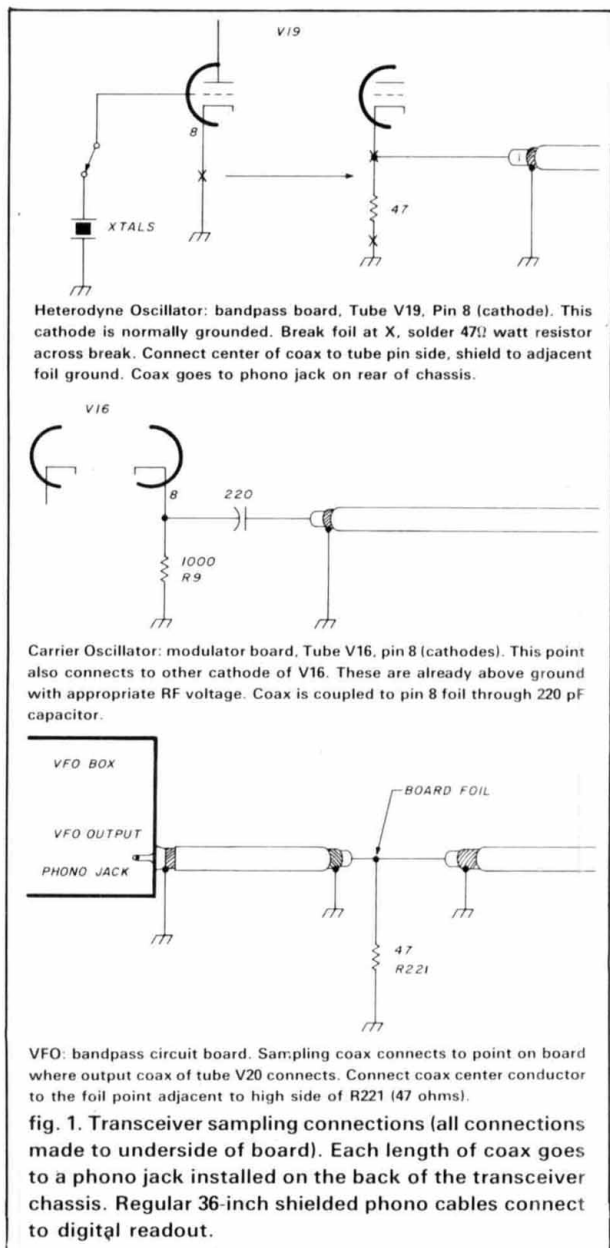**By Ed Murdoch, NU4F**, Route 1, Box 238, Omega, Georgia 31775

Heterodyne Oscillator: bandpass board, Tube V19, Pin 8 (cathode). This cathode is normally grounded. Break foil at X, solder 47Ω watt resistor across break. Connect center of coax to tube pin side, shield to adjacent foil ground. Coax goes to phono jack on rear of chassis.



Carrier Oscillator: modulator board, Tube V16, pin 8 (cathodes). This point also connects to other cathode of V16. These are already above ground with appropriate RF voltage. Coax is coupled to pin 8 foil through 220 pF capacitor.



VFO: bandpass circuit board. Sampling coax connects to point on board where output coax of tube V20 connects. Connect coax center conductor to the foil point adjacent to high side of R221 (47 ohms).

fig. 1. Transceiver sampling connections (all connections made to underside of board). Each length of coax goes to a phono jack installed on the back of the transceiver chassis. Regular 36-inch shielded phono cables connect to digital readout.



Photo B. Power supply components are mounted on rear chassis wall.

U2, these three circuits are gated sequentially into the Least Significant Digit (LSD) counter, U17, by multiplexer chips U3, U4, and U13 through U15. The gating pulses for *enable* and *inhibit* are developed from the timing chain combination of oscillator-buffer-feedback gates U5, divide-by-four flip-flop U6, and time-division decade counters U7 through U12. The reset pulses for pulse counters U17 through U22 come from U15, pin 3. The reset pulses for divide-by-four flip-flop U2 come from U16, pin 6. The transfer pulses for the latches come from U16, pin 3.

In order to feed the correct oscillator signal to the counters at the proper time, a time frame of four intervals is established. This is done by gating several combinations of outputs from U10, U11, and U12 in the timing chain. These in turn are interlocked by other gates to allow each oscillator to be counted once per frame and
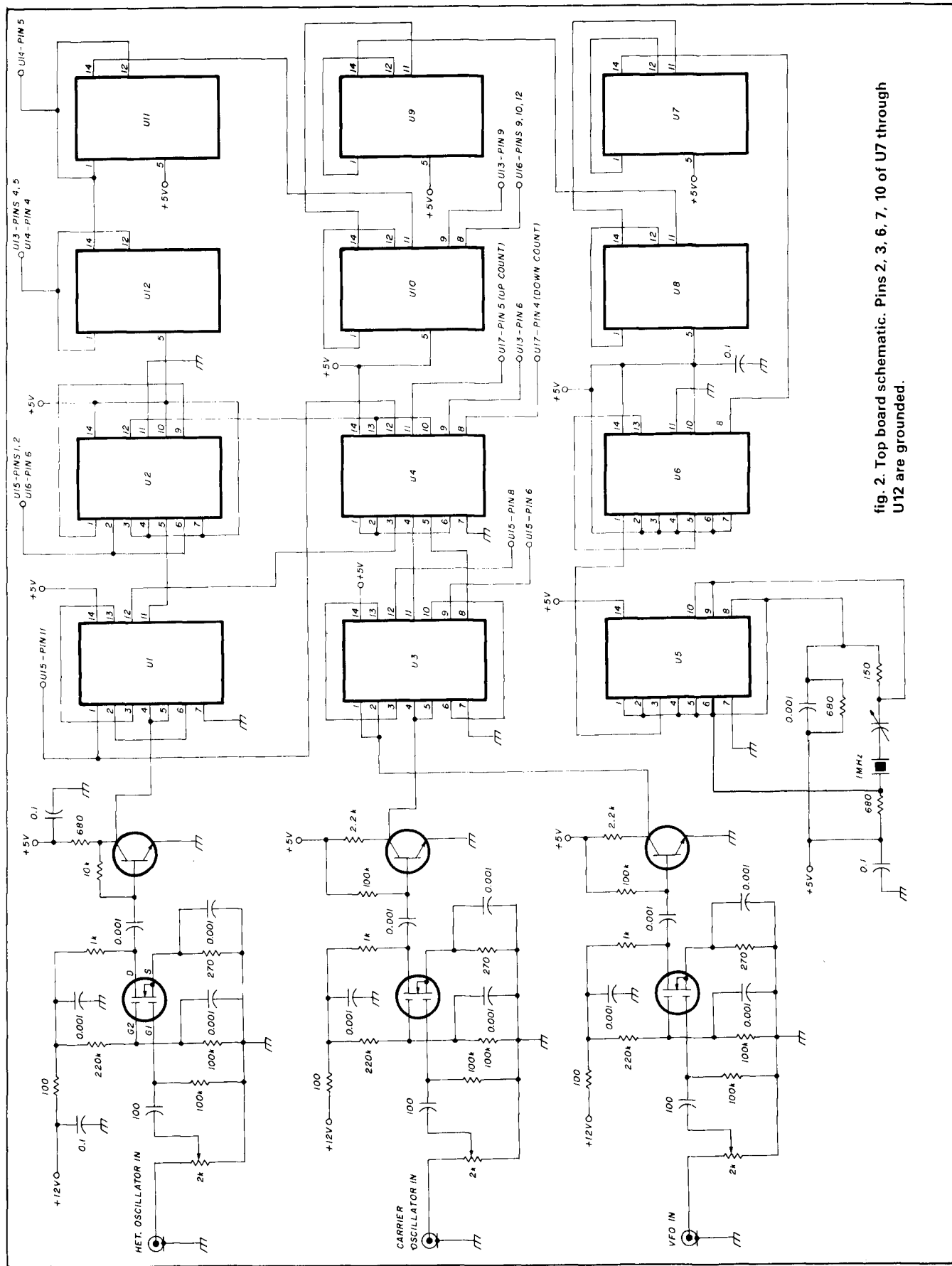
shifted to the up count (add) or the down count (subtract), as is appropriate. The fourth interval is used for pulse development by the RC network connected between U13, pin 8 and ground. After both reset pulses and the transfer pulse have been established, the next clock pulse starts the cycle again.

The counting section, which consists of a cascaded series of six 74LS192 up/down decade counters (with one counter for each display digit), provides a frequency divided-by-ten output to the following counter and its parallel output to its own digit decoder in binary-coded decimal (1-2-4-8, also referred to as ABCD in the accompanying figures). Therefore each counter has what it needs to produce the correct reading for its own LED digit, which it feeds to the digit by way of a 74LS75 latch. The divided-by-ten output is then passed on to the next counter chip, which acts in a similar fashion.

Each storage latch holds the previously transmitted number until the transfer pulse occurs, causing the latches to accept the newest measurement offered by their respective counter's ABCD outputs. Each of these "updates" is caused by a combination of reset pulses to the various flip-flops and counters so that each new count is synchronized. The latches feed the ABCD data to the input lines of their respective 74LS47 BCD to seven-segment decoder/drivers, which decode the ABCD numbers and provide the drive for the correct segments of the seven-segment display digit.

Overall synchronization is established by a master clock oscillator from which the various pulses, time intervals, and switching sequences are derived. The time occurrence of the individual gating pulses is also determined by frequency division (by divide-by-four flip-flops 74LS73, and by divide-by-ten and divide-by-two counters 74LS90). The clock frequency of 1 MHz was chosen to make frequency-division factors easily obtainable.

## construction

The circuits were planned on quad paper and then built up on two 4 1/2 x 6 5/8-inch circuit boards and one 2 3/4 x 3 3/4-inch board (**Photo A**). The two large

fig. 2. Top board schematic. Pins 2, 3, 6, 7, 10 of U7 through U12 are grounded.
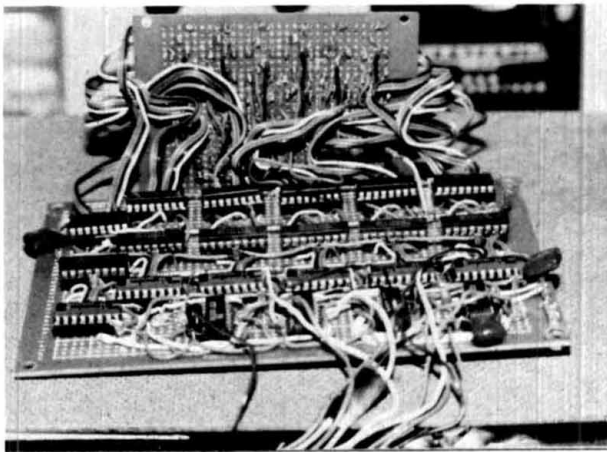
fig. 3. Bottom board schematic.

Photo D. A closer view of the bottom and digit boards illustrates interconnections.

boards are mounted upside-down in the chassis and separated by spacers. The top board contains the input wave shaping circuits, the timing chain, and part of the multiplex circuitry. The bottom board contains the remainder of the multiplex circuitry, the counters, latches, and decoder/drivers. The outputs of the decoder/drivers are cabled to their respective segment dropping resistors mounted on the third board, which also holds the digits. This board is at right angles to the other boards. A window is cut in the chassis front to accommodate the digits.

The power supply parts are mounted on the rear wall of the chassis. So are the three input jacks. Prototype wiring is shown in **Photo B**; the input wiring was later changed to coax.

## building the chassis

The first step is to determine the location of each part. Next, mark off and drill the mounting holes for the input phono jacks, the fuse holder, and front panel switch. Then drill the transformer and heat-sink-regulator mounting holes, tie-point holes, and holes in the chassis top for the circuit board bolts.

With an awl, mark guidelines for cutting the digit window. Drill holes in diagonally opposite corners of the outline to accommodate the sabre saw blade and cut the rough opening. *This is a tricky and possibly dangerous step, so I'd suggest you secure the chasiss firmly in a vise while you make the cut.* Stay slightly to the inside of the guidelines; use a small, flat file to smooth the edge of the opening to its finished size. For the window its self, I cut a piece of clear plastic (box covers are ideal) and glued it into place.

**Photo A** also shows the approximate board locations of all parts and wiring paths for the multiplexer interconnections. Other wiring shown in the remaining figures according to normal schematic drafting practice.

## the power supply

The power supply (**fig. 5**) is typical of so-called "economy" supplies in that a single secondary winding is used to develop two voltage levels. (The MOSFETs need 12 volts; the rest uses 5 volts. Both are regulated.) The transformer supplies 18 volts ac through a bridge rectifier to the filter for the 12-volt section, regulated by a 12-volt Zener diode; a center tap provides 9 volts ac to the filter of the 7805 5-volt regulator.

The power supply components, installed on the back of the chassis, are partially supported by tie points. The 7805 regulator is mounted on a standard T-220 type heat sink positioned directly against the chassis for improved heat removal. With the circuit boards in place, it's a pretty close fit; I blew out a bridge rectifier and the fuse by not watching a test probe closely enough while making tests. I have now covered exposed terminals with a tape wrap.

## circuit boards

The digit display board (**fig. 4** and **Photo C**) contains the six LED digits, sockets, and 42 1/2-watt 330-ohm dropping resistors — one resistor per digit segment. This board should be wired first. Note that this is the only place wire-wrap sockets are used. This is because I planned to support the digit board against the chassis front by its cable pressure and put several turns on each pin for extra stability. I made a seven-wire color-coded combination for each digit: a four-wire section plus a three-wire section.

After making all cable solder connections, cut off all

the pins except the 5-volt supply pins to about 1/4 inch, leave these longer (about 1/2 inch) so that the 5-volt bus can be run straight across.

There are no grounds on the digit board. Each segment "grounds" through its driver connection when activated; these are common anode devices.

The two decimal point positions are grounded through 330-ohm resistors over to the front ground bus on the bottom board. These decimal points divide the six digits into MHz and KHz separations.

## the bottom board

The bottom board contains multiplexer chips U13 through U16, decade counters U17 through U22, latches U23-U28, and decoder/driver chips U29 through U34, plus sockets (**Photo D**).

You'll have to offset three chips to fit all the parts on the board, but this poses no problem. In fact, it actually helps; because the column of offset chips represents the most-significant-digit position, you'll have a handy reference point to which you can refer as you add parts to the board.

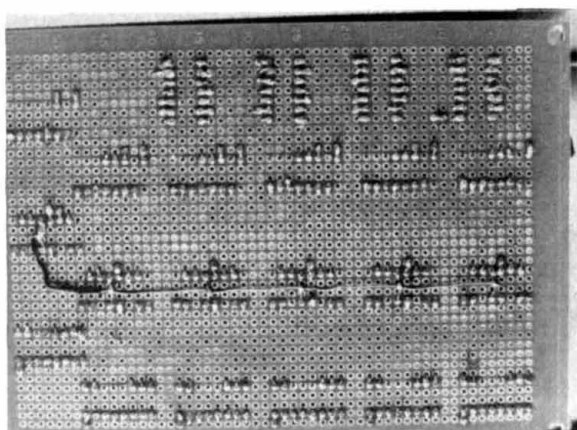**Photo E** shows the location of the two ground buses,



Photo E. Rear view of bottom board shows closeness of solder points and bus for latches that transfer pulse feed.
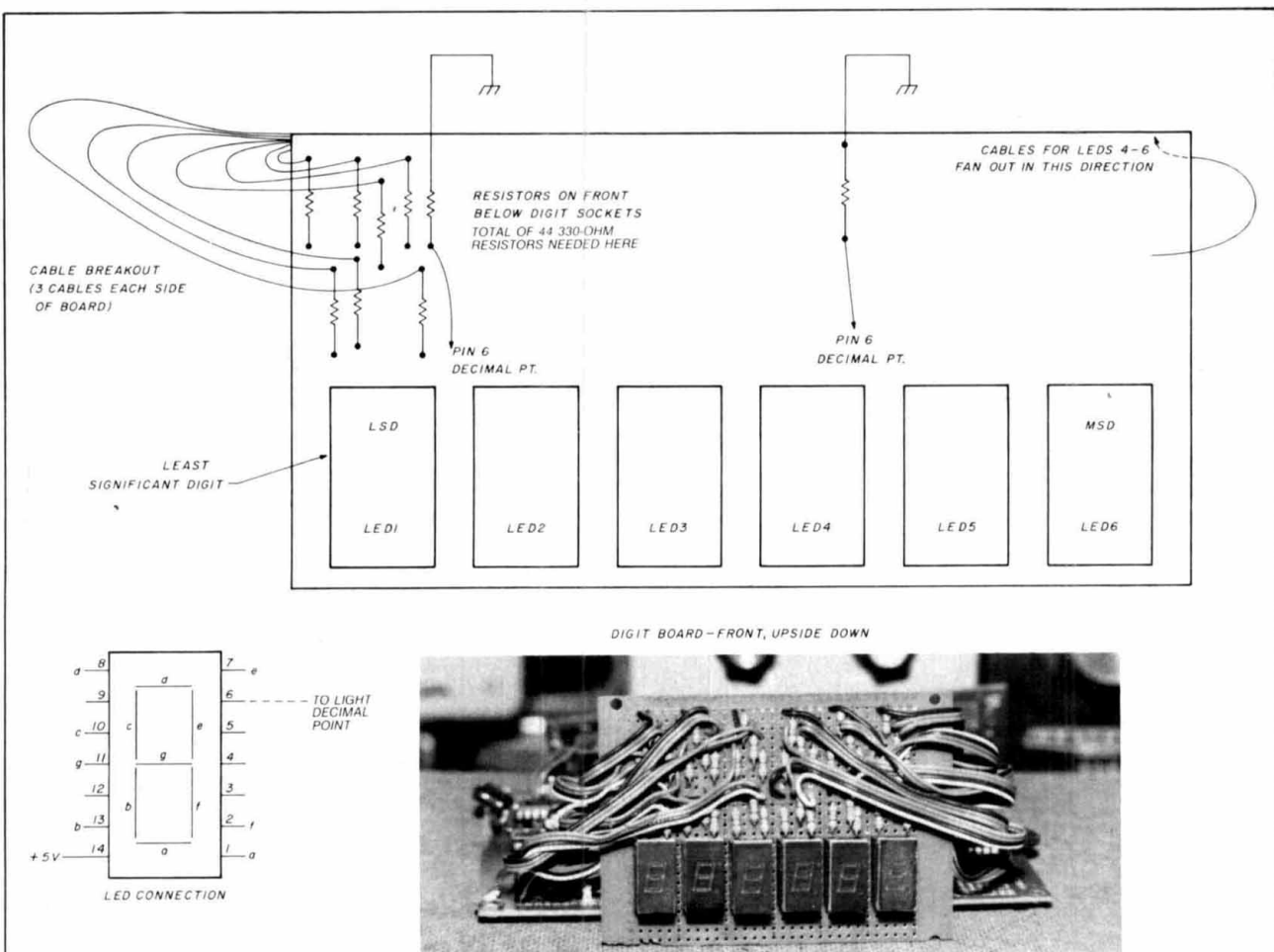


fig. 4. Digit board. Outputs of decoder/drivers are cabled to their respective segment dropping resistors. One cable section per digit goes to corresponding decoder on bottom board. Seven 330-ohm resistors per digit — except for LEDs No. 1 and No. 4, which have a resistor going from pin 6 to ground.
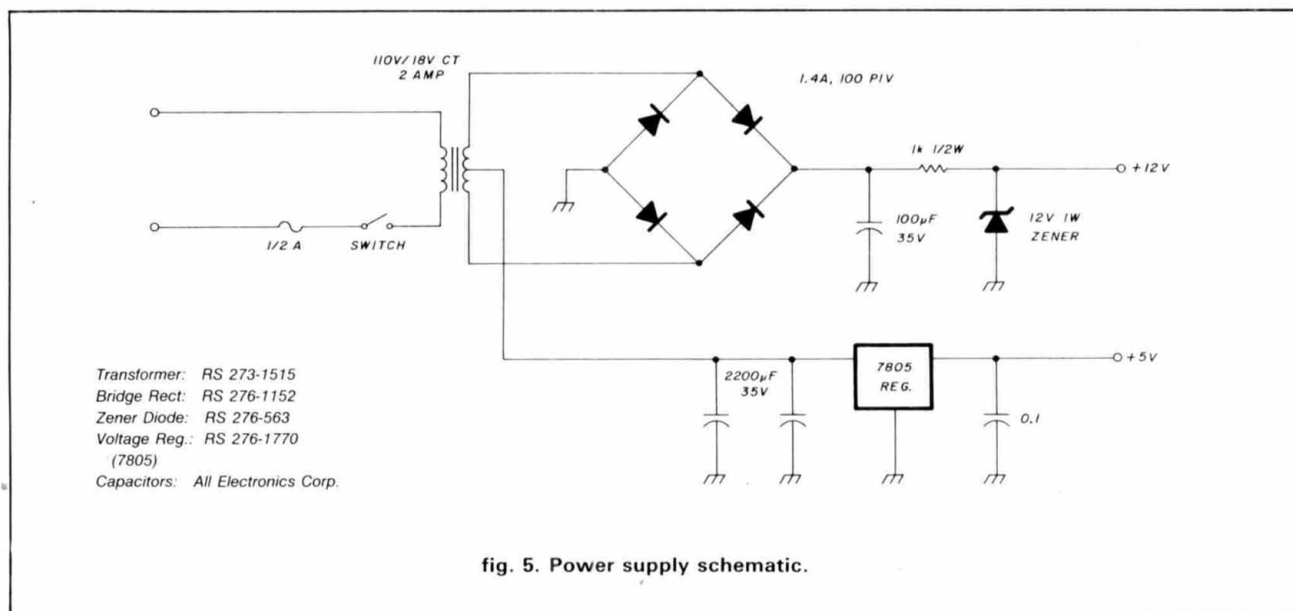
fig. 5. Power supply schematic.

Transformer: RS 273-1515
Bridge Rect: RS 276-1152
Zener Diode: RS 276-563
Voltage Reg.: RS 276-1770
    (7805)
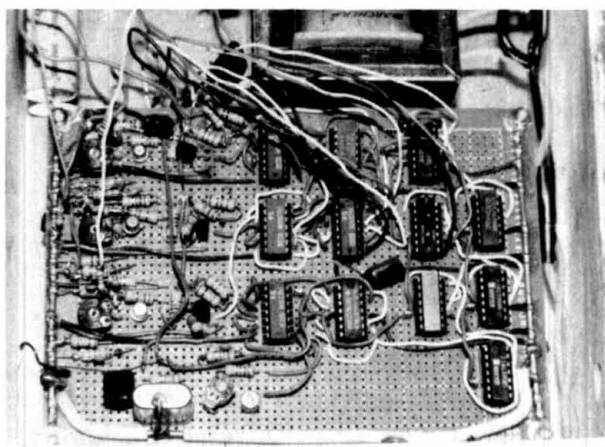Capacitors: All Electronics Corp.



Photo F. Clock oscillator has prominent location in lower left corner of top board view.

made from No. 12 wire and secured by lugs to the board mounting bolts. (While not an ideal ground, it works.) The photo also illustrates the closeness of the solder points on the pins. This was the part of the whole project that most concerned me. I tried to cut each wire so that after inserting it through the top of the board there would be just the right amount of bare wire left to bend over flat against the pin and spin around with a wiring tool so that no further wire cutting would be necessary. I'd crimp it slightly with my long-nose pliers to assure a tight fit and then solder very carefully. In the counter section of the board I soldered corresponding wires or corresponding cabled ABCD data runs. Then I verified both continuity and the absence of adjacent pin shorts before continuing. This approach paid off. I found two adjacent pin shorts and one cold solder joint that I fixed immediately, saving years of anguish. As I went along I also

aligned any bent pins.

In this same photo you can see a bus running under the center line of the latch sockets. This bus carries the transfer pulse to pins 4 and 13 of each latch, which are connected together on the bottom of the board (shown by dotted lines in **fig. X**). There simply wasn't room for this run on the top side.

Because the local Radio Shack was out of small 0.1-pF tantalum capacitors, I used their larger, standard PC-type for transient bypass and fitted them as best I could.

Most of the wiring of the multiplexer chips — on both bottom board and top board — is in the form of interconnection of gates in the same chip or in other multiplexer chips. On the bottom board I started at pin 1 on the top left side of chip U13 and went numerically pin-by-pin, finishing out each chip before going to the next. I made a color-coded tabulation of the off-board wires, leaving these about six inches long for later connection to the top board.

## top board

The top board (**fig. 2** and **Photo F**) contains the input preamp/pulse-shaper circuits, the clock oscillator U5, and associated time-division chips U6 through U12, as well as multiplexer chips U1 through U4.

Friends, I didn't know how many of life's simple pleasures I'd missed until I started working on the top board. As with the other board, I determined the layout on a board-size piece of quad paper. In an attempt to keep the input wires short, I crowded the preamp stages. Besides giving the whole thing the look of last year's campfire, it began to look as if I might have an interstage coupling problem on my hands. Actually, the only place such coupling ever did occur was between the wires from the input jacks. After I no longer had to remove the top board for anything, I changed these to coax.

I installed the 40673 preamp and 2SC945 pulse shaper circuits first, using 1/8-watt trim pots as the input impedance for each preamp, but I just tacked on the wires from the input jacks. I expected to have to experiment with the resistance to get it in the right range for the input circuits. (The samples from the transceiver have to develop a voltage across a load at their respective input stages to apply to the MOSFET gate inputs. There is a limit as to the amount of current flow through this load. The optimum resistance worked out to be about 2 k (which is the input impedance listed on the spec sheet for the SB-650).

Radio Shack couldn't help with 2-k pots, so I replaced the original 1-k units with 5-k, 1/2-watt trim pots, paralleled with a 3.3-k resistor under the board. This arrangement works perfectly. (**Figure 4** shows only a 2-k variable resistance.)

Though the 40673 **MOSFET** circuit is similar to that used in the SB-650, I first saw it in an article in *QST*.[1] The crystal clock oscillator design was also taken from this article.

The components of the 2SC945 pulse-shaping circuits were determined by experiment because I couldn't find any characteristics curves to determine the proper parameters for saturation.

Rather than worry about socket contact resistance and corrosion, I direct-wired the transistors. To minimize the danger of static blowout of the MOSFETs, I borrowed a dc-operated isolation-type iron from Bobby Hobby, KA4DPF, the friend who took the photo for this article.

Next I wired the clock oscillator, which was almost a vacation by comparison. I then mounted all the sockets for the IC chips. I wired miltiplexer chips U1 through U4 and the oscillator chip, U5, first. I followed the same wiring scheme on this multiplexer section as on the bottom board (starting at pin 1, upper left, etc.).

Then I wired time-division chips U6 through U12. Except for the divide-by-four flip-flop U6, the wiring almost duplicates itself from chip to chip. Chips U7 through U12 require that pins 2, 3, 6, 7, and 10 all be grounded. To prevent chaos, I first connected these pins on each chip together on the underside of the board, then connected them to a ground bus. I had to use a little spaghetti here and there to avoid other pins.

## final assembly

Connecting the digit board to the bottom board is the first step in the final assembly.

**Figure 4** shows a section of seven-conductor cable going to each digit resistor area. The cable is split into two sections each to allow for more flexibility in positioning the board against the window. Using the color coding of the various wires, I tabulated a wiring plan that made it quick and easy to connect the cable ends to the proper pins on the decoder/driver sockets. When I first planned this arrangement I was concerned that the digit board might not be secure enough without direct mounting on the chassis. Not to worry — you couldn't knock it loose with a baseball bat. Finally I connected those almost-forgotten off-board wires from the bottom board to their top-board destinations.

The main boards are mounted on four 1 1/2-inch, 6/32 bolts protruding downward from the top of the chassis (viewed in normal operating position). A 3/8-inch nylon spacer on each bolt separates the chassis from the bottom board, which is secured with washers and nuts. (The ground lead from the 2200 $\mu$F filter combination connects to a lug at the nearest bolt.) Three-quarter-inch aluminum spacers on the bolts support the top board, which is secured by nuts. Lugs carrying the top board ground buses go under these nuts.

## adjustments and calibration

Proper sampling levels are adjusted by placing the transceiver on the 29.5-MHz band, in the receive mode, and adjusting the three input trim pots to just slightly more than the level needed to cause a 29.5$^5$ MHz reading to lock on the display.

First I adjusted the 1-MHz clock oscillator trimmer to zero beat with WWV, using a portable receiver loosely coupled to the oscillator gate section by an insulated wire wrapped around the receiver's telescope antenna. Even with the economy-type trimmer the frequency stays within a few Hz after several hours of warmup, varying no more than about 100 Hz after 24 hours of continuous operation.

With the trim pots set at minimum, I switched the transceiver to the 29-MHz range; the heterodyne oscillator is at its highest frequency here, and losses through the sampling circuitry are greatest. (In other words, if it works here it should work anywhere.) At this point the display read all zeros, as was appropriate. Then I advanced the heterodyne oscillator trim pot until a firm reading in the region of 38 MHz was showing (this is the frequency of the heterodyne oscillator crystal on this band).

Then I adjusted the carrier oscillator trim pot for a marked drop in frequency reading, to about 34 + MHz; I adjusted the VFO trim pot for a further drop to 29 + MHz. I advanced each trim pot slightly and closed up the chassis.

Naturally the first thing I did was to tune down to 7335.0 USB. As I brought up the audio gain, I heard, with perfect clarity, "This is CHU, Canada. The time is . . ." — one of the sweetest sounds I have ever heard.

This readout can be adapted to some other rigs. By using the heterodyne oscillator input only, it can be used for low-voltage level frequency counting, with 100-Hz resolution.

If you have any questions, write (please enclose SASE) and I'll try to help.

## reference

1. Philip S. Rand, W1DBM, "The BEEPER: An Audible Frequency Readout for the Blind Amateur," *QST*, September, 1983, page 19.

**ham radio**

shown in *The Nautical Almanac* with the tabular method described in reference 9. For example, if the moon's position was at GHA 66 degrees with a north declination of 18 degrees, 26.5 minutes, we knew it would appear directly overhead in San Juan, Puerto Rico. This was a tedious procedure; sometimes we'd goof, but that was part of the challenge on EME communications.

Later some fortunate EMEers with access to large mainframe computers and moon orbital prediction programs could print out a year's worth of data showing the *local azimuth and elevation* angles of the moon every 10 or 15 minutes of the day. With personal computers, that's changed; accurate moon position programs are now available even for the least expensive PCs. One of the most popular is the one written by Lance Collister, WA1JXN. Just input your latitude and longitude and the program displays or prints out your *local azimuth and elevation* to the moon as well as the GHA, declination, and right ascension for any day, time, or increment of time desired.* **Figure 3** shows a sample printout; other output data shown will be discussed shortly.

### the EME window

For successful EME echoes, the moon must be above your horizon. You don't actually have to be able to *see the moon* for successful EME operation; you just have to be sure that you'd be able to see it if the skies were clear. The moon isn't usually visible to the naked eye — especially in daylight — when it's within one to two days of its new moon phase, but this may still be acceptable for EME operation.

Most EMEers know their local antenna azimuth and elevation limits based on the size of the antenna structure and any local obstructions. They translate these local parameters into GHA and declination limits. If you have a few different days of EME printout,
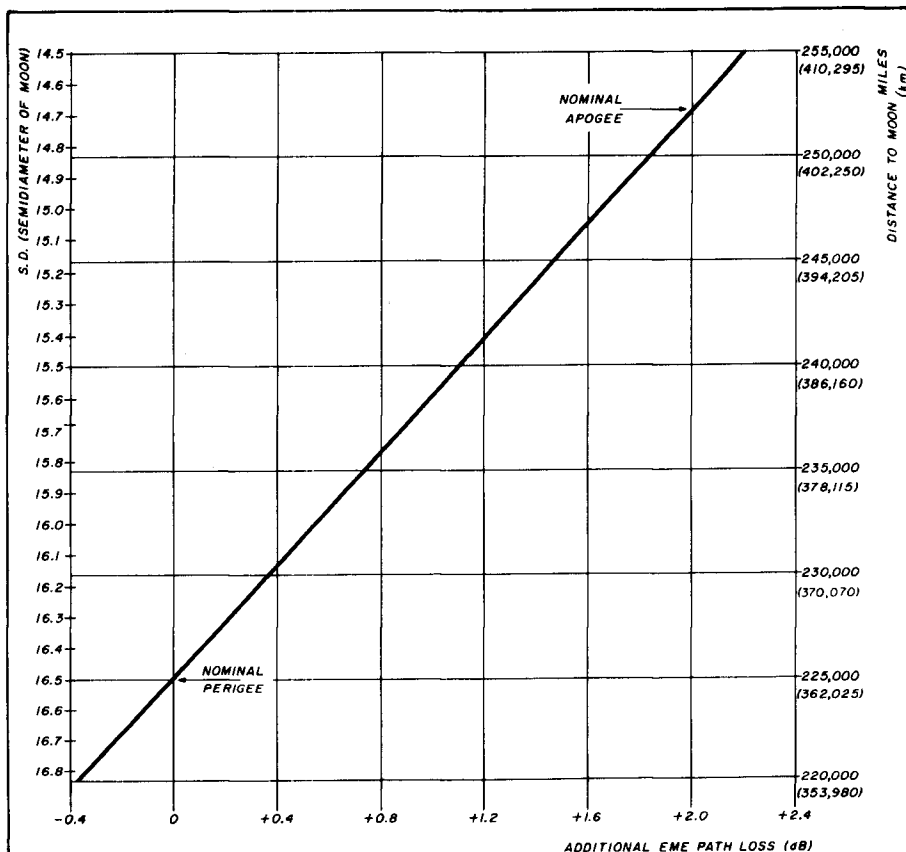
fig. 2. This graph shows the variations in EME path loss versus the distance to the moon. S.D. is the semidiameter, as explained in the text. To find additional attentuation to the moon, draw a line horizontally from either the S.D. or distance side to the pivot line and drop down to the additional path loss.

typically one at maximum northerly, one at maximum southerly, and another at zero moon declination, you can easily determine your EME window. Then it's just a simple matter of comparing your window with the window of the station you want to reach to see whether you have a *common window* at the desired schedule time. If you do, contacts at distances greater than 10 to 11,000 miles (16 to 18,000 km) are possible.

When 2-meter EME operation took off in the early 1970s, there were many stations using large tropo antenna arrays that were rotatable only in azimuth. Therefore, they could operate EME only when the moon was low on the horizon — usually referred to as a *rising or setting moon* — typically below 10 degrees of elevation.

This concept was further expanded and standardized by Bob Sutherland,

## short circuits
## HW-101 readout

In **fig. 2** (top board schematic) of NU4F's article, "A True-Frequency Digital Readout for the HW 101" (January, 1987, page 8), the connection between the 600-ohm resistor and the 1.0-MHz timing crystal, which goes to pin 6, U5, is also shown connected to the run from pins 1, 2, 4, 5, and 8. This connection should go only to pin 6, U5.

U13 through U16 were omitted from the parts list on page 12; these are 74LS00 Quad NAND gates.

## 2-meter Yagi

In **fig. 2** of W1JR's May column (see page 95), the spacing of the first director is shown as 26 7/8 inches. This should have been indicated as 26 7/16 inches. According to the author, this discrepancy would probably not affect performance.