XLS 3U SERIES
CIRCUIT DESCRIPTION AND SERVICE NOTES

INTRODUCTION

These notes are intended to assist maintenance and service of the XLS 3-rack-space family of amplifiers. Please refer to the relevant schematic diagrams and system diagram while reading this document.

The component references of the two amplifier channel electronics are appended "A" and "B" respectively. Shared circuitry (such as that of the protection system) has no suffix. This document will refer to channel A references only. Operation of channel B is identical except where explicitly noted. Voltage values in bold mentioned in the text are test voltages which may be used for diagnostic purposes. Please read the surrounding text which explains circuit operation and may qualify such measurements.

MECHANICAL CONSTRUCTION

The mechanical structure of the amplifier comprises three main components: chassis, front panel and cover.

The one-piece chassis incorporates rear panel, side panels, bottom cover and transformer mount.

The main PCB is fixed to the chassis using 4 M4x16 screws with insulating washers through the main heatsinks and 4 M4x8 screws for the edges of the board, one of which connects the chassis electrically to 0V on the PCB.

There are two heatsinks secured to the board with 3x No6 / 5/16" pozi pan 'B' point self tapping screws and 3x M3.5 shakeproof washers each. Output devices are bare mounted (with zinc oxide heatsink paste) to the heat-sinks with 2x No6 / 5/16" pozi pan 'B' point self tapping screws each. CAUTION: The heatsinks are LIVE at up to +95VDC on one AND -95VDC on the other.

The plugable input module and output module are secured using 4x No4 / 8 plastite screws and 4x M3 / 8 screws respectively.

The mechanical integrity of the amplifier is realised when the substantial frontpanel is fitted using 4x M4 /10 Flange Pozi Black screws at the sides and 2x M4 nuts behind the front. The cover is secured using 6x #8 / 3/8" Flange Pozi Black self tapping screws.

All internal wiring is plugable to allow quick removal of main PCB for repairs and servicing.

CIRCUIT DESCRIPTION

Input Stage

The input stage is built around one half of a TL072 dual operational amplifier, IC1A on the input board, configured as a unity-gain differential amplifier. Its correct operation depends on both of its input terminals being correctly terminated and, therefore, any gain errors around this stage may be a result of a faulty cable termination within the mating XLR connectors. There is no provision for trimming Common-Mode Rejection (CMR) but checking this can easily eliminate the input stage in the search for a fault.

CMR checkout procedure is as follows :

Inject a common-mode test signal at 1kHz and +4dBu to the channel under test. The common-mode test signal of the Audio Precision test system is suitable, otherwise connect the signal to both pins 2 & 3 via 56 Ohm or 47 Ohm resistors. Observe the amplifier output (with level control at maximum) which should be less than -9dBu.

Power for the input stage is derived from the main +HT and -HT supplies via 1W resistors R24 and R25 and shunt regulated to a nominal +18V, -18V by ZD3 and ZD4 respectively, all located on the main PCB. The output of the input differential amplifier is fed via DC blocking capacitor C7A and 100R “Build-out" resistor R10A to pin 5 of Header 2 (channel B - pin 2 of Header 3) and then exits the input board.

If LK1,2,3,4 are present and intact then the signal travels back onto the input board via pin 4 of Header 2 (channel B - pin 5 of Header 3).

Sub-Sonic filter and Clip Limiter

The Sub-Sonic filter is based around the other half of the TL072 dual operational amplifier, IC1A on the input board, configured as a Sallen & Key unity gain 2nd order Butterworth high pass filter. The two-pole three-position switch, SW1A, selects the following -3dB cutoff frequencies:
1) 30Hz: only C8A and C10A connected;
2) 15Hz: C11A and C12A connected in parallel with C8A and C10A respectively;
3) Off position: C14A bypassing C8A and C10A.

Limiter switch SW2 in its OFF position shorts R2A and disconnects LDR1A to turn the Clip Limiter off. In its ON position, SW2 connects R2A and LDR1A as a light-dependent voltage divider, controlling the level of the input signal. LDR1A faces LED2A, which is lit when the amplifier reaches about 1dB below clip (at the same time as the clip LED at the front). Because the resistance of LDR1A reduces as its cell area is illuminated, pushing the amplifier into clip will, therefore, cause the input signal to be reduced at the R2A -LDR1A divider. Thus the amplifier is Clip Limited.

The output of the filtering/limiting op-amp is AC coupled by C13A and built out by R11A, and continues to pin 3 of Header 2 (ch. B pin 4 of Header 3), at which point it re-enters the main board and makes its way to pin 1 of CN2A, a three-pin header making connection by wire to the level potentiometers: pin 1 is Top, pin 2 is Wiper, pin 3 is Bottom. The signal emerges from pin 2 and is fed to the input of the Power Amplifier.

POWER AMPLIFIER

The power amplifier consists of a fairly conventional Class A driver stage driving a Class AB bipolar output stage. Each stage will be dealt with individually.

Class A Driver

The input signal returned from the level control is fed via DC blocking capacitor C7A and R8A. DC bias current for the Class A input stage is supplied via R9A, while 33pF capacitor C54A prevents any extreme high frequency input signals from reaching the power amplifier and also provides a low source impedance at high frequencies to ensure frequency stability.

The first stage of the class A driver consists of Q1A and Q2A configured as a long-tailed pair differential

amplifier. Emitter resistors R10A and R11A de-sensitise the performance of the input stage to parameter variations of the two input transistors. The quiescent current for the input stage is delivered by current source Q3A. Diodes D1A and D2A provide a reference voltage of approximately 1.2V, which is applied to the base of Q3A. Approximately half of this (0.6V) will then appear across R13A (220R), which then sets the current, sourced from Q3A collector at approximately 2.7mA. In the quiescent state half of this current is driven through Q1A and Q2A. Hence the voltage dropped across emitter resistors R10A and R11A will be approximately equal at 135mV.

Overall voltage feedback of the amplifier is derived through R18A and R17A. R57A and C20A provide local feedback around the Class A section only to define the dominant pole of the amplifier. C56A connected in series with R66A gives 100% DC feedback to minimize any DC offset at the output. The reulting feedback signal is applied to the base of TR53A.

The collector currents of Q1A and Q2A are fed via D3A and D4A to R15A and R16A respectively. Hence, in the quiescent state, R15A and R16A should each exhibit a voltage drop of 1.35V or so.

Under normal conditions, the signals at the bases of Q1A and Q2A will be identical. However, under fault conditions, such as a DC offset at the output, the base voltages will become offset also. For example, in the event of a large DC offset of +50V at the output, a positive DC voltage will appear at the feedback point and hence at the base of Q2A. Although this would, in theory, be the full +50V, owing to C11A being rated at only 25V, the voltage will, in practice, be somewhat lower. However, the important issue is that the voltage is positive. In the event the voltage is negative this indicates that the feedback network is faulty (most likely R18A itself).

The voltage at Q2A base being positive while the base of Q1A is close to 0V will then reverse bias Q2A base-emitter hence turning off the transistor. Hence, no voltage should appear across R11A and R16A while double the normal voltage will appear across R10A and R15A (270mV and 2.7V respectively). Should this not be the case, it indicates a fault in the input stage itself.

The output of the input long-tailed-pair (i.e. the voltages at the anodes of D3A and D4A) are fed to a second long-tailed pair Q4A and Q5A. The bias current for this stage is set by resistor R19A thus: D3A drops approximately the same voltage as the base-emitter junction of Q4A; the same can be said of D4A and the base-emitter junction of Q4A; therefore the voltage across R19A is approximately equal to the voltage across R15A and/or R16A, i.e. 1.35V. This sets a current of about 6.75mA split between Q4A and Q5A. C12A and C13A provide a little Miller Feedback around Q4A and Q5A respectively. These capacitors can be important to the stability of the amplifier but do not define the dominant pole. It should also be noted that either of these capacitors becoming "leaky" (difficult to measure in circuit) will result in a DC offset at the output.

The collector of Q5A drives the output stage in conjunction with the collector of Q7A while the collector of Q4A drives current mirror Q6A/Q7A via R20A. In the quiescent state R20A will show a voltage drop of around 67.5V, and the current mirror emitter resistors R23A R24A and will show equal voltage drops of 160mV. Hence, for the same +50V DC offset, described earlier, one would expect no voltage drop across any of R20A, R23A or R24A, indicating that the feedback is attempting to correct the fault. Likewise, for a negative DC offset one would expect these voltages to be twice their usual value. If this is not the case then the second stage (Q4A-Q7A) is at fault.

The collectors of Q5A and Q7A are joined to form the output of the class A driver by the Vbe multiplier: R22A, R21A and Q8A(mounted on the heatsink), bypassed at AC by C15A, which sets the output stage

bias. The bias voltage across the Vbe multiplier should range between 2.4V (heatsink warm) and 2.5V (heatsink cold). Bias voltages outside this range indicate a fault with the Vbe multiplier and/or a fault in the second long-tailed pair (Q4A - Q5A, R19A, R20A, R23A, R24A). For example, too small a bias voltage could be caused by R19A being high, R24A being high, R21A being low, Q8A being faulty etc. Too high a bias voltage is rare, and would, most likely, be caused by a faulty transistor or resistor in the Vbe multiplier circuit.

C3A is is very important for ensuring HF Stability. A faulty capacitor in this position will usually cause excess distortion and in the case of anything less than 330pF can reveal a very spiky instability.

Power for the class A drivers is decoupled from +HT and -HT by D17, C19 and D18, C20 respectively.

Output Stage

The output stage consists of a symmetrical Siklai follower: Q9A-Q12A, R34A, R29A, R35A, R56A and C21A, generating the high current drive required for the parallel connected symmetrical follower output stage: Q13A-Q20A, R44A-R51A. V-I limiting is controlled by Q21A, Q22B, R36A-R43A, C1A, C2A, R20A, R25A-R28A, R30A, R33A, R55A, D7A-D9A, D11A, ZD3A-ZD6A.

As the output stage is symmetrical, the positive half only will be described (Q13A-Q16A, R44A-R47A, C2A, Q22A, R36A-R39A, R25A, R26A, R30A, R55A, D8A, D11A, ZD3A, ZD5A).

Output stage protection is accomplished by a three-slope V-I limiting circuit which has limiting characteristics chosen to emulate the Safe operating area of the output stage transistors at their maximum operating temperature.

The V-I limiting works by controlling Q22A: when the base-emitter voltage of Q22A exceeds about 0.65V then Q22A turns on and steals current, via D8A, from the input of the output stage and thereby limiting the output. So, V-I limiting is controlled by controlling the base-emitter voltage of Q22A.

Each output device has its own current sharing resistor -- R44A-R47A -- the voltage across which is proportional to the current flowing in the output device. These voltages are sampled and summed by R36A-R39A. C2A ensures stability when V-I limiting is activated.

The voltage across the output devices is sampled by R25A and R26A (R30A and ZD5A limit the voltage range to reduce off-load distortion) and this, summed with the output current derived signals from R36-AR39A, controls Q22A for output voltages less than about 3Vpk. Thus the amplifier is protected for short circuits because the base-emitter voltage of Q22A increases when output current increases and when voltage across the output devices increases.

For output voltages exceeding about 3Vpk, ZD3A conducts connecting R55A to sense the output voltage. In this case, as output voltage increases, the base-emitter voltage of Q22A reduces, thus the current limit is increased as the output voltage increases, defining the third slope of the limiting characteristic.

CLIP LED CIRCUIT

The clip LED (LED1A) is driven in series with the Limiter LED (LED2A) from the output of the amplifier via D13A with its threshold controlled by ZD7A and R58A. With no signal present, ZD7A and R58A generate a reference voltage at the anode of ZD7A which is 18V below the +HT supply rail. All the

current flowing through R58A comes from ZD7A. To turn the LEDs on, the amplifier is required to produce an output voltage approximately 5V above the reference, at which point ZD7A is no longer in breakdown and the current flowing through R58A comes from the output stage via D13A, LED1A and LED2A. Thus the "peak" LED threshold and the "Clip Limiter" threshold vary with the +HT voltage and thus the output loading conditions.

FAULTS IN THE OUTPUT STAGE

Output device failure usually leaves you with two or more of the Collector, Emitter, Base shorted together. Deciding which of the output devices is at fault is relatively simple. Use a desoldering tool to remove the solder from the device pins (Base and Emitter) and move the pins so that they are clear of the pads. Do this for all suspects. You can now measure each output device separately with a multimeter set on the diode tester. Remember to test for all possibilities. A good output device will measure like this:

Probe connections:

For MJ15024 (npn): red (Volts/Ohms), black (COM).
For MJ15025 (pnp): reverse the red and black probes

	Correct reading
Base > Emitter	> 500mV
Emitter > Base	Open Loop or no reading
Base > Collector	> 500mV
Collector > Base	Open Loop or no reading
Collector > Emitter	Open Loop or no reading
Emitter > Collector	Open Loop or no reading

No special selection is required when replacing output devices.

If an output device has failed, it is very likely that other parts of the output stage will also have been damaged, especially Q9A - Q12A and associated resistors/capacitors and Q21A, Q22A and other parts of the V-I limiting circuitry.

Other Causes of Apparent Output Stage Faults

Output DC offsets can be caused by faults outside of the output stage itself. In the event that no dead output devices are found, check the driver stages for correct operation. The fault-finding routine should start at the feedback point: check that the DC fault is reflected at this point. Then progress through the driver stages: check that the relevant current sources are operating correctly, and that the feedback is attempting to correct the fault.

Premature clipping may also be caused by faults not connected with output device failure. Most often the fault lies within the V-I limiting circuit. This can easily be confirmed by removing D7A and D8A from the circuit board and observing if the fault clears. Note that, counter-intuitively, a faulty D8A will show as a problem on the negative half-cycle, and a faulty D7A will show as a fault on the positive half cycle. Faults within the V-I limiting circuitry can also cause some extremely strange and gross distortion, especially off load. Note that R44A-R51A, the 'current sharing' resistors are part of the V-I limiting circuitry.

OUTPUT CONNECTIONS

The output of the amplifier is connected to Zobel Network R12A/C8A. This network presents a defined load impedance to the output stage at high frequencies to ensure stability. Either of R12A or C8A being faulty will result in the amplifier oscillating at high frequency, which may also be evidenced by mains "hum" and/or distortion at the output. This signal is fed via output choke L1A which isolates any load capacitance from the amplifier feedback to ensure stability.

The output is then fed through output relay RLY1A and on to the rear panel output connectors.

PROTECTION SYSTEM

The protection system is based around IC1, a TL074 quad op-amp.

The temperature of the heatsink is monitored by TH1, an LM35DZ temperature sensor integrated circuit producing 10mV / ^{0}C. The temperature signal is then multiplied by 10 by one op-amp (pins 8,9,10) & R16,R17. The output (pin 8) is fed directly to pins 6 & 13 serving as a temperature dependent (0.1V / ^{0}C) reference for two comparator circuits: one (pins 5, 6, 7) controls the relays and the other (pins 12, 13, 14) controls the fan speed.

The Fan can run at two speeds, the changeover happening at about 55^{0}C. R9 and ZD2 produce a reference voltage of 9.1V at the cathode of ZD2. This is divided by R18 & R19 to give about 5.5V at pin 12, the noninverting input, which is compared with the temperature signal at pin13, the inverting input.

1) Temperature signal is less than 5.5V: the output of the op-amp will be high (+24V), turning Q1 off and therefore Q2 off. The fan speed is controlled by R21 which forces approximately half speed.
2) Temperature signal is more than 5.5V: the output of the op-amp will be low (-5.6V), turning Q1 on and therefore Q2 on. R21 is now effectively shorted out by Q2 and the fan runs at full speed.

At turn-on, C16 will charge through R9 and R10 towards the 9.1V reference (ZD2). The voltage is fed to the non-inverting input (pin 5) of op-amp at pins 5,6,7 configured as a comparator with hysterisis (D9 and R11). The reference for the comparator is set by the temperature reference which is about 2.5V at room temperature (25^{0}C), When the voltage across C16 exceeds the temperature reference, the op-amp output will swing high (+24V) and turn Q3 on via current limiting resistor R13. When Q3 is on, it pulls current through the coils of RLY1 (softstart) and RLY1A, RLY1B on the output board. This also means that the collector of Q3 will swing low (close to 0V) effectively shorting out R15 and LED2 to turn LED2 (Protect, Yellow) off.

The output of each channel is fed via resistors R2 (Channel A) and R3 (Channel B) into C9. The combination of C9 with R2 and R3 forms a low-pass filter, and so at signal frequencies C9 will have no voltage across it. In the event of a DC offset appearing at the output; however, C9 will charge to a DC voltage. This voltage is limited to 3 diode drops (about 2V) by D3-D7 which also define a window comparator with R5, R6 and op-amp at pins 1,2,3. Nothing happens while the voltage across C9 is between about +1 and -1. If the voltage across C9 exceeds this then the output (Pin 1) of the comparator will swing low (-5.6V). This will discharge C16 (see previous paragraph) through D8 and thus open the RLY1, RLY1A, RLY1B and turn LED2 (Protect) on.

The network consisting of D1, D11, D12, R1, R4, C10 and C11 provides the rapid turn-off feature of the

protection system. R1 is connected via D11, D12 to the +/- 18V AC secondaries of the mains transformer. The union of D11 and D12 will have a negative going full-wave rectified version of the secondary voltage. This is averaged by C11 to a negative DC voltage, reverse biasing D2 and, therefore, has no effect on the protection system. Should the power be turned off, C11 will be rapidly charged towards the +24 rail via R4 (and D1, C10 which hold up the voltage while the supply discharges), forward biasing D2, resulting in the same action as for a DC fault in the amplifier.

POWER SUPPLY

The amplifier operates from nominal (off-load) +/- 65V (XLS 202), +/- 80V (XLS 402) or +/- 93V (XLS 602) supplies, with an auxiliary +/- 24V supply for the protection circuitry and the optional AMPSAP card. To generate the supplies, the mains transformer has one secondary with a center tap, two 18Vac taps and the usual end taps. The end tap outputs are rectified by BR1 and smoothed by C1,C3,C5,C7 to get +HT and C2,C4,C6,C8 to get -HT (note: not all of C1-C8 are installed on XLS 402 and XLS 202). The +/- 18Vac taps are rectified by D13-D16 and smoothed by C17 to get +24Vdc and C18 to get -24Vdc.

SOFT START SYSTEM

AC mains enters the board on fastons (Red, Black, Blue) and leaves for the transformer by way of connectors Main1 (220/240) and Main2 (110/120). The soft-start components include R22, PTC1, PTC2 and the contacts of RLY1. At switch-on, R22 limits surge current and PTC1, PTC2 protect R22 from overheating. After a few seconds, the protection circuit energizes RLY1 coil, closing RLY1 contacts which short out R22, PTC1, PTC2, allowing full power operation.

FAULT-FINDING HINTS

When powering-up a unit after repair, undetected faults may result in further damage when the unit is retested. To minimize the risk of damage, please follow this procedure:

1) If the unit is set to 220V/110V, lift the 'RED' faston and connect a 100W mains lamp between the RED wire and the 'RED' board mounted faston. If the unit is set to 240V/120V, lift the 'BLACK' faston and connect a 100W mains lamp between the black wire and the 'BLACK' board mounted faston.
2) Power up in the normal way. The lamp will initially glow brightly, and then dim down as the internal capacitances become charged. The unit may then be functionally tested with no load connected. Once the unit is operating correctly, the mains supply may be applied to the unit as normal, and the unit may be load tested.

In the event that the lamp does not dim down, this indicates that a major fault still exists, which must be remedied before full mains may be applied.

LOCATING MAJOR FAULTS

Major faults resulting in high current draw (as indicated by the series lamp refusing to dim) can be isolated as follows:

1) The secondaries of the transformer can be unplugged from the board. Should the fault persist, this indicates the fault to be with the mains transformer. However, this may not be the only fault.
2) It is now necessary to unplug and remove the board.
3) A faulty channel may be isolated to only a few possibilities

- □A faulty power supply capacitor
- A faulty output device

- Over-bias of the output stage: If the lightbulb is glowing brightly then a reading of more than + 2V across the Vbe multiplier (Q8A, R22A, R21A) indicates excessive current draw in the output stage.

XLS PROCEDURE TEST SPEC

Load switch set to 4 W position unless stated otherwise.
Test carried out on all versions unless stated otherwise.

1. Protected power-up.

2. Short circuit test. OUTSC.TST LOAD SWITCH S/C.
I/P -10dBu @ 10kHz, 1kHz and 100Hz.
O/P between 0dBu and -40dBu -- unit survives.

3. Sensitivity test. GAIN1.TST.
I/P 0dBu @ 10kHz, 1kHz and 100Hz.
O/P 0dBr +/- 0.5dB ref. 31.5dBu.
XLS 602TX O/P 0dBr +/- 0.5dB ref. 33.4dBu.

4. THD test. THDA.TST.

XLS 602 I/P +4dBu @ 20kHz, 10kHz, 1kHz and 100Hz.
O/P 0dBr +/- 0.5dB ref. 35.5dBu and
< 0.1, 0.06, 0.02, 0.02 % THD respectively.

XLS 602TX I/P +2.25dBu @ 20kHz, 10kHz, 1kHz and 100Hz.
O/P 0dBr +/- 0.5dB ref. 35.5dBu and
< 0.1, 0.06, 0.02, 0.02 % THD respectively.

XLS 402 &TX +3dBu @ 20kHz, 10kHz, 1kHz and 100Hz.
O/P 0dBr +/- 0.5dB ref. 34.5dBu and
< 0.1, 0.06, 0.02, 0.02 % THD respectively.

XLS 202 I/P +0dBu @ 20kHz, 10kHz, 1kHz and 100Hz.
O/P 0dBr +/- 0.5dB ref. 31.5dBu and
< 0.1, 0.06, 0.02, 0.02% THD respectively.

5. THD + capacitor load test. THDAC.TST LOAD SWITCH 4uF.

XLS 602 I/P +4dBu @ 10kHz, 3kHz and 1kHz.
O/P <0.2, 0.07, 0.07 % THD respectively.

XLS 602TX I/P +2.25dBu @ 10kHz, 3kHz and 1kHz.
O/P <0.2, 0.07, 0.07 % THD respectively.

XLS 402&TX I/P +3dBu @ 10kHz, 3kHz and 1kHz.
O/P <0.2, 0.07, 0.07 % THD respectively.

XLS 202	I/P +0dBu @ 10kHz, 3kHz and 1kHz. O/P <0.2, 0.07, 0.07 % THD respectively.
6. Noise test.	NOISEA.TST. O/P <-90dBr ref. 31.5dBu.
XLS 602TX	O/P @ 50Hz and 100Hz <-68dBu.
XLS 402TX	O/P @ 50Hz and 100Hz <-68dBu.
7. Volume Control.	LIMA.TST.
XLS 602	I/P +6dBu O/P ref. 37.5dBu.
XLS 602TX	I/P +3dBu O/P ref. 34.5dBu
XLS 402&TX	I/P +5dBu O/P ref. 36.5dBu.
XLS 202	I/P +2dBu O/P ref. 33.5dBu. CW 0dBr +/- 0.5dB. CCW -90dBu.
8. Limiter test.	LIMIT.TST (JMLIMIT.TST on XLS 202). I/P increase from 0dBu to +10dBu O/P ref. 31.5dBu.
XLS 602	O/P limit to +5dBr +/- 1dB.
XLS 402	O/P limit to +3dBr +/- 1dB.
XLS 202	O/P limit to 0dBr +/- 1dB.
9. 15Hz filter test.	FILT15.TST I/P -10dBu sweep 10Hz to 100Hz O/P ref. 21.5dBu. O/P Smooth curve with -3dBr @ 15Hz +/- 1dB.
10. 30Hz filter test.	FILT30.TST I/P -10dBu sweep 10Hz to 100Hz O/P ref. 21.5dBu. O/P Smooth curve with -3dBr @ 30Hz +/- 1dB.
11. CMRR.	CMRR.TST I/P 0dBu @ 10kHz, 3kHz, 1kHz. O/P <-30dBr @ 10kHz ref. 31.5dBu. O/P <-40dBr @ 3kHz & 1kHz ref. 31.5dBu.

Please note:
For the XLS 402TX version, the test limits are the same as that for the standard XLS 402 except for the noise test where an extra parameter is included as per the XLS 602TX.