Xs500 Circuit Description

Introduction

These notes are intended to assist maintenance and service of the Xs family of amplifiers. It is recommended that reference be made to the relevant schematic diagrams while reading this document.

The component references detailed in the text are for channel 1. This document will refer to channel 1 references only. Operation of channel 2 is identical except where explicitly noted. Voltage values mentioned in the text are test voltages that may be used for diagnostic purposes, although attention is drawn to the surrounding text that explains circuit operation and may qualify such measurements.

Switching Power Supply

AC mains is inserted via the snap-in IEC connecter on the chassis. Earth is connected directly to chassis from the body of the IEC connector. Live passes through the circuit breaker. Live and neutral pass through an EMI filter consisting of C15 and C18 (X2 rated), L1, L2 and C16, C17, C19, C20 (Y2 rated). C1 and C4 act as conducted EMI suppression caps. Live passes through the soft-start system, TH1 and RLY1. RLY1 shorts out TH1 when the power supply is running.

Live and neutral then pass to bridge rectifier BR2, which for the 230V setting (jumpers set to SP1-SP3 and SP2-SP5) full-wave rectifies mains, smoothing performed by reservoir capacitors C22, C23, C24, C25, C26, C27. In the 120V setting (jumpers set to SP1-SP2 and SP4-SP5), this power supply is configured as a voltage-doubler. Thus, the High Tension (+HT) DC generated is approximately equal for 230V mains and 120V mains. This will result in about 320VDC between 'LIVE GND' and +HT. 'LIVE GND' is named as such because it is not isolated from mains but it is the reference point for the power supply. If you need to stick a scope probe around the primary side with the unit plugged in you must connect mains via an isolation transformer. Without this, at best you will only trip your RCD breaker, at worst you or your scope may not live to regret it. Do not forget that 320VDC is still pretty shocking whether it is isolated or not.

R28 and R29 ensure proper voltage sharing of the reservoir caps.

Power for the switching controller circuit is provided from two sources. At start-up, the power comes from R30, R31, ZD1, D1 and C33. C33 is charged up to about 47V through D1 from zener regulator R30, R31 and ZD1. The command to start the power supply comes from the PIC (+5V for off, 0V to switch on) via R32. The LED in OPT1 is turned on which turns the transistor on, shorting out pins 5 and 4. While the transformer windings are cooler than 120°C the thermal cutout (between pins 21 and 22 of T900) will be a short circuit. R33 will be connected to the top of C33 and will form a zener regulator with ZD2. The output of this zener regulator is buffered by TR1, which then powers the controller for long enough until the second source of power is ready. The second source of power comes from the transformer on pins 16 and 17. This secondary is voltage-doubled by C47, D6, D5 and C46 and produces about 48VDC on VAUX. This is connected via D2 to the anode of C33 so the controller circuit can continue running. VAUX is used to directly power RLY1 to short TH1 out while the power supply is running. The circuit comprising R34, R35, ZD3, R36, TR2, and R37 shut down the power supply when the voltage on C33 falls below 32V. While the voltage on C33 is greater than 32V, TR2 is switched on and pulls pin 10 of IC6 down to 0V, which 'enables' IC6. When the voltage on C33 falls below 32V, TR2 switches off and pin 10 of IC6 is pulled up to 20V through R37, 'disabling' IC6.

The switching controller circuit is based around IC6, a SG3525 PWM controller. The switching frequency is set by R39 and C39 to about 85kHz. R38 controls the 'dead time' period, setting it to between 500ns and 1μs. Outputs appear at pins 11 and 14 of IC6. These two outputs are complementary; when one is high (20V), the other is low (0V). Due to the dead time control, neither outputs are high at the same time but both are low for the 'dead time' period. These outputs are fed through R40 and R41 to high current buffers

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TR3 and TR4 as well as TR5 and TR6. The buffered outputs push-pull drive the primary of the 'Pulse' transformer TX6. R42 is a damping resistor used to minimize ringing caused by imperfections in TX6. The transformer has two secondaries, each driving one IGBT in anti-phase. The turns ratio is 1.5:1 (primary:secondary) and due to the push-pull connection of the primary, the output of TX6 swings positive to about 15V to turn the IGBT on, falls to 0V switching the IGBT off during dead time and falls to about – 15V while the other IGBT is switched on.

IGBTs TR7 and TR8 form a half-bridge driver for T900. Snubbers R45, C43, R46, C44 damp any ringing that may occur. The drive for the transformer from the IGBTs is an 85kHz square wave almost hitting '+HT' at the top of its travel and bottoming out slightly above 'LIVE GND'. This drive is connected to the resonant inductor L3 and caps C29, C30, C31, C32 which in turn is connected to the primary of T900 pins 1 and 2. The other end of the primary at pins 19 and 20 connects between R28 and R29.

There are two main secondaries:
1. Pins 13 and 14 are the low voltage center tapped secondary winding. Output of this is full-wave rectified by D8, D9, D10, D11 and smoothed by C50 and C51. Further filtering is provided by L5, L6, and C52, C53 before passing to +15V and –15V regulators IC7 and IC8 respectively. The +15V and –15V outputs are 'decoupled' by C54 and C55 close to the regulators to ensure stability. D7 half-wave rectifies the secondary output. This is lightly smoothed by C49 and loaded by R51. This is passed via ZD5, R597, R590 and C546 to the PIC. While the power supply is running, this circuit will produce a digital 'high' at the PIC input. If the power supply stops for any reason, the small value of C49 means that the PIC will receive a digital 'low' well before any of the power supplies have drooped significantly, allowing the PIC time to prevent dips.

2. Pins 9, 10 are the main power center-tapped secondary. This is full-wave rectified by D18, D19, D16, D17 and smoothed by C60, C61 to produce +HT, -HT so that ±HT = ±100V. R53 is the negative rail bleeder.

Amplifier (Refer to Channel 1)

The amplifier consists of a 'Class A' driver and a 'Class AB' power output stage. The driver provides voltage gain only; the output stage provides current gain only. Audio signal enters the amplifier through DC blocking capacitor C124, then low-pass filter R111 and C101 and onto the base of TR103. R110 provides a low source impedance in case the front panel board is disconnected. R112 provides a DC path to ground for the base current of TR103.

The output of the amplifier is fed back through potential divider R117 and R115 to the base of TR104. C102 decouples the feedback signal at DC so that DC offsets generated by TR103 and TR104 are not amplified at the output. D104 and D105 protect C102 in the event of a DC fault. TR103 and TR104 form a Long-Tailed Pair to amplify the difference between the input signal and the feedback signal. The gain of the LTP is reduced by R108 and R109 to help prevent oscillations and de-sensitize the performance of the input stage to parametric variations of the two transistors. A bias current of about 2.8mA for this LTP is provided through R107 from current source TR102, R106, D100, D101, and R105. In the quiescent state half of this current is driven through each of TR103 and TR104. The collector current of TR103 and TR104 are loaded through D102 and D103 by R113 and R114. The outputs of TR103 and TR104 are taken from the anodes of D102 and D103 to the bases of another LTP – TR107 and TR108. C103 determines the frequency response to ensure stability. As before, R121 and R122 reduce the gain of this LTP and the bias current is set to about 8mA by R123. The collectors of TR107 and TR108 are loaded with a current mirror – TR105 and TR106 to maximize gain and provide a push-pull output.

Some of this output is fed back to the base of TR104 through C106 and R116. This defines the open-loop frequency response independently of the output stage characteristics to ensure stability.

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Finally, the V_{be} multiplier – TR109, R125 and R124 – provides the output stage with two voltage signals which are identical except they are offset by a voltage varying between about 2.1V (heatsink hot) and 2.4V (heatsink cold). C108 ensures that the two offset signals are identical at AC.

The current source consisting of TR102, R106, D100 and D101 determines the operating point of the whole class A driver. Therefore, one can mute the amplifier by switching this current source off. The current source is switched off by TR101, R104, and C100. When TR101 is switched on, D100 and D101 are shorted out through R104, which mutes the current source. C100 is discharged in the process. When TR101 is switched off, C100 charges up through R105 until D100 and D101 are fully conducting which activates the current source.

TR101 is controlled by TR100, R102, R101, ZD107, R103, and R100. If the PIC is absent or its +5V supply has failed, the 'MUTE1' line will be in a high impedance state, which will not allow proper operation. The 4.7V reference supplied by R101 and ZD107 and emitter resistor R103 sets the current through TR100 to approximately 200µA. This is enough to switch TR101 on and mute the amplifier. This is the default state. When working, the PIC controls the state of the 'MUTE1' line. To mute the amplifier, the 'MUTE1' line is set to 0V. The current through TR100 is then set to about 4.2mA since R100 is essentially in parallel with R103. This mutes the amplifier as before. To activate the amplifier, the 'MUTE1' line is set to +5V. This, through R100, reverse biases the base-to-emitter junction of TR100. Thus, TR100 is switched off, as is TR101 so the amplifier becomes active.

Under normal conditions the signals at the bases of TR103 and TR104 will be the same. However, under fault conditions, such as DC offset at the output, the base voltages will become offset also. For example, in the event of a large offset of +50VDC at the output, a positive DC voltage will appear at the feedback point and thus at the base of TR104. This DC voltage will make D105 conduct protecting C102, so the resultant voltage at the base of TR104 should be 0.6 + 50V x R115/(R115+R117), about 4V. However, the important issue is that this voltage is positive. In the event the voltage is negative this indicates that the feedback divider is faulty. The voltage at the base of TR104 being positive while the base of TR103 is nearly 0V will then reverse bias the TR104 base-to-emitter junction, turning off the transistor. Therefore, no voltage should appear across R109 and R114 while twice the normal voltage will appear across R108 and R113. Should this not be the case, it indicates a fault in the input stage itself. The same process should now cause TR104, TR105 and TR106 to be off and TR108 to be fully on…

Class AB Output Stage

The input of the output stage is loaded by C107. This defines the HF input impedance and thus prevents oscillations that are caused by the variable, non-linear and sometimes negative input impedance. Resistors R126 and R127 ensure that output offsets are minimized when the amplifier is muted. D114 and D115 prevent the output from exceeding the power supply rails in the face of 'flyback' pulses from reactive loads.

The output stage consists of a symmetrical Siklai follower – TR112, TR114, R128, TR113, TR115, R129, R131, R130, C114 – generating the high current drive required for the parallel connected symmetrical follower output stage – TR116, TR117, TR118, TR119, R142, R144, R146, R148, TR120, TR121, TR122, TR123, R143, R145, R147, R149. V-I limiting is controlled by D108, D109, TR110, TR111, R134, R136, R138, R139, C117, R135, R137, R140, R141, C118, R132, C115, R133, C116, D112, D113, ZD108, ZD109, R187. C150, C151, C152, C153 stabilize TR110 and TR111 to prevent oscillations in the output when sourcing high current into low impedance loads.

Protection Scheme

Output Stage

Output stage protection is accomplished by a three-slope V-I limiting circuit having limiting characteristics chosen to emulate the safe operating area of the output stage transistors and their maximum operating temperature. The V-I limiting works by controlling TR110: when the base-to-emitter voltage of TR110 exceeds about 0.65V, TR110 turns on and steals current, via D108, from the input of the output stage and thereby limits the output. Thus, V-I limiting is controlled by controlling the base-to-emitter voltage of TR110. Each output device has its own current sharing resistor – R142, R144, R146, R148 – the voltage across which is proportional to the current flowing in the output device. These voltages are sampled and summed by R134, R136, R138, R139. C117 ensures stability when V-I limiting is activated. The voltage across the output devices is sampled by R142, R144, R146, R148 (R162 and ZD103 limit the voltage range to reduce off-load distortion) and this, summed with the output current derived signals from R134, R136, R138, R139 controls TR110 for output voltages less than about 3Vpk. Thus, the amplifier is protected for short circuits because the base-to-emitter voltage of TR110 increases when output current increases and when voltage across the output devices increases. For output voltages exceeding about 3Vpk, ZD109 conducts connecting R162 to sense the output voltage. In this case, as output voltage increases, the base-to-emitter voltage of TR110 reduces, thus the current limit is increased as the output voltage increases, defining the 3rd slope of the limiting characteristic.

Bridge Imbalance Protection

During normal operation, the bridged output is fully differential mode with little or no common-mode signal component. Activation of the output stage current limiters erratically upsets this state, producing a large common-mode error – imbalance – that can destroy the output stages. The bridge imbalance detection is performed by R13, R12, R15, TR11 and R17. In two-channel mode, the 'BRIDGE1+2' line is pulled up to about +13V. This switches TR11 on through R17. The collector of TR11 is connected to pin 23 of IC1 (PIC). The input of the PIC is internally protected by diodes against inputs above +5V and below 0V. Thus, in two-channel mode, pin 23 of IC1 receives no signal. In bridge mode, the 'BRIDGE1+2' line is held at 0V, which switches TR11 off. Now pin 23 of IC1 can receive a signal. R13 and R12 sum the output of each channel, the result appearing across R15, which sets the sensitivity. If the bridge is balanced, the voltage across R15 will be 0V. If the bridge is unbalanced, there will be voltage across R15, which is also connected to pin 23 of IC1. When an imbalance is detected, the PIC immediately mutes both channels for approximately 4 seconds. The channels are then re-activated.

DC Protection

Each channel's output is connected through R20 and R21 to R578 and C539. C539 ensures that only DC is detected. For no DC fault, R579 pulls pin 9 of IC1 towards +5V. For a positive fault, D507 becomes forward biased and turns TR520 on, pulling pin 9 of IC1 towards 0V. For a negative fault, D508 becomes forward biased and turns TR521 and TR522 on, pulling pin 9 of IC1 towards 0V. In the event of a DC fault, the PIC switches the power supply off, waits and then tries again. C536, C537, C538, C540 prevent the full-wave rectification of power supply noise causing false alarms.

Front Panel and Small Signal Circuits

Refer to channel 1:

Audio signal enters the amplifier from the input board in balanced form, positive phase – 'hot' – on pin 1 of either J504 or J501 or on J1 pins 1/13 or 4/16. Negative phase 'cold' enters on pin 3 of either J504 or J501 or on J1 pins 2/14 or 5/17. The signals on each pin will always be out of phase but will not necessarily be equal in amplitude. This signal passes through RF1 and RF2, which shunt RF noise to chassis. R1 and R2 prevent thumps due to connection / re-connection. Signal then passes through dc blocking caps C5 and C6 and on to the front panel board through pins 1 and 2 of CN17.

The balanced signal is converted to single-ended by IC1-A (pins 1,2,3) and R1, R2, R3, R4, R52, R59 that form a standard differential amplifier. C25 and C26 shunt HF energy to ground. The signal exits pin 1 of IC1-A and is routed to two places, one being the signal LED circuit, the other being the level control P1, R5 and analog switch IC2-C. P1 is a standard 10K linear pot rather than a log taper pot. The level control is given an 'audio' taper by R5 so that the level is attenuated by 10dB at the center position (rather than 6dB for linear or 20dB for log). The analog switch is normally closed (pin 1 of IC2 low – 0V) allowing operation of the level control.

Up to this point, channel 1 and channel 2 have identical operation. Operation is dictated by the bridge switch position (rear panel).

1. Bridge Mode Off

    The 'BRIDGE1+2' signal line will be held high by R49 and LD9. Although LD9 will not be illuminated, enough current flows to pull pins 8 and 9 of IC2 high. This opens the switches IC2-C (pins 10 and 11) and IC2-D (pins 6 and 7). Channel 1 signal enters pin 5 of IC1, which is configured to have a gain of +14.5dB by R17, R15 and continues through R7 to pin 13 of CN1. Channel 2 signal enters pin 5 of IC3, which is configured to have a gain of +14.5dB by R30, R16 and continues through R14 to pin 15 of CN1.

2. Bridge Mode On

    The 'BRIDGE1+2' signal line will be held low by the rear panel bridge switch. LD9 will be illuminated and pins 8 and 9 of IC2 will be pulled low (0V). This closes the switches IC2-C (pins 10 and 11) and IC2-D (pins 6 and 7). Channel 1 signal enters pin 5 of IC1, which is configured to have a gain of +14.5dB by R17, R15 and continues through R7 to pin 13 of CN1. Closure of switch IC2-C connects this signal to pin 6 of IC3 through R29, which, in conjunction with R30, configures IC3-B to be a unity gain inverter (R16 does not affect the signal gain). Thus, the channel 1 signal is inverted and passed to channel 2 through R14 to pin 15 of CN1. Channel 2 signal is shorted to ground through switch IC2-D.

Signal LED

The signal is coupled from pin 1 of IC1 through C10 and across R35 to IC8 pin 3. Initial conditions: C15 has 0V across it and LD1 is off. Pins 1, 2 and 3 of IC8 are at 0V. A signal appears at pin 3 of IC8. It is moving from 0V in a positive direction. Due to the large open-loop gain of IC8, pin 1 will move in a positive direction at a much greater rate. This will forward bias the diode in D1 (which connects pin 1 to the top of C15) and charge up C15. When enough volts have accumulated on C15, LD1 will conduct, it is current limited by R34 and R33. R34 and R33 also form a potential divider applying negative feedback to pin 2, thus setting the sensitivity of the circuit. The signal at pin 3 now moves in a negative direction. Therefore, pin 1 will move negative at a much greater rate and the diode in D1 (which connects pin 1 to the top of C15) becomes reverse biased. The other diode in D1 (connecting pin 1 to pin 2) now conducts

preventing saturation of the op-amp. LD1 will continue to glow by discharging C15 until the voltage on C15 falls below that required to turn on LD1.

Clip LED

The clip detector circuit is on the main board consisting of IC100-A, R150, R152, R151, R154, R153, R155 and C119 & C120. These are connected to form a differential amplifier that samples the voltage between the base of TR103 and the base of TR104. This voltage is the difference between the input and the divided-down output of the amplifier. When the amplifier clips, there is a large difference between the input and the divided-down output, which is amplified by the differential amplifier. This passes from pin 1 through R155 to pin 21 of CN17 and onto the front panel board. Here it is full-wave rectified by D5 and D6, smoothed by C17 and the resultant voltage illuminates LD5 through R45.

System Management

Power for the management system is provided by a conventional transformer-rectifier-capacitor-regulator supply. TX5 receives AC mains through F1. The secondary passes to the bridge rectifier made of 1N4004 diodes D511, D512, D513 and D514. The rectified AC is then smoothed by C530 producing about 25VDC for 230VAC mains or 12.5VDC for 115VAC mains. The regulator circuit used is similar to the internal workings of an LM317. TR518 and TR519 form a Darlington pass transistor. R559 provides bias current for D506, a TL431. D506 combines a voltage reference of 2.5V and an amplifier in one package. C531 prevents oscillations. R560 and R561 set the output voltage to (5V – 2.5V) x (1+R560/R561).

The brain behind operations is IC1, a PIC16C57 microcontroller. This PIC is not a flash part. The clock is set to approximately 3.28MHz by the RC of R580 and C542 connecting to pin 27 of IC1.

Each of the rear heatsinks has an LM35DZ (T0-92), IC505 and IC506, attached via a clip. The voltage at pin 2 of each of these devices gives a measurement of temperature – 10mV/°C starting at 0V for 0°C. Continuing with channel 1, the temperature signal is filtered by R564 and C533 and enters pin 3 of IC502-A. This is configured to give a gain of 10.2 giving 102mV/°C. The output at pin 1 of IC502-A is coupled through potential divider R566 and R567 to pin 6 of IC502-B at which point the signal is 34mV/°C. IC502-B (pins 5, 6, 7), R568, C535, R576 and IC1 pins 6 and 7 comprise an analog-to-digital converter. At the start of conversion, pin 6 of IC1 is set to 0V for 1ms and discharges C535 through R576. Pin 6 of IC1 is then set to high impedance mode. At this point, pin 7 of IC502-B is at –13.5V because pin 5 is lower than pin 6. Now, the voltage on C535 ramps to about 600mV/ms because it is being charged by R568. The ramp stops at about 5.5V, limited by the protection diode on pin 6 of IC1. The voltage on C535 is connected to pin 5 of IC502-B so that when the ramp voltage exceeds the temperature voltage on pin 6, pin 7 changes to +13.5V. Pin 7 of IC502-B is connected to pin 7 of IC1 through R569. In this way, IC1 has a measure of time between the start of conversion and when pin 7 of IC1 receives logic 'high' which is proportional to the voltage at pin 6 of IC502-B. After 18ms, the conversion cycle starts again.

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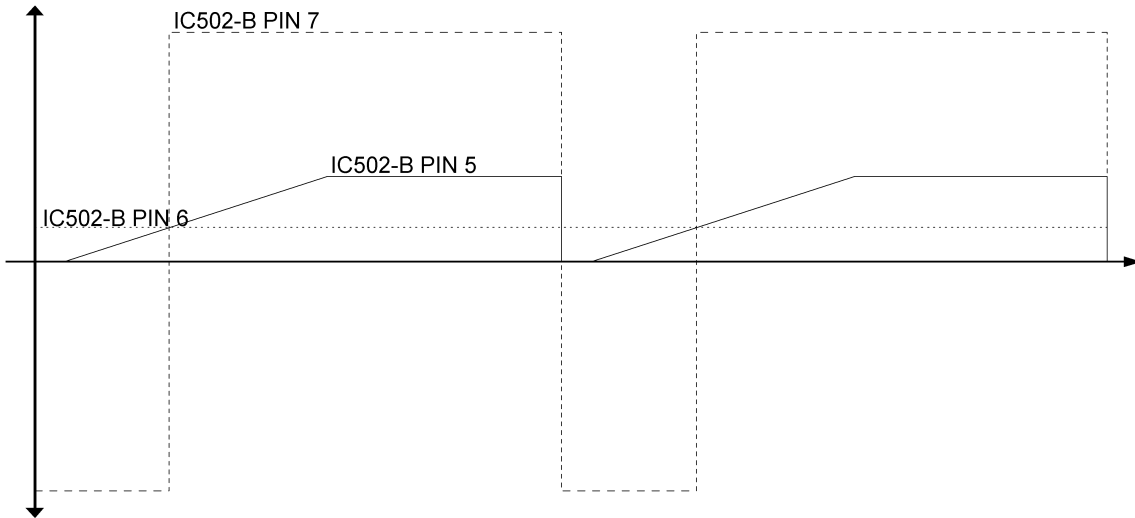
The heatsink temperature measurements are used to control the fan speed and to mute overheating channels. For instance, if the channel 1 heatsink temperature exceeds 85°C, channel 1 is muted. Channel 1 will be re-activated when the heatsink temperature falls below 75°C. The two fans are connected in parallel, the negative wires connected to –15V, the positive wires connected through R599 and R600 and the collector of TR530. If the heatsink temperature is less than 55°C, pin 17 of IC1 is set to +5V. This turns off TR527 which turns TR532 on, turning TR530 on leaving the fans powered through –15V. If the heatsink temperature exceeds 55°C, pin 17 of IC1 is set to 0V, switching TR527 on which turns TR532 off, turning TR530 off, which powers the fans with –24V. The fans are returned to slow speed (-15V) when the heatsink temperature falls below 50°C. The fans are completely switched off when a brownout condition is detected.

Service Notes:

When powering an Xs amplifier after repair, there is always a possibility that undetected faults will result in further damage when the unit is re-tested. To minimize the risk of further damage, it is recommend that the following procedure is adopted;

1. Disconnect the brown wire faston connected to the IEC inlet. Connect a 100W mains lamp in series (between this faston and the .250" tab on the IEC inlet).

2. Power the amp in the normal way. The lamp will initially glow brightly, then dim as the internal capacitances become charged. The unit may then be functionally tested with no load connected. Once satisfied that the unit is operating correctly, the mains supply may be applied to the unit as normal and the unit may be tested with a load.

If the lamp does not dim, this indicates a major fault still exists and must be repaired before full AC mains may be re-applied.

Locating Major Faults

Major faults resulting in high current draw (as indicated by the series lamp refusing to dim) can be isolated as follows:

1. Unplug the secondary harnesses from the main board. Should the fault persist, this indicates the fault to be with the mains transformer. However, the fault may not be confined strictly to the mains transformer.

2. Unplug and remove the main board. This requires removing all of the heat sink mounting screws with shoulder washers (NOT the T0-3 mounting screws). Check the bottom of the main board for visible signs of damage.

3. A faulty channel may be isolated to a few possibilities. The fault LEDs on the front panel are usually revealing when there is a faulty channel. The possible cause can be one of the following: faulty or shorted output device, faulty or shorted supply cap (primary or secondary), over-bias of the output stage.

4. If the unit is plugged into AC mains and none of the LEDs are illuminated on the front panel, the cause may be one of the following: connection between front panel board and main board (check the seating of CN17), TX5 may be suspect (measure primary and secondary for open circuits), make sure PIC (IC1) is seated fully and properly in IC socket, ensure that AC mains is connected (correctly) both to the IEC inlet and to the main board.

5. If quiescent current draw on the Xs900 is above 400W per channel, the fault is most likely one of the rail-switching FETs. Check FET500, FET501, FET502, FET503, FET600, FET601, FET602, FET603 for shorts.

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Channel Bias Setting

The bias setting for each channel of all Xs amplifiers should be set to 3.0mV respectively. This can be done by adjusting the bias pot for each channel while monitoring the voltage between the two test points provided for that channel on every Xs amp. For instance, if adjusting the bias on channel one of the Xs900, place one test lead of a DMM on TP101 and the other test lead on TP102. Slowly adjust R125 until the DMM reads 3.0mV. This setting drifts slightly with temperature so it is best to let the amp warm up for approximately 5 minutes or so prior to setting channel bias.

Basic Checks

If the fault LEDs are illuminated and not flashing, this indicates a DC fault on one or more of the channels of the amplifier. This can be isolated by removing the main board and output board from the chassis, disconnecting the output board from the main board header (leave the output harnesses connected to the main board), and powering the main board. The amp should run out of the chassis, enabling you to check for DC offset. Do not power the main board of the amp without the output harnesses attached to the main board as this can result in a failure.

If the unit displays flashing fault LED(s), check F1 first as it may be open. If F1 is ok, measure the resistance between the following points as there should no shorts:

1. Cases of the output devices to the heatsinks.
2. Across the outer leads of the driver transistors for each channel.
3. Cases of the output devices to the flag connectors on the main board.

If you locate a short in any of these locations, you have found the faulty channel. If these basic checks do not locate the fault, it is likely in the power supply.

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