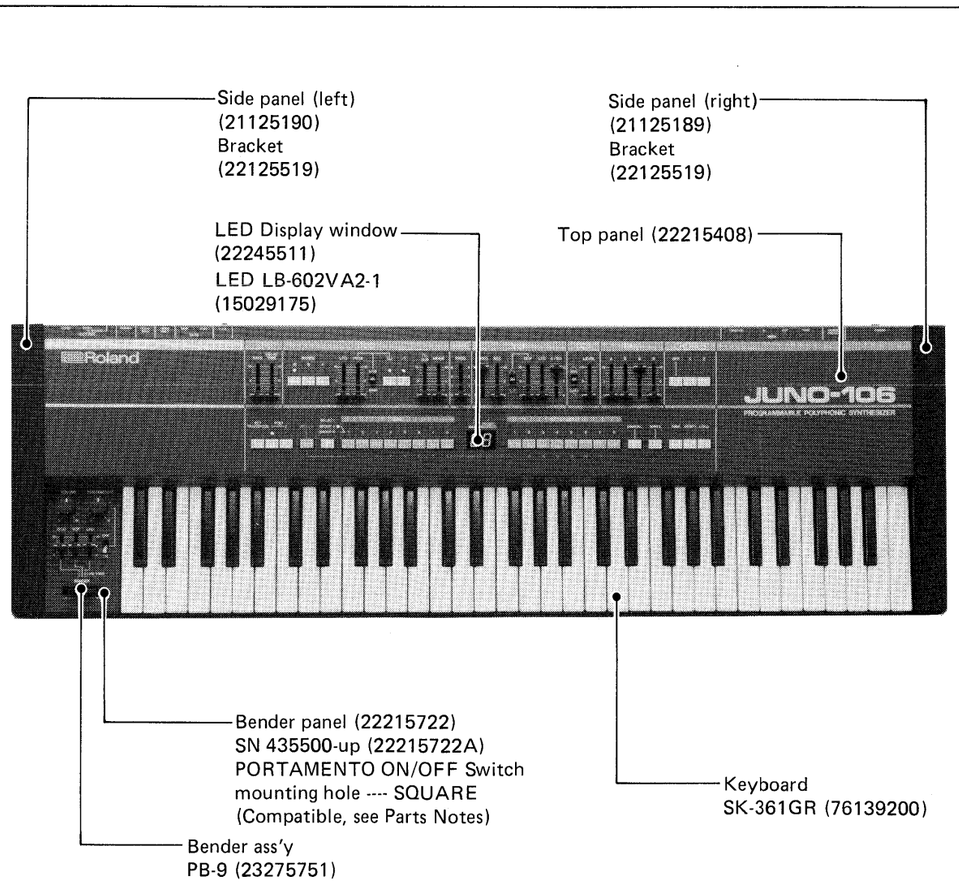
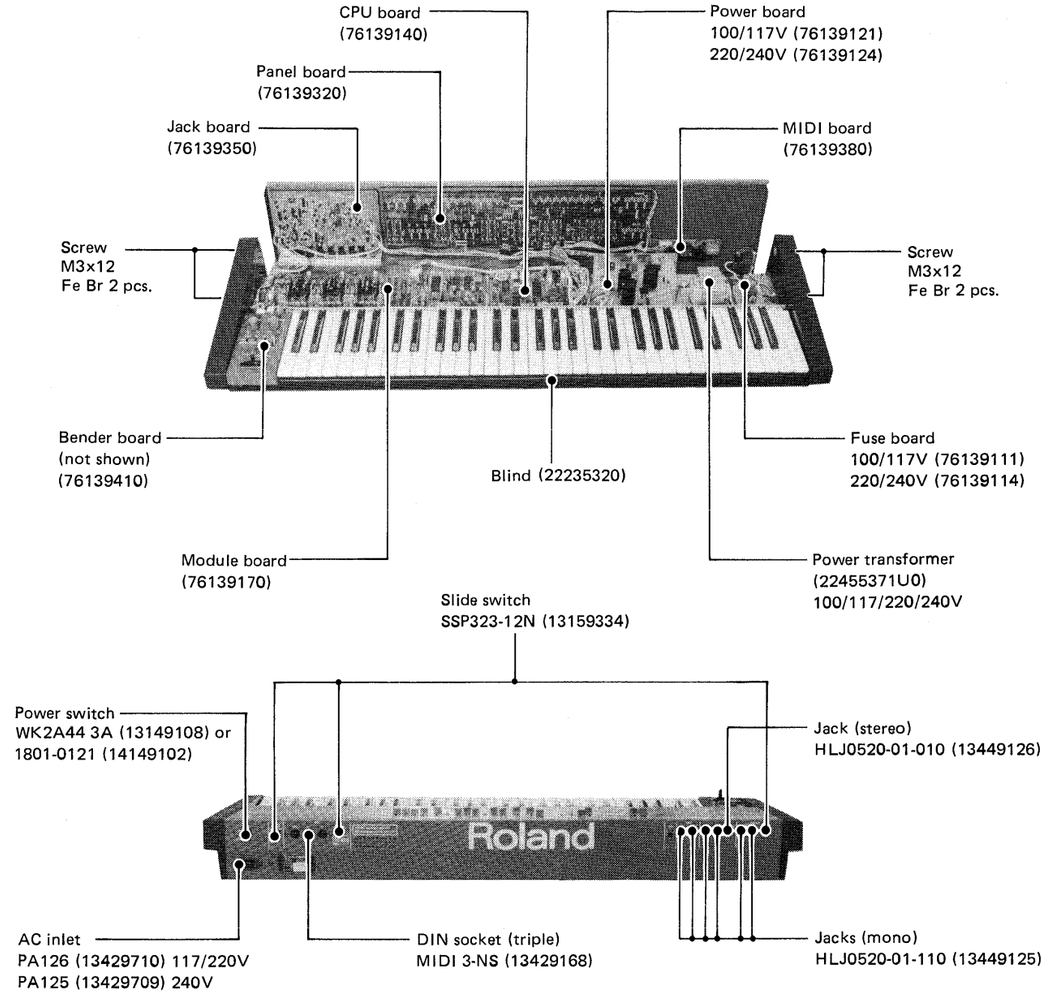
JUNO-106 SERVICE NOTES

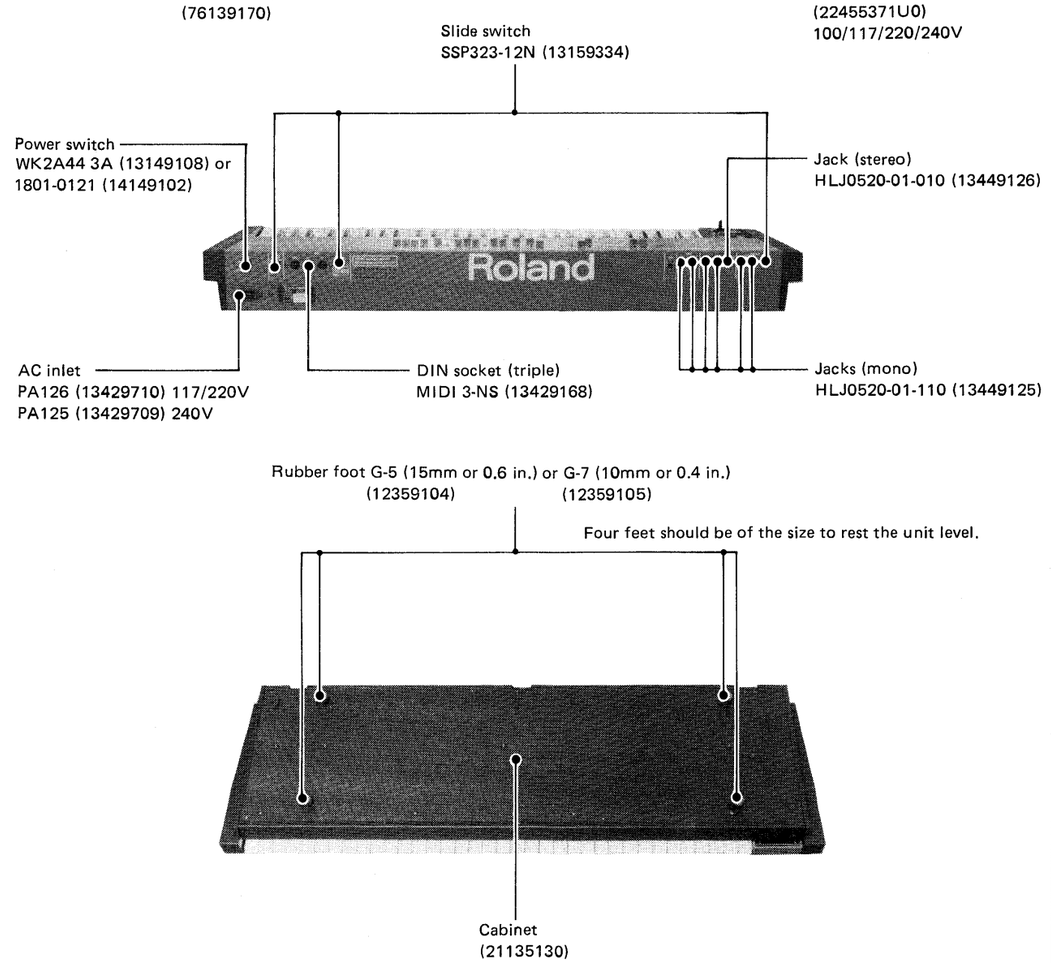
First Edition

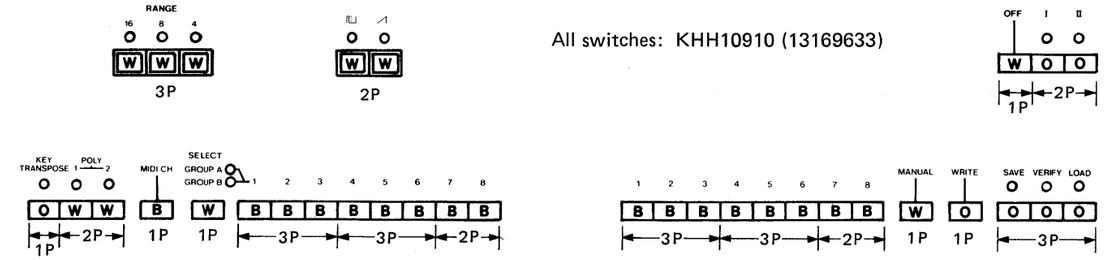
SPECIFICATIONS

KEYBOARD	61 keys, 5 octaves, C scale
DCO	
TUNE	±50 cents
LFO MOD.	±400 cents
BENDER	±1200 cents
VCF	
CUTOFF FREQ.	5Hz to 50kHz
RESONANCE	0 to self oscillation
ENV MOD.	±14 octaves
LFO MOD.	±3.5 octaves
BENDER	±3.5 octaves
KEY FOLLOW	+3/–2 octaves
ENV	
ATTACK TIME	1.5ms to 3s
DECAY TIME	1.5ms to 12s
SUSTAIN LEVEL	0 to 100%
RELEASE TIME	1.5ms to 12s
LFO	
RATE	0.1Hz to 30Hz
DELAY TIME	0 to 3s
AUDIO OUTPUT	L: –30dBm; M: –15dBm; H: 0dBm
DIMENSIONS	992(W)x320(D)x120(H)mm 39-1/16(W)x12-5/8(D)x 4-11/16(H) in.
WEIGHT	10kg/22 lb.
POWER CONSUMPTION	25W (20W--100V)

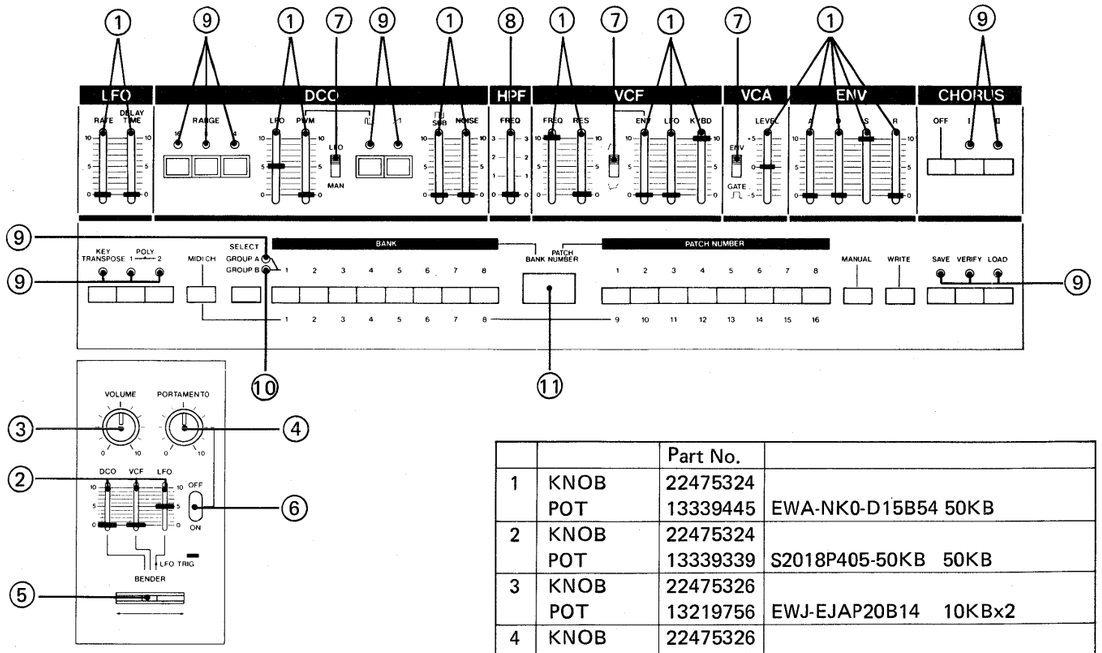








	Button		Part No.
W	WHITE	1P	22475593
		2P	22475590
		3P	22475587
B	BLUE	1P	22475594
		2P	22475591
		3P	22475588
O	ORANGE	1P	22475595
		2P	22475592
		3P	22475589



		Part No.	
1	KNOB	22475324	
	POT	13339445	EWA-NK0-D15B54 50KB
2	KNOB	22475324	
	POT	13339339	S2018P405-50KB 50KB
3	KNOB	22475326	
	POT	13219756	EWJ-EJAP20B14 10KBx2
4	KNOB	22475326	
	POT	13219241	EVH-5XAP20B54 50KB
5	BENDER	23275751	PB-9
6	LEVER SW	13139137	SLE622-18P (SN 380100—425499)
6	LEVER SW	13139152	SLE622-9C (SN 435500—)
	KNOB	22475336	
7	KNOB	22475325	
	SLIDE SW	13159147	SSY022-6N
8	KNOB	22475324	
	SLIDE SW	13159506	SW3028-4
9	LED	15029103	TLR-124 (red)
10	LED	15029105	TLG-124A (green)
11	LED	15029175	LB-602VA2-1

PARTS CHANGE NOTES

CPU IC1 CPU BOARD
IC29 MODULE BOARD

Various CPUs used on both boards

1. μPD7810G. . . . . .CPU Board, Module Board without internal ROM
2. μPD7811G-033/037/076 .CPU Board, Module Board with internal ROM that contains program for different model
3. μPD7811G-102-### . . . .with internal ROM that contains program dedicated to Module Board of JUNO-106
4. μPD7811G-101-### . . . .with internal ROM that contains program dedicated to CPU Board of JUNO-106

CPUs of 1 and 2 need an external ROM:
CPU Board - IC2
Module Board - IC37

CPU of 3 or 4 can replace existing CPU regardless of presence or absence of ROM. Although both CPUs do not require external ROM, it is harmless for their performance.

WAVE GENERATOR
ICs 4, 8, 12 MODULE BOARD

Three versions used on the board

1. MC5534 . . . . .incomplete 2-channel
2. MC5534-1 . . . .1-channel
3. MC5534A . . . .complete 2-channel

When replacing existing MC5534 series, use only MC5534A for better performance and easier job.

NOTE: Two ICs of 1 or 2 are accommodated together in the same mounting holes which are originally designed for one IC.

VCF/VCA ICs 3, 5, 7, 9 MODULE BOARD

Change from A1QH800170 to A1QH80017A
Compatible with each other. However, to avoid timbre difference among voices, mixing use of two versions in a unit is not recommended.

ICs 16, 19, 20 MODULE BOARD

Both TL072CP and TL082CP can be used.

ICs 23, 24, 26 MODULE BOARD

TC4051B (Toshiba) cannot be used.

PORTAMENTO SWITCH/ SLOT BENDER PANEL

SN 435500-up
Switch. . . . . .from SLE-622-18P (SLE622-9C with an aluminum sleeve) to SLE622-9C and synthetic knob (22475336).
This change is to reduce the chance of RAM memory from being shifted by static charges entering through the switch.
Bender Panel . . . .For accommodating above-mentioned square knob, mounting slot in the Bender Panel is also squared.

RUBBER FEET CABINET

From G-5 to G-7
G-5. . . . . .H: 15mm (0.6 in.)
G-7. . . . . .H: 10mm (0.4 in.)
Also diameter is different between the two.
To rest the unit level use four of a size.

JAPANESE VERSION ONLY

SN 418100-up
Transformer. . . . .change to 22455380N0 100V only.
SN 419000-up
Power Cable. . . . .change from detachable Cord Set (13439825) to Non-detachable cable (13439801) which requires Cord Holder (22195549) and Bushing instead of AC Inlet.

PARTS LIST

CASE

21135130	Cabinet	
21125189	Side panel	(right)
21125190	Side panel	(left)
22125519	Bracket	(R.L same)
22215408	Top panel	
22215722	Bender panel	(SN 380100-425499)
22215722A	Bender panel	(SN 435500-up)
22235320	Blind	
22245511	LED Display window	
12359104	Rubber foot G-5 h: 15mm (0.6 in.)	(SN 380100-405699)
or		
12359105	Rubber foot G-7 h: 10mm (0.4 in.)	(SN 405700-up)

KNOB, BUTTON

22475326	Knob	VOLUME, PORTAMENTO
22475324	Knob	slide Pot, SW
22475325	Knob	slide SW
22475336	Knob	PORTAMENTO (SN 435500-up)
22475593	Button (white)	1P
22475590	Button (white)	2P
22475587	Button (white)	3P
22475594	Button (blue)	1P
22475591	Button (blue)	2P
22475588	Button (blue)	3P
22475595	Button (orange)	1P
22475592	Button (orange)	2P
22475589	Button (orange)	3P

POWER SWITCH

13149108	WK2A44 3A	
or 14149102		1801-0121

PUSH SWITCH

13169633	KHH10910

LEVER SWITCH

13139137	SLE622-18P	(SN 380100-425499)
	SLE622-9C with aluminum sleeve	PORTAMENTO
13139152	SLE622-9C	(SN435500-up)

SLIDE SWITCH

13159334	SSP323-12N	MEMORY PROTECT, OUTPUT LEVEL, FUNCTION
13159147	SSY022-6N	PWM, VCF ENV, VCA
13159506	SW3028-4	HPF

PCB ASS'Y

76139140	CPU BOARD	(pcb 22915901)
76139170	MODULE BOARD	(pcb 22915902)
76139320	PANEL BOARD	(pcb 22915911)
76139350	JACK BOARD	(pcb 22915899)
76139410	BENDER BOARD	(pcb 22915899)
76139380	MIDI BOARD	(pcb 22915899)
76139121	POWER SUPPLY BOARD	(pcb 22915900) 100/117V
76139124	POWER SUPPLY BOARD	(pcb 22915900) 220/240V
76139111	FUSE BOARD	(pcb 22915981) 100/117V
76139114	FUSE BOARD	(pcb 22915981) 220/240V

JACK

13449126	HLJ0520-01-010	stereo
13449125	HLJ0520-01-110	mono
13429168	MIDI3-NS	DIN Triple

FUSE

12559335	GGS 1.0A	pri. 100/117V
12559510	CEE T400mA	pri. 220/240V
12559521	CEE T1.6A	sec. 200/240V
12559511	CEE T500mA	sec. 200/240V

BENDER UNIT

23275751	PB-9

POSISTOR

5229919	ERS-A33J 561T 560

RESISTOR ARRAY

13919310	RM-8 103J	10K x 8
13919311	RM-8 223J	22K x 8
13910114	RGSD 4x223K	22K x 4
13919146	RKM14L503F	R-2R 12 bit

POTENTIOMETER

[Slider]

13339445	EWA-NK0D15B54	50KB	30mm stroke
13339339	S2018P405-50KB	50KB	20mm stroke

[Rotary]

13279750	EVJ-ELAE02B54	50KB	TUNE
13219241	EVH-5XAP20B54	50KB	PORTAMENTO
13219756	EWJ-EJAP20B14	10KB x 2	VOLUME

[Trimmer]

13299182	EVN-E4AA00B53	5KB	
13299191	EVN-C3AA00B23	2KB	PS BRD, VR1 (SN 442000-up)
13299183	EVN-E4AA00B14	10KB	
13299184	EVN-E4AA00B24	20KB	
13299185	EVN-E4AA00B15	100KB	
13299186	EVN-E4AA00B54	50KB	
13299554	RVS0707V101-3-502 (BUL)	5KB	PS BRD, VR2

COIL

12449229	FKOB160MH15	AC Line Filter
or		
12449244	SC-02-15E	AC Line Filter
13529105	DSS310-55D223S	EMI Filter

POWER TRANSFORMER

22455371U0	100/117/220/240V
22455380N0	100V only

DIODE

15019126	1SS-133	
15019245	1B4B41	rectifier bridge
15019254	2B4B41	rectifier bridge
15019208	1SR35-200	
15019531	RD-6.8EB-3	zener
15029103	TLR-124 (LED)	red
15029105	TLG-124A (LED)	green
15029175	LB-602VA2-1 (LED)	display

PHOTO COUPLER

15229709	TLP552

IC

IMPORTANT:
Refer to PARTS CHANGE NOTES and schematic diagram when replacing. SELECTIVELY USED SEMICONDUCTORS

15179184	μPD-7810G	CPU external ROM version for both CPU and MOD Board
15179190	μPD-7811G-102-36	CPU internal mask-ROM version for MODULE BOARD
15179194	μPD-7811G-101-36	CPU internal mask-ROM version for CPU BOARD
15179649	2764-A649	EPROM CPU Board for external version CPU only
15179650	2764-B650	EPROM Module Board for external version CPU only
15179317	TC5517APL	RAM
or		
15179330	MB8416-20L	RAM
15179185	M82C53	Triple Programmable Interval Timers
15159310H0	HD14555BP	Dual Binary To 1-Of-4 Decoder/Demultiplexer
15159503	TC40H000	Quad 2-Input NAND Gate
15159505	TC40H004	Hex Inverter
15159514	TC40H032	Quad 2-Input OR Gate
15159506	TC40H138	3 to 8 Line Decoder/ Demultiplexer
15159532	TC40H161P	4 bit Counter
15159508	TC40H373	Octal D-type Latch
15159128T0	TC4050BP	Hex Buffer
15159113	HD14051BP	8ch Multiplexer/ Demultiplexer (exclude TOSHIBA)

15159114T0	TC4052BP	Differential 4ch Multiplexer/ Demultiplexer
15159116T0	TC4069UBP	Hex Inverter
15159133	TC40174BP	Hex D-Type Flip-Flop
15159701	M54522P	Transistor Array
or		
15159704T0	TD62084AP	
15149110B0	M54562P	Transistor Array
or		
15159117	M54564P	Transistor Array
15169346	HD74LS03	Quad 2-Input NAND Gate
15169117H0	HD7407P	Hex Buffers/Drivers
15189115	TL-022CP	Low-Power OP Amp
or		
15189146	IR9022	Low-Power OP Amp
15189119	TL-062CP	Low-Power JFET-Input OP Amp
15189154	TL-064	Low-Power JFET-Input OP Amp
15189129	TL-072CP	Low-Noise JFET-Input OP Amp
15189118	TL-082CP	JFET-Input OP Amp
15189136	M5218L	Low-Noise OP Amp
15189142	TA75558S	Low-Noise OP Amp
15229802	BA662A	VCA Custom IC
15229816	MC5534A	Wave Generator Custom IC
15229817	A1QH800170	VCF, VCA Custom IC
or		
152298170A	A1QH80017A	VCF, VCA Custom IC
15219124	μPC1252H2	VCA
15219213	MN3009	BBD
15169504	MN3101	BBD DRIVER
15199106M0	AN7805	Voltage regulator
15199117	M5230L	Voltage regulator
15199123	M5231L	Voltage regulator

CAPACITOR

13589465	ECQ-U2A473MN	Line Capacitor
13529104	DE7150F472MVA1	Line Capacitor
13659214M0	ECET25R682SW	6800μF/25V
13659223M0	ECET35R332SW	3300μF/35V

TRANSISTOR

15119113	2SA1015-GR (or 15119112 2SA1015-Y)
or	
15119106DR	2SA933-R (or 15119106D0 2SA933-Q)
or	
15119124	2SA1115-F (or 15119129 2SA1115-E)
15119814	2SB1015-D
15129114	2SC1815-GR (or 15129115 2SC1815-Y)
or	
15129113	2SC1740-R (or 15129141 2SC1740-Q)
or	
15129135	2SC2603-F (or 15129140 2SC2603-E)
151291080A	2SC945 Selected For Noise Generator
15129136	2SC2878A
15129827	2SD1406-O
15139103	2SK30A-GR (or 15139101 2SK30A-Y)

AC CORD, AC CORD SET

13439812F0	AC Cord Set	UC-704-J01	117V
13439813F0	AC Cord Set	EC-210-J06	220V
13439817F0	AC Cord Set	EC-702-J05	240V 2P
13439814F0	AC Cord Set	SC-415-J06	240V 3P
13439825F0	AC Cord Set	DC-320-J01	100V
or			
13439801	AC Cord	VFF 2.5m	100V
13429710	AC Inlet		117/220V
13429709	AC Inlet		240V
12369504	SR-4N-4	Cord Bushing 100V version without AC Inlet	
22195549		Cord Holder 100V version without AC Inlet	

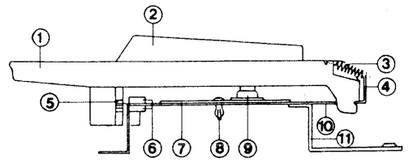
OTHERS

12389728	KMFC1034T1	8MHz	ceramic resonator MASTER OSC MOD BOARD
12389719	KMFC1007T31	12MHz	ceramic resonator (CPU/MOD BOARDS)
12569149	BR2325-1HC	Lithium Battery	

KEYBOARD

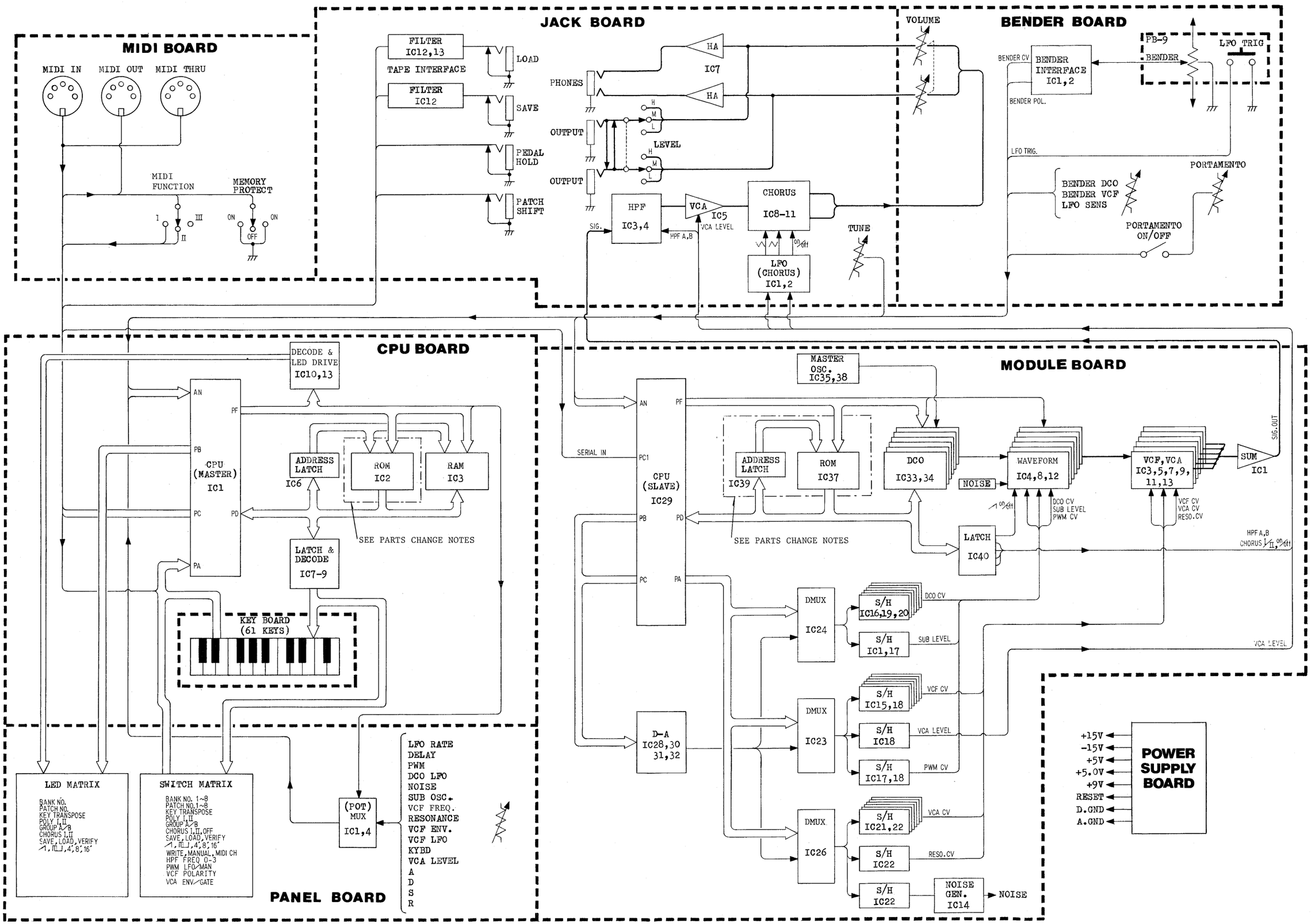
76139200	SK361GR	61 Keys

SK361GR Parts List



1	22575136	Natural Key	C.F
1	22575137	Natural Key	D
1	22575135	Natural Key	E.B
1	22575138	Natural Key	G
1	22575134	Natural Key	A
1	22575139	Natural Key	C'
2	22575140	Sharp Key	
3	22175132	Key Spring	
4	7612721000	Chassis H140	
5	22155716	Guide Bushing	
6	22265147	Level Felt H143	
7	76127220C0	OPH221,2(pcb 052H462)	
8	——	Nylon Rivet (NRP-345)	
9	2218520700	Contact Rubber	
9	2218520800	Contact Rubber	
10	22135406	Key Stopper H6	
11	22035120	Chassis Bracket	

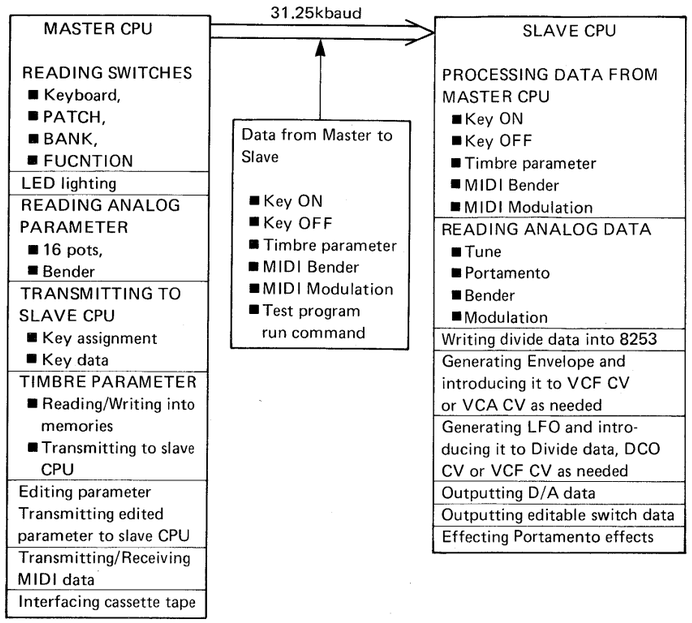
BLOCK DIAGRAM



CIRCUIT DESCRIPTIONS

GENERAL

There are two CPUs on the JUNO-106: IC1 (master on CPU Board) and IC29 (slave on Module board). Two CPUs share the tasks as shown below:



CPU BOARD

Master CPU μPD7810/7811

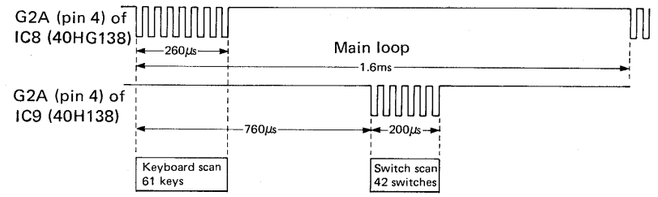
DESIGNATION		PIN NO.	FUNCTION
AN (ANALOG INPUT)	AN0	34	Analog Input
	1	35	
	2	36	
	3	37	
	4	38	BENDER CV
	5	39	LFO SENSE
	6	40	BENDER POLARITY
	7	41	LFO TRIGGER
PORT A	PA0	1	SWITCH READ
	1	2	
	2	3	
	3	4	
	4	5	
	5	6	
	6	7	
	7	8	
PORT B	PB0	9	DISPLAY LED DRIVE
	1	10	
	2	11	
	3	12	
	4	13	
	5	14	
	6	15	
	7	16	
PORT C	PC0	17	MIDI/SLAVE SERIAL OUTPUT
	1	18	MIDI/SERIAL INPUT
	2	19	MIDI/SLAVE CPU SELECT SIGNAL OUTPUT
	3	20	PEDAL HOLD SWITCH INPUT
	4	21	PROTECT SWITCH INPUT
	5	22	CASSETTE INTERFACE INPUT
	6	23	CASSETTE INTERFACE OUTPUT
	7	24	
PORT D (Data Bus)	PD0	55	ROM RAM ADDRESS / ROM RAM DATA / SW SCAN
	1	56	
	2	57	
	3	58	
	4	59	
	5	60	
	6	61	
	7	62	
PORT F	PF0	47	ROM ADDRESS / RAM ADDRESS
	1	48	
	2	49	
	3	50	
	4	51	
	5	52	ROM/RAM SELECT
	6	53	LED DYNAMIC SCAN & A/D MULTIPLEXER ADDRESS
	7	54	
XTAL-1		31	INPUTS FOR INTERNAL CLOCK OSCILLATOR
XTAL-2		30	
$\overline{RESET}$		28	RESET PULSE INPUT
$\overline{RD}$		44	RAM/ROM READ PULSE
$\overline{WR}$		45	RAM/LATCH WRITE PULSE
ALE		46	ADDRESS LATCH PULSE
MODE 0		29	---- 1: EXTERNAL ROM, ---- 0: INTERNAL ROM
MODE 1		27	---- 0: EXTERNAL ROM, ---- 1: INTERNAL ROM

The master CPU sends the slave CPU instructions and data to be performed by the slave through a line in serial format at 31.25 kbaud. The master also sends and receives MIDI data at 31.25 kbaud.

Although the master CPU sends out data for both MIDI OUT and the slave CPU from the same port C-0 at the same baud rate, it does not comply with MIDI specification in transmitting data to the slave CPU. The master CPU directs data to the correct route by applying a switching signal through port C-2 to IC14 gate: H for slave and L for MIDI OUT.

SWITCH READING

Master CPU IC1 on the CPU board reads 61 keyboard switches and 42 switches (Top panel, Rear panel) every 1.6ms. The CPU knows the status of the switches through the matrix consisting of 8X14; 14 times through one cycle, 8 at a time.
Scanning data from port D of IC1 is latched at IC7 outputs, and causes IC8 decoder to have sequential lows at its output pins on every negative going of G2A according to code on "C B A". The CPU reads, through port A, the keyboard switches on a "busbar" that is currently at low.
After 500μs has passed, IC1 starts reading the 42 switches in a similar way; this time through IC9 and port A.



KEYBOARD MATRIX

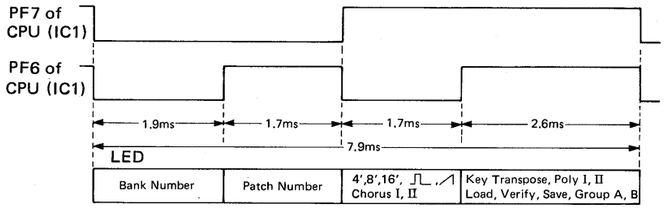
IC8 CBA	Port-A 0	1	2	3	4	5	6	7
000	C2	C#	D	D#	E	F	F#	G
001	G#	A	A#	B	C3	C#	D	D#
010	E	F	F#	G	G#	A	A#	B
011	C4	C#	D	D#	E	F	F#	G
100	G#	A	A#	B	C5	C#	D	D#
101	E	F	F#	G	G#	A	A#	B
110	C6	C#	D	D#	E	F	F#	G
111	G#	A	A#	B	C7	(C#)	(D)	(D#)

SWITCH MATRIX

IC9 CBA	Port-A 0	1	2	3	4	5	6	7
010	Bank number 1	2	3	4	5	6	7	8
011	Patch number 1	2	3	4	5	6	7	8
100	Range 16′	8′	4′	Waveform		Chorus off	1	2
101	PWM (L/M)	ENV (+/−)	VCA (E/G)	HPF (0,1,2,3)		not used		
110	KEY trans	Poly 1	Poly 2	MIDI chan	MIDI mode (1,2,3)		not used	Group SEL
111	Patch shift	Manual	Write	Save	Vrify	Load	not used	

LED LIGHTING

The LEDs in the table are lit sequentially in dynamic format.



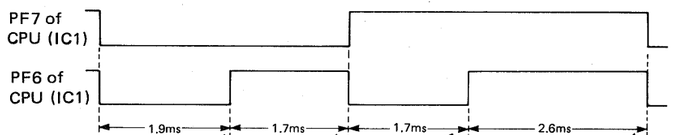
PF	Port-B							
76	0	1	2	3	4	5	6	7
00	Bank number display							
	(d)	(e)	(g)	(f)	(dp)	(c)	(b)	(a)
01	Patch number display							
	(d)	(e)	(g)	(f)	(dp)	(c)	(b)	(a)
10	Range			Waveform		not	Chorus	
	16'	8'	4'	⎍	⟋	used	1	2
11	KEY trans	Poly 1	Poly 2	Save	Vrify	Load	Group A	Group B

POTENTIOMETER & BENDER READINGS

Multiplexers IC1 and IC4 combine 16 pots VR1–VR16 into four channels and connect them to AN0–AN3 of CPU IC1 as shown below. To AN4–AN7 connect directly outputs from Bender Board Pots.

Two analog parameter groups - - - AN0–AN3 and AN4–AN7 are accomodated independently by two A/D converters in IC1.

NOTE: The master CPU does not transmit information coming through AN4–AN7 to the slave but to MIDI OUT. The bender outputs are also read by the slave CPU for use to control Juno-106 proper.



	Pots Reading-1	Pots Reading-2	Pots Reading-3	Pots Reading-4		Bender Reading
AN-3	LFO Rate	PWM	Delay	DCO LFO	AN-7	LFO Trig.
AN-2	Noise	Frequency	Resonance	Sub OSC	AN-6	Bender Polarity
AN-1	VCF ENV	VCA Level	VCF LFO	VCF KYBD	AN-5	LFO Sensitiv
AN-0	Decay	Sustain	Release	Atrack	AN-4	Bender CV

KEY ASSIGNMENT

The master CPU IC1 contains two key buffers in internal RAM: one for MIDI keys and one for built-in keyboard; each buffer maps (stores) the On/Off events of keys as they are played on the associated keyboad.

The master CPU performs logical inclusive OR of these two maps at an interval and takes necessary steps whenever the OR output of a particular note shows a difference from that of the preceding cycle.

a) When OFF to ON (a new key pressed) transition, the master CPU informs the slave CPU (on the Module board) of the note value, note ON and a module to be assigned to the key.

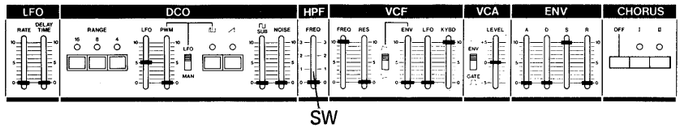
b) When ON to OFF (a key released), instructs the slave to free the voice from the key.

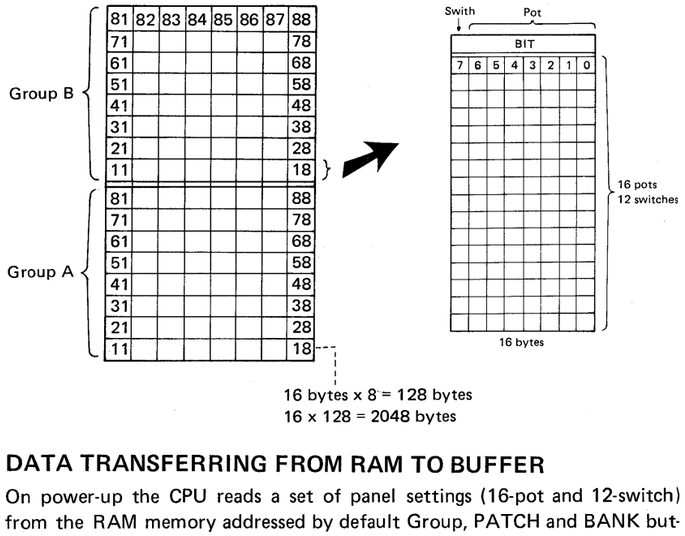
This OR sysstem allows MIDI and built-in keyboard to be played simultaneously. However, the system does not generate retrigger pulse, that is, when a key is already held down, pressing the same key on the other keyboard has no effects to the voice.

The master transmits data including the above to the slave in serial format and lets the slave works accordingly.

RAM & PARAMETER BUFFER

IC13 of CPU board is a 2048-byte RAM which is capable of storing 128 batches (128 presets). The address map below illustrates how 16-pot parameters and 12-switch status (on the front panel) for a particular preset voice are stored in the RAM.





DATA TRANSFERRING FROM RAM TO BUFFER

On power-up the CPU reads a set of panel settings (16-pot and 12-switch) from the RAM memory addressed by default Group, PATCH and BANK buttons. The CPU then writes this data into an internal buffer called Parameter Buffer.

Whenever another Group, BANK or PATCH button is selected, the CPU replaces contents in the buffer with the new ones that are read from the RAM; the CPU also sends the information to the slave CPU on the Module board to make new setting effective on the voice(s).

EDIT

The master CPU updates the parameter buffer upon receiving outputs from editable controls and switches (on the panel) or upon recognizing messages (MIDI FUNCTION set in III).

WRITING INTO RAM

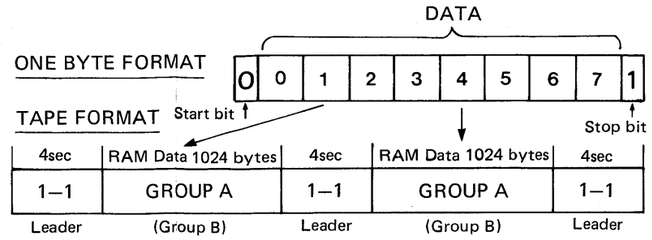
When a writing procedure is performed on the panel, the master CPU writes the contents in the buffer into the RAM, renewing RAM data to the edited values.

RAM ADDRESS, RAM SELECTION

To gain access to 2048-byte memories in the RAM, 11 address lines are required (2^{11}=2048). In addition to lower 8 bits provided by address latch IC6, higher 3 bits are supplied from CPU port F (PF0–PF2). Selection between RAM and ROM is established by PF5.

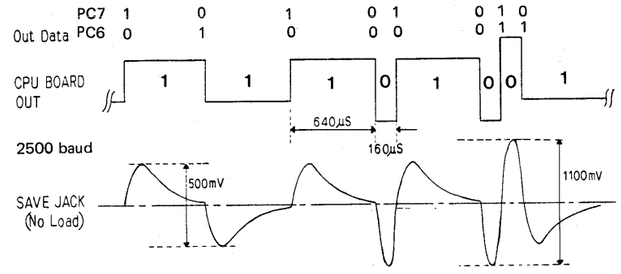
TAPE INTERFACE

The data transferring between JUNO-106 tape interface and the tape are to be configured as follows:



SAVE

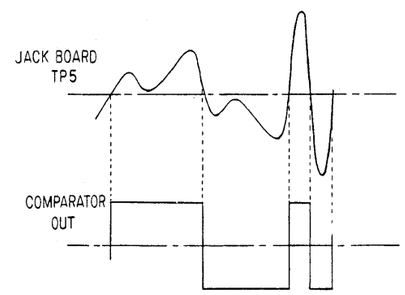
During the SAVE routine data of 1024 bytes (data group) are sent out twice from PC6 and PC7 of the master CPU. Each data is represented in 2-bit code that is selected between two available codes depending on values of the adjacent data. This selectable code arrangement makes every data distinct from the neighbors when converted into analog form at R22, 23 and 24.



LOAD

The audio waveform from the tape coming into Jack board is first differentiated and smoothed through IC12a and IC13b and converted to a rectangular (pulse) at IC13a output. The pulse is then applied through PC5 to the master CPU which measures the period of the pulse by detecting level changes (edges). The CPU recognizes the waveform as a useful data when the period is: a) less than 416μs as a 0 and b) within 416–960μs as a 1.

The CPU will cease Load routine when it correctly reads entire 1024-byte data group. The following conditions will cause the CPU to issue an error indication:



A byte is constructed in incorrect format.

Pass word recorded on the tape before the actual data is not found.

Checksum indicates unequal answer.

Length of the half-period is more than 960μs.

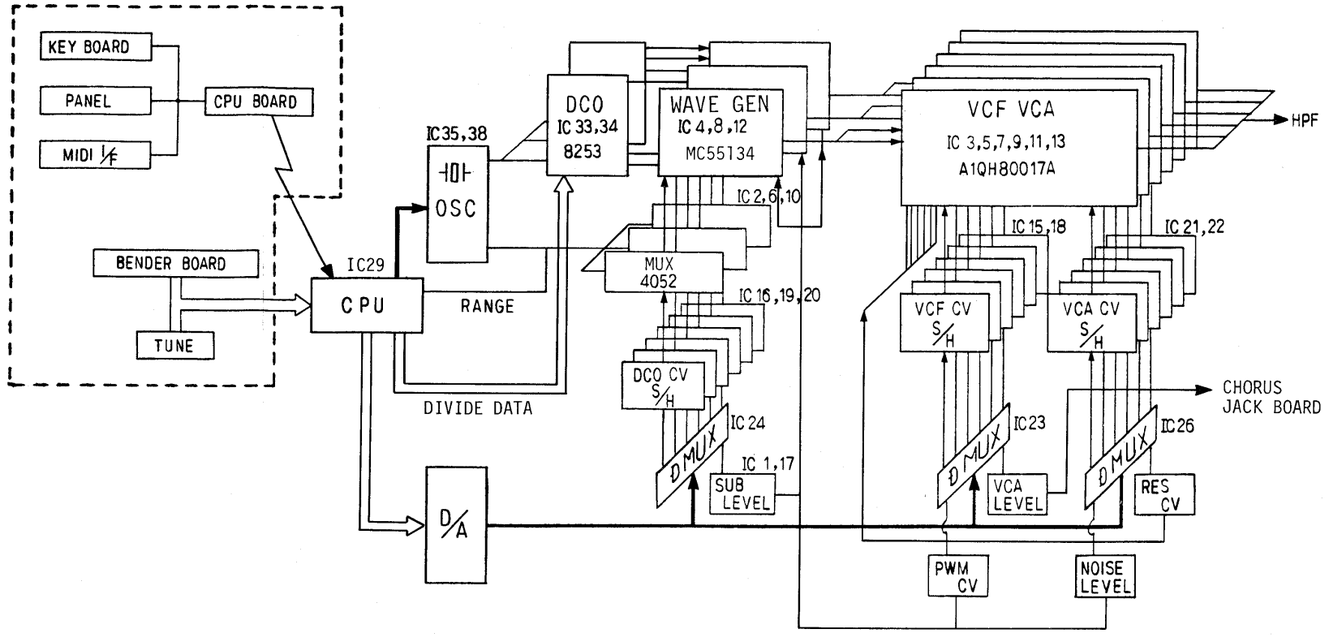
VERIFY

Verify circuitry and program work in similar way as in LOAD except that the 1024-byte data is checked against data in the RAM. In this case descrepancy between RAM and the tape is added to error conditions mentioned in the above LOAD routine.

MODULE BOARD

Slave CPU μPD7810/7811

DESIGNATION		PIN NO.	FUNCTION
AN (ANALOG INPUT)	AN0	34	TUNE
	1	35	PORTAMENTO
	2	36	LFO TRIGGER SWITCH
	3	37	LFO SENSE (DEPTH)
	4	38	BENDER VCF SENSE
	5	39	BENDER VCO SENSE
	6	40	BENDER POLARITY
	7	41	BENDER CV
PORT A	PA0	1	S/H DEMULTIPLEXER CHANNEL SELECT
	1	2	
	2	3	
	3	4	NOT USED
	4	5	S/H DEMULTIPLEXER CHIP SELECT — DCO CV
	5	6	VCF CV
	6	7	VCA CV
	7	8	NOT USED
PORT B	PB0	9	D/A CONVERTER DATA OUT (UPPER 6 BITS)
	1	10	
	2	11	
	3	12	
	4	13	
	5	14	NOT USED
	6	15	
	7	16	
PORT C	PC0	17	NOT USED
	1	18	SERIAL DATA RECEIVE LINE (FROM CPU BOARD)
	2	19	D/A CONVERTER DATA OUT (LOWER 6 BITS)
	3	20	
	4	21	
	5	22	
	6	23	
	7	24	
PORT D	PD0	55	ADDRESS LSB 8 BITS DATA OUT
	1	56	
	2	57	
	3	58	
	4	59	
	5	60	
	6	61	
	7	62	
PORT F	PF0	47	ADDRESS MSB 6 BITS
	1	48	
	2	49	
	3	50	
	4	51	
	5	52	
	6	53	RANGE SELECT
	7	54	
XTAL-1		31	12MHz CLOCK INPUT
XTAL-2		30	
$\overline{\text{RESET}}$		28	RESET PULSE INPUT
$\overline{\text{RD}}$		44	ROM READ TIMING PULSE
$\overline{\text{WR}}$		45	8253 LATCH WRITE TIMING PULSE
ALE		46	ADDRESS LATCH TIMING PULSE
MODE 0		29	---- 1: EXTERNAL ROM, ---- 0: INTERNAL ROM
MODE 1		27	---- 0: EXTERNAL ROM, ---- 1: INTERNAL ROM



OSC, DCO

OSC

The oscillator consists of a master oscillator (8MHz) and a divider IC35. The IC35 divides 8MHz by two, four or eight according to a position of RANGE (4', 8', 16') on the panel and feeds it to DCOs IC33 and IC34 which are 16-bit Programmable Interval Timers.

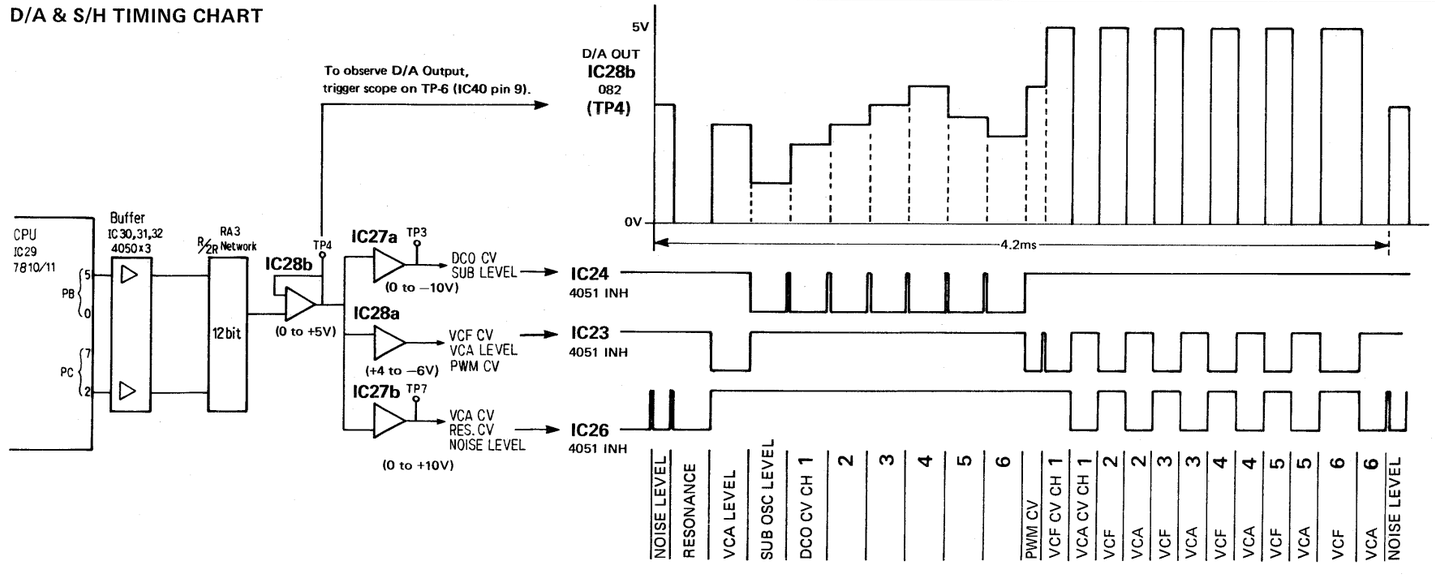
DCO

Each of three counters in one Timer divides OSC frequency by a number defined by a divide data represented on the data bus of the slave CPU IC29. The divide data is the sum of a key number and the outputs from LFO, Bender, Portamento and Tune for a particular note. The resultant at the output of each counter will be a rectangular of audio frequency.

D/A CONVERTER

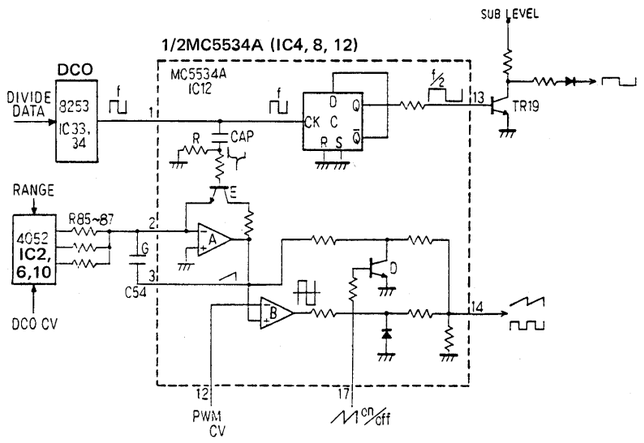
In controlling voices the slave CPU does not output each parameter independently, rather, it integrates some of parameters that are needed for a particular destination (DCO, VCF or VCA) and represents them as a 12-bit data (upper 6 bits at PB0—PB5 and lower 6 bits at PC2—PC7). The data is converted into an analog voltage which is conditioned and routed to the destination module from the demultiplexer (IC23, 24 or 26) as shown below.

D/A & S/H TIMING CHART



Note that the select code and INH for IC26 are level shifted at IC25 output. This is because that IC26 operates from ± 15V.

WAVE GENERATOR



MC5534 (IC 4, 8 and 12) is, with a given rectangular at CLK IN, capable of generating three different waveforms; divided by two rectangular, sawtooth and variable-width rectangular (Pulse Width Modulated). There are three versions in MC5534 series; of these MC5534A is the latest version containing complete two identical circuits. See Parts Change Notes in the Parts List section for detail.

SUB OSCILLATOR

This is self-explaining from the figure. The output amplitude being variable to a change of collector supply voltage (SUB LEVEL).

SAWTOOTH

For sawtooth and PWM waveforms, DCO CV is applied from the slave CPU in addition to DCO output.

The DCO CV will keep the sawtooth and pulse amplitude nearly constant (approx. 12Vp-p) over the frequency range (detailed later). Therefore, DCO CV includes LFO, BENDER, PORTAMENTRO and TUNE data as well as key value, but it does not contain RANGE data; the DCO CV sees RANGE at the output of 4052 (IC2, 6 or 10) which selects among R85, 86 and 87 in accordance with RANGE code (PF6 and 7 of the slave CPU). The DCO CV charges C54 through R85 (if 16') and discharges through transistor E on the positive going edges of DCO. If the RC time constant (C54 and R85, 86 or 87) remains unchanged, sawtooth amplitude becomes low at 4'. The same principle applies to key range over the keyboard; the output amplitude decreases as the note runs high. Therefore, DCO CV is made to become higher in proportion to key number.

PULSE MODULATED WAVE

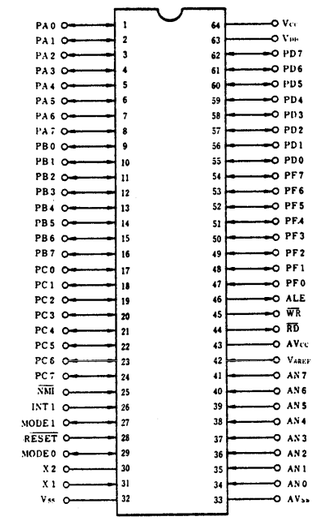
At ICB input, sawtooth wave is compared with PWM CV that determines the pulse duratation of ICB output; duty ratio is 50% at +6V PWM CV and 95% at +0.6V. With PWM OFF, PWM CV is −0.8V; this can swing and keep ICB output to High, disabling the rectangular.

VCF, VCA

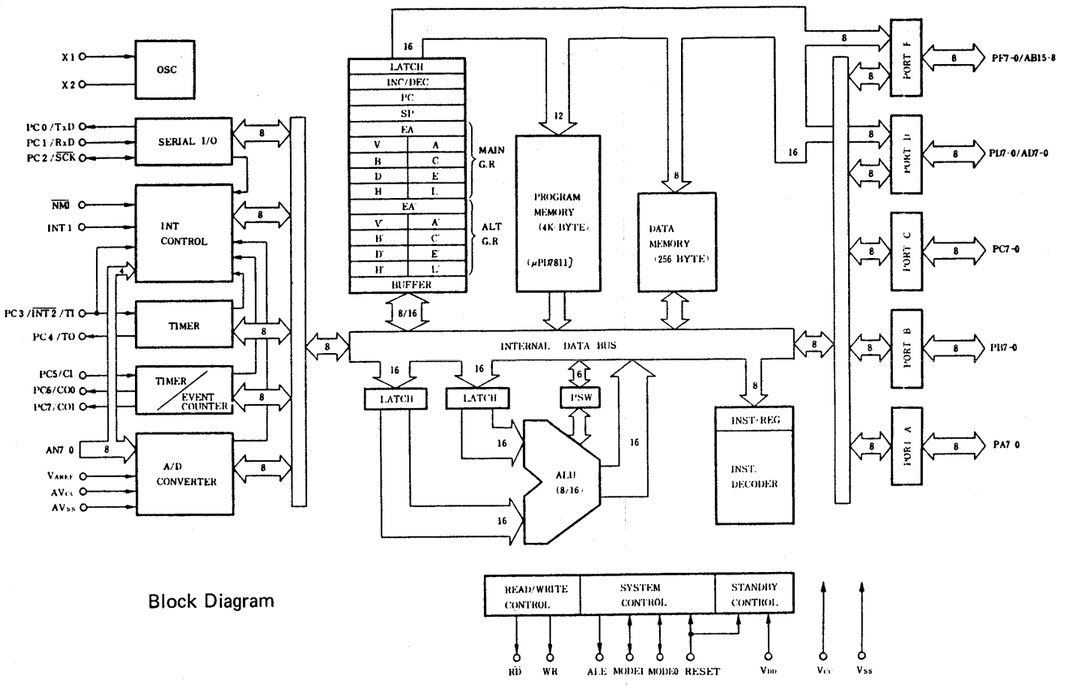
A1QH80017A is a one-chip VCF and VCA. Both VCF and VCA are individually controlled by the several parameters integrated into one voltage: VCF CV contains CUT OFF (VCF) frequency, ENV, LFO, Key follow and Bender; VCA CV includes ENV and GATE.

IC DATA

μPD7810G/μPD7811G



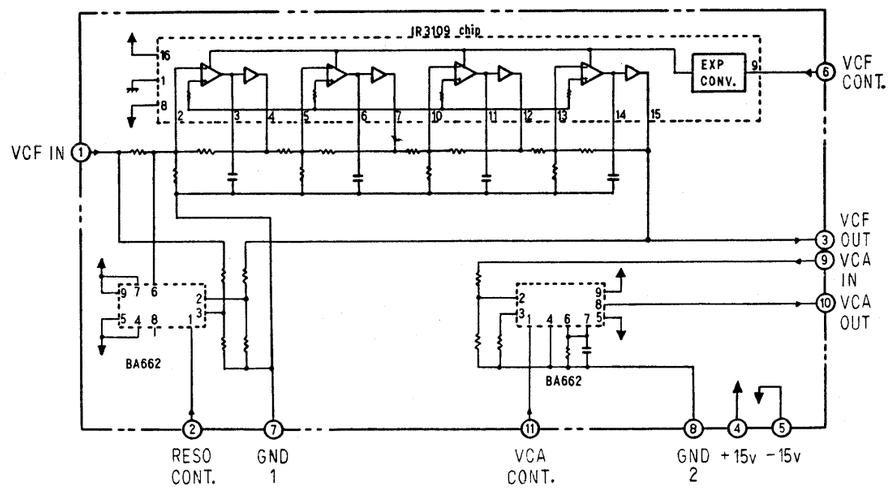
Pin Configuration



Block Diagram

A1QH800170, A1QH80017A

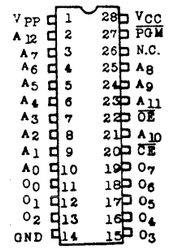
VCF VCA

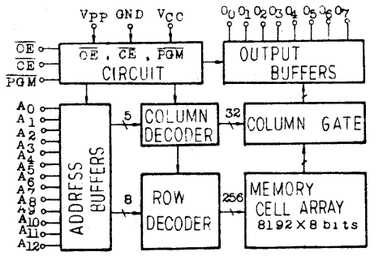


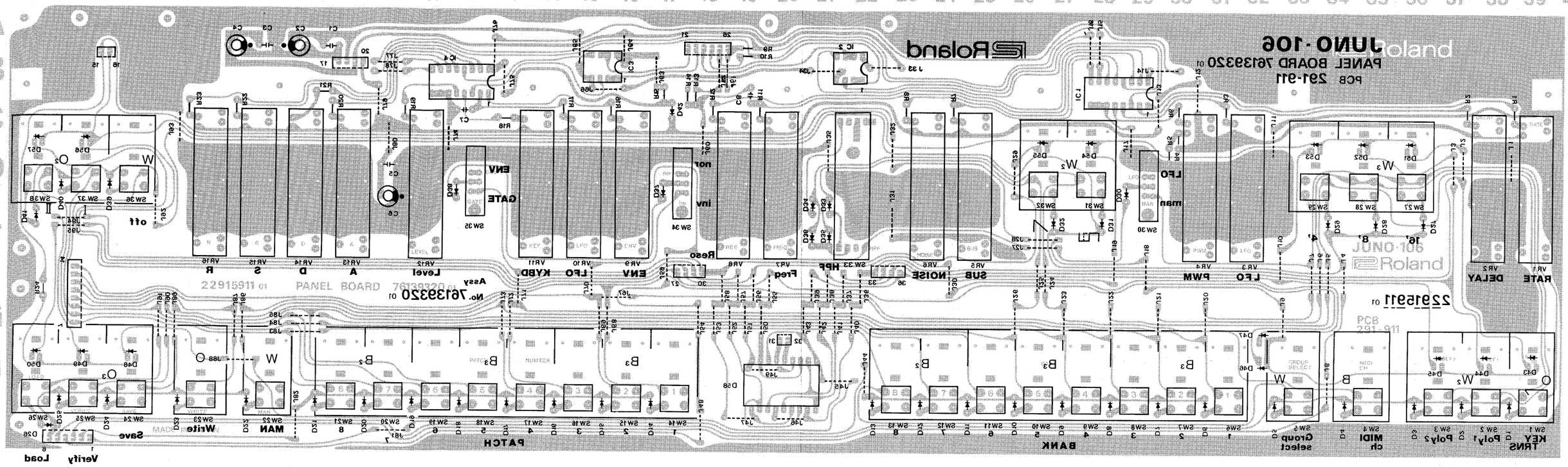
TMM2764D

64k-Bit EPROM

Pin Configuration

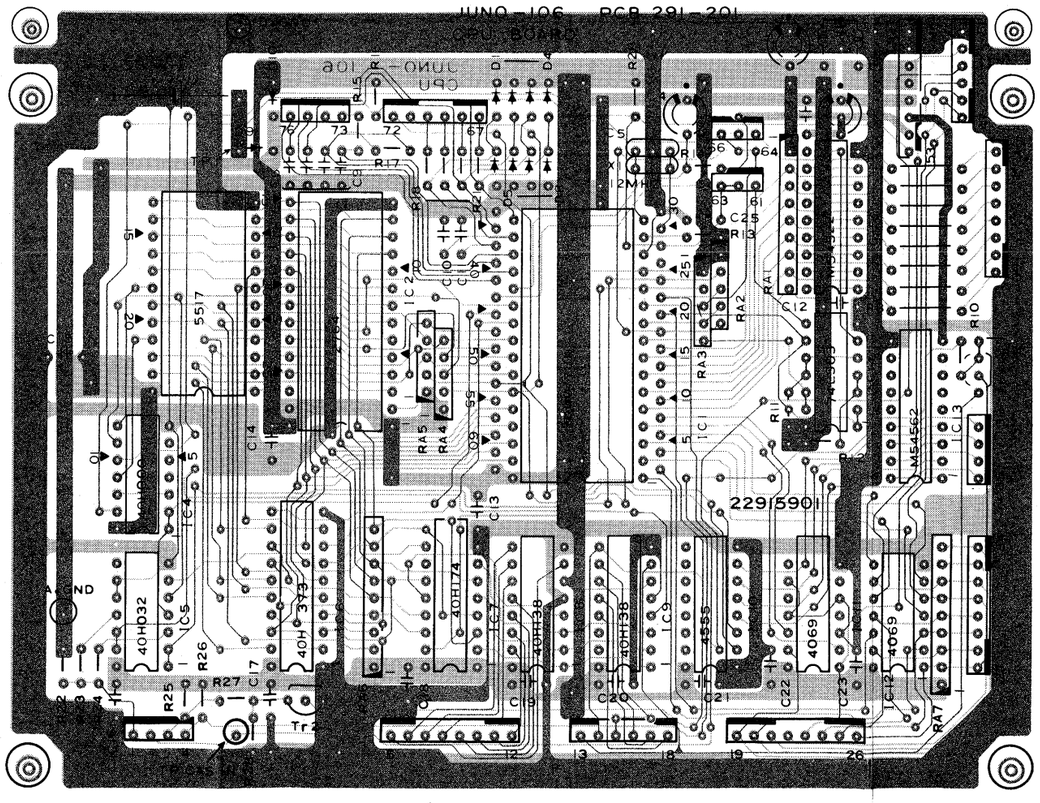






↑ PANEL BOARD
76139320
(pcb 22915911)

View from foil side



CPU BOARD →
76139140
(pcb 22915901)

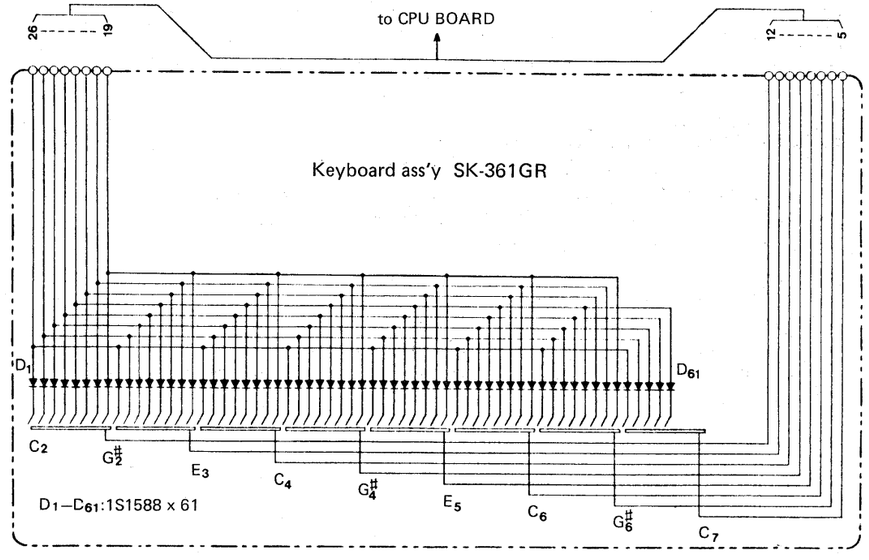
NOTE: BACKUP CIRCUITRY/BATTERY (CPU BOARD)

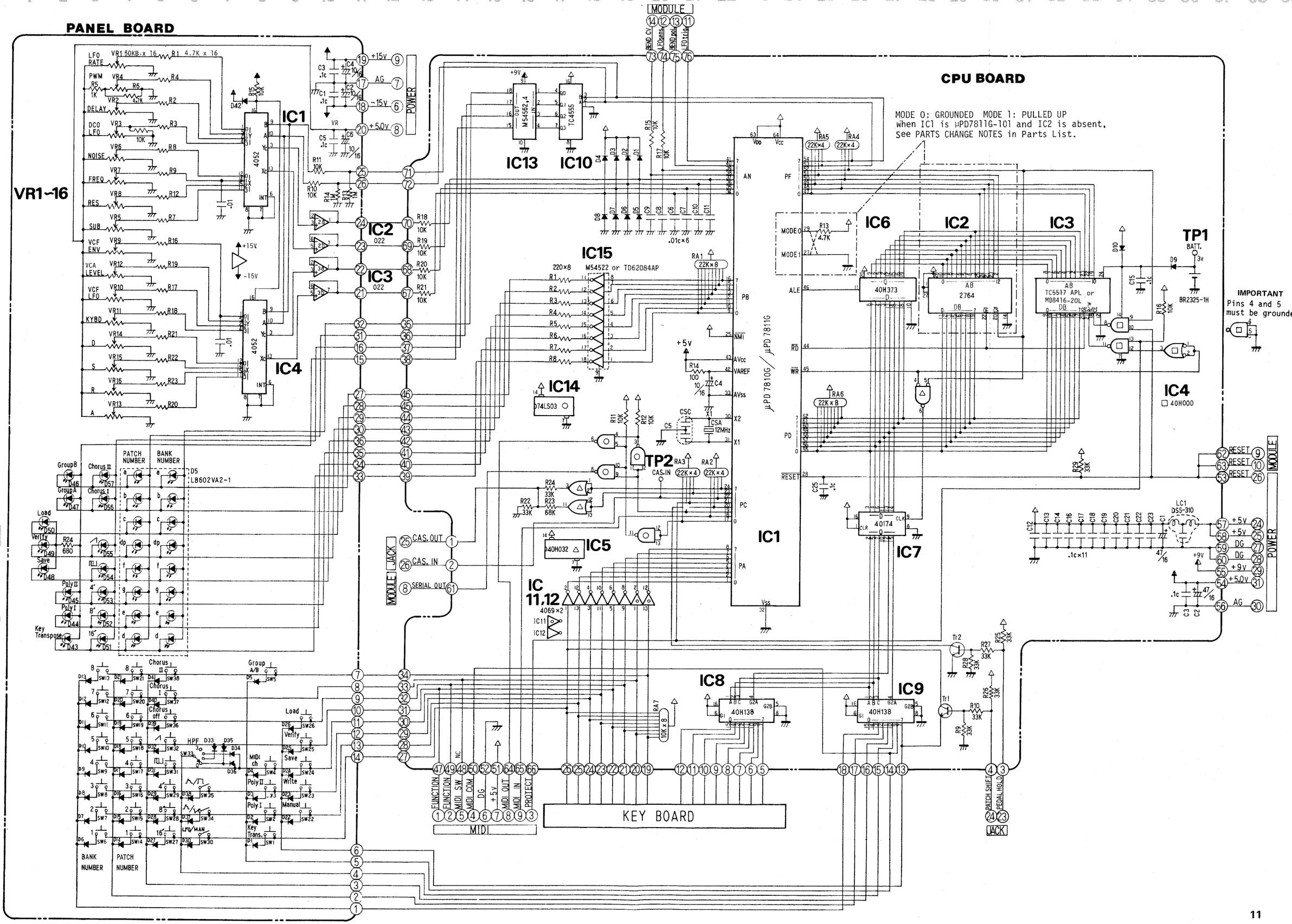
GROUNDING IC4 OPEN TERMINALS

— Mandatory On Units with Serial Numbers Up To 439000 —
To insure a longer battery life, short together IC4's pins 4, 5 and 7 (or a DG terminal) of the CPU board.
In practice, first connect a jumper wire to a digital GROUND and then to pins 4 and 5 to protect IC4 against static charges.

REPLACING BATTERY

Also replace the battery that cannot supply more than 2.8V under installed condition.
In replacing, be sure to observe polarity of the battery.
After mounting, check the voltage; it must be more than 3V.

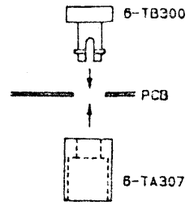



PANEL BOARD
VR1~16
LFO RATE
PWM
DELAY
DCO LFO
NOISE
FREQ
RES
SUB
VCF ENV
VCA LEVEL
VCF LFO
KYBD
D
S
R
A
VR1 50KB×16
R1 4.7K×16
IC1
IC2
IC3
IC4
4052
022
+15V
-15V
POWER
AG
MODULE
BEND CV
LFOsens
BEND pol
LFO trig
IC13
IC10
M54562,4
TC4555
CPU BOARD
MODE 0: GROUNDED MODE 1: PULLED UP
When IC1 is μPD7811G-101 and IC2 is absent.
See PARTS CHANGE NOTES in Parts List.
IC6
IC2
IC3
TP1
BATT.
3v
BR2325-1H
IMPORTANT
Pins 4 and 5
must be grounded.
IC15
220×8
M54522 or TD62084AP
IC14
74LS03
IC4
40H000
μPD 78106 / μPD 78116
IC1
IC5
40H032
IC7
40174
IC 11,12
4069×2
IC11
IC12
IC8
40H138
IC9
TP2
CAS.IN
CSC
CSA
12MHz
RESET
PATCH NUMBER
BANK NUMBER
LB602VA2-1
Group B
Group A
Load
Verify
Save
Poly II
Poly I
Key Transpose
Chorus II
Chorus I
Chorus off
HPF
LFO/MAN
MIDI ch
Group A/B
Write
Manual
Key Trans.
BANK NUMBER
PATCH NUMBER
MODULE JACK
CAS. OUT
CAS. IN
SERIAL OUT
MIDI
FUNCTION
FUNCTION
MIDI SW
NC
MIDI COM
DG
+5V
MIDI OUT
MIDI IN
PROTECT
KEY BOARD
PATCH SHIFT
PEDAL HOLD
JACK
LC1
DSS-310
POWER
+5V
DG
+9V
AG

MODULE BOARD

76139170

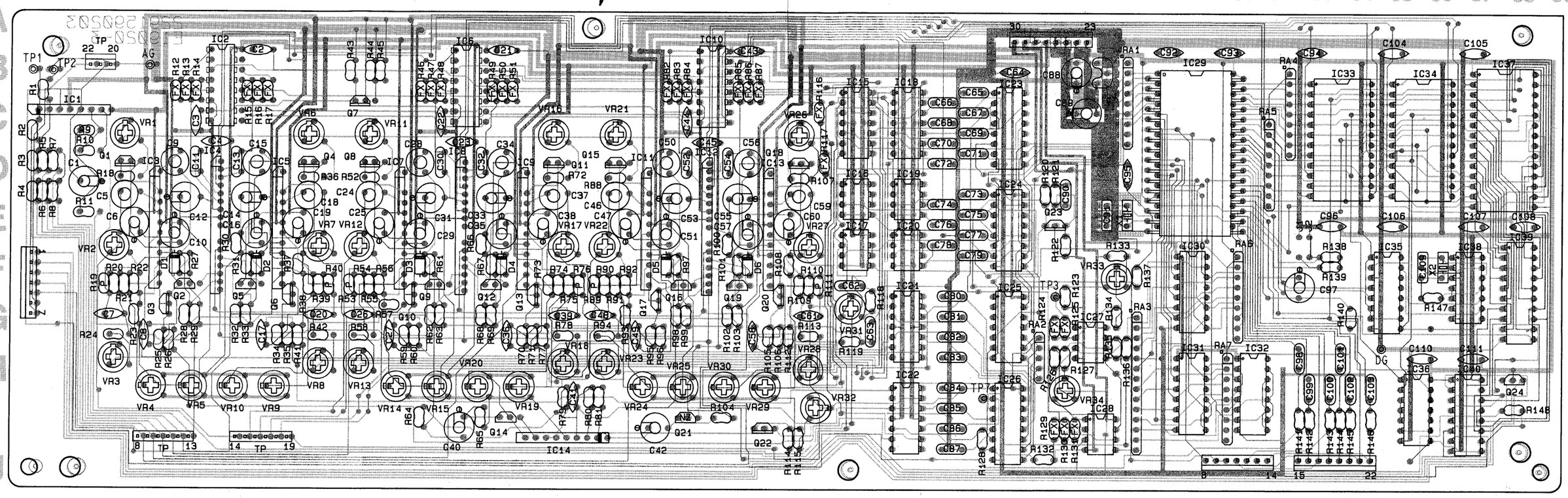
(pcb 22915902)



Resistor R20J
Metal oxide film resistor 1% 100ppm
Posistor (560 ohm)
Ceramic capacitor
Mylar
Electrolyte capacitor
Non-polar electro capacitor

Transistor 2SC-1815-Y or -1815-GR
Transistor 2SA-1015-Y or -1015-GR
Transistor 2SC-945P (selected for noise generator)
Diode 1SS-133

Trimmer pot. H0615C119
472: 4.7K 103: 10K 223: 22K
473: 47K 104: 100K



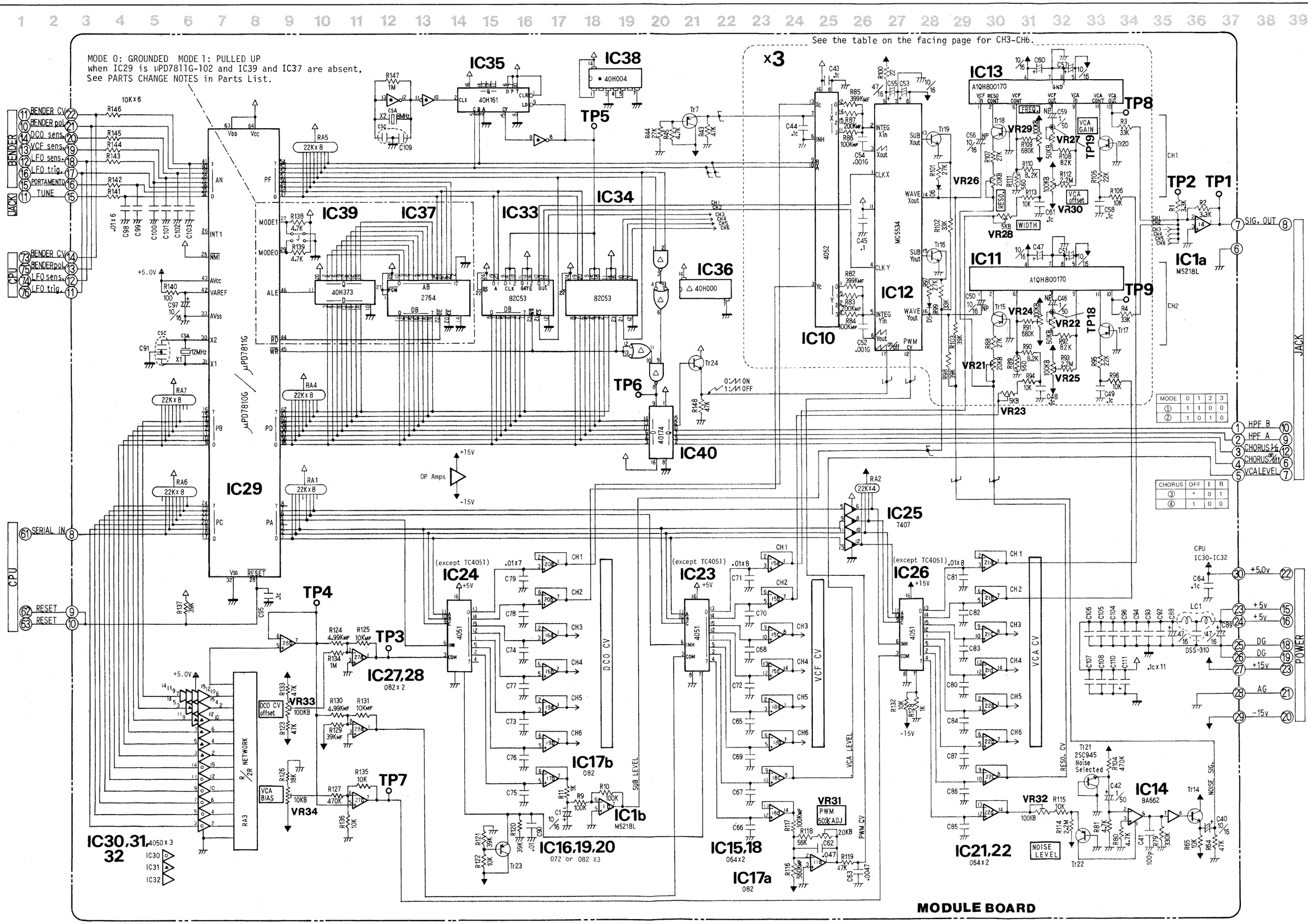
PCB 291-902
2291590203

PARTS DESIGNATION

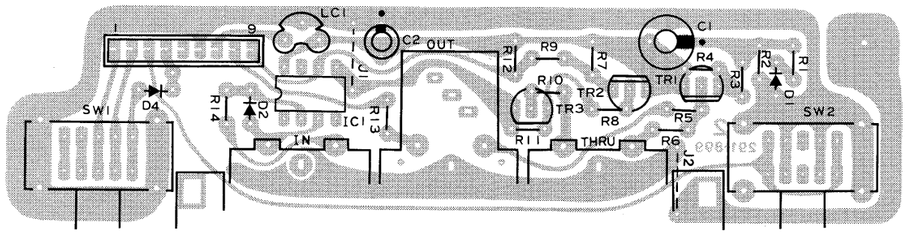
(in Dotted line, Schematic Diagram)

CH1	R87	R86	R85	IC10.X	C43	C44	C53	R100	C55	C53	C45	Tr19	R101	D6	R102	R103	IC12	IC13	C56	Tr18	R107	VR26	R109	VR29	R110	R113	C61	VR28	C59	VR27	R108
CH2	R83	R84	R82	IC10.Y			C52					Tr16	R97	D5	R99	R98		IC11	C50	Tr15	R88	VR21	R91	VR24	R90	R94	C48	VR23	C46	VR22	R92
CH3	R51	R50	R49	IC6.X	C21	C22	C32	R66	C33	C31	C23	Tr12	R67	D4	R68	R69	IC8	IC9	C34	Tr11	R72	VR16	R74	VR19	R75	R78	C39	VR18	C37	VR17	R73
CH4	R47	R48	R46	IC6.Y			C30					Tr9	R61	D3	R63	R62		IC7	C28	Tr8	R52	VR11	R55	VR14	R54	R58	C26	VR13	C24	VR12	R56
CH5	R17	R16	R15	IC2.X	C2	C3	C13	R30	C14	C12	C4	Tr5	R31	D2	R32	R33	IC4	IC5	C15	Tr4	R36	VR6	R38	VR9	R39	R42	C20	VR8	C18	VR7	R37
CH6	R13	R14	R12	IC2.Y			C11					Tr2	R27	D1	R29	R28		IC3	C9	Tr1	R18	VR1	R21	VR4	R20	R24	C7	VR3	C5	VR2	R22

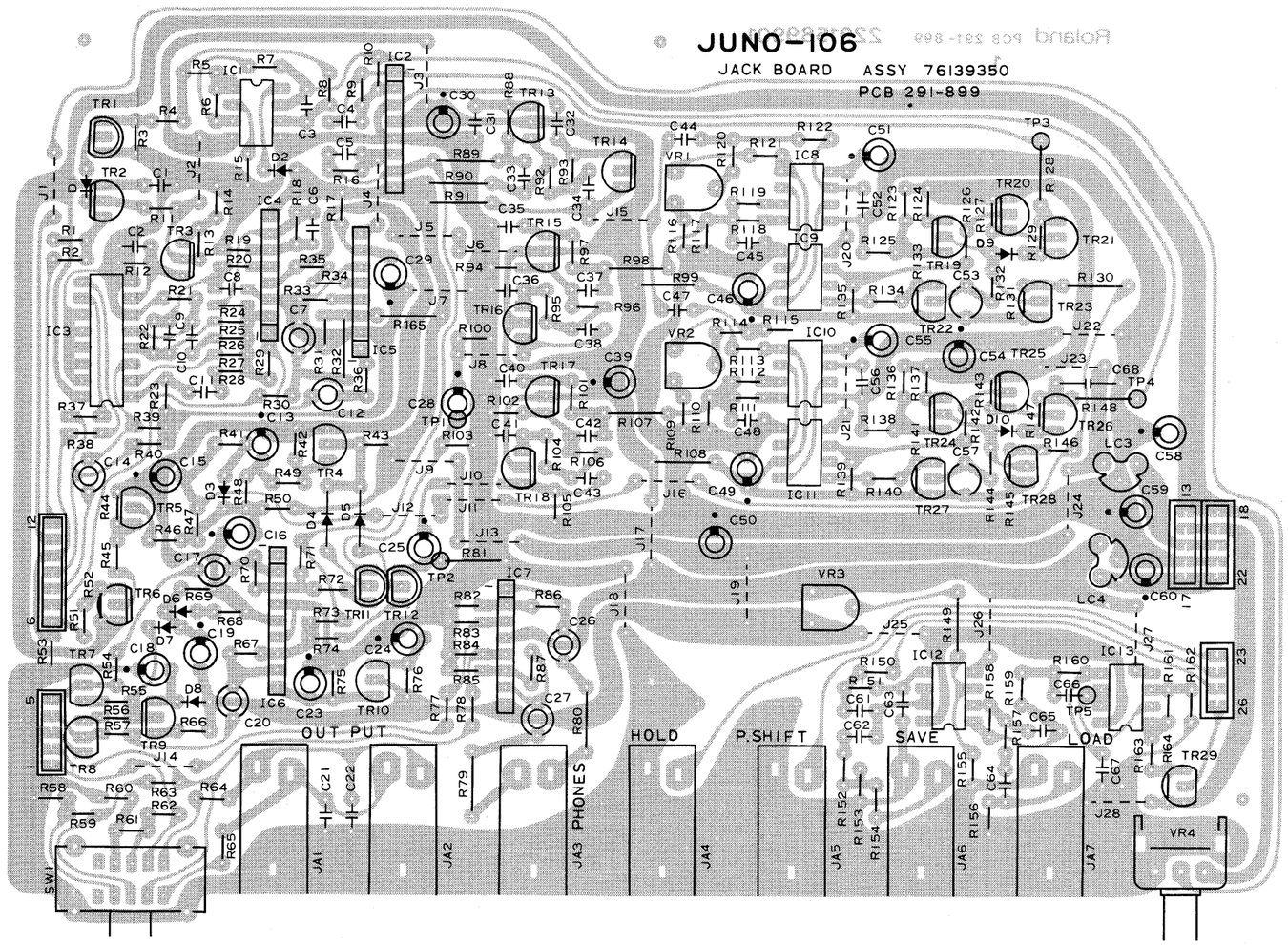
CH1	R111	R112	VR30	Tr20	R105	R106	C58	R3	C60	C57	TP19	TP8
CH2	R89	R93	VR25	Tr17	R95	R96	C49	R4	C47	C51	TP18	TP9
CH3	R76	R77	VR20	Tr13	R70	R71	C36	R5	C38	C35	TP17	TP10
CH4	R53	R57	VR15	Tr10	R59	R60	C27	R6	C25	C29	TP16	TP11
CH5	R40	R41	VR10	Tr6	R34	R35	C17	R7	C19	C16	TP15	TP12
CH6	R21	R23	VR5	Tr3	R25	R26	C8	R8	C6	C10	TP14	TP13

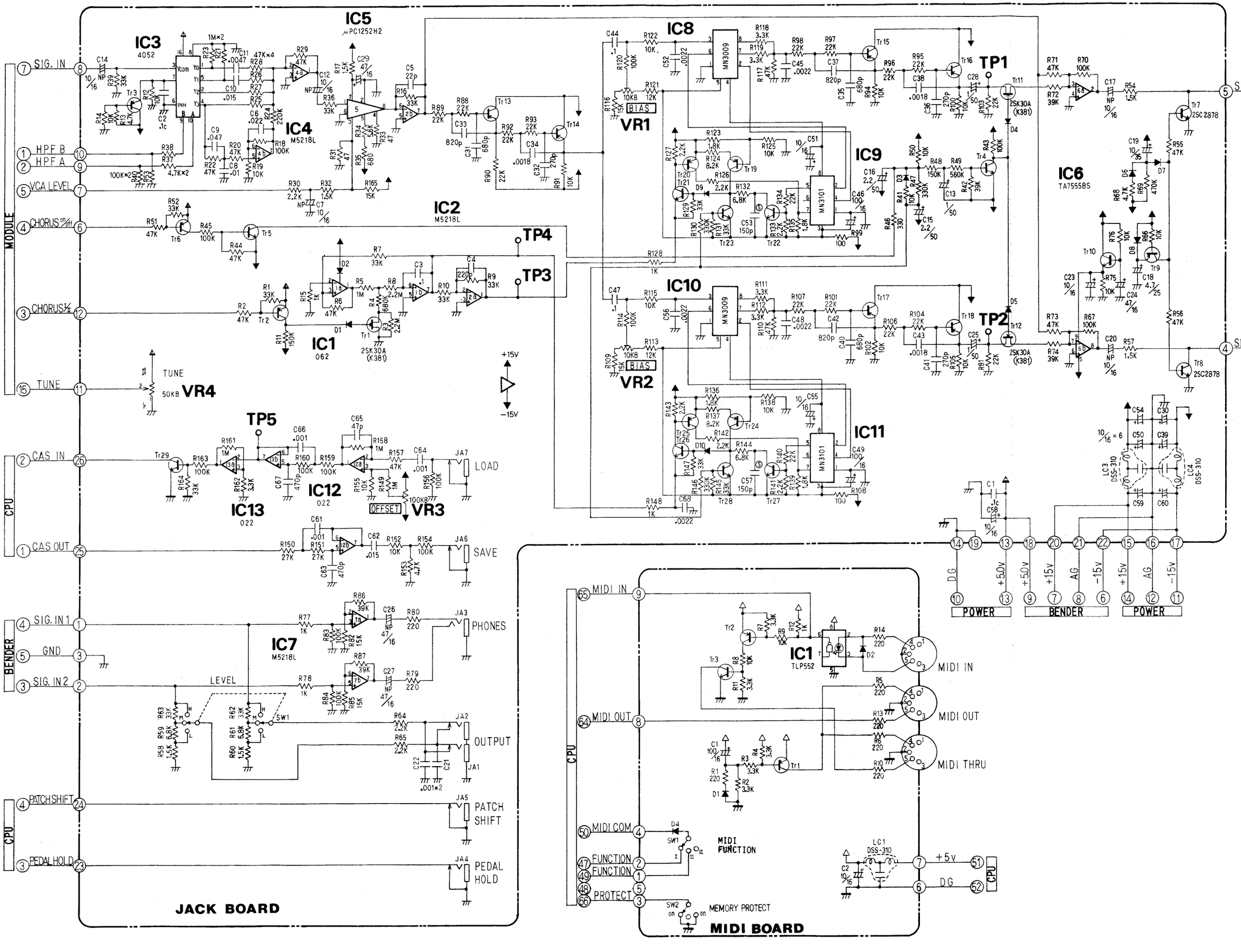

MODE 0: GROUNDED MODE 1: PULLED UP
When IC29 is μPD7811G-102 and IC39 and IC37 are absent.
See PARTS CHANGE NOTES in Parts List.
See the table on the facing page for CH3-CH6.
x3
IC35
IC38
TP5
IC34
IC39
IC37
IC33
IC36
IC40
TP6
IC29
μPD7811G
μPD7810G
TP4
TP3
IC27,28
082 x 2
IC24
IC23
IC26
IC25
7407
IC13
IC11
IC12
IC10
MC5534
4052
TP8
TP9
TP2
TP1
IC1a
M5218L
IC1b
M5218L
IC17b
082
IC16,19,20
072 or 082 X3
IC15,18
064 x 2
IC17a
082
IC21,22
064 x 2
IC14
BA662
IC30,31,32
4050 x 3
BENDER
JACK
CPU
BENDER CV
BENDER pol
DCO sens.
VCF sens.
LFO sens.
LFO trig.
PORTAMENTO
TUNE
SERIAL IN
RESET
SIG. OUT
HPF B
HPF A
CHORUS 1st
CHORUS 2nd
VCA LEVEL
DCO CV
VCF CV
VCA CV
PWM CV
RESO. CV
NOISE SIG.
POWER
MODE 0 1 2 3
① 1 1 0 0
② 1 0 1 0
CHORUS OFF I II
③ * 0 1
④ 1 0 0
MODULE BOARD

MIDI BOARD
76139380
(pcb 22915899)

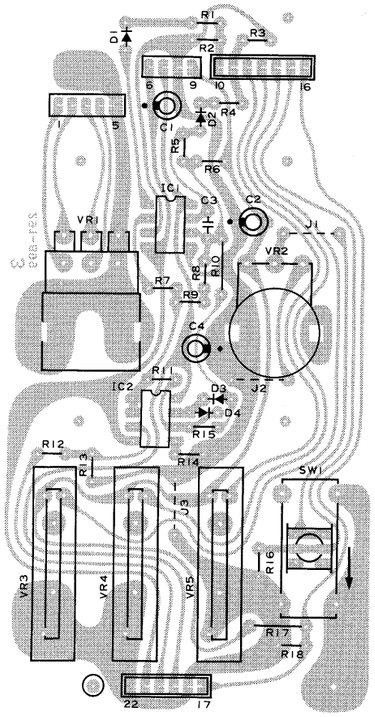


JACK BOARD
76139350
(pcb 22915899)

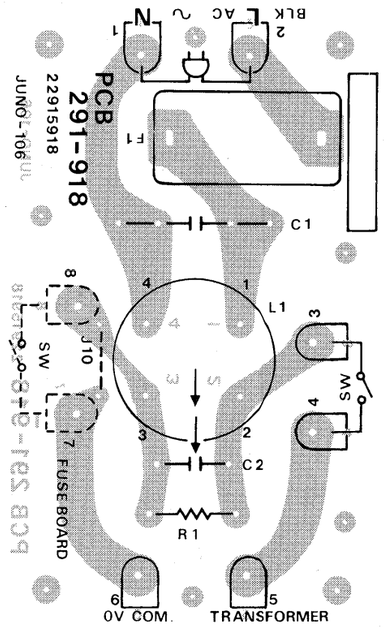



IC5
μPC1252H2
IC3
4052
IC4
M5218L
IC2
M5218L
IC1
062
IC8
MN3009
IC9
MN3101
IC10
MN3009
IC11
MN3101
IC6
TA75558S
IC7
M5218L
IC12
022
IC13
022
TP1
TP2
TP3
TP4
TP5
VR1
VR2
VR3
VR4
BIAS
OFFSET
TUNE
50KB
+15V
−15V
MODULE
SIG. IN
HPF B
HPF A
VCA LEVEL
CHORUS
TUNE
CPU
CAS IN
CAS OUT
PATCH SHIFT
PEDAL HOLD
BENDER
SIG. IN 1
GND
SIG. IN 2
LEVEL
SW1
SIG. OUT1
SIG. OUT2
LOAD
SAVE
PHONES
OUTPUT
PATCH SHIFT
PEDAL HOLD
JACK BOARD
MIDI IN
MIDI OUT
MIDI COM
FUNCTION
FUNCTION
PROTECT
MIDI THRU
MIDI FUNCTION
MEMORY PROTECT
SW2
MIDI BOARD
POWER
BENDER
POWER
DG
+5.0v
+5.0v
+15v
AG
−15v
+15v
AG
−15v
+5v
DG

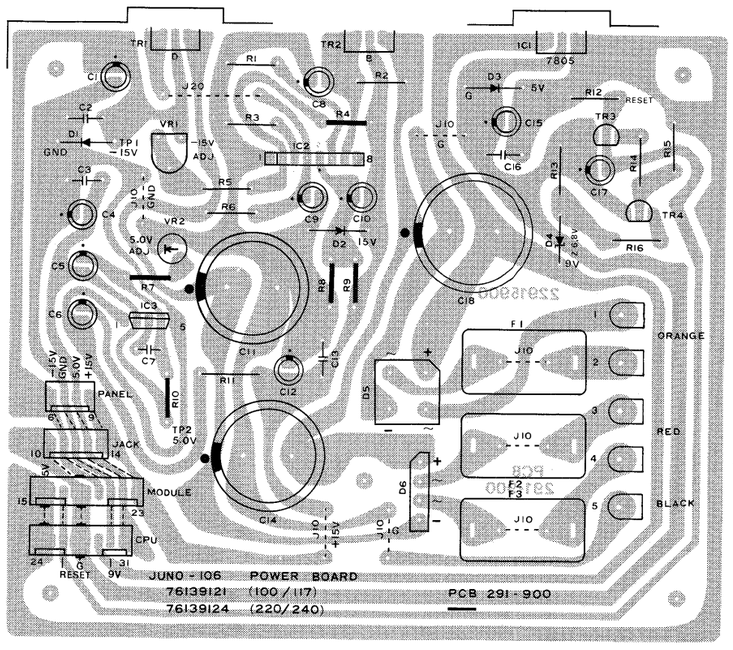
BENDER BOARD
76139410 (pcb 22915899)

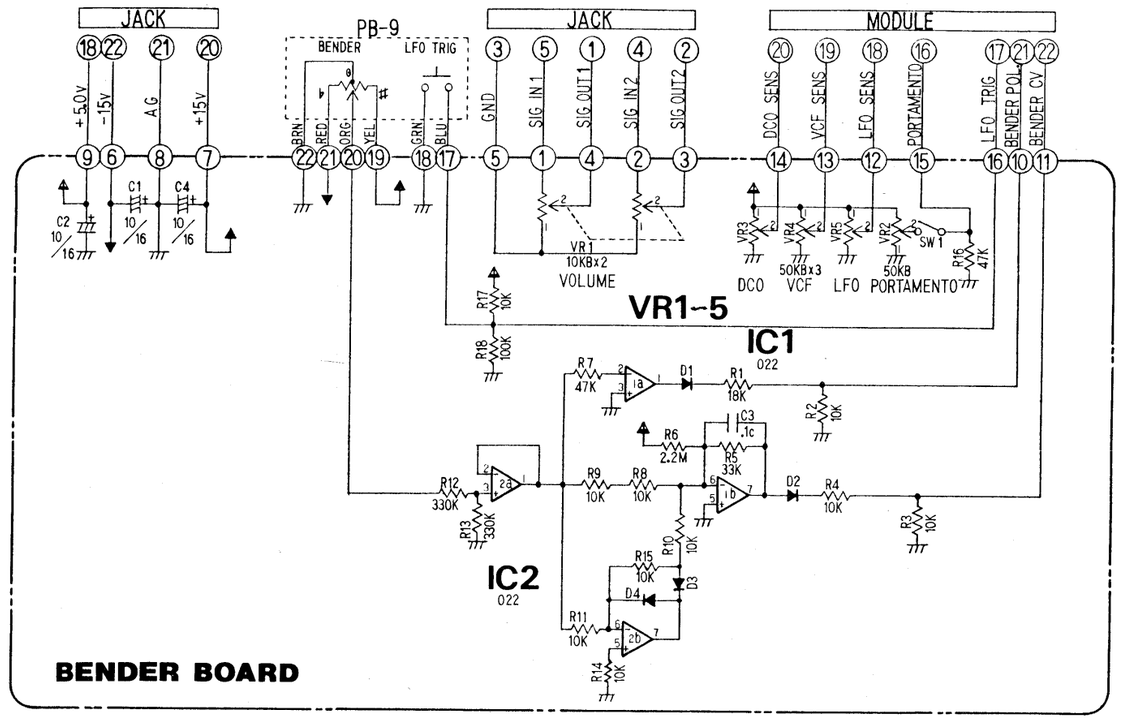


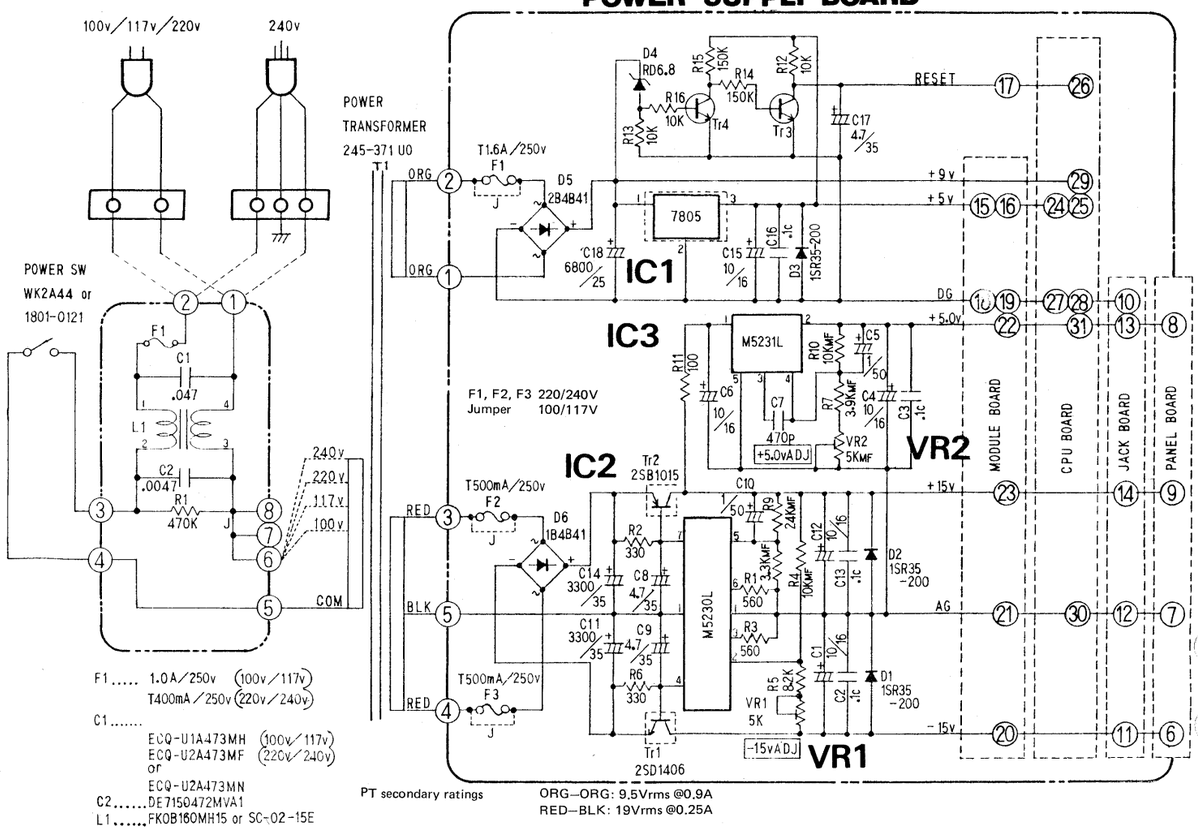
FUSE BOARD
76139111 100/117V (pcb 22915981)
76139114 220/240V (pcb 22915981)



POWER SUPPLY BOARD
76139121 100/117V
(pcb 22915900)
76139124 220/240V
(pcb 22915900)





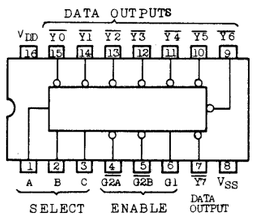


IC DATA

TC40H138P

3-to-8 Line Decoder/Demultiplexer

Pin Configuration



Truth Table

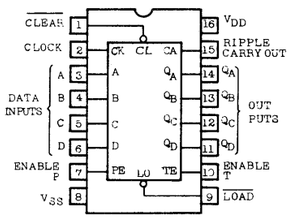
INPUTS						OUTPUTS							
ENABLE			SELECT										
G1	$\overline{G2A}$	$\overline{G2B}$	A	B	C	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
L	※	※	※	※	※	H	H	H	H	H	H	H	H
※	H	※	※	※	※	H	H	H	H	H	H	H	H
※	※	H	※	※	※	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	H	L	L	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	L	H	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

※ : Don't care

TC40H161P

Synchronous Presettable 4-bit Counter

Pin Configuration



Truth Table

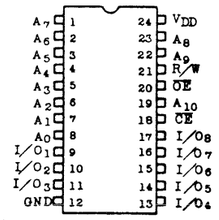
INPUTS										OUTPUTS				
CLEAR	LOAD	ENABLE P	ENABLE T	CLOCK	DATA INPUTS A	B	C	D		DATA OUTPUTS Q_A	Q_B	Q_C	Q_D	RIPPLE CARRY OUT
*	*	L	*	↓	Don't Care					No change				L
*	*	H	*	↓	Don't Care					No change				Able
L	*	*	*	*	Don't Care					All Reset				L
H	*	L	L	↑	Program Data					Program Output				L
H	*	H	L	↑	Program Data					Program Output				Able
H	*	L	H	↑	Don't Care					No count				L
H	L	H	H	↑	Don't Care					No count				Able
H	H	H	H	↑	Don't Care					Count up				Able

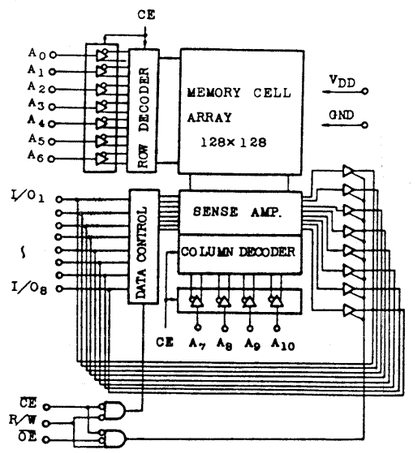
* Don't care

TC5517APL

16k-Bit Static RAM

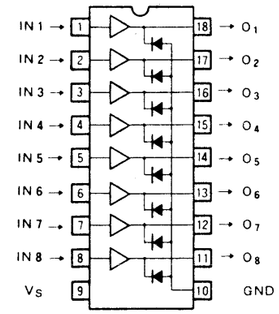
Pin Configuration





M54562, M54564

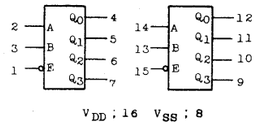
Pin Configuration



TC4555BP

Dual Binary To 1 Of 4 Decoder/Demultiplexer

Pin Configuration



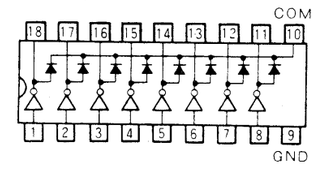
Truth Table

※ : Don't care

INPUTS			OUTPUTS TC4555BP			
$\overline{E}$	B	A	Q_3	Q_2	Q_1	Q_0
L	L	L	L	L	L	H
L	L	H	L	L	H	L
L	H	L	L	H	L	L
L	H	H	H	L	L	L
H	※	※	L	L	L	L

M54522

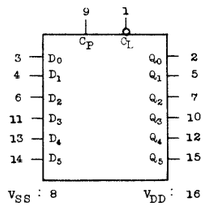
Pin Configuration



TC40H174P

Hex D-type Flip-Flop

Pin Configuration



Truth Table

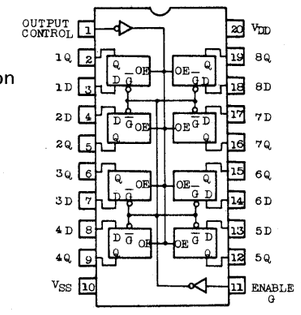
※ Don't Care

INPUT			OUTPUT
CLOCK	D_n	$\overline{CLEAR}$	Q_n
↑	H	H	H
↑	L	H	L
↓	※	H	No Change
※	※	L	L

TC40H373P

Octal D-type Latch (3-state output)

Pin Configuration



Truth Table

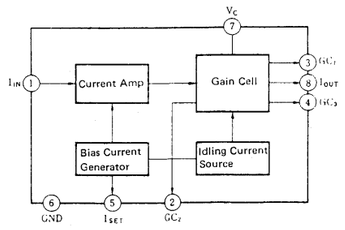
INPUTS			OUTPUT
OUTPUT CONTROL	ENABLE G	DATA	Q
L	H	H	H
L	H	L	L
L	L	※	Q_0
H	※	※	High Impedance

※=Don't care

μPC1252H2

Bipolar Analog Integrated Circuit

Block Diagram



TC4051BP

Single 8-Channel Multiplexer/Demultiplexer

TC4052BP

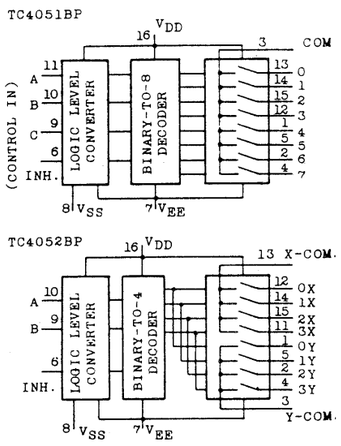
Defferential 4-Channel multiplexer/Demultiplexer

Truth Table

CONTROL INPUTS				"ON" CHANNEL	
INHIBIT	C △	B	A	TC4051BP	TC4052BP
L	L	L	L	0	0X, 0Y
L	L	L	H	1	1X, 1Y
L	L	H	L	2	2X, 2Y
L	L	H	H	3	3X, 3Y
L	H	L	L	4	—
L	H	L	H	5	—
L	H	H	L	6	—
L	H	H	H	7	—
H	※	※	※	NONE	NONE

※ Don't Care, △ Except TC4052BP

Block Diagram



ADJUSTMENT

Adjustment must be performed in the order listed below.

POWER SUPPLY BOARD
↓
ENTERING TEST MODE
↓
MODULE BOARD
↓
JACK BOARD
↓
CHECKING MIDI FUNCTION

CAUTION

Allow at least 10 minutes for warmup period; mandatory upon VCF adjustments.

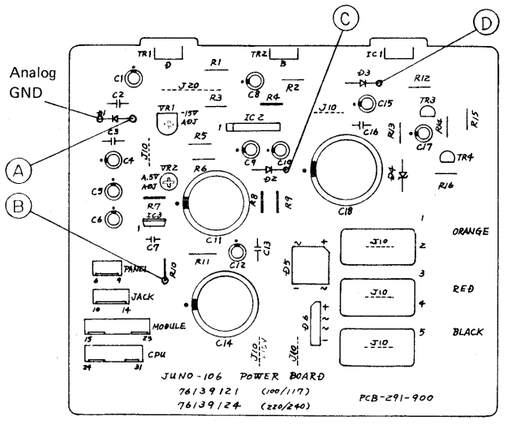
1. DC SUPPLY VOLTAGES (POWER SUPPLY BOARD)

CAUTION

Any slight adjustment on this board must be followed by a complete adjustment of the rest. Do not touch the trimmers inadvertently before checking the test points for voltage.

Test instrument: Digital voltmeter with 10mV resolution.

1-1. Adjust VR1 for −15V ± 10mV at Ⓐ.
1-2. Adjust VR2 for +5V ± 10mV at Ⓑ.
1-3. Verify +15V ± 0.8V at Ⓒ.
1-4. Verify +5V ± 0.5V at Ⓓ.



TEST PROGRAM

The following adjustments can be performed with the aid of Test Program stored in the CPU on the CPU Board.

To enter the test mode, hold KEY TRANSPOSE down and turn the JUNO-106 ON; the display window will read [00] indicating that the unit is in the test mode. During the test mode, each switch serves as follows:

SWITCH		FUNCTION DURING THE TEST MODE	
KEY ASSIGNMENT	POLY 1	UNISON:	All six modules are assigned simultaneously to a key being pressed.
	POLY 2	NON ROTARY:	The voices are assigned to the keys played in the order CH1 to CH6 as long as the previous keys are held down. One-key staccato always sounds CH1 only.
		The display window indicates currently assigned channel number.	
	POLY 1 & POLY 2	ROTARY:	The voices are assigned in cyclic manner; 7th key steals the voice from the 1st key.
		The display window indicates current channel number.	
BANK GROUP	GROUP A GROUP B	HOLD OFF HOLD ON	
TAPE CHECK LED	SAVE LED VERIFY LED	MIDI FUNCTION II CHECK MIDI FUNCTION I CHECK	
MIDI CH		Turns D/A output to 0V	

Pressing BANK buttons also evokes Test Program and sets the front panel controls as below. PATCH buttons have no effects in the test mode.

BANK NO.	TEST FUNCTION	LFO RATE	LFO DELAY	DCO RANGE	DCO ▭	DCO ◺	DCO SUB	DCO NOISE	DCO LFO	DCO PWM	DCO PWM MODE	HPF	VCF FREQ	VCF RESO	VCF ENV	VCF ENV POLA	VCF LFO	VCF KYBD	VCA ◺	VCA LEVEL	ENV A	ENV D	ENV S	ENV R	CHORUS
1	VCA OFFSET	5	0	8′			0	0	0	0	M	1	10	0	0	N	0	10	◺	5	0	0	0	0	0
2	SUB OSC	5	0	8′			10	0	0	0	M	1	10	0	0	N	0	10	◺	5	0	0	10	0	0
3	VCA GAIN VCF	5	0	8′			0	0	0	0	M	1	6.3	10	0	N	0	10	◺	5	0	0	10	0	0
4	◿	5	0	8′		ON	0	0	0	0	M	1	10	0	0	N	0	10	◺	5	0	0	10	0	0
5	PWM 50%	5	0	8′	ON		0	0	0	0	M	1	10	0	0	N	0	10	◺	5	0	0	10	0	0
6	NOISE LEVEL	5	0	8′			0	10	0	0	M	1	10	0	0	N	0	10	◺	5	0	0	10	0	0
7	VCF HIGH LOW	5	0	8′			0	0	0	0	M	1	10	10	0	N	0	10	◺	5	0	0	10	0	0
8	RE-TRIGGER	5	0	8′	ON		0	0	0	0	M	1	10	0	0	N	0	10	◺	5	0	1.3	0	1.3	0

Not all TEST FUNCTIONs are involved in the adjustment.

Edit functions also are active in test mode; when an edit is made, display window lights a dot. To return to the test mode, press the same BANK button again.

2. DCO CV OFFSET (MODULE BOARD)

Test instrument: Voltmeter (1mV resolution)
Test point: TP3
Key assignment: POLY 1 (UNISON during test mode).

2-1. Press MIDI CH button; D/A converter turns its output to 0V.

CAUTION

Pressing any key on the keyboard releases MIDI CH, letting the D/A to develop voltage according to that key. Press MIDI CH again to defeat the key voltage.

2-2. Adjust VR33 for 0V reading.
2-3. Leave MIDI CH ON for the next adjustment 3.

3. VCA BIAS (MODULE BOARD)

Test instrument: Voltmeter (1mV resolution)
Test point: TP7
Key assignment: POLY 1 (UNISON during test mode).

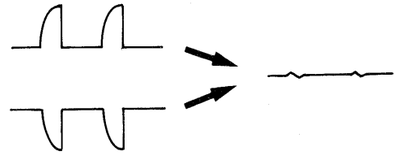
3-1. Press MIDI CH. Refer to "CAUTION in 2-1".
3-2. Adjust VR34 for a reading within +0.25V to +0.27V.

4. VCA OFFSET (MODULE BOARD)

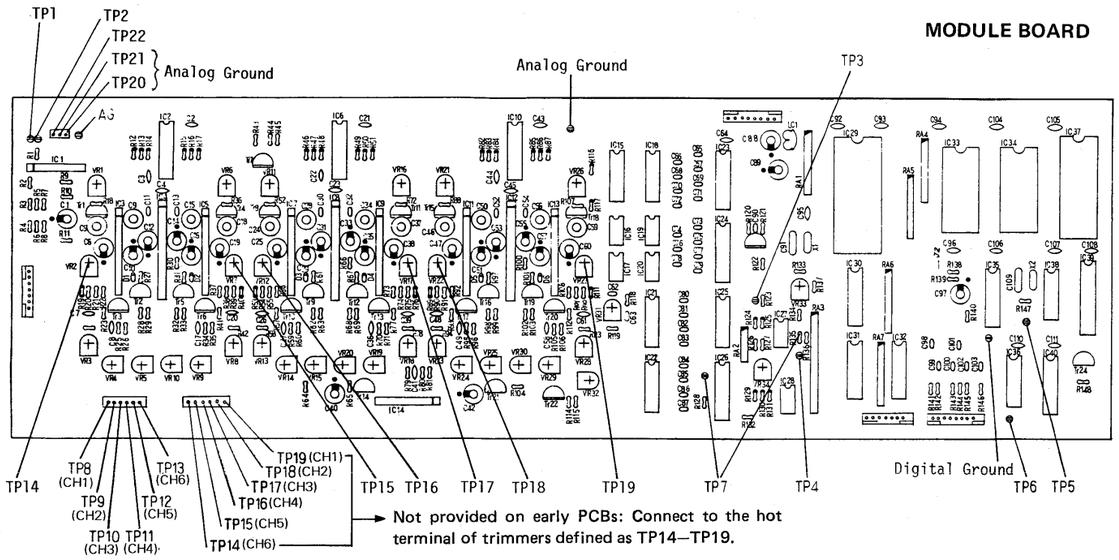
Test instrument: Oscilloscope
Test point. TP8 (CH1) to TP13 (CH6)
BANK: 1
Key assignment: POLY 1 (UNISON during test mode)

4-1. Adjust the following trimmers, respectively, for the minimum thumps.

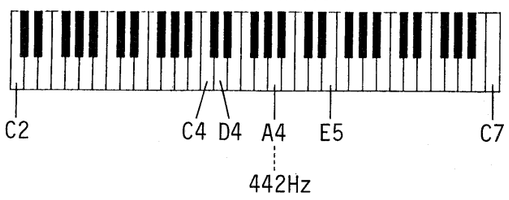
VR NO.	30	25	20	15	10	5
CH NO.	1	2	3	4	5	6



MODULE BOARD



KEY DESIGNATION



5. VCF RESONANCE (MODULE BOARD)

CAUTION

This adjustment must be done after 10 minutes has passed and after 3. VCA BIAS has been finished.

Test instrument: Oscilloscope
Test point: TP19 (CH1) to TP14 (CH6)
Key assignment: POLY 1 (UNISON during test mode).
BANK: 3

5-1. While holding down C4 key, adjust the trimmers listed below, respectively, for 4.8Vp-p sine wave.

VR NO.	26	21	16	11	6	1
CH NO.	1	2	3	4	5	6

6. VCA GAIN (MODULE BOARD)

CAUTION

This adjustment must follow 5. VCF RESONANCE.

Test instrument: Oscilloscope
Test point: TP8 (CH1) to TP13 (CH6)
Key assignment: POLY 1 (UNISON during test mode)
BANK: 3

6-1. While holding down C4 key, adjust the following trimmers, respectively, for 6Vp-p sinewave.

VR NO.	27	22	17	12	7	2
CH NO.	1	2	3	4	5	6

7. VCF FREQUENCY (MODULE BOARD)

CAUTION

This adjustment must be performed after 10-minute warmup has passed.

Test instrument: Frequency counter or Tuner
Test point: TP8 (CH1) to TP13 (CH6), or OUTPUT
Key assignment: POLY 1 (UNISON during test mode) or POLY 1 + POLY 2 (ROTARY during test mode) -- when checking at OUTPUT
BANK: 3

7-1. While holding C4 key, adjust the trimmers listed below, respectively, for 248Hz (B3 pitch).

VR NO.	29	24	19	14	9	4
CH NO.	1	2	3	4	5	6

8. VCF WIDTH (MODULE BOARD)

CAUTION

Perform this adjustment after at least 10-minute warmup.

Test instrument: Frequency counter or Tuner
Test point: TP8 (CH1) to TP13 (CH6), or OUTPUT (tuner method)
Key assignment: POLY 1 or POLY 1 + POLY 2 (OUTPUT)
BANK: 3

8-1. Holding C6 key down, adjust each trimmer listed below respectively for 992Hz (equal to B5 note).

VR NO.	28	23	18	13	8	3
CH NO.	1	2	3	4	5	6

NOTE: Procedures 7 and 8 interact. Repeat the steps in both paragraphs until satisfactory result is obtained (within ± 10 cents on the tuner).

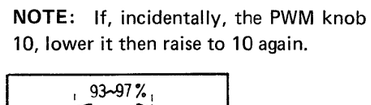
9. NOISE LEVEL (MODULE BOARD)

CAUTION

6. VCA GAIN must have been finished before this adjustment is performed.

Test instrument: Oscilloscope
Test point: TP8
Key assignment: POLY 1
BANK: 6

9-1. Holding any key on the keyboard down, adjust VR32 for 4Vp-p on the scope.



10. PWM (MODULE BOARD)

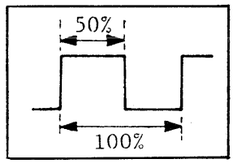
CAUTION

2. DCO CV OFFSET must have been finished.

50%

Test instrument: Oscilloscope
Test point: TP8 (CH1) to TP13 (CH6)
Key assignment: POLY 1
BANK: 5

10-1. While holding C4 key down, adjust VR31 for a 50% duty cycle.



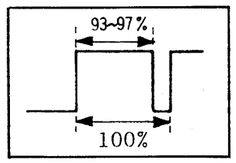
Tolerance: 48—52%

10-2. Confirm that the duty cycles of the rest channels (TP9 — TP13) are within 48 — 52%.

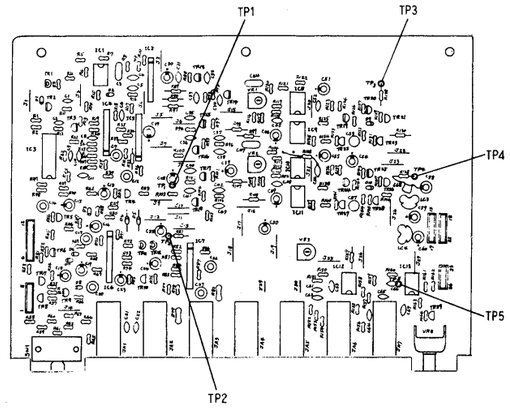
95%

10-3. Holding C4 key down, confirm that duty cycle of all channels are within 93 — 97% with PWM set at 10.

NOTE: If, incidentally, the PWM knob has been set at 10, lower it then raise to 10 again.



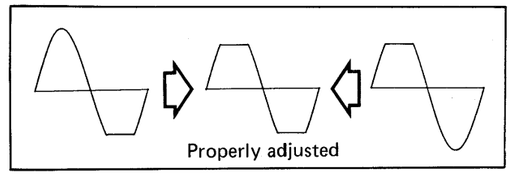
JACK BOARD



11. CHORUS BIAS (JACK BOARD)

Test instrument: Oscilloscope, Audio generator
Test point: TP1 (CH1), TP2 (CH2)
VCA LEVEL: 0
CHORUS: I

11-1. Feed 10Vp-p, 1kHz, sine wave into TP2 of the MODULE BOARD.
11-2. Adjust VR1 (CH1) and VR2 (CH2) on the JACK Board respectively so that positive and negative halve are symmetrical with respect to the center horizontal line.



12. LOAD OFFSET (JACK BOARD)

Test instrument: Voltmeter with 1mV resolution
Test point: TP5

12-1. Adjust VR3 for 0mV reading.

13. MIDI FUNCTION SWITCH CHECK

13-1. Verify the following with FUNCTION set at respective position.

I: only VERIFY LED lights
II: only SAVE LED lights
III: no LEDs light

MIDI NOTES

GENERAL PRECAUTIONS ON MIDI CONNECTION

Although all MIDI instruments function to MIDI specification, some precautions must be taken for satisfactory operation.
This is mainly due to MIDI revision. One of primary procedures to be correctly followed is setting of "Channel Mode" otherwise MIDI function fails from the beginning. Also remember that MIDI information is effective only when receiving device can recognize a given message and has software and hardware that duplicate function defined by the message.
On power up most Roland products complying with MIDI specification 1.0 default to OMNI ON, POLY. On the contrary, they transmit OMNI OFF and POLY mode messages from MIDI OUT jack. The reason is as follows.

MODE	RECEIVER
1 OMNI ON POLY	Voice messages are received from all Voice Channels and assigned to voices polyphonically.
2 OMNI ON MONO	Voice messages are received from all Voice Channels, and control only one voice, monophonically.
3 OMNI OFF POLY	Voice messages are received in Voice Channel N only, and are assigned to voices polyphonically.
4 OMNI OFF MONO	Voice messages are received in Voice Channels N thru N+M-1, and assigned monophonically to voices 1 thru M, respectively. The number of voices M is specified by the third byte of the Mono Mode Message.

N: Basic Channel

This is an inherent channel of an instrument, which cannot be changed by MIDI messages but may be changed by the panel function on the instrument.

The JUNO-106 has channel selections on the front panel.

Receiving instrument must be reset to OMNI OFF mode when it is to accommodate voice messages sent over the channel to which it is currently assigned while other voice messages are present in other channels. (Example. a system consists of one master and more than one slave, each assigned to different channel.) However, some instruments are incapable of changing modes on the front panel and need external OMNI OFF message.

To cure this problem a system including such instruments as slaves should be configured as below.

MASTER (1st slave)	SLAVE(s)
capable of producing OMNI OFF message (or POLY, see NOTES) 1. on panel or other means at desired time 2. on power up	incapable of turning to OMNI OFF mode by itself

In the above combination:

1. Slave must be powered ON before the master is turned ON.
   (When the second slave connects to MIDI OUT of the first slave, it is the first to be turned ON.)

2. Master and Slave(s) must be set in the same channel since mode messages will be recognized by the slave only when set in the channel to which the slave's receiver has been assigned.

NOTES:
1. Roland products with preliminary MIDI turn to OMNI OFF upon receiving POLY mode ON.
2. JUNO-106 transmits OMNI OFF and POLY messages on power-up.

MIDI IMPLEMENTATION

April 11, 1984

1. TRANSMITTED DATA

1-1. When MIDI FUNCTION is at 1.

Note events, Hold on/off and Channel Mode messages are sent.

Status	Second	Third	Description
1001 nnnn	0kkk kkkk	0100 0000	Note on
1001 nnnn	0kkk kkkk	0	Note off
1011 nnnn	0100 0000	0111 1111	Hold on from rear panel jack
1011 nnnn	0100 0000	0	Hold off
1011 nnnn	0111 1011	0	ALL NOTE OFF *2
1011 nnnn	0111 1100	0	OMNI OFF *1
1011 nnnn	0111 1111	0	POLY *1

NOTE: nnnn : MIDI channel number - 1, (if ch-1, nnnn = 0000)
kkkkkkk : 24 - 108
*1 On power up or when MIDI channel number is set.
*2 When all Notes are turned Off.

1-2. When MIDI FUNCTION is at 2.

Messages to be sent with FUNCTION set at 1, Program Change, Bender and LFO Modulation are sent.

Status	Second	Third	Description
1100 nnnn	0ppp pppp		Program Change Group-A : 0 - 63 Group-B : 64 - 127
1110 nnnn	0bb0 0000 (LSB)	0bbb bbbb (MSB)	Pitch Bender MSB LSB MAX (high) 127 96 CENTER 64 0 MIN (low) 0 0
1011 nnnn	0000 0001	0111 1111	LFO Modulation On
1011 nnnn	0000 0001	0	LFO Modulation Off

1-3. When MIDI FUNCTION is at 3.

Messages to be sent with FUNCTION set at 1, Bender, LFO Modulation and Exclusive Messages are sent.

2. RECOGNIZED RECEIVE DATA

2-1. When MIDI FUNCTION is at 1.

When power is first applied, receiver's mode is set to OMNI ON, POLY.
Notes events, Hold on/off and Channel Mode Messages are recognized.

Status	Second	Third	Description
1000 nnnn	0kkk kkkk	0vvv vvvv	Note OFF, velocity ignored
1001 nnnn	0kkk kkkk	0000 0000	Note OFF kkkkkkk = 0 - 127 (24 - 108)
1001 nnnn	0kkk kkkk	0vvv vvvv	Note ON kkkkkkk = 0 - 127 (24 - 108) vvvvvvv = 1 - 127, velocity ignored
1011 nnnn	0100 0000	0	hold OFF
1011 nnnn	0100 0000	0vvv vvvv	hold ON vvvvvvv = 1 - 127
1011 nnnn	0111 1011	0	ALL NOTES OFF
1011 nnnn	0111 1100	0	OMNI OFF
1011 nnnn	0111 1101	0	OMNI ON
1011 nnnn	0111 1110	0mmm mmmm	MONO
1011 nnnn	0111 1111	0	POLY

NOTES: Mode messages (123 - 127) are also recognized as ALL NOTES OFF.
The JUNO-106 does not respond to MONO mode select.

Mode messages are recognized as follows:

	POLY ($7F)	MONO ($7E) mmmmmmmm = 1	MONO ($7E) mmmmmmmm <> 1
OMNI OFF ($7C)	OMNI = OFF POLY	OMNI = OFF POLY	OMNI = ON POLY
OMNI ON ($7D)	OMNI = ON POLY	OMNI = ON POLY	OMNI = ON POLY

Recognized channels are as follows:

Mode	Voice messages	Mode messages
OMNI OFF mode	basic channel only	basic channel only
OMNI ON mode	all channels	basic channel only

2-2. When MIDI FUNCTION is at 2.

Messages to be recognized with FUNCTION set at 1, Program Change, Bender and LFO Modulation are recognized.

Status	Second	Third	Description
1100 nnnn	0ppp pppp		Program Change 0 - 63 : Group-A 11-88 64 - 127 : Group-B 11-88
1110 nnnn	0b00 0000	0bbb bbbb	Pitch Bender LS 6 bits are ignored
1011 nnnn	0000 0001	0vvv vvvv	LFO Modulation v = 0 (min) 127 (max)

NOTE: Sensitivity of the pitch bender and modulation can be adjusted at the receiver.

2-3. When MIDI FUNCTION is at 3.

Messages to be recognized with FUNCTION set at 2 and EXCLUSIVE messages are recognized.

3. EXCLUSIVE MESSAGES

3-1. When Group, Bank or Patch number is changed.

	Byte		Description
a	1111 0000	$F0	Exclusive
b	0100 0001	$41	Roland ID#
c	0011 0000	$30	function type
d	0000 nnnn	$0N	N+1 = MIDI channel, N = 0 - 15
e	0xxx xxxx		Program number 0 - 127
f	0zzz zzzz		value 0 - 127
			(18 bytes total for values)
g	1111 0111	$F7	EOX

*** Example ***

```
a  b  c  d  e  f  f  .  .  .  .  .  .  .  .
F0 41 30 00 00  39 2D 00 37 00 55 00 00 00

f  .  .  .  .  .  .  .  .  g
19 34 3B 20 56 28 00 1A 18  F7
```

3-2. When Manual Button is pressed.

	Byte		Description
a	1111 0000	$F0	Exclusive
b	0100 0001	$41	Roland ID
c	0011 0001	$31	function type
d	0000 nnnn	$0N	N+1 = MIDI channel, N = 0 - 15
e	0000 0000	$00	Number indicates "Manual"
f	0zzz zzzz		value 0 - 127
			(18 bytes total for values)
g	1111 0111	$F7	EOX

*** Example ***

```
a  b  c  d  e  f  f  .  .  .  .  .  .  .  .
F0 41 31 00 00  03 00 00 00 00 3F 3C 00 00

f  .  .  .  .  .  .  .  .  g
7F 45 00 00 7F 00 00 2A 19  F7
```

3-3. When pot(s) or switch(s) in the upper half of the front panel is manuplated.

	Byte		Description
a	1111 0000	$F0	Exclusive
b	0100 0001	$41	Roland ID
c	0011 0001	$32	function type
d	0000 nnnn	$0N	N+1 = MIDI channel, N = 0 - 15
e	0yyy yyyy		parameter number 0 - 17
f	0zzz zzzz		value 0 - 127
g	1111 0111	$F7	EOX

*** Example ***

```
a  b  c  d  e  f  g
F0 41 32 00 03  04  F7
```

3-4. Parameter number table.

* Potentiometers

p#	Function	p#	Function
0	LFO rate	8	VCF LFO
1	LFO delay	9	VCF KYBD
2	DCO LFO	10	VCA level
3	DCO PWM	11	attack
4	noise level	12	decay
5	VCF cutoff	13	sustain
6	resonance	14	release
7	VCF ENV	15	sub level

* Switches

Bit	6	5	4	3	2	1	0
p#	Function						
16	chorus 1: 1 0: 2	chorus 1: off 0: on	sawtooth 1: on 0: off	pulse 1: on 0: off		range 100: 4' 010: 8' 001: 16'	
17	0	0	HP filter 11: off 10: 1 01: 2 00: 3		VCA 1: gate 0: ENV	ENV 1: - 0: +	PWM 1: MAN 0: LFO