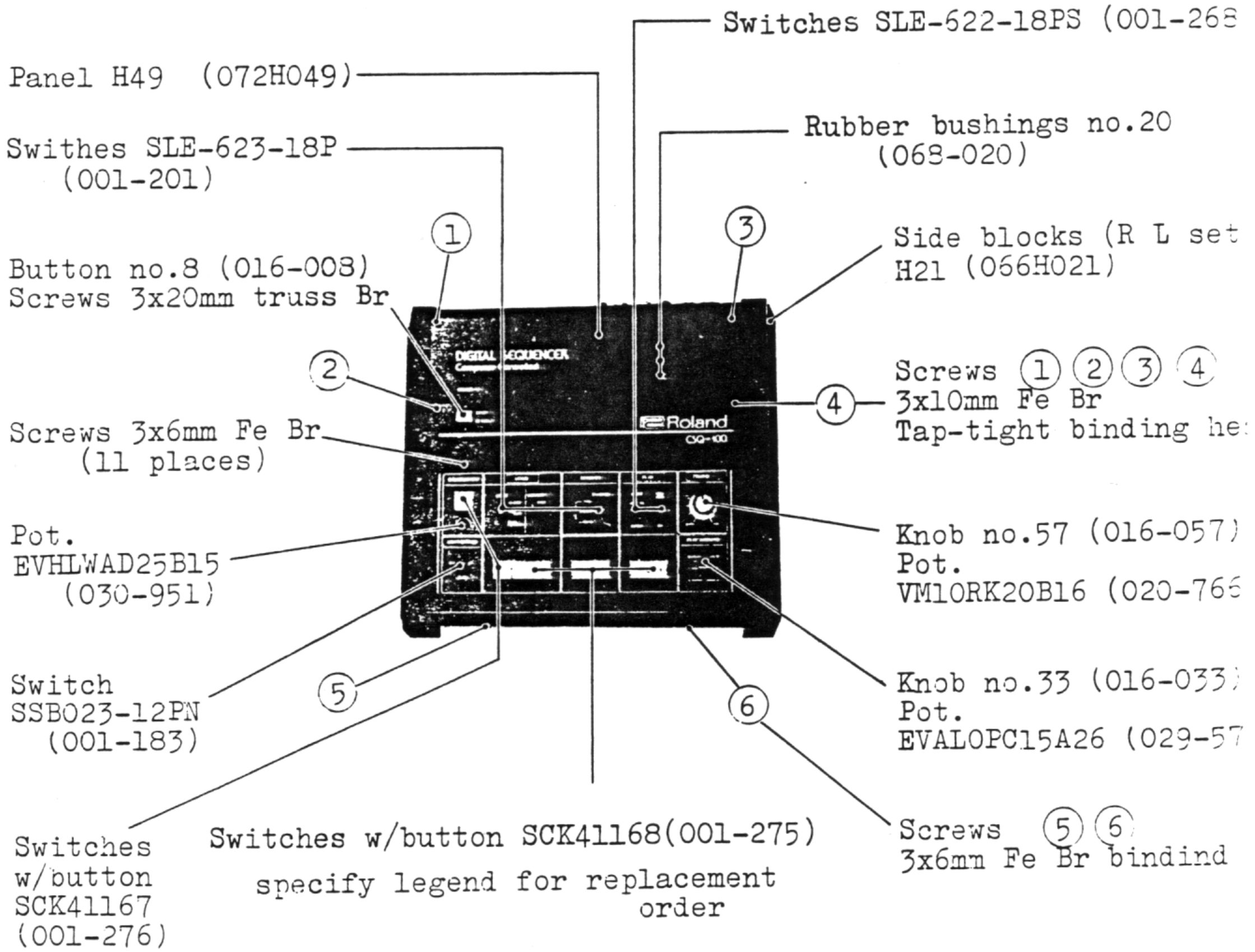
CSQ-100 SERVICE NOTES

Memory capacity ---- Up to 168 notes (84 notes/channel) 2 channels
CV output ---------- 1V/oct: -2V to +8V
CV input ---------- 1V/oct: 0V to +5V
Gate output -------- Off: 0V On: +15V
Gate input -------- Off: 0V On: +15V (threshold +2.5V)
EXT Start input ---- With switch: normally close, open to start
or pulse: +15V
EXT Step input ----- +15V pulse
Power consumptions-- 8 watts
Dimensions --------- 345W x 305D x 95H mm (13.6 x 12.0 x 3.7 in)
Weight ------------ 2.7 kg (5.94 lbs)

PANEL REMOVAL SCREWS: ① through ⑧ (⑦ ⑧ on the rear)

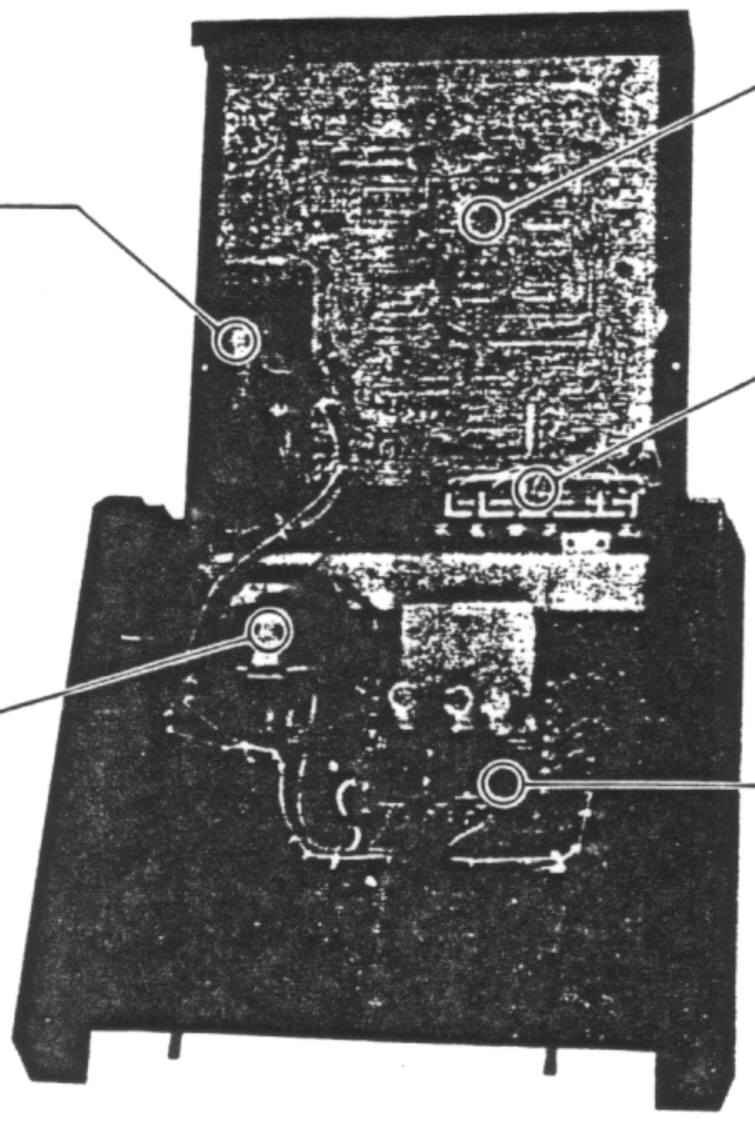


Switch

SDG5P 001-1 (001-215)
100V

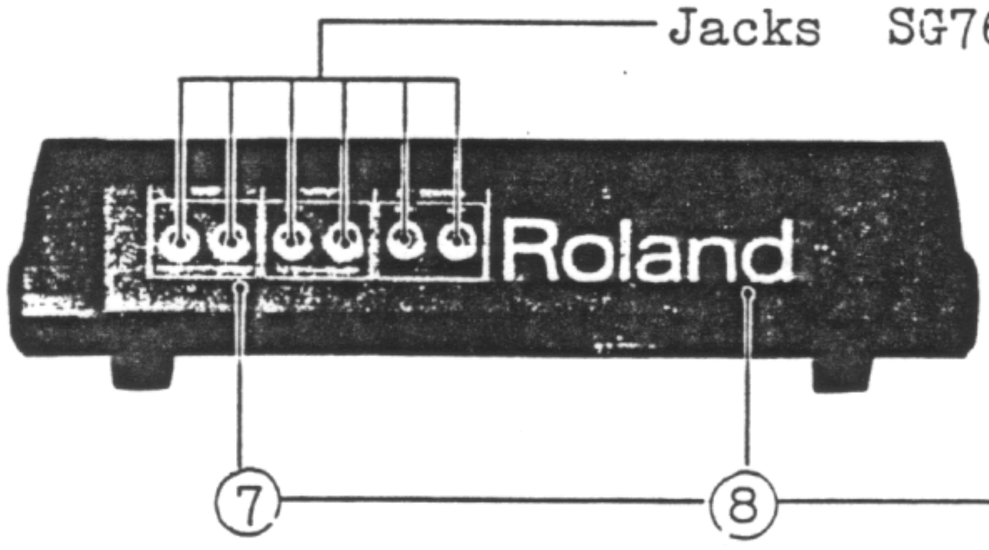
SDG5P 001-2 (001-216)
117V

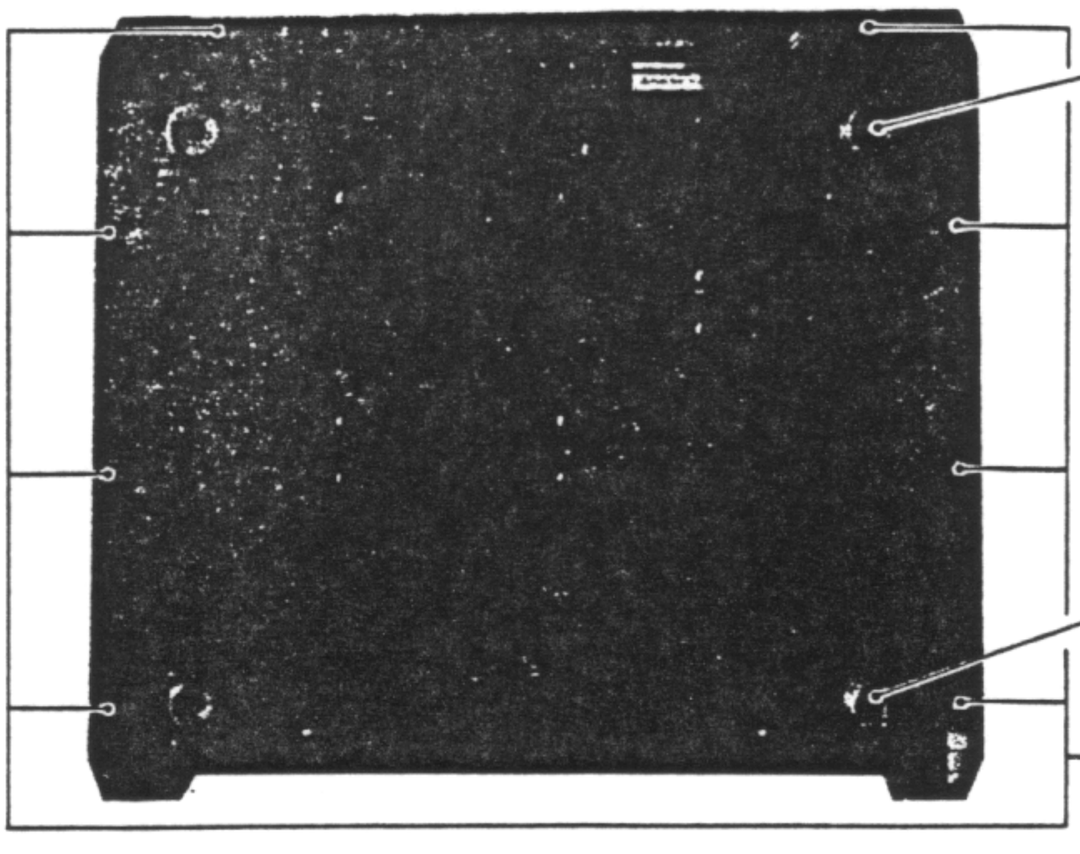
SDG5P-502 (001-217)
220/240V



022H024C 100/117V
022H024D 220/240V

PSH39 100V
PSH40 117V
PSH41 220/240V

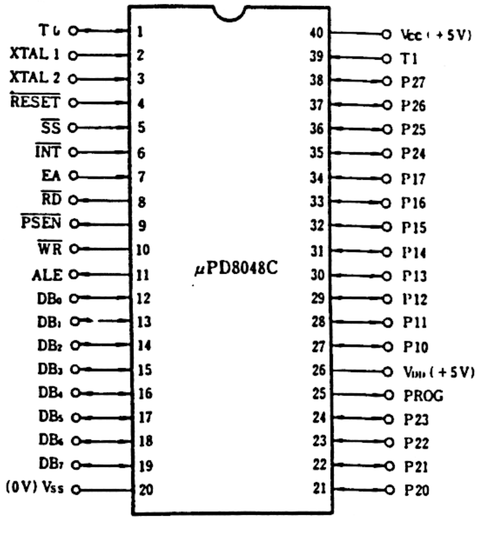




μ PD8048 Pin Description

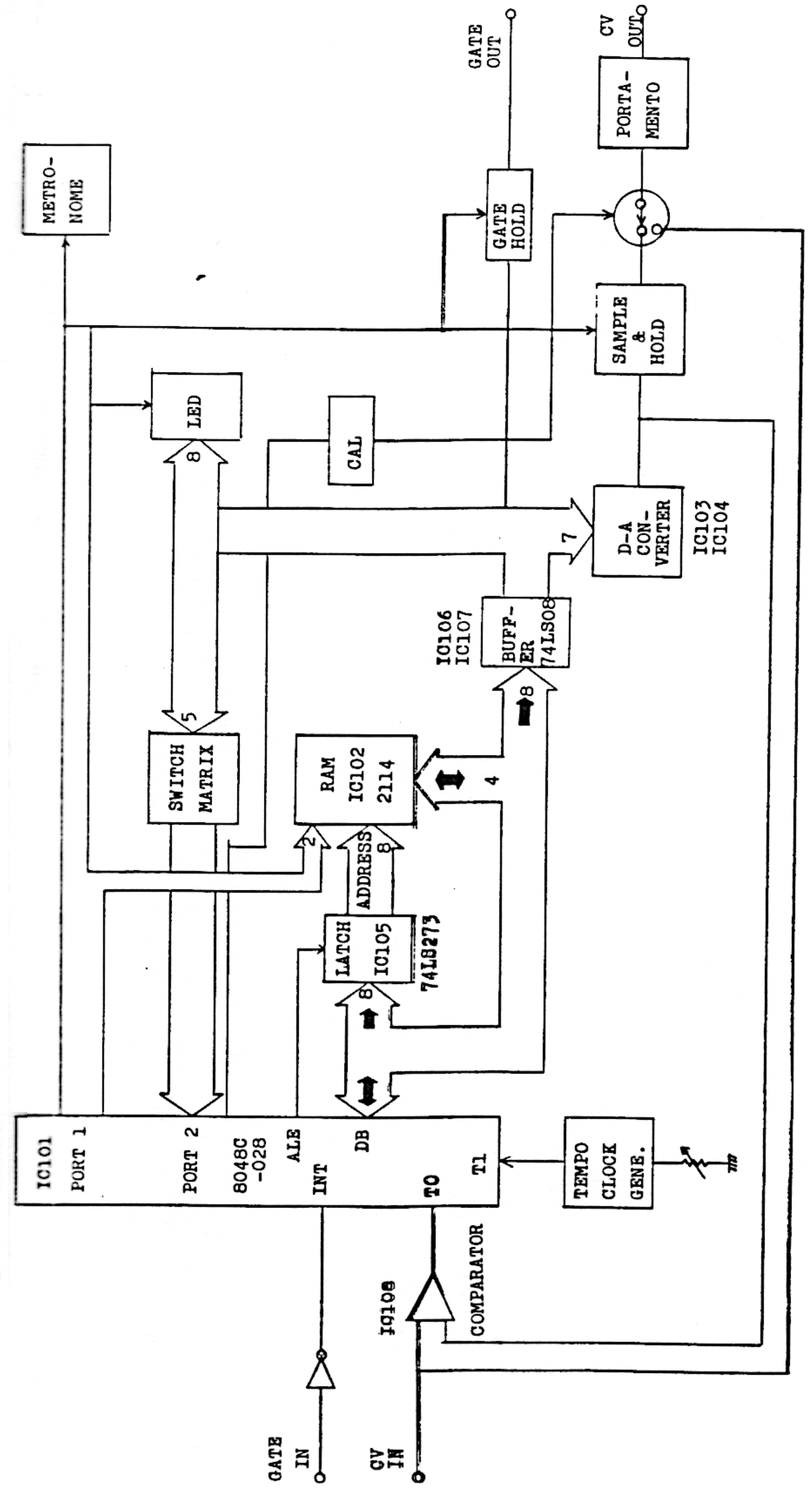
Designation		Pin No.	Function
DB (Data bus)	DB0	12	CV data (Switch scanning) / LED / RAM address (CV and GATE data during RAM address)
	1	13	
	2	14	
	3	15	
	4	16	
	5	17	
	6	18	
	7	19	Output Gate signal
P1 (Port 1)	P10	27	——
	11	28	RAM address
	12	29	——
	13	30	RAM address
	14	31	LED timing
	15	32	Output CV S/H and Gate hold timing
	16	33	——
	17	34	Metronome timing
P2 (Port 2)	P20	21	——
	21	22	——
	22	23	CV IN by-pass enable during the STOP mode
	23	24	——
	24	35	Read switches status during switch scanning
	25	36	
	26	37	
	27	38	
RESET		4	Input to reset the 8048 when power is on
INT		6	External gate input
T0		1	Digital data input suting A-D conversion
T1		39	Accepts TEMPO clock output
XTAL 1		2	External source inputs for internal oscillator
XTAL 2		3	

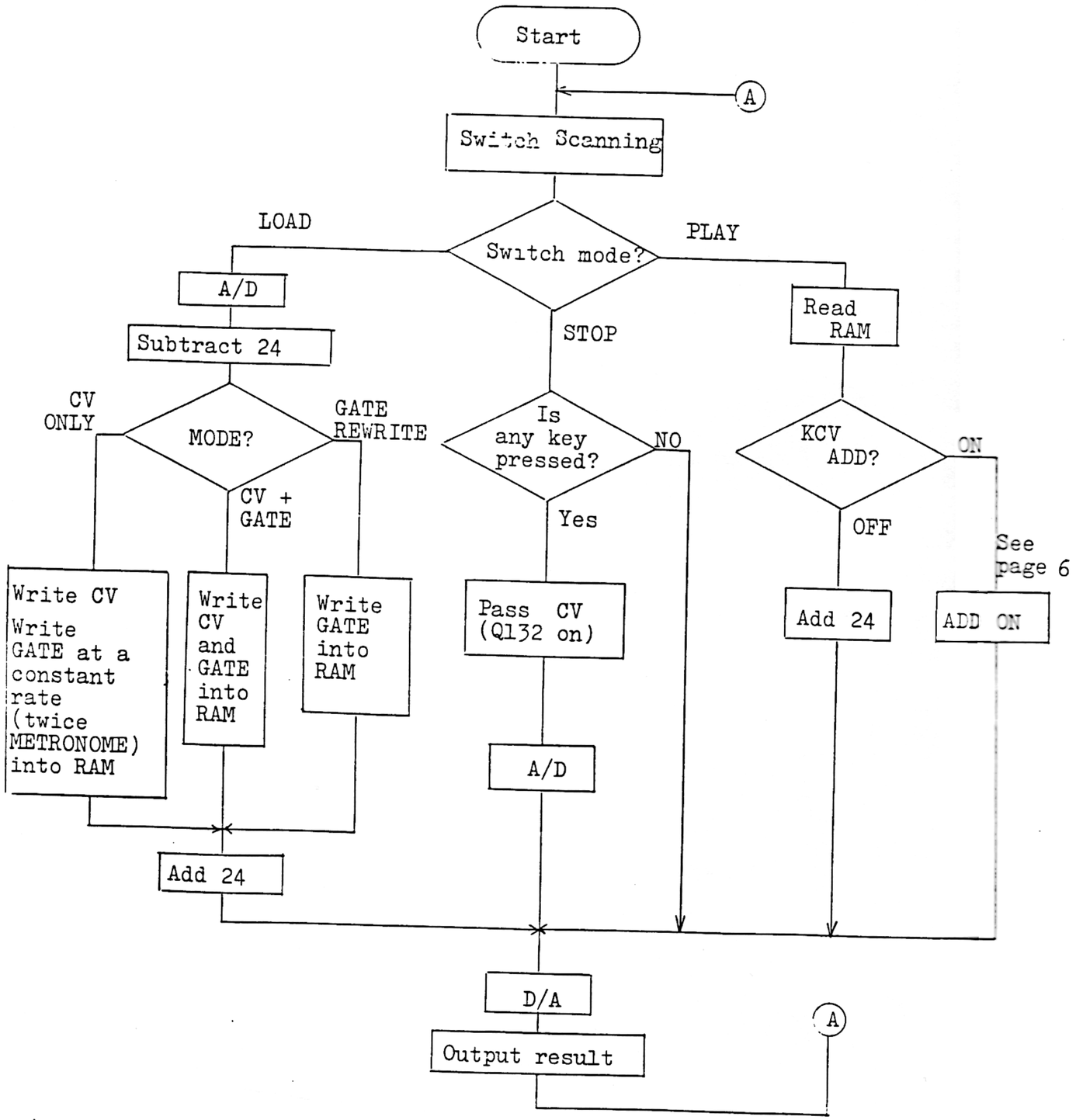
(Top View)



The uPD8048 is an 8-bit parallel computer fabricated on a single sillicon chip. The 8048 contains a 1k x 8 ROM program memory, 27 I/O lines, an 8-bit timer/counter and clock circuits.
Used in the CSQ-100 is a uPD8048C-028 version in which program and data dedicated to the CSQ-100 are stored in the program memory.

BLOCK DIAGRAM





CIRCUIT DESCRIPTION

This description is divided into parts: the general description which explains roughly the functions of CSQ-100, and the detailed description which centers around A/D and D/A converters since these are practically the heart in this instrument.
Complete unserstanding of A/D and D/A conversion circuits will aid in performing adjustments in Section II.

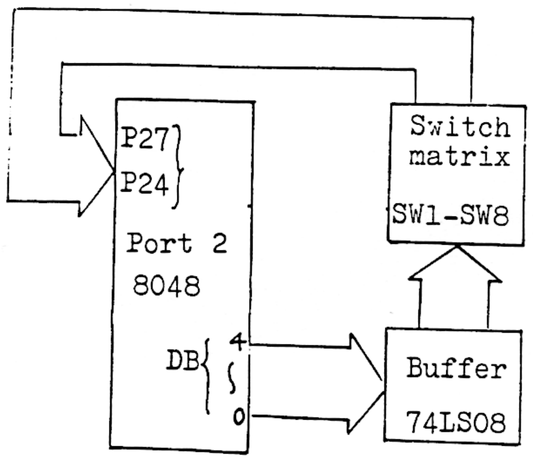
Function of " One chip computer" uPD8048

CSQ-100 performes its functions with uPD-8048 at the center position for all, including the following in its performance cycles:

1. Switch Scanning
2. D/A Conversion
3. A/D Conversion
4. Write/Read of Data to or from External RAM
5. Timing for lighting LED Indicator
6. Triggering of METRONOME
7. Holding of GATE OUT

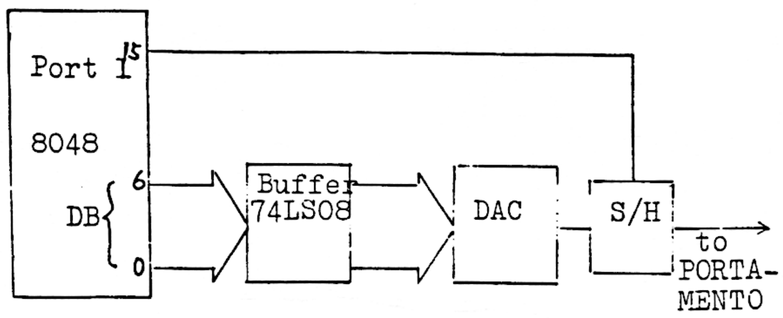
GENERAL

1. SWITCH SCANNING



µPD8048 starts its running cycles beginning with switch canning. Into DB0-DB4 (Data Bus) of 8048, 5-bit signals are being output according to the internal program, which are then brought to the switch matrix through the buffer. At first, L is output from DB4 while having H from other DB0 to DB3.
At the next instant, DB3 becomes to L while others change to H; and still next L on DB2 and so on, repeating such output changes 5 times on these bit signal combinations.
Depending on which key is depressed or in what position the switches are, corresponding signals are fed back through P24-P27 on Port 2.

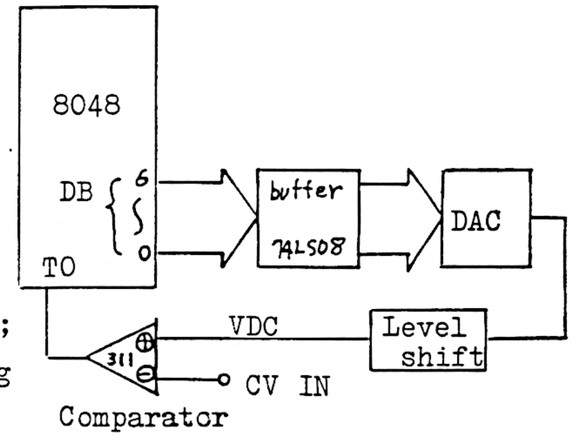
2. D/A CONVERSION - Digital to Analog -



The D/A converter transforms the sequential data (switch scanning, RAM address, CVs, etc.) which are being output from the 8048 through internal programming, into analog voltages.
Since the D/A converter (DAC) employed here is a summing type, with a weight-resistor-tree connected to an inverting input of an OP amp, each bit in the digital data is converted to an analog voltage in value to double the one immediately subordinate to each. When CV data are on output, pulses synchronized to CV data are supplied from P15 of Port 1 onto the Sample and Hold (S/H) circuit, and the analog CV voltage equivalent to the data are held on C124. (details disccused later)

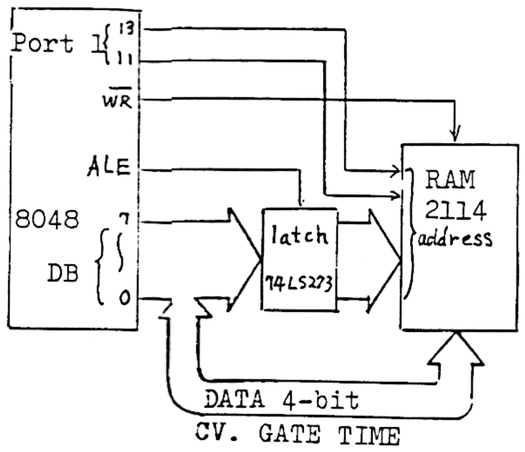
3. A/D CONVERSION (Analog to Digital)

Since the CV IN is an analog voltage, it must be converted to digital data for making the storing in RAM possible.
The method employed in the CSQ-100 is called "successive approximation conversion" where each bit, from DB6(for MSB;most significant bit) to DB0(for LSB; least significant bit), is being set successively to output "1" which, after being D/A converted, is to be compared with CV IN at the comparator (311).



The comparator will then output "0" (low) if CV VDC, or "1" (high) if CV VDC, onto TO. When H is output to TO, the corresponding digital data is "reset" and becomes 0.
Such set and "reset" is repeated 7 times for bits from DB6 to DB0 and with the resultant value from such "set" "reset" the digital data of the CV IN is produced.

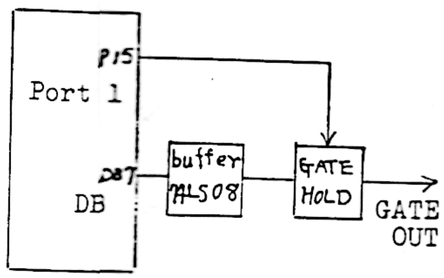
4. DATA (CV and GATE TIME) WRITE/READ to RAM



In the external RAM, memory cells are selected by the signal made in combination of the address signals latched on 74LS273 by the instruction signal from ALE (Address Latch Enable) and those from P11 and P13.
The data (CV and GATE TIME) are written when $\overline{WR}$ is "low" and are read when it is "high".
Although the data are in 8-bit format, they are written/read in two times separated to one-word-4-bit groups of lower and higher bits.

5. GATE HOLD

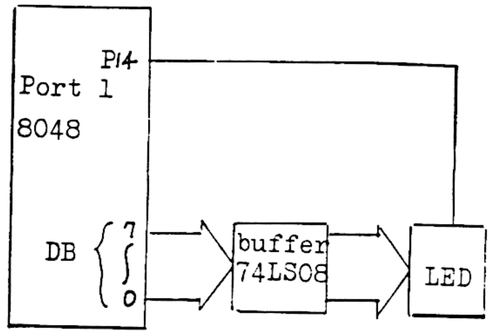
From DB7, the GATE signals are also being output.
They are held by the signal (the same as for S/H) to become output of GATE signal.



6. LIGHTING of LEDs

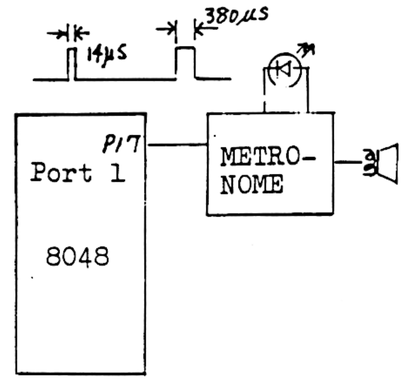
Signals for lighting LEDs (except TEMPO) are supplied from DB. However, because there are many signals on DB at every instance, timing pulses are given from P14 to control the LED circuits being fed only when there are output lighting signals.

The pulses are synchronized with those of TEMPO CLOCK GENERATOR and are output at the time rate one pulse for every eight CLOCK pulses. Because of this, lighting on/off cycling rate is also changed along with change in TEMPO, but the current amount to LED is still being kept unchanged through a means to maintain the duty ratio constant.

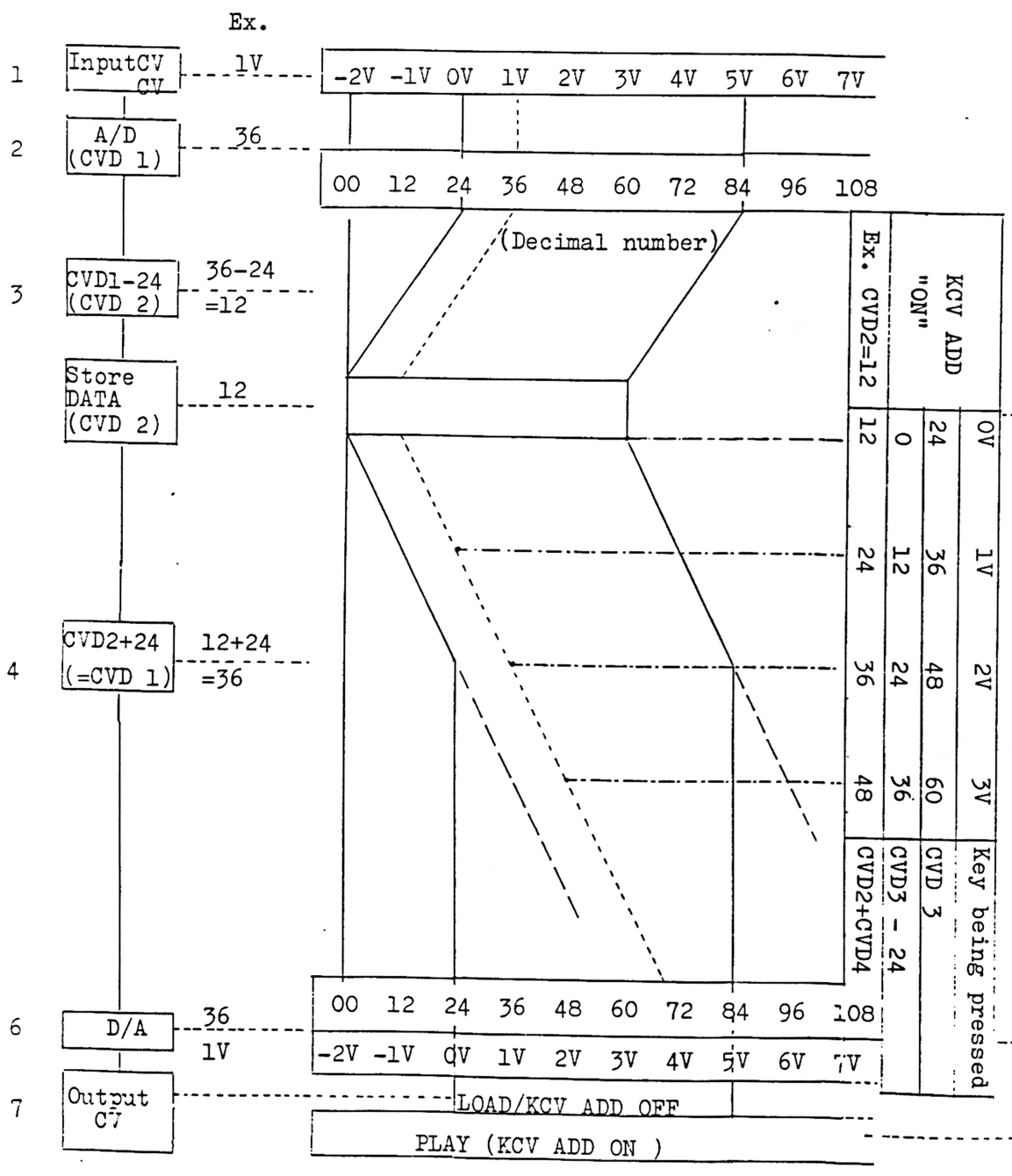


7. METRONOME DRIVE

In LOAD mode, two pulses synchronized to TEMPO are being output (in period 480 times the CLOCK pulse, in pulse widths of 14μs and 380μs for alternate output). METRONOME amp is driven by both pulses but since the shorter pulses of 14μs are filtered out by the integration circuit of R147 and C115 before arriving at LED, the longer pulses of 380μs only are used for lighting the TEMPO LED.

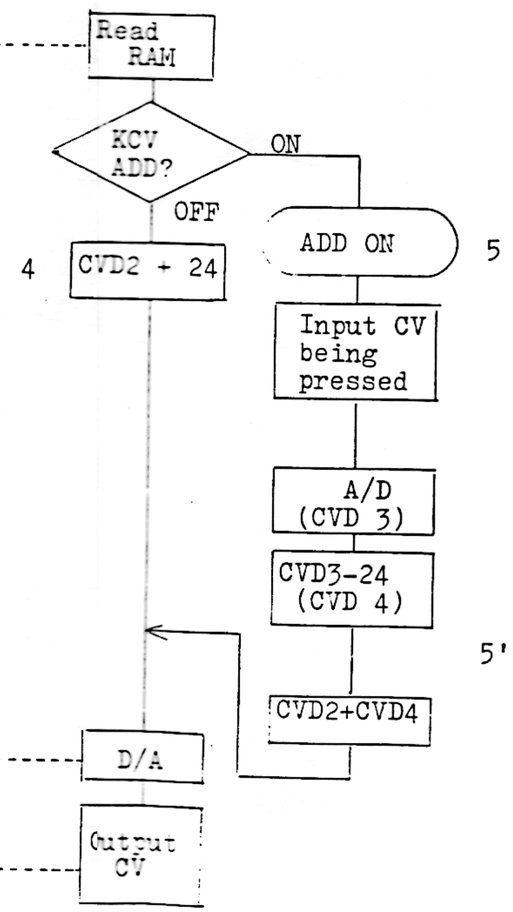


LOAD



Note:
The digital data in this manual are expressed in Decimals.

PLAY



DESCRIPTION of CICUIT FUNCTION
DETAILS

Since in the CSQ-100, the key voltage which are analog quantum are first converted to digital for storing in RAM and again afterward are converted to analog for CV OUT, these A/D and D/A conversions are just as important as the heart is to man.
It might be said that without understanding of these conversion principles and pertinent analog vs digital data relationship, all adjustment services which are related to key voltage circuits become difficult to perform correctly.
With this in mind, our description will proceed along with the line as numbered in the figure on the left page.

1. In the CSQ-100, the CV storage range runs from OV to +5V, or 61 notes.
2. Due to the reason to be touched on later, the lowest CV which is provided by this CSQ-100 is -2V. Therefore the digital data are made to correspond to 00 = -2V.
3. The voltages that can be stored in RAM are 0 to -5V, which makes the number of pitches to be 61 if taken in the ratio of 1V/oct. Although, in handling them, 6 bits (2^6 = 64) are enough, 7 bits would become necessary for the key voltage on the upper range if started from OV = 24. For this reason, numbers 24 are being subtracted after conversion to digital form to make OV = 00.(in decimal)
   The key voltage to correspond to th tal value "1" is about 83.3mV.
4. Reproduction of CV in ------ 1
   - LOAD or PL . ADD "off") -

...en D/A conversion is done after addition of 24, which is the same as subtracted before storing, into the data of RAM, the same digital analog voltage can be reproduced after D/A conversion.

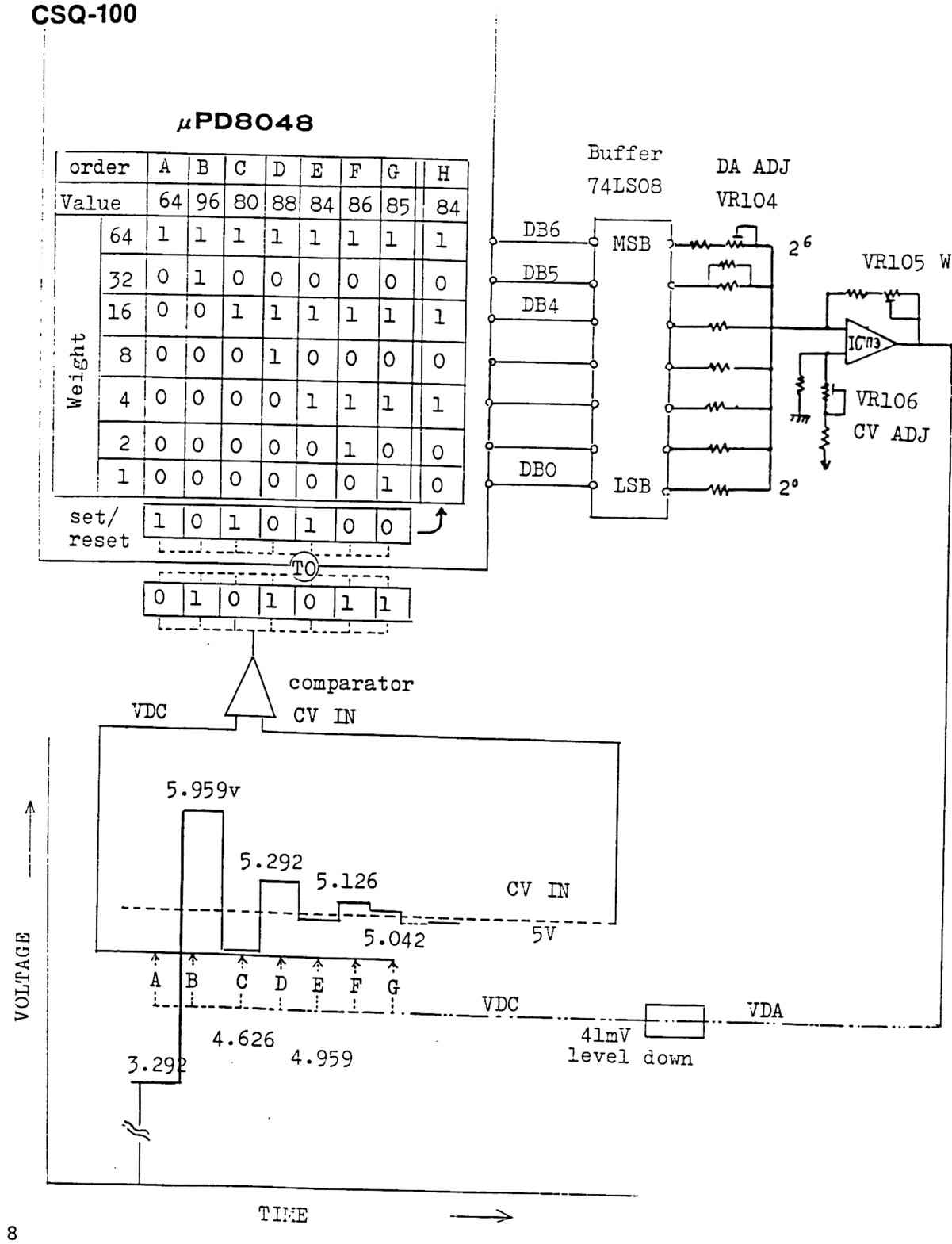
5. Reproduction of CV in Memory --------2
   - Transpose under PLAY mode, with KCV ADD "on"

CSQ-100 has the function to have a desired transposition of notes in PLAY mode by adding an external key voltage to the CV in memory. But, if transposition is required up or down, KCV must be varied also up or down from the center referenced by the key which produces on this mode the same orginal tones in pitch from the Memory.
Also, because the CSQ-100 has set this shift down range to be within 2V, the key to produce KCV=2V is made the reference key. For instance, when OV is stored in Memory, pressing a OV key, the lowest, will produce transposed output voltage -2V.
For this, the following must be true:

Digital data for OV stored in RAM (CV2 = 00)
+ KCV digital data of OV (CVD3 = 24)
= 00 (-2V)

To satisfy the above, " CVD2 + CVD3 - 24 = output data"

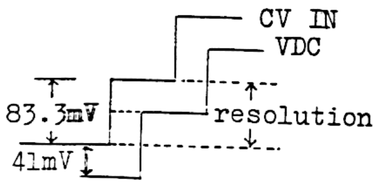
A/D and D/A CONVERSION - details-



When MSB is first set on, the signal "1" is output to DB6. When D/A converted, the analog voltage (VDA) here must be 3.333V which, after shifted down by 41mV, becomes 3.392V (VDC). This time VDC goes into noninverting input of the comparator and is compared with CV IN.
In the case shown in figure left, this CV is 5V, so CV IN> VDC bringing the comparator's output to L (0), to have DB6 remainded as has been set to "1".
Next, DB5 is set to "1". This time the digital data is the sum of DB6 and DB5, and the comparison becomes CV IN<VDC, to output H and to "reset" signal of TO and to have DB5 return to "0".
This kind of comparison is repeated 7 times down to DBO (LSB). The sum of the digital data of the bits remained "unreset", then, is made to be the data of this CV IN, with which the CV IN is stored in the external RAM.

VDC = VDA - 41mV
(precisely,41.7mV,and voltage differences between notes are 83.3mV or 84mV in turn)

Although CV IN is in fact an analog voltage, steps up or down like a stircase wave as the note changes. Therefore. if VDC is shifted down by an amount equal to about one-half of the voltage difference per key (step rate or resolution), a voltage fluctuation within the resolution value of the comparator does not bring effect on the digital data, as shown in the figure.



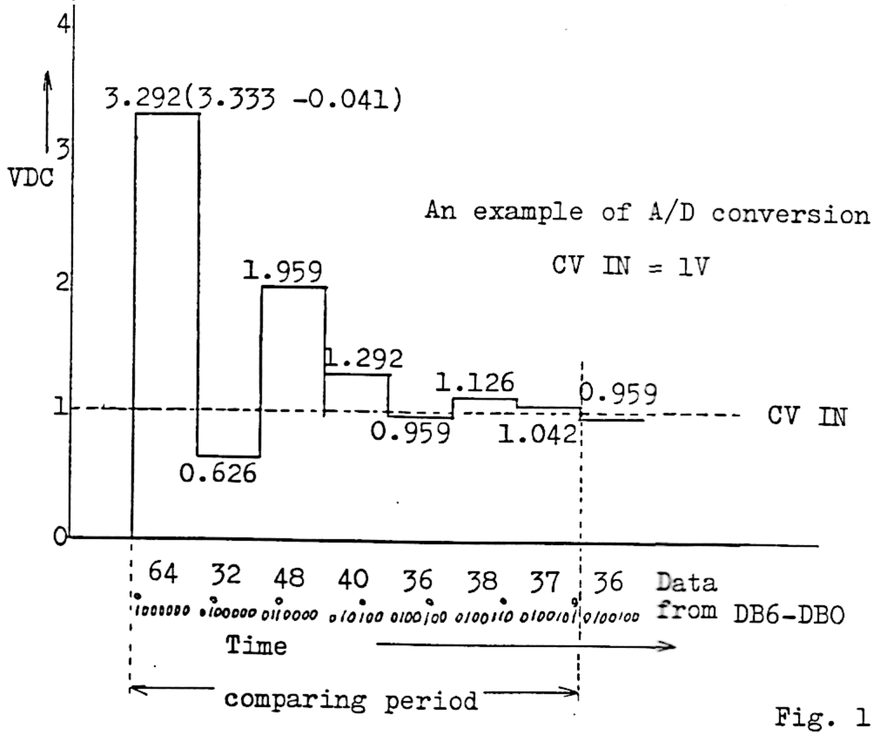


Fig. 1

RELATIONSHIP BETWEEN CV ADJ (VR106) and CV DATA

In LOAD mode and with the converter that is correctly adjusted, suppose that we turn VR106 (CV ADJ) slowly clockwise while holding 1V key depressed on the keyboard. Then you can observe VDA (i.e. CV OUT) increases gradually, and likewise VDC (VDA - 41.7mV) ascends along the dotted area as shown in Fig. 3. That is to say, although the digital data is unchanged, the voltage for that data is increased. But, still kept on turning VR106 to have VDC overcome 1V line for the digital data 36 as shown in Fig. 4, it causes the output of the comparator to be turned to "H" and the digital data re-written to 35. Fig. 5 shows that state as being adjusted by turning VR106 clockwise to have CV OUT again to 1.000V.
Still turning VR106 further will repeat the same as above and to rewrite to 34. But, when turned counterclockwise, the data will be rewritten to a larger number each time.

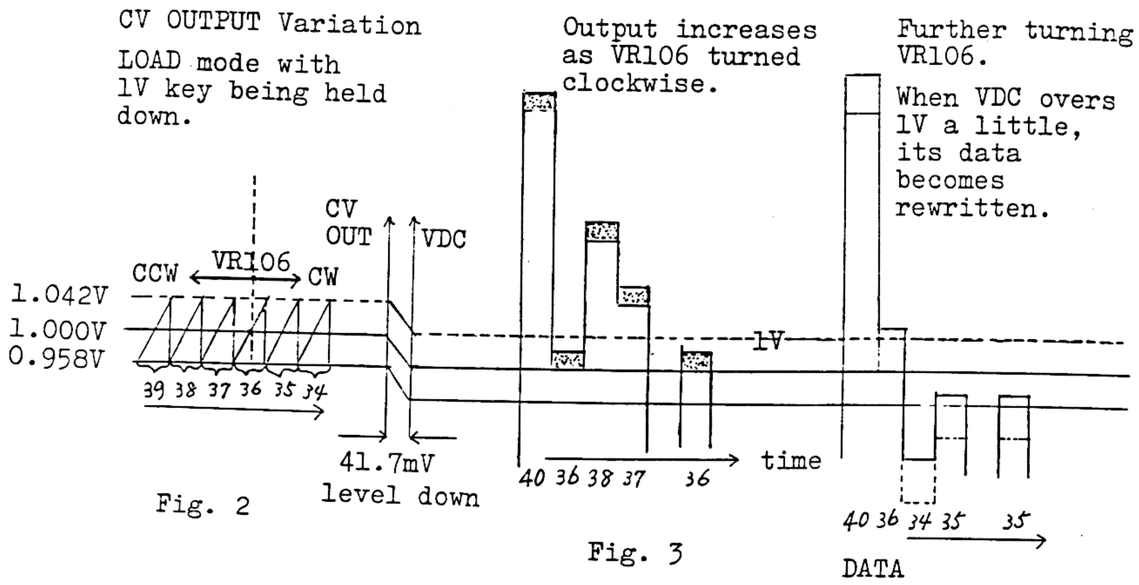


Fig. 2

Fig. 3

Fig. 4

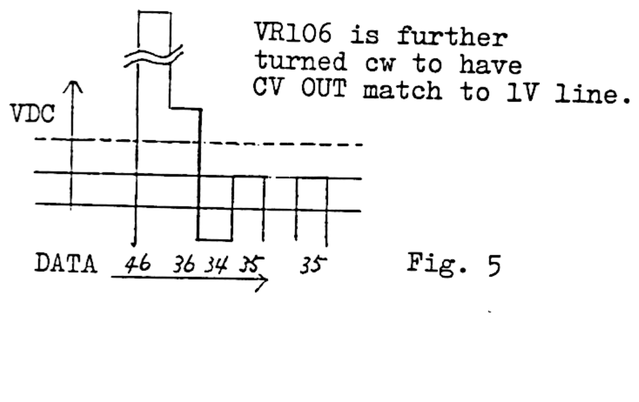


Fig. 5

When watching this on a digital voltmeter connected for observation, the display will be as illustrated in Fig. 2.
Now, suppose that we have turned VR106 a little too far to have the digital data 35 for CV IN of 1V (as in Fig. 5). It is all right and causes no problem as long as we have KCV ADD turned off, because under these circumstance, any shortage or excess of voltage could be compensated for by biasing thru this CV ADJ. potentiometer. But once we have turned KCV ADD on, the whole matter would become different, to be explained on next page.

WHEN DIGITAL DATA IS INCORRECT, ERROR WILL BE PRODUCED on CV OUT. with KCV ADD "ON"

Taking for instance the case of each having CV IN 1V converted into digital 35 (B and C, table below) in place of 36, we will explain as follows:

Note: The topmost numbers in the table refer to those on page 6.

	MODE	2 CVD1	3 substrac-tion	CVD2	4, 5' addition	6 D/A INPUT	7 CV OUT
A	LOAD (normal)	36	24	12	24	36	1V
B	KCV ADD "off"	35	24	11	24	35	1V
C	KCV ADD "on"	35	24	11	*(CVD-24) 47-24=23	34	0.9167V

* This is when the 2V key is depressed so as to have the same pitch on CV OUT with CV IN in memory

Case B is when VR106 is adjusted to reprodece CV OUT of 1V even if in earlier stage the digital data lacks 1.
In this case, since the numbers in preceding subtraction. and subsequent addition are both the same (24), the analog amount at the output receives no effect to differ after A-D-A conversions.

In C, however, despite the fact that the KCV (being pressed) is converted to digital data number short of 1, it is added to RAM-stored-data after subtracting 24. This means that there is a double shortage, bringing after all the shortage by 2 before D/A conversion prior to CV OUT. Through this D/A once again, 1 out of these 2 can be compensated for by VR106, but there is still remained of 1, which brings lack in pitch of a semitone ("1" in digital data) on tone reproduction.
Thus, a maladjustment of VR106 produces a deviation on reproduction when played with KCV ADD "on". Or, it can be said conversely that, through finding such deviation on analog voltage, it is possible to check digital data errors.

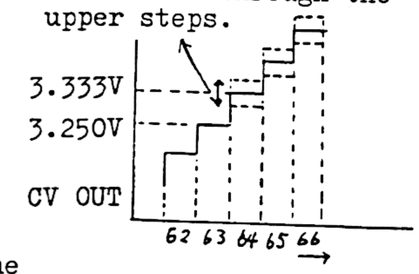
WIDTH ADJUSTMENT with VR105

This potentiometer VR105 is for use to correct the gain of IC113 so as to have D/A in proper relation of 1V/oct, that is, when the data changes by 1, CV OUT changes by 83.3mV.
When VR105 is required for readjustment, it may also be necessary to readjust VR106, since turning either VR results in interaction between adjustments, therefore, both VRs need to be adjusted in turn.
Also care must be exercised to avoid an excessive turn of the VRs which will bring difficulty in performing this adjustment.

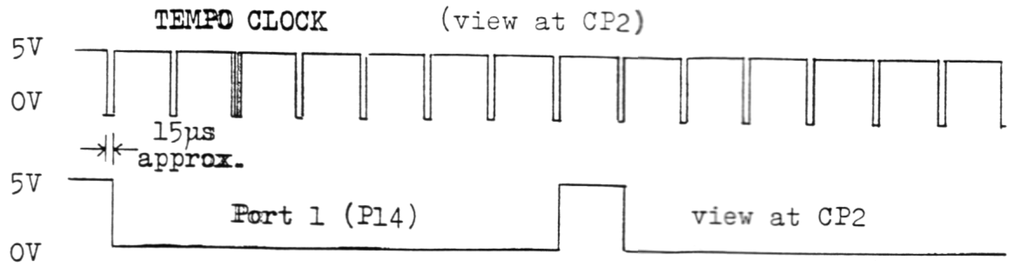
D/A ADJUSTMENT with VR104

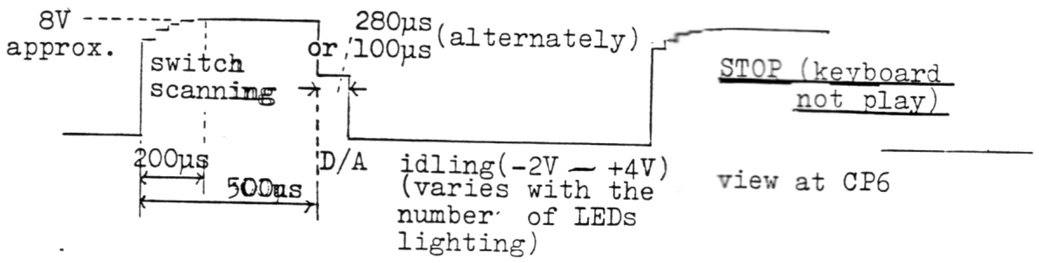
This potentiometer is for the gain adjustment of the D/A amp, and it is in particular for DB6. This DB6 is for the data weighing the most significant bit, so its adjustment is the most critical one and warrants the careful attention. Sources of fluctuation and deviation such as those coming from the preceding stage of IC103, IC104,on impedance or on output voltage,and resistance variation in resistor, etc. are to be compensated for by this VR104.

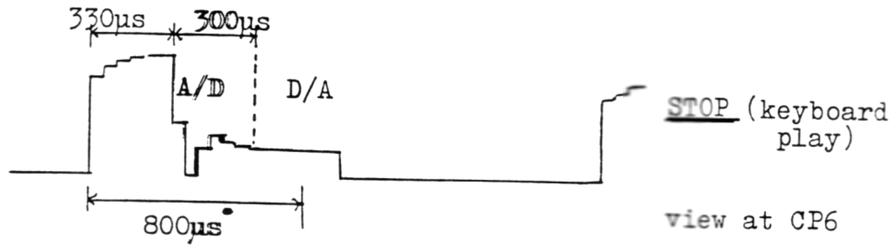
If this step deviates from normal,deviation is carried through the upper steps.

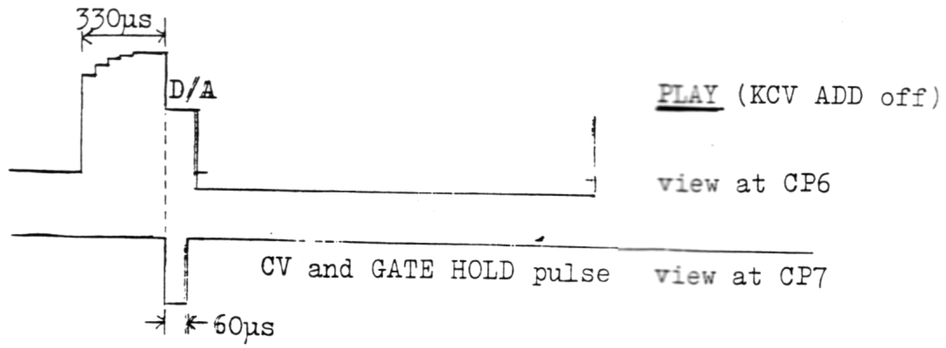


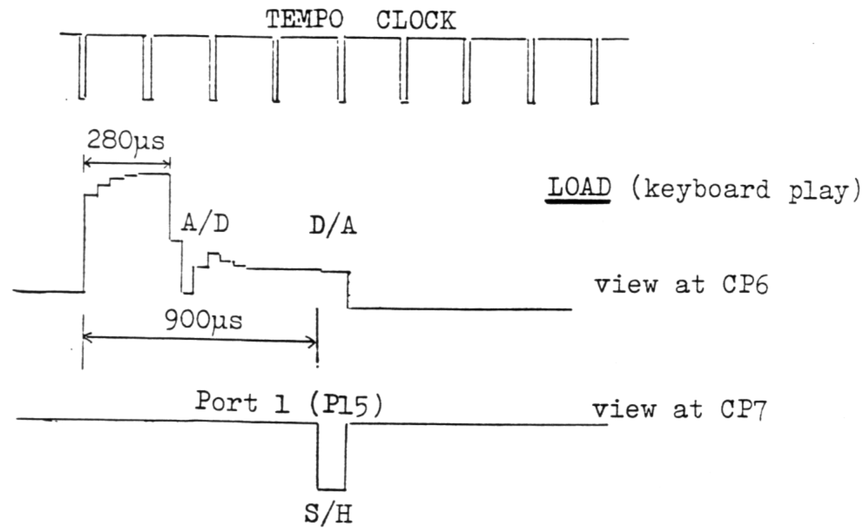
Since the digital data that makes DB6 active is in number over 64 or 3.333V in CV, fluctuation brought through DB6 data will effect all CV of higher voltages as shown in the figure.
In practice, it will be best to adjust VR104 as follows:
Set the LOAD mode and complete both CV ADJ and WIDTH ADJ,then, holding down the key for 4V. Set VR104 so that CV OUT equals 4.000V.

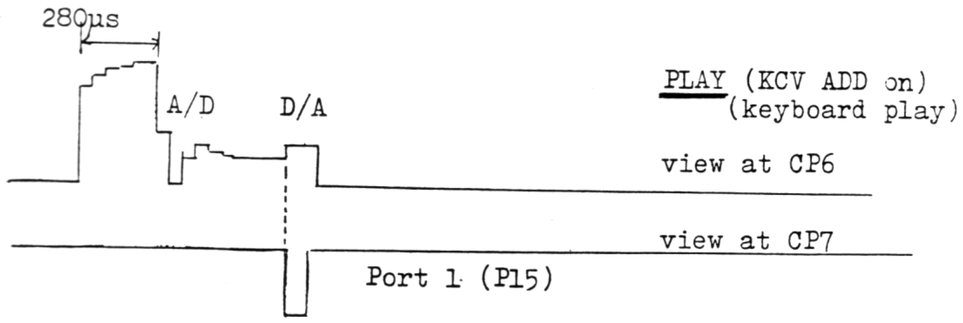

TEMPO CLOCK
(view at CP2)
5V
0V
15μs
approx.
5V
0V
Port 1 (P14)
view at CP2

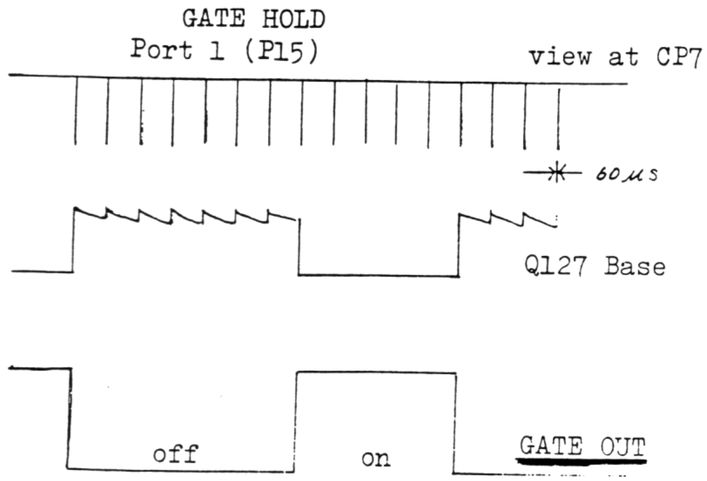

8V
approx.
switch
scanning
280μs
or 100μs
(alternately)
STOP (keyboard
not play)
200μs
500μs
D/A
idling(-2V — +4V)
(varies with the
number of LEDs
lighting)
view at CP6

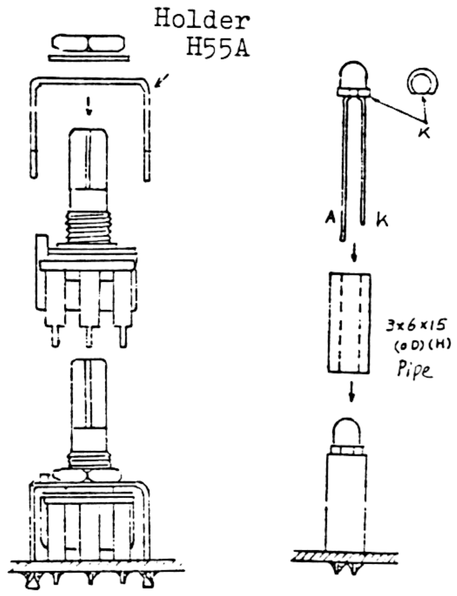

330μs
300μs
A/D
D/A
800μs
STOP (keyboard
play)
view at CP6

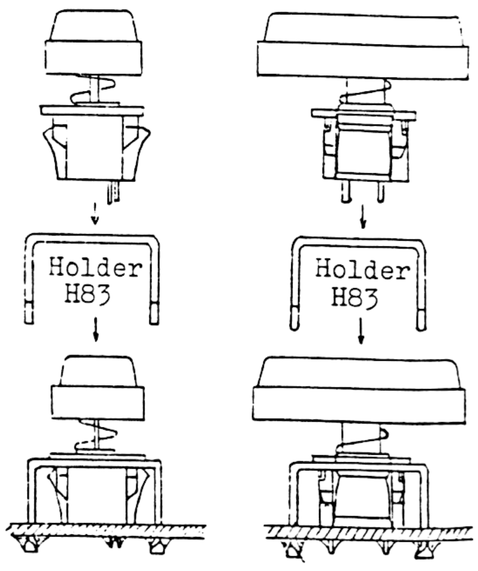

330μs
D/A
PLAY (KCV ADD off)
view at CP6
CV and GATE HOLD pulse
view at CP7
60μs


TEMPO CLOCK
280μs
LOAD (keyboard play)
A/D
D/A
view at CP6
900μs
Port 1 (P15)
view at CP7
S/H


280μs
A/D
D/A
PLAY (KCV ADD on)
(keyboard play)
view at CP6
view at CP7
Port 1 (P15)


GATE HOLD
Port 1 (P15)
view at CP7
60μs
Q127 Base
off
on
GATE OUT

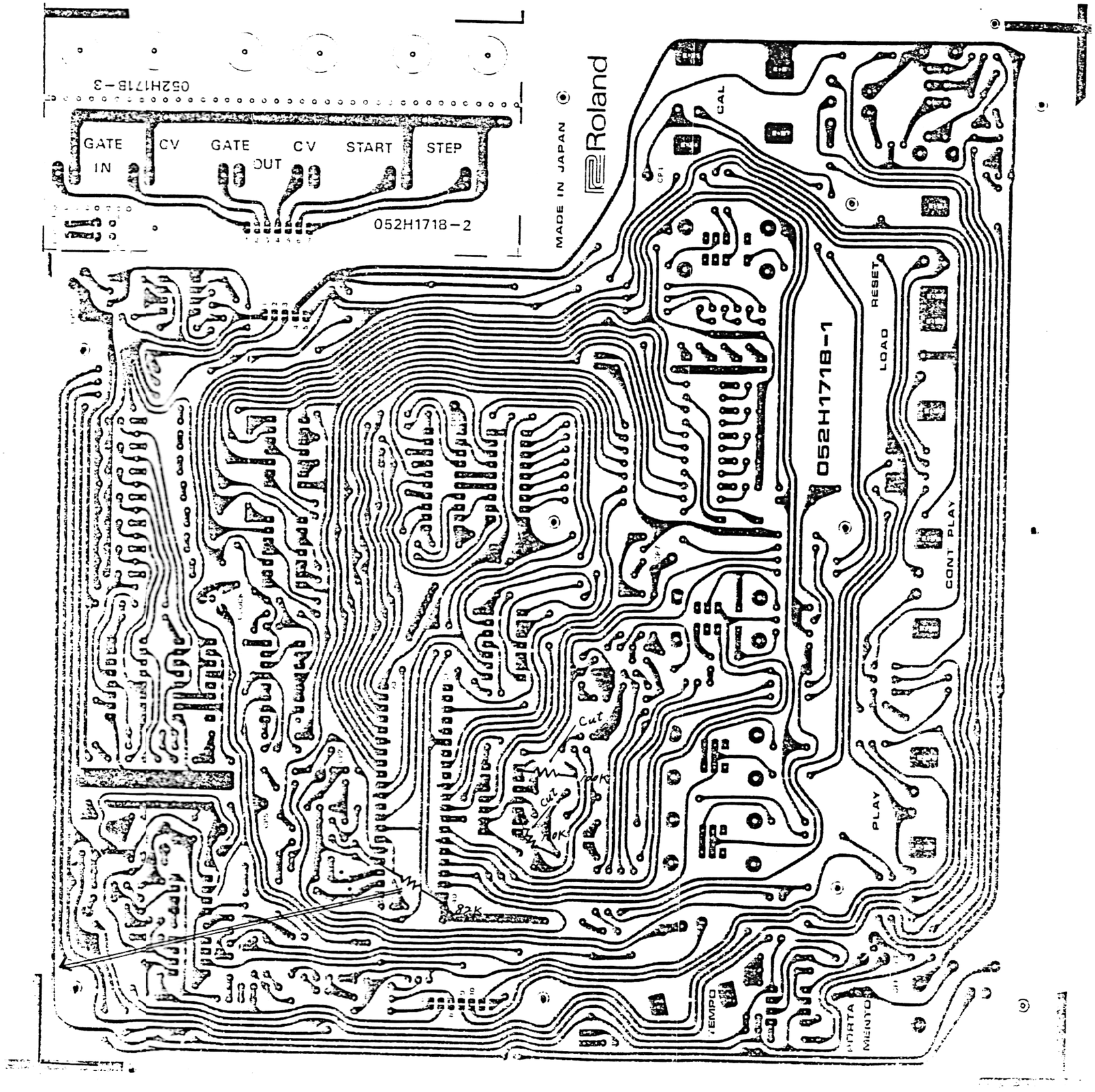




Improvement on RESET SENSE

Increasing C104 capacitance from 1 mfd to 10 mfd may make RESET pulse more stable.

Note: 82k is unnecessary when existing C106 is 0.47/50.



SP101
EAF-
16R02C
EVH-
LWAD25B15

SSB023
-12PN

Jacks SG7622 #08

PUSH CAL

RESET

LOAD

STOP/
CONTINUE
PLAY

PLAY

EVA-LOPC15A26

VM10R
K20B16

5046-07A

OPH31B (149H031B) (052H171B-1)

OPH70B (149H070B) (052H171B-2)

R-25J

CRA¼FX
CRB¼FX (1% 100PPM)

* CRA¼BY (0.1% 50PPM)

** CRA¼DY (0.5% 50PPM)

SR-19R

RJ-6P

2SA733-P or 2SA826-Q

2SC1815GR or 2SC945P

2SK30A-GR

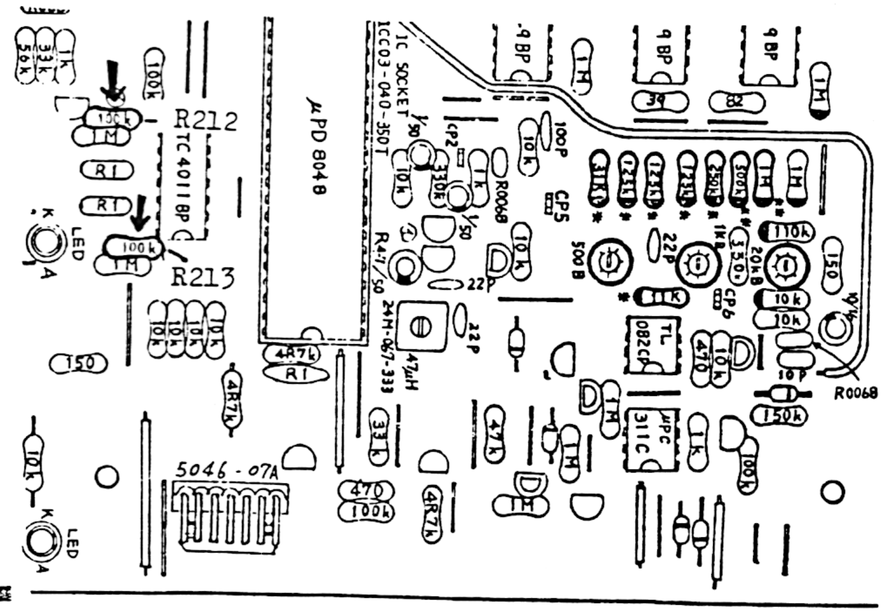
TLR124 (RED)

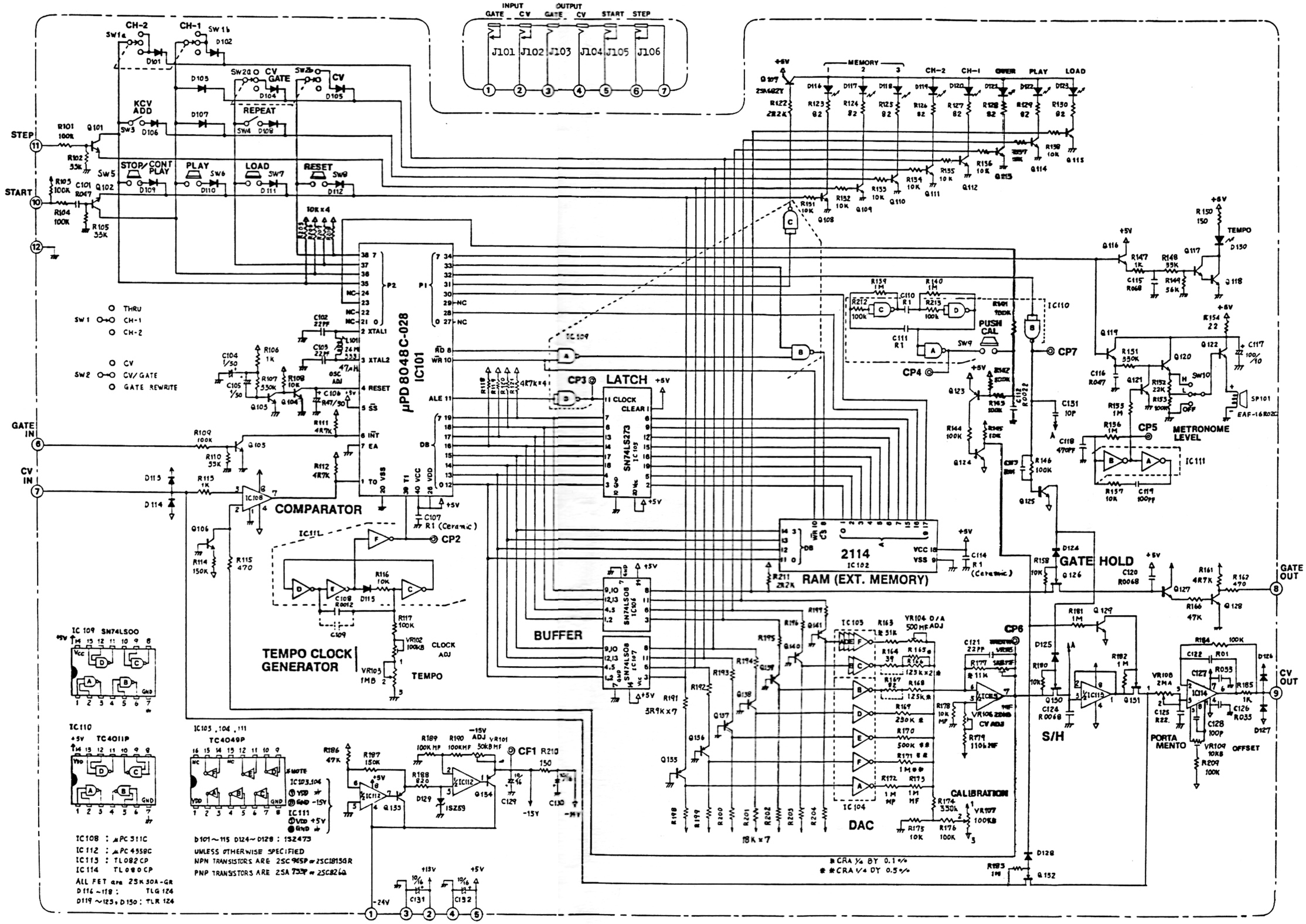
TLG124 (GREEN)

Difference between OPH31's:

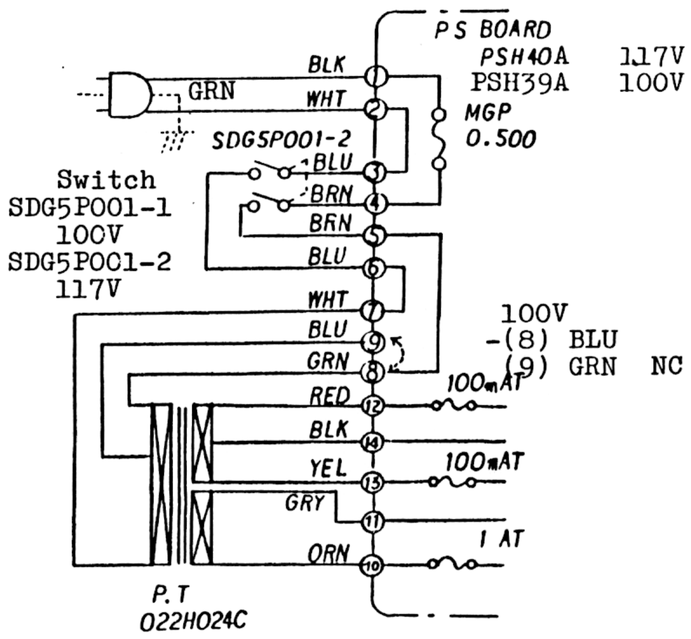
OPH31D - R212, R213 (100K) are mounted on the component side with the pattern provided

OPH31B - Both 100Ks are attached on the foil side with pertinent pattern cut

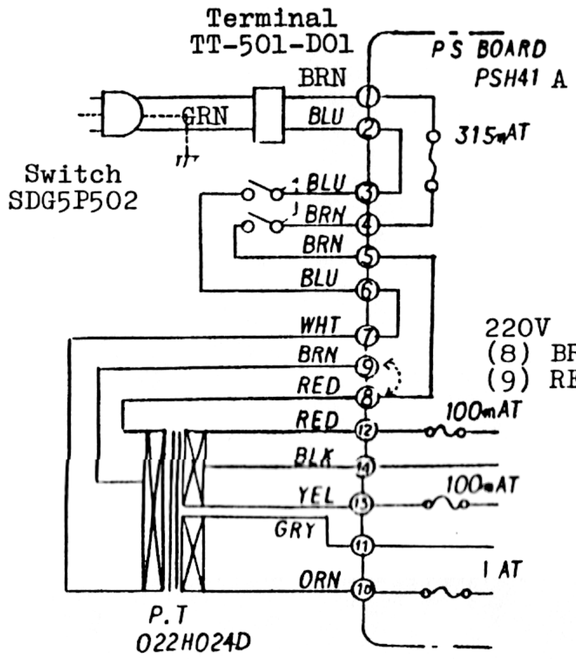



INPUT GATE CV
OUTPUT GATE CV START STEP
J101 J102 J103 J104 J105 J106
CH-2 CH-1
KCV ADD
REPEAT
STOP/CONT PLAY
PLAY
LOAD
RESET
STEP
START
GATE IN
CV IN
MEMORY 2 3 CH-2 CH-1 OVER PLAY LOAD
THRU CH-1 CH-2
CV CV/GATE GATE REWRITE
μPD8048C-028 IC101
LATCH
SN74LS273 IC105
2114 IC102
RAM (EXT. MEMORY)
BUFFER
SN74LS08 IC106
COMPARATOR
TEMPO CLOCK GENERATOR
TEMPO
CLOCK ADJ
DAC
CALIBRATION
PUSH CAL
GATE HOLD
S/H
PORTAMENTO
OFFSET
METRONOME LEVEL
TEMPO
GATE OUT
CV OUT
CP1
CP2
CP3
CP4
CP5
CP6
CP7
IC 109 SN74LS00
IC110 TC4011P
IC105 ,104 ,111 TC4049P
IC108 : μPC311C
IC112 : μPC4558C
IC113 : TL082CP
IC114 : TL080CP
ALL FET are 2SK30A-GR
D116~118 : TLG124
D119~125, D150 : TLR124
D101~115 D124~D128 : 1S2473
UNLESS OTHERWISE SPECIFIED
NPN TRANSISTORS ARE 2SC945P or 2SC1815GR
PNP TRANSISTORS ARE 2SA733P or 2SC828
* CRA 1/4 BY 0.1%
* * CRA 1/4 BY 0.5%

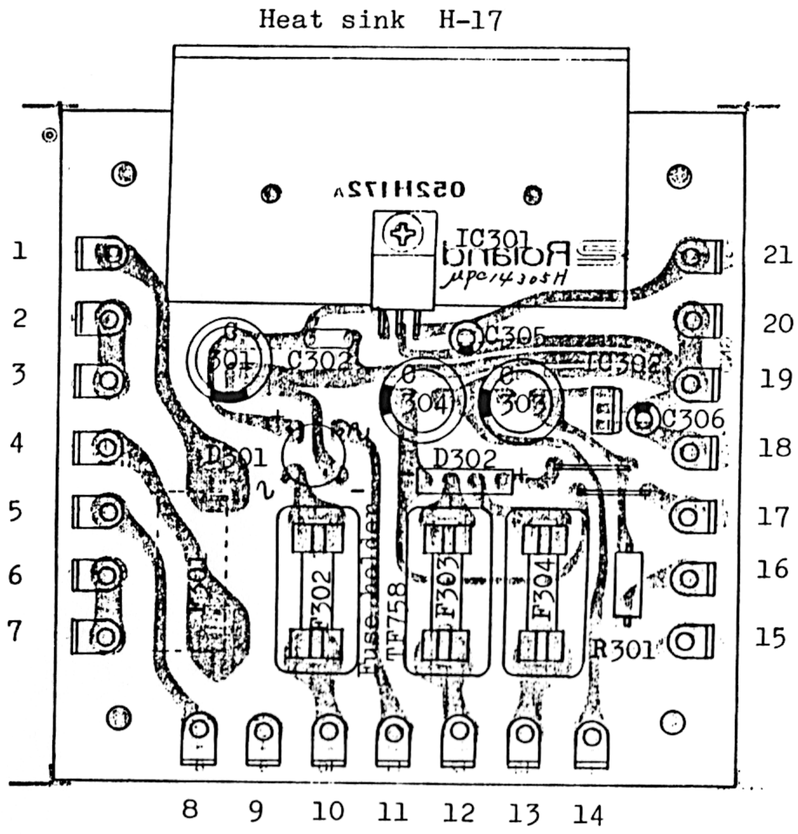
100/117V

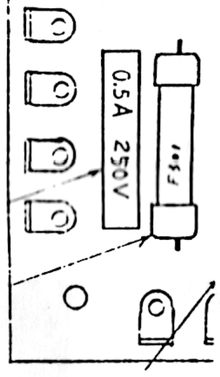


220/240V

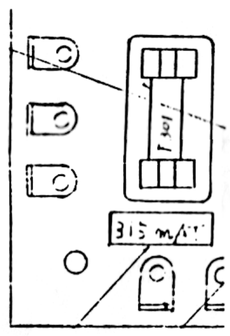


POWER SUPPLY BOARD
PSH39A (146H039A) 100V
PSH40A (146H040A) 117V
PSH41A (146H041A) 220/240V
(Etch mask 052H172A)

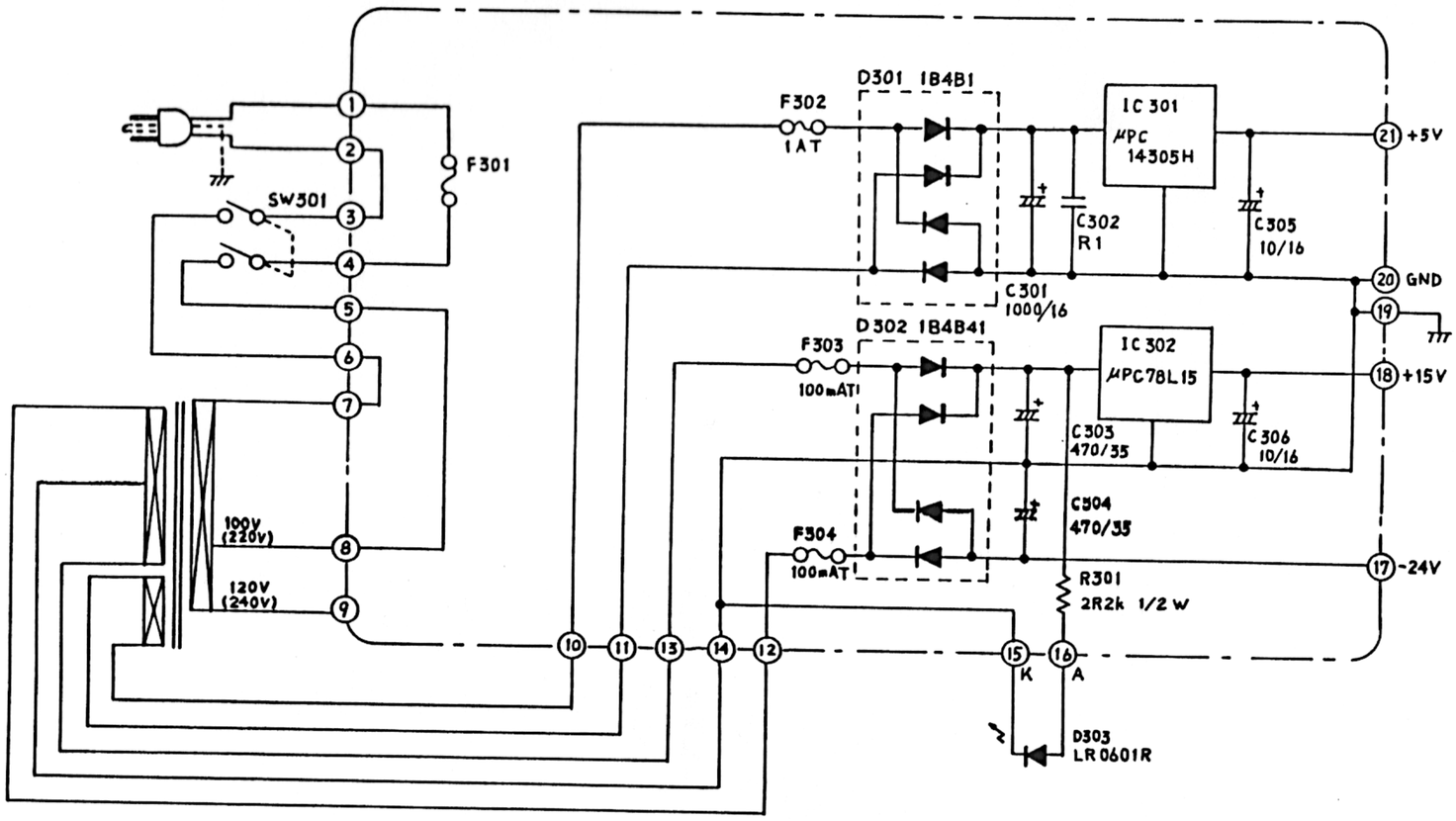




F301:
PSH39/40
MGP 0.500 CSA
(008-040)



F301:
PSH41
SEMKO
T315mA
(008-061)



ADJUSTMENTS

The adjustment is composed of 2 parts: Section I and Section II. It is recommended that the adjustment which is necessitated after the replacement of failing component or others are, as a rule, to be conducted as described in Section I.

Definitions
In this adjustment, the following terms have following meanings,

DVM	Digital Voltmeter
LOAD, PLAY, etc.	Key on the CSQ-100 control panel
2V key, 3V key, etc.	A key on the synthsizer being used, which provides that KCV
TEMPO, CAL, FAST, etc. (capital letters)	Control, switch, jack, legend on the CSQ-100
SCOPE	Oscilloscope
CP1, CP2, etc.	Check point on the PCB.

Note: Before attempting adjustment, warm-up period for no less than 10 minutes should be given.

CAUTION: Care must be taken not to turn the adjusting potentiometers excessively.

SECTION I

Adjustment is usually necessary only after replacing parts.

CALIBRATION PROCEDURES

After replacement of		Connect,- to	Adjust or Check	for (remark)
IC101 (μPD8048) L101 (47uH)	1.	Frequency counter, CP3	L101	365kHz ± 10kHz (8048 Clock frequency)
IC110 (TC4011P)	2.	Scope, CP4		(waveform check)
IC111 (TC4049P,	3.	Frequency counter, CP2	VR102 Clock Adj.	(Tempo clock frequency) 4.7kHz ± 5% with TEMPO at FAST
Check that frequency is 0.7kHz $^{+5\%}_{-10\%}$ with TEMPO set at SLOW. If this range deviates, readjust VR102 with TEMPO at FAST within the range of 4.7kHz ± 5%. Or, vary the capacitance of C109.				
IC114 (TL080CP)		No connection at CV IN jack	VR109 Offset	(Depress RESET)
	4.	CV OUT, DVM		0 ± 0.5mV
IC112 (μPD4558) D129 (1SZ59)	5.	DVM, CP1	VR101 -15V Adj.	-15V ± 2mV
Note: Since any variation in the DC supplies will have the most pronounced effect on the DA converter, check CV OUT for error through the next steps (6).				
IC103, IC104 (TC4049) IC113 (TL082-P)		CV IN, GATE IN, Synth's CV GATE out	VR106 CV Adj.	(DA Adj.) CAUTION: Adjustment of the DA converter is very subtle. Always rotate ADJ. pots by slow degrees, excessive turn will bring great difficulty into the subsequent adjustment attempts,requring a waste of time.
	6.	DVM, CV OUT		

Setting:

PORTAMENT on the synthesizer ------- Off or minimum
LOAD MODE ---------- CV/GATE
MEMORY ---------- CH-1
PLAY MODE ---------- KCV ADD ON
REPEAT
TEMPO ---------- center
PORTAMENT ---------- 0
CALIBRATION (knob) ---------- center

(Continuation of Step 6 from previous page)

6-1. Press RESET and LOAD.

6-2. Depress the 2V key, DVM must read 2.000V ± 3mV.
When DVM reads within 3mV, adjust CALIBRATION pot for 2V CV OUT with PUSH CAL depressed. Then proceed to 6-3, 6-4.
If reading is outside ± 3mV range, set CALIBRATION pot at center, and adjust VR106 (CV Adj.) for 2.000V ± 3mV reading.

6-3. Verification of KCV ADD function
While depressing the 2V key, push PLAY. DVM must read the same.

A. If reading changes, it means that VR106 (CV Adj.) has been set at incorrect point. Proceed to Section II

B. When the reading is steady, make sure that DVM readings are within the ranges in the table shown below with respective key depressed.(RESET-LOAD-2V key-PLAY-2V key-3V key-4V key)

key being depressed	DVM reading (CV OUT)
2V	2.000V ± 2mV
3V	3.000 ± 2mV
4V	4.000V ± 2mV

If any of the readings exists outside the limit, make asjustment under SECTION II, 1-6.

6-4. Press RESET and LOAD.
While depressing 4V key, press PLAY.
DVM must read 6.000V ± 3mV. If not, proceed to SECTION II, 1-7.

SECTION II

1. ADJUSTING DA CONVERTER

Some procedures are the same as described under Section I.
In the following steps, adjustment should be made with specified key being depressed.

1-1. Connection and Settings: Follow the instruction "6" in Section I.

1-2. Press RESET and LOAD.

1-3. While depressing 2V key, adjust VR106 (CV Adj.) for 2.000V reading. then, press PLAY.

A. If the reading stays unchanged, proceed to step 1-6.

B. If it changes, proceed to step 1-4. (note the reading)

1-4. Press RESET, LOAD and 2V key.
While depressing the 2V key, adjust VR106 for a following "2"V according to the deviation noted at step 1-3,B.
As discussed earlier (RELATIONSHIP, CV ADJ and DATA), DVM reading will repeat the cycle of 2V ± 41mV as VR106 being turned.
Ordinal number in the right colum of the table below shows number of repetition.

DVM reading at step 1-3,B (approx)	Turn VR106 in this direction	Stop turning when DVM reads 2.000V of
2.083V	clockwise	1st
2.167V	clockwise	2nd
2.250V	clockwise	3rd
1.917V	counterclockwise	1st
1.833V	counterclockwise	2nd
1.750V	counterclockwise	3rd

1-5. Press RESET, LOAD, 2V key and PLAY. (2V key held down)
DVM must keep the same reading.

1-6. Press RESET and LOAD.

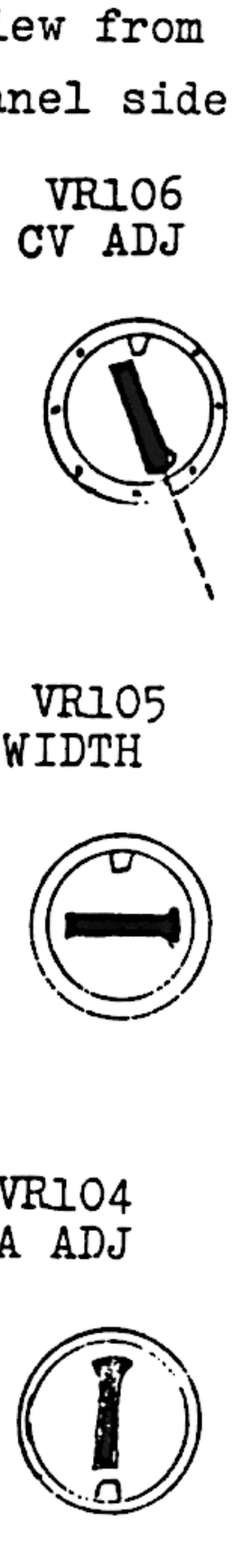
	key to be pressed	adjust	for reading	
1-61	3V	VR105(WIDTH)	3.000V	repeat until DVM reads
1-62	2V	VR106(CV Adj)	2.000V	3.000V and 2.000V
1-63	4V	VR104(DA Adj)	4.000V	repeat until respective
1-64	2V	VR106	2.000V	voltages are displayed
1-65	3V	VR105	3.000V	on DVM

1-7. Press RESET, LOAD, 4V key (holding down) and PLAY.
DVM should read 6.000V ± 2mV.

1-8. If DVM proves that deviation is outside this range, it may be cured by turning VR105, but this adjustment will affect steps 1-64,1-65.
Turn VR105 within the limit of 2.000V ± 2mV and 3.000V ± 2mV.

2. CHECKING CV OUT
With DVM connected to CV OUT and LOAD pressed.
Check tha DVM readings for 1V/oct through entire keyboard.

Note: When difficulties arise in relation to WIDTH and CV adjustment, VR104, VR105 and/or VR106 might have been set too far from their proper position.
Reset them to the approximate positions illustrated in figure right.
Adjust again from appropriate step.



072H049	Panel H49
066H021	Side block H21 set of L and R
061H080	Chassis H80
068-020	Bushing no.20 panel
111-021	Rubber Foot G-5 rear
111-023	Rubber Foot G-7 front
016-008	Button no.8 gray power switch
016-057	Knob no.57 TEMPO
016-033	Knob no.33 PORTAMENTO
063-012	Strip no.12 knob no.33

POWER TRANSFORMERS

022H024C	100V/117V
022H024D	220V/240V
022-136	Coil 24M-067-033 47μH
009-012	Jack SG7622 no.8 mono
068-018	Bushing no.18 red jack
068-005	Bushing no.5 jack
121-005	Washer no.5 jack

FUSES

008-040	MGP 0.500 CSA prim 117V
008-061	SEMKO T315mA prim. 220/240V
008-056	SEMKO T100mA sec.
008-066	SEMKO T1A sec.
012-003	Fuse clip TF758

SWITCHES

001-215	SDG5P 001-1 power 100V
001-216	SDG5P 001-2 power 117V
001-217	SDG5P 502 power 220/240V
001-068	SLE-622-18PS lever
001-201	SLE-623-18PS lever
001-183	SSB-023-12PN slide
001-276	SCK41167 key
001-275	SCK41168 key

PCBs

149H031D	OPH31D (052H171D-1)	
149H070D	OPH70D (052H171D-2)	
146H039A	PSH39A (052H172A)	100V
146H040A	PSH40A (052H172A)	117V
146H041A	PSH41A (052H172A)	220/240V
048H017	Heat sink H17 PSH-	
042-039	Check point 59BS8806	

POTENTIOMETERS

029-577	EVALOPC15A26 2MA slide PORTAMENTO
030-951	EVHLWAD25B15 100KB CALIBRATION
028-766	VM10RK20B16 1MB TEMPO
030-465	SR19R 10KB trimmer
030-471	SR19R 100KB trimmer
030-644	RJ-6P 500B trimmer
030-645	RJ-6P 1KB trimmer
030-646	RJ-6P 50KB trimmer

RESISTORS

044-927	CRA¼BY	11K	0.1%	50PPM
044-932	CRA¼BY	31K	0.1%	50PPM
044-929	CRA¼BY	125K	0.1%	50PPM
044-930	CRA¼BY	250K	0.1%	50PPM
044-972	CRA¼DY	500K	0.5%	50PPM
044-973	CRA¼DY	1M	0.5%	50PPM
044-838	CRB¼FX	10K	1%	
044-846	CRB¼FX	100K	1%	
044-860	CRA¼FX	1M	1%	

CAPACITOR

037-035	Disk seramic 0.1 mfd +80 % -20	12V

SEMICONDUCTORS

LSIs

179-028	μPD8048C-028 8-bit microcomputer or μPD8048C-077 can be interchanged	
020-202	μPD2114LC	RAM

ICs

020-203	SN74LS00N	
020-204	SN74LS273N	
020-120	SN74LS08N	
020-040	TC4011BP	
020-075	TC4049BP	
020-199	μPC311C	
020-100	TL082CP	
020-200	TL080CP	
020-097	μPC4558C	
020-205	μPC14305	+5V regulator
020-206	μPC78L15	+15V regulator

TRANSISTORS

017-016	2SK30A-GR	FET
017-106	2SC1815-GR	
017-024	2SA733-P	
017-034	2SA682-Y	

DIODES

018-014	1S2473	
018-097	1SZ59 temperatue compensated	zener
018-089	1B4B41	rectifier stack
018-	1B4B1	rectifier stack

LEDs

019-028	TLR-124	red
019-029	TLG-124	green
019-009	LR0601R	red

WAFER TERMINALS, TERMINAL, WIRING ASSEMBLIES

010-195	Terminal 5046-05A	
010-196	Ternimal 5046-07A	
042-032	Terminal TT 501-D01 line cable	
053H046	Wiring Assy	A
053H047	Wiring Assy	B
053H048	Wiring Assy	C

MISCELLANEOUS

065H050	Dust cover H50
120-001	Long nut no.1 3x10mm
120-003	Long nut no.3 3x18mm (stand-off or spacer)
012-043	IC Socket ICC030-040-350T (uPD8048)
064H076	Holder H76
064H055A	Holder H55A
064H083	Holder H83

Commonly available parts:
Resistors of 1/4W, 5%,
Mylars,
Electrolytics
are omitted.