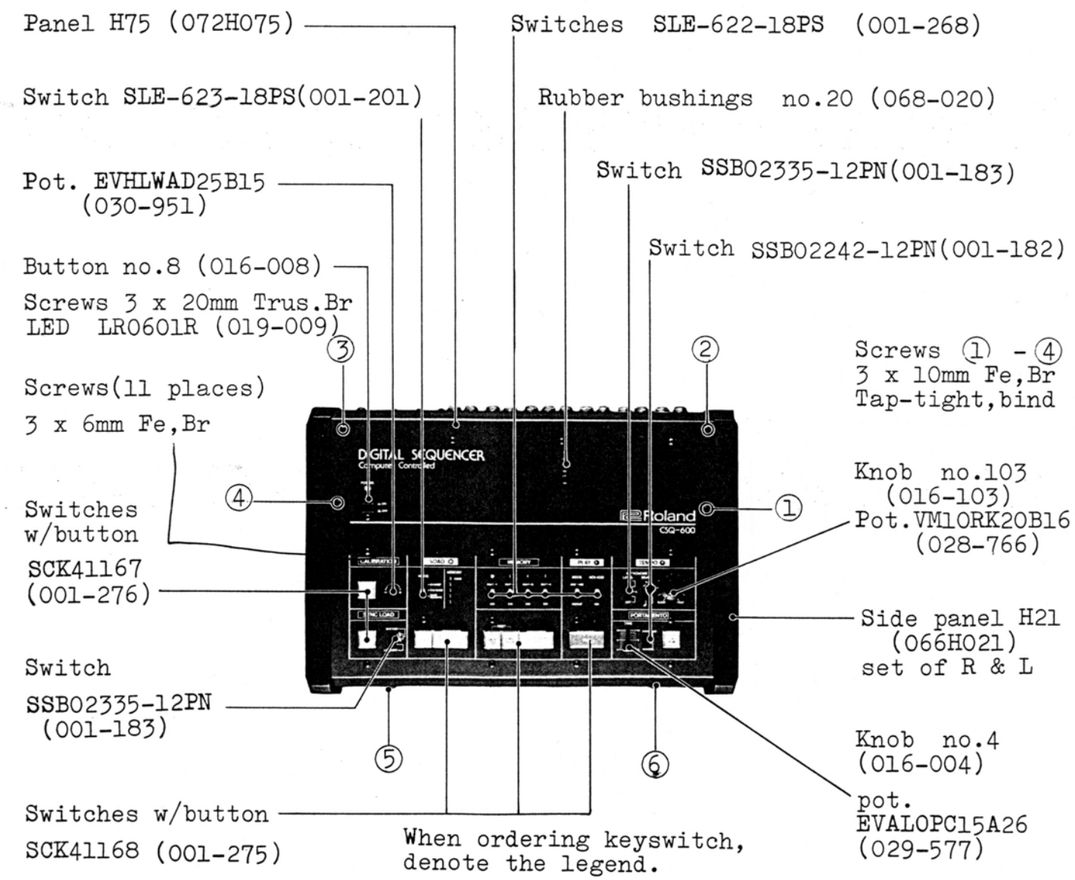
CSQ-600 SERVICE NOTES

First Edittion

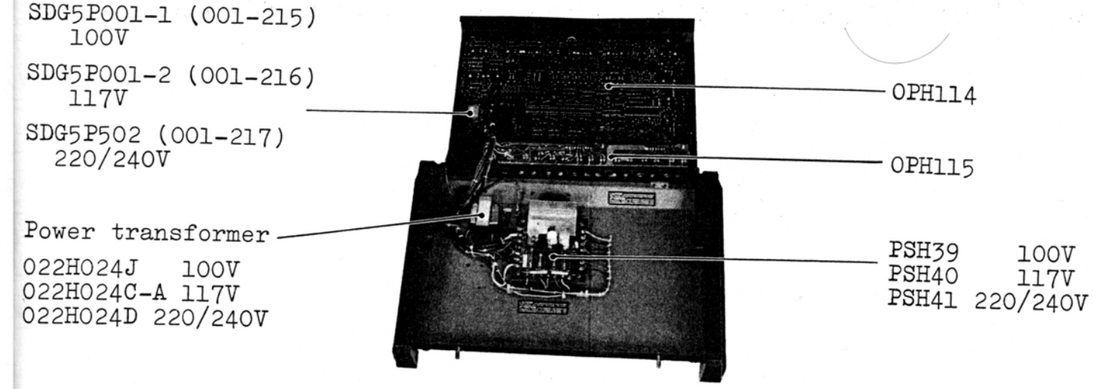
Maximum storage capacity -----	600 notes (150 notes/part x 4)
CV ------- Input - 1V/oct, 0V to +5V;	Output - 1V/oct, -2V to +8V
GATE ----- Input - Threshold +2.5V;	Output - Off: 0V, On: +15V
CLOCK ----------	Output & Input - 700Hz to 4.7kHz
STEP PULSE INPUT ----------	Threshold +2.5V
START & STOP PULSES INPUT ----	Close-Open or +15V
START PULSE OUTPUT ----------	Normal: 0V, LOAD or PLAY: +15V
STOP PULSE OUTPUT ----------	Normal: +15V, LOAD or PLAY: 0V
Power consumption ----------	8 watts
Dimensions ----------	450 (W) x 305 (D) x 95 (H) mm 17.7 x 12.0 x 3.7 in
Weight ----------	3.8 kg 8.58 lbs



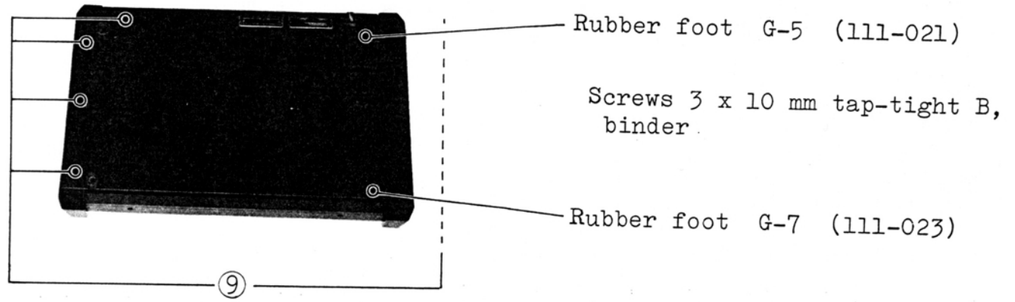
DISASSEMBLY

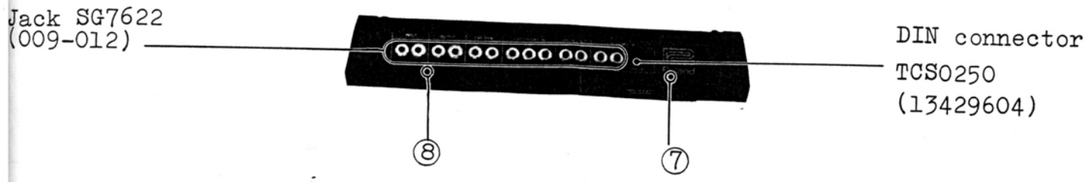
TO AVOID ABRASION on inside surfaces of side panels, open the top and side panels simultaneously by removing the screws indicated with circled numbers, except ① - ④.

OPH114 can be removed off the top panel by unscrewing at the foil side and by pulling out TEMPO and TIME knobs on the top panel.



* In ordering PCB replacement, suffix alphabet to the name , if any.





μPD8048C

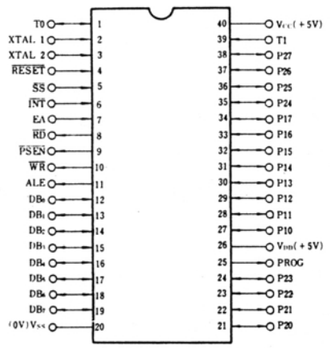
Designation		Pin No.	Function
DB (Data bus)	0	12	CV data
	1	13	CV data
	2	14	CV data
	3	15	Switching scanning
	4	16	LED
	5	17	RAM address
	6	18	CV and GATE data during RAM address
	7	19	Output Gate signal
P 1 (Port 1)	0	27	RAM address, LED select
	1	28	RAM address
	2	29	RAM address
	3	30	RAM address
	4	31	LED timing
	5	32	Output CV S/H, Gate hold timing
	6	33	RAM CS enable
	7	34	Metronome timing
P 2 (Port 2)	0	21	...
	1	22	...
	2	23	CV IN by-pass enable during the STOP mode
	3	24	Portamento ON/OFF
	4	35	Read switches status during switch scanning
	5	36	
	6	37	
	7	38	
RESET		4	Input to reset the 8048 when power is ON
INT		6	External gate input
TO		1	Digital data input during A-D conversion
T1		39	Accepts TEMPO clock output
XTAL 1		2	External source inputs for internal oscillator
XTAL 2		3	

μPD8048C-077 & μPD8048C-256
Difference in Function between the Two in STOP MODE

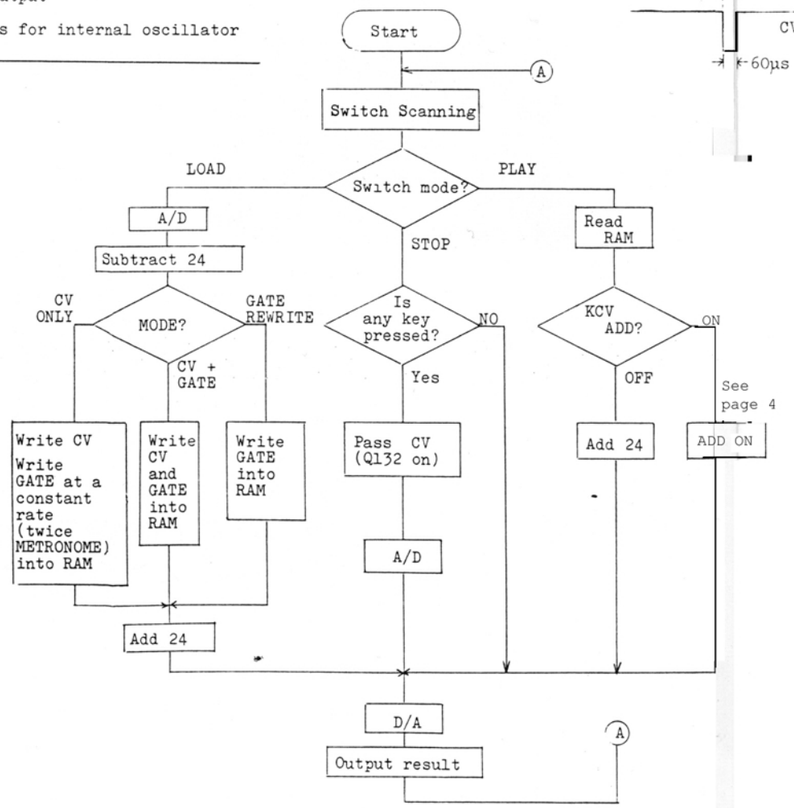
-077
Accesses to another memory chip upon PART switches resettings.

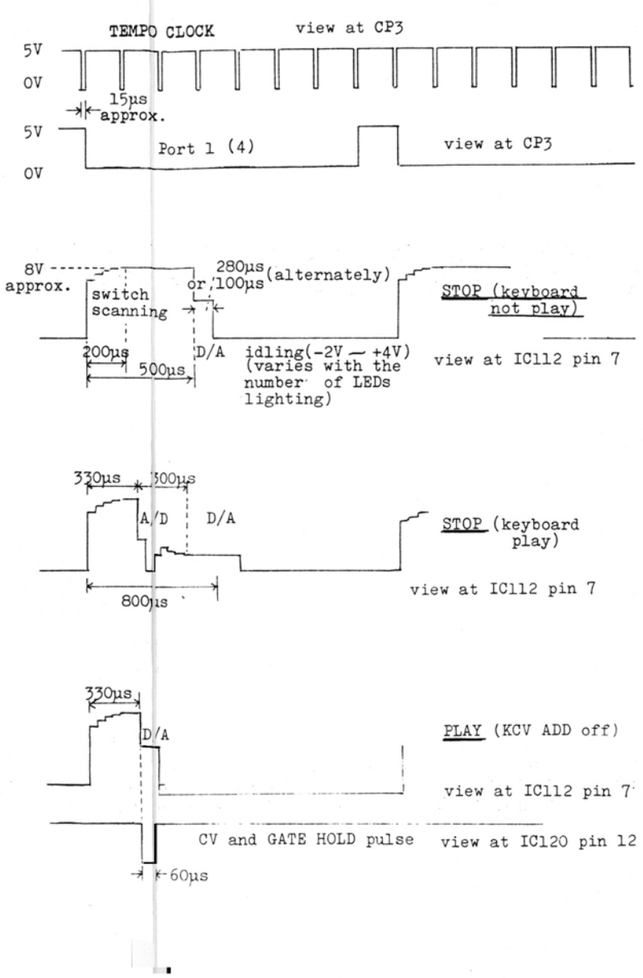
-256
Keeps the same PART until PLAY or LOAD is pressed.

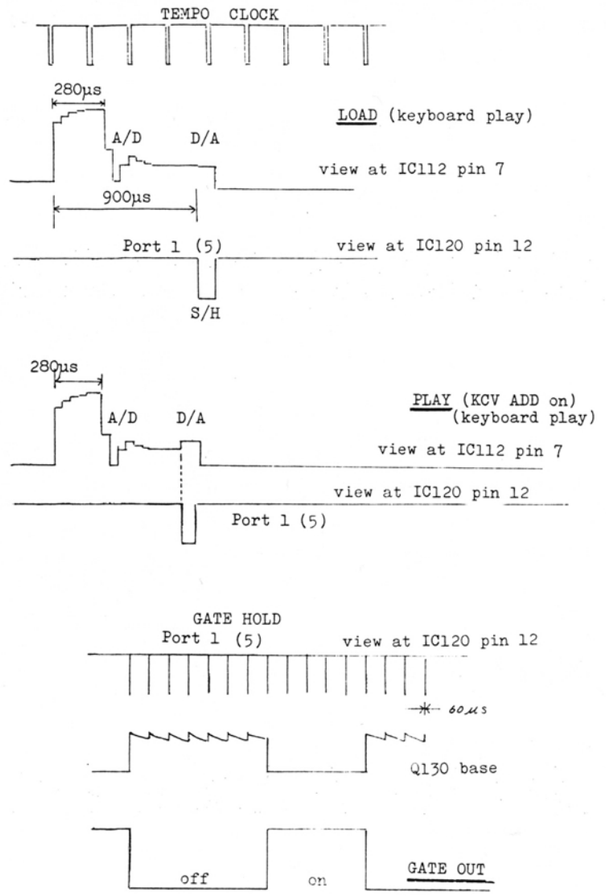
(Top View)



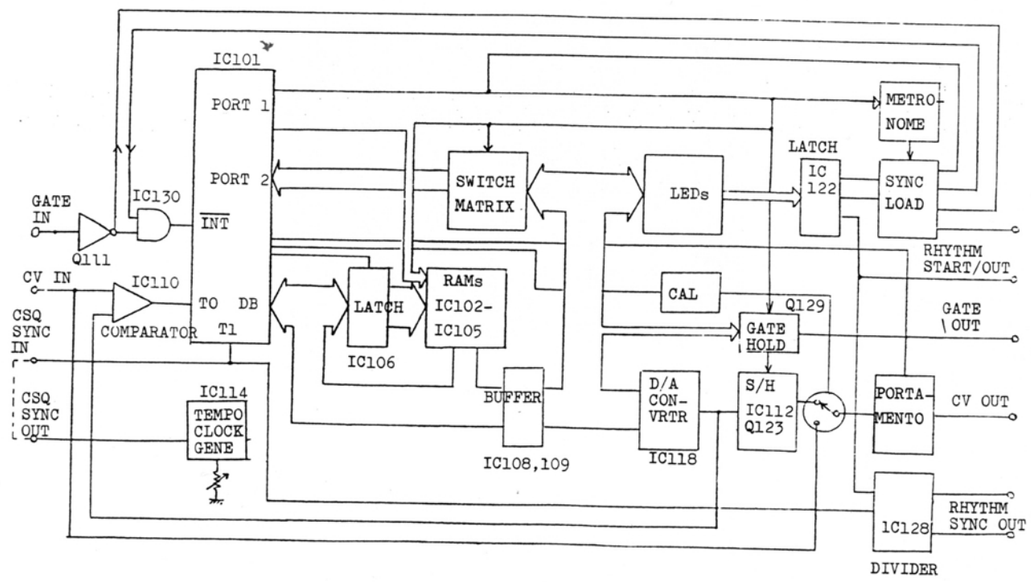
The μPD8048 is an 8-bit parallel computer fabricated on a single sillicon chip. The 8048 contains a 1k x 8 ROM program memory, 27 I/O lines, an 8-bit timer/counter and clock circuits.
Used in the CSQ-600 is a μPD8048C-077 or 256 version. Program and data dedicated to the CSQ-600 are stored in the resident memory.







BLOCK DIAGRAM



CIRCUIT DESCRIPTION

This description is composed of two parts: the General description which outlines the functions of CSQ-600, and the Details which centers around A/D and D/A converters since these are practically the heat of this unit. Complete understanding of A/D and D/A conversion circuits will be a great help in performing adjustments in Section II. Also described in Details are functions of SYNC LOAD and RHYTHM SYNC circuits.

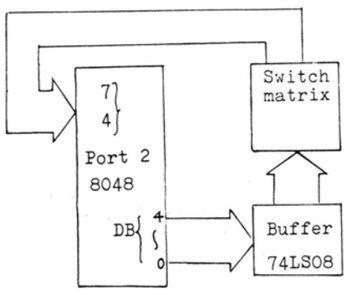
Function of "One chip computer"
μPD8048

CSQ-600 performs its functions with μPD-8048 at the center position for all, including the following in its performance cycles:

1. Switch Scanning
2. D/A Conversion
3. A/D Conversion
4. Write/Read of Data to or from External RAM
5. Timing for Lighting LED Indicator
6. Triggering of METRONOME
7. Holding of GATE OUT

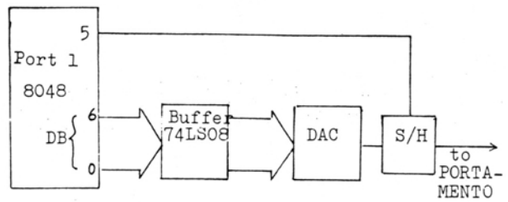
GENERAL

1. SWITCH SCANNING



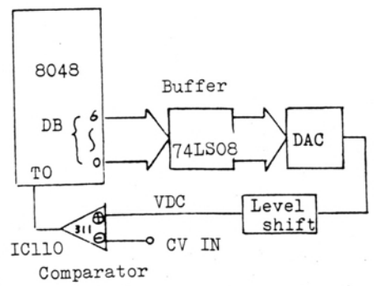
μPD8048 starts its running cycles beginning with switch scanning. Into DB0-DB4(data bus) of 8048, 5-bit signals are being output in accordance with the resident program, which are then brought to the switch matrix via the buffer. At first, L is output from DB4 while having H from other DB0 to DB3. At the next instant DB3 becomes L while DB4 to H; and still next L on DB2 and so on, repeating such output changes 5 times on these bit signal combinations. Depending on which key is depressed or in what position the switches are, corresponding signals are fed back through 4-7 on Port 2.

2. D/A CONVERSION -Digital to Analog -



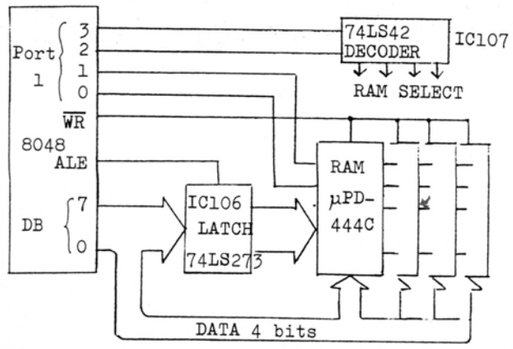
The D/A Converter transforms the sequential data (switch scanning, RAM address, CVs, etc.), which are being output from the 8048 through internal programming, into analog voltages.
Since the D/A converter (DAC) employed here is a summing type, with a weight-resistor-tree connected to an inverting input of an op amp, each bit in the digital data is converted to an analog voltage in value to double the one immediately subordinate to each. When CV data are on output, pulses synchronized with CV data are supplied from no.5 of port 1 to the Sample and Hold (S/H) circuit, and the analog CV voltage corresponds to the data are held on C121.

3. A/D CONVERSION - Analog to Digital -



Since the CV IN is an analog voltage, it must be converted to digital data for making the storing in RAM possible.
The method employed in the CSQ-600 is called "successive approximation conversion" where each bit, from DB6 (for MSB: most significant bit) to DB0 (LSB: least significant bit), is being set successively to output "1" which, after being D/A converted, is to be compared with CV IN at the comparator (311).
The comparator will then output "0" (low) if CV > VDC, or "1" (high) if CV < VDC, onto TO. When H is output to TO, the corresponding digital data is "reset" and becomes 0. Such "set" and "reset" is repeated 7 times for bits from DB6 to DB0 and with the resultant value from such "set" and "reset", the digital data of the CV IN is produced.

4. ADDRESSING EXTERNAL DATA MEMORY



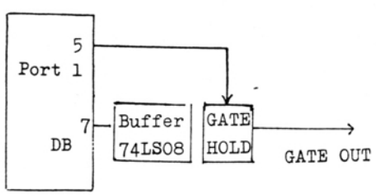
Although the data are 8-bit format, they are divided into two groups of 4-bits, upper and lower 4 bits, and are written/read into separately from external RAMs(μPD444C). Storage locations for PARTs are as follows. Every block consists of 256 bytes.

* μPD444 is a 1k-byte (1k-word by 4-bit) CMOS RAM organized as 256-byte x 4.
1k = 1024, 4096 bits

LOWER HALF		UPPER HALF	
IC102	IC103(*)	IC104(*)	IC105
PART 1	PART 3	PART 1	PART 3
PART 1	PART 3	PART 1	PART 3
PART 2	PART 4	PART 2	PART 4
PART 2	PART 4	PART 2	PART 4

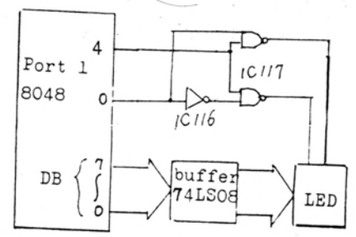
Decoded signals from Port 1 nos. 2 and 3 select a RAM.
Signals from Port 1 nos. 0 and 1 select a chip in the RAM.
Address signals from DB, latched on IC106 by ALE, select memory cells in the chip.
When $\overline{WR}$ goes low, the data are written into, and when high, read from the cells.

5. GATE HOLD



From DB7, the GATE signals are also being output. They are held by the signal (the same as for S/H) to become output of GATE signal.

6. LIGHTING of LEDs

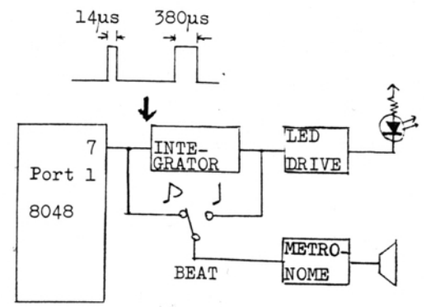


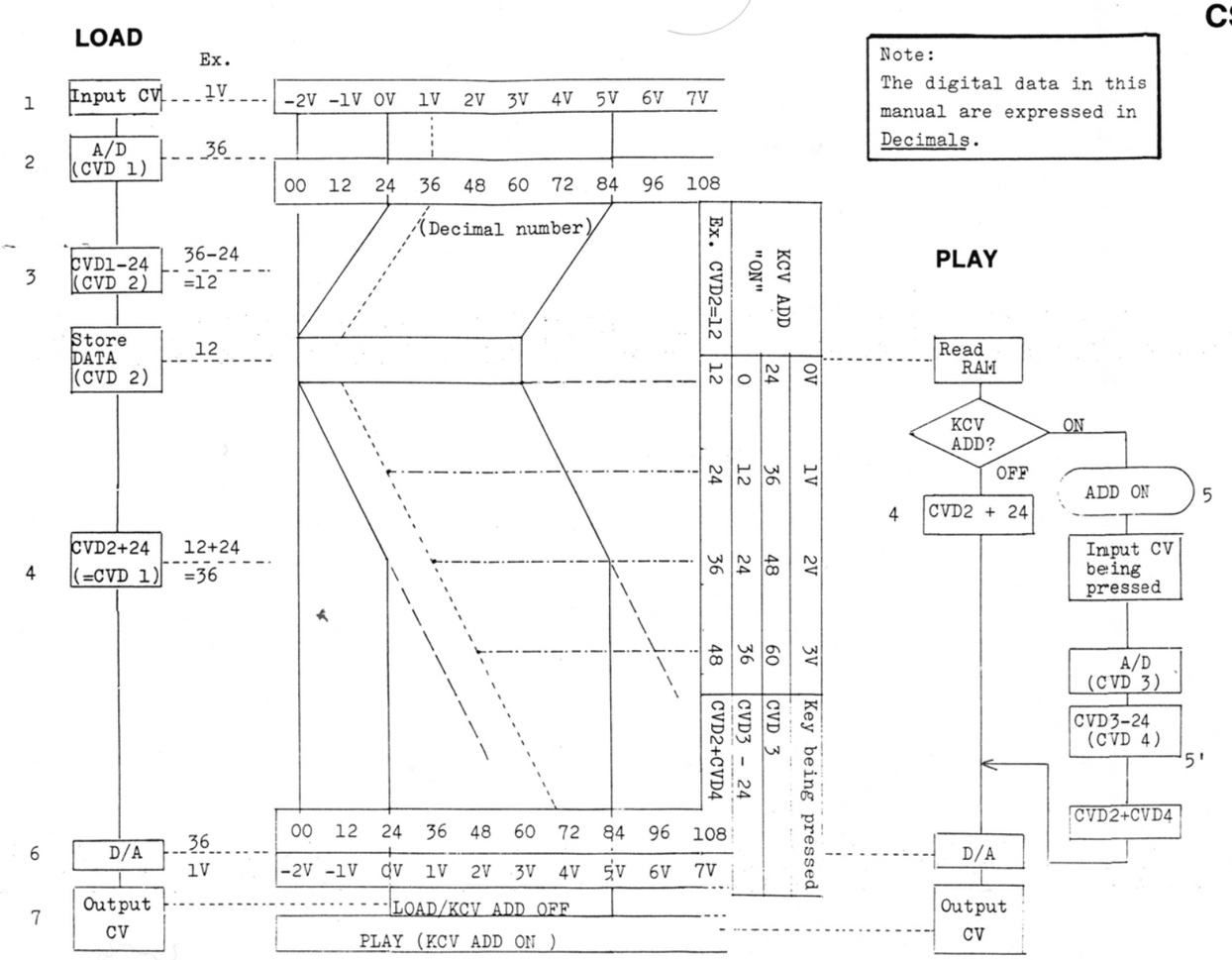
Signals for lighting LEDs (except TEMPO) are supplied from DB. However, various signals are transferred over DB lines at every instance, timing pulses are given from Port 1 nos. 0 and 4 to control the LEDs being driven when there are lighting signals.
The pulses are synchronized with those of TEMPO CLOCK GENERATOR and are output at a rate of one pulse for every eight CLOCK pulses. Because of this, lighting on/off cycling rate is also changed along with change in TEMPO, but the current amount to LED is still being kept unchanged through a means to maintain duty ratio constant.

(*)REMARK: According to my measurements there is a typo:
IC104 is LOWER HALF for Part3 and 4 - IC103 is UPPER HALF for Part 1 and 2.
Lower Half is most significant nibble, Upper Half is least significant nibble

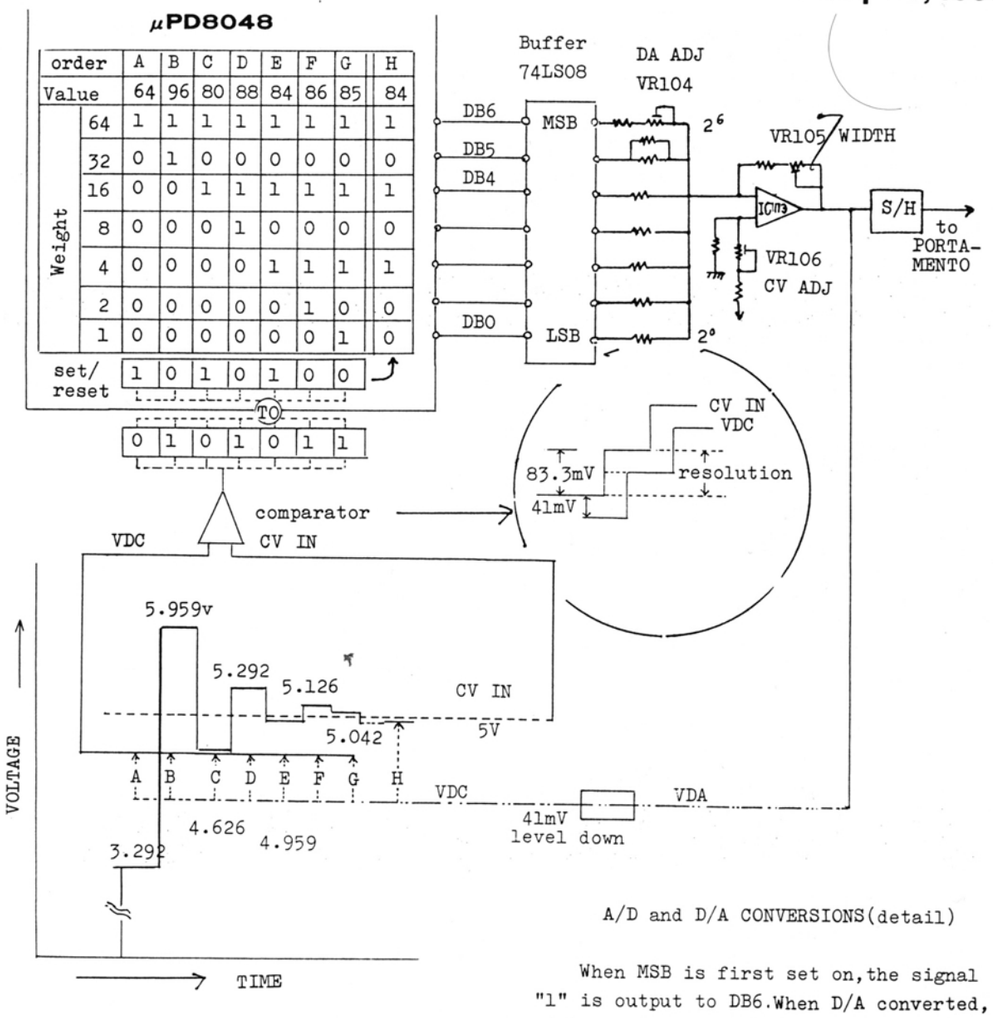
7. METRONOME DRIVE

In LOAD mode, two pulses concurrent with TEMPO are being output (in period 480 times the CLOCK pulse, in pulse width 14μs and 380μs for alternate output). METRONOME amp is driven by both pulses but since the shorter pulses of 14μs are filtered out by the integration circuit before arriving at LED, the longer pulse of 380μs only is used for lighting the TEMPO LED.





Note:
The digital data in this manual are expressed in Decimals.



A/D and D/A CONVERSIONS(detail)

DETAILED CIRCUIT DESCRIPTION

Since in the CSQ-600, the key voltage which are analog quantam are first converted to digital for storing in RAM and again afterward are converted to analog for CV OUT. These A/D and D/A conversions are just as important as the heart is to man. It might be said that without understanding of these conversion principles and pertinent analog vs digital data relationship, all adjustment services which are related to key voltage circuits become difficult to perform correctly. With this in mind our description will proceed along with the line as numbered in the figure above.

1. Storage capacity of the RAM in the CSQ-600 is 5 volts in terms of analog quantity. It accepts KCV within the range of 0V to 5V or 61 notes.

2. As described on later section 5, CSQ-600 is so designed that it can output -2V KCV from 0V KCV input. Therefore, the smallest CV to be processed in the CSQ-600 circuitry is -2V and the digital data are made to 00 for -2V, 24 for 0V.

3. For this reason, storing data for KCV IN lower than 0V into RAM is unnecessary. Besides, 6 bits (2^6 = 64) are enough in handling voltages 0 to 5V; the number of pitches are 61 if taken in the ratio of 1V/oct. But 7 digits would be required for covering 61 notes if started from 0V = 24.
To make 0V = 00(in decimal), numbers 24 are being subtracted after A/D conversion. Digit "1" in the data corresponds to analog voltage 83.3mV or 84mV - a potential difference between adjacent keys on the keyboard.

4. Reproduction of CV in Memory --- 1
- LOAD or PLAY (with KCV ADD "off") -
In this case, when D/A conversion is done after addition of 24, which is the same as subtracted before storing, to the data from RAM, the same original analog voltage can be reproduced after D/A conversion.

5. Reproduction of CV in Memory ----- 2
- Transpose under PLAY mode, with KCV ADD "on" -

CSQ-600 has the function to have the notes in play mode transposed up or down by adding an external key voltage to the CV from memory: with a 2 volts key voltage added original notes are reproduced in the same pitch as they were; and 0V key added, the notes are downed by 2 octaves.
The key that delivers 2V KCV is designated as a reference key in this book.
For instance, when 0V is stored in cells, depressing a 0V key(the lowest key to be accommodated) will cause the CSQ-600 to output -2V. To furnish this the following must be ture:

0V digital data stored in RAM (CVD2 = 00)
+ 0V KCV digital data (CVD3 = 24) = 00

To satisfy the above,

" CVD2 + CVD3 - 24 = output data"

When MSB is first set on, the signal "1" is output to DB6. When D/A converted, the analog voltage (VDA) here must be 3.333V which, after shifted down by 41mV, becomes 3.292V (VDC). This time VDC goes to noninverting input of the comparator and is compared with CV IN. In the case shown in figure above, this CV is 5V, so CV IN > VDC bringing the comparator's output to L, to have DB6 remainded as has been set to "1". Next, DB5 is set to "1". This time the digital data is the sum of DB6 and DB5, and the comparison becomes CV IN < VDC, to output H and to "reset" signal of TO and to have DB5 return to "0". This kind of comparison is repeated 7 times down to DB0 (LSB). The sum of the digital data of the bits remained "unreset", then, is made to be the data of this CV IN, with which the CV IN is stored in the external RAM.
Although CV IN is in fact an analog voltage, it steps up or down like a stircase wave as the note changes. Therefore, if VDC is shifted down by an amount equal to about one-half of the voltage difference between adjacent keys (KCV resolution), a voltage fluctuation within the resolution of the comparator does not bring effect on the digital data, as shown in the circle in the figure avobe.

RELATIONSHIP BETWEEN CV ADJ (VR106) and CV DATA

In LOAD mode and with the converter that is correctly adjusted, suppose that we turn VR106 (CV ADJ) slowly clockwise while holding 1V key depressed on the keyboard. Then you can observe VDA (i. e. CV OUT) increases gradually, and likewise VDC (VDA - 41.7mV) ascends along the dotted area as shown in Fig. 3.
That is to say, although the digital data is unchanged, the voltage for that data is increased.
But, still kept on turning VR106 to have VDC overcome 1V line for the digital data 36 as shown in Fig. 4, it causes the output of the comparator to be turned to "H" and the digital data re-written to 35.

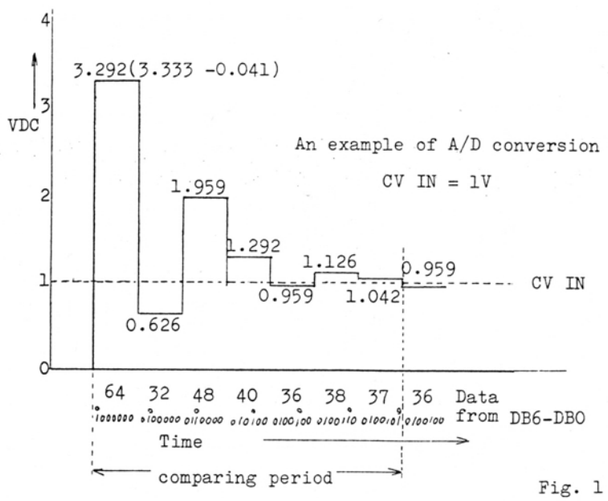


Fig. 1

Figure 5 shows that state as being adjusted by turning VR106 clockwise to have CV OUT again to 1.000V.

Still turning VR106 further will repeat the same as above and to rewrite to 34.
But, when turned counterclockwise, the data will be rewritten to a larger number each time.

When watching this on a digital voltmeter connected for observation, the display will be as illustrated in Fig. 2.

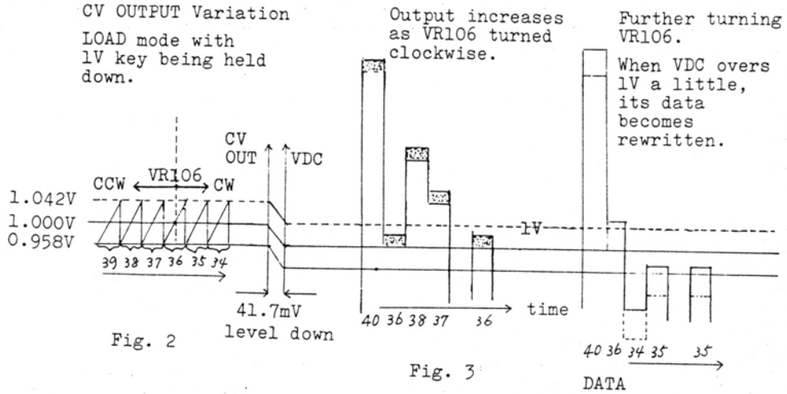


Fig. 2

Fig. 3

Fig. 4

Now, suppose that we have turned VR106 a little too far to have the digital data 35 for CV IN of 1V (as in Fig.5). It is all right and causes no problem as long as we have KCV ADD turned off, because under these circumstances, any shortage or excess of voltage could be compensated for by biasing through this CV ADJ potentiometer.
But, once we have turned KCV ADD on, the whole matter would become different, to be explained in the next paragraph.

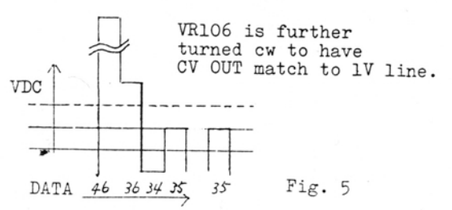


Fig. 5

WHEN DATA IS INCORRECT, ERROR WILL BE PRODUCED on CV OUT With KCV ADD "ON"

Taking for instance the case of each having CV IN 1V converted into digital 35 (B and C, table right) in place of 36, we will explain as follows:

NOTE: Figures in top row refer to those in illustration at left on opposite page.

	MODE	2 CVD1	3 substraction	CVD2	4, 5' addition	6 D/A INPUT	7 CV OUT
A	LOAD (normal)	36	24	12	24	36	1V
B	KCV ADD "off"	35	24	11	24	35	1V
C	KCV ADD "on"	35	24	11	*(CVD-24) 47-24=23	34	0.9167V

* This is when the 2V key is depressed so as to have the same pitch on CV OUT with CV IN in memory

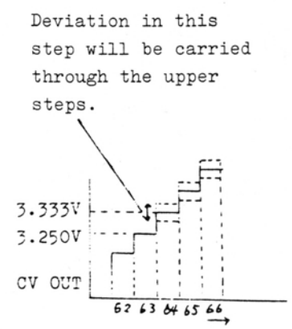
Case B is when VR106 is adjusted to reproduce CV OUT of 1V even if in earlier stage the digital data lacks by 1.
In this case, since the numbers in previous subtraction, and subsequent addition are both the same (24), the analog amount at the output receives no effect to differ after A-D-A conversions.
In C, however, despite the fact that the KCV (being pressed) is converted to digital data number short of 1, it is added to RAM-stored-data after subtracting 24. As a result there is a double shortage, bringing after all the shortage by 2 before D/A conversion prior to CV OUT. Through this D/A once again, 1 out of these 2 can be compensated for by VR106, but there is still remained of 1, which brings lack in pitch of a semitone ("1" in digital data) on tone reproduction.
Thus, a maladjustment of VR106 produces a deviation on reproduction when played with KCV ADD "on". Or, it can be said conversely that, through finding such deviation on analog voltage, it is possible to check digital data errors.

WIDTH ADJUSTMENT with VR107

This potentiometer VR107 is for use to correct the gain of IC112 so as to have D/A in proper relation of 1V/oct, that is, when the data changes by 1, CV OUT changes by 83.3mV.
When VR107 is required for readjustment, it may also be necessary to readjust VR106, since turning either VR results in interaction between the adjustments. Therefore, both VRs need to be adjusted in turn.
Also care must be exercised to avoid an excessive turn of the VRs which will bring difficulties in performing these adjustments.

D/A ADJUSTMENT with VR104

This potnetiometer is for the gain adjustment of the D/A converter, and it is in particular for DB6. This DB6 is for the data weighing the most significant bit, so its adjustment is the most critical one and warrants the careful attention. Sources of fluctuation and deviation such as those coming from the preceding stage of IC118, IC119, on impedance or on output voltage, and resistance variation in resistor, etc. are to be compensated for by this VR104.
Since the digital data that makes DB6 active is in number over 64 or 3.333V in CV, fluctuation brought through DB6 data will effect all CV of higher voltages as shwón in the figure. In practice, it will be best to adjust VR104 as follows:
set the LOAD mode and complete both CV ADJ and WIDTH ADJ, then, holding down the key for 4V. Set VR104 so that CV OUT equals 4.000V.



RHYTHM SYNC

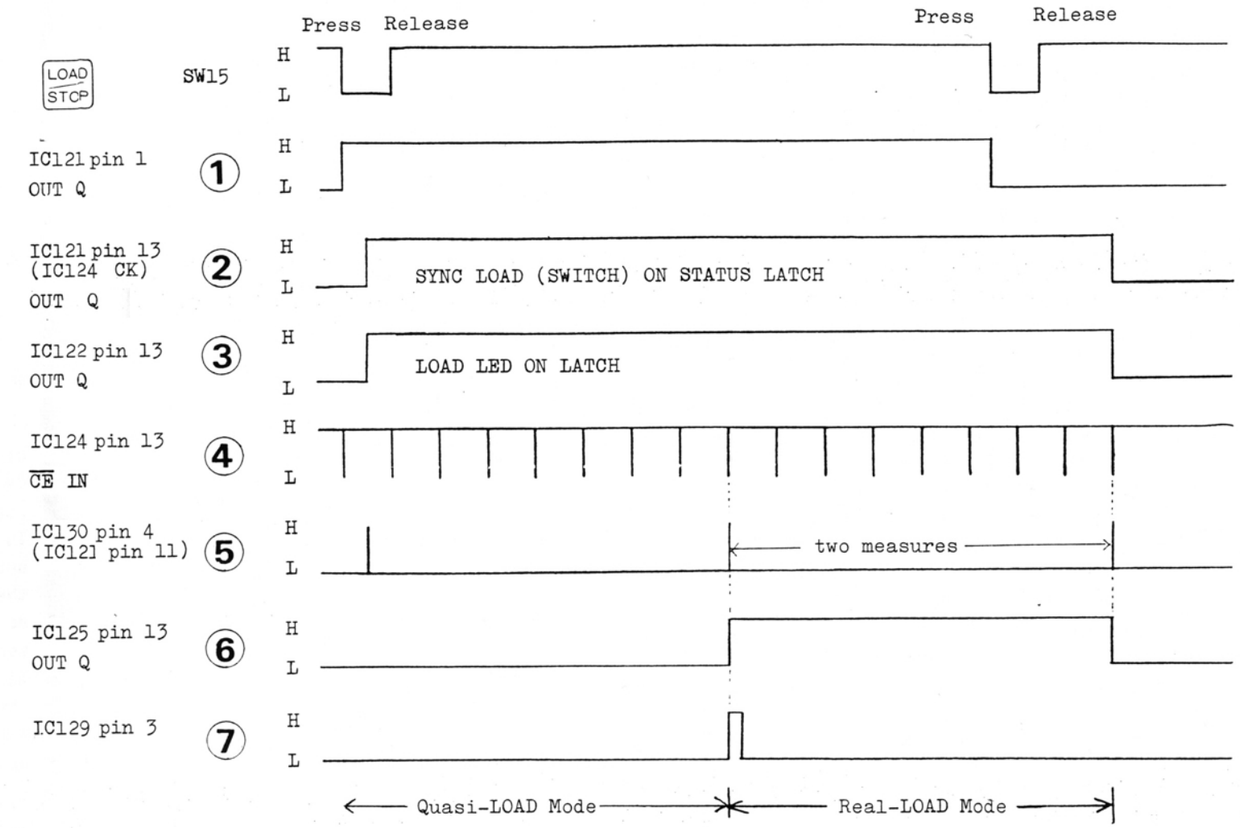
- CLOCK PULSE -

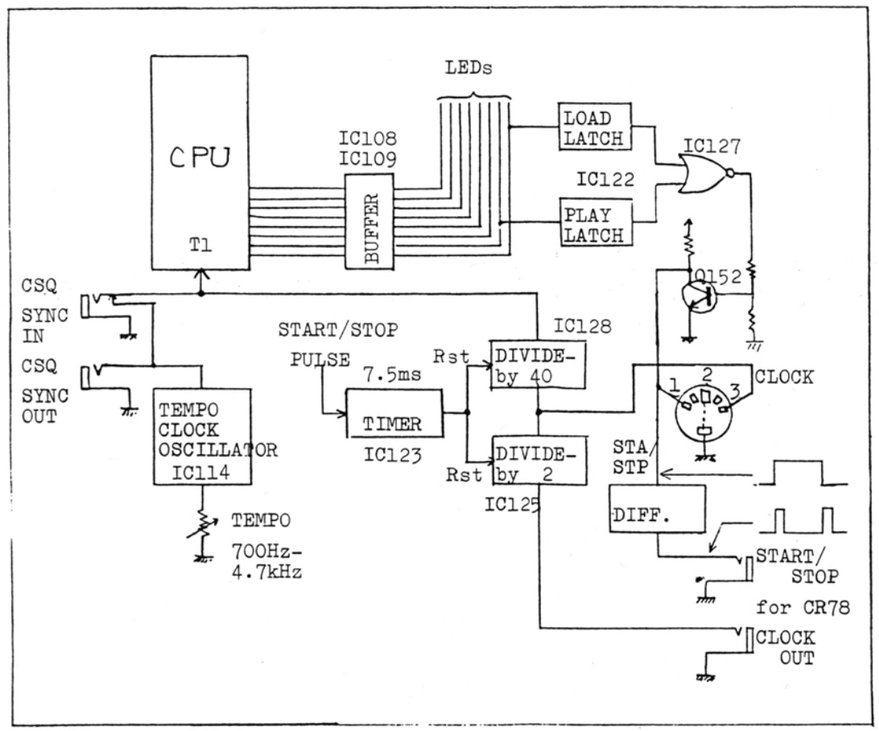
In CSQ-600, tempo (duration of a beat) for BEAT ♩ is designed equal to that of 120 clocks of the tempo oscillator. CPU 8048 divides tempo oscillator's output by 8 in frequency - 960/8 = 120.
The output of the oscillator is also divided by 40 in IC128 to create tempo of 24 clocks to be used for CLOCK OUT through DIN socket, 24 clocks per ♩. This output is further divided by 2 in IC125 to provide tempo for BEAT ♪ consisting of 12 clocks, TEMPO CLOCK for CR78.

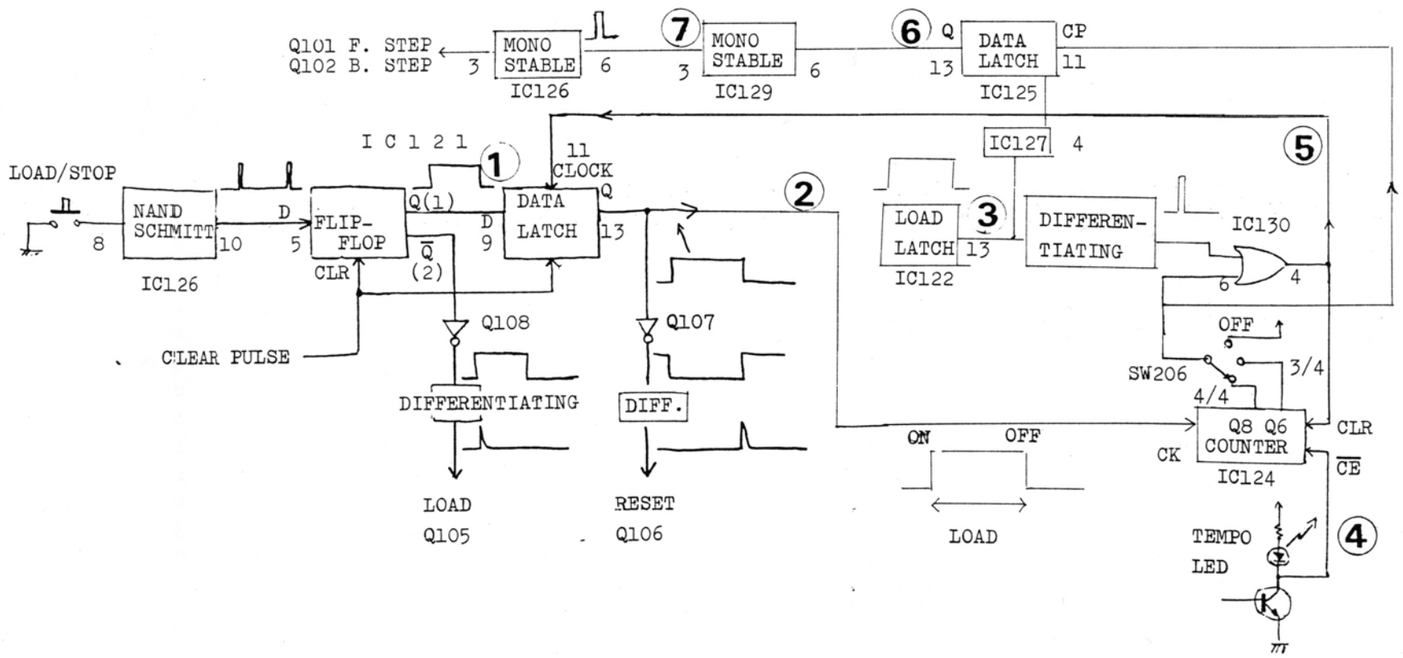
- START & STOP PULSES -

Rhythm unit, when connects and works with CSQ-600, starts and stops in synchronous with the switchings of LOAD/PLAY and STOP/RESET on the sequencer.
Either ½IC122 senses LED drive signal (LOAD or PLAY) and latches it which is sent to NOR gate IC127.
Upon receiving one of latched signals, IC127 output switches to low and stays low during PLAY or LOAD mode. For starting and stopping CR78 rhythm the high output (inverted) from Q152 is differentiated at its rising and falling edges; resulting pulses are then ORed and inverted respectively to become distinct positive going pulses. CR78 will run and stop only when positive going pulse is applied to its START/STOP jack.

* Output from pin 3 of Timer IC123 signals Clock dividers to keep clock pulses low for 5-10ms after PLAY or LOAD is pressed.

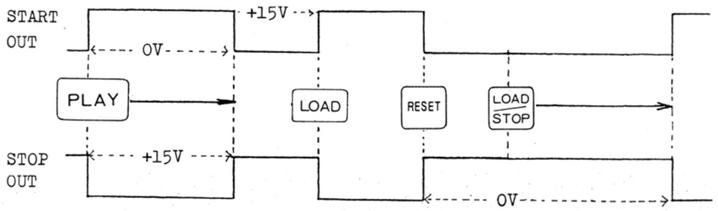






TEST ON EXT CONTROL OUTS

Connect an oscilloscope to EXT CONTROL OUT jacks.
Load notes over few measures.
Set: PLAY mode to ONE TIME;
METRONOME BEAT to ♩;
SYNC LOAD RHYTHM to 4/4.



- SYNC LOAD

Refer to the diagram and the waveforms on the facing page

Since this function seems very intricate to understand, first read through, skipping the sentences headed with *, for clarification.
Assuming that LOAD/STOP is first pressed after power is on with RHYTHM (SW206) set in 4/4.

1. NAND SCHMITT trigger, IC126 developes positive going pulse on pin 10.

   * This circuit eliminates LOAD/STOP switch contact chatterings.

2. Unpon receiving this pulse, T-type flipflop ½IC121 Q (pin 1) switches to high and $\overline{Q}$ (pin 2) to low which, after inverted in Q108 and differentiated, conducts Q105 with its rising edge, duplicating the LOAD (SW13) "on".
   Although LOAD LED goes on and stays on, the status may be called Quasi-LOAD mode since inhibit signal is fed to $\overline{INT}$ terminal on CPU from IC131 pin 9 through IC130 pins 1-3. Any signals at CV and GATE IN terminals are ignored by the CPU.

   * Three-input NOR gate IC131 pin 9 keeps the high inhibit signal as long as three inputs are low, retaing it for two measures - to the leading edge of ⑥ , after LOAD/STOP button is pressed.
   * Quasi-LOAD mode period allows the performer to set BEAT and TEMPO for the rhythm he times to before CSQ-600 proceeds to real-LOAD mode. Missing gate signals at the begining of real-LOAD mode caused by inadvertent key play will result in "RESET" loadings.

3. The rest half of IC121 is used for latching LOAD/STOP switching data. High on D(pin 9) is latched with a signal ⑤ coming at pin 11 and Q (pin 13) goes high ②.

   * The latched data remains unchanged until the next latch signal comes -once per two measures, even if LOAD/STOP is pressed again and Q(pin 1) turned to low.
   * Two flip flops in IC121 are reset with clear pulse applied to CLR (pins 4. 10) - at power turning on and at the end of LOAD or PLAY mode, and are inactive when SW206 is set in LOAD OFF (pulled up to +B).

4. Decade counter IC124, when H ② is placed on CK pin, increments the count at the falling edges of LED drive signal entering $\overline{CE}$ pin at the BEAT rate. The positive going pulse is present on Q8 pin when counting reaches 8. The very first pulse on ④ is canceled because of the first counter clear pulse ⑤ is fed through IC130 pin ④
   Q8 output is directed to:

A) IC125 CP(pin 11) to latch the data from IC127 pin 4 (PLAY or LOAD latch).
   Positive-going edge of latched output ⑥ then triggers monostable IC129 which in trun outputs a pulse on pin 3 and sends it to IC126 pin 6. ⑥ also connects to 3-input NOR gate IC131 that turns pin 9 from high to low removing inhibit signal from $\overline{INT}$. CSQ-600 is now set in complete LOAD mode. Consequently, if signal is not fed through GATE IN, the signal on IC126 pin 6 is NANDed with that on pin 5, generating positive pulse from pin 3 to fire Q101(F.STEP) and Q102(B.STEP).
   Short-circuiting of both F.STEP and B.STEP signals CPU to reconize it as a RESET load.

B) CLR(pin 5) of counter itself through pin 4 of IC130 to reset. Counter reads LED drive pulses for the next two measures.

   * Two measures is composed of eight ④ pulses when RHYTHM is set in 4/4, and is composed of six when set in 3/4.
   * Q111 removes H on IC126 pin 5 when GATE IN is present on the input terminal(8).

RESET

Pressing LOAD/STOP button in progression of LOAD mode inverts the outputs on pins 1 and 2 of IC121, but latched high signal ②is maintained until ⑤ is applied to pin 11 at the end of the two measures. When ⑤ is received, L on pin 9 is latched and transferred over pin pin 13.
Inverted and differentiated pulse from negative going edge of ② turns on Q106 parallel with RESET switch contacts.
With H voltage removed on CK terminal, counter IC124 becomes inactive and seases increment.

PARTS LIST

PANEL

072H075	Panel H75	(top)
066H021	Panel H21 set of R and L	(sides)
061H114	Chassis H114	
068-020	Bushing no.20	top
111-021	Rubber foot G-5	rear
111-023	Rubber foot G-7	front

SWITCH. KNOB

001-215	SDG5P001-1 power	100V
001-216	SDG5P001-2 power	117V
001-217	SDG5P502 power	220/240V
001-268	SLE-622-18PS	lever
001-201	SLE-623-18PS	lever
001-182	SSB-02242-12PN	slide
001-183	SSB-02335-12PN	slide
001-276	SCK41167	key
001-275	SCK41168	key
016-004	Knob no.4	PORTAMENTO
016-103	Knob no.103	TEMPO
016-009	Button no.9 black power switch	

SOCKET

19429004	DIN connector 180256	
009-012	Jack SG7622 no.8	mono
068-018	Bushing no.18	red
068-005	Bushing no.5	black
121-005	Washer no.5	
012-043	ICC030-040-350T	IC

TRANSFORMER. COIL

022H024J	PT-H24J	100V
022H024C-A	PT-H24C-A	117V
022H024D	PT-H24D	220/240V
022-136	Coil 24M-067-033	47μH

FUSE. FUSE HOLDER

008-040	MGP 0.500 CSA	prim. 117V
008-061	SEMKO T315mA	prim. 220/240V
008-056	SEMKO T100mA	sec.
008-066	SEMKO T1A	sec.
012-003	Fuse clip TF758	

CIRCUIT BOARD ASSY

149H114B	OPH114B (marking 052H229B)
149H115B	OPH115B (marking 052H258B)
146H039A	PSH39A (marking 052H172A) 100V
146H040A	PSH40A (marking 052H172A) 117V
146H041A	PSH41A (052H172A) 220/240V

SEMICONDUCTOR

LSI

1517910177	μPD8048C-077 or	8-bit micro-
15179113	μPD8048C-256	computer
15179305	μPD444C	RAM

IC

020-203	SN74LS00N
15169304	SN74LS04N
020-204	SN74LS273N
15169310	SN74LS42N
020-120	SN74LS08N
020-051	TC4001BP
020-040	TC4011BP
020-041	TC4013BP
020-075	TC4049BP
15159122T0	TC4017BP
020-093	TC4025BP
15159123T0	TC4071BP
15159124T0	TC4093BP
15159302T0	TC4518BP
020-199	μPC311C
020-100	TL082CP
020-200	TL080CP
020-097	μPC4558C
020-205	μPC14305 +5V regulator
020-206	μPC78L15 +15V regulator
15219109H0	HA17555PS or NE555P

CMOS IC COMPATIBILITY

Most equivalents might be replacement for the existing one and IC of different manufacturers may be found in different CSQ-600s. However, in some cases, corresponding components' value changes may be involved upon replacing for the best performance, e.g. IC118, IC119 - see circuit diagram.

Diode

018-014	1S2473	
15019624	1SZ52	zener
018-089	1B4B41	rectifier stack
15019243	1B4B1	rectifier stack

LED

019-028	TLR-124	red
019-029	TLG-124	green
019-009	LR0601R	red

Transistor

017-016	2SC1815-GR	
017-024	2SA733-P	
017-034	2SA682-Y	
15119601	2SB605-L	
15139106 (017-103)	2SK117-GR	FET

POTENTIOMETER

029-577	EVALOPC15A26	slide	PORTAMENTO
030-951	EVHLWAD25B15(L)		CALIBRATION
028-766	VM10RK20B16(L)		TEMPO
030-465	SR19R 10KB		trimmer
030-471	SR19R 100KB		trimmer
030-644	RJ-6P 500B		trimmer
030-645	RJ-6P 1KB		trimmer
030-646	RJ-6P 50KB		trimmer

(L): Right angle terminals

RESISTOR

044-927	CRA¼BY	11K	0.1%	50PPM
044-932	CRA¼BY	31K	0.1%	50PPM
044-929	CRA¼BY	125K	0.1%	50PPM
044-930	CRA¼BY	250K	0.1%	50PPM
044-972	CRA¼DY	500K	0.5%	50PPM
044-973	CRA¼DY	1M	0.5%	50PPM
044-838	CRB¼FX	10K	1%	
044-846	CRB¼FX	100K	1%	
044-860	CRA¼FX	1M	1%	

CAPACITOR

037-035	Ceramic $0.1\mu F^{+80}_{-20}\%$ 12V disc

TERMINAL. WIRINGS

010-193	Terminal	5046-03A
010-197	Terminal	5046-07A
010-200	Terminal	5046-10A
042-032	TT 501-D01	power cord
053H103	Wiring assy	A
053H104	Wiring assy	B
053H105	Wiring assy	C
053H106	Wiring assy	D
042-039	Check point	59BS8806

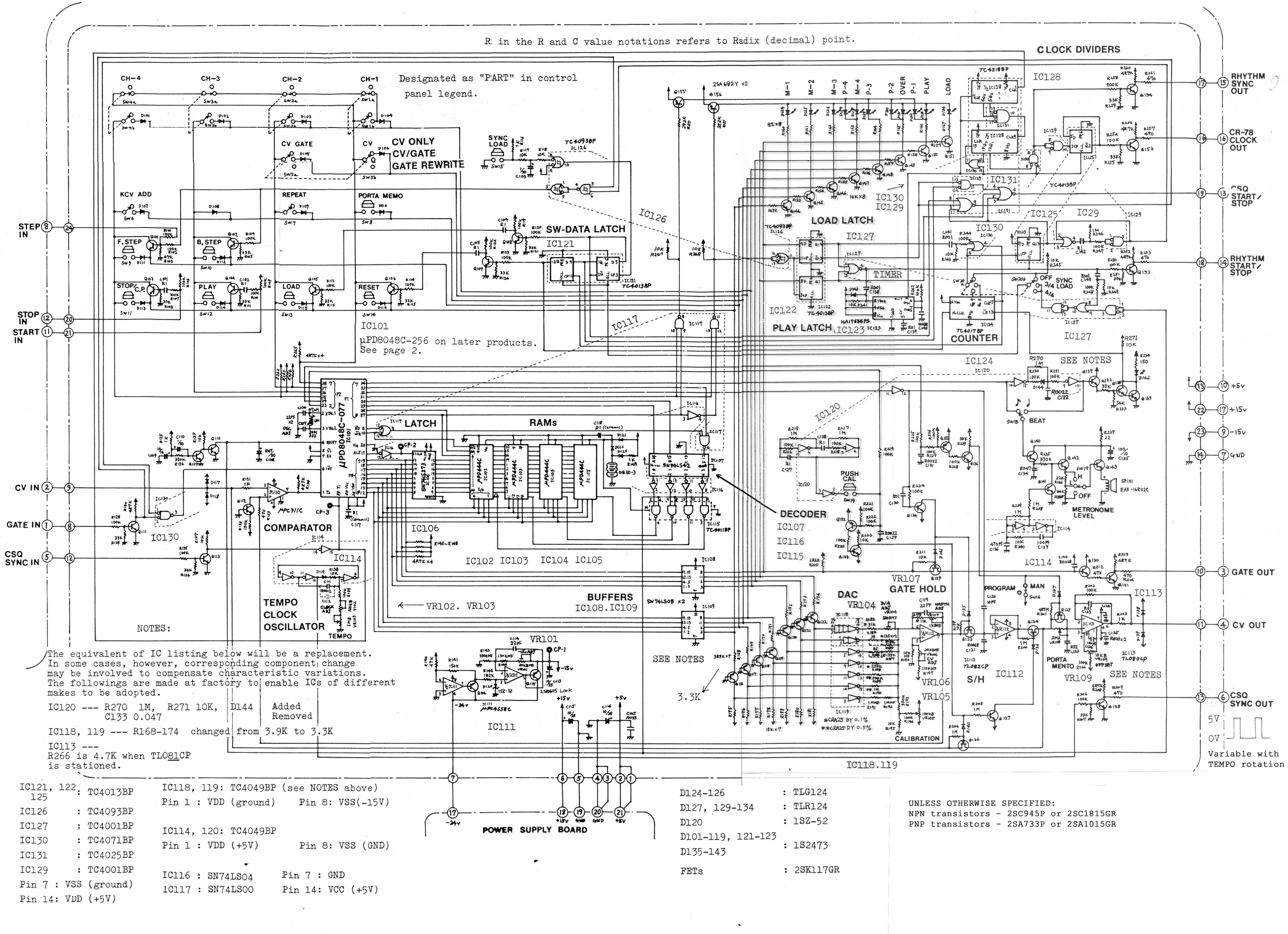
OTHERS

048H017	Heat sink	H17
120-001	Long nut no.1	3 x 10mm
120-003	Long nut no.3 (stand off or spacer)	3 x 18mm
064H076	Holder H76	
064H055A	Holder H55A	
064H083	Holder H83	
064H092	Holder H92	
065-190	Dust cover	no.190
065-065	Dust cover	no.65
065-005	Dust cover	no.5

NEW NUMBERING IS APPLIED TO SOME NEW COMPONENTS

CD-503 Battery

R in the R and C value notations refers to Radix (decimal) point.



The equivalent of IC listing below will be a replacement. In some cases, however, corresponding component change may be involved to compensate characteristic variations. The followings are made at factory to enable ICs of different makes to be adopted.

IC120 --- R270 1M, R271 10K, D144 Added
C133 0.047 Removed

IC118, 119 --- R168-174 changed from 3.9K to 3.3K

IC113 ---
R266 is 4.7K when TL081CP is stationed.

IC121, 122, 125 : TC4013BP
IC126 : TC4093BP
IC127 : TC4001BP
IC130 : TC4071BP
IC131 : TC4025BP
IC129 : TC4001BP
Pin 7 : VSS (ground)
Pin 14: VDD (+5V)

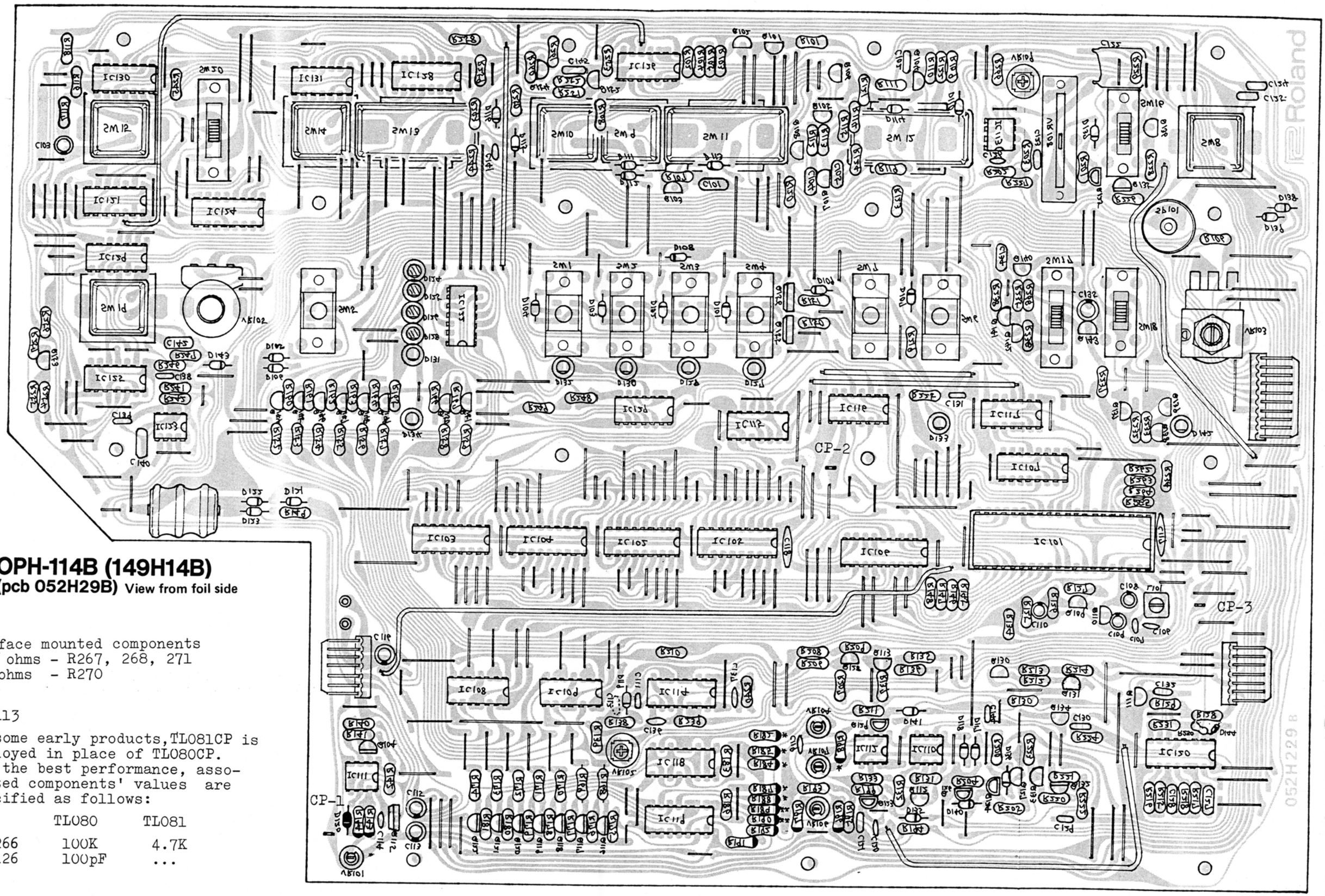
IC118, 119: TC4049BP (see NOTES above)
Pin 1 : VDD (ground) Pin 8: VSS(-15V)

IC114, 120: TC4049BP
Pin 1 : VDD (+5V) Pin 8: VSS (GND)

IC116 : SN74LS04 Pin 7 : GND
IC117 : SN74LS00 Pin 14: VCC (+5V)

D124-126 : TLG124
D127, 129-134 : TLR124
D120 : 1SZ-52
D101-119, 121-123
D135-143 : 1S2473
FETs : 2SK117GR

UNLESS OTHERWISE SPECIFIED:
NPN transistors - 2SC945P or 2SC1815GR
PNP transistors - 2SA733P or 2SA1015GR



OPH-114B (149H14B)
(pcb 052H29B) View from foil side

Surface mounted components
10k ohms - R267, 268, 271
1M ohms - R270

IC 113

In some early products, TL081CP is employed in place of TL080CP. For the best performance, associated components' values are specified as follows:

	TL080	TL081
R266	100K	4.7K
C126	100pF	...

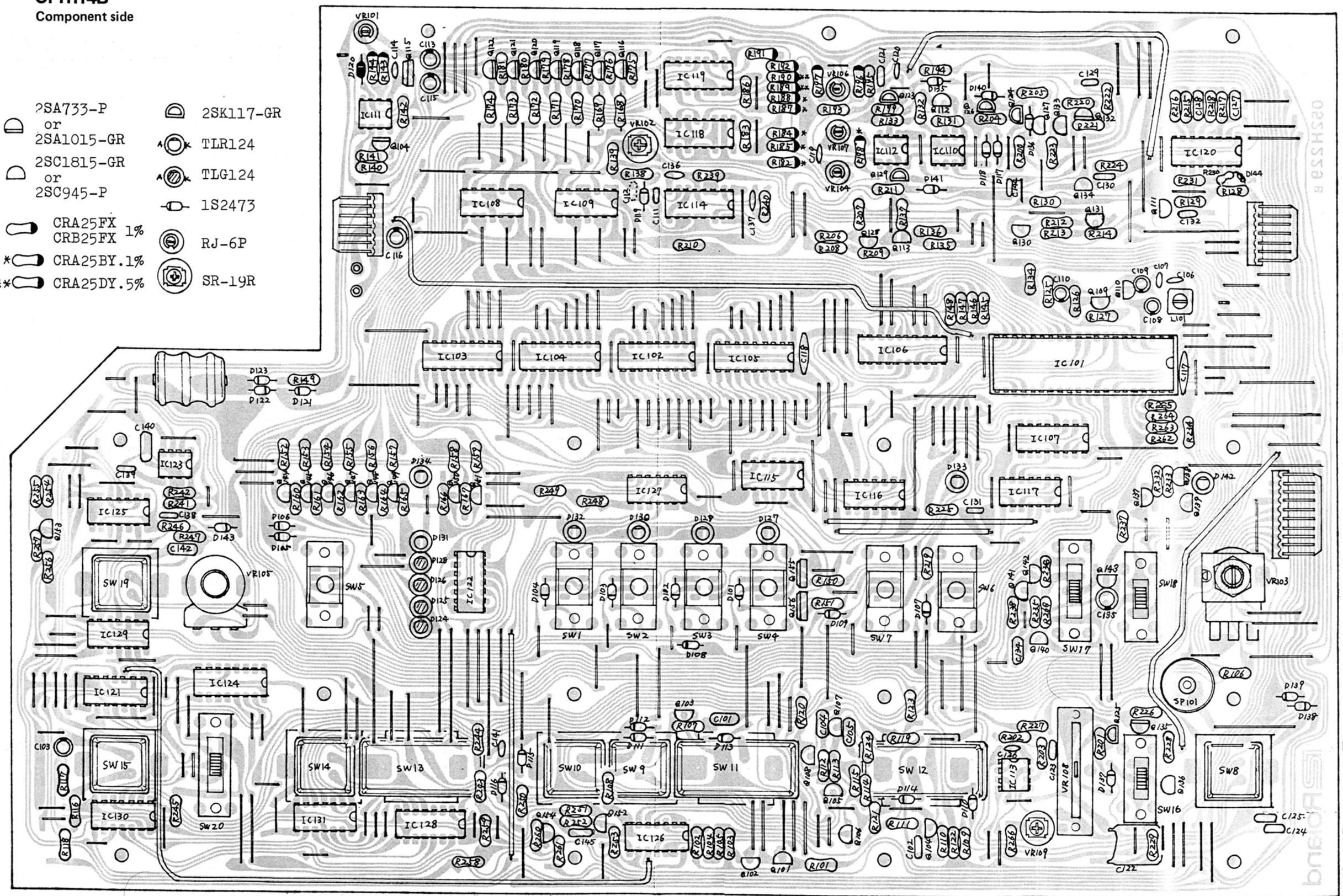
The printed wiring layouts of this page and back side are registered to help simulate turning the pc board inside out without removing the front panel off.

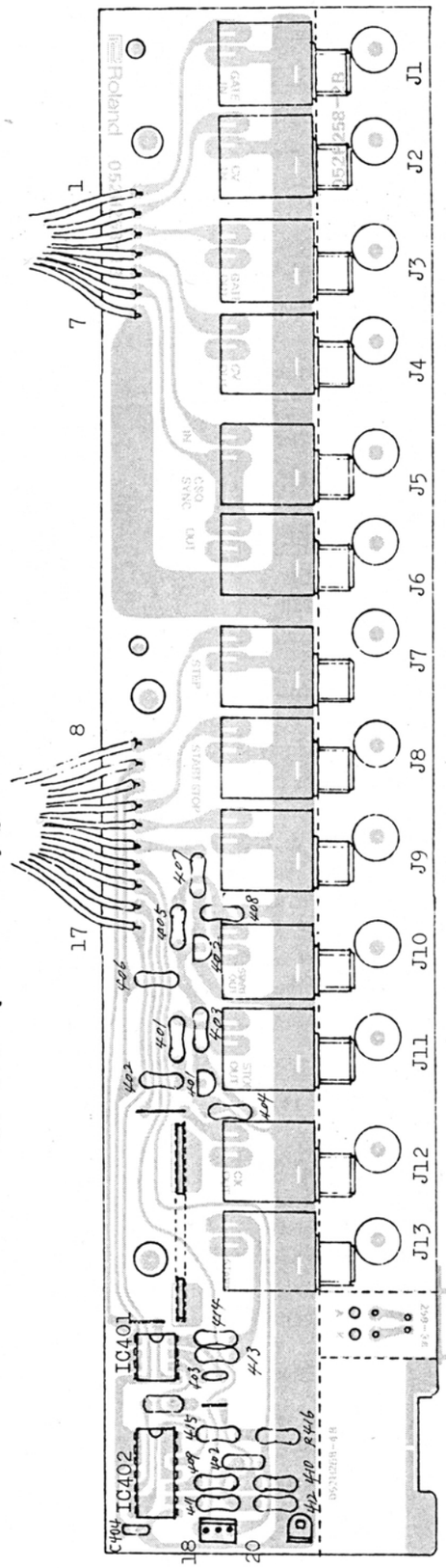
REMARK: I rotated the image. This is the position which the pcb has in an opened CSQ-600. Also the partnumbers are much more readable. FA

OPH114B

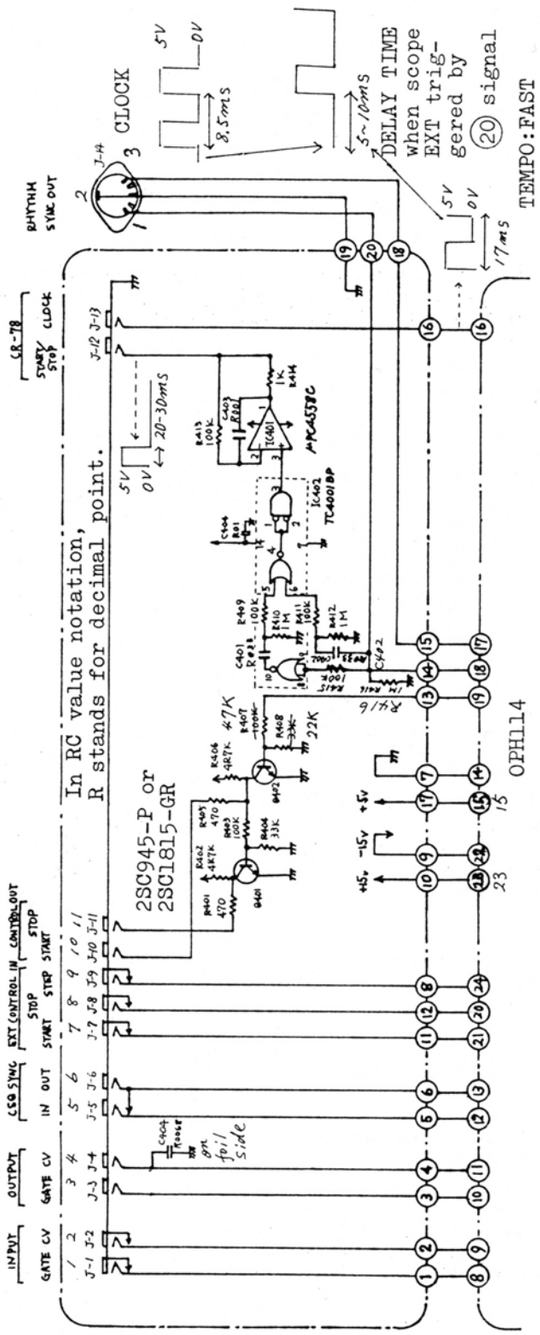
Component side

2SA733-P or 2SA1015-GR
2SC1815-GR or 2SC945-P
CRA25FX CRB25FX 1%
*CRA25BY.1%
**CRA25DY.5%
2SK117-GR
TLR124
TLG124
1S2473
RJ-6P
SR-19R

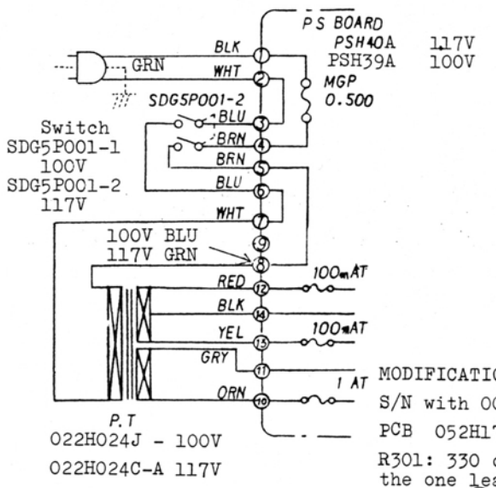




OP-115B (149H115B) (pcb 052H258B) View from foil side

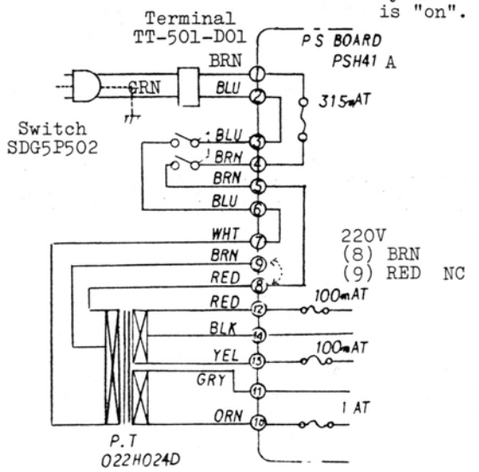


100/117V



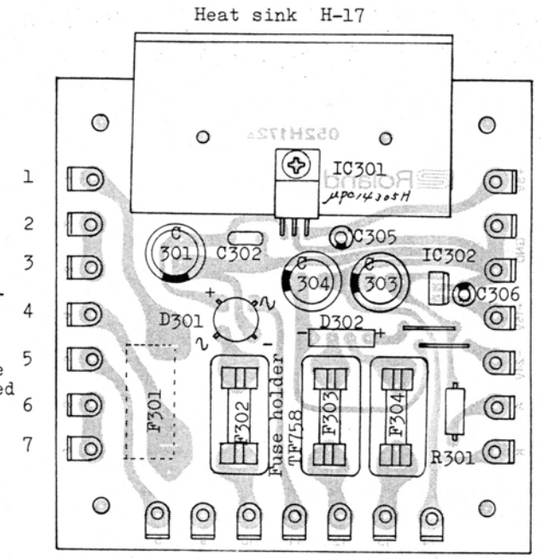
MODIFICATION
S/N with 001050
PCB 052H172C
R301: 330 ohms with the one lead connected to ㉑ . This prevents D303 from being lit when CSQ600 is "off"while synthesizer connected is "on".

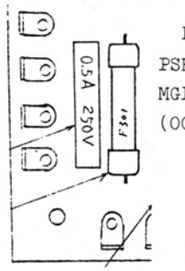
220/240V



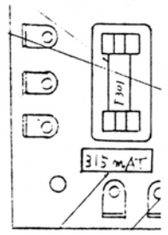
POWER SUPPLY BOARD
PSH39A (146H039A) 100V
PSH40A (146H040A) 117V
PSH41A (146H041A) 220/240V
(Etch mask 052H172A)

When replacing, use C version.

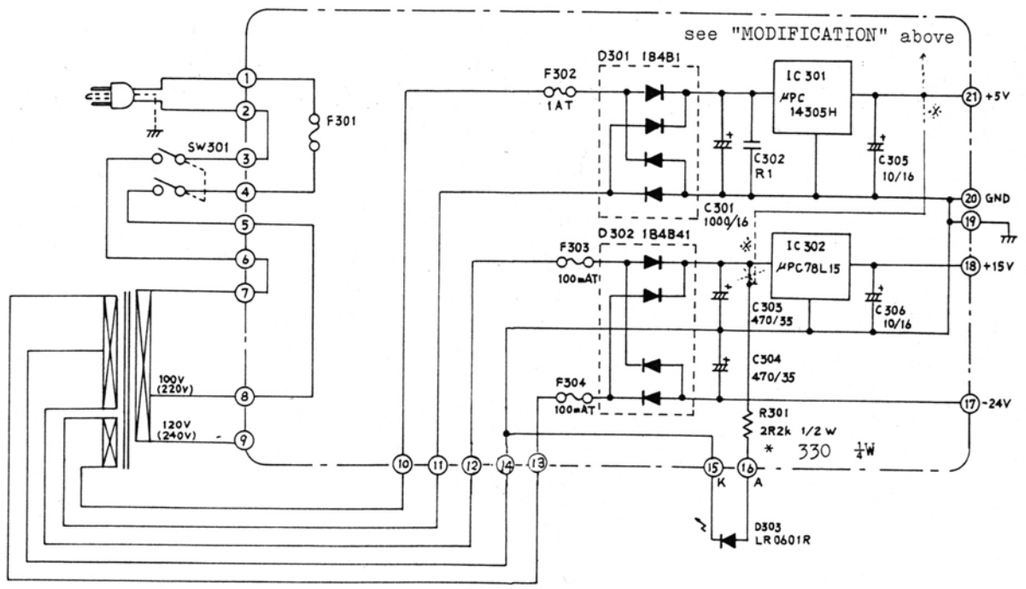




F301:
PSH39/40
MGP 0.500 CSA
(008-040)



F301:
PSH41
SEMKO
T315mA
(008-061)



ADJUSTMENTS

The adjustment is composed of two parts: Section I and Section II. It is recommended that the adjustment which is necessitated after the replacement of failing component or others are, as a rule, to be conducted as described in Section I.

Difinitions
In this adjustment, the following terms have the following meanings.

DVM --- Digital voltmeter Scope --- Oscilloscope
LOAD, PLAY, etc. ---------- Key on the CSQ-600 control panel

2V key, 3V key, etc. ------- A key on the synthesizer keyboard connected
TEMPO, CAL, FAST, etc. ----- Control,Switch,Jack,Legend on the CSQ-600
CP1, CP2, etc. ------------- Check point on the PCB

NOTE: Allow at least ten minutes for warm up period before adjusting.
CAUTION: Do not trun adjusting potentiometers excessively.

SECTION I

Adjustment is usually necessary only after replacing parts:

CALIBRATION PROCEDURES

After replacing		Connect-, to	Adjust, or Check	for (remark)
IC101 (μPD8048) L101 (47μH)	1.	Frequency counter, CP2	L101	365kHz±10kHz (8048 Clock frequency)
IC114 (TC4049))	2.	Frequency counter, CP3	VR102 Clock Adj.	(Tempo clock frequency) 4.7kHz±5% with TEMPO at FAST
Check that frequency is 0.7kHz $^{+5\%}_{-10\%}$ with TEMPO set at SLOW. If deviates from this range, readjust VR102 for within the range of 4.7kHz±5% with TEMPO set at FAST. Or, tailor C112.				
IC113 (TL080CP)	3.	No connection, CV IN jack / DVM, CV OUT	VR109 Offset	(Press RESET) 0±0.5mV
IC111 (μPC4558) D120 (1SZ52)	4.	DVM, CP1	VR101 -15V Adj.	-15V±2mV
NOTE: Since any variation in the DC supplies will have the most pronounced effect on the D-A converter, check CV OUT for error through the next steps (5).				
IC118,IC119 (TC4049) IC112 (TL082CP)	5.	CV IN, Synthe CV OUT / GATE IN, Synthe GATE OUT / DVM, CV OUT	VR106 CV Adj.	(D/A Adj.) CAUTION: Adjustment of the DA converter is very subtle. Always rotate Adj. pots by small degrees, excessive turn will bring great difficulty on the subsequent adjustments, requiring a waste of time.

Setting:
PORTAMENTO on the synthesizer ------ Off or TIME "0"
LOAD MODE ---- CV/GATE
MEMORY ------- PART-1 TEMPO ---------- Its midpoint
PLAY MODE ---- KCC ADD ON PORTAMENTO ------- TIME 0
REPEAT CALIBRATION ------ Its midpoint

- TO BE CONTINUED -

continued from the preceding table

5-1. Press RESET and LOAD.

5-2. Press 2V key, DVM should read 2.000±3mV.
When DVM reading is within ±3mV, adjust CALIBRATION pot for 2V CV OUT with PUSH CAL depressed. Proceed to 5-3 and 5-4.
If reading is outside ±3mV range, set CALIBRATION pot at its midway and adjust VR106 (CV Adj.) for 2.000± 3mV reading.

5-3. Verfication of KCV ADD Function
While pressing 2V key, push PLAY. DVM should read the same value.
a) If reading changes, it means that VR106 has been set at incorrect point. Proceed to Section II.
b) When the reading is steady, make sure that the DVM readings are within the ranges shown in the table below with respective key pressed:
RESET-LOAD-2V key-PLAY-2V key-3V key-4V key

Key being played	DVM reading (CV OUT)
2V	2.000±2mV
3V	3.000±2mV
4V	4.000±2mV

If any of the readings deviates from the limit, make adjustment under Section II, - 1-6.

5-4. Press RESET and LOAD.
While playing 4V key, push PLAY.The meter should read 6.000±3mV. If not, proceed to Section II,- 1-7.

SECTION II

1. ADJUSTING DIGITAL TO ANALOG CONVERTER

- Refer to NOTE at the end of this page -

Some procedures are the same as described in Section I. In the following steps, adjustment should be made with specified key being held down.
Connections and Settings - follow the instruction "5" in Section I.

1-1. Press RESET and LOAD.

1-2. While playing 2V key, adjust VR106 (CV Adj.) for 2.000V reading. Then, press PLAY.
a) If the reading stays still, proceed to step 1-5.
b) If changes, proceed to step 1-3(note the reading).

1-3. Press RESET , LOAD and 2V key.
While holding down the 2V key, adjust VR106 for the following "2V" according to the deviation noted at step 1-2, b.
As discussed earlier (RELATIONSHIP between CV ADJ and DATA), DVM reading will repeat the cycle of 2V±41mV as VR106 is being turned.
Ordinal numbers in the right colum of the table at top right show number of repetition.

DVM reading at step 1-2. b	Turn VR106 in this direction	Stop turning when DVM reads 2.000V of
2.083V	clockwise (CW)	1st
2.167V	CW	2nd
2.250V	CW	3rd
1.917V	counterCW (CCW)	1st
1.833V	CCW	2nd
1.750V	CCW	3rd

1-4. Press RESET, LOAD, 2V key and PLAY.(2V key held down) DVM must keep the same reading.

1-5. Press RESET and LOAD.

	Key to be pressed	Adjust	for reading	(remark)
a)	3V	VR107 (WIDTH)	3.000V	Repeat until exact readings are obtained
b)	2V	VR106 (CV ADJ)	2.000V	
c)	4V	VR104 (DA ADJ)	4.000V	Repeat until respective voltages are displayed on DVM
d)	2V	VR106	2.000V	
e)	3V	VR107	3.000V	

1-6. Press RESET, LOAD, 4V key (kept down) and PLAY. DVM should read 6.000±2mV . If a discrepancy is noted, it may be cured by the sacrifice of d and e adjustments of above 1-5 with their readings allowed to deviate within tolerance.

a) Return to steps d and e of 1-5. This time, adjust only VR107 for the readings which decrease deviation at 6.000V, e.g. if 6.000+3mV, set VR107 for 2.000 minus 1-2mV and 3.000V minus 1-2mV and again proceed to 6.000V adjustment. Readings within ±2mV of d and e may be considered as the tolerance.

2. CHECKING CV OUT

With DVM connected to CV OUT and LOAD pressed,check DVM readings for 1V/oct across keyboard.

NOTE: Most difficulties in getting correct voltages of WIDTH and CV result from wrong settings of adjustment trimmers; VR104,VR107 and/or 106 might have been set too far from their proper position.Reset them to the approximate positions illustrated in the figures below. Adjust again from appropriate step.

VIEW FROM PANEL SIDE