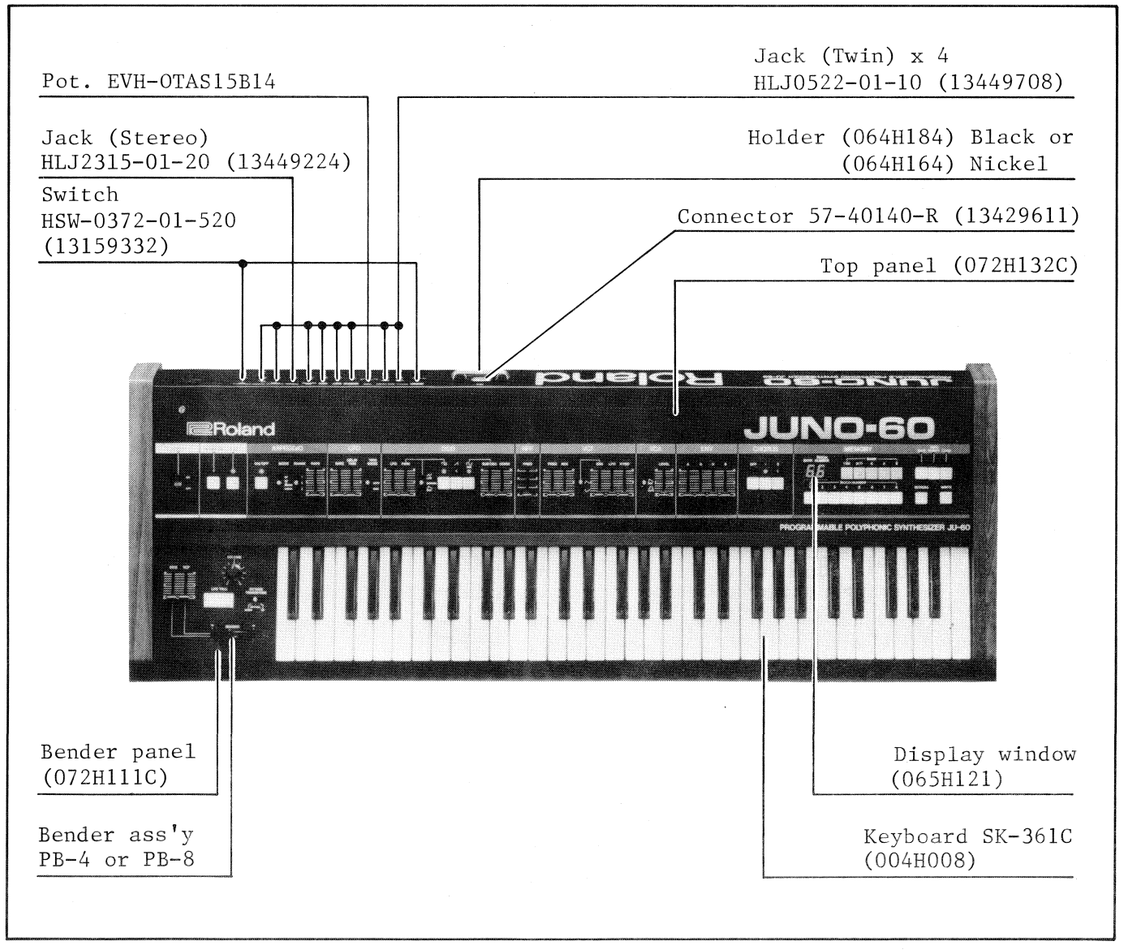
JUNO-60 SERVICE NOTES *First Edition*

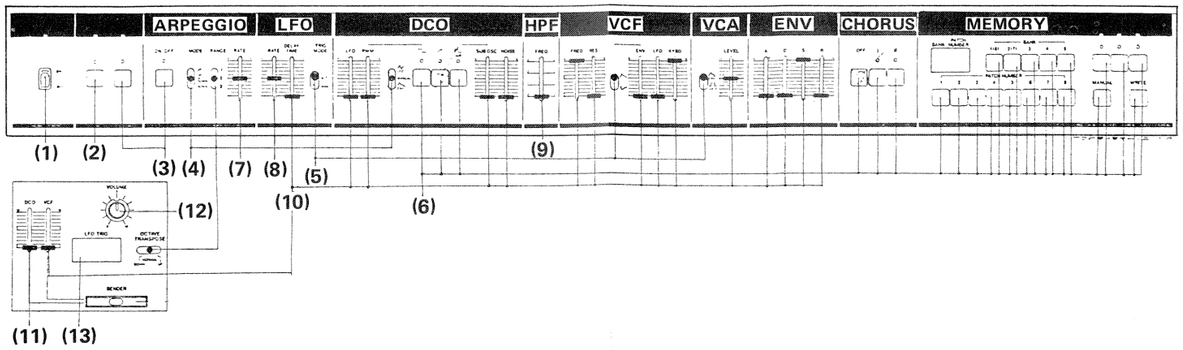
SPECIFICATIONS

Keyboard	61 keys, 5 octaves	
VCF	RESONANCE	(0 – Self Oscillation)
	KEY Follow	(0 – 100%)
ENV	ATTACK Time	(1ms – 3s)
	DECAY Time	(2ms – 12s)
	SUSTAIN Level	(0 – 100%)
	RELEASE Time	(2ms – 12s)
LFO	RATE	(0.3– 20Hz)
	DELAY TIME	(0 – 1.5s)
ARPEGGIO	RATE	(1.5– 50Hz)
MEMORY	PATCH NUMBER	(1 – 8)
	BANK	(1 – 7)

Rear Panel	Output Level (L: –30dBm/M: –15dBm/H: 0dBm)
	ARPEGGIO CLOCK Input (1 step/ pulse= +2.5V or more)
	TUNE (±50 Cents)
Dimensions	1060 x 378 x 113mm
(W x D x H)	41–3/4 x 14–7/8 x 4–7/16in.
Weight	12kg/26lbs. 7oz.
Power Consumption	30W

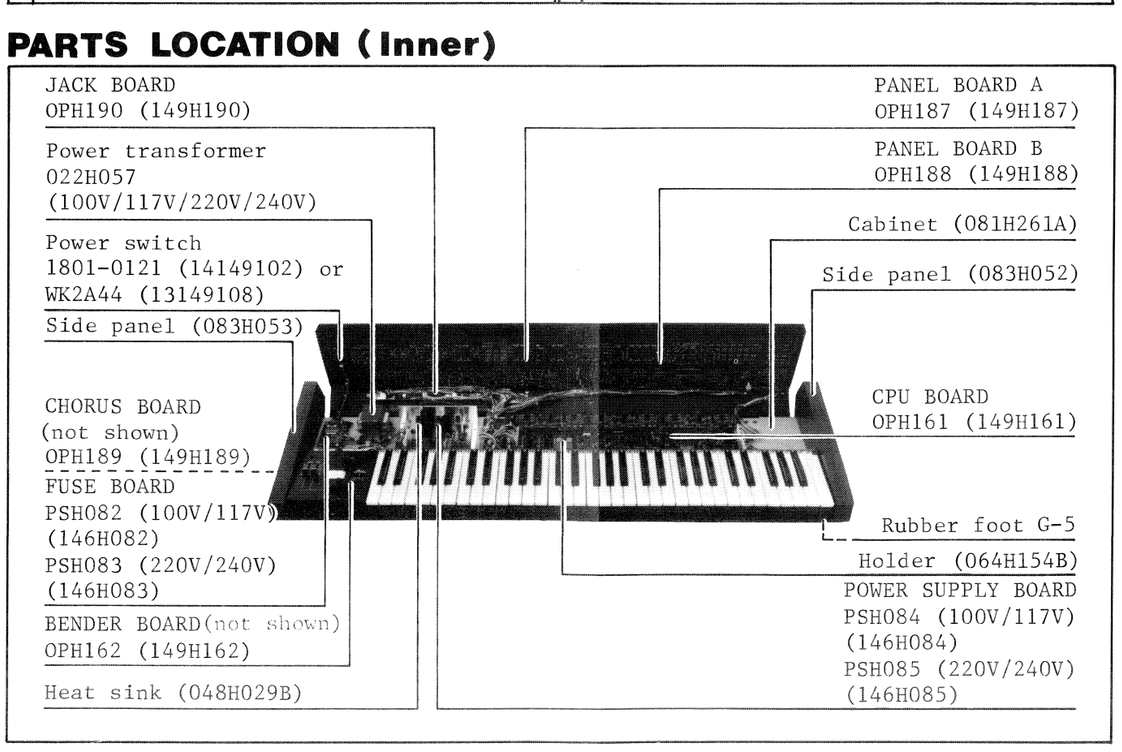
PARTS LOCATION (Top)



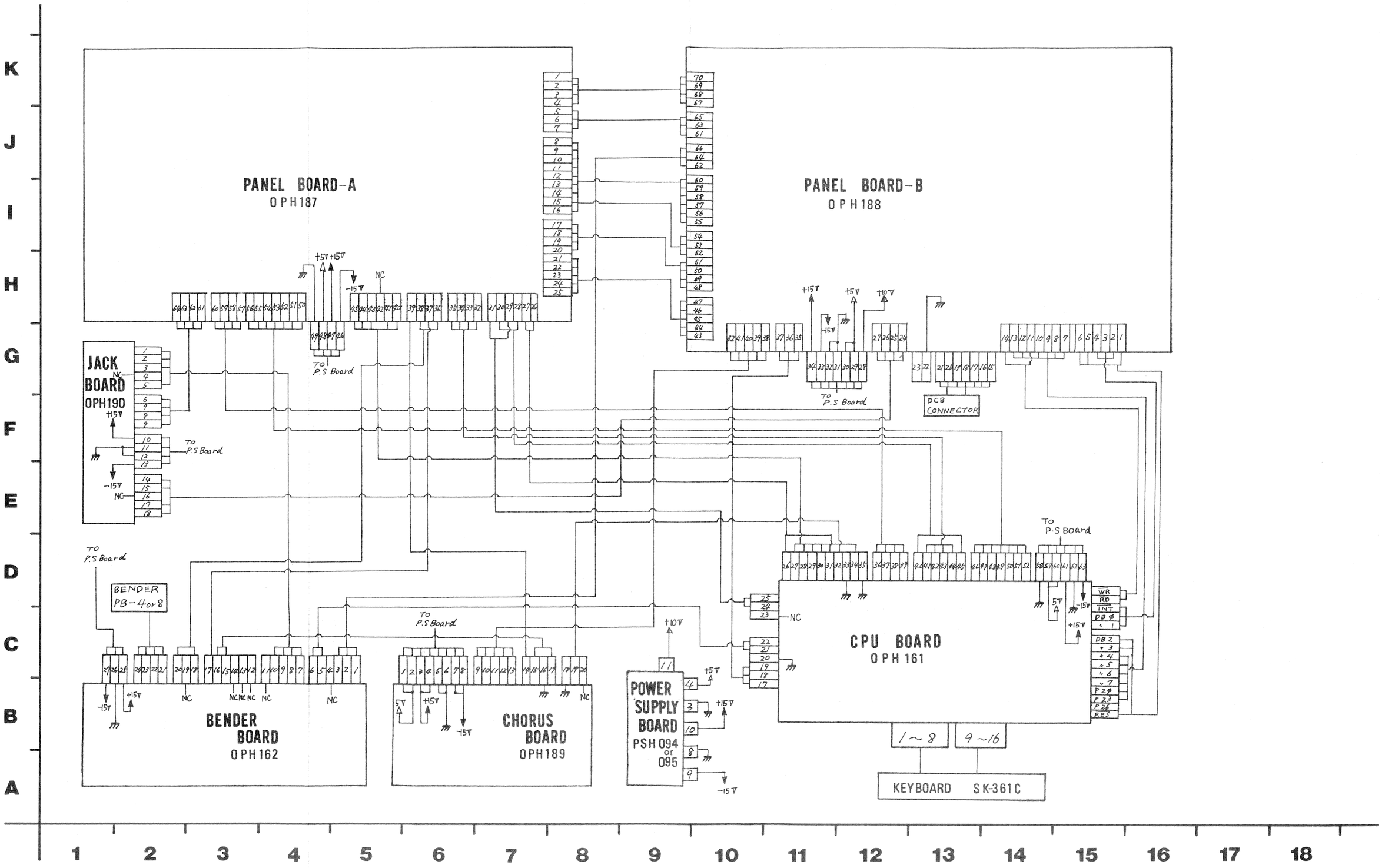


1	Switch 1801-0121 (13149102)		7	Pot. EVA-TOHC14A161MA (13339418)	Knob (016H004)
2	Switch SUT11A-1 (13129321)	Button	8	Pot. EVA-TOHC14A5450KA (13339410)	
3	Switch SUT11A-2 (13129322)	Orange (016H029)	9	Switch EVA-A03C14AGA (13159505)	
		Yellow (016H030)	10	Pot. EVA-TOHC14B5450KB (13339419)	
		White (016H036)	11	Pot. EVA-TOHC14A1410KA (13339416)	
4	Switch SLE-623-18P (13139135)		12	Pot. EWJ-EJAP20B1410KBX2 (13219759)	Knob (22470128)
5	Switch SLE-622-18P (13139136)		13	Switch ass'y KEH10003 (13129717) Switch (KEH10903) (See p. 13.)	
6	Switch KEJ10901 (13169605)	Button			
		Orange (016H037)		ALL LEDs TLR124 (15029103)	
		Yellow (016H038)			
		Grey (016H043)			
		White (016H044)			

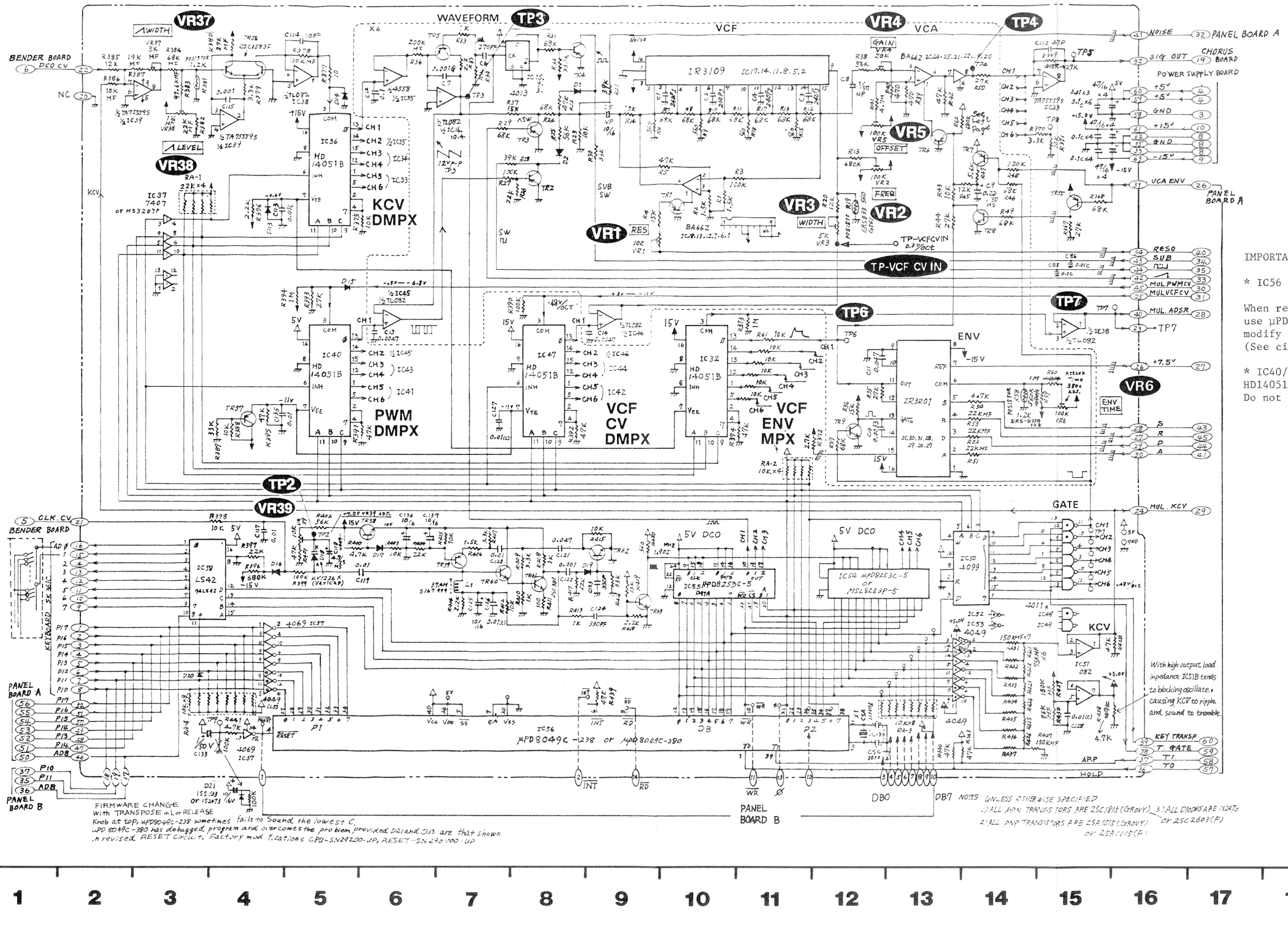
PARTS LOCATION (Inner)



INTERCONNECTION DIAGRAM



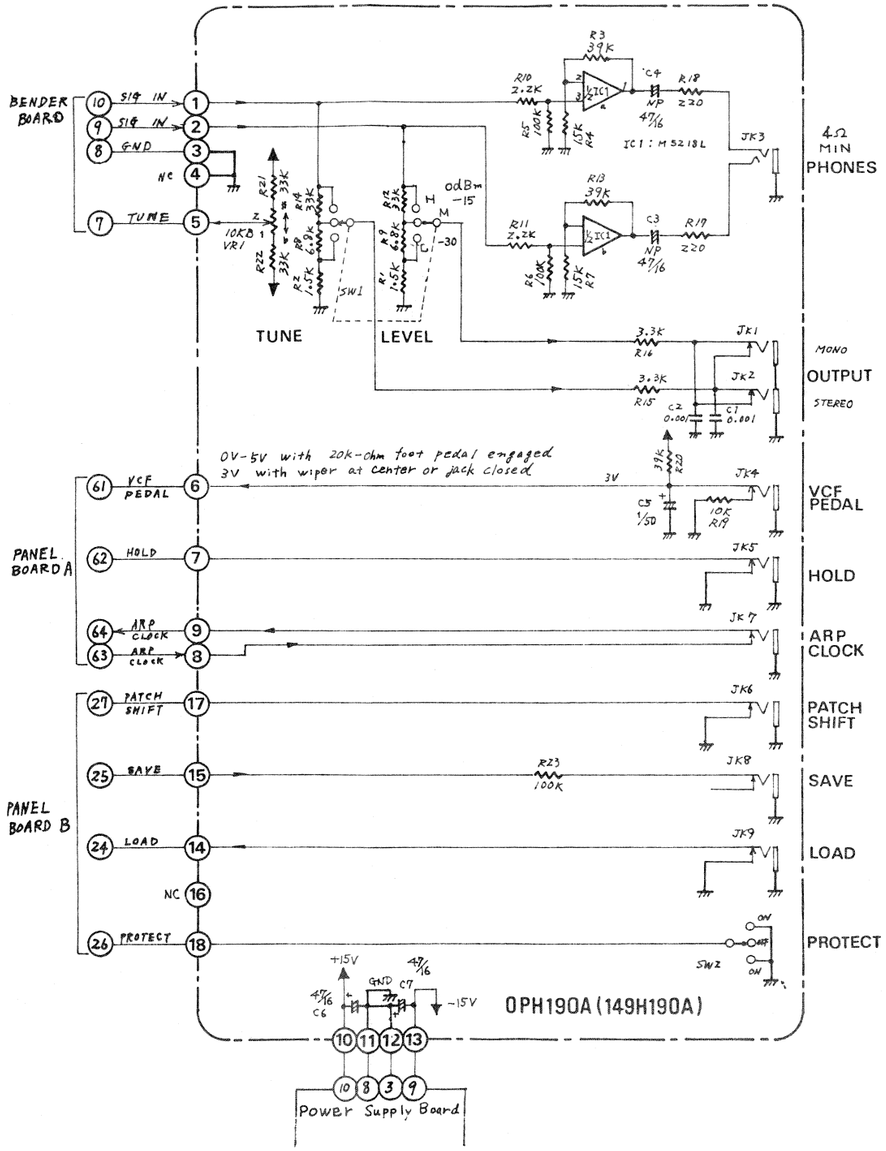
CPU BOARD



IMPORTANT (IC changes)

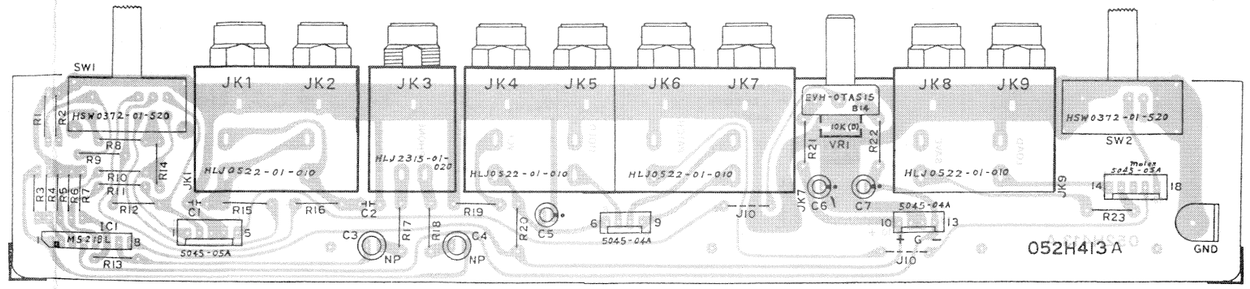
* IC56 (μPD8049C-238 to μPD8049C-380)
When replacing μPD8049C-238, use μPD8049C-380 version and modify RESET circuit. (See circuit diagram.)

* IC40/IC47
HD14051B only.
Do not use equivalents.



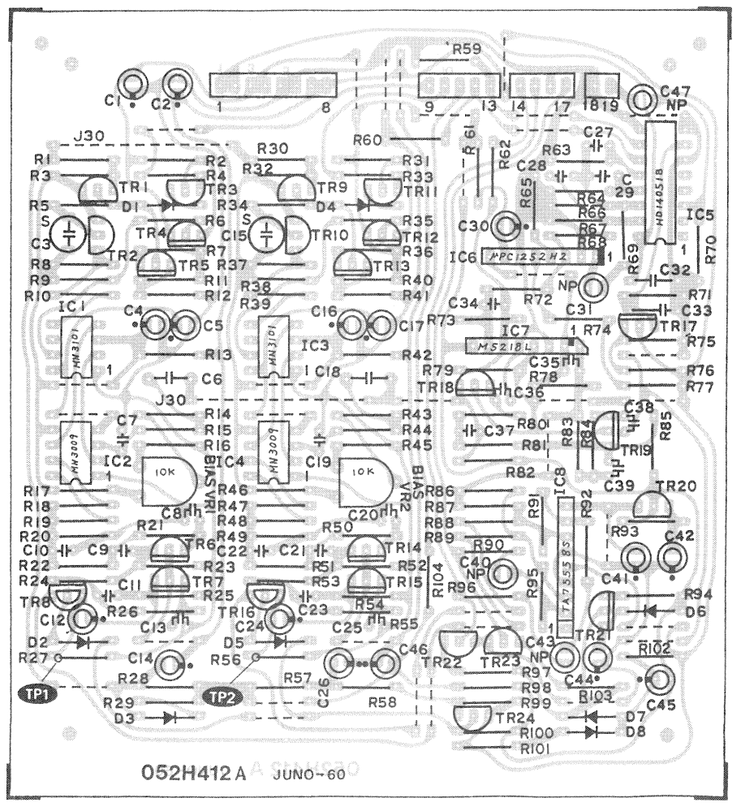
JACK BOARD

OPH190A (149H190A) (pcb 052H413A)

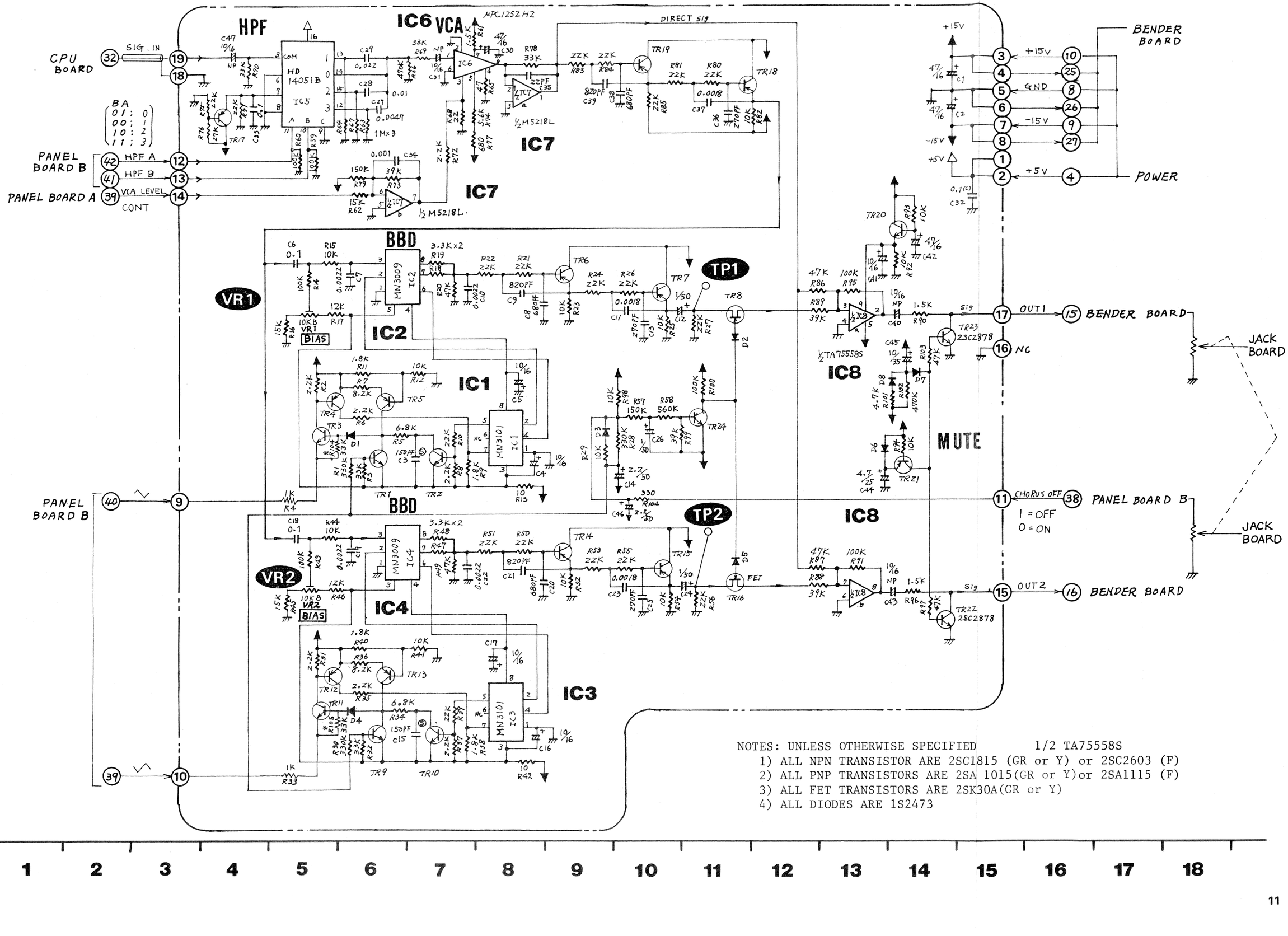


CHORUS BOARD

OPH189A (149H189A) (pcb 052H412A)

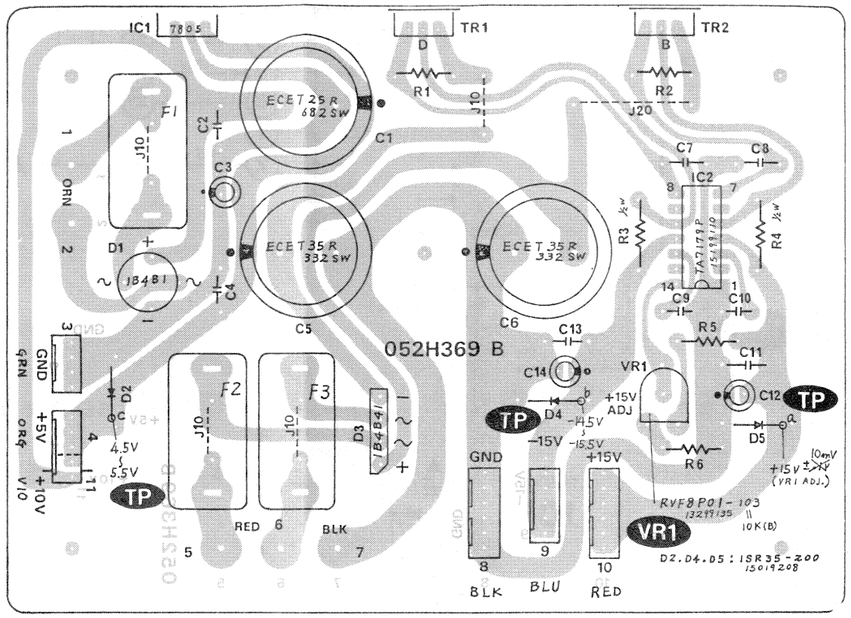


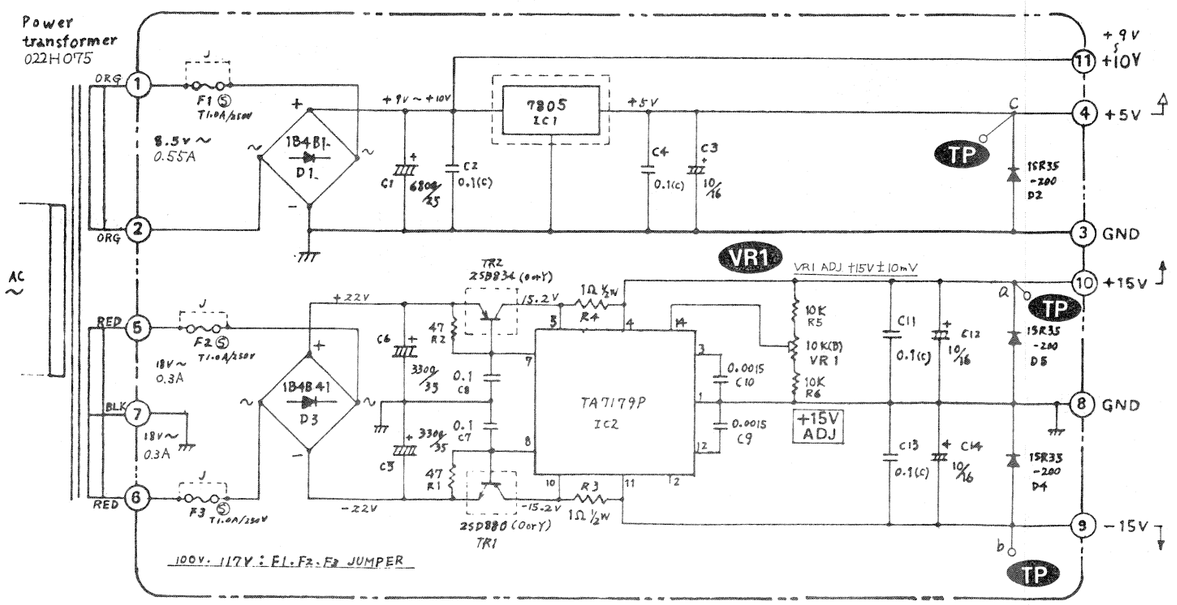
CHORUS BOARD



POWER SUPPLY BOARD

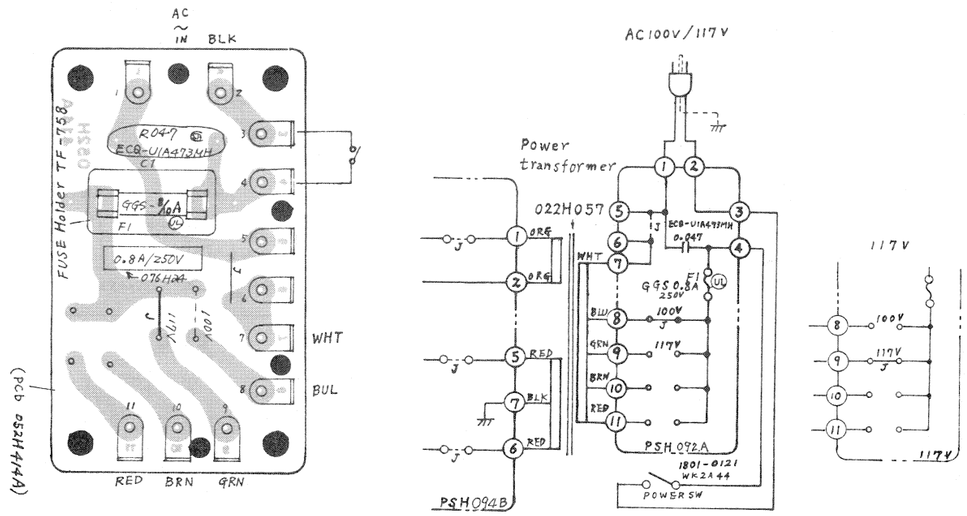
PSH094B (146H094B) 100/117V
PSH095B (146H095B) 220/240V
(pcb 052H369B)



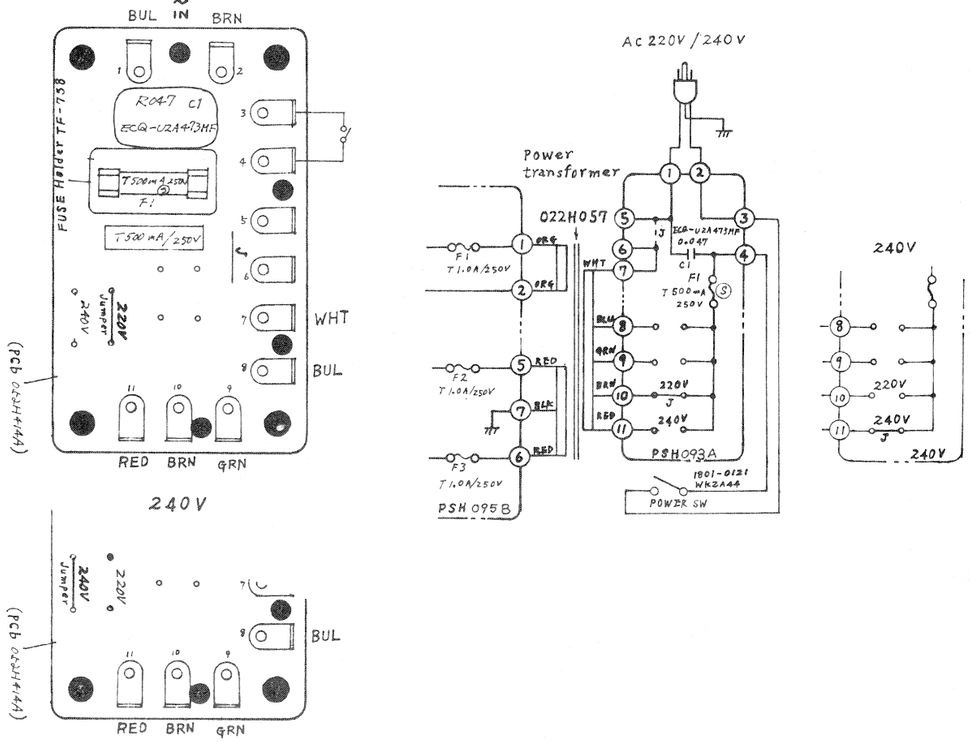


FUSE BOARD

PSH092A (146H092A) 100/117V

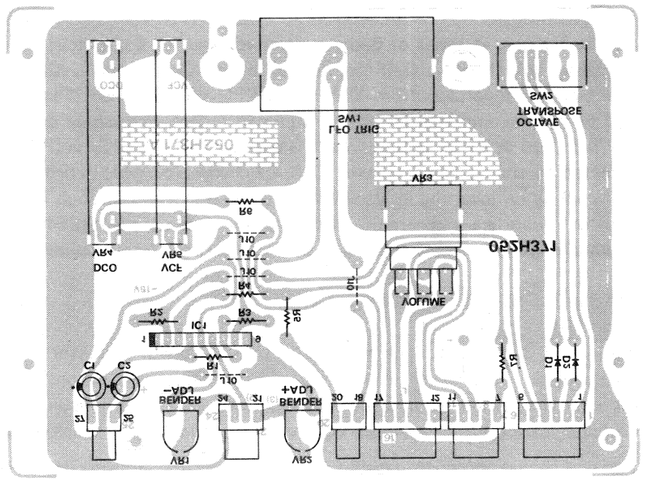


PSH093A (146H093A) 220/240V
(pcb 052H414A)

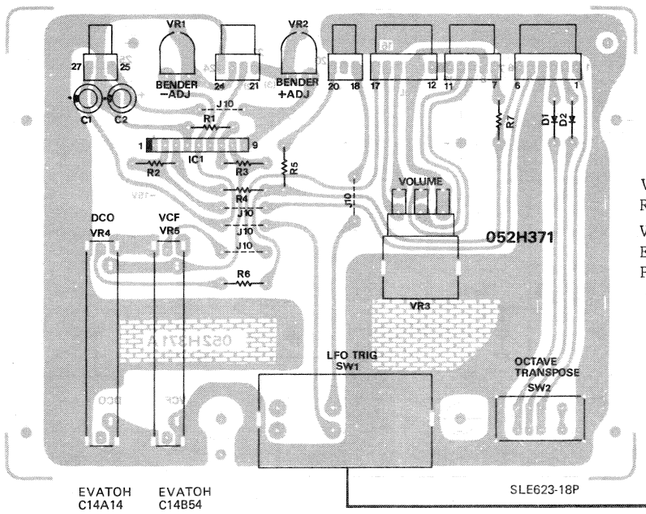


BENDER BOARD

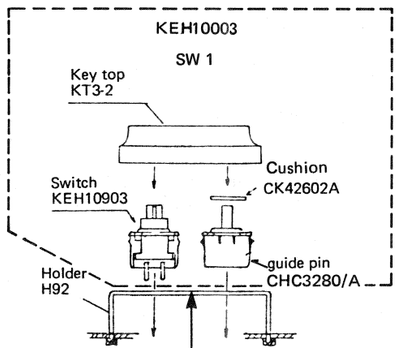
OPH162A (149H162A) (pcb 052H371A)



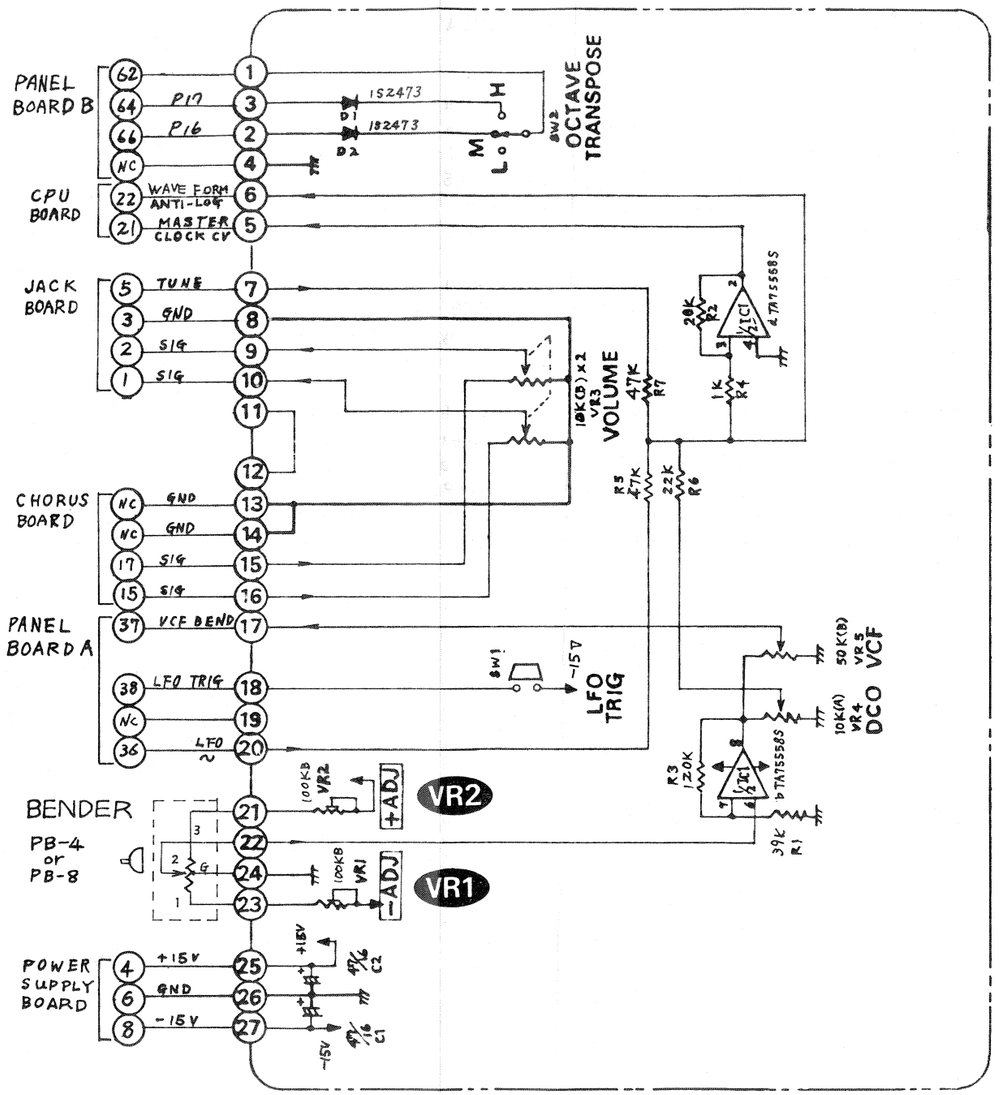
View from foil side



VR1, VR2
RVF8P01-104
VR3
EWJEJA
P20B14



View from component side



CPU BOARD

KEYBOARD AND SWITCH (NON PROGRAMMABLE) SCANNING

The CPU IC58 on the CPU Board applies sequential scanning data (in the leftmost column in Table 1 below) to Address Decoder IC58, setting its appropriate output pin low. Each pin will be connected to port 1 through switch contacts being closed and through inverters IC53 and IC57. The combination of highs and lows at port 1 (pins) tells the CPU which key is pressed, not pressed, or which position the switches are set.

Note: TRANSPOSE switch on Bender Board is not read directly but through SW LATCH IC9 on Panel Board B. TRANSPOSE is scanned beforehand together with the programmable switches by another CPU on Panel Board B.

The CPU IC56 stores two kinds of program for use in different applications, and knows its application at the very first of the scanning cycle. After power on reset, the CPU first issues bits 1001 (see bottom of Table 1) and knows that voices to be assigned to keys played are 6 (L, H, L at Port P10–P12) and that the model it is now installed is the JUNO-60 (L at P17). If the CPU malfunctions, voltages on these port pins and associated circuits (including D20) should be checked.

BUS 6543	PORT-1 0	1	2	3	4	5	6	7
0000	C	C#	D	D#	E	F	F#	G
0001	G#	A	A#	B	C	C#	D	D#
0010	E	F	F#	G	G#	A	A#	B
0011	C*	C#	D	D#	E	F	F#	G
0100	G#	A(442)	A#	B	C	C#	D	D#
0101	E	F	F#	G	G#	A	A#	B
0110	C	C#	D	D#	E	F	F#	G
0111	G#	A	A#	B	C	(C#)	(D)	(D#)
1000	TRANSPOSE		ARP & KEY ASSIGN		ARP RANGE		ARP ON	KEYTRANS
1001	L	H	L	not in use				L

Table 1

KEY ASSIGNMENT

Six channels are assigned to the keys played in the order CH1–CH6, in the cyclic manner, that is, when the 7th key is played while previously played 6 keys are still held, the 7th key steals the first voice.

Three more assignment modes are provided for test purpose. See Adjustment section of this manual.

DIGITAL COMMUNICATION

The JUNO-60 is furnished with a DCB interface for linking with external digital instruments. When the DCB interface circuit on Panel Board B is engaged in communication, it coordinates the transfer of data between two instruments by applying Low to INT of the CPU on the CPU Board (will be detailed under DCB Interface section).

SOUND SOURCE

When a key is played on the keyboard, the CPU (CPU BOARD) provides a set of independent data – Divisor for the programmable counters (IC54, IC55) and CV for WAVEFORM and VCF, to keep the voices sound alike with pitch differences corresponding to a key held.
Fig. 1 shows a simplified block diagram of sound source system, for clarity.

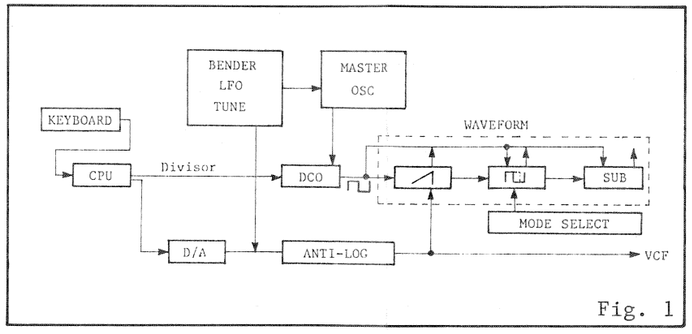


Fig. 1

Master Oscillators TR58-TR62

An LC oscillator having a variable capacitance diode (D18) to which control voltages from BENDER, LFO and TUNE, – common to all the VCOs, are supplied.

Variable range:
BENDER . . . . . ±700 cents
LFO . . . . . ±300 cents
TUNE . . . . . ±50 cents
When these voltages are summed together, the maximum shiftable range of the master oscillator is ±1050 cents or from 1MHz to 3.5MHz with the center frequency at approximately 1.9MHz. The output signal is routed to programmable counters IC54 and IC55 through TR63.

Programmable Counters IC54 and IC55

Programmable counter 8253 containing three 16-bit counters is capable of dividing high frequency signals, generated at the Master oscillator, by up to 65535. Assume that the master oscillator runs at 1902810Hz and a divisor is 4305, the counter develops 442Hz rectangular signals.
Each time key(s) is played, the CPU extracts division data for that key from the internal PROM and delivers it to DATA IN of the counters in 8 bit x 2 format.

Waveform Conversion

SAWTOOTH GENERATOR

Analog voltages (a series of 6 key control voltages for 6 channels) from D/A converter will change in 0.48/oct steps as different keys are played. KCVs are combined with voltages from TUNE, and LFO and BENDER if any, and are fed to anti-log amplifier TR56. The summed voltage increases or decreases in 1V/oct steps at TR56 output, which is passed on to one of S/Hs (IC33-IC35) selected by analog Demultiplexer IC36. C7 charges (current) in proportion to CV coming on inverting input pin of IC16 and discharges through TR5 at the rate of square wave generated from programmable counter (IC54 or IC55), maintaining the sawtooth amplitude constant over the frequency range.

VARIABLE PULSE WIDTH

Besides its direct application as sound source, sawtooth generator also serves as a source for asymmetrical square wave. Sawtooth wave is routed to (–) pin of comparator/S&H circuit where the voltage on (+) pin determines the sampling period of the sawtooth wave thus duty cycle of the square wave.

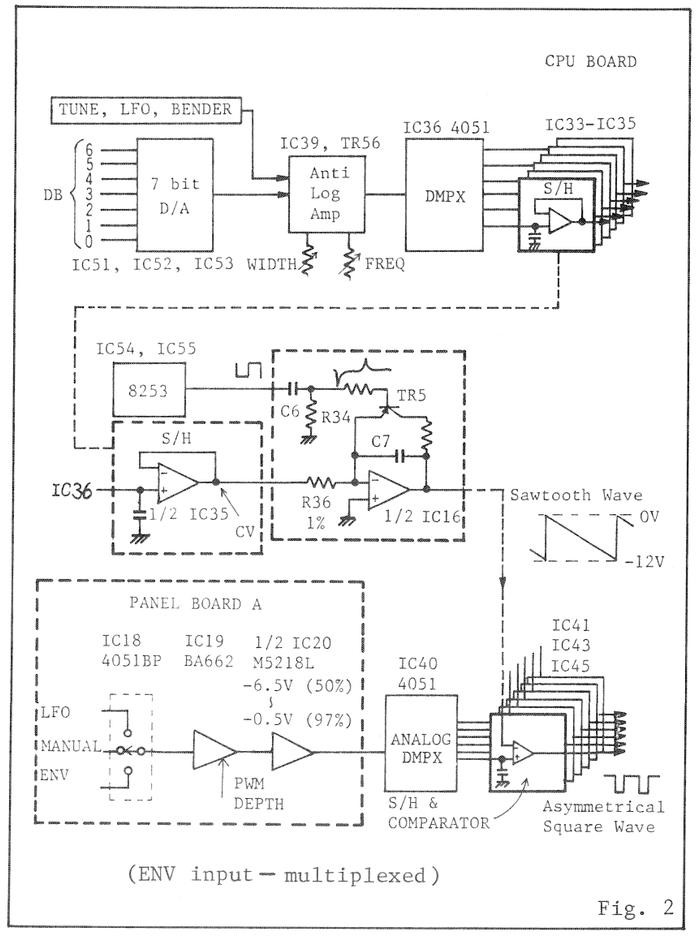


Fig. 2

SUB OSCILLATOR

Square wave from programmable counter is also delivered to flip-flop where it is divided in half, and applied to TR4 base. The amplitude of TR4 output can continuously be varied by setting of SUB VR20 on Panel Board A.

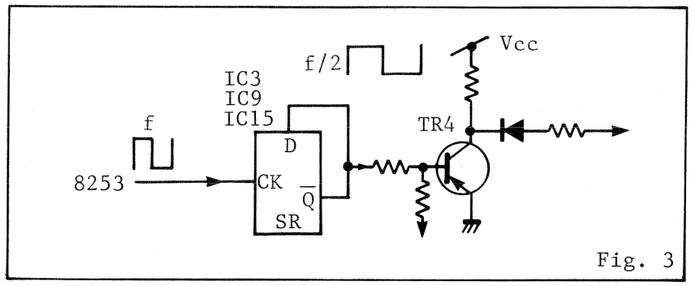


Fig. 3

VCF Control Voltages

While 6 contour voltages developed at ENV generator are running directly to mated VCAs on the exclusive line, they are multiplexed and carried through a common bus together with other control signals for VCF application. On the input pin of summing amp there is another multiplexed voltage (KCV) from D/A converters IC51-IC53 on CPU Board. These multiplexings are synchronized for stable data travel.

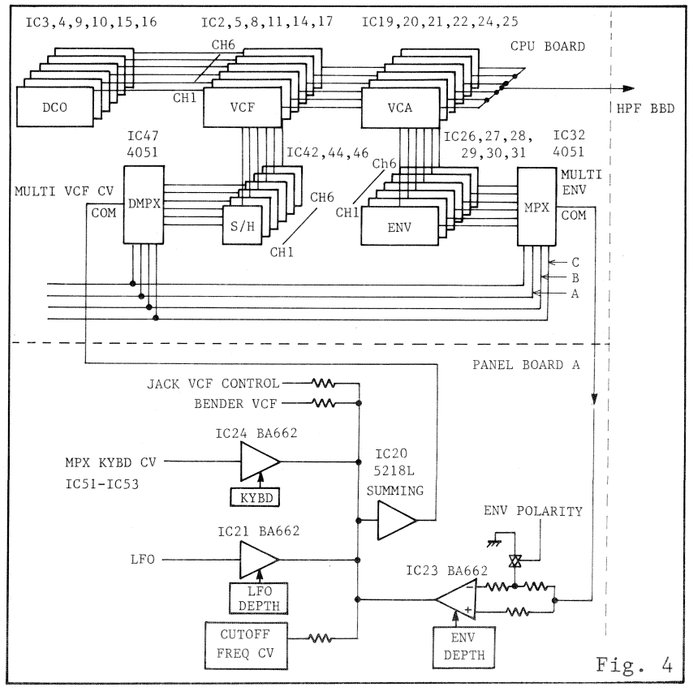


Fig. 4

PANEL BOARD B

CPU μPD80C49C–028

DESIGNATION	PIN NO.	FUNCTION
DB (Data Bus) DBφ	12	Prog SW Scan Display Drive / RAM Address / RAM Data / Slider and Switch Data / A/D Data
1	13	
2	14	
3	15	
4	16	
5	17	
6	18	
7	19	
PORT 1 P1φ	27	Prog SW Read / Display LED Drive
11	28	
12	29	
13	30	
14	31	
15	32	
16	33	
17	34	
PORT 2 P2φ	21	4051 x 4 Address (MPX, DMPX)] RAM x 2 Address
1	22	
2	23	
3	24	Chip Select 4051 CS x 4 40174B, TC40H273P WR Enable
4	35	
5	36	
6	37	
7	38	Tape Interface Output
XTAL-1	2	Inputs for Internal Clock Oscillator
XTAL-2	3	
$\overline{RESET}$	4	Reset Pulse Input
Tφ	1	Tape Interface Input
T1	39	A/D Comparator Input
INT	6	Protect SW Input (Low = Protect ON, High = Protect OFF)
$\overline{RD}$	8	RAM Read Pulse
$\overline{WR}$	10	RAM Write Pulse, 40174, 40H273 Latch Pulse
ALE	11	Address Latch Pulse

Table 2

The flowchart (Fig. 5) will be an aid in reading the description in this section.

① When a new BANK/PATCH button is pressed, the CPU calls "Read RAM" subroutine.
When BANK, PATCH and WRITE buttons are pressed, the CPU calls "Write RAM" routine.

② When the CPU finds a certain amount of descrepancy between the preceding reading and the new reading, it sets Edit Flag and updates the data being delivered.

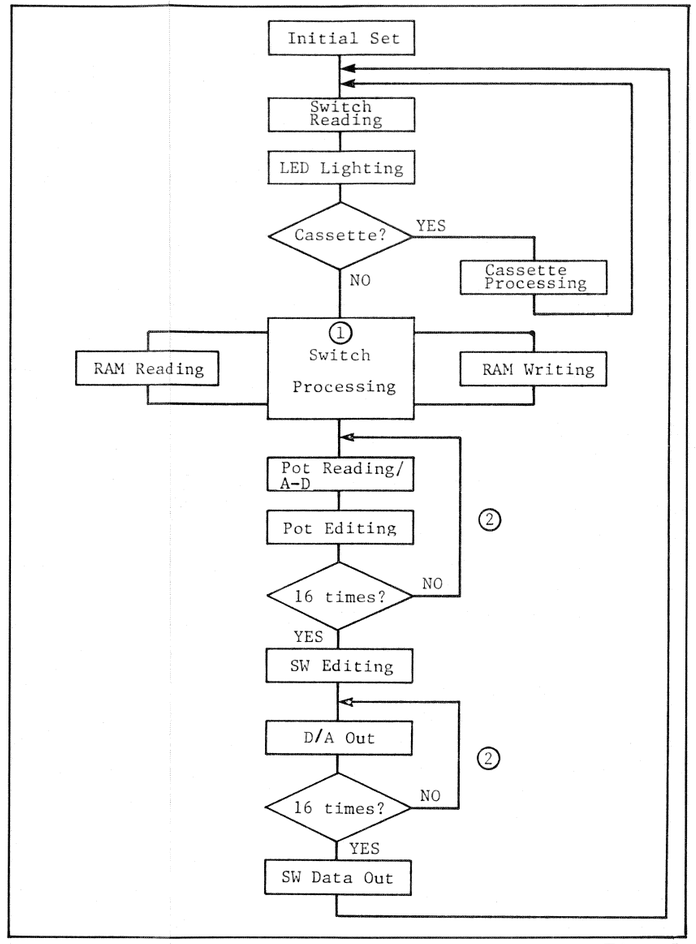


Fig. 5

SWITCH READING

The matrices for the programmable switches and memory switches are located on Panel Boards A, B and Bender Board. They are bussed together on Panel Board B. The bus is divided into five sections with maximum eight switches per section. Each bus section and switch contact are connected to the CPU on Panel Board B: bus section through Latch IC15 (latched on PROG) and through Decoder IC16; contact through Port 1.
The CPU maintains a serial data output (from DB) and reads the resultants from Port 1, in the same manner as described previously under KEY SCANNING.

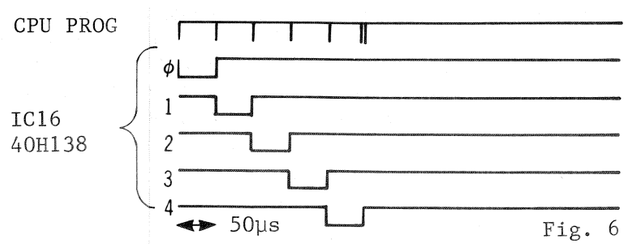


Fig. 6

40H -138	PORT-1 0	1	2	3	4	5	6	7
0	Manual	Write	Save	Verify	Load	not used	not used	not used
1	1	2	Bank Number 3	4	5	not used	not used	not used
2	1	2	Patch Number 3	4	5	6	7	8
3	Chorus 1	WAVEFORM Pulse/Sawtooth/SUB			Chorus 2	Chorus OFF	Transpose L/M/H/HH	
4	ENV Polarity	PWM MODE ENV/MAN/LFO		HPF Cutoff Freq		VCA ENV	Patch Shift	TRIG MODE

Table 3

SWITCH DATA OUTPUT

Of the switches read during the above switch scanning, 11 programmable switches are organized in 14 bit group in the CPU and are divided into two fields when being sent out from the CPU. At the very end portion of the program loop, the CPU first issues 6-bit data on the data bus and IC13 latches it into IC8 with ALE. Then the next 8-bit is directly fed to IC9. IC8 and IC9 latch out 14 bit data at the same time when the Port 2 presents bits X1110XXX.

It should be noted that TRANSPOSE information only is routed to and involved in the CPU Board switch matrix for further processing, while the remaining switch data are delivered directly to respective destinations.

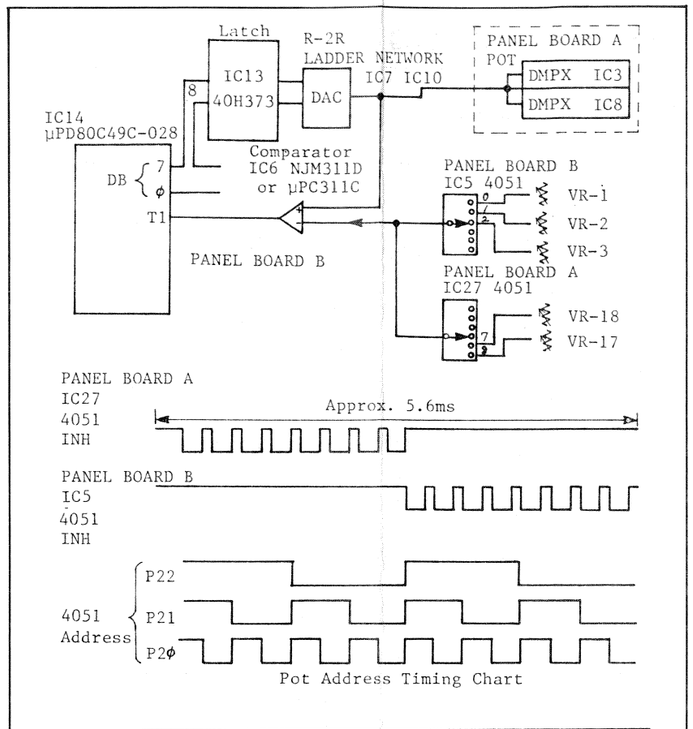
	IC PIN NUMMBER	SW FUNCTION	IC8,IC9 OUTPUT			
IC8 40174B	10	VCA ENV SEL	0=⎍, 1=⎍			
	12	HPF CUTOFF FREQ.	0	0	1	1
	15		0	1	2	3
			1	0	0	1
	9	PWM MODE	0	0	1	1
			LFO	MAN	ENV	X
	5		0	1	0	1
	2	ENV POLARITY	0=∩, 1=∪			
IC9 40H273	5	TRANS-POSE	0	0	1	1
			L	M	H	X
	2		0	I	0	1
	12	LFO TRIGGER	0=AUTO, 1=MAN			
	19	CHORUS 2	0=ON, 1=OFF			
	15	SUB OSC ON/OFF	0=ON, 1=OFF			
	16	⎍ ON/OFF	0=ON, 1=OFF			
	9	⎍ ON/OFF	0=ON, 1=OFF			
	6	CHORUS 1	0=ON, 1=OFF			

Table 4

POTENTIOMETER MULTIPLEXERS AND ADC (PANEL BOARDS A, B)

MULTIPLEXER

All 16 programmable pots are divided between Panel Boards A and B, with each 8 pot group connected to an associated Pot Multiplexer. Pot MPX and ADC (Analog to Digital Converter) allow the computer on the Panel Board B to read and therefore to store the knob settings into RAM for a patch. Addresses specifying the pots to be sampled are fed from Port 2 as shown in Fig. 7. Pot MPX program starts with VR17 DELAY TIME when INH is applied from Latch IC19 on Panel Board B. The MPXer IC27 (Board A) sequentially connects each pot wiper (on Board A) to the ADC which represents analog equivalent of Pot Value in 8 bit format.



	VR	PARAMETER	PORT 2 6 5 4 3	2	1	φ
PANEL BOARD B	1	VCF Env Depth	1 0 0 0	0	0	0
	2	VCF LFO Depth		0	0	1
	3	VCF KYBD Follow		0	1	0
	4	VCA Level		0	1	1
	5	Env Attack		1	0	0
	8	Env Release		1	0	1
	6	Env Decay		1	1	0
	7	Env Sustain		1	1	1
PANEL BOARD A	22	Cutoff Freq	1 0 0 1	0	0	0
	21	Noise Level		0	0	1
	20	Sub OSC Level		0	1	0
	23	Resonance		0	1	1
	19	Pulse Width		1	0	0
	16	LFO Rate		1	0	1
	18	DCO LFO Depth		1	1	0
	17	Delay Time		1	1	1

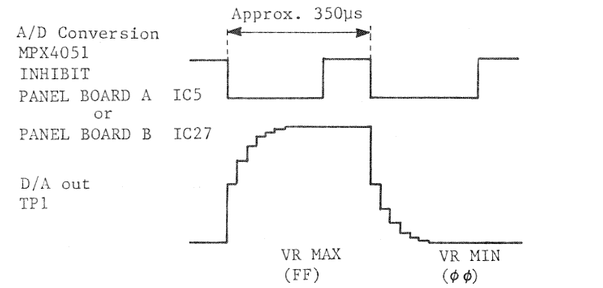
Fig. 7

ADC

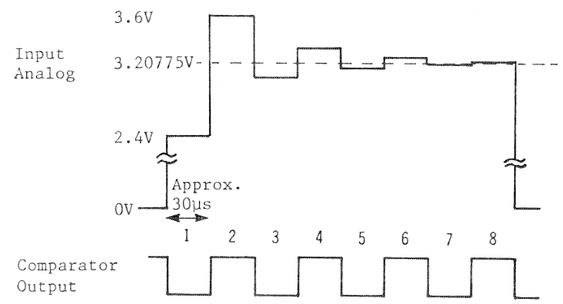
The ADC is based on a Successive Approximation consisting of DAC, comparator and CPU's internal "register". To convert a Pot value the CPU (Board B) first issues 10000000 on the data bus. IC13 latches MSB which is weighted by ladder resistors, converted to 2.4V of analog equivalent then passed on to non-inverting input pin of IC6, comparator. Being fed lower voltage on (+) input than on (–) input signal being compared, the comparator turns its output low, telling the computer to keep MSB high. Then the CPU places the next bits 11000000 which caused (+) input of the comparator to rise to 3.6V, which, in turn caused comparator output to turn high, resetting DB6 to 0.

In the same manner the CPU compares all the bits down to DB0 against the comparator's (–) input signal and establishes the digital data for that Pot value.

This procedure is repeated 16 times for all 16 pots.



The analog voltages at the VRs are converted into 8-bit digital data.



D/A Converter Input

	1	2	3	4	5	6	7	8
DB7	1	1	1	1	1	1	1	1
DB6	0	1	0	0	0	0	0	0
DB5	0	0	1	1	1	1	1	1
DB4	0	0	0	1	0	0	0	0
DB3	0	0	0	0	1	1	1	1
DB2	0	0	0	0	0	1	0	0
DB1	0	0	0	0	0	0	1	1
DBφ	0	0	0	0	0	0	0	1

Fig. 8

POT DATA OUTPUT

An 8-bit data representing pot setting is placed on the CPU bus 16 times for each pot. Each 8-bit is latched by IC13, D/A converted by R-2R and sent to IC3 and IC8 (POT DMPLXER) on Board A, where it is distributed to a channel addressed by port 2.0-2.3 of the CPU (Board B) at a sampling rate of INH from IC19 (Board B).

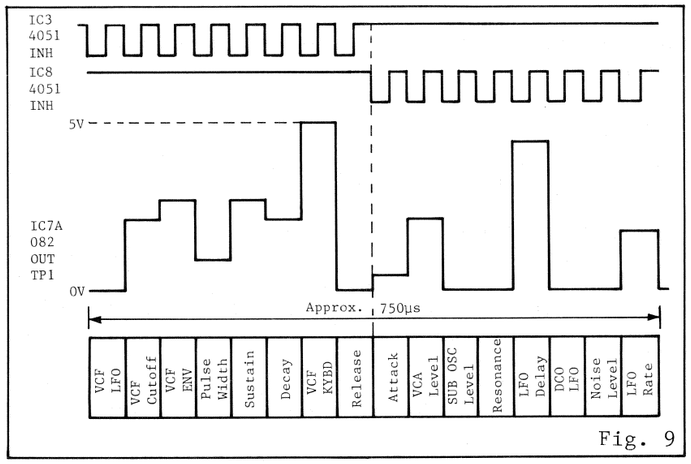


Fig. 9

DISPLAY LED LIGHTING

Being an I/O port, the Port 1 changes its state to output mode immediately after finishing switch readings, delivering display LED driving signals to LED board. Alternately swinging outputs (pins 9 and 10) of IC16 allow upper and lower LEDs to conduct at duty cycle of nearly 50 of dynamic lighting. The peirod 7.2ms in the timing chart (Fig. 10) is the time required for the CPU to complete one program loop.

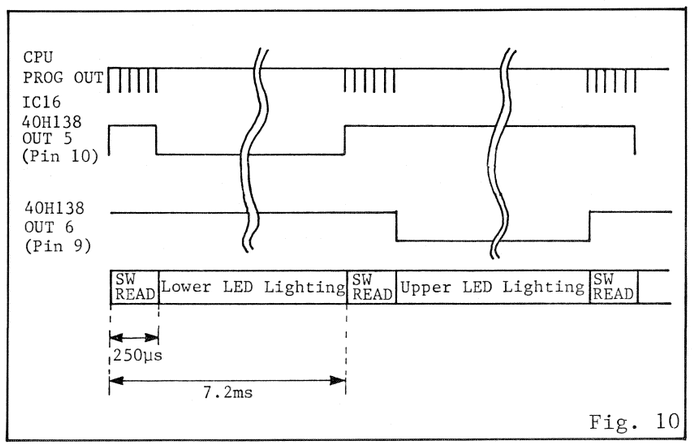


Fig. 10

MEMORY

Two identical RAMs (4K bit – 4x1024) make up the patch memory, which can store up to 1K byte (8x1024 words). Each memory cell is addressable with 10 bits. MSB 2 bits come from ports 2.0 and 2.1. The remaining LSB 8 bits from Data bus are latched into RAMs by IC13 with ALE.
RAM chip select (CS) is accomplished under the conditions
Port 2 = X1111XXX
$\overline{WR}$ or $\overline{RD}$ = low
$\overline{RESET}$ = high.
The CPU can extract RAM memory only when $\overline{WR}$ is ANDed with PROTECT at IC18.

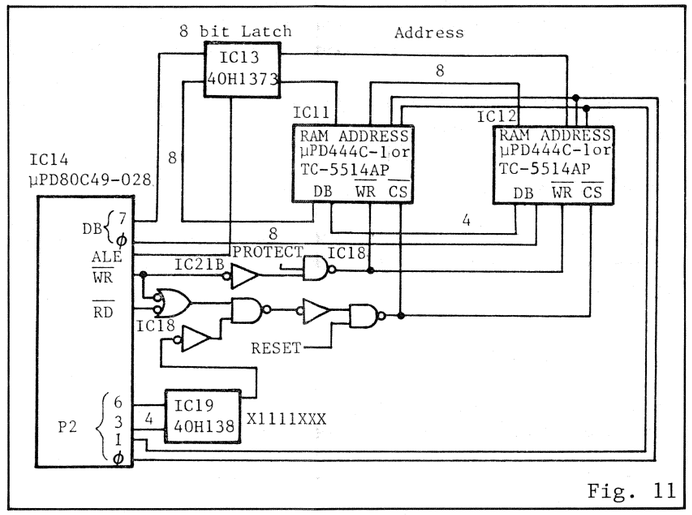


Fig. 11

TAPE INTERFACE

The CPU (Board B) transfers the programmed data to or from a cassette recorder through Interface circuitry at approx. 340 baud (340 bits/s).

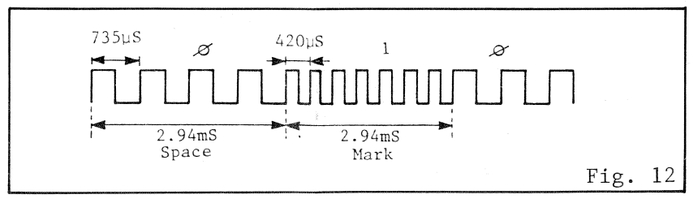


Fig. 12

SAVE

Pressing SAVE button allows the CPU to convert a set of patch data bits to square waves: 0 (space) to four cycles of 1.36kHz and 1 (mark) to seven cycles of 2.38kHz, and to send them from Port 2.7. The modulated bits are applied through IC21E (inverter) to IC22A (LPF) where their high order harmonics are rolled off by 12dB/oct slope and lower components by C22 (6dB/oct HPF) before being passed on to SAVE jack.

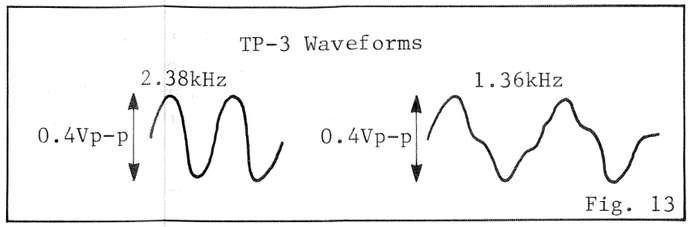


Fig. 13

LOAD & VERIFY

Data from tape reach TO of the CPU by way of C23 x R82, HPF to eliminate DC component and fluctuation; IC23A, amp and LPF (12dB/oct); IC23B, comparator to have their shape restored to rectangular whose wavelength enables the CPU to perform calculation on the input wave lengths to determine the bits value (0 or 1). The tape interfacing directly involves the software and forces the CPU to stop most of other jobs (lighting display, refreshing S/H, reading pots and switches). During the tape modes output 0 (pin 15) of IC16 (decoder) is clamped to low to let a tape mode indicator light up and to allow the CPU to escape from the tape routine when MANUAL is pressed.

DCB (Digital Communication Bus)

The JUNO-60 can be controlled from the external equipment which transmits the control voltage in the form specified in this section. The JUNO-60 can also control an external "musical instrument" which accepts data made in the form described in this section. The CPU on the CPU Board communicates with an external equipment through DCB (Digital Communication Bus). IC24 on the Panel Board B interfaces them (CPU and EXT instrument).

INTERFACE

The IC24 is the 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. In the JUNO-60 the 8251A is configured as Asynchrous Receiver/Transmitter (USART).
The 8251A will signal the CPU (on the CPU Board) whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of 8251A, when INT goes low under one of the following conditions, by turning C/$\overline{D}$ to high (1) and READ to low (0), entering Interrupt Handling Routine.

INT LOW CONDITIONS: RxRDY – 1 (H)
or TxEMPTY – 1 (H) and TX BUSY – 1 (H)
(DCB connector)

* RxRDY: 1 (H)
This output indicates that 8251A contains a character that is ready to be input to the CPU, requiring the CPU to accept the data.

* TxEMPTY: 1 (H) & TX BUSY: 1 (H)
When the 8251A has no characters to transmit, TxEMPTY will go "high" which is inverted by IC27D (Panel Board B) and applied to pin 4 of IC27C. If the receiving party is transmitting RX BUSY (which is a low TX BUSY at the JUNO-60's DCB connector), IC27C cannot turn IC27B output to low, having INT signal remain low.

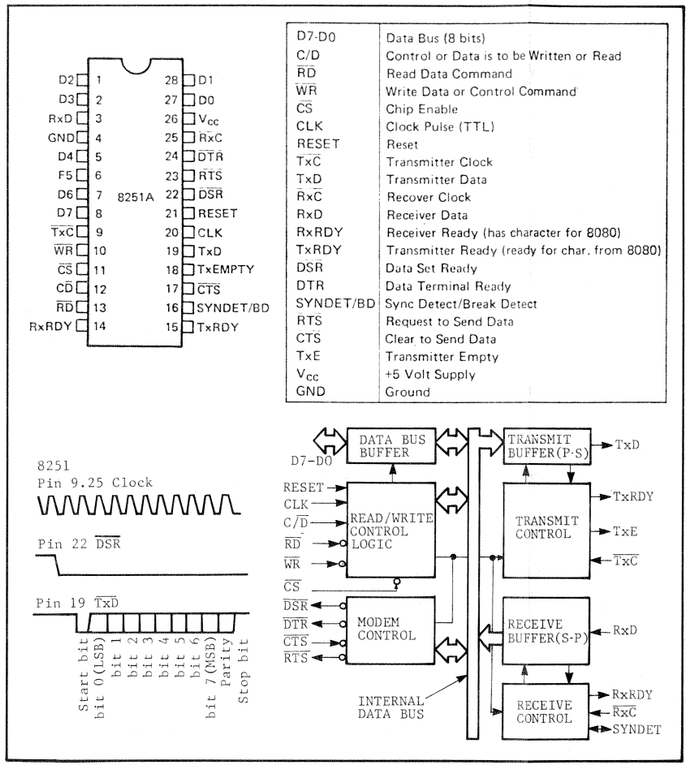


Fig. 14

DCB DATA FORMAT

The Data format described in this section is commonly applicable to Roland products furnished with the DCB connector. Variations unique to individual models and problems which might happen in linking the JUNO-60 to other DCB instruments will be discussed in more detail later.

GENERAL SPECIFICATIONS

* BLOCK

Basically, a block is comprised of three codes: one Identifier, one or more Data Codes and one End Mark. The transmitter can send a block (containing identical information) either continuously or intermittently at 10ms–100ms intervals to assure stable information transmission. In an interval transmission system, the transmitter must send a new block upon occurring of change in the information. The new block must contain both changed and unchanged data.

* IDENTIFIER

At the head of each block is a 1-byte identifier which uses a value within 0F1H (241) through 0FEH (254) to signify the kind of DATA CODE that follows. 0FDH (253) – PATCH CODE, 0FEH (254) – KEY CODE, others are undefined. Any data which follows an Identifier must not include these values.

* DATA CODE

A Data code is comprised of one section or series of sections (each 1 byte, called channel–CH) containing the information defined by the identifier. The code length (number of channels) depends on circuit configuration of the transmitter. Once a communication is established over DCB, the code length and the transmission order of the channels should not be changed throughout the communication.
Some identifiers will be accompanied by the code of predetermined length. (Exp. PATCH CODE–1 byte.)

* END MARK

An End Mark is necessary unless the code length is predetermined by the identifier or the block is to be automatically terminated by the identifier of the next block.

* DATA PROCESS

The receiver begins processing data code at the moment it accepts the End Mark or the Identifier at the head of the next block.

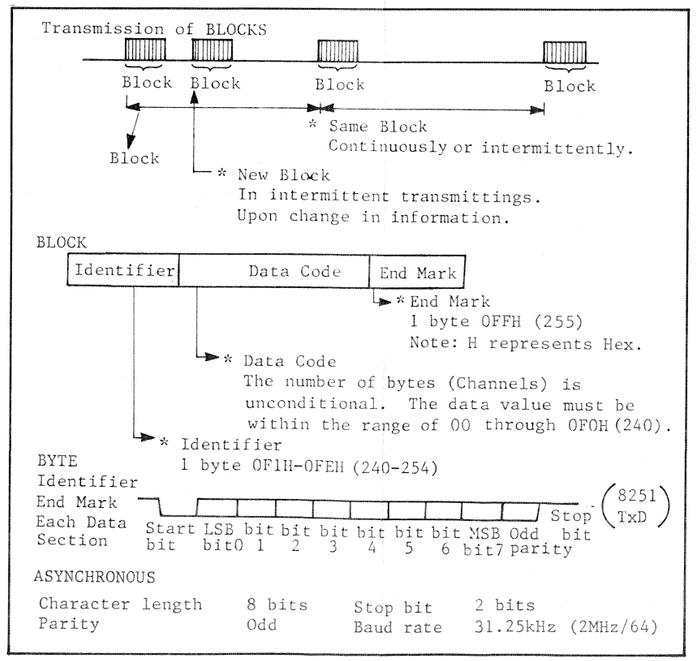


Fig. 15

DETAILED SPECIFICATIONS

This part mainly discusses the Key Code, only which the JUNO-60 deals with and problems that may arise in linking the JUNO-60 with other DCB instruments, e.g. OP-8 and JP-8. Some differences in the data format and transmission will exist between models.

* BLOCK

The JUNO-60 transmits blocks continuously, while the JP-8 and OP-8 intermittently.

* IDENTIFIER

Two Identifiers are already defined:

0FDH (253): Patch Code
Indicates that the code is 1-byte format representing Patch Number or Patch Preset Number.
This code is employed in the JP-8 and the OP-8. The JUNO-60 does not deal with this code. It ignores the data following this identifier.

0FEH (254): Key Code
This signals the receiver that the following data is for key information (key number and gate).
The length of the data:
JP-8 and OP-8 – 8 bytes
JUNO-60 – 6 bytes

* DATA CODE

Patch Code

The JP-8 and OP-8 send this code together with the Key code for each change in Patch data and do not transmit it again.
This block does not accompany End Mark.

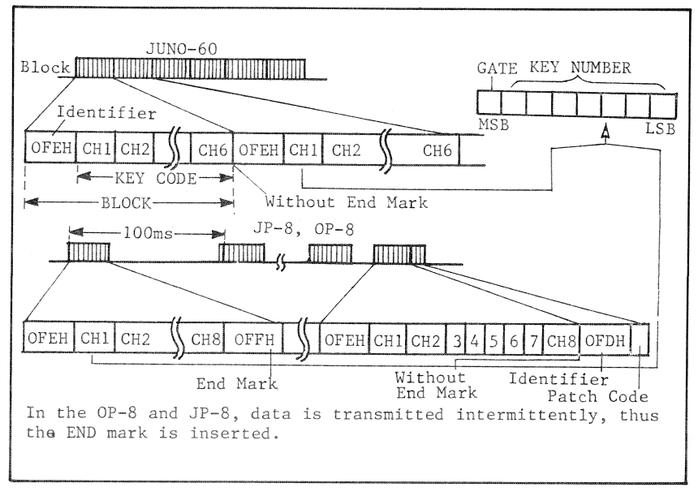


Fig. 16

Key Code

The Key Code is preceded by the Key Code Identifier (0FEH 254). Since the JUNO-60 is so configured that it accomodates only Key Code, the CPU (CPU BRD) returns to the main routine if identifier bits is other than 0FEH, ignoring the subsequent data.
The transmitter assigns the keys played on its keyboard to individual channels, coding each key information in 8-bit format where MSB 1 bit represents GATE ON (1) or OFF (0). The remainder (7 bits) represents key designation (name) listed in the table below (Fig. 17) (Hexa-decimal). Then, the transmitter places all the channels on the DCB sequentially in the order of its key assign mode. The receiver, upon receiving channels, assigns its voices to them by its own key assign mode which will differ between models. Fig. 17shows some rather distinguishable key assignments. The transmitter need not delete the unnecessary channel(s), instead it turns MSB to 0 (GATE OFF).

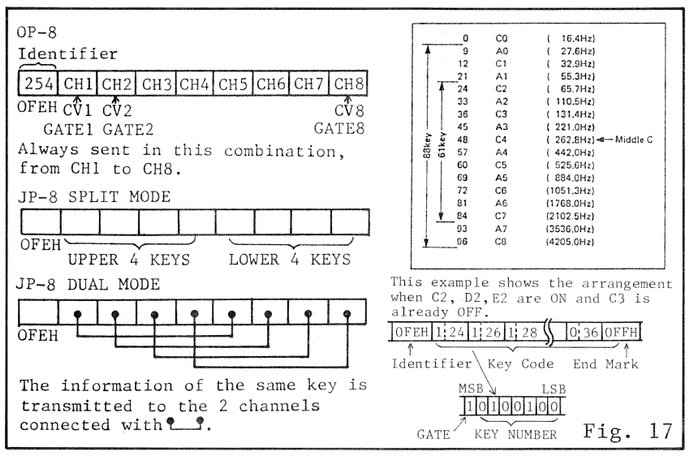


Fig. 17

KEY ASSIGN TO BUILT-IN & EXTERNAL KEYBOARDS

When "external keyboard" is connected to the JUNO-60 through the DCB, the CPU recognizes it as one being connected to the built-in keyboard in parallel and assigns its voices to whichever the key played on both keyboards. However, if two keys of the same note are played at a time on both keyboards, the program gives priority to the key first played as long as the GATE is ON. This fact may trick the player when he plays the JUNO-60 with SUSTAIN set shorter than the gate duration of the note being reproduced. For example, if he plays C4 right after the C4 note activated by DCB dies away, it doesn't sound. To retrigger the gate both keys must once be made OFF, then one key is pressed again.

KEY CODE INCLUDING MORE THAN SIX CHANNELS

What will happen if more than 6 channels are fed from the external keyboard to the JUNO-60? In this case, of course, 7th and subsequent keys have to wait until reserved channels are cleared, either by releasing of keys or by software. The software steals a voice from a channel whose gate first turned ON among 6 channels. Then the program assigns the voice again to 7th channel and so on as long as new channels are coming. This featue enables the JUNO-60 to accept limitless channels within a key code. Contrast to this, the JP-8 can receive 8 channels only at a time.

LINKING DCB DEVICES

Two cables are available for connecting DCB units, DCB Cable H172 and H165.

DCB Cable H172 is uni-directional, with the signal-flow direction shown by the arrow on the connector.
When connecting two JUNO-60 or JP-8 units, be sure to connect the cable so that the arrow points away from the JUNO-60 or JP-8 unit to be played, and towards the JUNO-60 or JP-8 unit to be controlled.
Also, when controlling the JUNO-60 with the OP-8, DCB Cable H172 can be used to connect the OP-8 to the JUNO-60.
Be sure to connect the cable so that the arrow points away from the OP-8 and towards the JUNO-60. Otherwise, the JUNO-60 may operate incorrectly.
On the other hand, DCB Cable H165 is a bi-directional cable in which sent from the TX-terminal on a unit returns to the RX-terminal on the unit, causing regeneration.

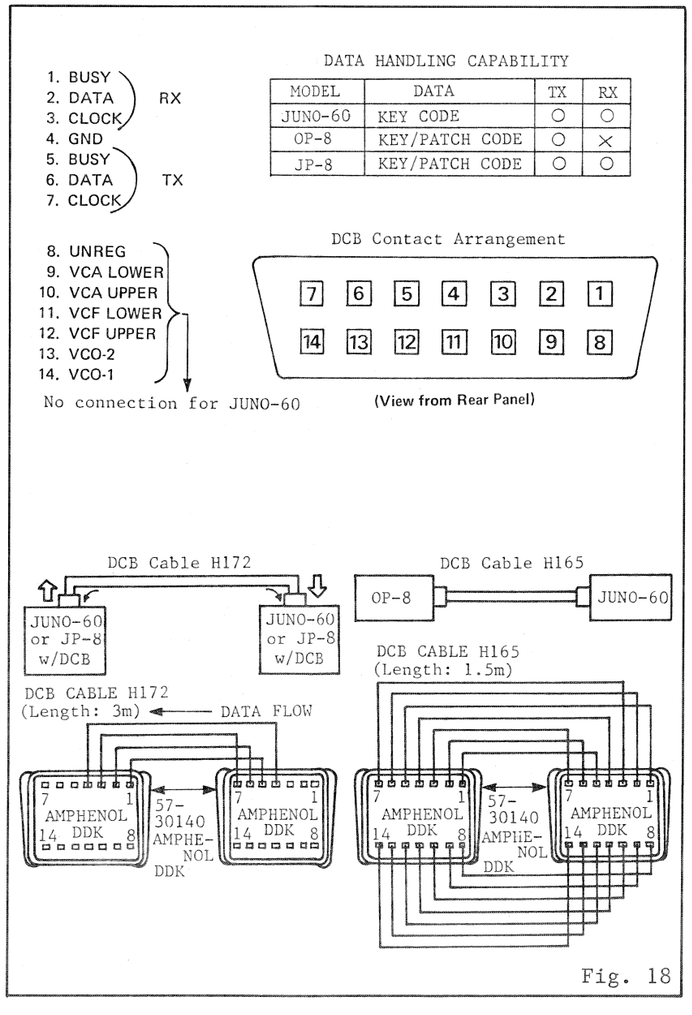


Fig. 18

GROUND LOOP NOISE

Because of the AC ground, a "ground loop" may be created when the DCB cable is connected between the JUNO-60 and its party (equipment). As a result, a certain-level digital noise may occur. In the later JUNO-60 the noise is considerably reduced by rearrangement of ground paths together with installation of Panel Board B of improved version, 052H411C (pattern relayout).
The modification is conducted at the factory on the units with serial numbers 253800 and subsequent.
For the units prior to SN253800, alternative modification can be made for the purpose of noise reduction.
See Fig.19.

Note: This modification has no effects on the later units.

Caution: Do not disconnect GND from DCB connector (Pin 4). Floating digital GND path may induce noise in other signal path.

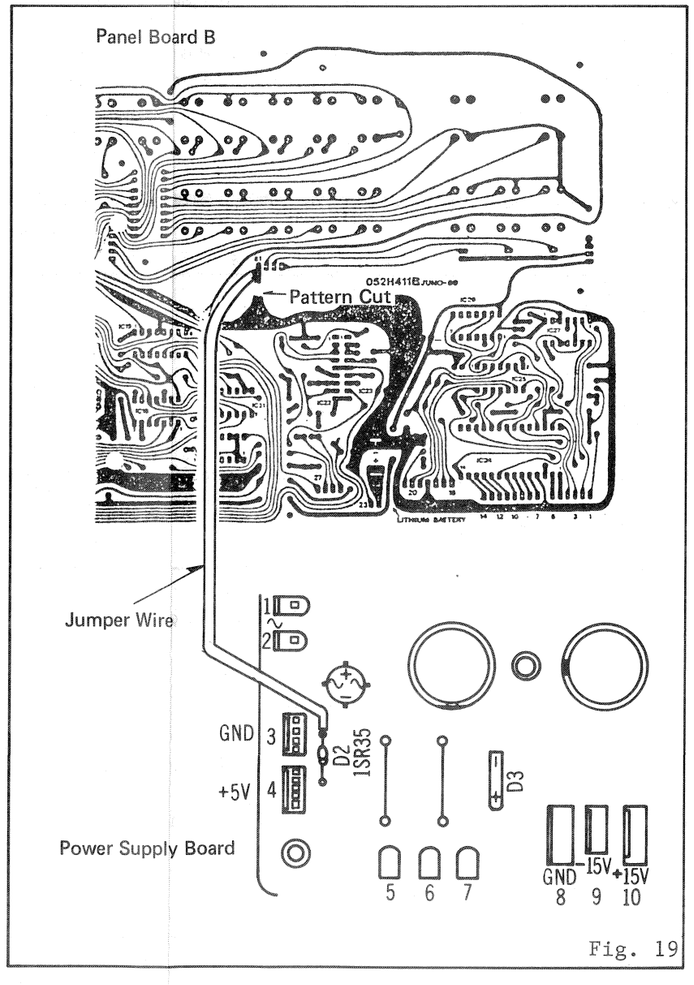


Fig. 19

RAM MEMORY TEST

The JUNO-60 has RAM TEST Program. In the RAM test mode, the program writes to each RAM chip and reads the data back to find any defective memory cell that may exist in the RAMs. If there is an error, the memory address will be displayed in the PATCH NUMBER window in Hexadecimal figure, as exampled below. (Fig. 21)

Caution: * All programmable data will be erased during the test. Save them on tape before testing.
* RAM should not always be defective if indicated by "error display". Check DATA BUS and their associated ICs, Trs, etc. for short or open.

HOW TO RUN TEST PROGRAM

1. Set controls as indicated by arrow.
2. Insert a bare plug into PATCH SHIFT jack on the rear panel to open the circuit.
3. While pressing CHORUS OFF and II buttons, switch the power on.

The program starts with the lowest address, so if a RAM is seriously defective, it displays "00" and stops there. When program sees an error, it won't step to the next address unless correction is made.

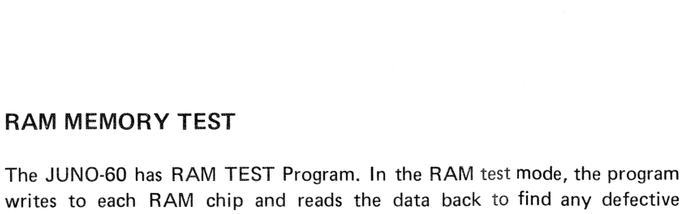


Fig. 20

If no defect is found in the RAM during the test, write data 81 (a continuous square wave sound) into all of the tone numbers so that Manual symbol ☐ will be displayed in the LED Display.

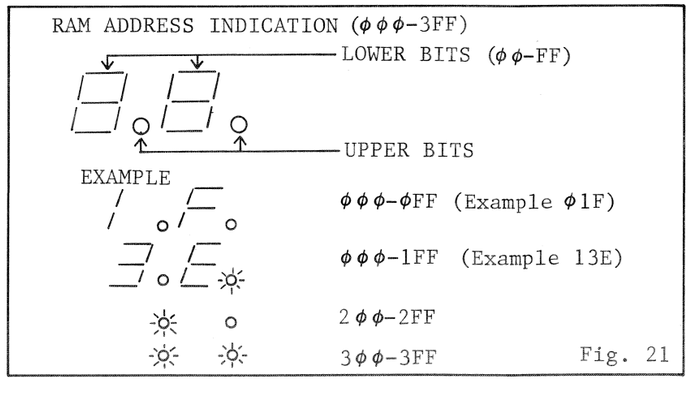
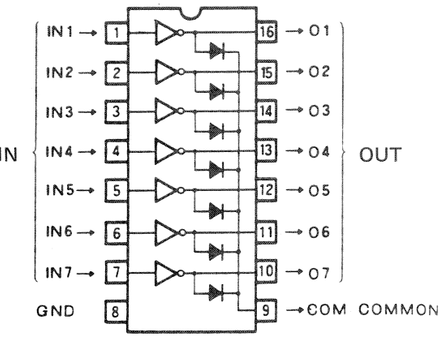


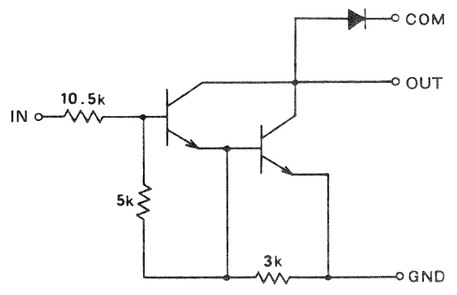
Fig. 21

M54528P
7-Segment Driver

Pin Connection



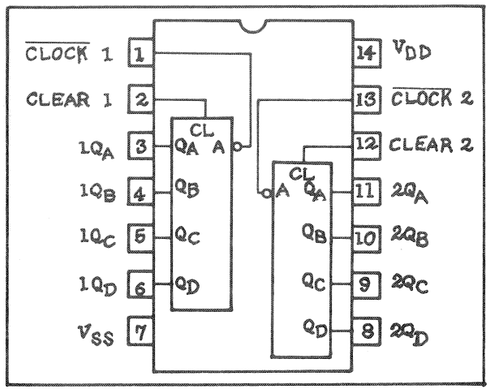
Circuit Diagram



COM and GND are common for 7 circuits.

TC40H393P
Dual 4-bit Binary Counter

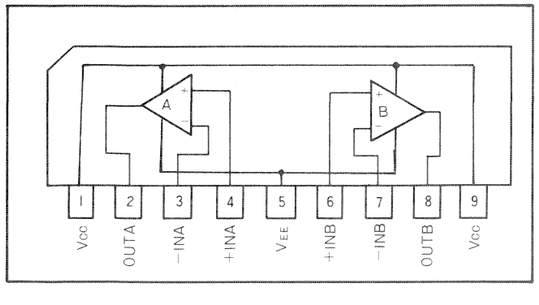
Pin Connection



COUNT SEQUENCE

COUNT	OUTPUT			
	Q_A	Q_B	Q_C	Q_D
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

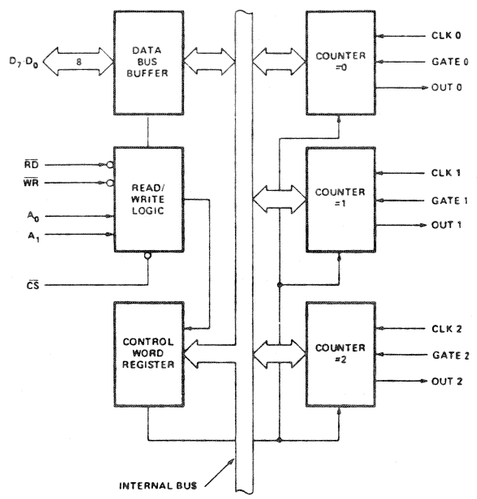
TA75558S
TA75559S
OP-Amp

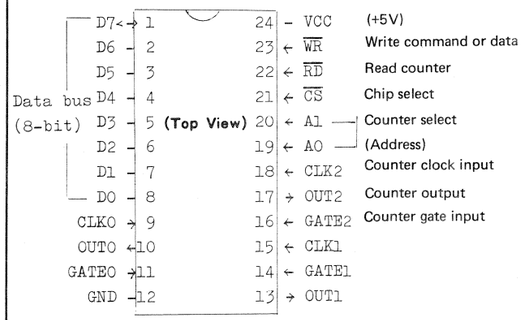


μPD8253C-5 or MSL8253P-5

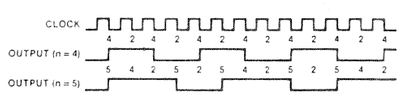
Triple Programmable Interval Timers

BLOCK DIAGRAM





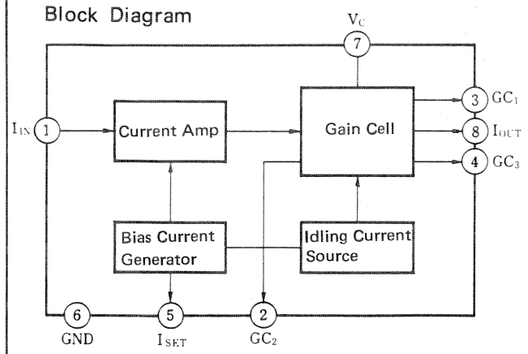
MODE 3: Square Wave Generator



μPC1252H2

Bipolar Analog Integrated Circuit

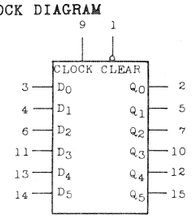
Block Diagram



TC40174BP

Hex D-Type Flip-Flop

BLOCK DIAGRAM



V_{DD} : 16, V_{SS} : 8

TRUTH TABLE

INPUTS			OUTPUT
CLOCK	D_n	$\overline{CLEAR}$	Q_n
↑	H	H	H
↑	L	H	L
↓	※	H	Q_n•
※	※	L	L

△ : Level change

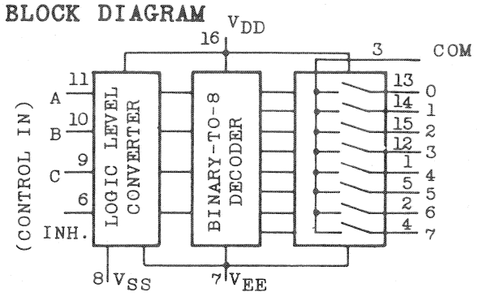
• : No change

※ : Don't care

TC4051BP

Single 8-Channel Multiplexer/Demultiplexer

BLOCK DIAGRAM



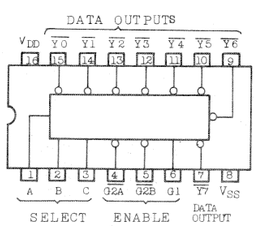
TRUTH TABLE

CONTROL INPUTS				"ON" CHANNEL
INHIBIT	C	B	A	TC4051BP
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	※	※	※	NONE

※ Don't Care Except TC4052BP

TC40H138P

3-To-8 Line Decoder/Demultiplexer



INPUTS						OUTPUTS							
ENABLE			SELECT										
G1	$\overline{G2A}$	$\overline{G2B}$	A	B	C	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
L	※	※	※	※	※	H	H	H	H	H	H	H	H
※	H	※	※	※	※	H	H	H	H	H	H	H	H
※	※	H	※	※	※	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	H	L	L	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	L	H	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

※ : Don't care

ADJUSTMENT SUMMARY

IMPORTANT:

* Use an oscilloscope unless otherwise specified.

* Before starting the adjustment procedures, check the power supply voltages.

* These adjustment procedures assume that the JUNO-60 has not yet been adjusted at all. When adjusting a particular section, be sure to confirm that the adjustments for previous sections which may affect the present section adjustment results have been completed. For example, for the VCF adjustments, if the waveform is to be checked at either the VCA OUTPUT or the OUTPUT jack, then the VCA adjustments must have been completed.
  Table 5 below shows interrelated adjustments and those adjustments which must be performed when IC(s) or related parts of the circuit are modified.

Circuit (Stage)	Adjustment Items	
CPU BOARD		
MASTER OSCILLATOR	2-1	BIAS
	2-2	TUNE
	3	BENDER
WAVEFORM	4	SAWTOOTH
	9	PWM
PANEL BOARD A		
LFO (IC11/IC14)	7	LFO
	8-6/8-7	VCF LFO
KCV (IC24)	8-3/8-4	KYBD
ENV (IC23)	8-8/8-9	VCF ENV
VCF CV MIX (IC20)	8-2	FREQ
DCO LFO (IC13)	7-2	GAIN
	7-3	OFFSET
VCF LFO (IC21)	8-6/8-7	VCF LFO
VCF	8-1/8-2/8-5	VCF (Affected channel only.)

Table 5

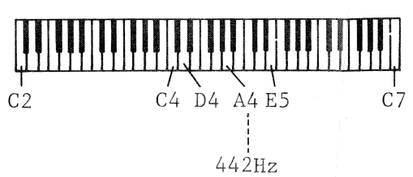


Fig. 22 Key Designation

TEST PROGRAM

For easier adjustment, the two CPUs in the JUNO-60 store the Test Programs. The JUNO-60 ADJUSTMENT PROCEDURES basically use these Test Programs. However, if no Test Mode (or Patch Number) is specified for a particular adjustment, the adjustment is to be performed manually.

TEST MODES

1. Key Assign (CPU BOARD)

To enter the Test Mode, hold the KEY TRANSPOSE button down, turn the Power ON, then continue holding the KEY TRANSPOSE button down for 2 seconds. The 3 Key Assign Modes can be selected through the ARPEGGIO MODE selector.

UP (UNISON): Six voices are assigned to the same key simultaneously.

UP & DOWN (ROTARY): The CPU assigns channels (voices) in a cyclic order (i.e., 1, 2, ... 6, 1, etc.) to the keys (or repeatedly-struck single key) being played (legato or staccato) and remembers the last channel even after the key(s) is released. New assignment will start with the next channel. Note that the first key does not always activate CH1.

DOWN (NON-ROTARY): If a second key is pressed while one key is pressed, CH2 is activated. If any preceding keys are open, the channel with the smallest number takes priority for the next assignment. For example, if any 4 keys are pressed, (activating CH1-CH4), then 3 keys released (including the first key), and one key again pressed, CH1 will again be activated.

To escape the Test Mode, turn the Power OFF and wait 3 seconds before turning the POWER ON again.

Note: There are 2 adjustment methods; (1) using test point TP4, etc., and (2) listening to a sound(s) through the OUTPUT jack. Also, CH2-CH4 can be adjusted by listening to the beat sound between channels. Perform these audible adjustments in the NON-ROTARY Key Assign Mode by setting ARPEGGIO to DOWN. For example, in order to produce sounds at CH1-CH4, sequentially hold keys 1 through 4, and release keys 2 and 3. (Fig. 23) If HOLD button remains ON, an extraneous sound will be heard. Turn HOLD button OFF as necessary.

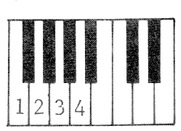


Fig. 23

2. Patch Number (PANEL BOARD B)

Insert a bare plug into the PATCH SHIFT jack in order to open the Jack Circuit. The CPU on the Panel Board B then enters the Test Mode, displaying a meaningless "11" in the Patch Number Display window. As a result, the Panel Setting Programs used for the adjustments, which are stored in BANKs 8 and 9, can be read. To call BANK 8, hold BANK button 5 down and press 3.

Note: The Patch Number does not have to be set unless otherwise specified.

Edit Mode

In the Test Mode, once a Patch Number is selected, the visual panel setting has no relation to the sound being reproduced. However, some panel controls may need resetting for editing purposes, since the same Patch Number may be used as the basic setting for several adjustments. For example, when a control is to be set to "1" and the control is already in position "1", it may actually be set to "3" by the CPU. In this case, move the control until the 2 dots in the Patch Number Display window light up, then return the control to "1".

Caution: Before performing adjustment, check to see if the Edit Mark is displayed in the Patch Number Display window. If the Edit Mark is displayed, select any other number, then again select the desired Patch Number.

NUMBER	NAME	TRANSP	LFO			DCO								HPF	VCF						VCA		ENV				CHORUS
			RATE	DELY	MODE	LFO	PWM	MODE	PULS ⊓	SAWT ◿	SUBO	SLUBEL	NOIS		FREQ	RESO	POLA	ENV	LFO	KYBD	E/G	LEVL	A	D	S	R	
81	B-1	N	6.5	0	A	0	0	M	ON			0	0	1	10	0	N	0	0	10	E	5	0	0	10	0	0
82	B-2	N	6.5	0	A	0	0	M	ON			0	0	1	10	0	N	0	0	10	E	10	0	0	10	0	0
83	VCA	N	6.5	0	A	0	0	M				0	0	1	10	0	N	0	0	10	E	10	0	0	0	0	0
84	VCF	N	6.5	0	A	0	0	M				0	0	1	3	10	N	0	0	0	E	10	0	0	10	0	0
85	PWM	N	2	0	A	0	10	M	ON			0	0	1	10	0	N	0	0	10	E	10	0	0	10	0	0
86	LFO1	N	6.5	0	M	10	0	M	ON			0	0	1	10	0	N	0	0	10	G	10	0	0	10	0	0
87	LFO2	N	6.5	0	M	0	0	M				0	0	1	3.5	10	N	0	10	0	E	10	0	0	10	0	0
88	ENV	N	6.5	0	A	0	0	M	ON			0	0	1	10	0	N	0	0	10	E	10	10	0	0	0	0
91	VCFH	D	6.5	0	A	0	0	M				0	0	1	10	10	N	0	0	10	E	10	0	0	10	0	0
92	VCFL	N	6.5	0	A	0	0	M				0	0	1	0	10	N	0	0	10	E	10	0	0	10	0	0
93	VCFE	N	6.5	0	A	0	0	M				0	0	1	0	10	N	10	0	0	E	10	0	0	10	0	0
94	VCFE	N	6.5	0	A	0	0	M				0	0	1	10	10	R	10	0	0	E	10	0	0	10	0	0
95	DCO	N	2	0	A	10	0	M	ON			0	0	1	10	0	N	0	0	10	E	10	0	0	10	0	0
96	D-A	N			A			M	ON					1			N				E						0
97	OOH	–	0	10	A	0	0	L				0	0	1	0	0	N	0	0	0	G	0	0	0	0	0	0
98	OFFH	D	10	0	M	10	10	–	ON	ON	ON	10	10	3	10	10	R	10	10	10	E	10	10	10	10	10	3

Table 6 Panel Control Settings by Test Program

ADJUSTMENT PROCEDURES

1. POWER SUPPLY VOLTAGE (POWER SUPPLY BOARD)

Use a digital voltmeter with a resolution of millivolt.

(1) Adjust VR1 for +15V ± 10mV at "a".
(2) Check the voltage at "b". It should be −14.5V to −15.5V.
(3) Check the voltage at "c". It should be +4.5V to +5.5V.
Refer to Fig. 24.

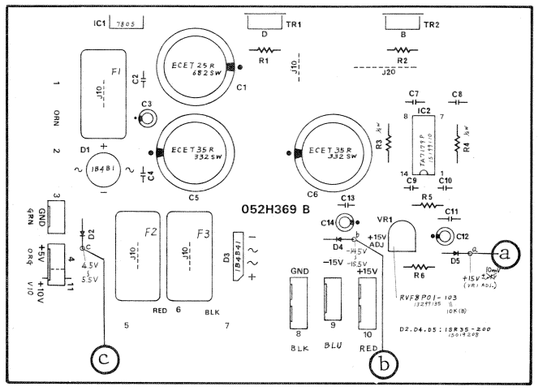


Fig. 24

2. MASTER OSCILLATOR (CPU BOARD)

2-1. BIAS

Test Point: TP2

(1) Connect digital voltmeter to TP2.
(2) Adjust VR39 for +7.70V.

2-2. TUNE

Test Point: OUTPUT
Patch Number: 82
Test Mode: UP
Control: TUNE (REAR PANEL) = center

(1) Connect Tuner, strobe, or other suitable equipment to OUTPUT jack.
(2) Hold down A4 key and adjust L1 for 442Hz using a nonferrous tool.

3. BENDER (BENDER BOARD)

Test Point: OUTPUT
Patch Number: 82

Note: Check to see if Edit Mark is ON. If so, select another Patch Number and again select "82" (see "Patch Number" section).

Test Mode: UP
Control: DCO (BENDER PANEL) = 10

(1) Connect proper tuning system to OUTPUT.
(2) Press HOLD.
(3) Press E5 key. Hold BENDER lever in leftmost position and adjust −ADJ VR1 for 442Hz. Press HOLD to release.
(4) Press HOLD again. Press D4 key.
(5) With BENDER lever in rightmost position, adjust +ADJ VR2 for 442Hz.

4. SAWTOOTH (CPU BOARD)

Test Point: CH1 TP3 (Rightmost TP3 on CPU BOARD)
Patch Number: 82
Test Mode: UP
Controls: HOLD = ON
OCTAVE TRANSPOSE = DOWN

Note: If OCTAVE TRANSPOSE is already in DOWN, reset it to NORMAL or UP, then to DOWN. This is for editing (see "Edit Mode" section).

(1) Press C2 key and adjust VR38 for 12Vp-p.
(2) Press C7 key and adjust VR37 for 12Vp-p.
(3) Press other key(s), and confirm 12V ± 1Vp-p.

Note: Reset OCTAVE TRANSPOSE to NORMAL for the remaining adjustments.

Caution: This adjustment will affect item 9, the PWM ADJUSTMENTS.

5. VCA (CPU BOARD)

5-1. GAIN

Test Point: TP4 pins 1–6 (CH1–CH6)
Patch Number: 82
Test Mode: UP
Control: HOLD = ON

(1) Connect oscilloscope to TP4 pin 1 (CH1).
(2) Press C4 key and adjust VCA GAIN VR4 of CH1 for 4Vp-p.
(3) Repeat steps (1) and (2) for TP4 pins 2–6 (CH2–CH6).

5-2. OFFSET

Test Point: TP4 pins1–6 (CH1–CH6)
Patch Number: 83
Test Mode: UP

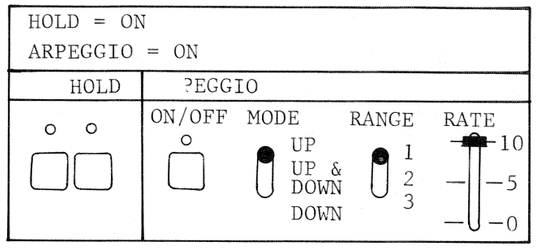


Fig. 25

(1) Connect oscilloscope (with V gain at maximum) to TP4 pin 1 (CH1).
(2) While pressing any two keys, adjust OFFSET VR5 of CH1 so that the pulses are minimized. (Fig. 26)
(3) Repeat steps (1) and (2) for TP4 pins 2–6 (CH2–CH6).

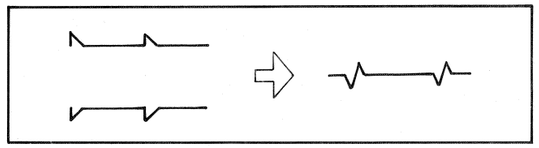


Fig. 26

(4) Press HOLD and ARPEGGIO OFF.

6. NOISE (CPU BOARD/PANEL BOARD A)

Caution: While adjusting PANEL BOARD A, use a screwdriver with a short shank to avoid short-circuiting to the heat sink of the POWER SUPPLY BOARD.

Test Point: TP4 (CPU BOARD)
Patch Number: 82
Controls: NOISE = 10
⊓⊔ (PWM) = OFF

While pressing any key, adjust NOISE LEVEL VR14 (PANEL BOARD A) for 4Vp-p. (Fig. 27)

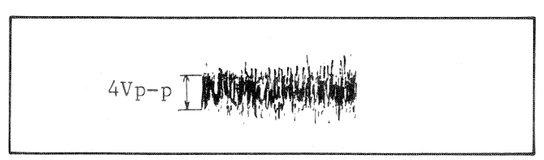


Fig. 27

7. LFO (PANEL BOARD A)

Preset the following controls for LFO adjustments unless otherwise specified.

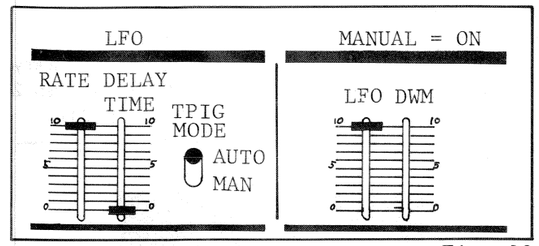


Fig. 28

Test Point: TP19 (PANEL BOARD A), Terminal 36 (PANEL BOARD A) or Terminal 20 (BENDER BOARD)

7-1. RATE

(1) Set oscilloscope to 10ms/cm, 2V/cm.
(2) Adjust LFO RATE VR1 for 45ms. (Fig. 29)

7-2. GAIN

(1) Set oscilloscope to 10ms/cm, 2V/cm.
(2) Adjust DCO LFO GAIN VR2 for 14Vp-p. (Fig. 29)

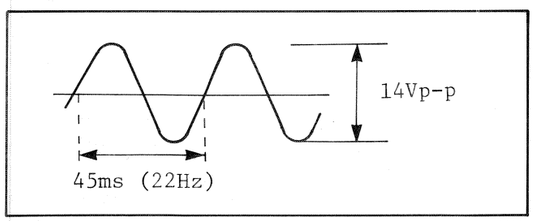


Fig. 29

7-3. OFFSET

(1) Set oscillocope V gain at maximum.
(2) Set TRIG MODE to MAN (Manual).
(3) Adjust DCO LFO OFFSET VR3 so that the horizontal line rests on the GND potential. (Fig. 30)

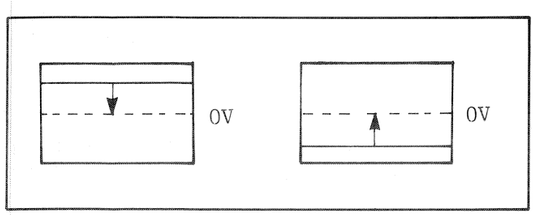


Fig. 30

7-4. DELAY

Note: HOLD must be OFF.

(1) Reset TRIG MODE to AUTO. Set DELAY TIME to "10".
(2) Set oscilloscope to 2V/cm, 0.5s/cm.
(3) Adjust DELAY TIME VR4 so that when a key is pressed, the waveform disappears, then 2 seconds later, begins to reappear. (Fig. 31)

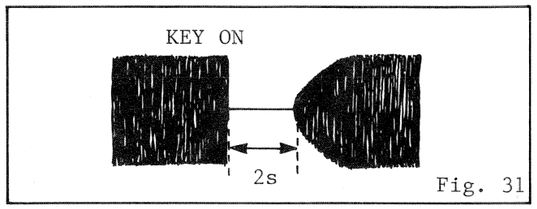


Fig. 31

8. VCF (CPU BOARD/PANEL BOARD A)

Note: VCA adjustments must have been completed.

Caution: Items 8-1 through 8-5 must be adjusted in sequence.

8-1. RESONANCE

Test Point: TP4 pins 1–6 (CH1–CH6) (CPU BOARD)
Patch Number: 84
Test Mode: UP

(1) Connect oscilloscope to TP4 pin 1 (CH1).
(2) Press any key and adjust RES VR1 (CPU BOARD) for 4Vp-p. (Fig. 32)
(3) Repeat steps (1) and (2) for TP4 pins 2–6 (CH2–CH6).

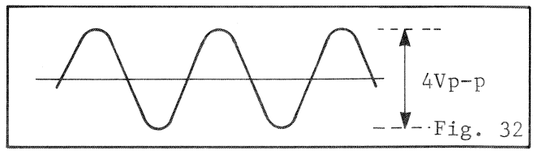


Fig. 32

8-2. FREQUENCY

Test Point: TP4 pins 1–6 (CH1–CH6) (CPU BOARD)
Patch Number: 84
Test Mode: UP

Note: FREQ VR2 of CH1 (CPU BOARD) should not be set too close to FCW or FCCW position.

(1) Connect either Tuner or frequency counter to TP4 pin 1 (CH1).
(2) Press any key and adjust 248Hz ADJ VR5 (PANEL BOARD A) for 248Hz (=B3 note).
(3) Repeat steps (1) and (2) for TP4 pins 2–6 (CH2–CH6) reading 248Hz ADJ VR5 as FREQ VR2 of CH2–CH6 (CPU BOARD).

8-3. KYBD OFFSET

Patch Number: 84
Test Mode: UP

Note: Either method (I) or (II) can be used as desired.

(I) Test Point: TP4

(1) Connect either Tuner or frequency counter to TP4 pin 1 (CH1).
(2) Press C4 key.
(3) Set KYBD to "10" and adjust KYBD OFFSET VR11 (PANEL BOARD A) for 248Hz.

(II) Test Point: VR3 HOT (TP-VCF CV IN) (CPU BOARD)
Control: HOLD = ON

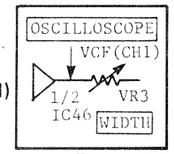


Fig. 33

(1) Press C4 key.
(2) While repeatedly moving KYBD to "10" and "0", adjust VR11 (PANEL BOARD A) so that the voltage variation is minimized.

Note: This adjustment can be made by listening to the sound from the Amp through the OUTPUT jack. Set ARPEGGIO to UP & DOWN or to DOWN. If necessary, HOLD should be turned OFF to silence the unneeded channel.

8-4. KYBD GAIN

Test Point: TP4 pin 1 (CH1) (CPU BOARD)
Patch Number: 84
Test Mode: UP
Control: KYBD = 10

Note: WIDTH VR3 of CH1 (CPU BOARD) should not be set too close to FCW or FCCW position.

(1) Connect either Tuner or frequency counter to TP4 pin 1 (CH1).
(2) Press C6 key and adjust KYBD GAIN VR10 (PANEL BOARD A) for 992Hz (B5 note).

8-5. WIDTH

Caution: Items 8-1 through 8-5 must be adjusted in sequence.

Test Point: TP4 pins 2–6 (CH2–CH6) (CPU BOARD)
Patch Number: 84
Test Mode: UP
Control: KYBD = 10

(1) Connect either Tuner or frequency counter to TP4 pin 2 (CH2).
(2) Press C6 key and adjust WIDTH VR3 of CH2 (CPU BOARD) for 992Hz.
(3) Repeat steps (1) and (2) for TP4 pins 3–6 (CH3–CH6).

8-6. VCF LFO OFFSET

Test Point: OUTPUT
Patch Number: 87

(1) Hold any key down.
(2) Quickly slide LFO up and down and adjust VCF LFO OFFSET VR9 (PANEL BOARD A) so that the pitch does not vary.

8-7. VCF LFO GAIN

Test Point: VR3 HOT (TP-VCF CV IN) (CPU BOARD)
Patch Number: 87

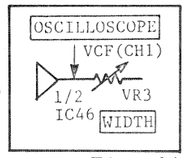


Fig. 34

With LFO TRIG pressed, adjust VCF LFO GAIN VR8 (PANEL BOARD A) for 6Vp-p.

Note: When observed at the OUTPUT jack, the frequency should vary between 40–50Hz and 4–5kHz.

8-8. VCF ENV OFFSET

Test Point: OUTPUT or TP4 (CPU BOARD)
Patch Number: 84
Controls: VCA ENV/GATE = GATE
ENVS = 0
(Refer to "Edit Mode" section.)

(1) Press any key.
(2) Quickly slide ENV (VCF) up and down and adjust VCF ENV OFFSET VR13 (PANEL BOARD A) so that the frequency does not vary.

Note: When TP4 is used as the test point, adjust VR13 so that the waveform is stable, or without jitter.

8-9. VCF ENV GAIN

Test Point: TP4 pin 1 (CH1) (CPU BOARD)
Patch Number: 93

Press any key and adjust VFC ENV GAIN VR12 (PANEL BOARD A) for approx. 30kHz. (T = approx. 34μs). (Fig. 35)

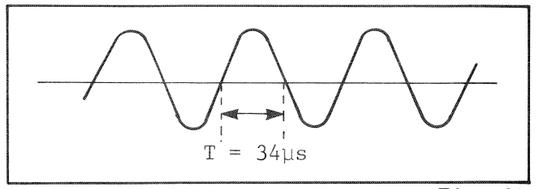


Fig. 35

9. PWM (CPU BOARD/PANEL BOARD A)

Note: Before this adjustment, the Sawtooth Adjustment must have been completed.

9-1. PWM 50%

Test Point: TP4 pins 1–6 (CH1–CH6) (CPU BOARD)
Patch Number: 82
Test Mode: UP

(1) Connect oscilloscope to TP4 pin 1 (CH1).
(2) Press C4 key and adjust PWM 50% VR6 (PANEL BOARD A) so that duty ratio of pulse is 50%. (Fig. 36)

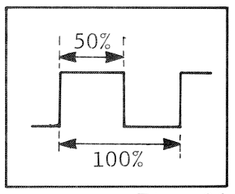


Fig. 36

(3) Connect oscilloscope to TP4 pins 2–6 (CH2–CH6), and confirm that duty ratios are 47–50%.

9-2. PWM 95%

Test Point: TP4 CH1 (CPU BOARD)
Patch Number: 85

(1) Connect oscilloscope to TP4 pin 1 (CH1).
(2) Press C4 key and adjust PWM 95% VR7 (PANEL BOARD A) so that duty ratio is 95%. (Fig. 37)

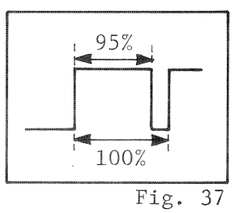


Fig. 37

10. ENVELOPE (CPU BOARD)

Test Points: TP6 pin 1 and TP7
Patch Number: 88
Test Mode: UP

(1) Disconnect 10P- and 5P-connectors (connected to ports WR through RESET) on rightmost side of CPU BOARD.
(2) Connect oscilloscope (2V/cm, 0.5s/cm) to TP6 pin 1.
(3) Adjust ENV TIME VR6 of CH1 for 3-second attack time from pressing of key. (Fig. 38)

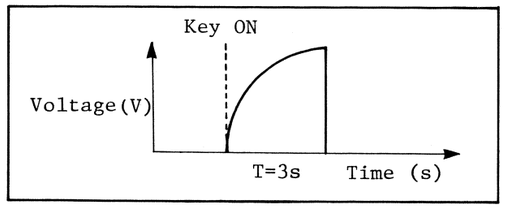


Fig. 38

(4) Reconnect oscilloscope to TP7. Reset oscilloscope time base to 50μs/cm.
(5) Holding down any key will display six growing waves on oscilloscope; CH1 being at leftmost position.
Align rise time of remaining waves to CH1 rise time (coincidental max. to 0 transitions is desired.) (Fig. 39)

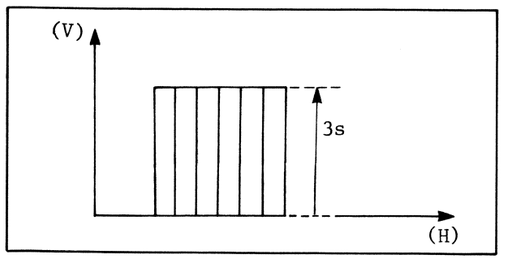


Fig. 39

(6) Check 6 sounds for synchronization in A, D, S and R phases by sweeping respective sliders.

Note: After adjustment, reconnect the connectors.

Note: CHORUS BOARD is located under BENDER BOARD.

Test Points: TP1
TP2

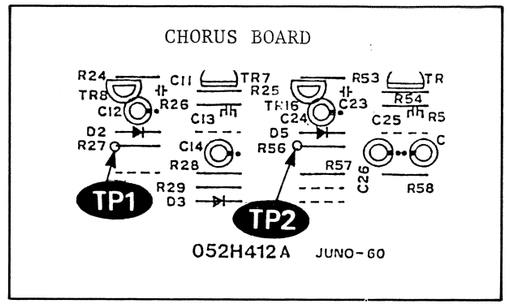


Fig. 40

Controls: MANUAL = ON
VCA LEVEL = Approx. 0
CHORUS = I

(1) Feed test signal (6Vp-p, 1kHz, SINE) to TP8 (CPU BOARD).
(2) Connect oscilloscope to TP1.
(3) Adjust BIAS VR1 (CHORUS BOARD) so that top and bottom portions of waveform are not clipped. (Fig. 41)

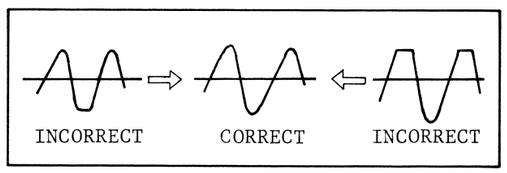


Fig. 41

(4) Reconnect oscilloscope to TP2.
(5) Adjust BIAS VR2 (CHORUS BOARD) so that top and bottom portions of waveform are not clipped. (Fig. 41)

PARTS LIST

CASES

081H261A	Cabinet	
083H052	Side panel	(right)
083H053	Side panel	(left)
072H132C	Top panel	
072H111A	Bender panel	
064H184	Holder Black	
or	(DCB connector)	
064H164	Nickel	
065H121A	LED Display window	
	Rubber foot G-5	

KNOBS, BUTTONS

22470128	Knob	(VOLUME)
016H004	Knob	(slide Pot, SW)
016H029	Button(orange)	SUT11A-1/2
016H030	Button(yellow)	SUT11A-1/2
016H036	Button(white)	SUT11A-1/2
016H037	Button(orange)	KEJ10901
016H038	Button(yellow)	KEJ10901
016H043	Button(gray)	KEJ10901
016H044	Button(white)	KEJ10901
	Key top (ivory)	KT3-2
	(See KEY SWITCH UNITS.)	

POWER SWITCH

13149108	WK2A44	
or		
14149102	1801-0121	

PUSH SWITCHES
(without button)

13129321	SUT11A-1	momentary
13129322	SUT11A-2	maintained
13169605	KEJ10901 DCO, MEMO, TAPE, CHORUS	

LEVER SWITCHES

13139136	SLE-622-18P	DPDT
13139135	SLE-623-18P	DP3T

SLIDE SWITCHES

13159332	HSW0372-01-520	MEMORY PROTECT
13159505	EVA-A03C14AGA	HPF FREQ

KEY SWITCH UNITS (LFO, TRIG)
(See p. 13 for detail.)

13129717	KEH10003	ass'y
13129714	KEH10903	switch proper
13129719	CHC32801A	guide pin
22269208	CK42602A	rubber cushion
12479703	KT3-2	key top

PCBs

149H161C	CPU BOARD (pcb 052H370C)	0PH161C
149H187C	PANEL BOARD A (pcb 052H410C)	0PH187C
149H188C	PANEL BOARD B (pcb 052H411C)	0PH188C
149H194A	LED BOARD A (pcb 052H415A)	0PH194A
149H162A	BENDER BOARD (pcb 052H371A)	0PH162A
149H189A	CHORUS BOARD (pcb 052H412A)	0PH189A
149H190A	JACK BOARD (pcb 052H413A)	0PH190A
146H094B	POWER SUPPLY BOARD (pcb 052H369B)	PSH094B 100/117V
146H095B	POWER SUPPLY BOARD (pcb 052H369B)	PSH095B 220/240V
146H092A	FUSE BOARD (pcb 052H414A)	PSH092A 100/117V
146H093A	FUSE BOARD (pcb 052H414A)	PSH093A 220/240V

JACKS

13449708	ELJ0522-01-10	(twin, mono)
13449224	HLJ2315-01-20	(stereo)

CONNECTORS

13429611	57-4014-R	DCB (connector) socket
012H026	5714S	DCB connector cap

FUSES

12559331	GGS-0.8A	pri.(100/117V)
12559511	CEE T500mA	pri.(220/240V)
12559513	CEE T1.0A	sec.(220/240V)

BENDER UNIT

029-022	PB-4 or PB-8 (compatible)	

POSISTORS

15229909	ERS-B33G561	560
15229910	ERS-B33G122	1.2k

RESISTOR ARRAYS

13829821	RGSD 8 x 103k	10k x 8
13910113	RGSD 4 x 103k	10k x 4
13910114	RGSD 4 x 223k	22k x 4
13919117	RGSD 8 x 333k	33k x 8
13919118	RK600601611 or RGSD16L104G	Ladder Network

PARTS LIST

POTENTIOMETERS

Slider

13339410	EVA-T0HC14A54	50kA
13339419	EVA-T0HC14B54	50kB
13339418	EVA-T0HC14A16	1MA
13339416	EVA-T0HC14A14	10kA

Rotary

13219759	EWJ-EJAP20B14	10kB x 2
13219401	EVH-0TAS15B14	10kB (TUNE)

Trimmer

13299134	RVF8P01-502	5kB
13299135	RVF8P01-103	10kB
13299169	RVF8P01-203	20kB
13299136	RVF8P01-503	50kB
13299137	RVF8P01-104	100kB
13299553	RVS0707V101-102M (BUL)	1kB
13299554	RVS0707V101-502M (BUL)	5kB

COIL

022A018	S167999	37μH

POWER TRANSFORMER

022H057	(100/117/220/240V)

DIODES

15019103	1S2473 or IS1555
15019243	1B4B1 (rectifier bridge)
15019245	1B4B41 (rectifier bridge)
15019249	KV1226-X or Y (varicap)
15029103	TLR-124 (LED) red
15029141	LT-8001P (LED) used as a zener
15029404 or 15029410	LN526RA (LED) display LB602VA2

ICs

IMPORTANT:
REPLACEMENTS FOR SELECTIVELY USED SEMICONDUCTORS

Some semiconductors exclusive to the JUNO-60 are selected among various equivalents, even from the same brand to meet design requirements. Correct replacement can be obtained only when these specialities are distinguished in the order sheet.

Expls:

151793050A	μPD444C-1 only (JUNO-60)
15179147	μPD8049C-380 replacement for -238 version(JUNO-60)

Also identify the model "JUNO-60" to imply the reason for ordering special semiconductors.

15179135 or 15179147	μPD8049C-238 CPU (CPU BOARD) μPD8049C-380 For replacement, use 380 version. See p. 9 for necessary modification.
15179137	μPD8049C-028 CPU (PANEL BOARD B)
15179311 or 151793050A	TC5514AP-3 1024 x 4 bit or CMOS Static RAM μPD444C-1 (selected) For replacement, use μPD444C-1
15179327	or TC5513AP-20.
15179110	μPD8253C-5 or MSL8253P-5 Triple Programmable Interval Timers
15179138	μPD8251AC or MSL8251AP Programmable Communications Interface
15159503	TC40H000P Quad 2-Input NAND Gate
15159504	TC40H002P Quad 2-Input NOR Gate
15159505	TC40H004P Hex Inverter
15159506	TC40H138P 3-to-8 Line Decoder/ Demultiplexer
15159507	TC40H273P Octal D-type Flip-Flop
15159508	TC40H373P Octal D-type Latch
15159509	TC40H393P Dual 4-bit Binary Counter
15159104H0	HD4011B Quad 2-Input NAND Gate
15159105H0	HD14013B Dual D-type Flip-Flop
15159112H0	HD14049B Hex Inverter/Buffer
15159128H0	HD14050B Hex Buffers
15159113H0	HD14051B Single 8ch Multiplexer
15159115T0	TC4066B Quad Analog Switch
15159116T0	TC4069UB Hex Inverter
15159120T0	TC4099B Quad Analog Switch
15159133T0	TC40174B Hex D-type Flip-Flop
15169117	7407 or MS307P Hex Buffers/Drivers
15169341	74LS14 Hex Schmitt Trigger Inverters
15169310	74LS42 BCD-to-Decimal Decoder
15219125	M54528P 7-Segment Driver
15189119	TL062CP OP Amp
15189118	HA17082PS/NJM082D, μPC4082C or TL082CP OP Amp
15189148	NJM072S J FET Input Dual OP Amp
15189111	NJM311D or μPC311C Voltage Comparators
15189136B0	M5218L OP Amp
15189142	TA75558S OP Amp
15189105N0	μPC4558C OP Amp
15229801	IR3109 VCF
15229807	IR3R01 ADSR
15229802	BA662A VCA
15189143	TA75559S Dual OP Amp
15219213	MN3009 BBD
020-224	MN3101 BBD Driver
15219124	μPC1252H2 (VCA)
15199106	AN7805 +5V Voltage Regulator
15199110T0	TA7179P 15V Voltage Regulator

CAPACITORS

13659223M0	ECET35R332SW	3300μF/35V
13659224M0	ECET25R682SW	6800μF/25V
13589461	ECQ-U1A473MH polypropylene	0.047μF

TRANSISTORS

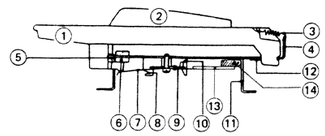
15119805	2SB834-O or Y
15129816	2SD880-O or Y
15119113	2SA1015-GR or Y or 15119124, 2SA115-GR or Y
15129117	2SC1923-O or Y or 2SC381-R
15129128	2SC752-G or O
15129114	2SC1815-GR or Y or 15129135, 2SC2603-GR or Y
15129130	2SC1583-F or G
151291080A	2SC945 SELECTED FOR NOISE
15119601	2SB605-K or L or 2SB926-S or T
15129600	2SD571-L2A
15139103	2SK30A-GR or Y (FET)
15129136	2SC2878-A or B

OTHERS

12389801	KMFC1002T 4MHz (Ceramic resonator CSA 4MHz and paired CSC300)
12389800	KMFC1005T1 6MHz (Ceramic resonator CSA 6MHz and paired CSC300)
12389807	KMFC1037T 11MHz (Ceramic resonator CSA 11MHz and paired CSC300)
12569111	CR-1/3N 3V Litium battery

KEYBOARD

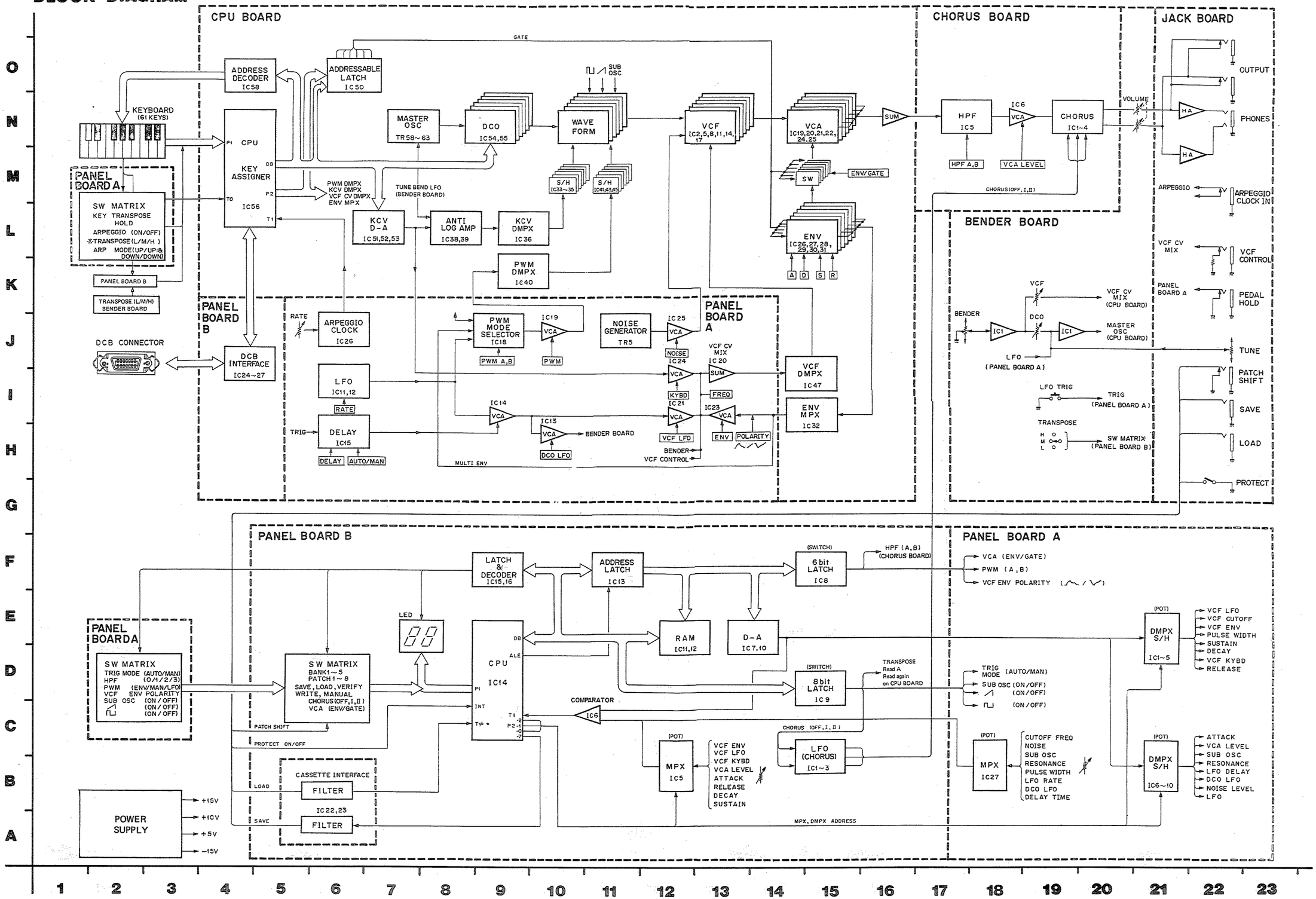
004H008	SK-361C	(61 keys)



KEYBOARD PARTS
SK-361C (004H008)

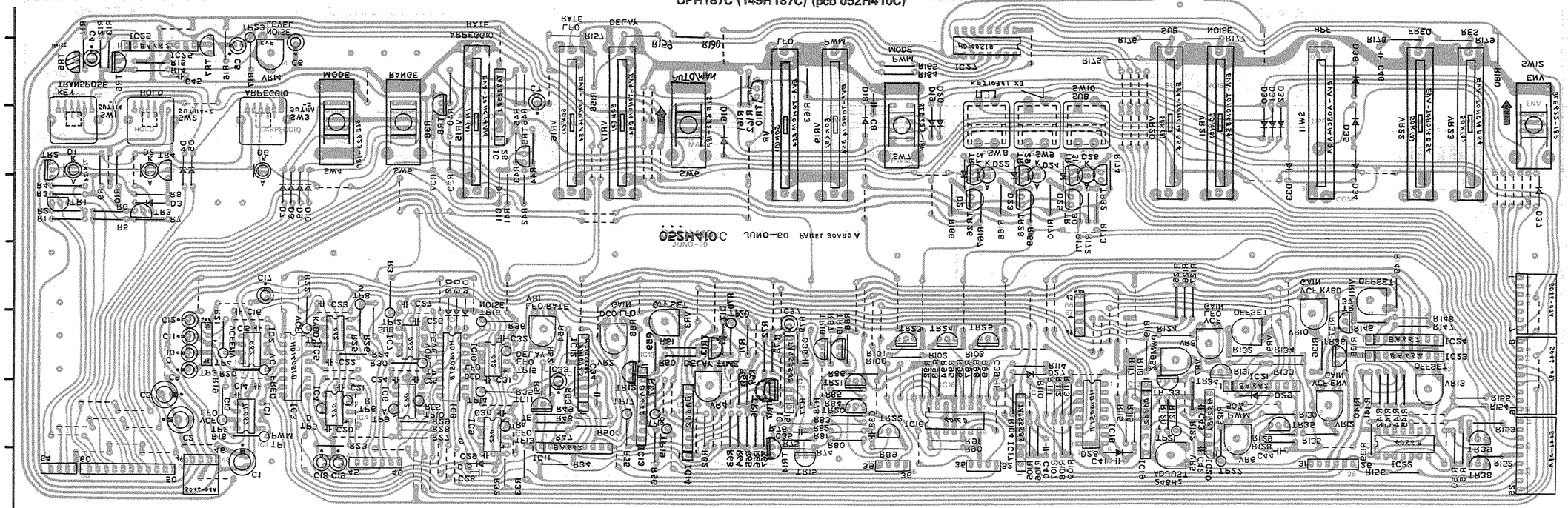
NO	PART NO	DESCRIPTION	
1	106H026	Natural key	C F
1	106H027	Natural key	D
1	106H028	Natural key	E B
1	106H029	Natural key	G
1	106H030	Natural key	A
1	106H031	Natural key	C' F'
2	106H032	Sharp key	black
3	070H029	Key spring	H29
4	061H086A	Chassis	H86A
5	068H004	Guide bushing	H4
6	101H141	Level felt	H141
7	071H044	Contact leaf	H44
8	071H051	Busbar 8P	H51
	071H054	Busbar 5P	H54
9	043H007	Switch unit 12P	H7
	043H008	Switch unit 13P	H8
10	104H029	Busbar holder	H29
11	062H024	Chassis bracket	H24
12	098H006	Key stopper	H6
13	052H283-5	Matrix board	H283-5
14	107H059	Cushion	H59

BLOCK DIAGRAM



PANEL BOARD A

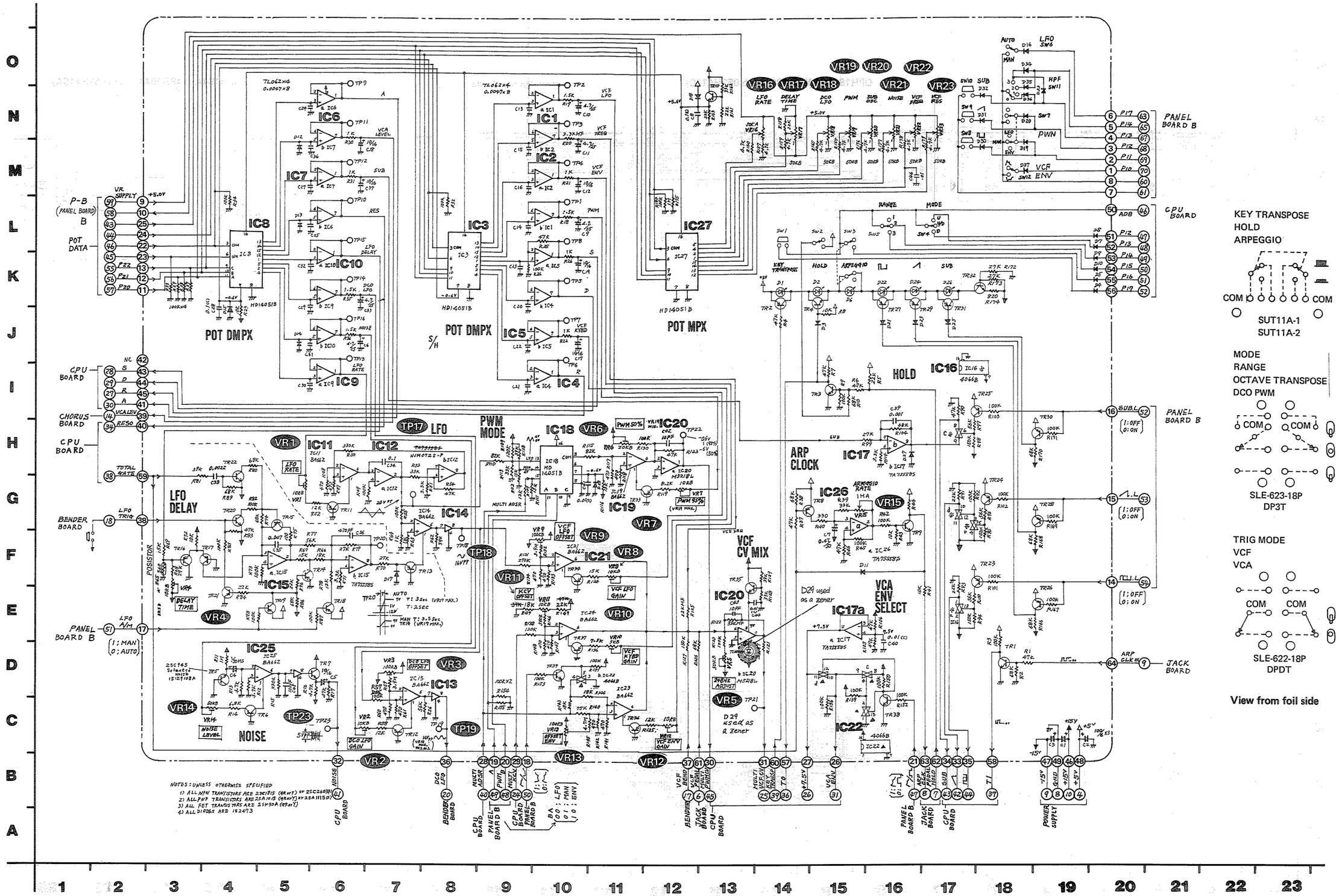
OPH187C (149H187C) (pcb 052H410C)



View from foil side

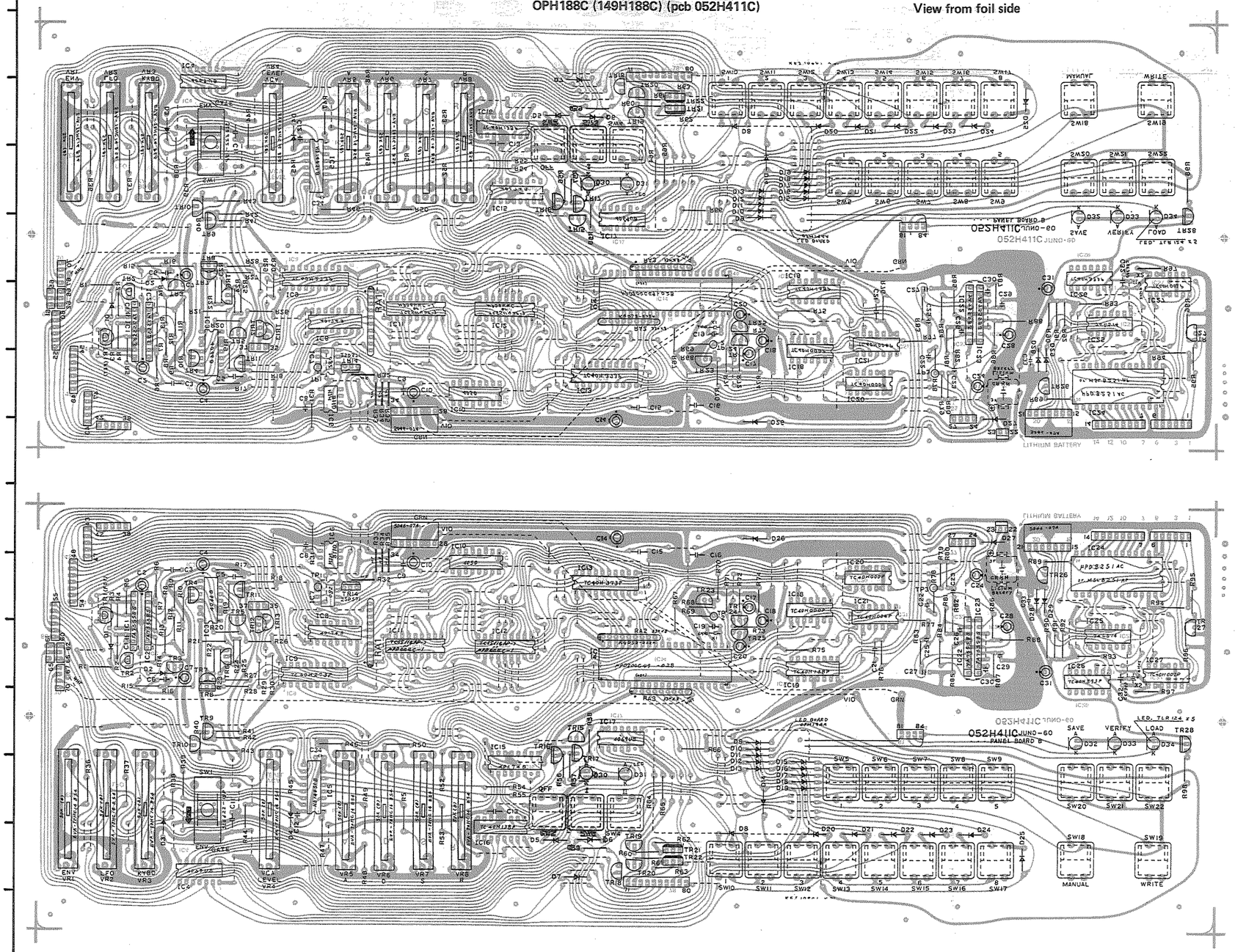
View from component side

PANEL BOARD A



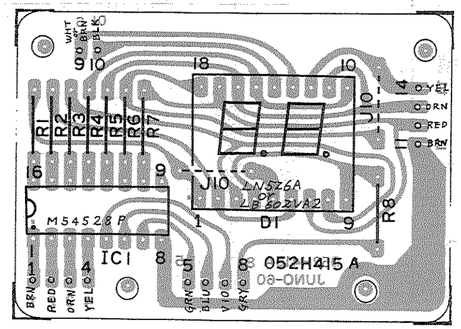
PANEL BOARD B

OPH188C (149H188C) (pcb 052H411C) View from foil side



LED BOARD

OPH194A (149H194A) (pcb 052H415A)



CHANGE INFORMATION (Panel Board B)

See circuit diagram for detail.

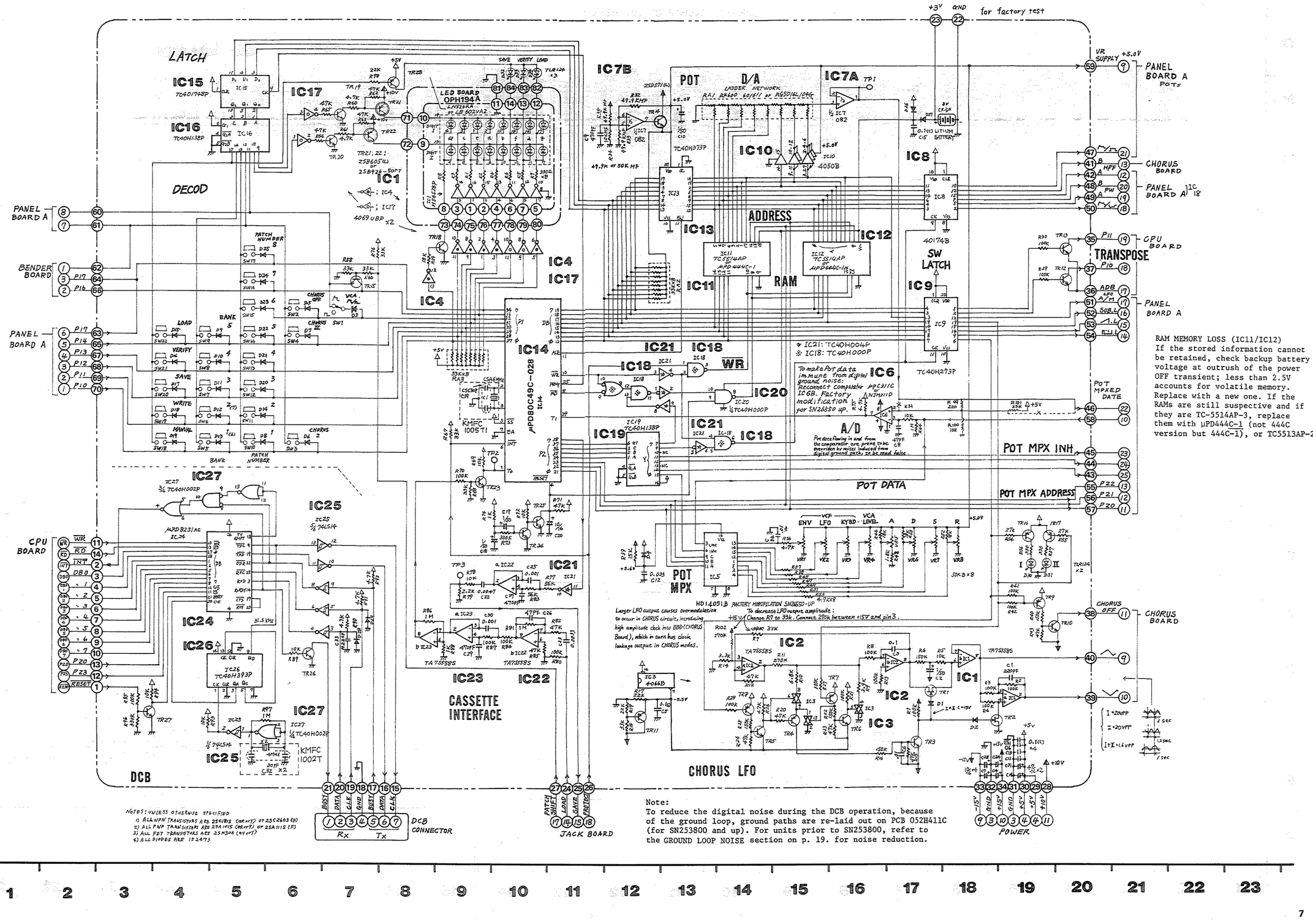
1. Pattern Re-layout (SN253800 up)
   Provide foil pattern exclusive to display signal return (terminals 81/31) on 052H411C. This additional pattern substantially relieves audio signal from noise.

2. IC6 Reconnection (SN265500 up)
   Pull up pin 2 of IC6 to guard pot data from digital noise.

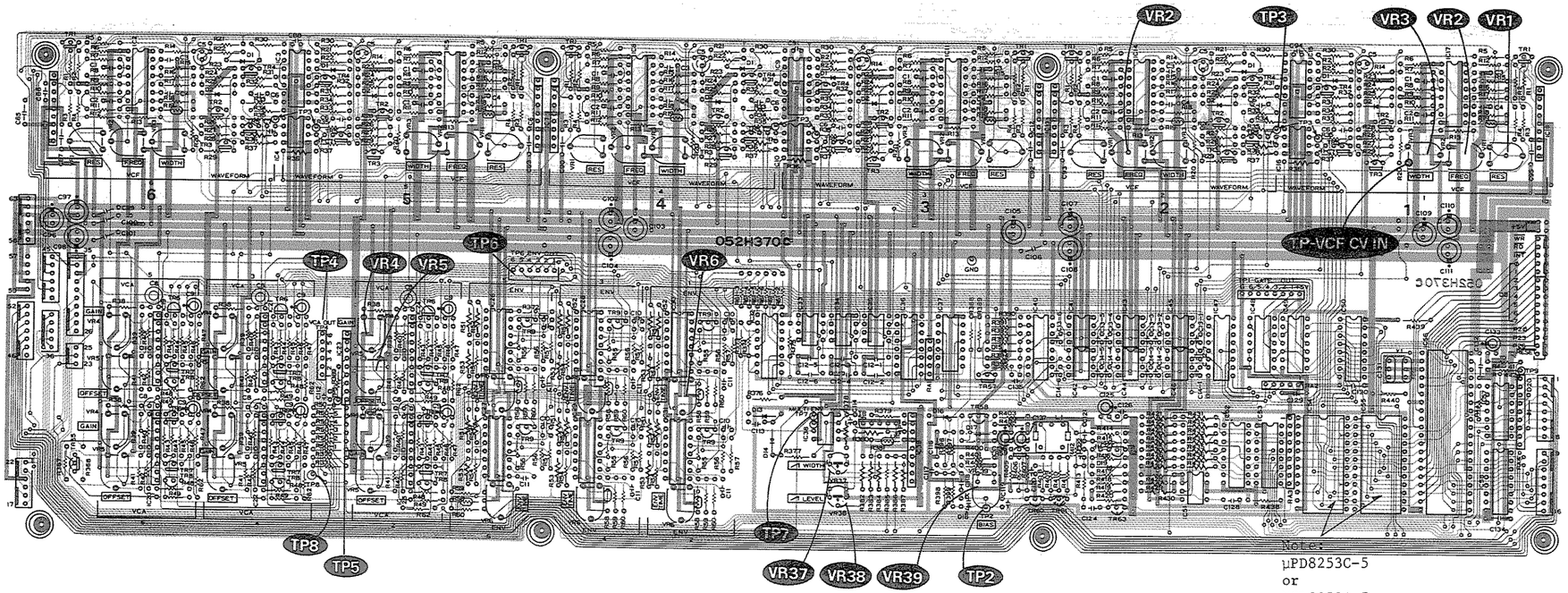
3. IC2 Reconnection (SN265500 up)
   Decrease LFO amplitude to eliminate overmodulation.

4. Change RAMs IC11 and IC12
   (SN undefined)
   From TC5514AP to TC5513AP-20 or μPD444C-1 for positive memory storage.

PANEL BOARD B

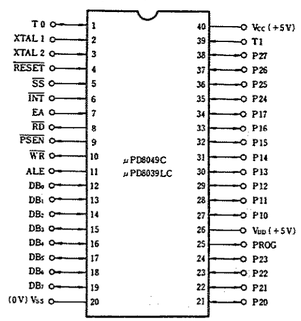


OPH161C (149H161C) (pcb 052H370C)



μPD8049C-238 or 380

(Top View)



DESIGNATION		PIN NO.	FUNCTION
DB (Data Bus)	DBφ	12	Keyboard & Function SW Scan Data Outputs ← 8253 (IC54, 55) Division Data Outputs → KCV Data Outputs (synchronized with KCV & GATE address outputs.) ⇕ GATE, Total GATE, Key TRANSPOSE LED
	1	13	
	2	14	
	3	15	
	4	16	
	5	17	
	6	18	
	7	19	
PORT 1	P1φ	27	Keyboard & Function SW Scan Data Inputs
	11	28	
	12	29	
	13	30	
	14	31	
	15	32	
	16	33	
	17	34	
PORT 2	P2φ	21	8253 (IC54, 55) Address → 4099 (IC50), 4051 (IC32, 36, 40, 47) Address Outputs
	21	22	
	22	23	
	23	24	Not in use
	24	35	– 8253 (IC55) Select Pulse Output
	25	36	– 8253 (IC54) Select Pulse Output
	26	37	Not in use
	27	38	4099 (IC50), 4051 (IC36, 40, 47) Select Pulse Output
	XTAL-1	2	Internal Clock Oscillator Inputs
	XTAL-2	3	
	RESET	4	Reset Pulse Input
	Tφ	1	GATE Hold Signal Input
	T1	39	Arpeggio Clock Input
	WR	10	8253 Write Pulse Output