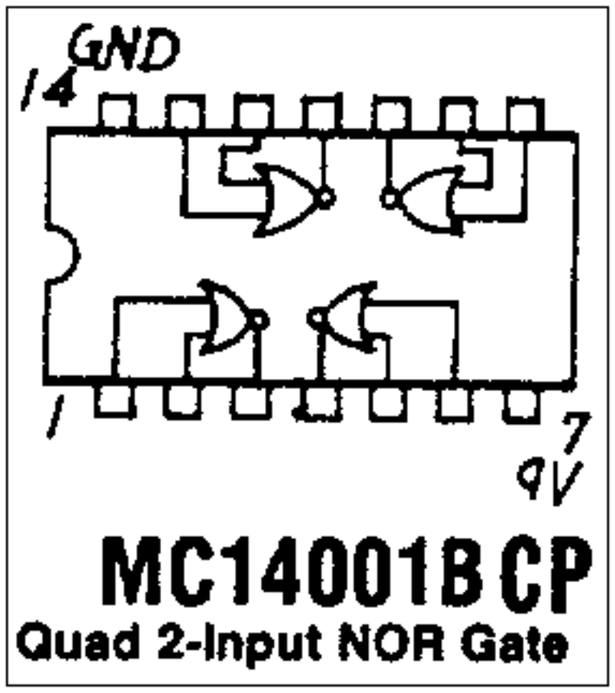
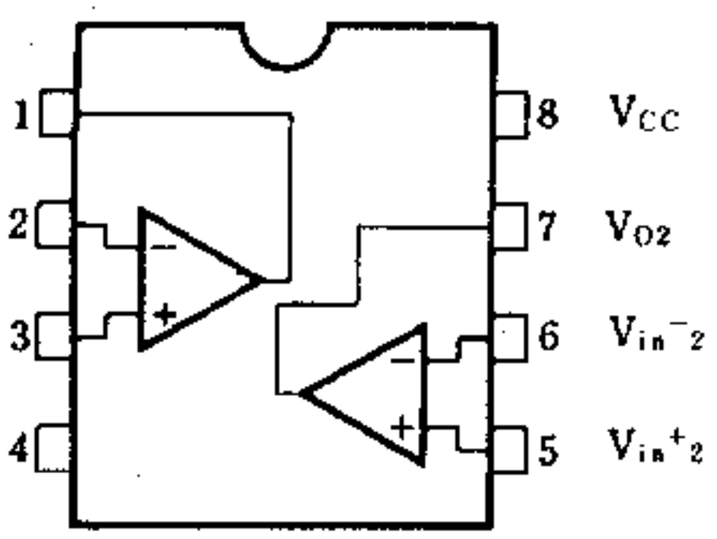


MC14001BCP

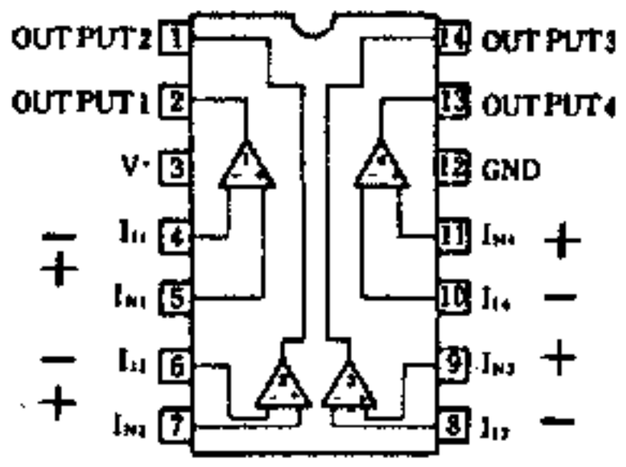
Quad 2-Input NOR Gate

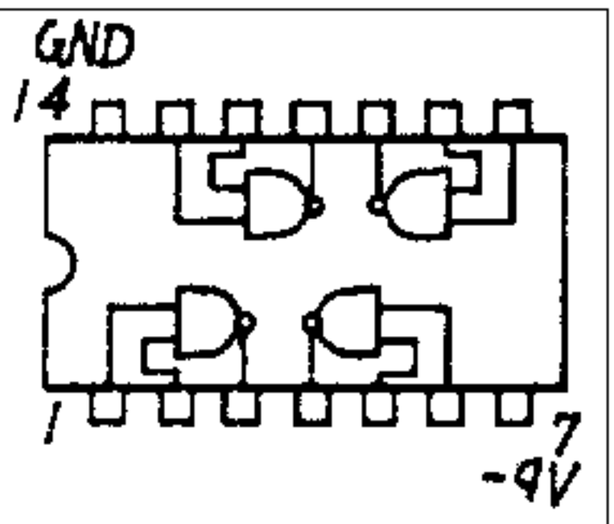
NJM2904



AN6912

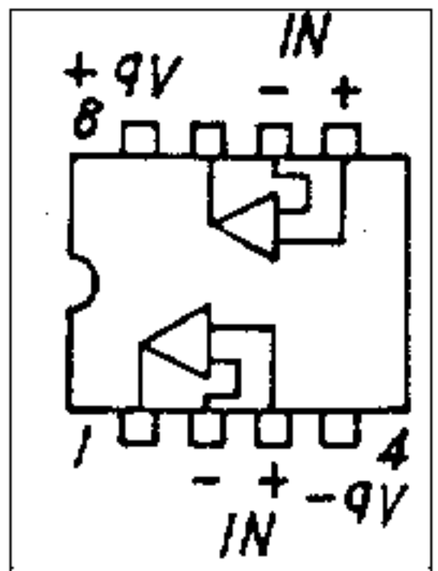
Quad Comparator





TC4011BP

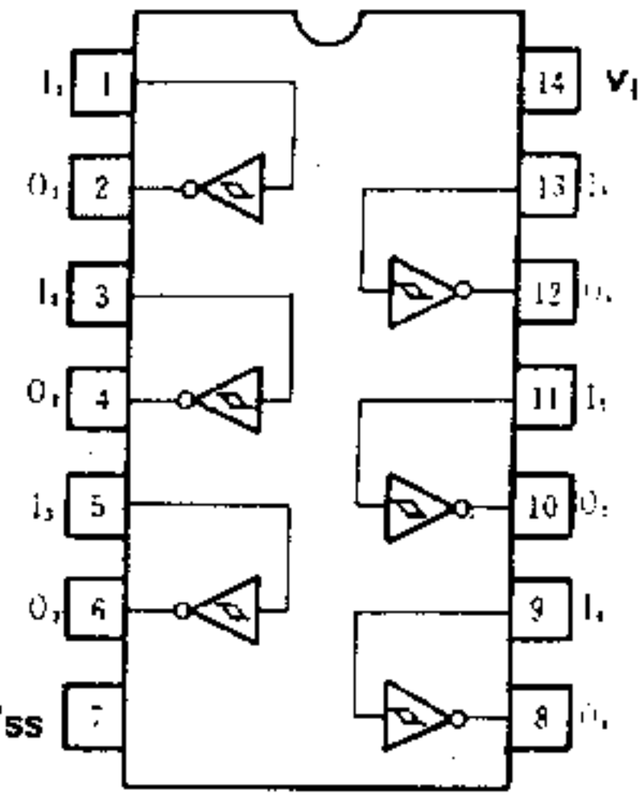
Quad 2-Input NAND Gate



μPC4558C

HD14584B

Hex Schmitt Trigger



MC14013B

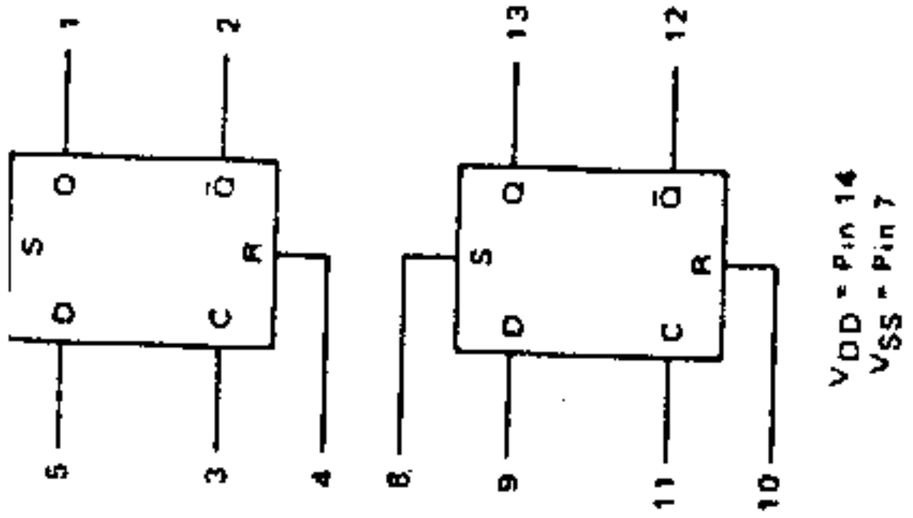
DUAL TYPE D FLIP-FLOP

TRUTH TABLE

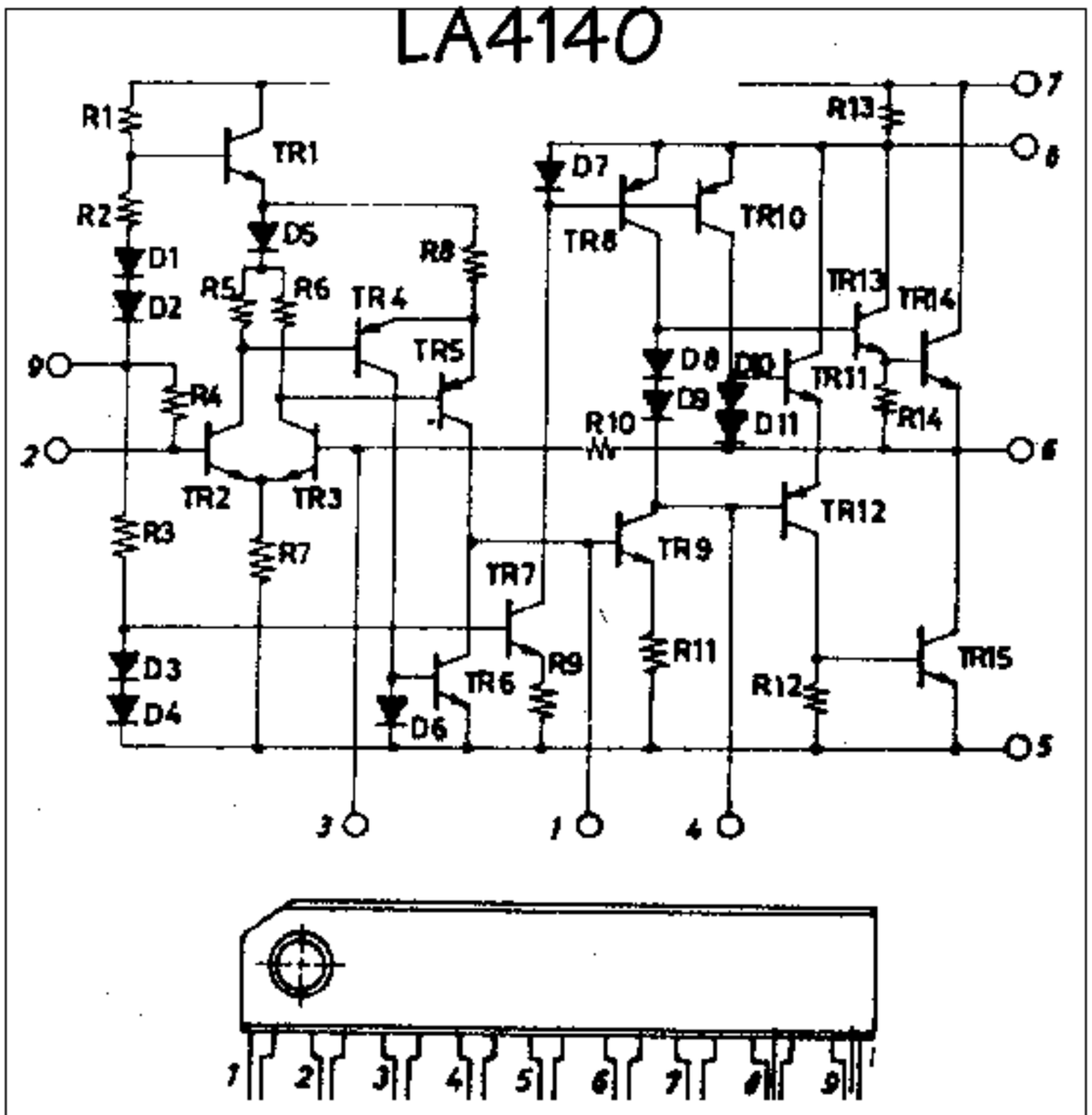
INPUTS				OUTPUTS	
CLOCK[1]	DATA	RESET	SET	Q	$\bar{Q}$
↑	0	0	0	0	1
↑	1	0	0	1	0
↓	X	0	0	Q	$\bar{Q}$
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

No Change

X = Don't Care
↑ = Level Change



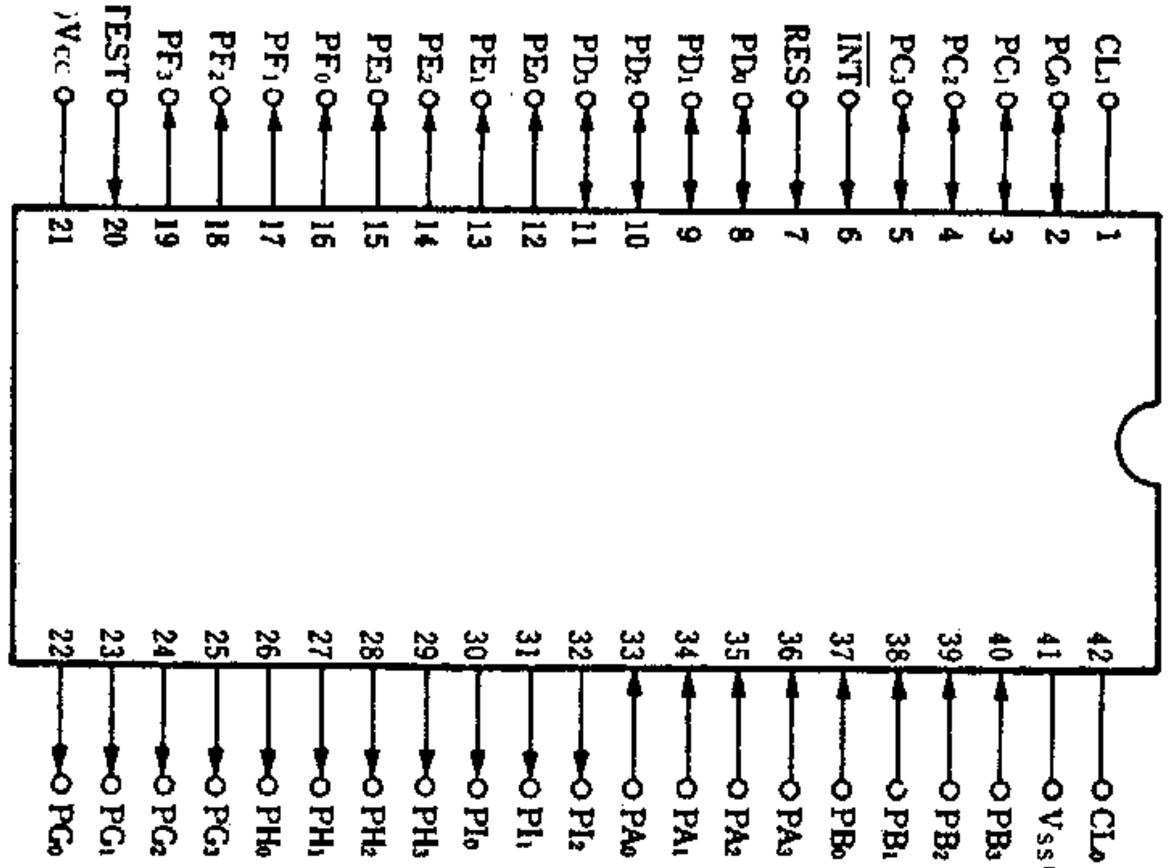
LA4140



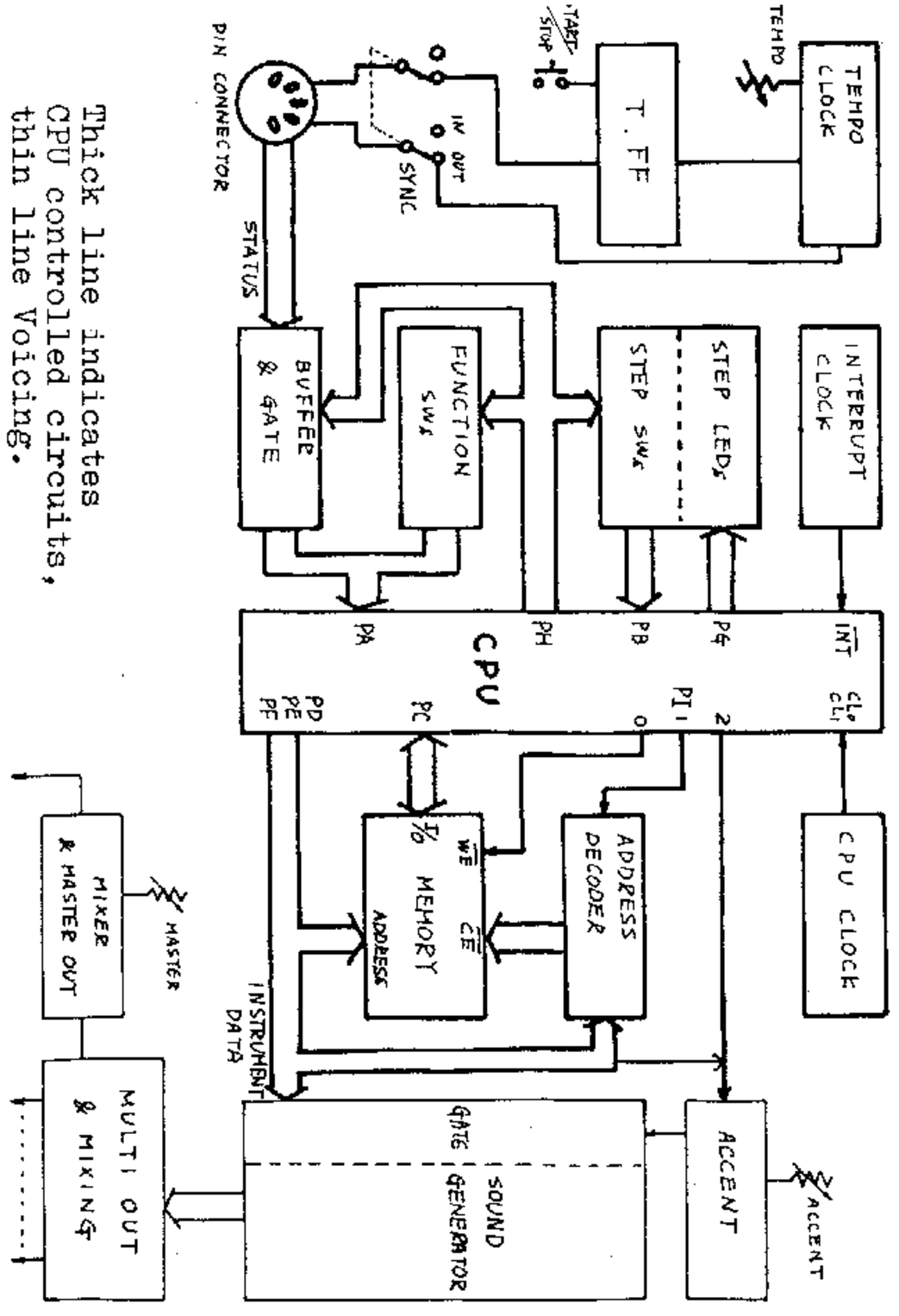
μPD650C–085 FUNCTIONAL DESCRIPTION

		No.			
PH (Port H)	0	26	Scanning signal outputs to switches Switching signal outputs to STATUS BUFFER & GATE		
	1	27			
	2	28			
	3	29			
PA (Port A)	0	33	Switch scanning signal inputs STATUS (TEMPO CLOCK. START/STOP. TAP) inputs		
	1	34			
	2	35			
	3	36			
PB (Port B)	0	37	Inputs from STEP Switches (RHYTHM SELECT Swtiches)		
	1	38			
	2	39			
	3	40			
PG (Port G)	0	22	Drive signals to STEP LEDs		
	1	23			
	2	24			
	3	25			
PE (Port E)	0	12		CH	
	1	13	I/II	OH	
	2	14	Memory bank	CY	
	3	15	select	HT	
PD (Port D)	0	8	MEMORY ADDRESSES These pins use CE from ADDRESS Decoder to select cells in RAM to be accessed		INSTRUMENT DATA These data need COMMON TRIG to trigger Sound Generators being designated
	1	9	Rhythm numbers		
	2	10			
	3	11			
PF (Port F)	0	16		LT	
	1	17	Step	SD	
	2	18	numbers	BD	
	3	19		AC	
PC (Port C)	0	2	Data Inputs/Outputs		
	1	3			
	2	4			
	3	5			
PI (Port I)	0	30	Memory WE		
	1	31	Memory CE (associated with PE-2, 3 at ADDRESS DECODER)		
	2	32	Trigger Pulse (INSTRUMENT) output		

μPD650C
(Top View)



BLOCK DIAGRAM



SUB BOARD

(PCB 291-494C)

SWITCH BOARD

(PCB 291-492C)

TEMPO
OSC
IC 1, Q 2
DFF DIVIDER IC 2a
OUTPUT Q3
IN PUT
MONO MULTI C4, R7
DFF DIVIDER IC 2b
OUTPUT Q4
INPUT
SCHMITT TRIGGER IC 1
RUN STOP
SWITCH BOARD
BOOSTER Q403 - 406
BOOSTER Q407 - L10
LED DRIVER Q401, 402
TAP
I II
BAR
CLEAR
GATE Q411
RUN STOP
TEMPO CLOCK
TAP
MODE SWITCH
SCALE
INSTR-UMENT SWITCH
TAP PULSE SHAPER Q6
STATUS BUFFER GATE IC 3 Q5,7,8
MODE, SCALE, INST. ENCODER
GND
CPU CLOCK IFT
INTER -RUPT CLOCK IC 1
C MOS MEMORY IC 7,8
MICRO PROCESSOR IC 4
AC
BD
SD
LT
HT
CY
OH
CH
BD
Q14,15
OSC IC 15 A
OSC IC 15 B
LEVEL
SD
Q18 19
Q17
ATTACK
ENV Q16
VCA Q 30
OSC IC 10 A
HPF Q 32
LEVEL
W.N.
LT
Q303 304
Q307
ATTACK
LPF Q308
VCA Q310
OSC IC 9 A
ENV Q305, 306
OSC IC 9 B
Q301 302
ATTACK Q308
HT
SUB BOARD
WHITE NOISE Q31
ACCENT Q9, 10, 11
LEVEL
COMMON TRIGGER
IC 16
OSC
OSC
OSC
OSC
OSC
OSC
Q 28, 29
BPF IC 15B
ENV Q35
VCA Q39
VCA Q38
HPF Q40
HPF IC 12B
BPF C 15A
LEVEL
CY
LED DRIVER Q413, 414
(SWITCH BOARD)
Q26 27
ENV Q36
ENVELOPE SHUT OFF Q24, 25
TEMPO CLOCK
VCA Q37
HPF IC 12A
LEVEL
ENV Q31, C42
Q21 22
OH
CH
IC 11
MONO MULTI Q34
MONO MULTI Q33
TRIG LT
TRIG HT
1.5V×4
C MOS MEMORY BACK UP
5V Q45, 46
15V MC 1020
6V Q42
POWER SUPPLY
A.C. ADAPTOR IN
MIXER IC 14A
VOLUME
IC 14B
OUTPUT
HEADPHONE AMP. IC 13
(SUB BOARD)
H.P. OUT
LEVEL

MAIN BOARD

TEMPO

VR1 1MC

TM2 100KB

(TM2 : 22 KB, R12 : 100 K) for 1~46 lot

R12 47K

Q2

D4 R13 47K C10 0.001 R22 47K

D3 R8 1M C5 1/50

IC 1 HD14584B

14 PIN : +5V
7 PIN : GND

C8 0.039

D1

TEMPO CLOCK RATE 8mS AT MAX

R4 470K C3 220P

(TP)

IC 2a HD14013BP

14 PIN : +8
7 PIN : GND

R4 470K C2 220P

C4 0.01

IC 2b

R7 1M D2

R247 SURFACE MOUNTING 3.3K 20 lot ~ 1280 lot

(R9: 82K, R10: 390K) for 1~6 lot

R9 150K TM1 100KB R71 33K

R10 150K (TP)

INT CLOCK RATE 1.8mS

D5 R11 10K C7 0.068

TI S74230

CPU CLOCK RATE 2.2µS

(TP) C26 0.01

6 INT 7 PR 21 Vcc 20

42 CL0

1 CL1

+8

+6V

SW. BOARD

D411 D415 D419 D423 D412 D416 D420 D424 D413 D417 D421 D425 D414 D418 D422 D426

R416 100 R417 100 R418 100 R419 100

Sw 8 Sw 12 Sw 16 Sw 20 Sw 9 Sw 13 Sw 17 Sw 21 Sw 10 Sw 14 Sw 18 Sw 22 Sw 11 Sw 15 Sw 19 Sw 23

C403 100/6.3

D407 10E-2 D408 10E-2 D409 10E-2 D410 10E-2

Q403 Q404 Q405 Q406 Q407 Q408 Q409 Q410

R412 3.3K R413 3.3K R414 3.3K R415 3.3K

R431 15K R432 15K R433 15K

R420 2.2K R421 2.2K R422 2.2K R423 2.2K

R407 47K R408 47K R409 47K R410 47K

D427 SW7 BAR SW5 CLEAR SW25 D402 D403

R430 15K R405 15K R406 15K

Q411 R425 10K

D404 D406 D405

TAP SW24

C401 1/50

R/S SW6 D401 R402 680 R401 47K Q401 R403 5.6K Q402 R404 1K D428

R1 47K R3 33K R2 1K C1 1/50 RUN STOP Q1

SYNC IN/OUT SW1

Q4 R14 47K R18 1K R16 22K

Q3 R15 47K R17 22K

Q6 R27 33K R29 22K R28 10K

R35 1K

MODE SW4 PRE SCALE SW2 SW3 INSTRUMENT

C H O H C > H T L S B D A C

Q13 C6 100/6.3 R23 10K

R26 15K (33K@15K for 1~14 lot, 15K - surface mounting)

R30 15K

C12 0.01 R36 22

Q5 R20 100K R21 15K R19 33K C11 0.01 R34 1M

Q7 R31 470K R30 100K R37 15K

Q8 R33 100K R32 33K R38 15K

IC 3 HD14001BP

14 PIN : +8
7 PIN : GND

D8 D9 D10 D11

33 PA0 34 1 35 2 36 3

IC 4 µPD 650 C-128

Vss 41

SYNC
IN/STOP
MD
EMPO
CLOCK
AP

IC 7 µPD444C

IC 8 µPD444C

PC0 2 1 3 2 4 3 5

R76 3.3K R77 3.3K R78 3.3K R79 3.3K

R72 R73 R74 R75 15K × 4

R83 33K

WE CE

PF3 19 2 18 1 17 0 16

R24 R25 R45 82K

Q12 R48 33K D25 R46 82K R47 47K

PE3 15 2 14 1 13 0 12

PD3 11 2 10 1 9 0 8

R82 49 81 150 47K × 4

SW. BOARD Q412 R424 10K R411 3K

IC 6 HD14011BP

P1 0 30 1 31 2 32

R70 15K

R41 47K D6 D7 D12

AC

C29 100/6.3

B D S D L T H T C Y TRIG O H C H

ACCENT

+15H

R39 4.7K Q9 R53 100 C14 47/16

VR2 10KB

R40 22K Q10 Q11 AC LEVEL

R42 33K R43 4.7K R44 4.7K

SW. BOARD D429 D430 R429 680 R428 680

Q413 R426 10K R427 47K Q414 C402 10/16

Pattern Group

MAIN BOARD

BASS DRUM

BD LEVEL

SNARE DRUM

SD LEVEL

Power Supply

Noise Generator

POWER & SW VOLUME

OUTPUT

HEADPHONE

SUB BOARD

LOW TOM

HIGH TOM

L,H TOM LEVEL

CYMBAL

CY LEVE

O,C HIHAT LEVEL

OPEN HIHAT

CLS'D HIHAT

HEADPHONE AMP. (SUB BOARD)

ALL NPN TRANSISTORS ON THE MAIN
AND THE SUB BOARD ARE 2SC9

ALL PNP TRANSISTORS ON THE MAIN
AND THE SUB BOARD ARE 2SA7

ALL NPN TRANSISTORS ON THE SW. B
ARE 2SC202

ALL PNP TRANSISTORS ON THE SW. B
ARE 2SA937

ALL DIODES ARE 1S2473

ALL OP AMP'S ARE JRC2904
IC15 μPC4558

to p.4 4-D