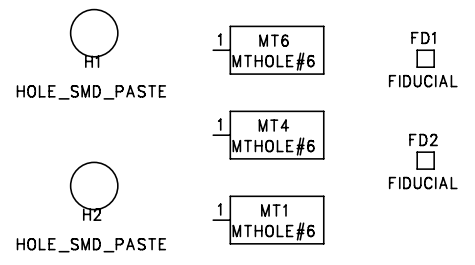
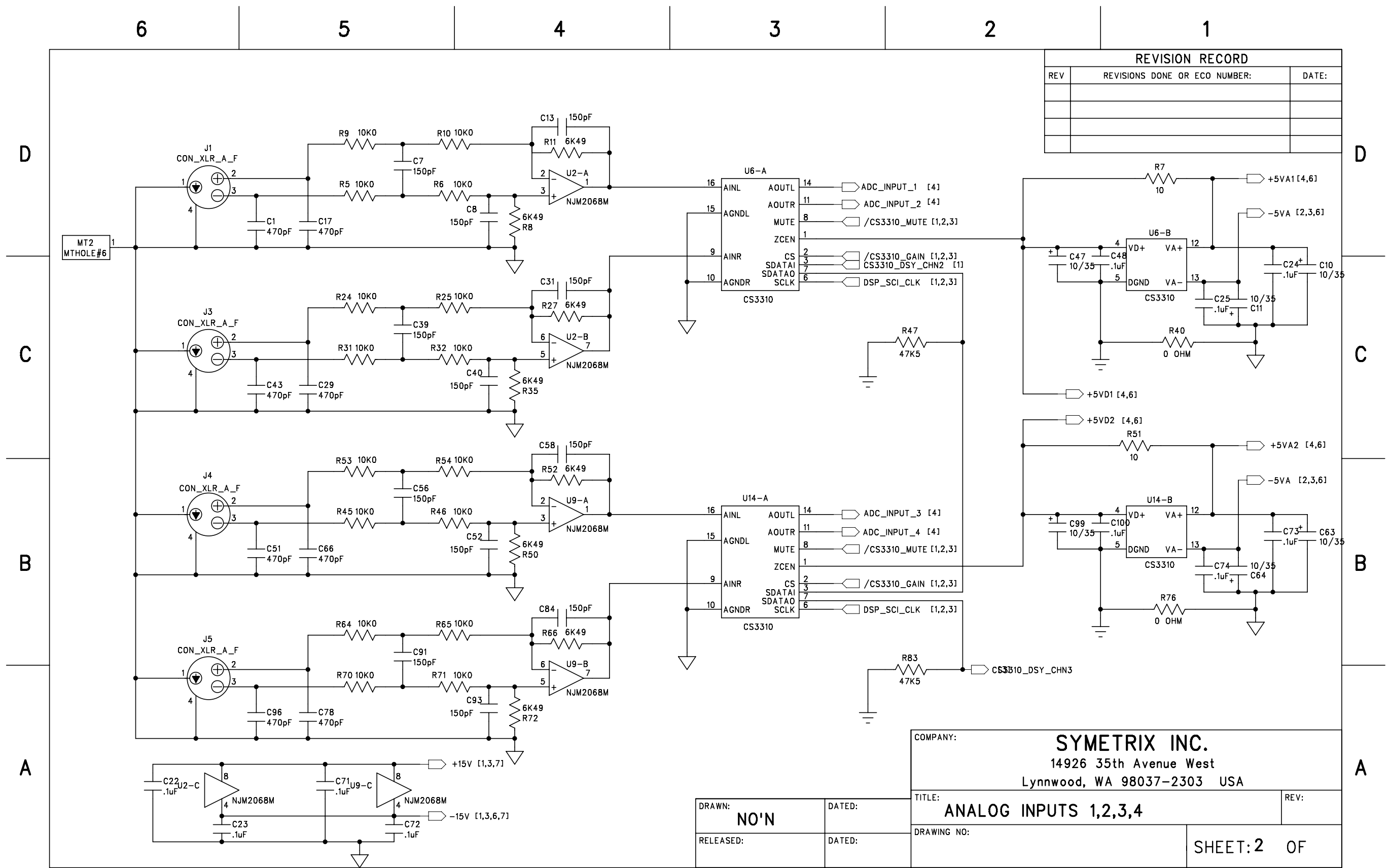


REVISION RECORD		
REV	REVISIONS DONE OR ECO NUMBER:	DATE:



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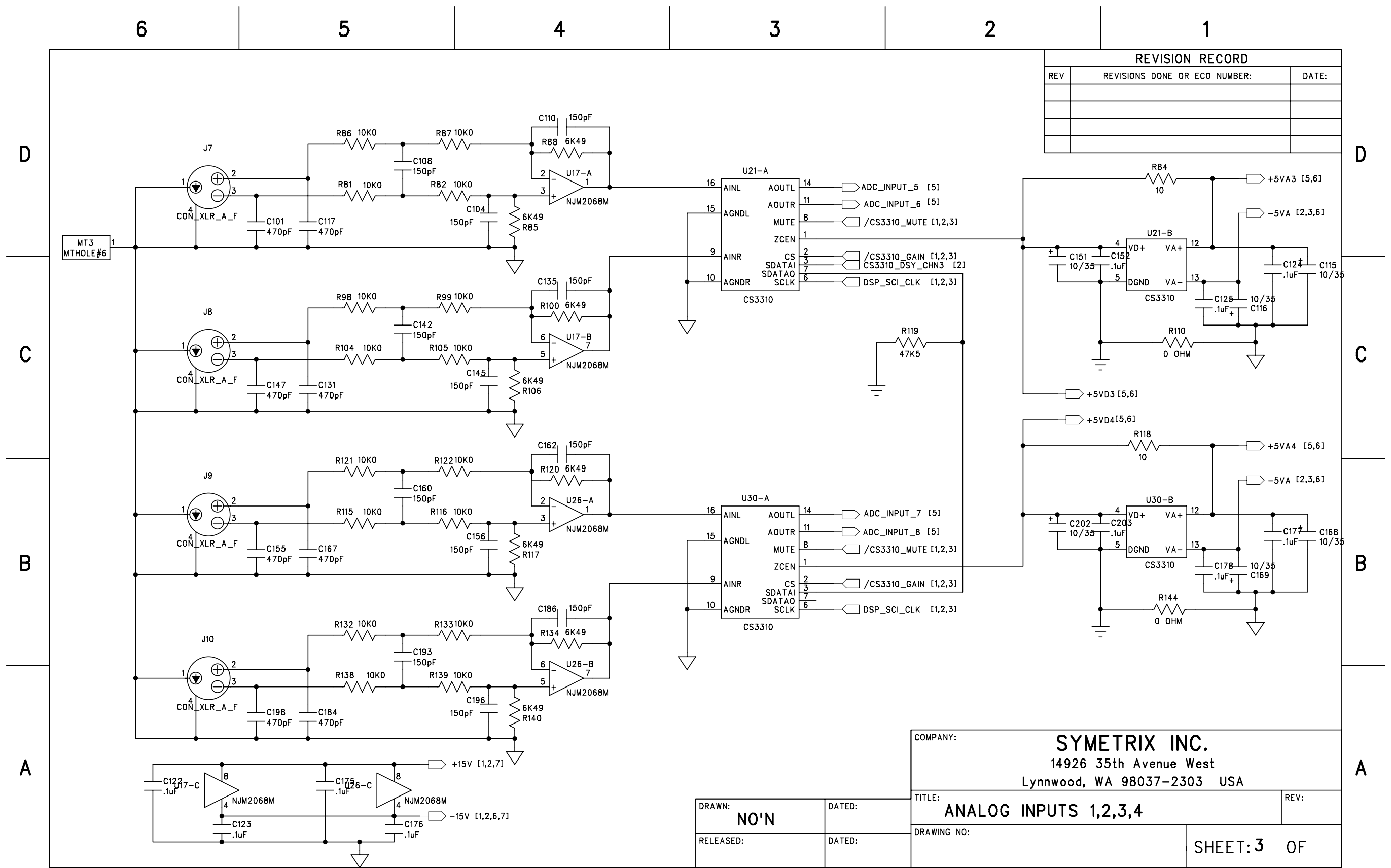
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RELEASED:	DATED:	DRAWING NO:	SHEET: 1 OF 10



REVISION RECORD		
REV	REVISIONS DONE OR ECO NUMBER:	DATE:

COMPANY: **SYMETRIX INC.**
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DRAWN: NO'N	DATED:	TITLE: ANALOG INPUTS 1,2,3,4	REV:
RELEASED:	DATED:	DRAWING NO:	SHEET: 2 OF



REVISION RECORD		
REV	REVISIONS DONE OR ECO NUMBER:	DATE:

COMPANY: **SYMETRIX INC.**
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TITLE: **ANALOG INPUTS 1,2,3,4**

REV: _____

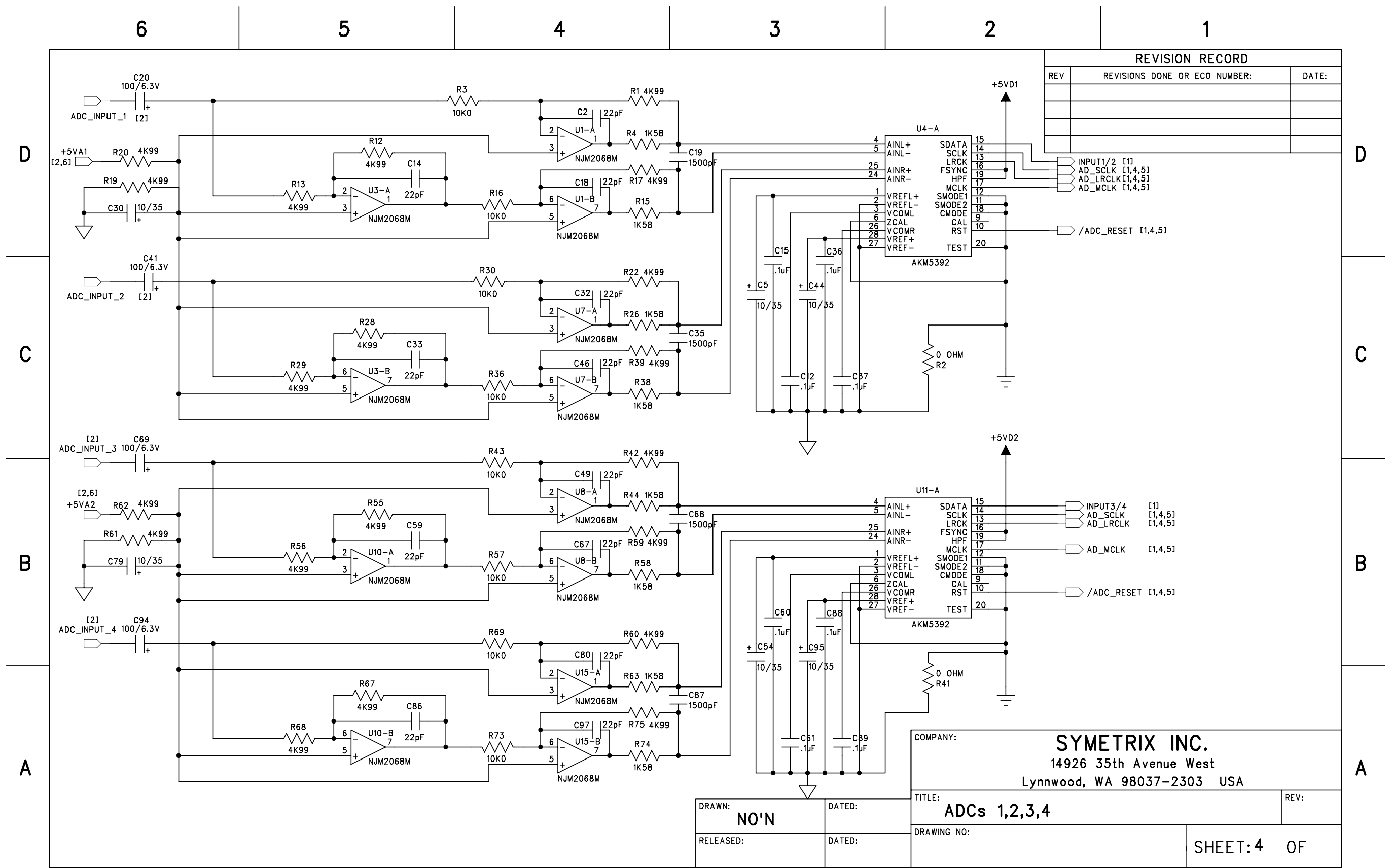
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SHEET: **3** OF _____

DRAWN: NO'N	DATED: _____
RELEASED: _____	DATED: _____

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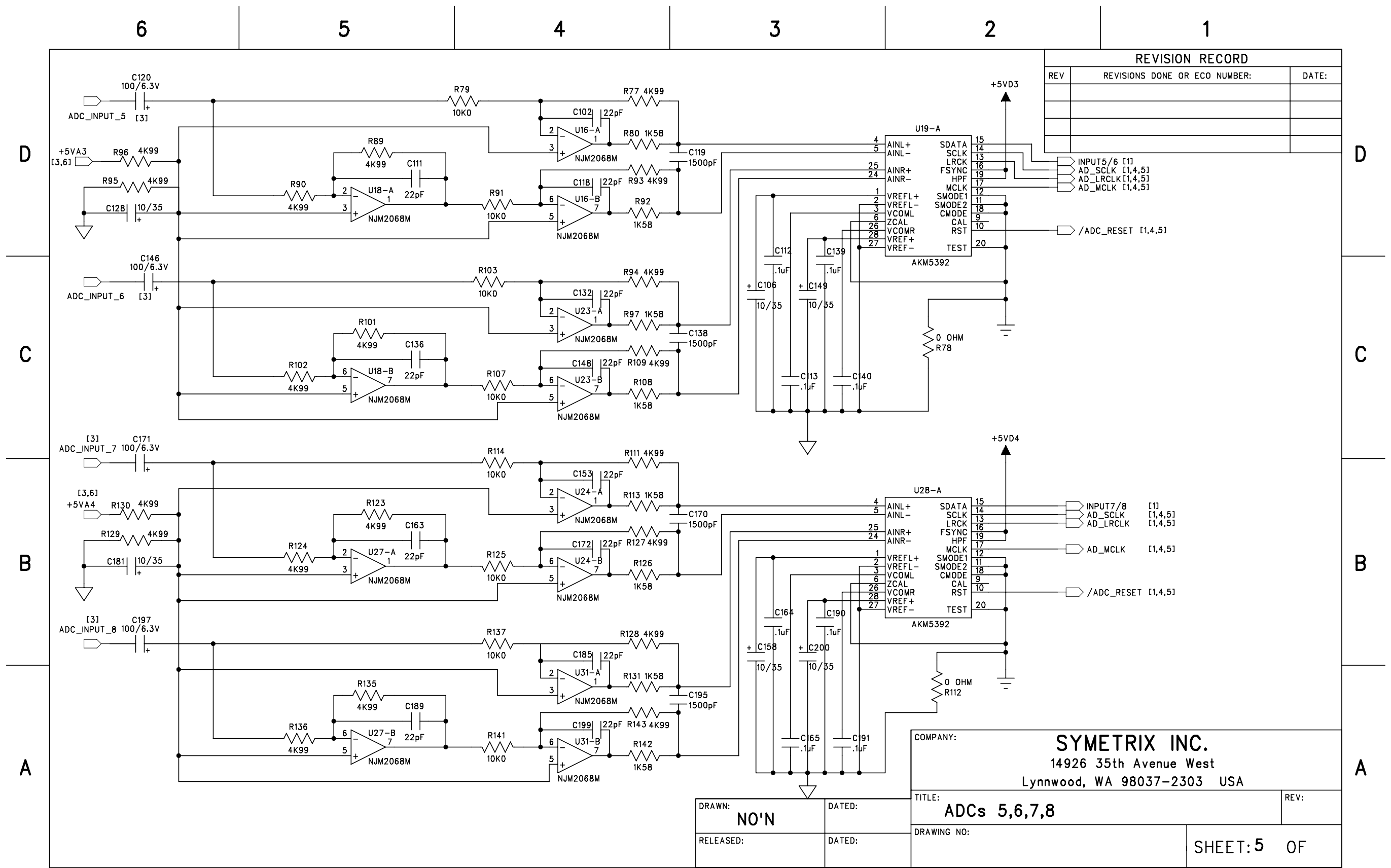
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REVISION RECORD		
REV	REVISIONS DONE OR ECO NUMBER:	DATE:

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DRAWN: NO'N	DATED:	TITLE: ADCs 1,2,3,4	REV:
RELEASED:	DATED:	DRAWING NO:	SHEET: 4 OF



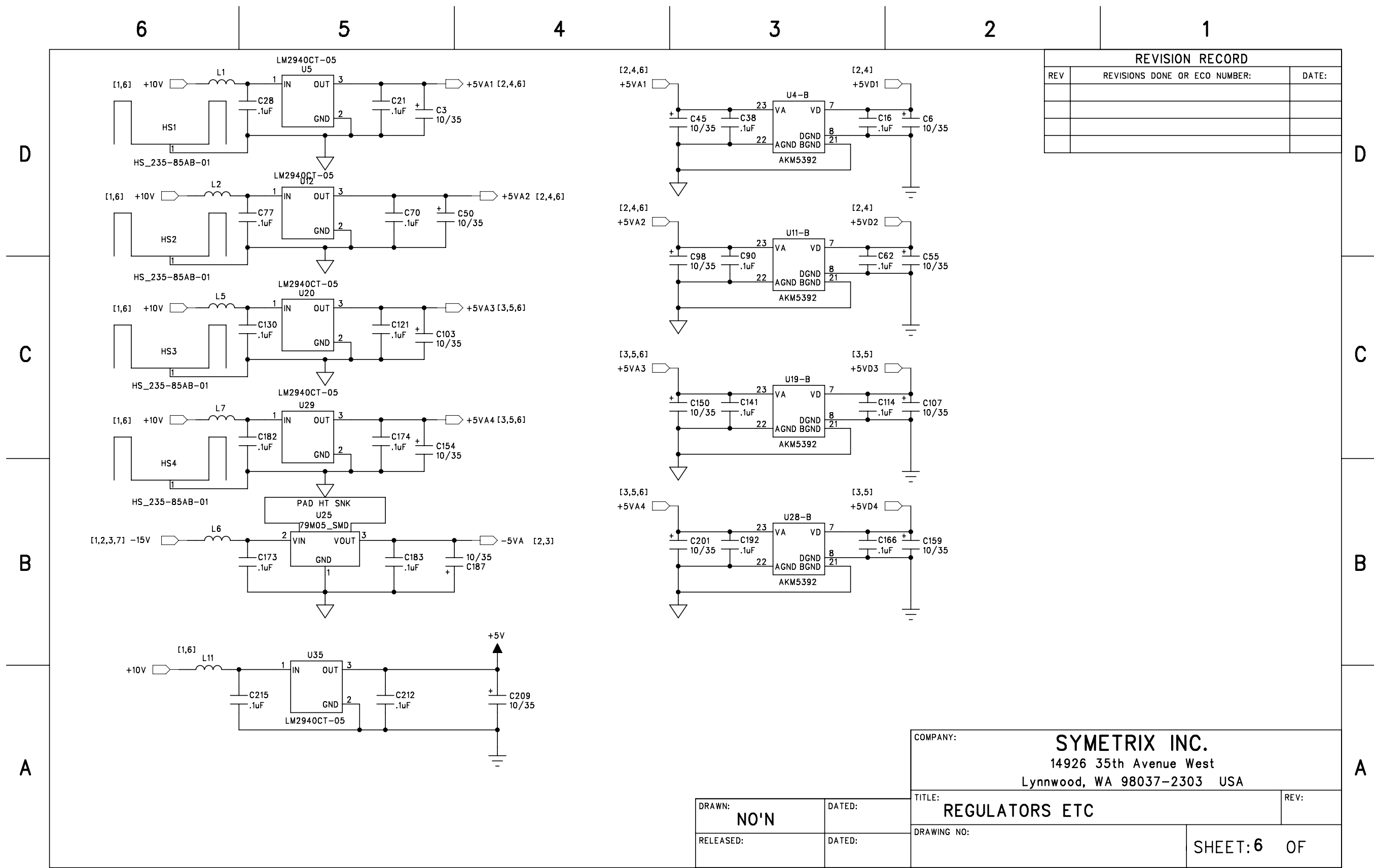
REVISION RECORD		
REV	REVISIONS DONE OR ECO NUMBER:	DATE:

15	SDATA	INPUT5/6 [1]
14	SCLK	AD_SCLK [1,4,5]
13	LRCK	AD_LRCLK [1,4,5]
16	FSYNC	
19	HPF	
17	MCLK	AD_MCLK [1,4,5]
12	SMODE1	
11	SMODE2	
18	CMODE	
9	CAL	
10	RST	/ADC_RESET [1,4,5]
20	TEST	

15	SDATA	INPUT7/8 [1]
14	SCLK	AD_SCLK [1,4,5]
13	LRCK	AD_LRCLK [1,4,5]
16	FSYNC	
19	HPF	
17	MCLK	AD_MCLK [1,4,5]
12	SMODE1	
11	SMODE2	
18	CMODE	
9	CAL	
10	RST	/ADC_RESET [1,4,5]
20	TEST	

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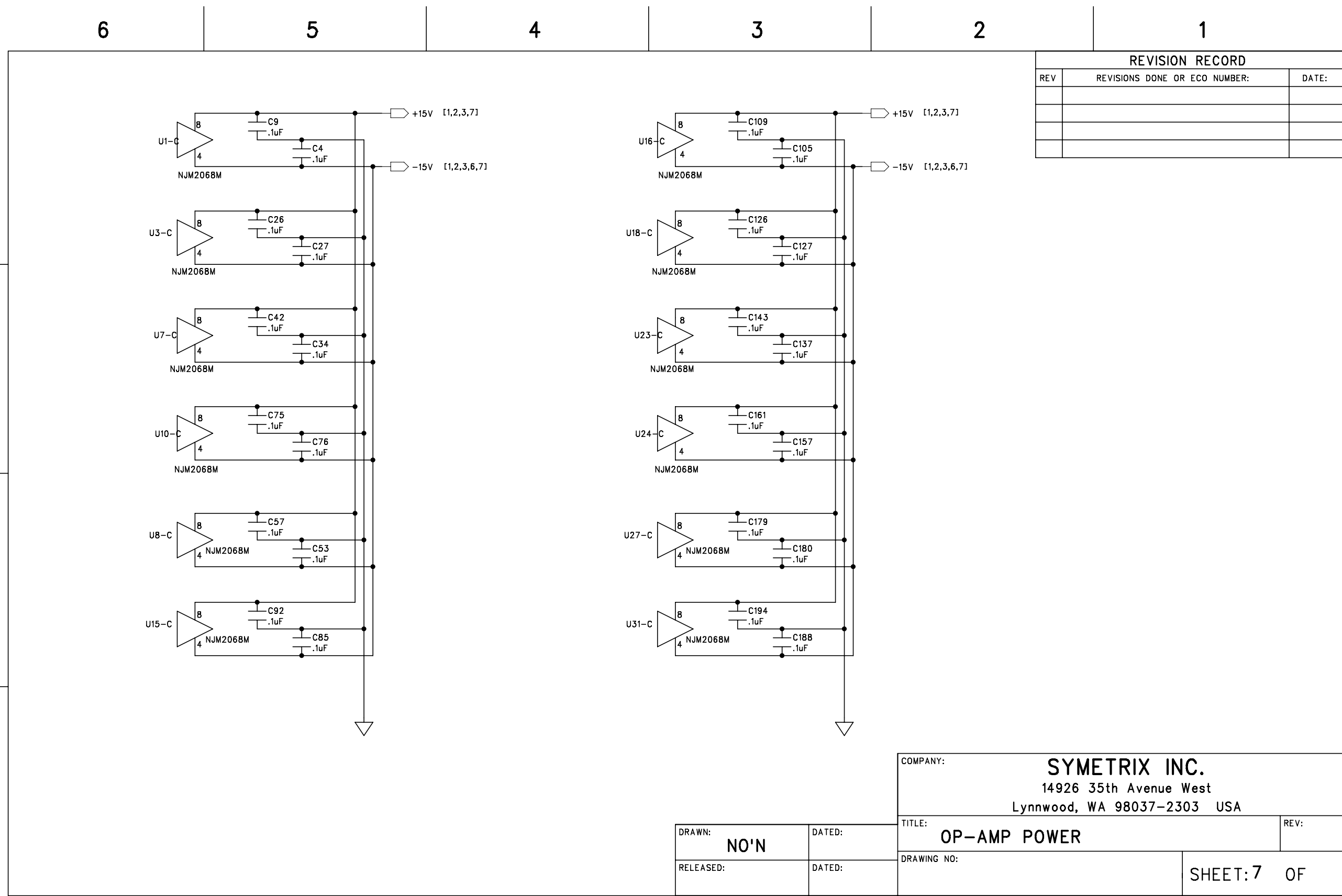
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RELEASED:	DATED:	DRAWING NO:	SHEET: 5 OF



REVISION RECORD		
REV	REVISIONS DONE OR ECO NUMBER:	DATE:

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DRAWN: NO'N	DATED:	TITLE: REGULATORS ETC	REV:
RELEASED:	DATED:	DRAWING NO:	SHEET: 6 OF



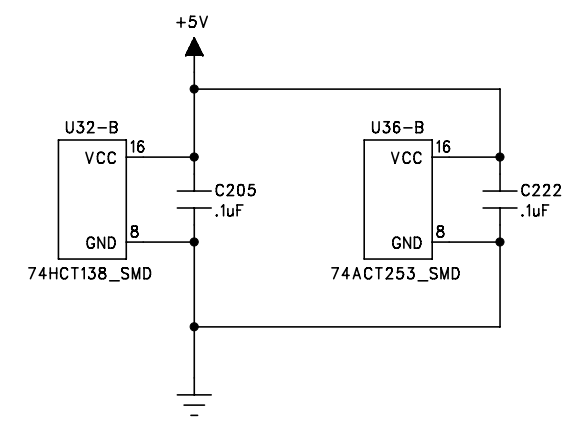
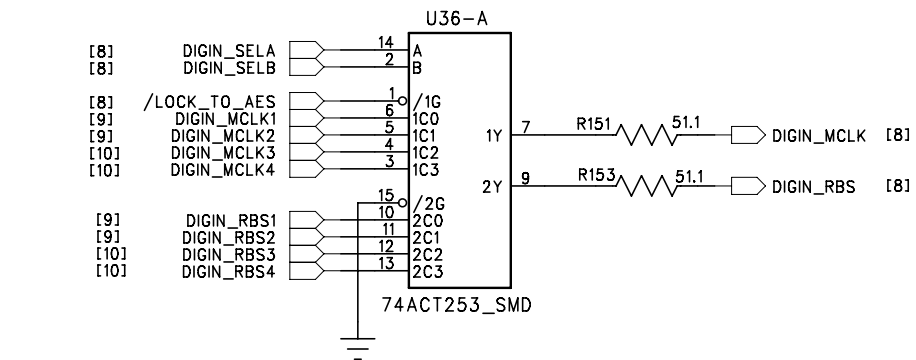
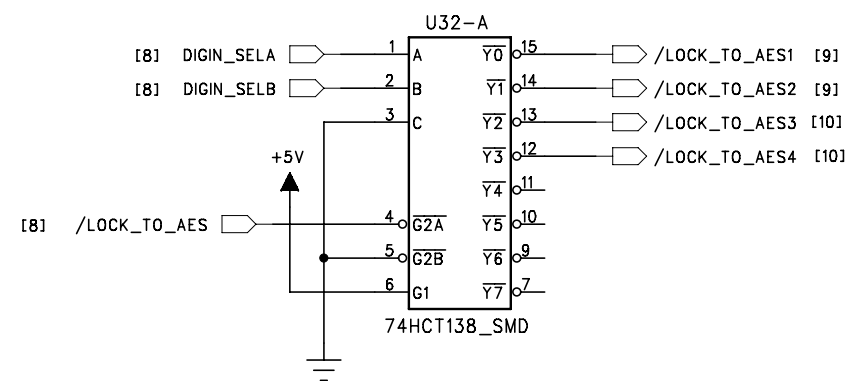
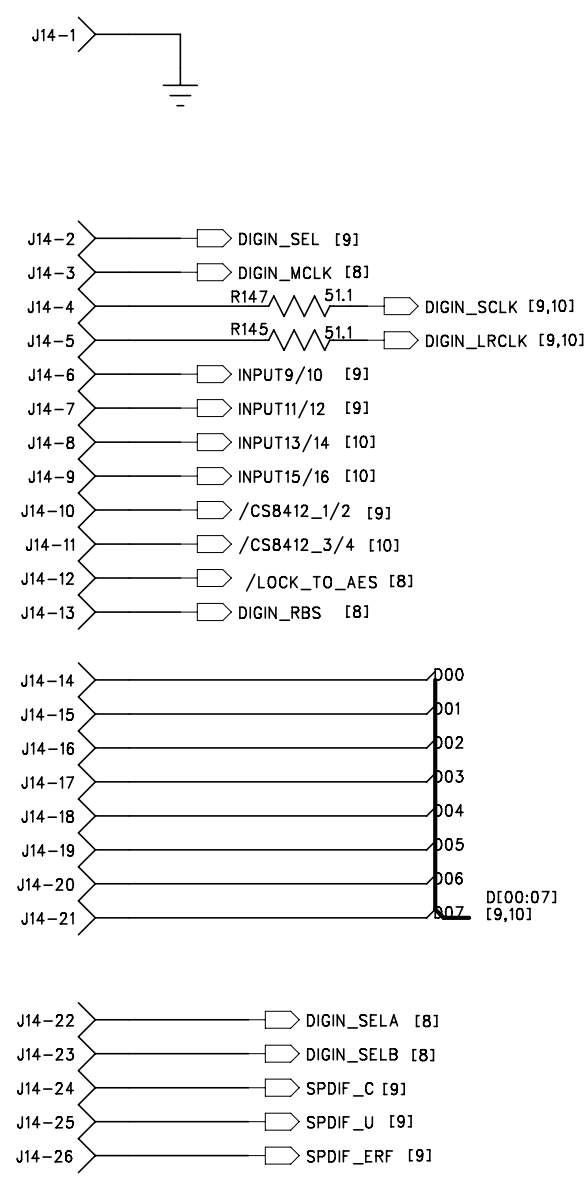
REVISION RECORD		
REV	REVISIONS DONE OR ECO NUMBER:	DATE:

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DRAWN: NO'N	DATED:	TITLE: OP-AMP POWER	REV:
RELEASED:	DATED:	DRAWING NO:	SHEET: 7 OF

6 5 4 3 2 1

REVISION RECORD		
REV	REVISIONS DONE OR ECO NUMBER:	DATE:



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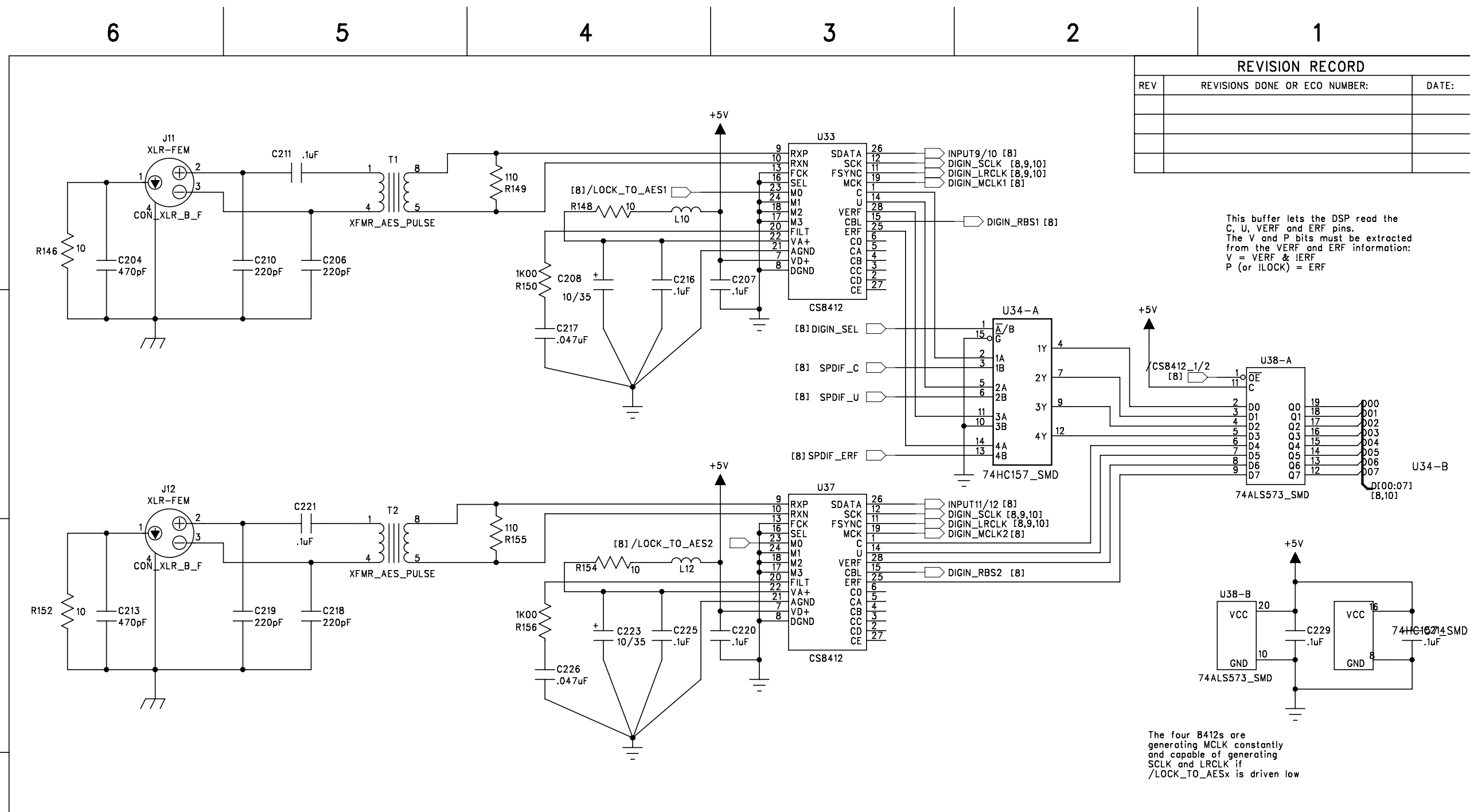
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COMPANY: SYMETRIX INC. 14926 35th Avenue West Lynnwood, WA 98037-2303 USA	
DRAWN:	DATED:
TITLE: DIGITAL INPUT CONN & POWER	
DRAWING NO:	
RELEASED:	DATED:
REV: SHEET: 8 OF	



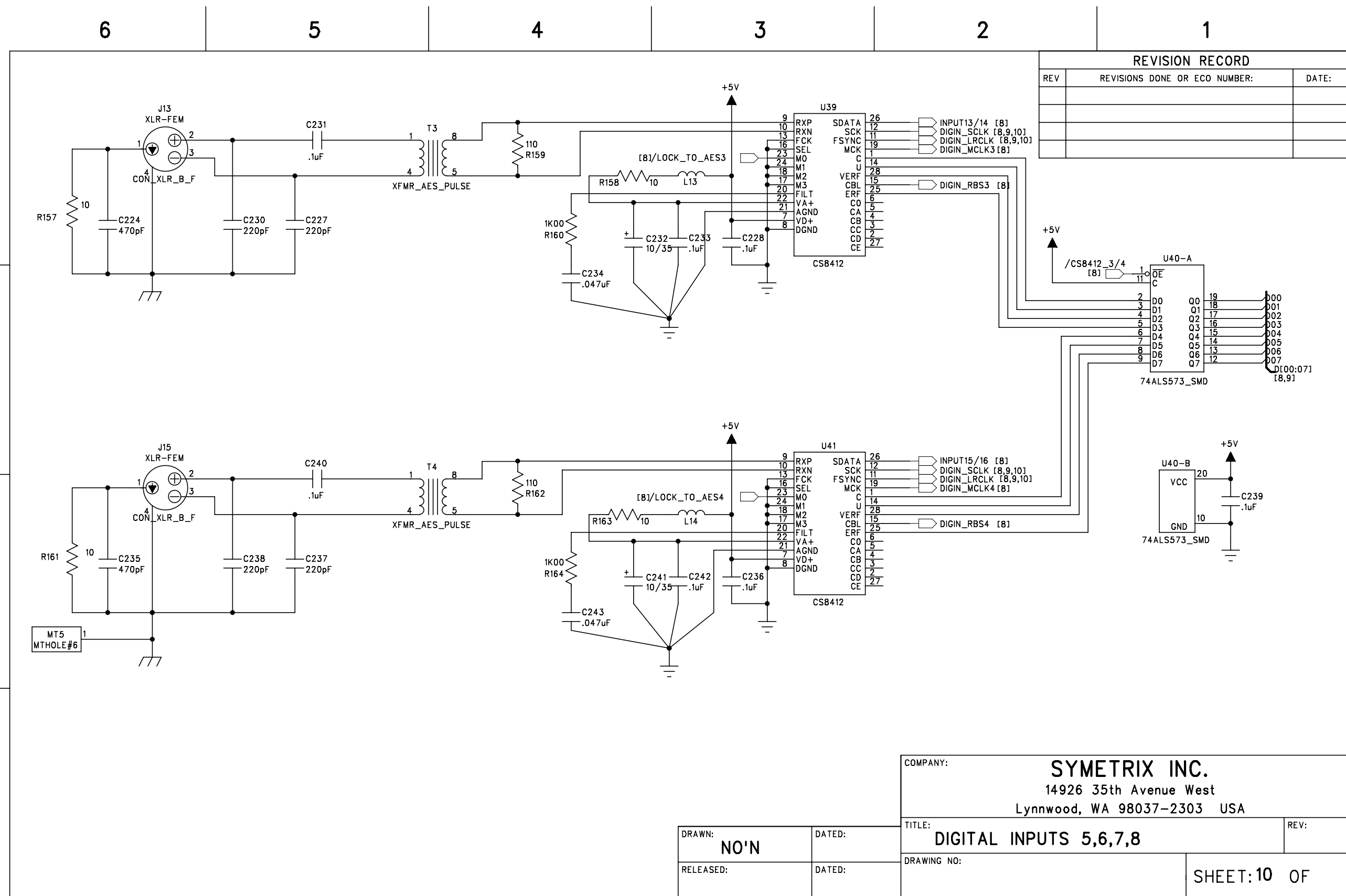
REVISION RECORD		
REV	REVISIONS DONE OR ECO NUMBER:	DATE:

This buffer lets the DSP read the C, U, VERF and ERF pins. The V and P bits must be extracted from the VERF and ERF information: V = VERF & !ERF P (or !LOCK) = ERF

The four 8412s are generating MCLK constantly and capable of generating SCLK and LRCLK if /LOCK_TO_AESx is driven low

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DRAWN: NO'N	DATED:	TITLE: DIGITAL INPUTS 1,2,3,4	REV:
RELEASED:	DATED:	DRAWING NO:	SHEET: 9 OF



REVISION RECORD		
REV	REVISIONS DONE OR ECO NUMBER:	DATE:

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DRAWN: **NO'N**
 DATED:
 RELEASED:
 DATED:

TITLE: **DIGITAL INPUTS 5,6,7,8**
 REV:

DRAWING NO:
 SHEET: **10** OF