Improving VCO Phase Noise Performance Through Enhanced Characterization

By David Vye
Ansoft Corporation

Improved EDA tools allow engineers to easily test and optimize their designs during simulation, before the expensive and time-consuming prototype phase

Minimizing phase noise is a concern of VCO designers because of its direct impact on system performance. Reduction of phase noise begins with noise characterization and continues through modeling and simulation of the design. Many factors affect the accuracy of a phase noise simulation and measurement, and all can be accurately addressed through the use of phase noise simulation along with prudent passive component selection and resonator modeling. Optimum results can best be achieved when the considerations described in this article are followed. The Ansoft Designer EDA tools will be used as the reference in this discussion.

In order to ensure an acceptable level of simulation accuracy for VCOs operating at RF frequencies and above, every component of the linear network including transmission lines and discontinuities must be accurately characterized to several harmonics of the fundamental oscillation frequency. This is essential because the accuracy of the oscillation signal (which affects the noise analysis) and the noise analysis itself greatly depend on the linear network. As a result, any inaccuracies in the linear network characterization will affect the quality of the system's phase noise simulation.

To obtain the best results, the simulation should accurately reflect what will ultimately be fabricated, including actual circuit board dimensions and material properties as well as valid component models of any parasitic behavior. For surface mount components, engineers often rely on equivalent circuit models or measured S-parameters to represent these parts. While component vendors may be able to manufacture and characterize their parts through measurements, board designers need an alternative method for determining circuit performance before fabrication.

By equating physical attributes directly to electrical performance, electromagnetic (EM) simulation is ideal for board characterization. As planar EM technology becomes faster and more integrated into the design process, many engineers are adapting its use for board modeling and design verification. Design environments such as Ansoft Designer, which support the use of circuit components and planar EM co-simulation, allow engineers to simulate complete networks with surface mount component models and appropriately characterized board designs. The designer can incorporate a highly accurate electrical representation of the traces that define the circuit without having to generate a set of S-parameters and manually insert this data.

While the use of schematic-based distributed models (Figure 1) offers a quick method for initial design and optimization, planar EM simulation eliminates the problems associated with model validity caused by range restrictions (such as ratios of width to height) and arbitrary geometries that can be difficult to model with discrete distributed models. EM simulation directly models complex trace metals and all their associated parasitic effects such as interconnect coupling. If the simulation tools support planar EM parameterization along with circuit-planar EM hierarchical design, the overall circuit may be tuned and optimized through manipulation of the physical structure.
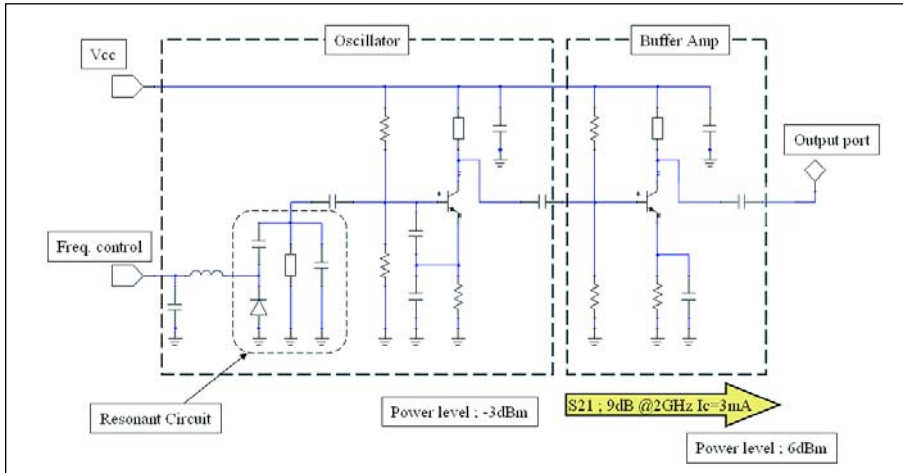
Figure 1 · VCO and buffer amplifier design based on lumped element and simple transmission line models.
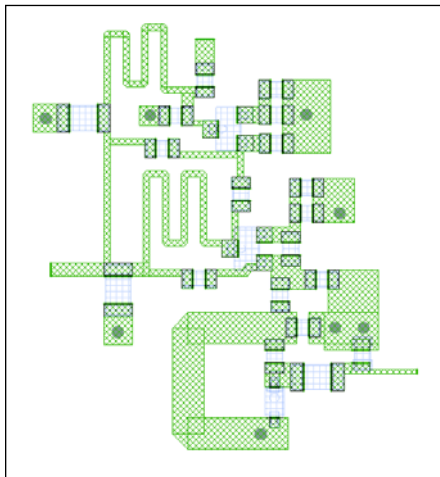

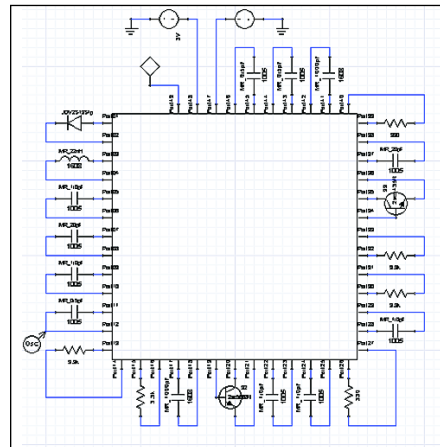**Figure 2 · The VCO layout view, showing the physical design.**

Figure 3 · Schematic view showing resonator EM structure as multi-port symbol.

One difficulty when applying EM-based simulations to a free-running oscillator with a high-Q resonator is the uncertainty of the nonlinear oscillation frequency, which is linked to the resonator circuit. Characterizing the resonator with fine frequency steps will reduce potential interpolation error at the cost of increased simulation time. The engineer must also remember to characterize the resonator at an appropriate number of harmonic frequencies if an accurate phase noise simulation is to be obtained. This increase in frequency points can detract from the speed

advances offered by today's more powerful planar EM tools.

To avoid these problems, Ansoft Designer offers multiple methods of planar EM co-simulation that may be specified by the user. For self-driven circuits such as an oscillator, the user may select the fast frequency sweep option to cover a broad frequency range using dynamic frequency steps. The fast frequency sweep option detects sharp resonances and automatically refines the step size to better capture the changing impedances. Coarse frequency steps may be defined to eliminate EM simulations

from being performed in regions outside the range of likely oscillations or harmonics. For source-driven nonlinear circuits such as amplifiers, the user may select the discrete frequency co-simulation option so that it is automatically employed only at the discrete harmonic frequencies specified by the nonlinear simulation setup. The desired co-simulation attribute is easily specified through the EM component analysis options.

An example of a circuit-planar EM-based resonator design is shown in Figures 2 and 3. The hierarchical approach to this design utilizes a 12-port planar EM "sub-design" that is electrically attached to all surface mount components, ports, and a DC source at the design's top-level. In the schematic view (Figure 3), the planar EM component is represented by the 12-port symbol. The fully synchronized layout view shows details of the resonator's physical attributes, including vias and footprints for all SMT components.

By constructing the resonator with physical layouts of critical transmission lines and component footprints early in the design cycle, it is possible to ensure that the structure will be realizable. EM co-simulation verifies the structure's results, and Ansoft Designer allows circuit and planar structure hierarchy and parameter passing so that variables created by the designer can be used to define geometries and then be swept during analysis for parametric studies. This allows the performance trade-offs between Q-factor, tuning range, output power, and phase noise to be analyzed. In addition, planar EM simulation may be used to examine the current distribution in the structure, in order to investigate undesirable effects such as excessive coupling between an oscillator and buffer amplifier (Figure 4).

With the tools in place to properly characterize the linear network, the engineer should then consider the nonlinear aspects of the simulation.
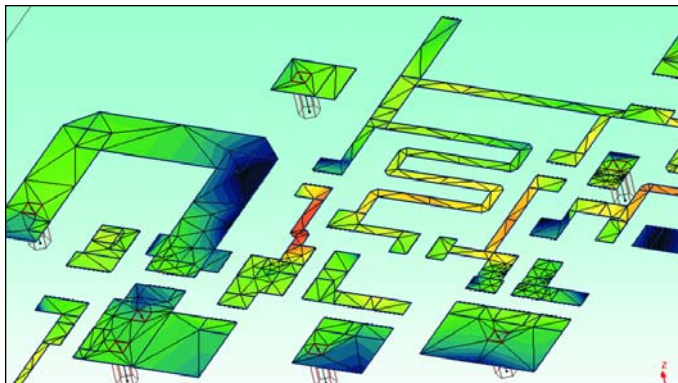
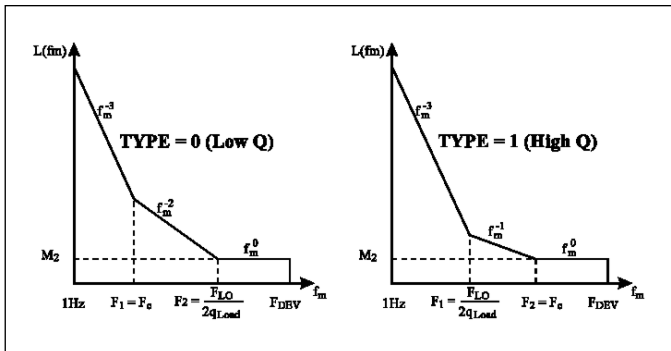Figure 4 · Plot of current distribution in a linear network.

Figure 5 · Phase noise curves for both high-Q and low-Q oscillators.

It is imperative that the simulation resolve the nonlinear analysis with a sufficient number of harmonics in order to accurately simulate accurate power levels. To achieve high accuracy, a convergence test should be run in which the number of harmonics for each analysis is increased and a plot is made of the desired output quantity, e.g. power and phase noise at a specific offset frequency versus the number of harmonics. Once the graph converges within a desired tolerance, it is possible to determine the minimum number of harmonics required to achieve that accuracy. The linear network must be accurately characterized to the frequency represented by this minimum harmonic number.

Obviously, the accuracy of the nonlinear model or models plays a large role in the quality of the overall simulation. The noiseless response of the nonlinear device model must be accurate in order to produce reasonable noise prediction of the overall circuit. The manner in which noise properties of a nonlinear model are characterized and implemented varies from simulator to simulator. In Ansoft Designer, the noise model for the active device consists of two contributions: the shot noise and the flicker noise. The flicker noise is determined from the modeled flicker noise coefficient (KF), flicker noise exponent (AF), and the exponent defining the frequency of the flicker noise (FCP).

Extracting the KF and AF is quite difficult, and extraction at low frequencies by direct measurement of the noise voltage at kilohertz frequencies may not provide valid results when the device is used at microwave frequencies. It is a good idea to build a reference oscillator that can be more easily characterized at a few hundred megahertz, so that noise characterization can be carried out with greater certainty. The flicker noise coefficients can then be extracted from the phase noise measurement of the reference oscillator. It may also be possible to extract bias-dependent KF from such a setup, as the flicker noise model in the transistor is somewhat idealized and using KF vs. bias can improve accuracy. The characteristic phase noise curves for both high-Q and low-Q oscillators are shown in Figure 5.

Simulation accuracy is generally verified by comparing its results with measurement of the actual device. The designer should confirm that the fundamental and harmonic powers and bias currents compare well with measurement results before performing more difficult phase noise measurements. Experience has shown that the measured versus simulated fundamental output powers should agree to within 1 dB, and the harmonic powers should agree to within a few dB, with a looser tolerance on the higher harmonics.

Finally, it is also important to remember that accurate phase noise measurements are quite difficult to achieve, and may be prone to error. Consequently, care must be exercised in making these measurements if the comparison of simulated results with hardware test data is to be meaningful. In addition, several methods are commonly used to measure phase noise, and achieving the same results with each method to an agreement of 1 to 2 dB is difficult. However, by properly characterizing all linear and nonlinear components used in the phase noise simulation, along with a well-characterized phase noise measurement system, accuracy levels within a few dB may be achieved.

Summary

Minimizing phase noise is essential for any communications system to achieve its greatest potential. Since the VCO is one of the key contributors to overall phase noise performance, it is important to reduce its phase noise contribution as much as possible. While the guidelines for VCO simulation provided in this article are not the only ones designers must consider, they can help avoid pitfalls that can increase the time required to achieve excellent results.

Author Information

David Vye is Product Marketing Manager for Ansoft Designer. He can be reached by e-mail at: dvye@ansoft.com