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4600
DIGITAL MULTIMETER

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FOR YOUR SAFETY

Before undertaking any maintenance procedure, whether it be a specific troubleshooting or maintenance procedure described herein or an exploratory procedure aimed at determining whether there has been a malfunction, read the applicable section of this manual and note carefully the WARNING and CAUTION notices contained therein.

The equipment described in this manual contains voltages hazardous to human life and safety and which is capable of inflicting personal injury. The cautionary and warning notes are included in this manual to alert operator and maintenance personnel to the electrical hazards and thus prevent personal injury and damage to equipment.

If this instrument is to be powered from the AC Mains through an autotransformer (such as a Variac or equivalent) ensure that the instrument common connector is connected to the ground (earth) connection of the power mains.

Before operating the unit ensure that the protective conductor (green wire) is connected to the ground (earth) protective conductor of the power outlet. Do not defeat the protective feature of the third protective conductor in the power cord by using a two conductor extension cord or a three-prong/two-prong adapter.

Maintenance and calibration procedures contained in this manual sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures carefully and heed Warnings to avoid "live" circuit points to ensure your personal safety.

Before operating this instrument.

1. Ensure that the instrument is configured to operate on the voltage available at the power source. See Installation section.
2. Ensure that the proper fuse is in place in the instrument for the power source on which the instrument is to be operated.
3. Ensure that all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

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SECTION 1 GENERAL DESCRIPTION

1.1 GENERAL.

1.1.1 The Dana Model 4600 is a compact, highly accurate, four digit instrument featuring autorange, auto polarity, 80 dB normal mode noise rejection, 140 dB common mode noise rejection, and 10,000 megohm input resistance on the DC functions .2 and 2 volt ranges. Available options include Battery Pack, Data Output, and Read, Hold Probe.

1.1.2 The basic instrument has full multimeter capability measuring full scale inputs from 10 μV to 1000 volts on five DC voltage ranges, from 10 μV to 1000 volts on five AC voltage ranges, from 10 mOhms to 20 Megohms on six ohms ranges, 10 namps to 2 amps on five AC current ranges, and 10 namps to 2 amps on five DC current ranges.

1.1.3 High reliability is insured by the use of LSI MOS and solid-state circuitry, including the display. Protection from possible introduction of fault voltage is provided through both mechanical and electrical means. The use of separate input terminals, while routing inputs only when the proper function is selected, reduces the chance of signals reaching the wrong circuitry. The current functions are protected on all ranges by a 2.5 amp fuse; the DC volts function is designed to handle inputs of 1000 volts DC or rms AC on all ranges; the AC volts function is designed to handle inputs of 1000 volts DC or 1000 volts rms AC to 20 kHz, decreasing to 200 volts at 100 kHz on all ranges.

1.1.4 Also available is the Option 51 Isolated Output (designated 4600-51). The option provides the function, range, polarity, and numeric readout data in BCD form both serially and in parallel.

1.1.5 Accessories available for 4600 include:

Option 61	Carrying case.
Option 70	Battery pack for operation – up to four hours continuous use in areas where no AC power is available.
Option 80	Shielded input cable, for use in high noise environments.
Option 81	Hold Probe, provides pushbutton control of Measure/Hold functions.
Option 82	5 KV HV Probe, extends DC voltage measurement to 5 KV.
Option 83	50 KV HV Probe, extends DC voltage measurements to 50 KV.
Option 84	RF Probe, measures RF voltages to 200 MHz.
Option 88	Deluxe test leads, include assorted tips.
Option 89	Standard test leads, with replaceable tips.

1.2 MECHANICAL DESCRIPTION.

1.2.1 The basic DMM is designed as a bench top instrument and comes equipped with a bail handle to simplify carrying. The bail handle rotates 360° and may be used as a "kickstand" for easy measuring and control access.

1.2.2 All components of the basic instrument including the power supply are mounted on two printed circuit boards and housed in a high-impact plastic case. Access to the interior of the instrument for calibration and maintenance is made by removing three screws on the back panel.

1.3 ELECTRICAL DESCRIPTION.

1.3.1 The model 4600 utilizes the dual-slope integration method of analog-to-digital conversion. This technique minimizes the number of components for increased reliability and lower cost while having inherent advantages of stability and noise rejection.

1.3.2 The circuitry consists of a signal conditioning section, digital section, and an analog-to-digital converter.

1.3.3 The analog-to-digital (A/D) converter changes a dc signal fed into it into a representative digital signal. The method used to perform this task is called dual-slope integration.

1.3.4 The digital section measures the output of the A/D converter to produce a numeric value on the instrument display that represents the value of the input signal. The digital section also provides range control and decimal placement.

1.3.5 The signal conditioning section scales, filters, and, when required, converts the input signal to a full scale ± 2 volts for the A/D converter.

1.4 SPECIFICATIONS.

1.4.1 Specifications are provided in table 1.1.

Table 1.1 - Specifications

DC VOLTAGE	
Full Range Display:	±.19999, ±1.9999, ±19.999, ±199.99, ±1000.0
Resolution:	.005% of range except 1000 volt range, .01% of range 10 μV on .2 volt range
Accuracy:	6 Months, 23°C ± 5°C (after zeroing) .2V Range ±(0.02% of reading + 2 digits) 2V, 20V, 200V Ranges ±(0.01% of reading + 1 digit) 1000V Range ±(0.01% of reading + 1 digit)
Temperature Coefficient:	0 to 50°C 2V, 20V, 200V, 1000V Ranges ±(0.001% of reading + .1 digit)/°C .2V Range ±(0.002% of reading + .5 digit)/°C
Input Resistance:	.2V Range $10^{10}\Omega$ minimum 2V Range $10^{10}\Omega$ minimum 20V, 200V, 1000V Ranges 10 MΩ ± .25%
Normal Mode Noise Rejection:	80 dB at 50 and 60 Hz and at multiples of 10 Hz ± 0.1%. 50 dB at 59 Hz, general slope increasing at 12 dB/octave
Common Mode Noise Rejection:	140 dB DC 120 dB at 50 and 60 Hz
Settling Time to 0.01% of Full Scale Step Input:	(With 10 Kohm Source) 700 milliseconds 2.5 seconds maximum on 1 KV range for 1 KV step input

OHMS	
Full Range Display:	.19999 KΩ, 1.9999 KΩ, 19.999 KΩ, 199.99 KΩ, 1999.9 KΩ, 19.999 MΩ
Resolution:	10 milliohms on .2 KΩ range
Accuracy:	6 Months, 23°C ± 5°C .2 KΩ Range ±(0.05% of reading + 2 digits) 2K, 20K, 200 KΩ Range ±(0.05% of reading + 1 digit) 2000 KΩ Range ±(0.1% of reading + 1 digit) 20,000 KΩ Range ±(0.2% of reading + 1 digit)
Temperature Coefficient:	0 to 50°C .2 KΩ Range ±(0.005% of reading + 1 digit)/°C 2 KΩ, 20 KΩ, 200 KΩ Ranges ±(0.0025% of reading + .1 digit)/°C 2000 KΩ Range ±(0.005% of reading + .1 digit)/°C 20,000 KΩ Range ±(0.005% of reading + .1 digit)/°C
Settling Time to Rated Accuracy:	Less than 700 msec on all ranges
Maximum Input Voltage:	250V DC or peak AC all ranges
Current through Unknown and Voltage across Unknown:	Range / Current / Voltage .2 KΩ / 1 mA / 0.2 volts 2 KΩ / 1 mA / 2 volts 20 KΩ / 100 μA / 2 volts 200 KΩ / 10 μA / 2 volts 2000 KΩ / 1 μA / 2 volts 20,000 KΩ / 0.1 μA / 2 volts
Open Circuit Voltage:	7 volts maximum

Table 1.1 - Specifications continued

AC VOLTS	
Full Range Display:	.19999, 1.9999, 19.999, 199.99, 2000.0V rms
Resolution:	10 microvolts on the .2 volt range
Accuracy: (From 1% of range to 100% of range)	6 Months, 23°C ± 10°C .2 Volt Range 30 Hz to 50 Hz ±(0.1% of reading + 70 digits) 50 Hz to 500 Hz ±(0.1% of reading + 30 digits) 500 Hz to 50 kHz ±(0.08% of reading + 16 digits) 50 kHz to 100 kHz ±(.7% of reading + 40 digits) 2,200 Volt Ranges 30 Hz to 50 Hz ±(0.25% of reading + 20 digits) 50 Hz to 20 kHz ±(0.1% of reading + 9 digits) 20 kHz to 50 kHz ±(0.1% of reading + 10 digits) 50 kHz to 100 kHz ±(.7% of reading + 14 digits) 20 Volt Range 30 Hz to 50 Hz ±(.25% of reading + 30 digits) 50 Hz to 20 kHz ±(.1% of reading + 12 digits) 20 kHz to 50 kHz ±(.1% of reading + 16 digits) 50 kHz to 100 kHz ±(.7% of reading + 16 digits) 2000 Volt Range (10V to 500V) 30 Hz to 50 Hz ±(0.45% of reading + 10 digits) 50 Hz to 20 kHz ±(0.15% of reading + 5 digits)

AC VOLTS continued	
Accuracy: (con't)	2000 Volt Range (500V to 1000V) 30 Hz to 50 Hz ±(0.5% of reading + 10 digits) 50 Hz to 20 kHz ±(0.2% of reading + 5 digits)
Temperature Coefficient:	30 Hz to 10 kHz ±(0.01% of reading + .4 digits)/°C 10 kHz to 100 kHz ±(0.05% or reading + .1 digit)/°C
Common Mode Noise Rejection:	Less than 80 dB at 50 Hz and 60 Hz with 1 Kohm imbalance in either lead
Input Impedance:	1 Megohm with 100 pF shunt capacitance with .22 μF in series on all ranges
Zero Offset:	**Range** .2V 40 digits max 2V 5 digits max 20V 30 digits max 200V 5 digits max 2000V 5 digits max
Settling Time (To 100% of range):	1% of range to F.S. or F.S. to 1% of range Step settles to 0.1% of final value within 1.5 seconds

CURRENT AC	
Full Range Display:	.19999 mA, 1.9999 mA, 19.999 mA, 199.99 mA, 1999.9 mA
Shunt Values:	.2 mA 1 KΩ 2 mA 100Ω 20 mA 10Ω 200 mA 1Ω 2000 mA 0.1Ω
Input Protection:	2.5 Amp Fast Blow Fuse
Accuracy: (From 1% of range to 100% of range)	6 Months, 23°C ± 5°C 50 Hz – 10 kHz .2, 2, 20, 200 mA Range ±(0.2% of reading + 20 digits) 2000 mA Range ±(0.3% of reading + 20 digits)
Temperature Coefficient:	±(0.015% of reading + .6 digits)/°C

Table 1.1 - Specifications continued

CURRENT DC	
Full Range Display:	±.19999 mA, ±1.9999 mA, ±19.999 mA, ±199.99 mA, ±1999.9 mA
Shunt Values:	.2 mA 1 KΩ 2 mA 100Ω 20 mA 10Ω 200 mA 1Ω 2000 mA 0.1Ω
Input Protection:	2.5 Amp Fast Blow Fuse
Accuracy:	6 Months, 23°C ± 5°C .2, 2, 20, 200 mA Ranges ±(0.12% of reading + 4 digits) 2000 mA Range ±(0.3% of reading + 20 digits)
Temperature Coefficient:	0 to 50°C ±(0.01% of reading + .2 digits)/°C

GENERAL	
Ranging:	Automatic or Manual
Digitizing Technique:	Dual Slope
Signal Integration Time:	100 msec ± .25%
Read Rate:	400 msec per reading 2-1/2 reading per second ±.25%
Maximum Common Mode Voltage:	1 KV DC or peak AC input to Earth Ground
Power Requirements:	100, 120, 220, 240 volts ±10% from nominal. 50 to 400 Hz, 10 watts maximum
Storage Temperature:	−20° C to 75° C −20° C to 65° C w/battery opt.
Operating Temperature:	0 – 50°C
Warmup:	30 minutes to 6 month accuracy
Weight (Approx.):	Std: 2.3 Kg (5 lbs.) With Battery Option: 3.2 Kg (7 lbs.)
Dimensions:	73mm x 200mm x 250mm (2.87 x 7.87 x 9.84 inches)

SECTION 2 INSTALLATION & OPERATION

2.1 GENERAL.

2.1.1 This section covers the incoming inspection, installation, storage and operation of the Model 4600 DMM.

2.2 UNPACKING & INSPECTION.

2.2.1 The Model 4600 is enclosed between two molded, plastic-foam forms and packaged in a double-walled cardboard carton for shipment. The plastic forms hold the instrument securely in the carton and absorb any reasonable external shock normally encountered in transit.

2.2.2 Prior to unpacking, examine the exterior of the shipping carton for any signs of damage. Carefully remove the DMM from the carton and inspect the exterior of the instrument for any signs of damage. If damage is found, notify the carrier immediately.

2.3 BENCH OPERATION.

2.3.1 The instrument comes equipped with a bail handle that doubles as a carrying handle and as a "kickstand" for elevating the front of the instrument.

2.4 RACK MOUNTING.

2.4.1 The rack mounting kit (Option 60) allows the user to mount the instrument Offset Left or Offset Right in a standard 19-inch rack and requires 3-1/2 inches of vertical mounting space. The kit consists of a rack mount panel, left and right case supports, two brackets, and 8 securing nuts.

2.4.2 The option is shown in figure 2.1 and assembled as described below:

a. Index rack mount panel for desired position (Offset Left or Offset Right).

b. Place the left and right case supports over the two sets of studs on the case supports face out. Mount the case supports to the panel with four of the securing nuts and washers.

c. Set the instrument bail to the rear of the instrument. Place the instrument between the case supports with the bail handle passing through the slots in the case supports.

d. Place the slotted part of each bracket over the case support studs so that the curved portion of each bracket goes around the bail. Secure the brackets with the remaining four nuts and washers.

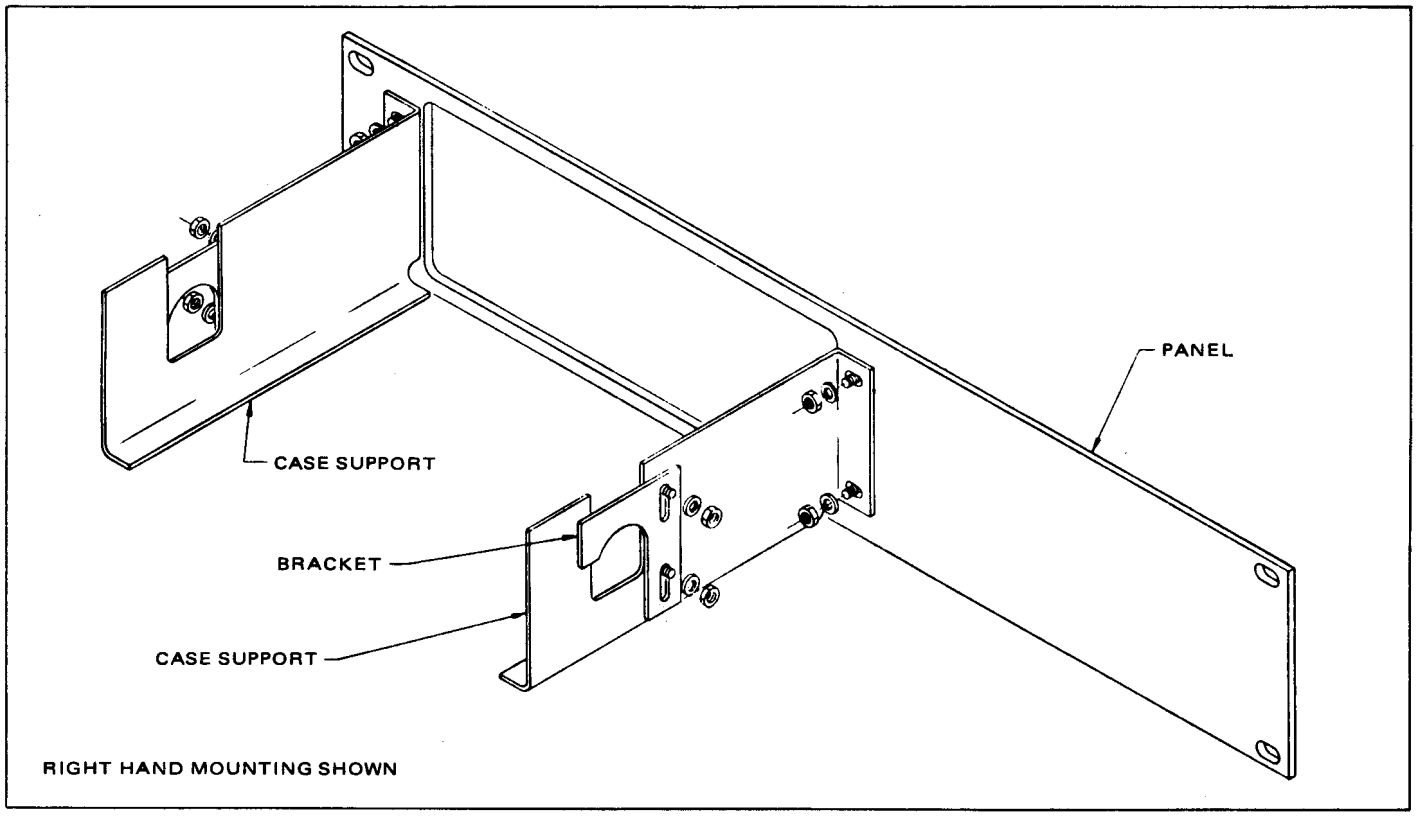
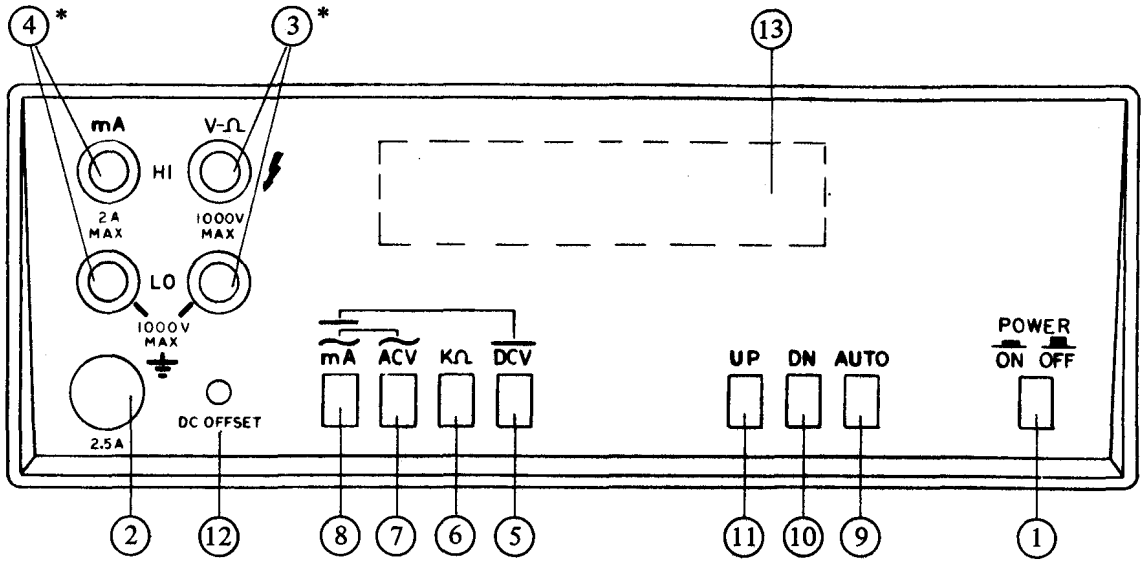


Figure 2.1 - Rack Mount Installation

Table 2.1 - Front Panel Identification



(1) POWER Switch, push on, push off.

(2) POWER Fuse Holder, 2.5 Amp, protects measurement circuitry on current measurements.

(3)* VOLTAGE-OHMS measurement input jacks.

(4)* CURRENT measurement input jacks.

(5) DC VOLTS Function Select Switch, push on.

(6) KOHMS Function Select Switch, push on.

(7) AC VOLTS Function Select Switch, push on.

(8) MA Function Select Switch, push on, push off. Used with DC volts and AC volts select switches.

(9) AUTO selects range most compatible with input signal. Push on, push off.

(10) DN. Causes instrument to downrange. Momentary on.

(11) UP. Causes instrument to uprange. Momentary on.

(12) DC OFFSET. Allows user to compensate out unwanted input signal bias.

(13) DISPLAY consists of four full decade readouts "0 – 9" and a "±1" readout, all .43 inch yellow LED types.

*See CAUTION, paragraph 2.9.5.2

2.5 POWER REQUIREMENTS.

2.5.1 Power is supplied to the instrument through a standard 6-foot long detachable power cord connected to power input jack J201.

2.5.2 The power fuse holder is located next to the power input jack and uses a .25 ampere fast blow fuse.

2.5.3 The instrument is designed for operation at a line voltage of 100, 120, 220, 240 volts ± 10%, 50 to 400 Hz. The instrument is set to the desired voltage by the position of the line voltage printed circuit board in connector J14 on the main printed circuit board.

2.5.4 Access to the line voltage adjustment PCB is gained by removal of 3 screws at the rear of the instrument and the removal of the case (see table 2.2).

WARNING

Removal of covers exposes potentially lethal voltages. Avoid contact with internal electrical connections while unit is connected to AC power source.

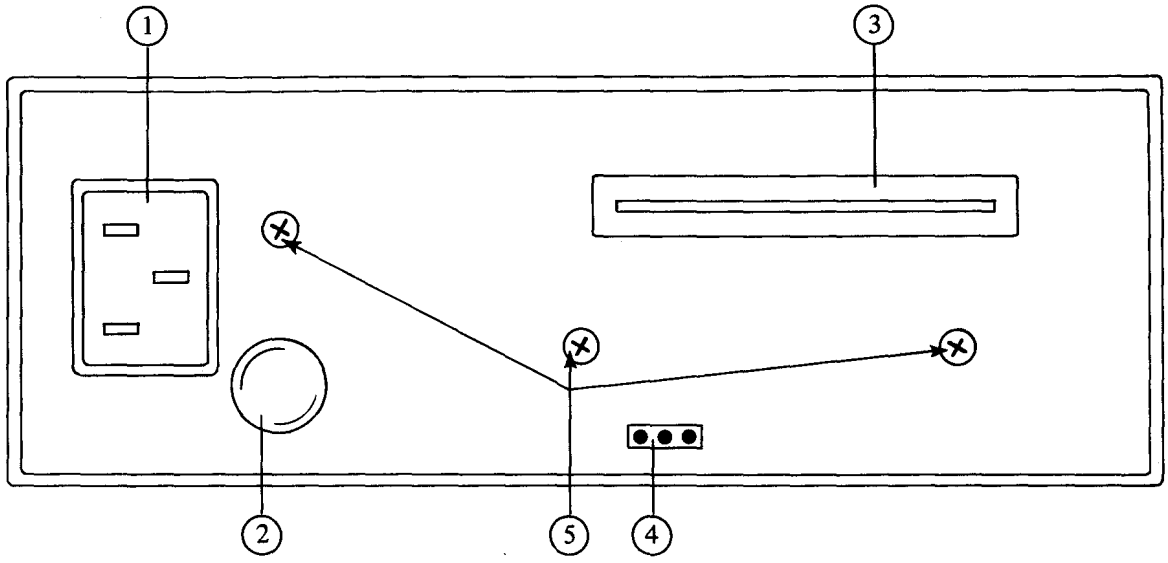
2.5.5 Selection of the line voltage is accomplished by removing the instrument from its case and positioning a printed circuit jumper so that the desired line voltage appears in the aperture in the right hand side of the case. Figure 2.2 illustrates the location of the PCB jumper and figure 2.3 illustrates the aperture with the jumper in place for 120 volt operation.

2.6 STORAGE REQUIREMENTS.

2.6.1 The instrument can be stored at temperatures ranging from –20°C to +70°C† at 75% relative humidity

† to +65°C with battery option

Table 2.2 - Rear Panel Identification



(1) POWER Receptacle J201. This receptacle receives power cable.

(2) FUSE Holder, .25 Amp fast blow, is in series with high side of power line & power transformer.

(3) BCD OUTPUT Connector J202. Available only on instruments equipped with the option 51 BCD output option.

(4) READ/HOLD Control Connector. Receives Read/Hold Switch option.

(5) DISASSEMBLY Screws. Removal of these screws permits removal of case.

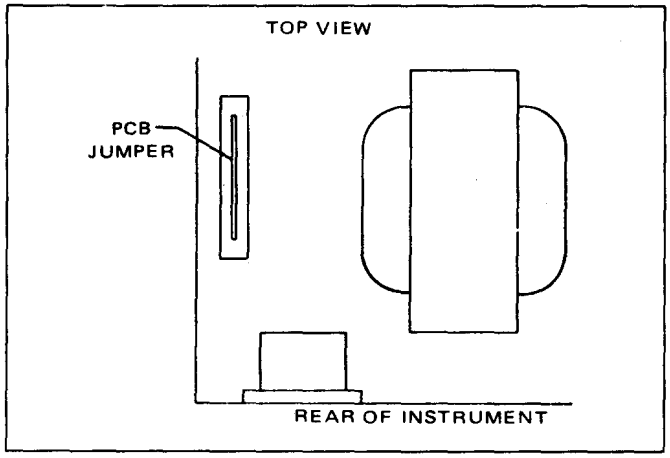


Figure 2.2 - Line Selector PCB Jumper Location

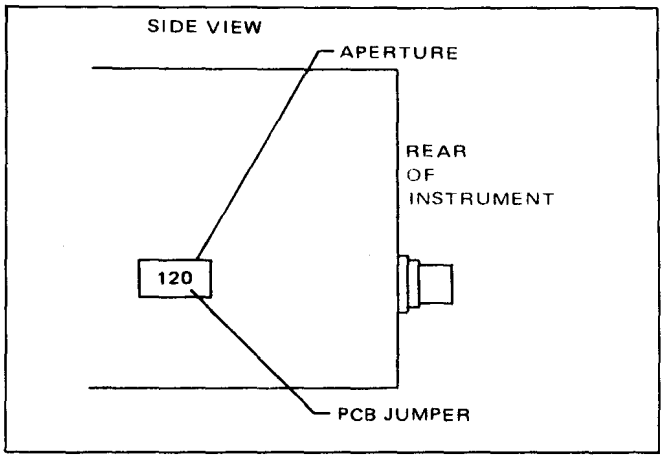


Figure 2.3 - Line Voltage Indicator Aperture

without adversely effecting operation or accuracy. The instrument must be brought up to operating range (0°C to 50°C) before power is applied.

2.7 RESHIPMENT PACKAGING REQUIREMENTS.

2.7.1 The shipping carton with its molded plastic foam form and plastic dust cover is specifically designed to provide the required support necessary for safe shipment. Whenever possible, these should be used for reshipment.

2.7.2 If the original packing materials are not available, proceed as follows:

a. Wrap instrument in plastic or heavy paper.

b. Place packing material around all sides of instrument and pack in cardboard box.

c. Place instrument and inner container in a sturdy cardboard or wooden box. Mark box with appropriate precautionary labels.

2.8 INPUT/OUTPUT/CONTROLS.

2.8.1 In tables 2.1 and 2.2 are described the operating controls and their function. Also described are input and output connectors.

2.9 OPERATION.

2.9.1 Operation consists of selecting the desired function, selecting autorange or manually selecting the desired range, applying the input signal and reading the results on the instrument readout.

2.9.2 Autorange.

2.9.2.1 In autorange the instrument automatically selects the range most appropriate for the signal being measured.

2.9.2.2 As the input signal changes, the instrument changes ranges as required. Upranging occurs at 100% of range and downranging occurs at 5% of range.

2.9.3 Manual Range.

2.9.3.1 When autorange is not selected, the instrument is in manual range. Higher or lower ranges are selected by pressing the UP or DN range buttons. A new range is selected at the read rate within the range limits of the selected function as long as the UP or DN buttons are pressed.

2.9.3.2 The available ranges for each function are given in table 2.3.

Table 2.3 - Available Ranges

DCV	DCI (mA)	ACV	ACI (mA)	KΩ
.2	.2	.2	.2	.2
2	2	2	2	2
20	20	20	20	20
200	200	200	200	200
1000	2000	1000	2000	2000
—	—	—	—	20,000

2.9.4 Overrange.

2.9.4.1 Overrange occurs when the signal being monitored is greater than the instrument can measure with the range selected.

2.9.4.2 Overrange is indicated by the display flashing at the read rate.

2.9.5 Signal Input.

2.9.5.1 Signal input is through four banana jacks on the front panel. These jacks accept standard probe banana plugs and are spaced to accept dual banana plugs. Several probe sets for the 4600 are available from the factory (see Section 1).

2.9.5.2 The left hand pair of input jacks are reserved for DC and AC current measurements; the jacks on the right are for voltage and resistance measurements.

> **CAUTION**
>
> Do not connect test leads between the mA and V-Ω jacks. Application of voltage or current between these jacks can damage the instrument.

2.9.5.3 As a general rule for voltage measurements, the Hi side is connected to the highest impedance point to be measured and the LO side is connected to the point nearest ground. If shielding is used on the input cables, it should be tied to the LO input side unless it is used in the Ohms function. The shield then should be tied to the LO current input side.

2.9.5.4 Maximum inputs are shown in table 2.4.

Table 2.4 - Maximum Inputs

Current	Max current input 2 Amps (current jacks)
Volts DC	DC, rms AC 1000 volts
Volts AC	1000V DC to 20 kHz rms decreasing linearily to 200V at 100 kHz
Kohms	250 volts max.
Common Mode	1000 volts DC or peak AC max. from input to earth ground, data output common tied to earth ground

2.9.6 Function Select.

2.9.6.1 The select buttons for AC volts, kilohms, and DC volts are interlocked; when one of these buttons is pushed, any other button in the set is released.

2.9.6.2 The current button is selected in addition to the AC volt or DC volt button for current measurement and is unselected when current measurement is no longer desired.

2.10 HOLD/READ PROBE (Option 81).

2.10.1 This option consists of a probe with a built-in switch that connects to J203 on the rear panel.

2.10.2 With the option plug inserted in J203 in the read position, the instrument takes readings only as long as the switch is held down.

2.10.3 With the option plug inserted in J203 in the hold position, the instrument goes into the hold mode when the switch is pressed.

2.11 BCD OUTPUT (Option 51).

2.11.1 This option provides function, range, polarity, and the display value in BCD form for printer or other digitally operated device. It is designed to interface with units requiring serial or parallel output. The option is covered in detail in Section 3.

NOTE

Option 51 is not available for units equipped with the Option 70 battery pack.

2.12 BATTERY PACK (Option 70).

2.1.2.1 With the battery pack option the instrument becomes completely portable, taking measurements for up to four hours of continuous use. Recharging occurs when the instrument is connected to the power line and the power switch is set to the OFF position.

2.12.2 When the battery charge drops below operating level, the condition is indicated by a LED lamp on the instrument front panel. To fully recharge the batteries requires about 16 hours.

NOTE

Option 70 is not available for units equipped with the Option 51 BCD Output.

CAUTION

On units equipped for battery pack operation (Option 70) the batteries are charging when the instrument is connected to the AC power source and the instrument is turned off. The batteries charge in approximately 16 hours; it is recommended that the unit be unplugged during extended periods of non-use to avoid possible damage to the batteries.

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SECTION 3 BCD OUTPUT

3.1 GENERAL.

3.1.1 The Model 4600 Option 51 Isolated Output provides the function, range, polarity, and numeric readout data in BCD form, both serially and in parallel, from a single connector on the instrument rear panel. The output data is completely isolated from the measurement portion of the 4600, thereby preserving the common mode noise characteristics of the instrument.

3.2 MECHANICAL DESCRIPTION.

3.2.1 All components for the option are on a single printed circuit board that is mounted above the instrument main PC board by four spacers; an aluminum shield, located between the boards, prevents any digital noise generated on the option board from affecting the measurement circuitry on the Main board.

3.2.2 One end of the option board forms an edge connector that extends out the back of the instrument through a slot provided for this purpose. This connector is the option output connector and is designated J202.

3.3 ELECTRICAL DESCRIPTION.

3.3.1 The option, shown in simplified block diagram form in figure 3.1, consists of a floating section, a grounded section, and six optical couplers.

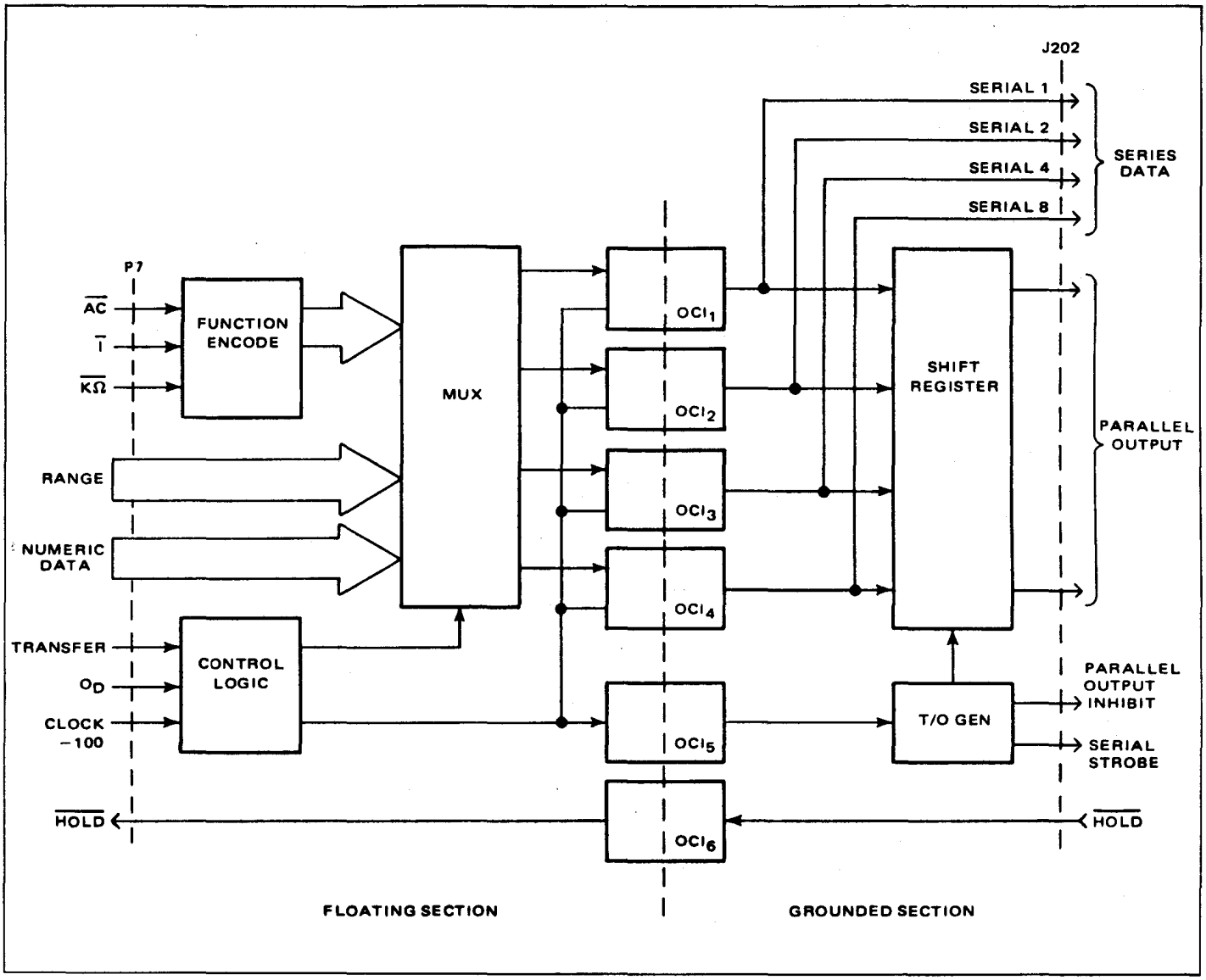

Figure 3.1 - BCD Output

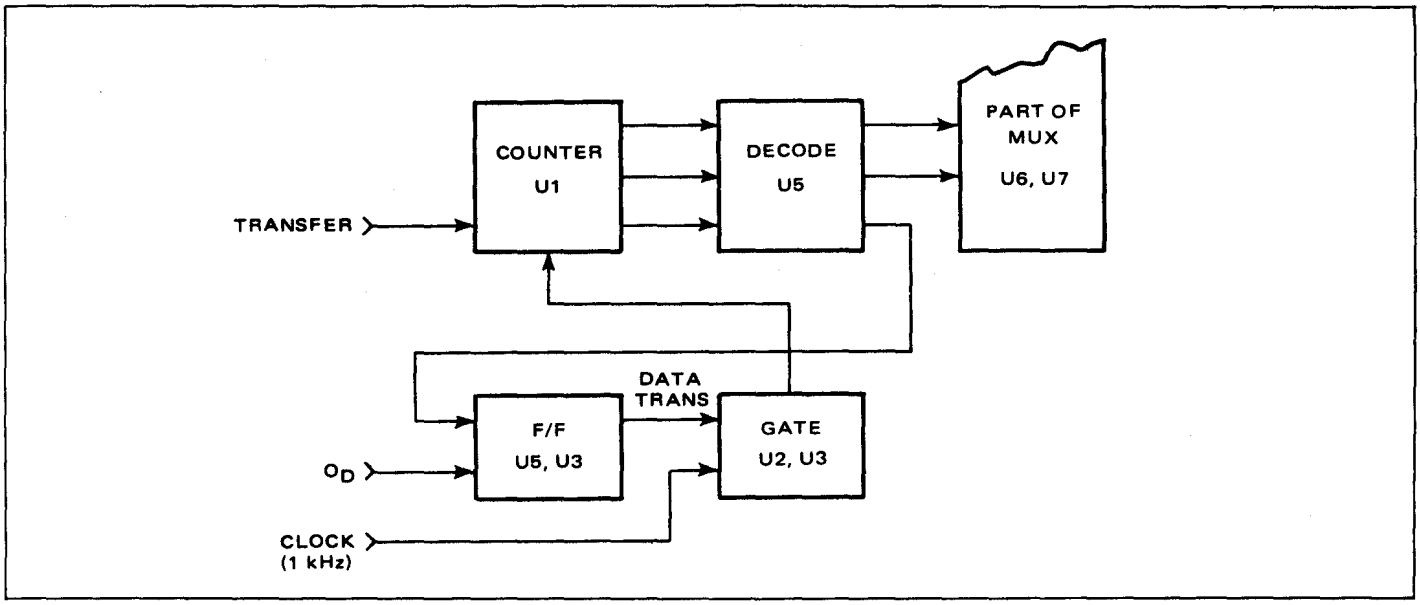

Figure 3.2 - Control Logic

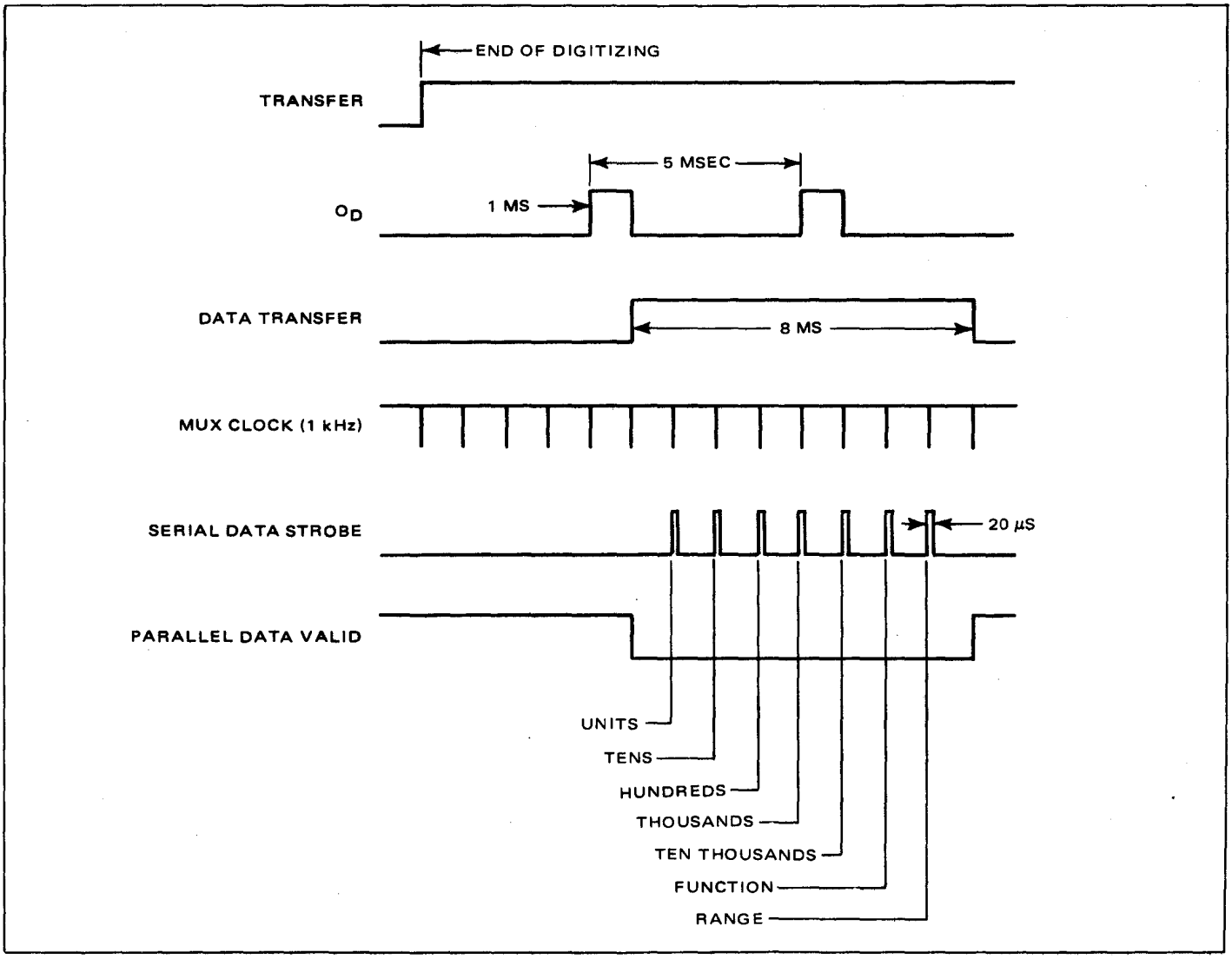

Figure 3.3 - Timing Diagram

3.3.2 The floating section encodes and multiplexes the binary data from the measurement portion of the instrument and transmits the data through optical couplers 1 through 5. The sixth coupler is used for HOLD (see paragraph 3.4.7). The floating section consists of: Function Encode, the Multiplexer (MUX), and the Control Logic.

3.3.2.1 The multiplexer consists of two dual 4-line to 1-line data selector/multiplexers, U6 and U7. The multiplexer receives inputs from the function encode circuitry and control signals from the control logic, both located on the option board, and range and numeric data from the display board. The multiplexer has a 4-bit byte output which drives the four optical data couplers; the output byte corresponds to one of the three possible input bytes, selected by the control logic.

3.3.2.2 The Control Logic, shown simplified in figure 3.2, consists of an R/S flip-flop (U5, U3), gate circuit (U2, U3), counter (U1), and decode logic (U5). The control logic generates the operational logic for the multiplexer and the strobe signal which drives the five data optical couplers and provides timing information for the grounded side. The circuitry operates by following a predetermined series of steps shown in figure 3.3. The operation starts when the TRANSFER line goes true, permitting counter U1 to count as soon as pulses are received from the gate circuit. When O_D, a strobe signal from the counter/multiplexer on the Display board, is received the negative going edge of the signal sets the flip-flop output true (Data Transfer). The data transfer signal enables the gate, allowing the 1 kHz clock signal (also from the counter/multiplexer on Display board) to advance counter U1. The output of the counter is decoded by U5.

3.3.2.3 The clock advances the counter through seven steps. At the same time seven strobe pulses are generated. The operation of the control logic is synchronized with the strobing action of the counter/multiplexer of the measurement circuitry so that during the first five steps of counter U1, the five readout data bytes to the MUX are selected and the readout value being strobed to the display is being routed through the multiplexer and optical couplers. The sixth step the multiplexer selects the encoded Function byte. The seventh step the multiplexer selects the Range byte. On the eighth step, the flip-flop is reset and the gate is inhibited, preventing the advancement of the counter or the generation of additional strobe signals. The counter is reset when TRANSFER goes false.

3.3.2.4 The function encoding circuitry converts the $\overline{+}$ polarity, $\overline{AC}$, $\overline{I}$, and $\overline{K\Omega}$ inputs into a BCD coded output for use by the multiplexer.

3.3.3 The grounded portion of the option converts the data from the optical isolators to provide the output data in series and parallel form for a recorder or other digitally operated device at connector J10. The grounded portion consists of a shift register, a dual timeout generator and hold circuitry.

3.3.3.1 The shift register consists of four 8-bit parallel out serial shift registers, each of which is driven by one of the four data optical couplers (OCI 1 through 4). The outputs of the optical couplers are also used as the serial outputs, being binarily weighted (1-2-4-8). The strobe pulse is received through optical coupler (OCI 5) and applied to the command inputs of the dual one-shot.

3.3.3.2 One output pair of the one-shot is programmed to generate an eight millisecond pulse (PARALLEL DATA VALID and its reciprocal, INHIBIT PARALLEL DATA); the other output pair is programmed to generate a 20 microsecond pulse (SERIAL DATA STROBE and its reciprocal $\overline{\text{SERIAL DATA STROBE}}$). Serial Data Strobe is inverted and used to strobe the shift register.

3.3.3.3 The hold circuit permits the user to electrically stop the instrument from taking new readings through the BCD output connector. The circuit consists of the 2 transistors (one on the grounded portion and the other on the floating portion) and an optically coupled isolator (OCI 6).

3.4 OPERATION.

3.4.1 Provided with the Option 51 is the mating connector (Dana P/N 600810), a key (Dana P/N 600811) for preventing misalignment of the connector, mounting screws, and 44 connector pins (Dana P/N 600809). Pin identification is provided in table 3.1. The pins used, however, depend on the type of operation used (serial or parallel).

3.4.2 All output lines are from TTL logic and are referenced to pin 2. A reference +5 volt output is provided at pin 1 for printer reference. Output levels of the data output are defined as:

Logic Hi: +2.4 volts minimum

Logic Lo: +0.8 volts maximum (8 ma current sink)

3.4.3 Function Codes.

3.4.3.1 The function codes are shown in table 3.2.

Table 3.1 - Pin Location J202

	J202		
+5V Ref	1	A	
Earth Ground	2	B	
	3	C	Serial Data Strobe
	4	D	Parallel Data Valid
	5	E	$\overline{\text{Serial Data Strobe}}$
	6	F	Inhibit Parallel Data
	7	H	$\overline{\text{Hold}}$
Serial Output (4)	8	J	Serial Output (8)
Thousands (4)	9	K	Thousands (8)
Function (4)	10	L	
Range (4)	11	M	+ Polarity
Hundreds (4)	12	N	Hundreds (8)
Tens (4)	13	P	Tens (8)
Units (4)	14	R	Units (8)
Serial Output (2)	15	S	Serial Output (2)
Thousands (1)	16	T	Thousands (2)
10 Thousands (1)	17	U	10 Thousands (2) (OL)
Function (1)	18	V	Function (2)
Range (1)	19	W	Range (2)
Tens (1)	20	X	Hundreds (2)
Hundreds (1)	21	Y	Tens (2)
Units (1)	22	Z	Units (2)

Table 3.2 - Function Codes

Function	F1	F2	F4	F8	Dec
– DC	0	0	0	0	0
+ DC	1	0	0	0	1
ACV	1	1	0	0	3
– DCI	0	0	1	0	4
+ DCI	1	0	1	0	5
ACI	1	1	1	0	7
KΩ	1	0	0	1	9

3.4.4 Range Codes.

3.4.4.1 The range codes are shown in table 3.3.

Table 3.3 - Range Codes

Range	R1	R2	R4	Dec
20,000	1	0	1	5
2,000	0	0	1	4
200	1	1	0	3
20	0	1	0	2
2	1	0	0	1
.2	0	0	0	0

3.4.5 Serial Output.

3.4.5.1 The data output is available in serial form on four lines; strobe data is available in logic true and inverted true form. Pin identification for lines used in serial out is provided in table 3.4.

Table 3.4 - Serial Out Pin Location

	J202		
+5V Ref	1	A	
Earth Ground	2	B	
	3	C	Serial Data Strobe
	4	D	
	5	E	$\overline{\text{Serial Data Strobe}}$
	6	F	
	7	H	$\overline{\text{Hold}}$
Serial Output (4 lines)	8	J	Serial Output (8 lines)
	9	K	
	10	L	
	11	M	
	12	N	
	13	P	
	14	R	
Serial Output (2 lines)	15	S	Serial Output (2 lines)
	16	T	
	17	U	
	18	V	
	19	W	
	20	X	
	21	Y	
	22	Z	

3.4.5.2 At the completion of the measurement, the data strobe output generates seven 20 μsecond pulses at a 1 kHz rate. During each strobe pulse, a new data byte appears at the data output lines. The serial data is shown in table 3.5.

Table 3.5 - Serial Data Out

Word	Bit			
	8	4	2	1
1	8	4	2	1
2	80	40	20	10
3	800	400	200	100
4	8K	4K	2K	1K
5	0	0	20K (OL)	10K
6	F8	F4	F2	F1
7	0	R4	R2	R1

3.4.6 Parallel Output.

3.4.6.1 The data is available in standard BCD form (parallel) on twenty-four lines of J202 as shown in table 3.6.

3.4.6.2 Data at the output pins is available when Parallel Data pin D is true (8 milliseconds). Inhibit Parallel Data is the inverted output of pin D and can be used when negative true logic is required for a print pulse.

3.4.7 Hold.

3.4.7.1 The hold line is an external command line. When held at logic low, prevents a new measurement cycle from starting. Any measurement in progress when hold is commanded is allowed to complete.

Table 3.6 - Parallel Out Pin Location

	J202		
+5V Ref	1	A	
Earth Ground	2	B	
	3	C	
	4	D	Parallel Data Valid
	5	E	
	6	F	Inhibit Parallel Data
	7	H	$\overline{\text{Hold}}$
	8	J	Thousands (8)
Thousands (4)	9	K	
Function (4)	10	L	
Range (4)	11	M	
Hundreds (4)	12	N	Hundreds (8)
Tens (4)	13	P	Tens (8)
Units (4)	14	R	Units (8)
	15	S	
Thousands (1)	16	T	Thousands (2)
10 Thousands (1)	17	U	10 Thousands (2) (OL)
Function (1)	18	V	Function (2)
Range (1)	19	W	Range (2)
Tens (1)	20	X	Hundreds (2)
Hundreds (1)	21	Y	Tens (2)
Units (1)	22	Z	Units (2)

3.4.7.2 The value of the last measurement remains in the display and is available at the parallel data output lines (although no new parallel data output pulse is generated). The data is not present at the serial data output lines following the last reading taken.

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SECTION 4 THEORY OF OPERATION

4.1 GENERAL.

4.2 This section describes the operation of the Model 4600 DMM and includes the basic technique used as well as a more detailed explanation of the major functional portions.

4.3 CIRCUIT DESCRIPTION.

4.4 A functional block diagram of the instrument is presented in figure 4.1. The diagram is divided into four major areas for purposes of discussion; (1) Signal Conditioning, (2) Digitizing, (3) Ranging, and (4) Display. Measurement signals applied to the input terminals are routed to the appropriate signal conditioning device by the function controls. Because the isolator amplifier operates with low voltages, dc measurement signals higher than 2 volts must be scaled down. This is accomplished by the attenuator. The attenuator also changes the source current flow on the ohms ranges and provides the required shunting on ac current ranges. The ac converter contains its own voltage attenuator for the ac voltage ranges above 2 volts.

4.5 The ac converter produces a dc output level proportional to the ac measurement applied to its input. On the ac ranges this dc signal is applied to the isolator.

4.6 The ohms amplifier produces a dc output level proportional to the direct current at its input on the ohms ranges. Like the ac converter, the dc output voltage produced by the ohms amplifier is applied to the isolator input.

4.7 The isolator functions as a buffer to prevent application of "normal-mode" noise or "common-mode" voltages to the integrator circuit. It also serves to provide a high input impedance on the low voltage dc ranges of the instrument. The output of the isolator is applied to the integrator for conversion to a digital count.

4.8 The integrator is a dual-slope conversion device which charges a capacitor for a fixed time period to a level which is dependent upon the level of the measurement signal (see figure 4.2). The capacitor is then discharged at a fixed rate by switching a reference signal of opposite polarity onto the input of the integrator. As the capacitor discharges it crosses the zero volt level and begins to charge in the opposite direction. A null detector in the integrator circuit senses this zero-crossing and produces a "null-detect" signal. The null detect signal is used by the Timing and Control circuits to stop the measurement counter. Thus, the count value in the measurement counter is a direct digital representation of the measurement signal voltage applied to the instrument.

4.9 The Timing and Control circuits provide the integrator and counter with the synchronization required to perform the analog to digital conversion of the measurement signal. The instrument performs continuous measurement cycles. The measurement cycle is illustrated in figure 4.3.

4.10 Note that the digitize cycle is divided into four major periods. The first, which is 100 milliseconds long, is the signal integrate period. During this time the Timing and Control circuits apply the measurement signal to the input of the integrator. The integrator, during this period, charges a capacitor to a level determined by the value of the measurement signal. During the next period the Timing and Control circuits apply a reference voltage opposite in polarity to the measurement signal to this capacitor in order to discharge it. The capacitor is discharged at a fixed rate and as the charge on the capacitor reaches zero the integrator produces a null detect signal which is used by the Timing and Control circuits to stop the count in the measurement counter. Thus, the value of the count in the measurement counter is directly proportional to the value of the measurement signal. During the signal integrate period the Timing and Control circuits detect the polarity of the measurement signal and store this information in a flip-flop.

4.11 The measurement counter is a special integrated circuit chip which includes the measurement counter, a latch to store the count, a decoder, and multiplexer. The measurement count stored in the latch is in BCD code and must be converted to a 7-line code for application to the LED display. This is accomplished by the 4-to-7 line decoder. The multiplexer, in the measurement counter, transfers one digit of information at a time from the latch to the 4-to-7 line decoder. The 7-line code from the decoder is applied to all of the LED display digits in parallel. The MUX switching line turns on each LED digit as its code appears on the output of the 7-line decoder. Thus, the LED display devices are actually flashing in sequence but the display rate is of a frequency that makes the LEDs appear to be continuously illuminated.

4.12 Range control is accomplished either manually from the front panel or automatically by the internal range control logic. There are three switches on the front panel of the instrument labeled UP, DOWN, and AUTO. If the operator desires to use the auto ranging feature he simply pushes in the Auto pushbutton (a latching type switch). If it is desired to use manual range control the Auto range switch is unlatched and the operator then has control through use of the UP and DOWN pushbuttons. The range control logic configures the voltage attenuator and current shunt to scale down measurement input signals. In

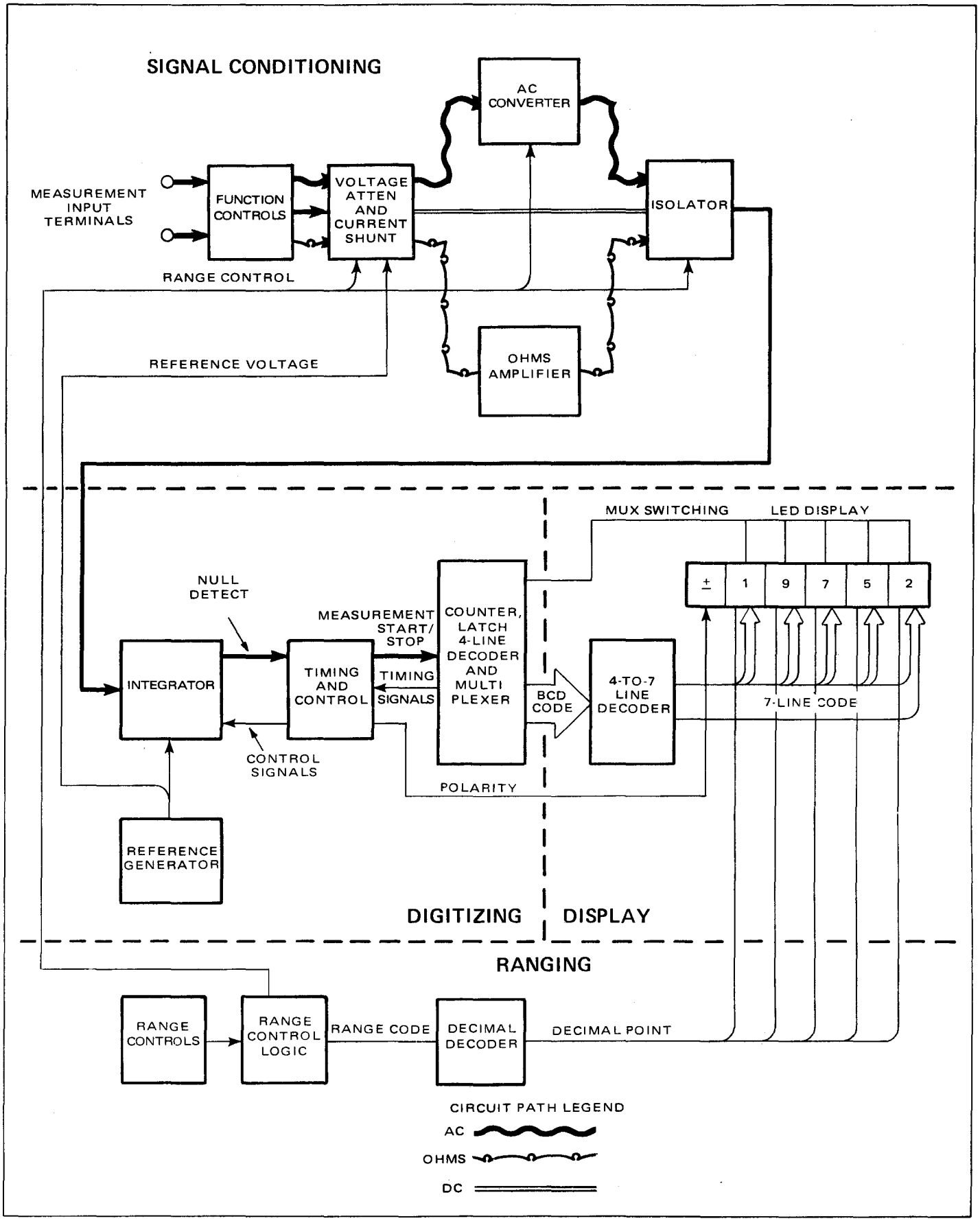

Figure 4.1 - Functional Block Diagram

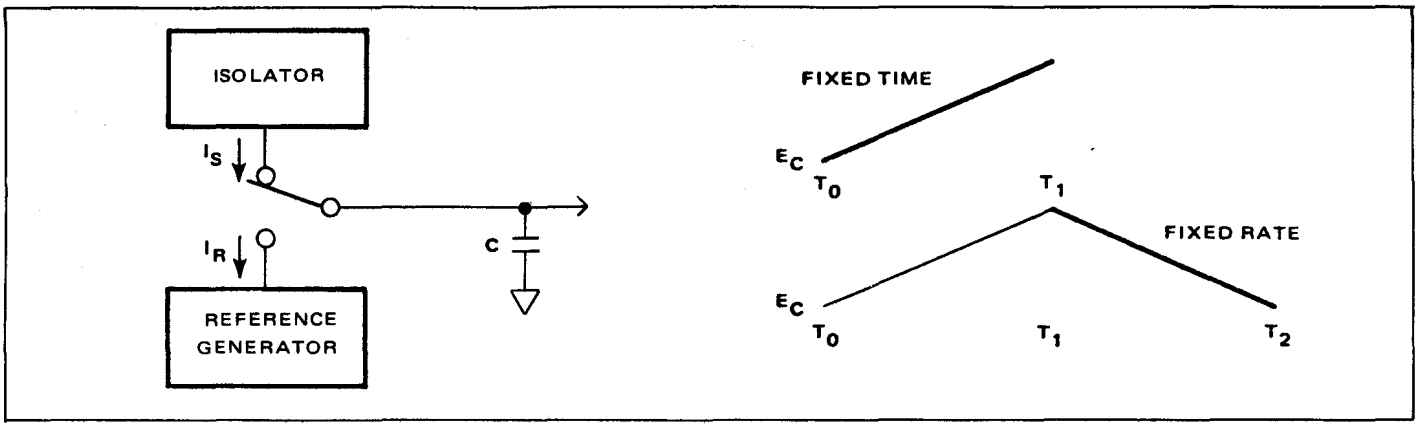

Figure 4.2 - Dual Slope Integration

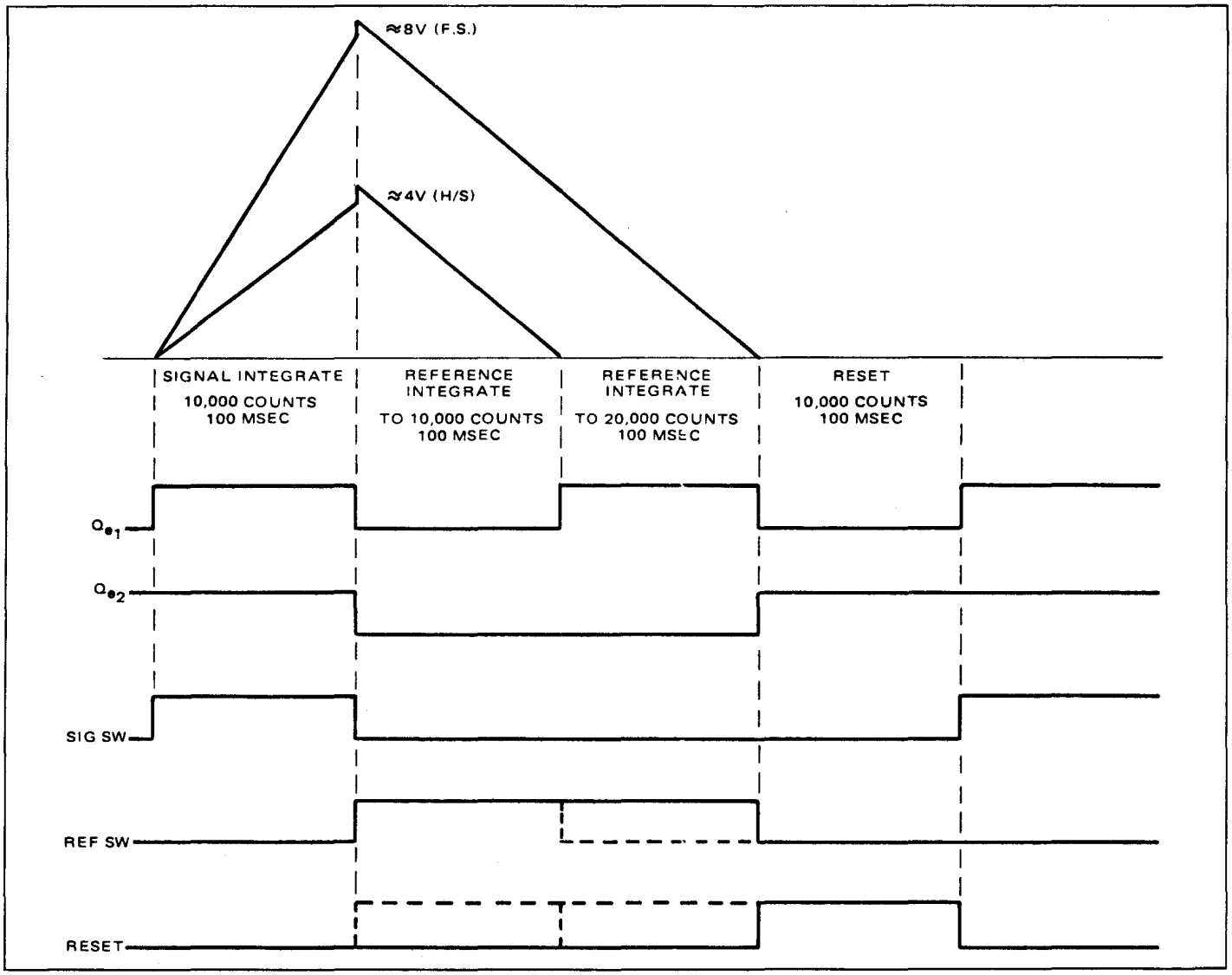

Figure 4.3 - Display Cycle Timing Using Dual Slope Integration Technique

addition, it controls the attenuator in the AC Converter circuit. The isolator gain is also controlled by the range control logic and is switched from X1 to X10 gain, depending on the selected operating range of the instrument. The range code from the range control logic is applied to the decimal decoder which provides the signals to the LED displays to properly locate the decimal point.

4.13 Function Controls.

A simplified block diagram of the function controls is illustrated in figure 4.4. The function controls consist of front panel pushbuttons labeled Milliamps, AC Volts, Kohms, and DC Volts. Note that there are two sets of input terminals for applying measurement signal to the input

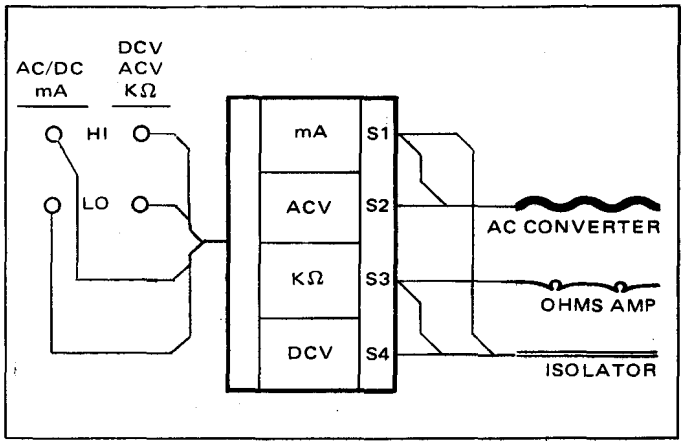

Figure 4.4 - Function Controls

of the instrument. One set of input terminals is for measurement of ac and dc milliamps. The other set of input terminals is used for measuring dc volts, ac volts and Kohms. The four function control switches route the input measurement signal through one of three paths when making ac measurements of either voltage or current. The measurement signal is routed from either set of input terminals to the input of the AC Converter. When making dc voltage or current measurements the measurement signal is applied to the input of the isolator and, in like fashion, the ohms measurement signal is routed to the input of the ohms amplifier. Although the block diagram shows that the measurement signal is applied to the input of one of these three circuits, measurement signals are actually routed through the voltage attenuator and current shunt circuits for prescaling purposes. This is discussed in more detail in the following paragraph.

4.14 *Voltage Attenuator and Current Shunt.* This circuit is shown in simplified form in figure 4.5. The attenuator and shunt circuit performs the following functions; 1) attenuation of input measurement voltages on the 20, 200, and 1000 volt dc ranges, 2) scales down the ohms current source when the instrument is on the Kohms ranges, 3) acts as a shunt when on the ac or dc current ranges, and 4) the attenuator and shunt circuit contains two series resistance strings with pick-off points selected by range relays. In figure 4.5 the left-hand resistance string is the voltage range attenuator and ohms current source divider. The right-hand resistance string serves as the ac and dc current shunt, and also has pick-off points selected by range relays. In the upper left-hand corner of figure 4.5 note that the dc measurement signal is switched around the attenuator on the low ranges and goes directly to the isolator. On the 20, 200, and 1000 volt ranges the dc measurement signal is switched onto the top of the range

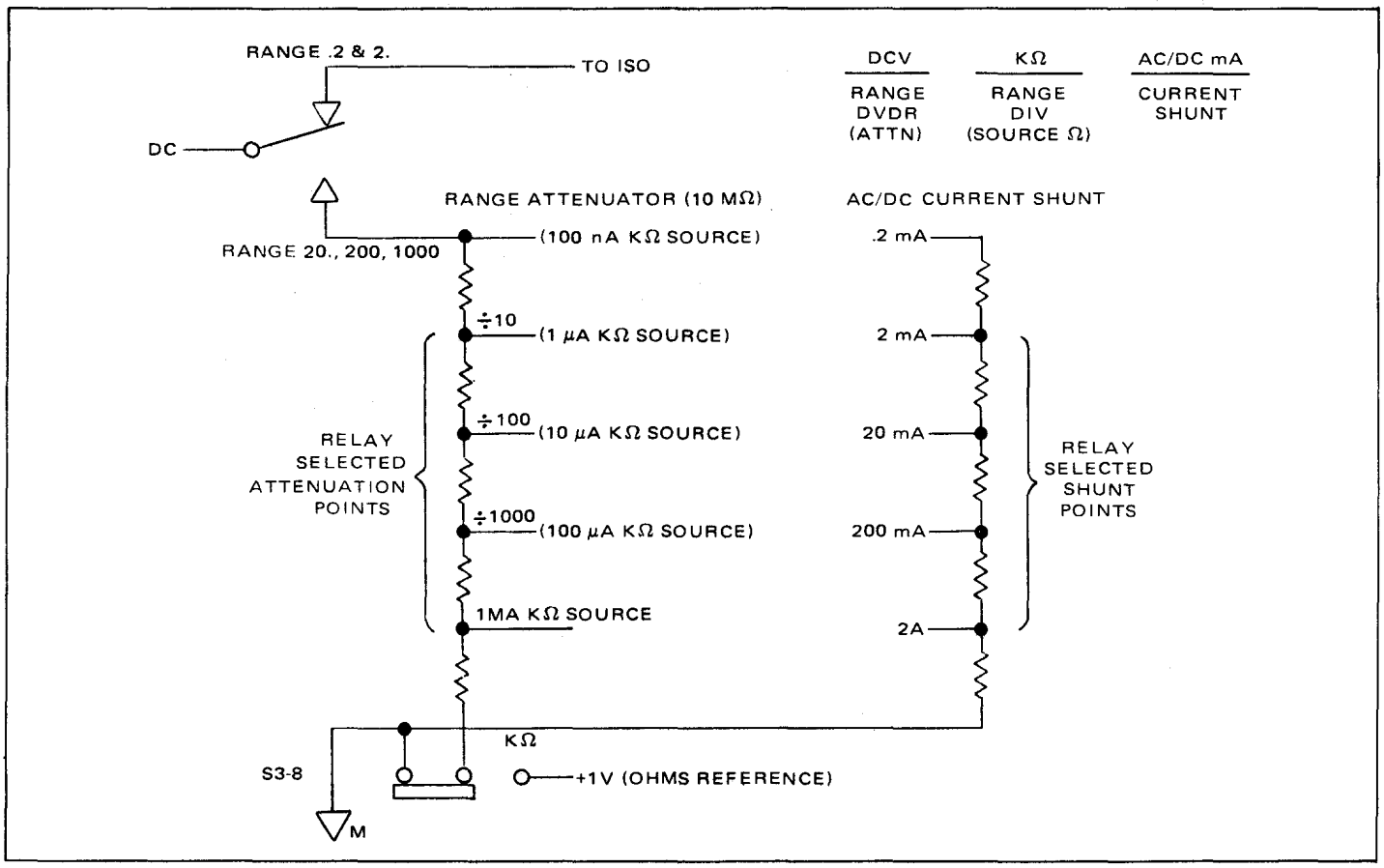

Figure 4.5 - Voltage Attenuator and Current Shunt

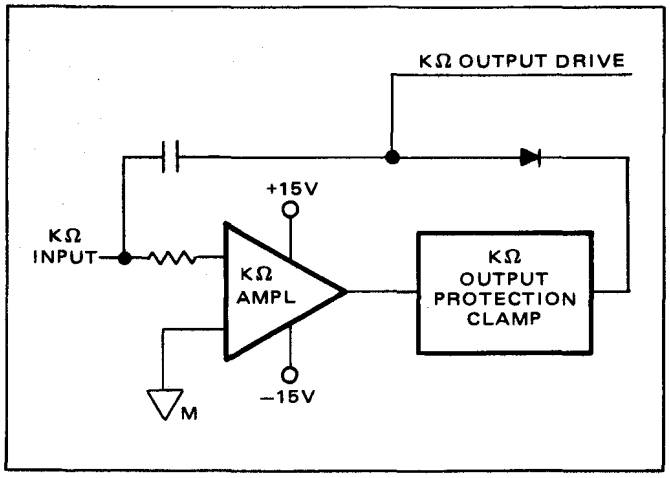

Figure 4.6 - Ohms Amplifier

attenuator resistance string. On these ranges the isolator is connected to the appropriate point on the range attenuator resistance string for prescaling.

4.15 When the instrument is used to measure ac or dc current, the measurement signal is applied to the top of the right-hand resistance string, the ac/dc current shunt. The range relays then select the appropriate pick-off point in the shunt resistance string and apply that signal to the input of the isolator.

4.16 When the instrument is used to measure resistance, S3, in the lower left corner of figure 4.5, is switched to the Kohm position and the range relays pickoff the appropriate point to apply, as a current source, to the input of the ohms amplifier. Configuration of the attenuator and shunt is thus accomplished by accommodation of the function control setting and the state-of-the-range relays.

4.17 *Ohms Amplifier.* A simplified functional block diagram of the ohms amplifier is illustrated in figure 4.6. The ohms amplifier may be viewed as a current-to-voltage converter in that it produces an output voltage directly proportional to the input current. The input current is directly proportional to the value of the resistance being measured. The output voltage produced by the ohms amplifier is always a negative voltage because the source current is derived from the positive one volt ohms reference supply.

4.18 *AC Converter.* The AC Converter is shown in simplified form in figure 4.7. As shown on the diagram it consists of an input attenuator network, a rectifier amplifier, and an output filter. The input attenuator network serves to scale down the input measurement voltage and is controlled by the range relays K1 and K2. On the .2 and 2V ranges neither of these relays is energized and the input voltage is applied directly to the rectifier amplifier. On

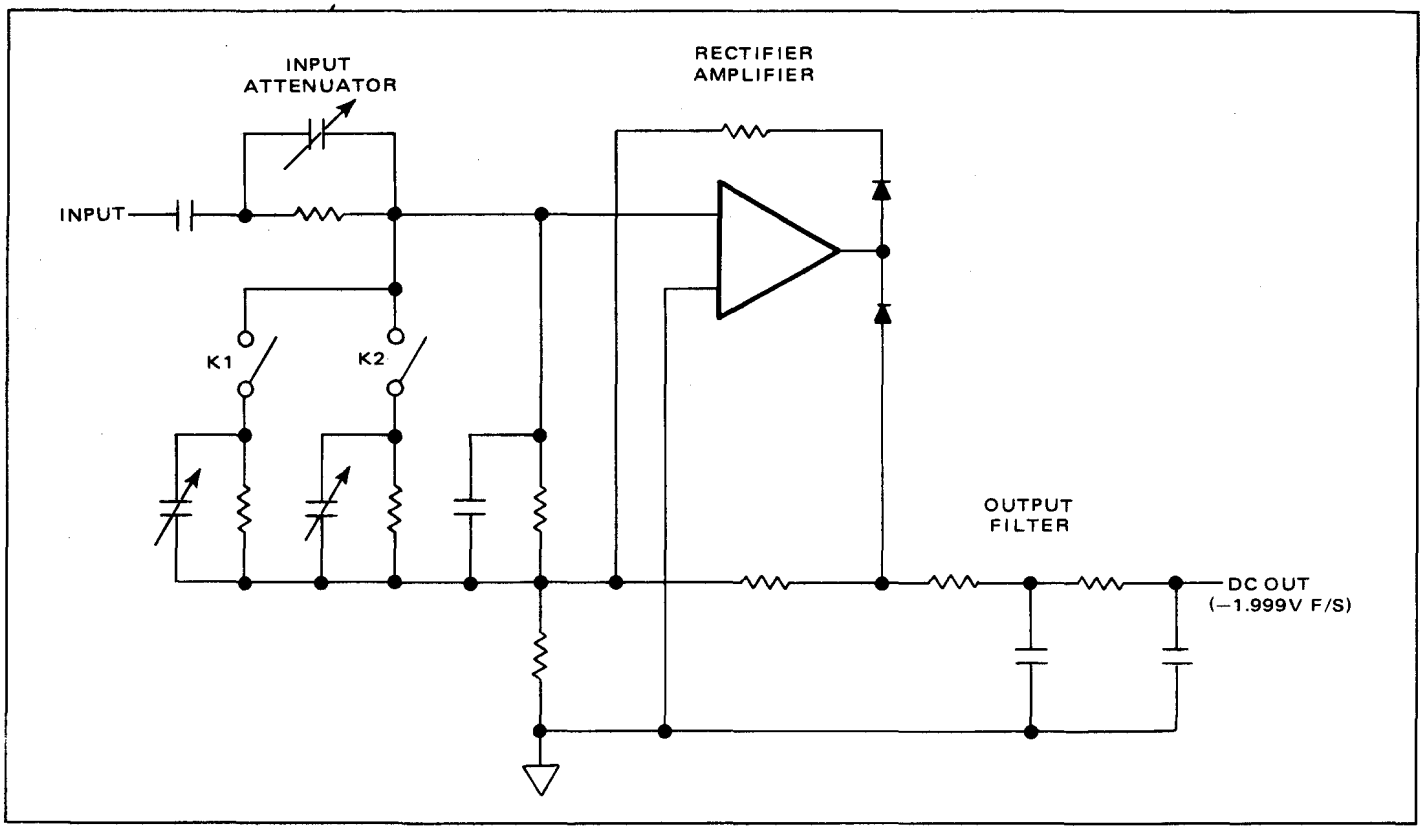

Figure 4.7 - AC Converter (Averaging)

the 20V and 200V ranges K1 is energized. It should be noted at this point that the isolator has a gain of 1 or a gain of 10, depending on the range the instrument is set. Thus, the combination of K1 and isolator gain configure the instrument on the various ac ranges. K2 is energized on the 1000V range. The rectifier amplifier consists of an operational amplifier and two rectifier diodes which convert the input measurement signal to a dc voltage which is then smoothed by the output filter network.

4.19 *Isolator.* The isolator, shown in figure 4.8, consists of an input clamp, an isolator amplifier, a bootstrap amplifier, and a gain switching network. The various prescaled and processed input measurement voltages are applied to the input of the isolator which is clamped to prevent application of more than ±5V to the input of the isolator amplifier. The isolator amplifier is an operational amplifier with a gain of 1 or a gain of 10, depending upon the control signals applied to the gain switches by the range control logic of the instrument. The isolator accepts either positive or negative voltage levels at its input on one of two ranges; (1) zero to .1999 volts or (2) zero to 1.999 volts. Because of the gain switching, controlled by the range control logic, the output of the isolator is always zero to 1.999 volts dc. Note that the negative and positive supply voltage for the isolator amplifier is supplied by the bootstrap amplifier. These voltage sources are labeled + bootstrap voltage (+ BSV) and – bootstrap voltage (– BSV). The purpose of the bootstrap amplifier is to provide the isolator amplifier with a supply voltage which is always

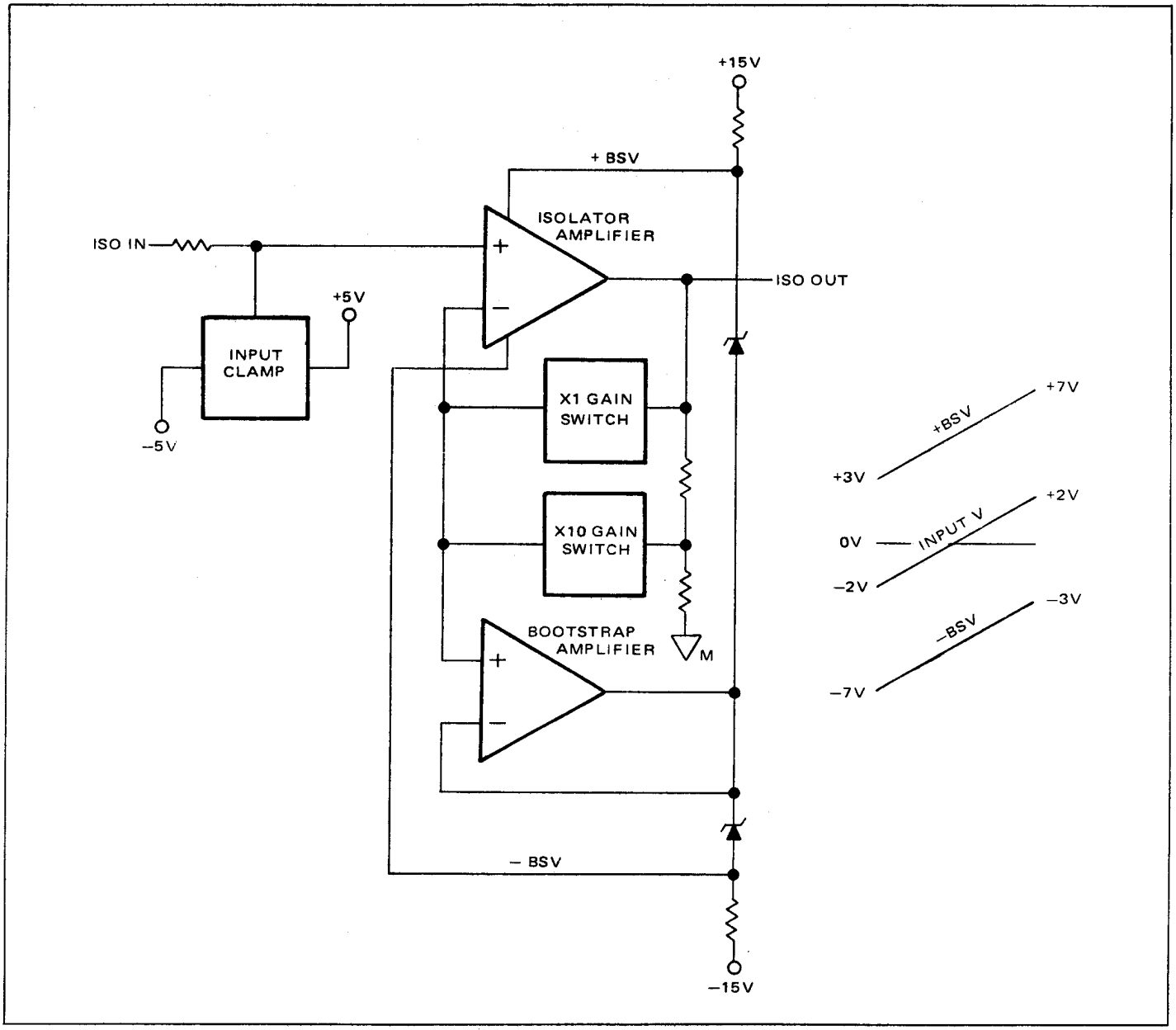

Figure 4.8 - Isolator

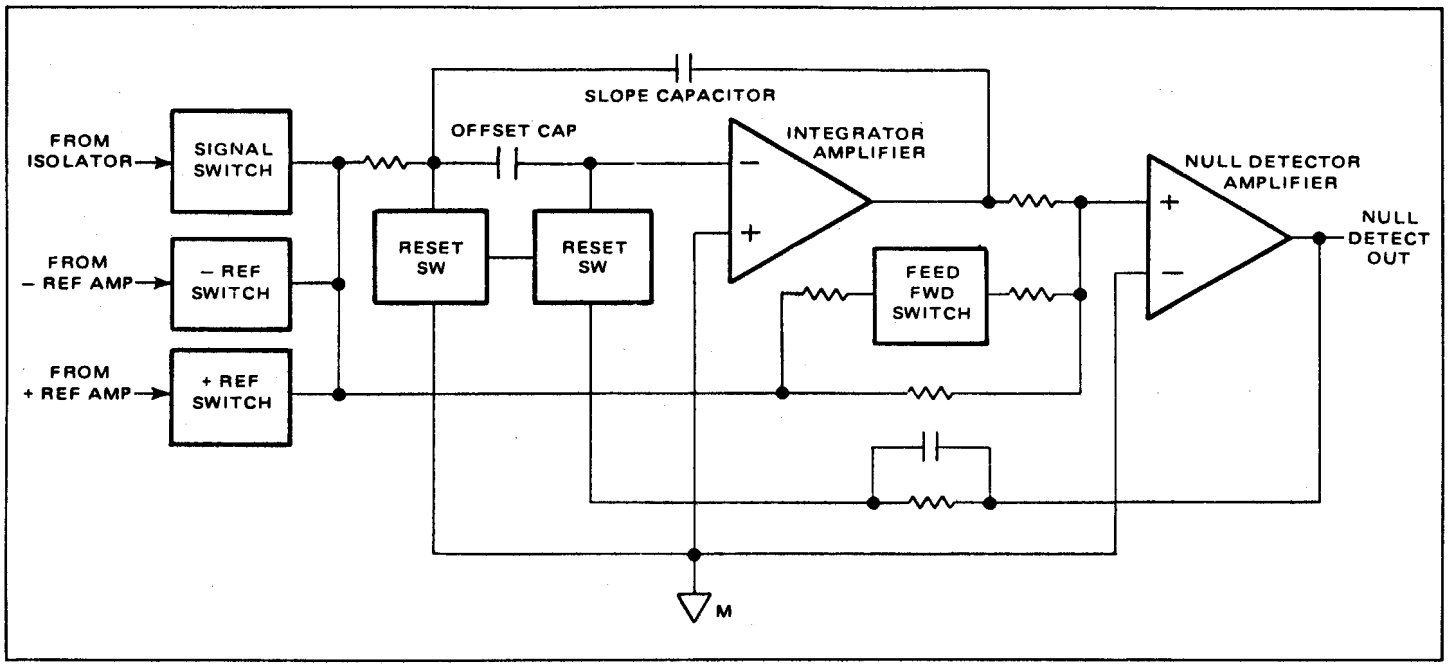

Figure 4.9 - Integrator

centered about the input measurement signal to the isolator amplifier. The + BSV voltage is always 5 volts higher than the input signal and the – BSV is always 5 volts lower than the input signal voltage. Thus, the isolator amplifier is always supplied with source voltages centered around the input signal. This combination provides high input impedance to avoid loading the circuit under test.

4.20 *Integrator.* The integrator is the circuit which performs the analog-to-digital conversion of the measurement signal and is illustrated in figure 4.9. The integrator uses the dual slope integration technique to perform the analog-to-digital conversion. Refer to figure 4.3 for the cycle timing relationships that relate to the dual slope integration. During the reset portion of the measurement cycle the two reset switches close placing the offset capacitor across the output of the null detector amplifier. This charges the offset capacitor to a level equal to any offset voltage that appears at the output of the null detector amplifier. At the beginning of the signal integrate portion of the measurement cycle the reset switches open and the signal switch closes, thus placing the offset capacitor in series with the measurement signal from the isolator at the input of the integrator amplifier. Thus a positive or negative offset voltage is added to or subtracted from the signal being measured. The output of the integrator amplifier charges the slope capacitor for a fixed period of time (100 milliseconds). The charge placed on the capacitor is dependent on the magnitude or level of the measurement signal from the isolator. Refer to figure 4.3, note that there are two slopes shown representing the capacitor charging slope; these represent two measurement levels. Note that the time is the same for the charge for both measurements but that the charging rate and the final charge level is different. From this it can be seen that the signal integrate period is always the same length but the charging rate and level of the capacitor varies with the measurement signal. At the end of the signal integrate period the feed forward switch adds a small amount of charge to the capacitor to make up for a slight delay which is incorporated to allow similar lines and circuits to settle out between the reference integrate and signal integrate portions of the measurement cycle. This causes the slope capacitor charge voltage to increase slightly. At the beginning of the reference integrate period of the measurement cycle the signal switch opens and either the – reference switch or the + reference switch closes to apply a reference voltage to the input of the integrator amplifier opposite in polarity to the voltage of the measurement signal previously applied. This reference voltage is applied to the integrator amplifier and causes the slope capacitor to discharge at a fixed rate. When the slope capacitor reaches the zero level the null detector amplifier produces a null detect pulse. Note that in figure 4.3 that for both measurements the rate of discharge was the same, e.g., the slope is the same angle. Also note that for different measurement signals input the zero crossing occurs at a different point in time. Thus, it can be seen that the time periods of the reference integrate portion of the measurement cycle is proportional to the value of the measurement signal. The output of the null detector is used by the Timing and Control circuits to stop the measurement counter. On figure 4.3 the Q_{e1} and Q_{e2} signals shown are timing signals generated by the measurement counter chip and used by the Timing and Control circuits for circuit synchronization and generation of control signals.

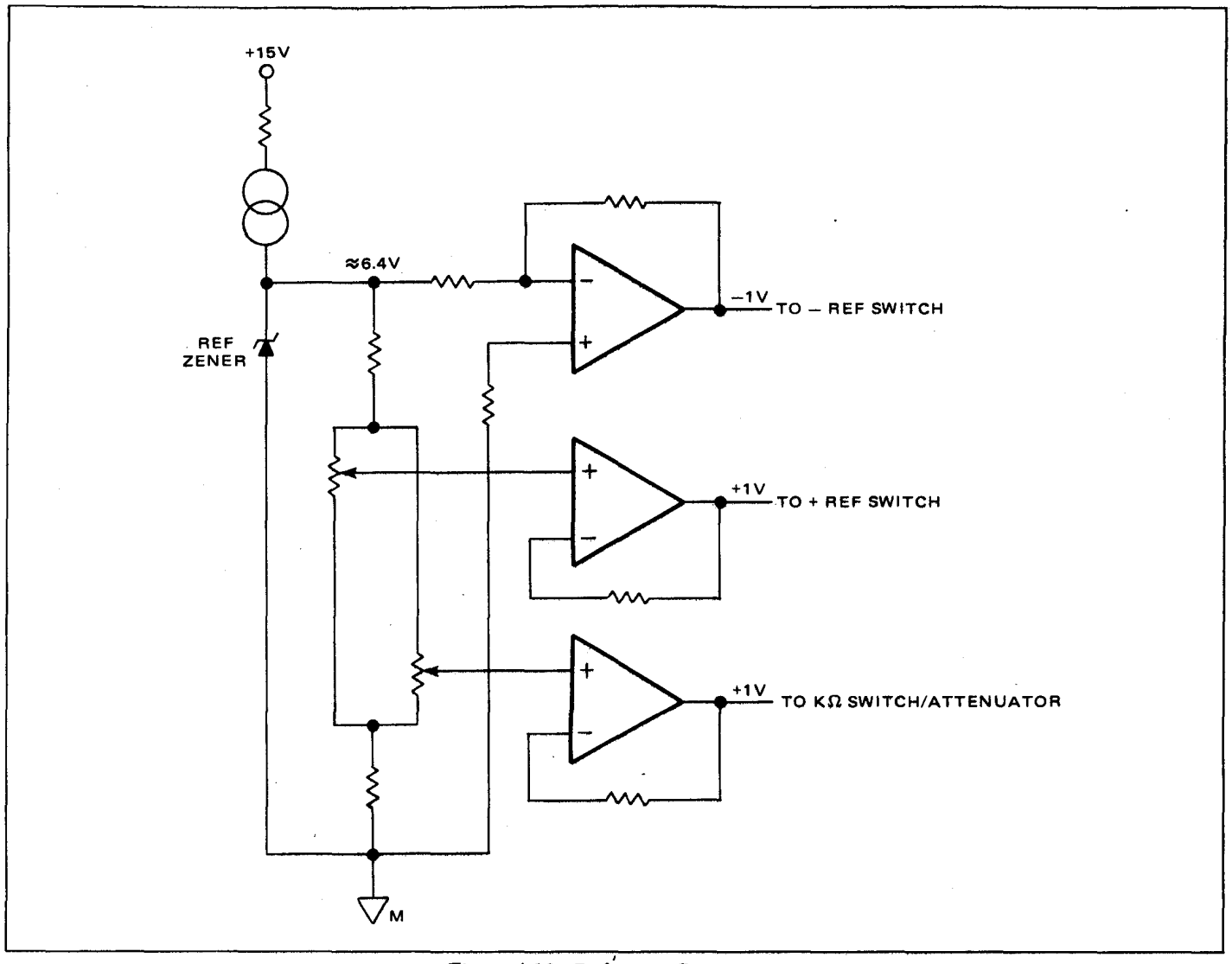

Figure 4.10 - Reference Generator

4.21 *Reference Generator.* The reference generator is the source of the + and – reference voltage used by the integrator and of the +1V source used for ohms measurement at the voltage attenuator and current shunt circuit. The reference generator is illustrated in figure 4.10. The reference device is a selected high stability zener diode operated at its zero temperature coefficient current. It produces approximately 6.4V. As shown in figure 4.10, this 6.4V is applied across a voltage divider network which provides the reference input to three operational amplifiers. The –1V reference amplifier is configured with feedback calculated to cause it to produce exactly –1V dc output for the – reference source. The other two 1V reference amplifiers are connected to a voltage divider through potentiometers which are adjusted to provide +1V dc from the reference source. These two amplifiers are operated at unity gain, are non-inverting, and produce a positive 1V dc output.

4.22 *Timing and Control Circuit.* Operation of the 4600 is controlled by the Timing and Control circuits (figure 4.11, block diagram). These circuits provide synchronization and control signals which control the sequence of operation referred to as the measurement cycle. Figure 4.12 illustrates the measurement cycle timing. Note that the timing waveforms in the upper portion of the figure illustrate timing and polarities for a positive measurement signal while the lower portion illustrates the negative input example.

The differences between the upper and lower portions of the figure are the polarity of the input signal, the integrator slope and polarity, the timing of signal switch, reference switch and reset switch. The following description of the operation of the timing and control circuits refers to the simplified block diagram (figure 4.11) and the timing chart (figure 4.12).

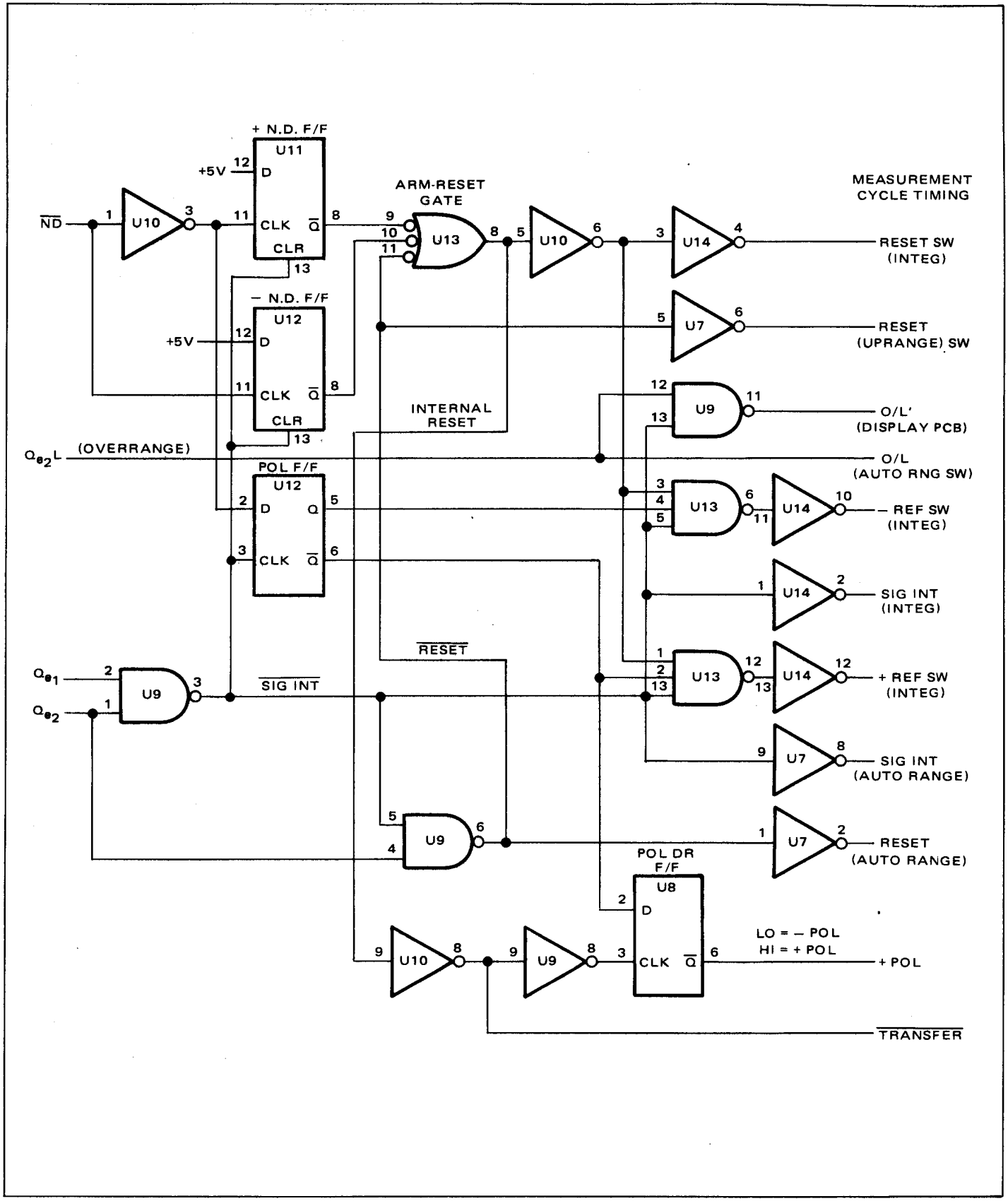

Figure 4.11 - Timing and Control Circuit, Simplified Block Diagram

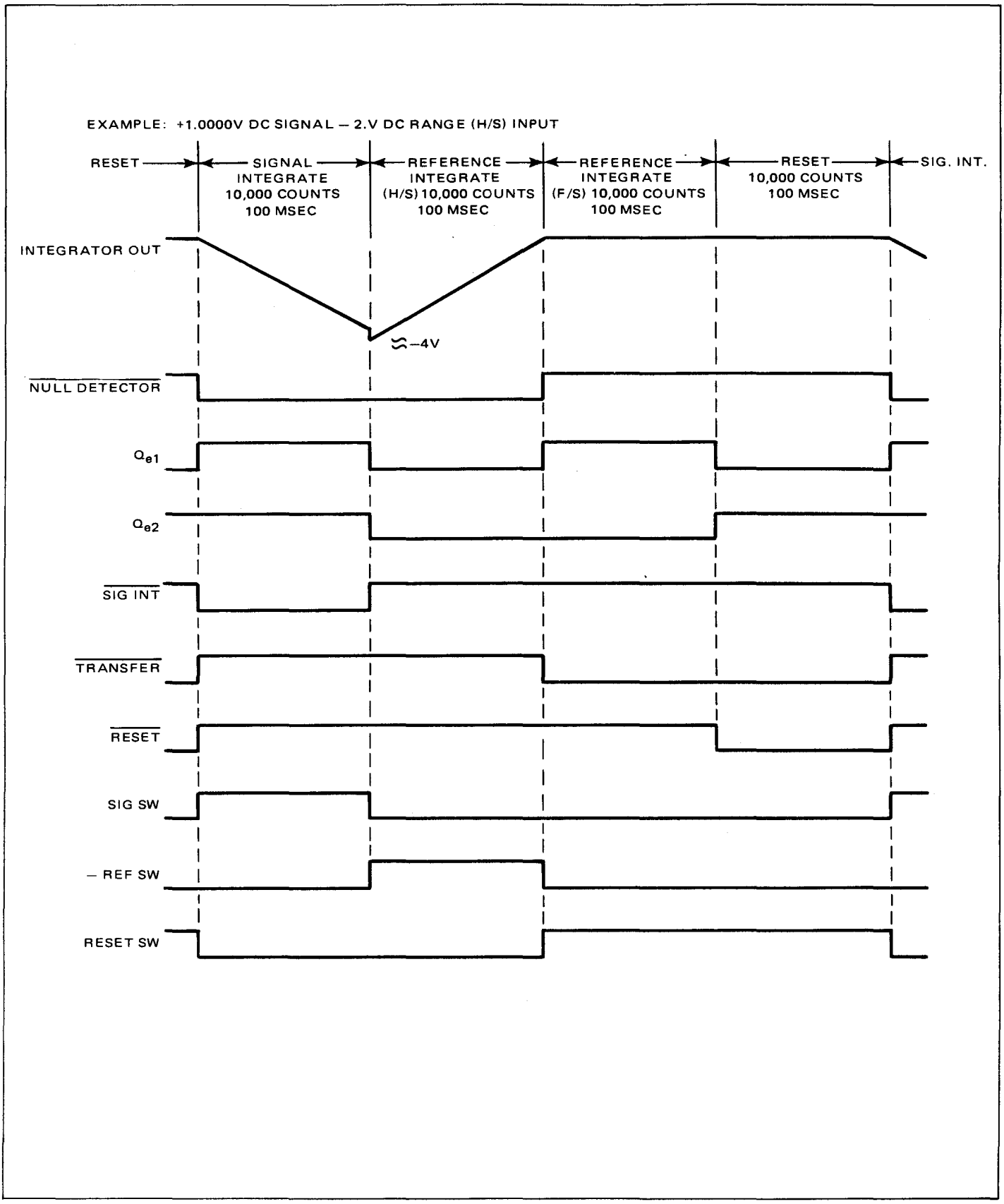

Figure 4.12 - Measurement Timing Cycle

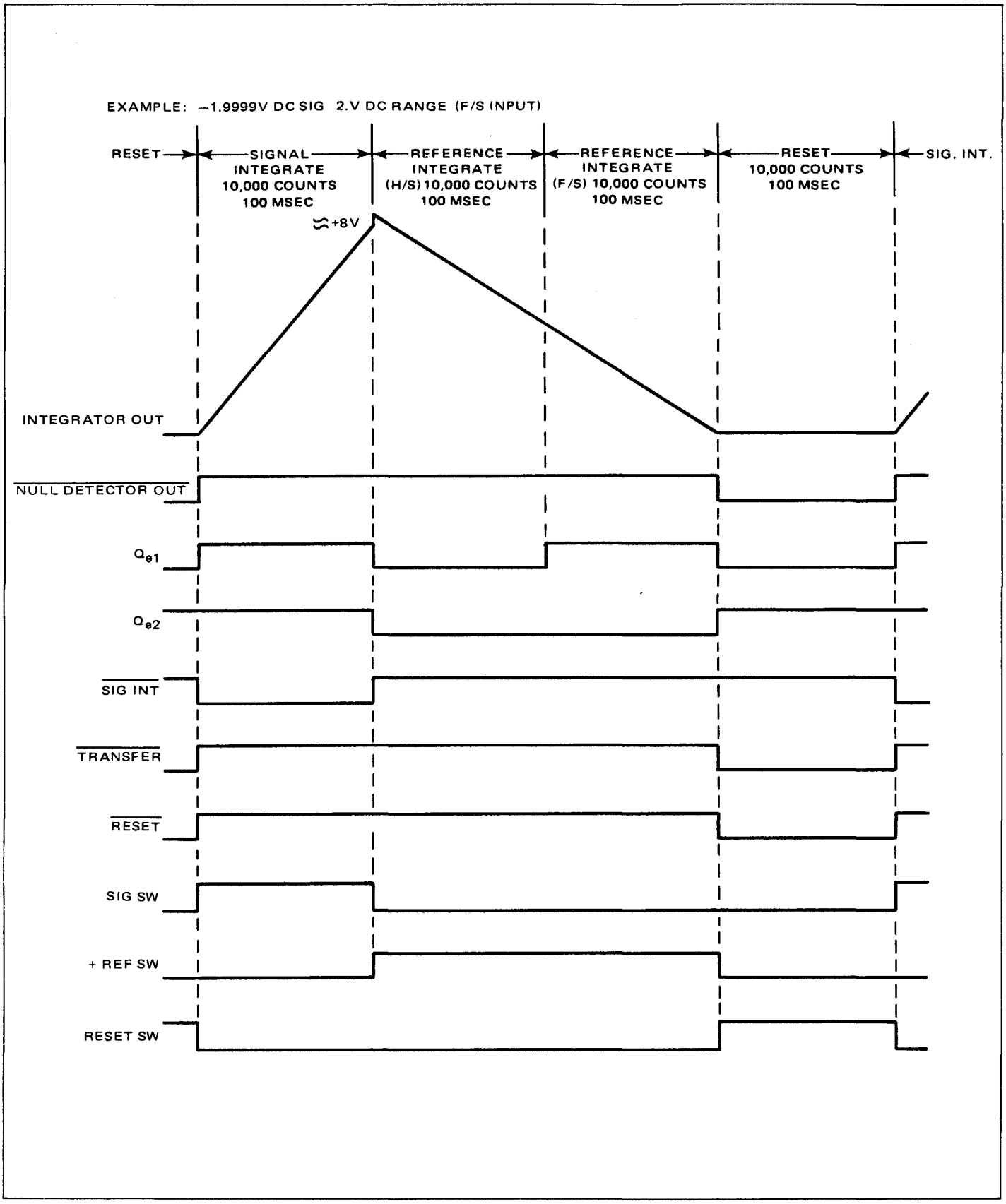

Figure 4.12 - Measurement Timing Cycle continued

Table 4.1 - Sequence Chart

+ Signal = 1.0000V DC, 2. Range

Q_{e1} = High, Q_{e2} = High	(1)	$\overline{\text{SIG INT}}$ goes low
	(2)	+ N.D. F/F (U11) $\bar{Q}$ goes high
	(3)	– N.D. F/F (U12) $\bar{Q}$ goes high
	(4)	$\overline{\text{RESET}}$ goes high
	(5)	INTERNAL RESET goes low (caused by 2, 3, 4)
	(6)	$\overline{\text{TRANSFER}}$ goes high (Armed for digitizing sequence)
	(7)	RESET SW goes low (releases sw's from Auto Zero)
	(8)	SIG SW goes high (connects iso out to integrator in)
	(9)	NULL DETECTOR OUTPUT goes low (to detect polarity)
	(10)	POL F/F Q OUTPUT goes high (to enable – ref sw @ ref int)
		POL F/F $\bar{Q}$ OUTPUT goes low (set pol dr F/F $\bar{Q}$ output high)
Q_{e1} = Low, Q_{e2} = Low	(1)	$\overline{\text{SIG INT}}$ goes high
	(2)	SIG SW goes low (disconnects iso out from integrator in)
	(3)	– REF SW goes high (connects –1V ref to integrator in)
Q_{e1} = High, Q_{e2} = Low	(1)	NULL DETECTOR OUTPUT goes high (zero detect)
	(2)	+ N.D. F/F (U11) $\bar{Q}$ goes low (causes internal reset to go high)
	(3)	INTERNAL RESET goes high (causes $\overline{\text{transfer}}$ to go low)
	(4)	$\overline{\text{TRANSFER}}$ goes low (signals CMOS counter to stop count)
	(5)	– REF SW goes low (disconnects –1V ref from integrator in)
	(6)	RESET SW goes high (closes reset switches – Auto Zero)
Q_{e1} = Low, Q_{e2} = High	(1)	RESET SW is high (Auto Zero)

In addition to the illustrations, a sequence chart is presented in table 4.1. This chart is a synopsis of the sequence of operation of the timing and control circuits for one measurement cycle. Its basic purpose is for reference after reading the detailed description presented in the following paragraphs. It will also serve as a handy reference to use while reading the detailed description.

Four timing segments are established by the CMOS chip, 3814 counter, on the Display PCB. With an internal clock frequency of 100 kHz, these four timing sequences are exactly 100 msec in duration. They are established by the output of the last counter bit (1/2 decade), Q_{e1} and Q_{e2}. The timing sequences are as follows:

$Q_{e1} = 1, Q_{e2} = 1$

100 msec, count from 30,000 to 39,999 called $\overline{\text{Signal Integrate}}$

$Q_{e1} = 0, Q_{e2} = 0$

100 msec, count from 00,000 to 09,999 called reference integrate. This count total limit is referred to as half-scale

$Q_{e1} = 1, Q_{e2} = 0$

100 msec, count from 10,000 to 19,999 called reference integrate. This count total limit is referred to as full-scale

$Q_{e1} = 0, Q_{e2} = 1$

100 msec, count from 20,000 to 29,999 called reset (fixed)

In the following example, a +1.0V dc input signal is applied to the isolator amplifier input. The isolator, at a gain of 1, has an output voltage of +1.0V dc. When the signal integrate period is detected, this +1.0V dc is applied to the integrator input, resulting in a negative going slope, to approximately –4.0V at the end of the 100 msec period. The null detector input senses the negative integrator slope voltage and causes the null detector output to go to a negative TTL level. The null detector low output is inverted through U10 and applied to U12-2, the D input of the polarity F/F. This causes U12-6, the $\bar{Q}$ output to be logic low, which when applied to the D input of the polarity drive F/F, U8-2, causes the $\bar{Q}$ output, U8-6 to be logic high to annunciate the "plus" symbol on the readout.

At the start of the signal integrate sequence, the output of U9-3, $\overline{\text{signal integrate}}$, goes logic low. This logic level is applied to the "clear" inputs, pin 13, of U11 and U12. This causes the $\overline{Q}$ outputs of U11 and U12 to go logic high, which is applied to the inputs of U13, pins 9 and 10 respectively. $\overline{\text{Signal integrate}}$ at a logic low causes the output of U9-6 to go logic high, which is also applied to the pin 11 input of U13, which results in the output U13-8 to be at logic low and when inverted through U10 causes the output at pin 8 to be logic high. This signal is called $\overline{\text{transfer}}$. When the start of signal integrate occurs, $\overline{\text{transfer}}$ must go to a logic high (ARMED), so that when a zero crossing (null detect) occurs the falling edge of $\overline{\text{transfer}}$ signals the CMOS 3814 counter that the BCD count is to be terminated and transferred to the latches for multiplexing to the readout segments in digit sized bytes.

When $\overline{\text{signal integrate}}$ is at a low state, at the beginning of a digitize sequence, it is inverted through U14 to drive the bi-lateral signal switch, U16A, to connect the isolator output to the integrator input, that starts the integrator output to ramp in a negative slope for a period of 100 msec.

At the start of signal integrate, when the output of U13 pin 8 goes low; this is inverted through U10-6 and U14-4 that drives the reset bi-lateral switches, U16B and U16C, to release the integrator from the reset state called "Auto Zero."

At the end of $\overline{\text{signal integrate}}$, U9-3 goes logic high, that when inverted through U14, disables the signal bi-lateral switch, disconnecting the integrator input from the isolator output. As previously mentioned, the Q output of the polarity F/F, U12-5 is at a high state. Also the output of U13 pin 8 is logic low, which when inverted through U10 applies logic high levels to the three inputs of U13, causing the output at pin 6 to go logic low. This inverted output drives the "–" reference bi-lateral switch, U15C; connecting a –1.0V dc to the integrator input during the second sequence called reference integrate, whose purpose is to drive the integrator output signal back to a zero level. When the zero is detected, the output of the null detector changes to a high state; which, when inverted through U10, causes a low level at the clock input, pin 11 of U11, of the Plus Signal Detect F/F, whose $\overline{Q}$ output goes logic low, causing the output of U13 pin 8 to go logic high. This output, double inverted, causes the reset bi-lateral switches, U16B and U16C, to close; placing the integrator in a configuration called "Auto Zero." The inverted output of U13 pin 8 also causes the $\overline{\text{transfer}}$ to go to a logic low that signals the termination of the clock count in the CMOS 3814.

At this point, the digitizing sequence is only at the end of sequence 2, but because a zero detect (null detect) has been sensed, the next sequence, state 3, is an "internal" reset until sequence 4, which is a fixed reset sequence.

If a null detect is sensed, during sequence state 2, before 1000 counts (5% of range), and the DMM is not on the lowest range (in auto range) a down range is commanded.

If a null detect is not sensed before 19,999 counts is accumulated in the CMOS 3814, an "overload" is annunciated on the readout, flashing 20000, for a manual range or highest range per function. If the DMM is in auto range and overload is sensed, the range counter, U4 is advanced one range. This is a result of the Q_{e2} output of the CMOS 3814 counter, which is latched as an output called $Q_{e2}L$. When null detect has not been sensed and the 4th sequence is detected as the fixed reset period the $Q_{e2}L$ line goes logic high to detect "overload" or "up range."

If the input signal to the DMM is of negative polarity, the inverted output of the null detector is applied to the polarity F/F "D" input at U12-2, which now causes the $\overline{Q}$ output at pin 6 to be logic low to be applied to 1) U13-2 to enable the Plus Reference bi-lateral switch when the reference integrate sequence two is entered and 2) U8-2, "D" input to the Polarity Drive F/F to cause the $\overline{Q}$ output of U8 pin 6 to be logic low or minus polarity.

The output of the null detector, for a negative input signal, goes to a logic low level when zero detect is sensed, this causes the $\overline{Q}$ output, pin 8 of U12, to go logic low causing the $\overline{\text{transfer}}$ to go logic low, terminating the CMOS count.

4.23 *Counter.* The heart of the instrument is the 3814 Digital Voltmeter logic array, shown on figure 4.1 as the counter, latch, 4-line decoder, and multiplexer. A more detailed illustration of this device is shown in figure 4.13. It contains four full decade counters, two overflow latches, an underrange output, an overrange output, outputs to drive a BCD to seven segment converter, and decoded outputs to strobe the display. The 3814 counts four full digits and the overrange digit. The 100 kHz clock drives the CP input to the 3814 chip. The decade counters change state on the rising edge of the clock pulse.

4.24 The output of the second decade is gated with the clock pulse to provide a divide-by-one hundred (÷100) output. This clock pulse is used to drive the step input of the 3814 and a synchronous timing pulse for the data output/programming operations. The step input clocks a ring counter that drives the multiplexer.

4.25 The 1 output of the fourth decade counter in the 3814 is buffered and used as a divide-by-two thousand

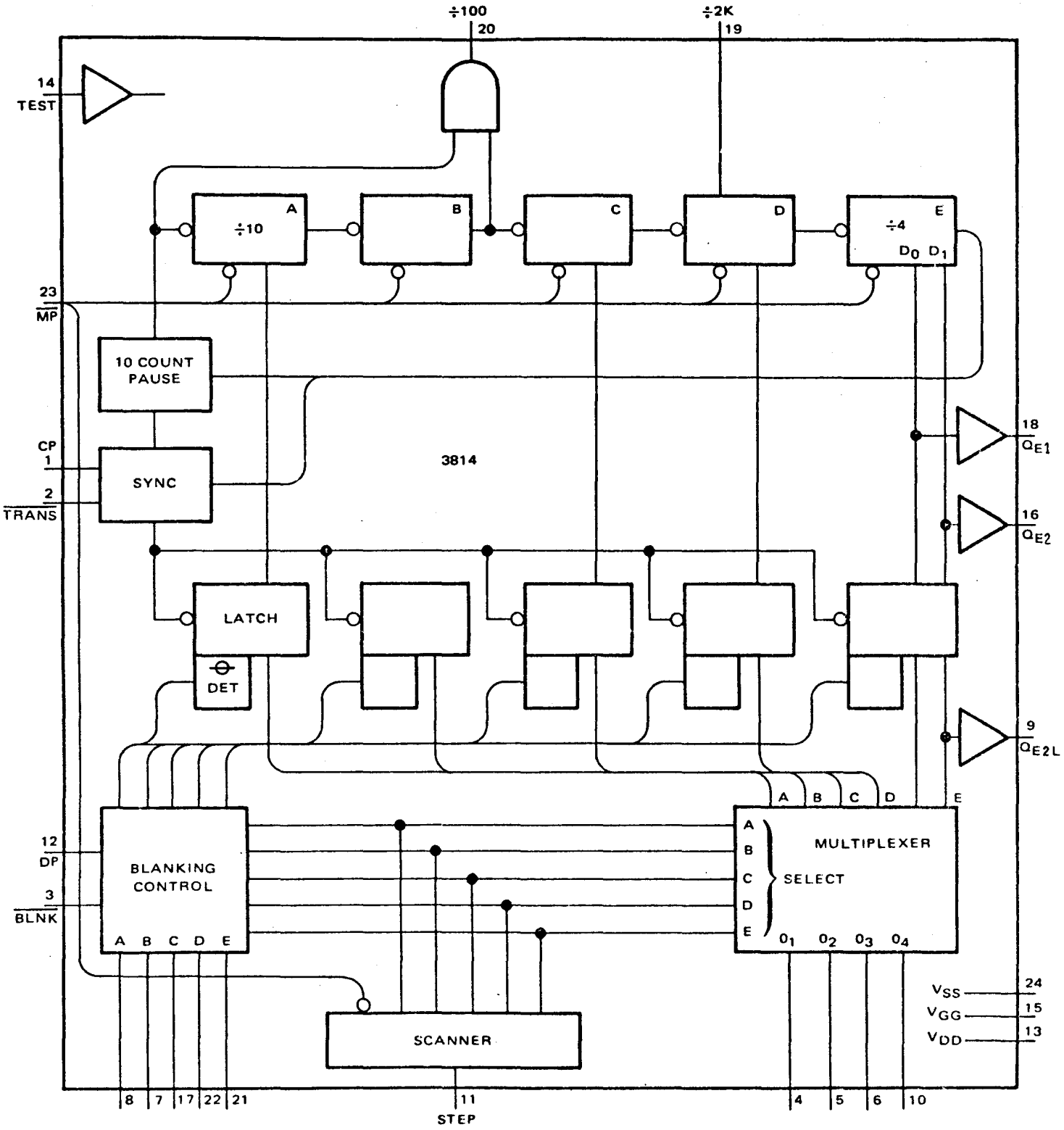

Figure 4.13 - Logic Array

(÷2,000) output. This output is used to indicate a signal that is less than 5% of full scale. If the transfer pulse is enabled before the divide-by-2,000 output goes high the output will signal the auto range circuitry that a range change must be made.

4.26 The Q0 and Q1 flip-flop outputs of the 5th counter are designated as Q_{e1} and Q_{e2} outputs. These outputs step the DMM through the various periods of the integration process. The signal codes are:

Q_{e1}	Q_{e2}	
1	1	100 ms – Signal integration – decade counts from 30,000 to 39,999
0	0	100 ms – Reference integration – decade counts from 00,000 to 9,999 H/S
1	0	100 ms – Reference integration – decade counts from 10,000 to 19,999 F/S
0	1	100 ms – Reset – decade counts from 20,000 to 299,999

4.27 The Q_{e2} output is latched and used as the $Q_{e2}L$ output. If a DMM uses a full scale count of 19,999 using the 3814, the high state of $Q_{e2}L$ is used to indicate an overrange condition. The $Q_{e2}L$ output causes the display to read 20,000 at a flashing rate.

4.28 The edge sensitive transfer input causes the BCD data in the counters to be stored in the latches on the falling edge. Synchronization with the clock is necessary to prevent loading and storing erroneous counter states at a "carry" is trickling through the counters. A transfer command is accepted once during an integration cycle. An internal flip-flop is reset by the counter transition from 39,999 to 00,000. It is set when a transfer occurs and remains set until the next integration sequence. No transfers will be accepted when this flip-flop is set.

4.29 The clock pulse is constantly adding counts to the counter. As previously mentioned the states of Q_{e1} and Q_{e2} control the state of events that take place during an integration sequence.

4.30 $Q_{e1} = 1$ and $Q_{e2} = 1$. The counter advances from 30,000 to 39,999. This is the signal integration period. At this time the DMM input signal which has been attenuated, amplified, converted, and/or filtered and connected to the integrator input through a bi-lateral switch. The feed forward circuit of the integrator adds 10 digits of voltage to the integrator output to mask the switching transients that occur during the transitions from signal integrate to reference integrate.

4.31 $Q_{e1} = 0$ and $Q_{e2} = 0$. During this period the signal switch is turned off and a reference (plus or minus) is connected to the input of the integrator through a bi-lateral switch. The decade counter is set to 00,000 and the 3814 will ignore the next 10 counts. Because of the 3814, the first 10 counts are ignored. This period allows for masking the noise at the time when the signal integration is switched to the reference integration to prevent false zero detection at or near zero analog input signals. The count is started from 00,000 until the null detector crosses zero and signals the end of the reference integration period. Zero detect signals the transfer input to store the BCD count of the decade counters into the latches. If the transfer occurs before the ÷2000 output goes true, the signal is less than 5% of full scale and a down range is commanded if the DMM is in auto range.

4.32 $Q_{e1} = 1$ and $Q_{e2} = 0$. This reference integration period is from 10,000 to 19,999 which is the F/S capability of the DMM.

4.33 $Q_{e1} = 0$ and $Q_{e2} = 1$. This is the reset period when the analog and reference inputs to the integrator are removed and bi-lateral switches short the integrator input to the output in a configuration called auto zero. The count of this period is from 20,000 to 29,999. If the $Q_{e2}L$ output goes true before zero detect signals a transfer, an uprange is commanded if the DMM is in auto range and/or overload is detected and the display indicates overrange.

4.34 The step input from the ÷100 output presents the multiplexed BCD outputs capable of driving a single decoder/driver, such as a SN7447. The decoded outputs 0_a to 0_e drive transistor circuitry that strobes the anodes of the display devices one at a time.

4.35 *4-to-7 Line Decoder.* The 4-to-7 line decoder is shown on figure 4.14. This device is simply a matrix decoder that converts BCD code to 7-line code for display purposes. It's driven by the BCD code from the 3814 counter chip and its 7-line output is tied in parallel to all of the display LEDs.

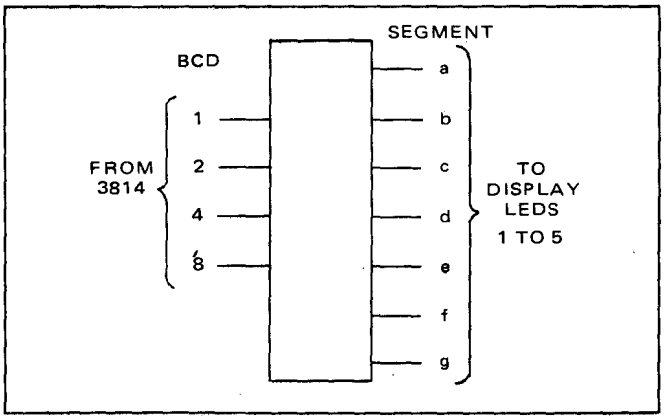

Figure 4.14 - 4-to-7 Line Decoder

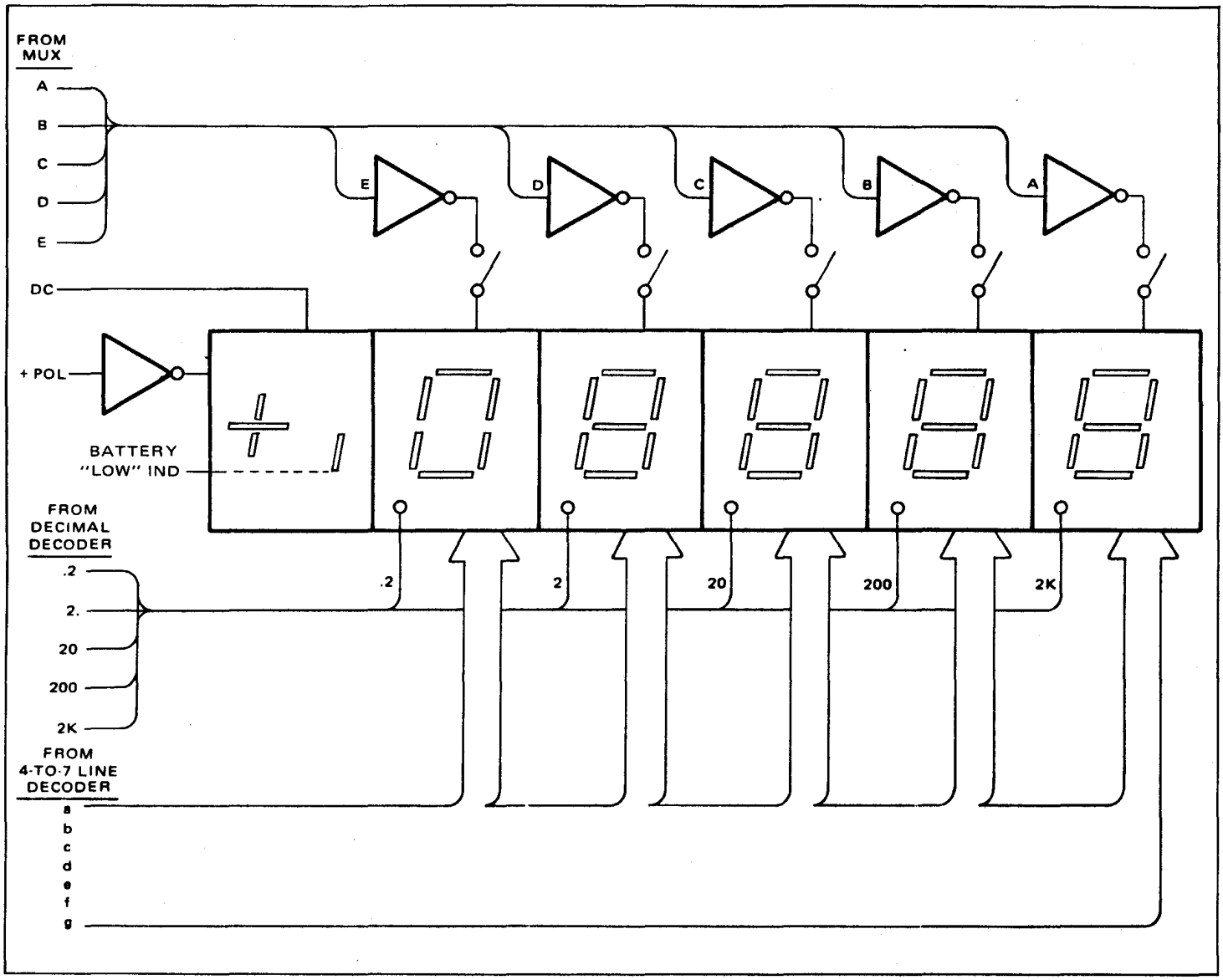

Figure 4.15 - LED Display

4.36 *LED Display.* A functional diagram of the display circuit is shown on figure 4.15. The display consists of five 7-bar LED display devices and the polarity display device. The output of the 7-segment decoder is tied in parallel to the inputs of the five 7-line display devices. When the digit code and 7-bar form is on the line for the low order digit display device the multiplexer in the counter chip will energize the enable line A and the device will display the numeric value on the 7-line bus at that time.

The counter then changes the code on the output bus to the next digit and the multiplexer energizes the strobe line B. This is repeated until all the codes have been displayed on the display devices and the sequence begins again with the lower digit. The LEDs are illuminated only as long as the strobe lines A through E from the multiplexer are energized. However, this display strobe frequency is such that the LEDs appear to be continuously lit due to the persistence characteristic of the human eye. The decimal output from the decimal decoder is applied directly to the appropriate display device. The polarity signal is applied to the polarity display LED. The polarity signal is detected and produced by the Timing and Control signals and is shown on figure 4.1.

4.37 *Range Control Logic.* The range control logic is illustrated in simplified form in figure 4.16. The range control circuits control the gain of the isolator, the attenuation in the AC Converter and the attenuation in the voltage attenuator and current shunt circuits. In addition, the range control circuits provide a range code to the

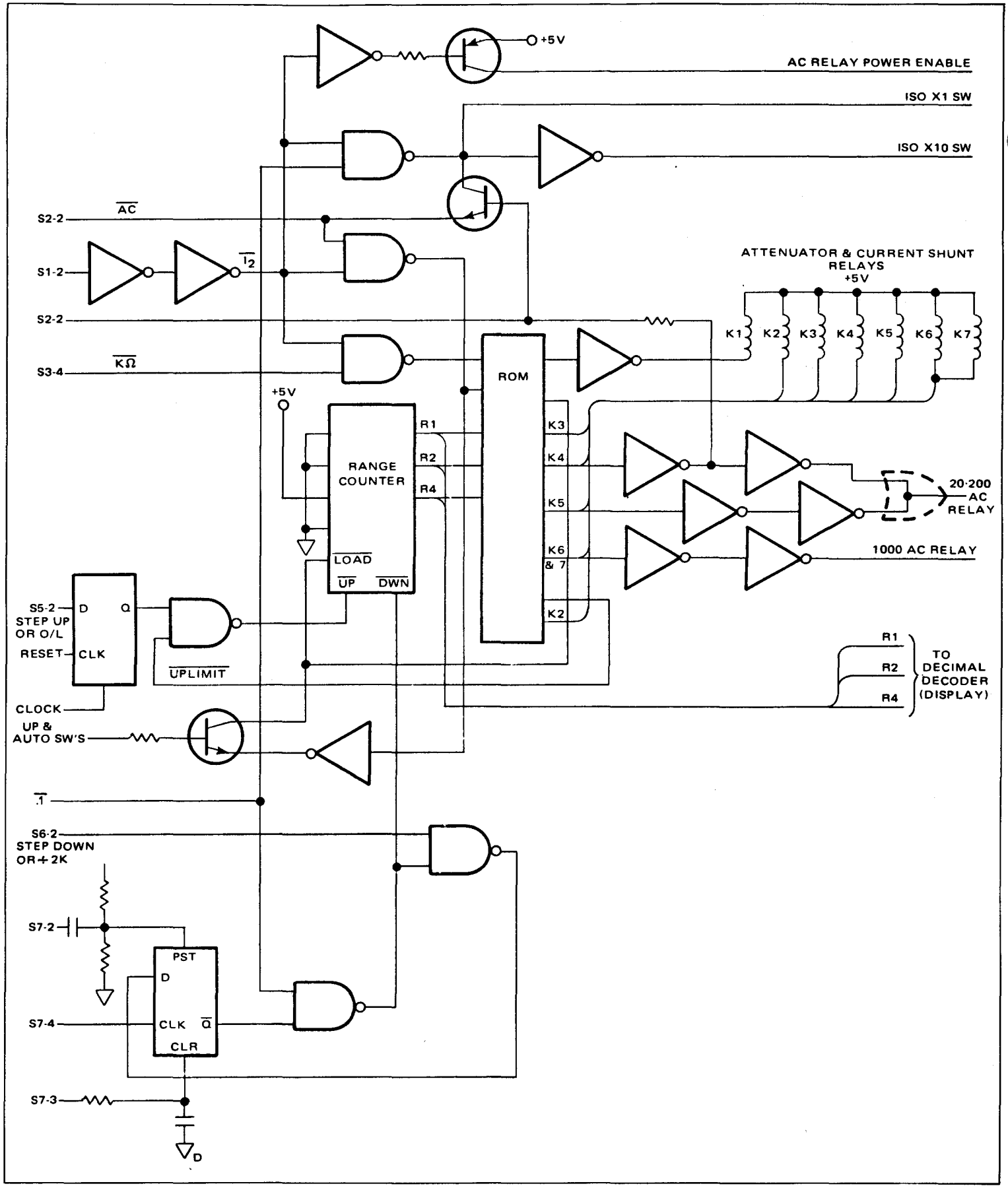

Figure 4.16 - Range Control

decimal decoder for positioning of the decimal point on the front panel display. The heart of the range control circuits is the range counter, a three state UP/DOWN counter controlled by a pair of UP/DOWN flip-flops. When the range is to be stepped up manually the switch closure from S5-2 in combination with the clock applies a pulse to the UP input of the range counter, thereby increasing the count. Manual down ranging is accomplished in exactly the same way by a switch closure from S6-2 when the DOWN pushbutton is depressed. In auto range, the same UP or DOWN flip-flops are set by two signals which come from the counter. If the counter reaches a count which is greater than 100% of the measurement count prior to the null detect it produces an overload (O/L) signal. This signal is applied to the step-up flip-flop and causes the range counter to step up one count. If the null detect signal should occur before the counter reaches the 5% point in its count a signal termed divide by 2K (÷2K) is produced indicating that the measurement is less than 5% of full scale. This divide by 2K signal is applied to the step-down flip-flop, which causes the range counter to count down one step. Thus, the manual pushbuttons, or the internal logic, cause the range counter to step to the proper range and produce the range codes R1, R2, and R4. The range code has applied to the decimal decoder to locate the decimal point on the front panel display. In addition the range codes are applied to the read-only memory, which is configured by internal firmware, to produce relay control signals which configure the attenuator and current shunt relays. The isolator gain is controlled by the range counter, read-only memory, and by the switch positions of the function control switches on the front panel.

SECTION 5 MAINTENANCE

5.1 INTRODUCTION.

5.1.1 This section contains information necessary to check the calibration of the Model 4600, perform calibration adjustments and to troubleshoot the instrument in case of malfunction. The calibration checks are also used for receiving inspection or specification validation purposes. This maintenance information is organized to provide for two levels of maintenance.

5.1.2 The section is divided into three major subsections; (1) Calibration Checks, (2) Calibration Adjustment and (3) Troubleshooting Performance Tests. The troubleshooting is further divided into Unit Performance Tests and Subassembly Performance Tests. The unit level performance tests are designed to check the instrument by function, such as AC Volts, and enable isolation of a malfunction to a replaceable module or subassembly. The subassembly performance tests are designed to check the operation of a module or subassembly and isolate a malfunction to an individual component or circuit.

5.2 CALIBRATION CHECKS.

5.2.1 This subsection of the maintenance section contains instructions and reference information for checking the calibration of the Model 4600 DMM. The instructions are presented in tabular form and are organized by instrument function. In addition, the test setup and interconnection is illustrated for each calibration check.

Table 5.1 - DCV Calibration Check

Input and Control Setting		Performance Standard
Function: DCV Range: Auto Input Terminals: J3 (Hi) and J4 (Lo) connected with a copper jumper		
DMM Range	Signal Input	Readout
.2	0.00000	+.00002 to −.00002 (NOTE: offset greater than ±2 digits will require adjustment of R45 (front panel) on .2 range)
.2	+0.19900	+.19894 to +.19906
.2	−0.19900	−.19894 to −.19906
2.	+1.9900	+1.9897 to +1.9903
2.	−1.9900	−1.9897 to −1.9903
20	+19.900	+19.897 to +19.903
20	−19.900	−19.897 to −19.903
200	+199.00	+198.97 to +199.03
200	−199.00	−198.97 to −199.03
2000	+1000.0 (max. input)	+0999.8 to +1000.2
2000	−1000.0 (max. input)	−0999.8 to −1000.2

DMM downranges in auto, from 2000 Range to 210 Range @ ±0099.9 Vdc.

DMM downranges in auto, from 200 Range to 20 Range @ ±009.99 Vdc.

DMM downranges in auto, from 20 Range to 2 Range @ ±00.999 Vdc.

DMM downranges in auto, from 2 Range to .2 Range @ ±0.0999 Vdc.

DMM upranges in auto, from .2 Range to 2. Range @ ±.20000 Vdc.

DMM upranges in auto, from 2. Range to 20 Range @ ±2.0000 Vdc.

DMM upranges in auto, from 20 Range to 200 Range @ ±20.000 Vdc.

DMM upranges in auto, from 200 Range to 2000 Range @ ±200.00 Vdc.

Short input terminals J3 and J4 and manually UP or DOWN range DMM, and check:

.2 range for maximum offset of ±2 digits
2. range for maximum offset of ±1 digit
20. range for maximum offset of ±1 digit
200. range for maximum offset of ±1 digit
2000. range for maximum offset of ±1 digit

Table 5.2 - ACV Calibration Check

Input and Control Setting			Performance Standard
Function: ACV Range: Auto Input Terminals: J3 (Hi) and J4 (Lo) connected with a copper jumper			
DMM Range	Signal Input	Frequency	Readout
.2	0 VAC		.00000 to .00040
2	0 VAC		0.0000 to 0.0005
20	0 VAC		00.000 to 00.030
200	0 VAC		000.00 to 000.05
2000	0 VAC		0000.0 to 0000.5
.2	0.19900 VAC	30 Hz to 50 Hz	.19810 to .19990
.2	0.19900 VAC	50 Hz to 500 Hz	.19850 to .19950
.2	0.19900 VAC	500 Hz to 50 kHz	.19868 to .19932
.2	0.19900 VAC	50 kHz to 100 kHz	.19720 to Overload (manual range) or 0.2005 (auto range to 2. range)
2.	1.9900 VAC	30 Hz to 50 Hz	1.9830 to 1.9970
2.	1.9900 VAC	50 Hz to 20 kHz	1.9871 to 1.9929
2.	1.9900 VAC	20 kHz to 50 kHz	1.9870 to 1.9930
2.	1.9900 VAC	50 kHz to 100 kHz	1.9746 to Overload (manual) or 02.005 (auto to 20 range)
20	19.900 VAC	30 Hz to 50 Hz	19.820 to 19.980
20	19.900 VAC	50 Hz to 20 kHz	19.868 to 19.932
20	19.900 VAC	20 kHz to 50 kHz	19.864 to 19.936
20	19.900 VAC	50 kHz to 100 kHz	19.743 to Overload (manual) or 020.05 (auto to 200 range)
200	199.00 VAC	(Spec is the same as the 2. range)	
2000	20.00 to 500.00	30 Hz to 50 Hz	0496.7 to 0503.3
2000	20.00 to 500.00	50 Hz to 20 kHz	0498.7 to 0501.3
2000	500.00 to 1000.0 (max.)	30 Hz to 50 Hz	0994.0 to 1006.0
2000	500.00 to 1000.0 (max.)	50 Hz to 20 kHz	0997.5 to 1002.5

Table 5.3 - KOhms Calibration Check

Input and Control Setting		Performance Standard
Function: Kohms Range: Auto Input Terminals: J3 (Hi) and J4 (Lo) connected with a copper jumper		
DMM Range	Signal Input	Readout
.2 Kohm	199 Ohms	.19888 to .19912
2 Kohms	1.99 Kohms	1.9889 to 1.9911
20 Kohms	19.9 Kohms	19.889 to 19.911
200 Kohms	199. Kohms	198.89 to 199.11
2000 Kohms	1.99 Mohms	1987.9 to 1992.1
20,000 Kohms	19.9 Mohms	19859 to 19941

Table 5.4 - DCV/mA Calibration Check

Input and Control Setting		Performance Standard
Function: DCV/mA Range: Auto Input Terminals: J1 (Hi) and J2 (Lo) connected with a copper jumper		
DMM Range	Signal Input	Readout
.2	+199 μA DC	+.19872 to +.19928
2	+1.99 mA DC	+1.9872 to +1.9928
20	+19.9 mA DC	+19.872 to +19.928
200	+199. mA DC	+198.72 to +199.28
2000	+1.99A DC	+1982.0 to +1998.0

Table 5.5 - ACV/mA Calibration Check

Input and Control Setting			Performance Standard
Function: ACV/mA Range: Auto Input Terminals: J1 (Hi) and J2 (Lo) connected with a copper jumper			
DMM Range	Signal Input	Frequency	Readout
.2	199 μA AC	50 Hz to 10 kHz	.19840 to .19960
2	1.99 mA AC	50 Hz to 10 kHz	1.9840 to 1.9960
20	19.9 mA AC	50 Hz to 10 kHz	19.840 to 19.960
200	199 mA AC	50 Hz to 10 kHz	198.40 to 199.60
2000	1.99A AC	50 Hz to 10 kHz	1982.0 to 1998.0

5.3 CALIBRATION ADJUSTMENTS.

5.3.1 Test setup and adjustment instructions are presented in this subsection. If performance of the calibration checks indicate the need for adjustment, perform the appropriate adjustment procedure. Like the calibration checks the adjustment procedures are organized by instrument function. This section covers the calibration of the Dana Model 4600 Digital Multimeter and is designed to return the instrument to its published specification for indefinite periods of time. The procedure consists of applying known input levels and adjusting the appropriate component for the indicated value. A list of equipment required to perform the calibration procedure is provided in table 5.6.

5.3.2 Disassembly of the instrument case is as follows:

a. Place instrument on a flat level surface with the bail extended towards the back of the instrument.

b. Disconnect the power cable and remove the screws on the back panel.

c. Slide the instrument out of the case.

5.3.3 The following steps are performed prior to making any adjustments to the instrument.

a. Check the line voltage requirements stamped on the serial tag located on the back of the instrument and insure that the available power source is the same. Connect the instrument to the line and set the power switch to ON. Allow at least 30 minutes for the instrument to temperature stabilize.

b. Refer to the operating manuals provided with the test equipment to be used and provide appropriate warmup time.

WARNING

Removal of covers exposes potentially lethal voltages. On units equipped with battery pack option the power supply charges the batteries even though the power switch is in the off position. Avoid contact with internal AC primary circuits when instrument is connected to the AC line.

Table 5.6 - Required Equipment

NOTE

Minimum use specifications are the principal parameters required for performance of the calibration, and are included to assist in the selection of alternate equipment, which may be used at the discretion of the calibrating activity. Satisfactory performance of alternate items shall be verified prior to use. All applicable equipment must bear evidence of current calibration.

Item	Minimum Use Specifications	Calibration Equipment
DC Voltage Standard	Adjustable, .003% Accuracy	FLUKE 332B
AC Voltage Standard	Adjustable .1V RMS – 1 KV RMS, 400 Hz to 100 kHz .03% Accuracy	HP 745/746
Microvoltmeter	10 μV resolution, center zero	FLUKE 845AR
Resistance Standards	1 KΩ, 10 KΩ } Known to .01%	ESI SR-1 Series
Tools: Phillips #1 screwdriver, insulated blade adjustment tool	—	—

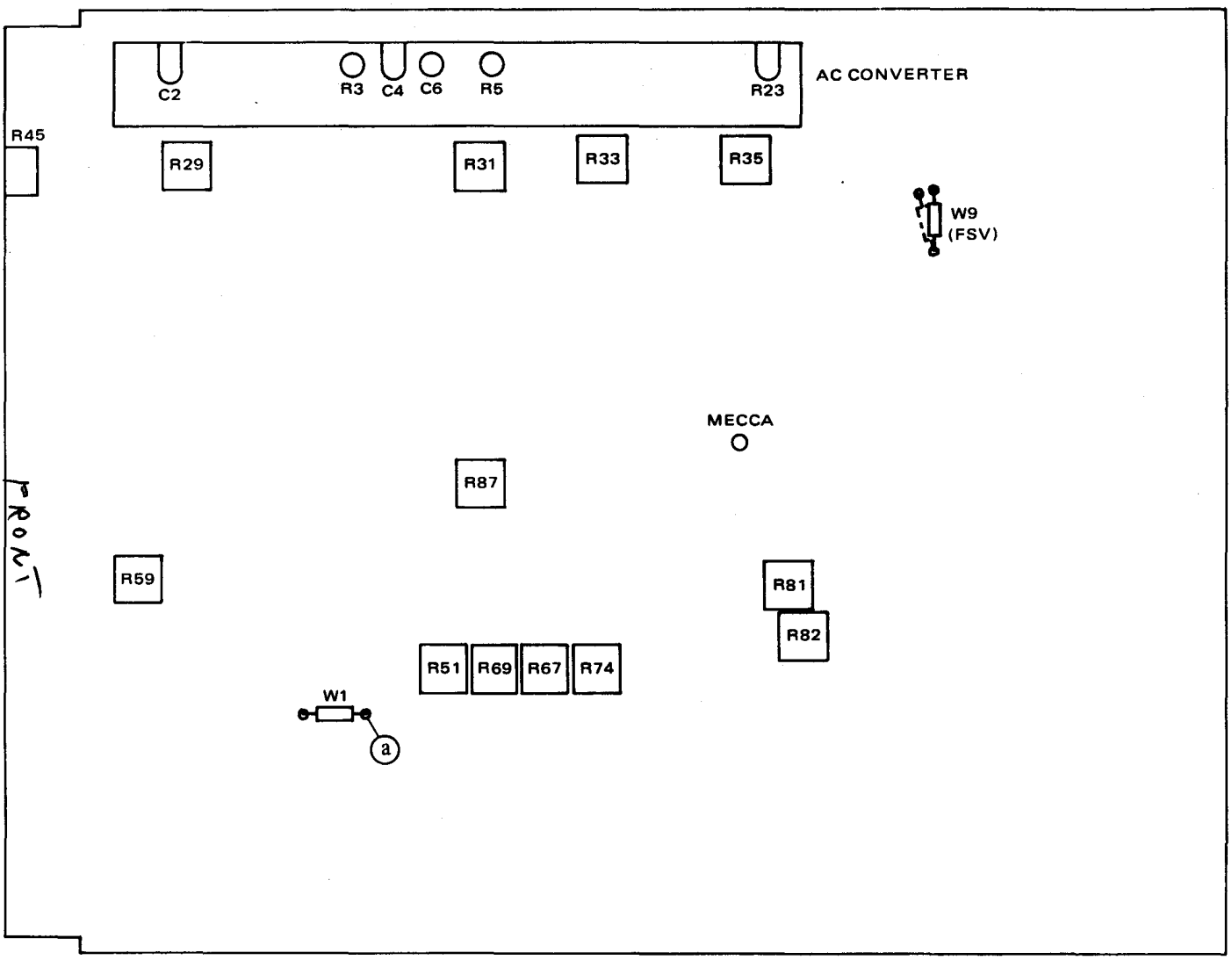

Figure 5.1 - Calibration Points

c. Set the instrument controls as follows:

FUNCTION: Volts DC

RANGE: 200 mV

INPUT: Shorted

5.3.4 The locations of the calibration points as called for in the procedure are indicated in figure 5.1.

5.3.5 CALIBRATION PROCEDURE.

5.3.6 The following steps are for zeroing the instrument prior to range calibration.

a. Disconnect W1 jumper. Apply a 1 millivolt dc signal to the integrator side of W1 (a), referenced to Mecca. The polarity of this signal should be such that R82 has no effect if adjusted.

b. Adjust R81 for a display of 00010 (disregard decimal). Reverse the polarity of the 1 millivolt signal and adjust R82 for a display of .00010.

c. Apply +1.9900 to W1 and adjust R74 for a reading of +19900.

d. Apply –1.9900 to W1 and adjust R67 for a reading of --19900.

e. Remove 1 millivolt dc signal from W1 (a) and reconnect W1. Connect a microvoltmeter "high" input to W1 and "Low" input to MECCA. Short DMM input terminals.

f. Select dc function and .2 volt range. Adjust front panel zero R45 for a microvoltmeter reading of 0 ± 10 μV.

g. Select 20 volt range and adjust R59 for a microvoltmeter reading of 0 ± 10 μV. Repeat steps f and g until no adjustment is required for the 0 ± 10 μV reading.

5.3.7 The remainder of the procedure consists of a separate table for each function. After the function and range have been selected, the component listed in the ADJUST column is adjusted for the indicated display value. Where no adjustment is indicated, the calibration step is for verification of proper instrument operation.

5.3.8 At the completion of the procedure, remove power cord from line. Reassemble case by reversing the procedure of paragraph 5.3.2.

Table 5.7 - DC Calibration Adjustment

FUNCTION	RANGE	INPUT	ADJUST	DISPLAY	REMARKS
DC	.2V	+.19900	R51	+.19900	
	20V	+19.900	R29	+19.900	
	200V	+199.00	R31	+199.00	
	1 KV	+1000.0	R33	+1000.0	
Reduce input voltage to zero volts and remove from input.					

Table 5.8 - AC Calibration Adjustment

FUNCTION	RANGE	INPUT	ADJUST	DISPLAY	REMARKS
AC	1 KV	1 KV @ 1 kHz	R23	1000.0	
	1 KV	1 KV @ 20 kHz	C2	1000.0	Reduce input to .2 volts
	.2V	.19900 @ 1 kHz	R3	.19900	
	.2V	.19900 @ 70 kHz	C4	.19900	
	20V	19.900 @ 1 kHz	R5	19.900	
	20V	19.900 @ 70 kHz	C6	19.900	
Remove signal from input					

Table 5.9 - Resistance Calibration Adjustment

FUNCTION	RANGE	INPUT	ADJUST	DISPLAY	REMARKS
KΩ	.2 KΩ	Short	R87	.00000	
	20 KΩ	10.000 KΩ	R69	10.000	Repeat until no adjustment required
	2 KΩ	1.0000 KΩ	R35	1.0000	

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5.4 TROUBLESHOOTING PERFORMANCE TESTS.

5.4.1 This section contains Unit and Subassembly performance tests. The unit performance tests are designed to isolate a malfunction to a replaceable module or printed circuit board. In some cases where the printed circuit board is large and complex, the unit test is designed to isolate the malfunction to a functional area of the board.

The unit performance tests are organized by instrument function such as AC volts, DC volts or Kohms. A "singlethread" diagram is provided for each of the unit performance tests. These diagrams show the primary signal path through the instrument for the individual function of the instrument.

5.4.2 The subassembly performance tests are designed to isolate a malfunction to a component or small group of components on a printed circuit board.

These tests are organized by subassembly such as the display PCB or the AC converter board.

5.4.3 Both the unit and subassembly performance tests present test setup instructions, step by step instructions for monitoring the circuit under test and performance standards in the form of voltage levels or oscilloscope waveforms. In addition the tests are fully illustrated by either the "singlethread" diagrams or schematics which illustrate the test point location within the circuit under test. For ease in locating the physical test point within the instrument, pictorial drawings are provided on pages facing the schematic.

5.4.4 Test points called out in the performance tests may be actual physical test points provided as convenience test points or they may simply be circuit locations such as the end of a resistor or the emitter of a transistor. In either case the test points appear in the performance test tables as black squares or diamonds. These "flags" also appear on the corresponding schematic and on the pictorial drawing in the drawing section of this manual.

5.4.5 Note that the test points are numbered sequentially so as to start at the input of a circuit and progress to the output. The performance standard for each test point is shown in the table if it is a voltage standard; the waveform standards are provided on waveform illustration pages immediately following the performance test table. The numbered test points refer to square black test point flags  appearing on the assembly drawing and schematics in the drawing section (6). These black square test point flags indicate voltage measurement points. Similarly the alphabetic test points refer to black diamond shaped flags  appearing on the assembly drawings and schematics. The Alphabetic diamond flags indicate oscilloscope test points.

5.4.6 To perform subassembly performance tests refer to the appropriate test table, perform the preliminary test setup presented as the first few steps of the test. When the setup is complete proceed with test and verify that the measurement at each test point is within tolerances called for in the performance standard column of the test. If at any point in the test you do not obtain the required voltage or signal refer to the appropriate schematic to determine the area of the malfunction. Resort to conventional troubleshooting methods to identify the faulty component or circuit. The term conventional troubleshooting methods as used here means checking individual semiconductors, resistors and capacitors in and around the area of malfunction.

5.4.7 Unit Performance Tests.

5.4.8 Tables 5.10 through 5.14 present the unit performance tests. Note that the tables contain performance standards for voltage measurements and waveforms. The tolerance required for troubleshooting is looser than operating tolerances because the technician is generally looking for the presence of the signal rather than an exact high tolerance standard. This allows the use of a much broader range of test equipment and also allows the use of test equipment that is not subject to high accuracy calibration requirements. Troubleshooting, unlike calibration, may be done with any equipment that is accurate to 5%.

5.4.9 The performance tests presented in this section are:

DC Volts Unit Performance Test	Table 5.10
AC Volts Unit Performance Test	Table 5.11
KOhms Unit Performance Test	Table 5.12
DC Milliamps Unit Performance Test	Table 5.13
AC Milliamps Unit Performance Test	Table 5.14

WARNING

Removal of covers exposes potentially lethal voltages. On units equipped with battery pack option the power supply charges the batteries even though the power switch is in the off position. Avoid contact with internal AC primary circuits when instrument is connected to the AC line.

Table 5.10 - DCV Unit Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: .2 (Manual) Input Terminals: J3 (Hi) and J4 (Lo) connected to a DC voltage standard set at ±0.19900V	DC Voltage Input	S3-2 (N/C)	1	Fig. 5.2	NOTE: All measurements are referenced to TP1 (MECCA) ±0.19900V DC ± Tol.
	Isolator Input	S1-4 (N/C)	2	Fig. 5.2	±0.19900V DC ± Tol.
	Isolator Output	E17	3	Fig. 5.2	±1.9900V DC ± Tol.
Range: 2 (Manual) Set DC voltage standard to ±1.9900V	DC Voltage Input	S3-2 (N/C)	1	Fig. 5.2	±1.9900V DC ± Tol.
	Isolator Input	S1-4 (N/C)	2	Fig. 5.2	±1.9900V DC ± Tol.
	Isolator Output	E17	3	Fig. 5.2	±1.9900V DC ± Tol.
Range: 20 (Manual) Set DC Voltage standard to ±19.900V	DC Voltage Input	S3-2 (N/C)	1	Fig. 5.2	±19.900V DC ± Tol.
	Isolator Input	S1-4 (N/C)	2	Fig. 5.2	±1.990V DC ± Tol.
	Isolator Output	E17	3	Fig. 5.2	±1.990V DC ± Tol.
Range: 200 (Manual) Set DC voltage standard to ±199.00V	DC Voltage Input	S3-2 (N/C)	1	Fig. 5.2	±199.00V DC ± Tol.
	Isolator Input	S1-4 (N/C)	2	Fig. 5.2	±1.990V DC ± Tol.
	Isolator Output	E17	3	Fig. 5.2	±1.990V DC ± Tol.

Table 5.10 continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Range: 1000 (Manual) Set DC voltage standard to ±1000.0V	DC Voltage Input	S3-2 (N/C)	1	Fig. 5.2	±1000.0V DC ± Tol.
	Isolator Input	S1-4 (N/C)	2	Fig. 5.2	±1.000V DC ± Tol.
	Isolator Output	E17	3	Fig. 5.2	±1.000V DC ± Tol.

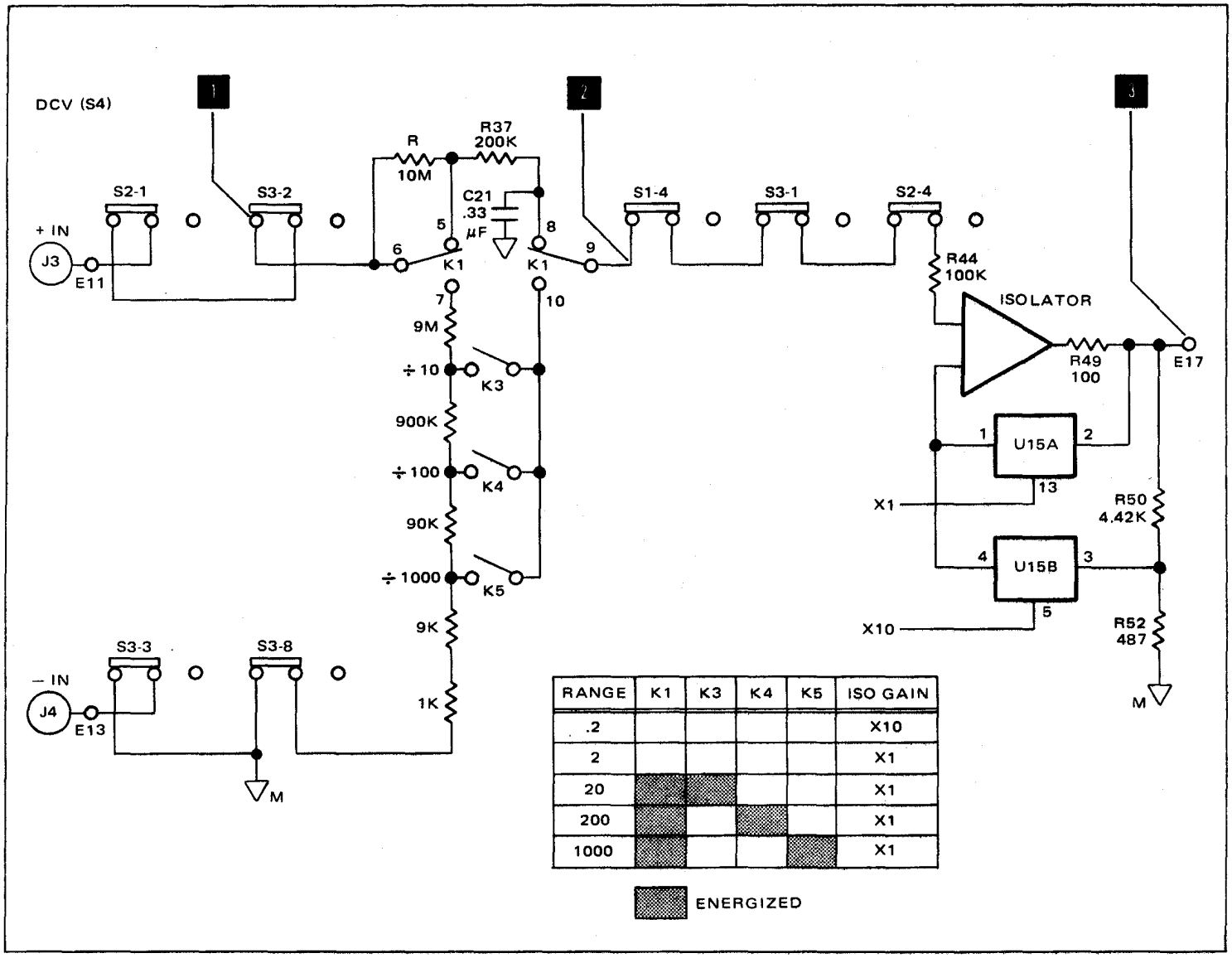


Figure 5.2 - DCV Single Thread Diagram

Table 5.11 - ACV Unit Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: ACV Range: .2 (Manual) Input Terminals: J3 (Hi) and J4 (Lo) connected to an AC voltage standard set at 0.1990V @ 10 kHz					NOTE: All measurements are referenced to TP1 (MECCA)
	AC Signal Input	S1-1 (COM)	1	Fig. 5.3	0.1990V AC ± Tol.
	Isolator Input	S2-4 (COM)	2	Fig. 5.3	–0.1990VDC ± Tol.
	Isolator Output	E17	3	Fig. 5.3	–1.9900VDC ± Tol.
Range: 2 (Manual) Set AC voltage standard to 1.990V @ 10 kHz	AC Signal Input	S1-1 (COM)	1	Fig. 5.3	1.990V AC ± Tol.
	Isolator Input	S2-4 (COM)	2	Fig. 5.3	–1.990VDC ± Tol.
	Isolator Output	E17	3	Fig. 5.3	–1.990VDC ± Tol.
Range: 20 (Manual) Set AC voltage standard to 19.9V @ 10 kHz	AC Signal Input	S1-1 (COM)	1	Fig. 5.3	19.9V AC ± Tol.
	Isolator Input	S2-4 (COM)	2	Fig. 5.3	–0.1990VDC ± Tol.
	Isolator Output	E17	3	Fig. 5.3	–1.990VDC ± Tol.
Range: 200 (Manual) Set AC voltage standard to 199.0V @ 10 kHz	AC Signal Input	S1-1 (COM)	1	Fig. 5.3	199.0V AC ± Tol.
	Isolator Input	S2-4 (COM)	2	Fig. 5.3	–1.990VDC ± Tol.
	Isolator Output	E17	3	Fig. 5.3	–1.990VDC ± Tol.
Range: 1000 (Manual) Set AC voltage standard to 1000.0V @ 10 kHz	AC Signal Input	S1-1 (COM)	1	Fig. 5.3	1000.0V AC ± Tol.
	Isolator Input	S2-4 (COM)	2	Fig. 5.3	–1.000VDC ± Tol.
	Isolator Output	E17	3	Fig. 5.3	–1.000VDC ± Tol.

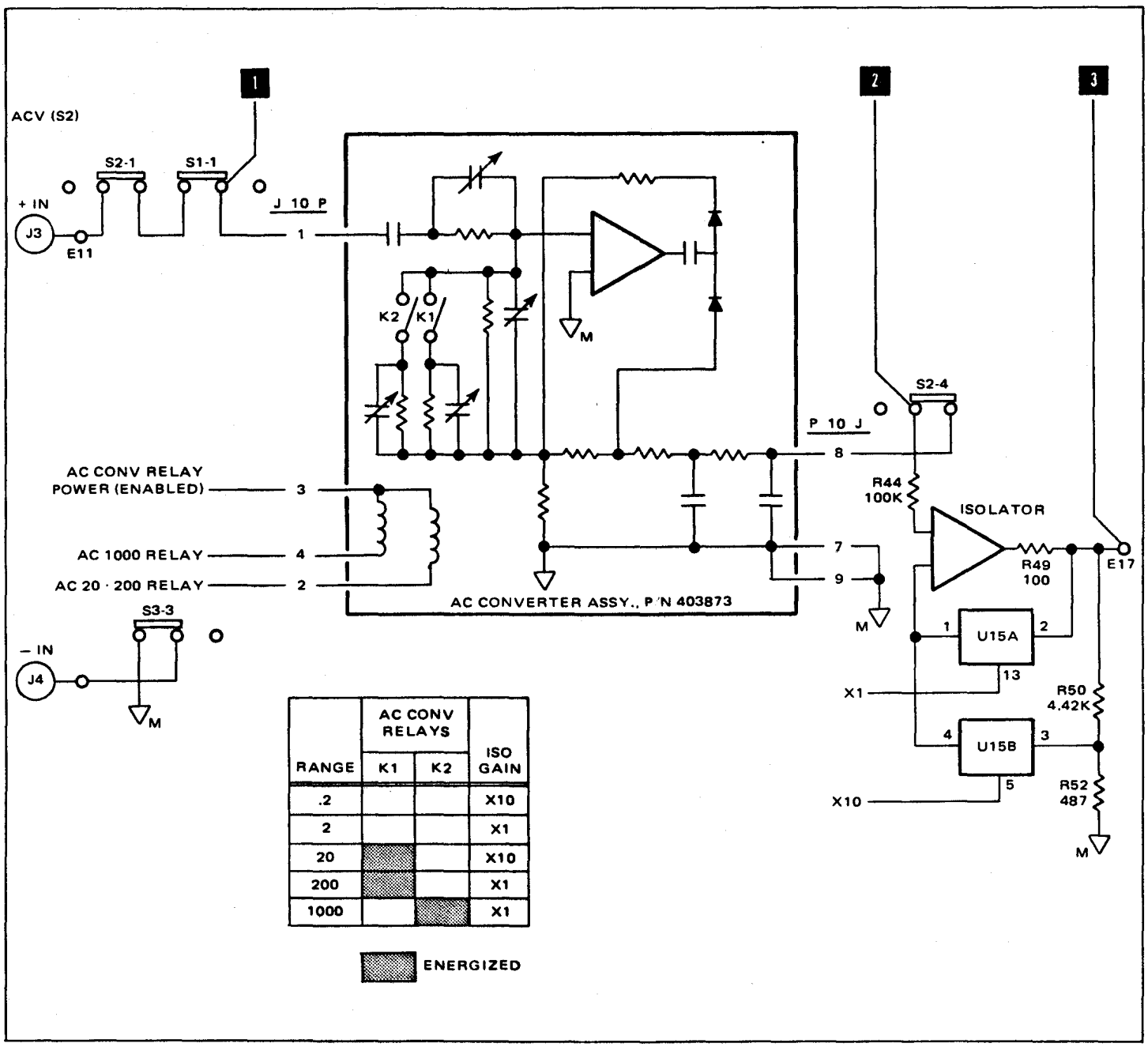


Figure 5.3 - ACV Single Thread Diagram

Table 5.12 - KOhms Unit Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: KOHMS Range: .2 (Manual) Input Terminals: J3 (Hi) and J4 (Lo) connected to an ohms standard set to 199Ω	+1V DC Ohms Reference	S3-8 (COM)	1	Fig. 5.4	NOTE: All measurements are referenced to TP1 (MECCA) +1.000V DC ± Tol.
	NOTE: Ohms Ref voltage is constant for all Kohms measurements				
	Kohms Amp Summing Node	S3-5 (COM)	2	Fig. 5.4	0.000V DC ± Tol.
	NOTE: Summing Node voltage is constant for all Kohms measurements				
	Isolator Input	S2-4 (COM)	3	Fig. 5.4	−0.199V DC ± Tol.
	Isolator Output	E17	4	Fig. 5.4	−1.990V DC ± Tol.
Range: 2 (Manual) Set Ohms standard to 1.99 Kohms	Isolator Input	S2-4 (COM)	3	Fig. 5.4	−1.990V DC ± Tol.
	Isolator Output	E17	4	Fig. 5.4	−1.990V DC ± Tol.
Range: 20 (Manual) Set Ohms standard to 19.9 Kohms	Isolator Input	S2-4 (COM)	3	Fig. 5.4	−1.990V DC ± Tol.
	Isolator Output	E17	4	Fig. 5.4	−1.990V DC ± Tol.
Range: 200 (Manual) Set Ohms standard to 199. Kohms	Isolator Input	S2-4 (COM)	3	Fig. 5.4	−1.990V DC ± Tol.
	Isolator Output	E17	4	Fig. 5.4	−1.990V DC ± Tol.
Range: 2000 (Manual) Set Ohms standard to 1.99 Mohms	Isolator Input	S2-4 (COM)	3	Fig. 5.4	−1.990V DC ± Tol.
	Isolator Output	E17	4	Fig. 5.4	−1.990V DC ± Tol.
Range: 20000 (Manual) Set Ohms standard to 19.9 Mohms	Isolator Input	S2-4 (COM)	3	Fig. 5.4	−1.990V DC ± Tol.
	Isolator Output	E17	4	Fig. 5.4	−1.990V DC ± Tol.

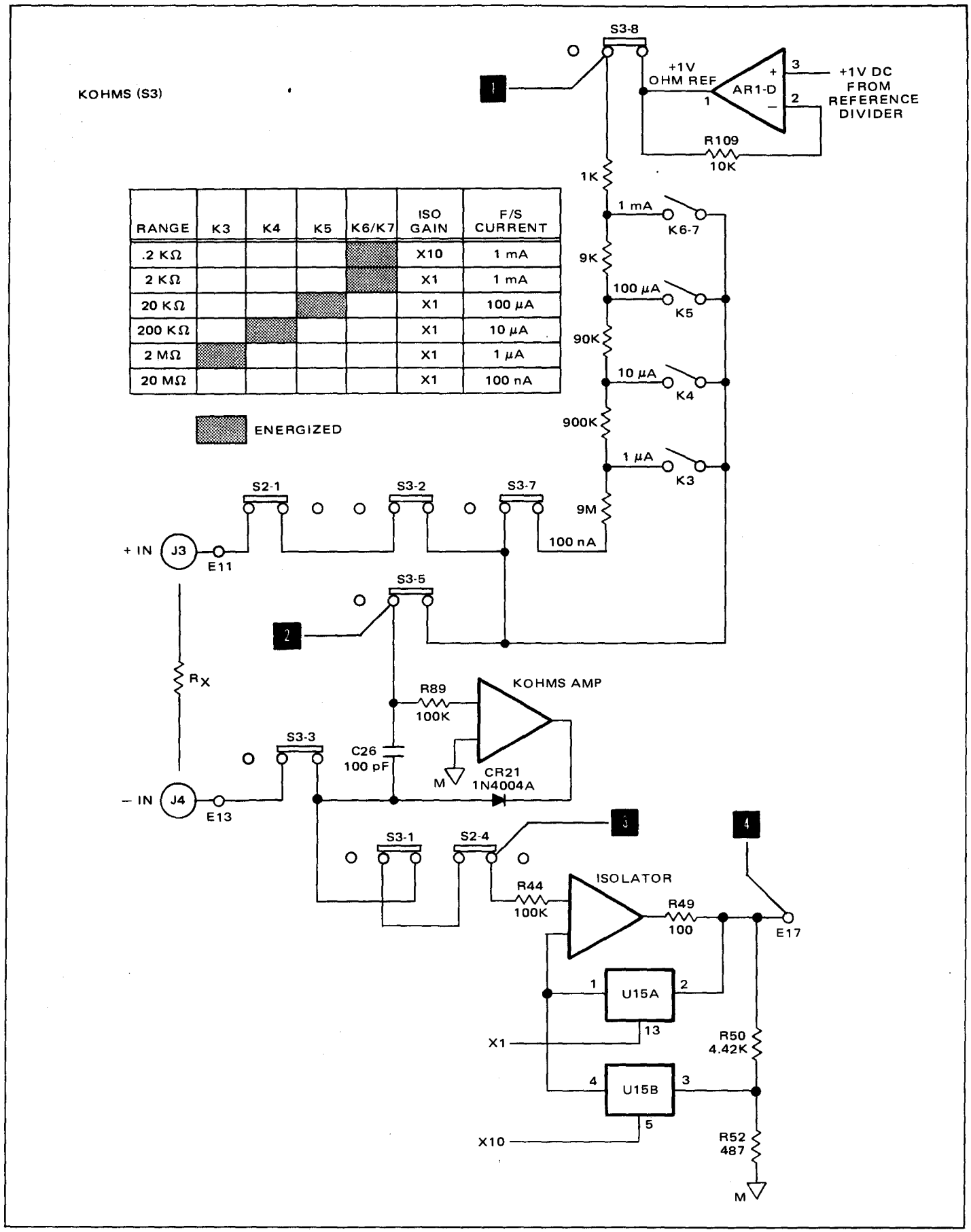
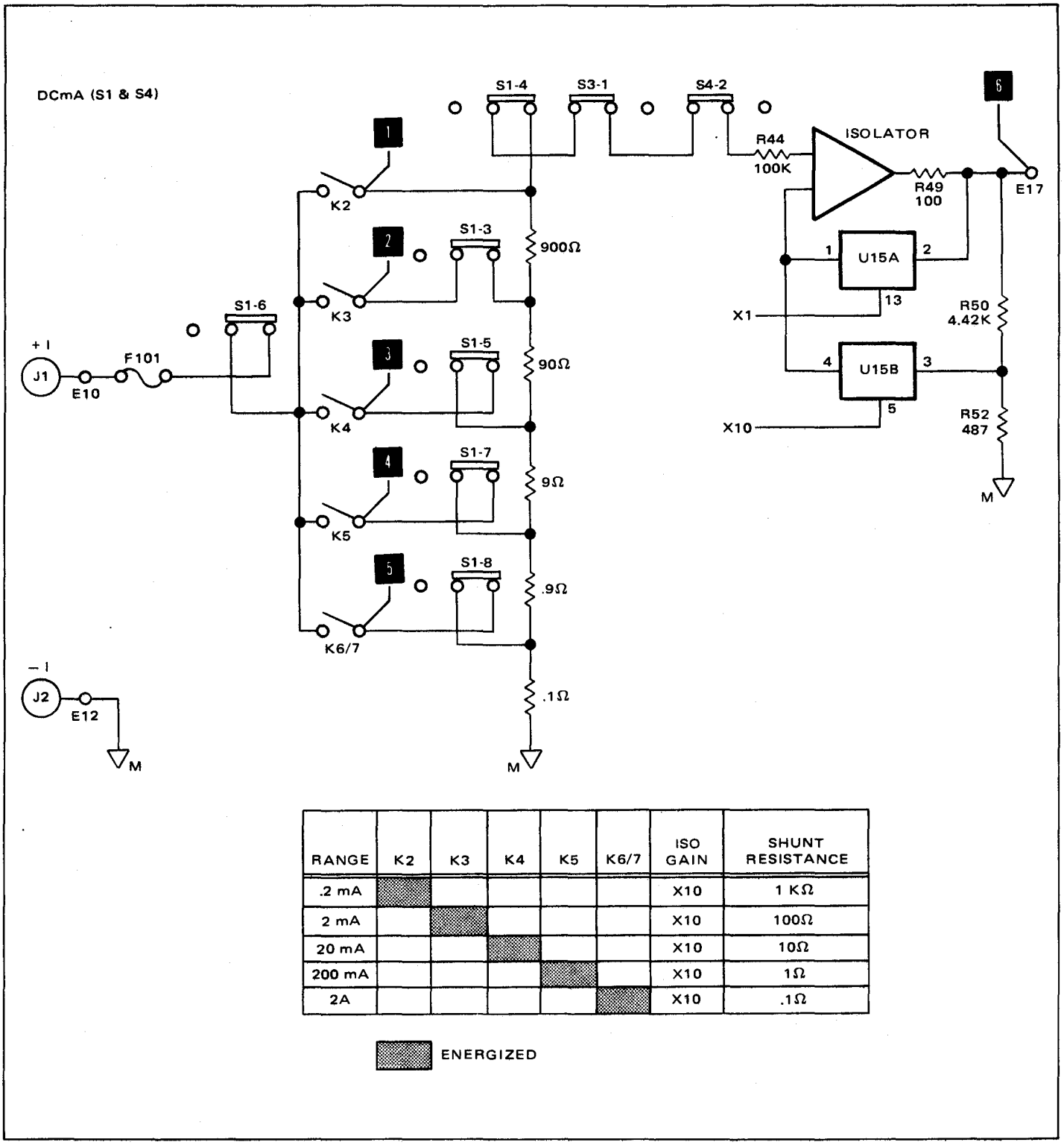


Figure 5.4 - KOhms Single Thread Diagram

Table 5.13 - DCmA Unit Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DC & mA Range: .2 (Manual) Input Terminals: J1 (Hi) and J2 (Lo) connected to a current standard set to ±199 μA DC	Current Shunt/ Isolator In	K2	1	Fig. 5.5	NOTE: All measurements are referenced to TP1 (MECCA) ±0.1990V DC ± Tol.
	Isolator Output	E17	6	Fig. 5.5	±1.990V DC ± Tol.
Range: 2 (Manual) Set current standard to ±1.99 mA DC	Current Shunt/ Isolator In	K3	2	Fig. 5.5	±0.1990V DC ± Tol.
	Isolator Output	E17	6	Fig. 5.5	±1.990V DC ± Tol.
Range: 20 (Manual) Set Current standard to ±19.9 mA DC	Current Shunt/ Isolator In	K4	3	Fig. 5.5	±0.1990V DC ± Tol.
	Isolator Output	E17	6	Fig. 5.5	±1.990V DC ± Tol.
Range: 200 (Manual) Set current standard to ±199 mA DC	Current Shunt/ Isolator In	K5	4	Fig. 5.5	±0.1990V DC ± Tol.
	Isolator Output	E17	6	Fig. 5.5	±1.990V DC ± Tol.
Range: 2000 (Manual) Set current standard to ±1.9A DC	Current Shunt/ Isolator In	K6/K7	5	Fig. 5.5	±0.1990V DC ± Tol.
	Isolator Out	E17	6	Fig. 5.5	±1.990V DC ± Tol.



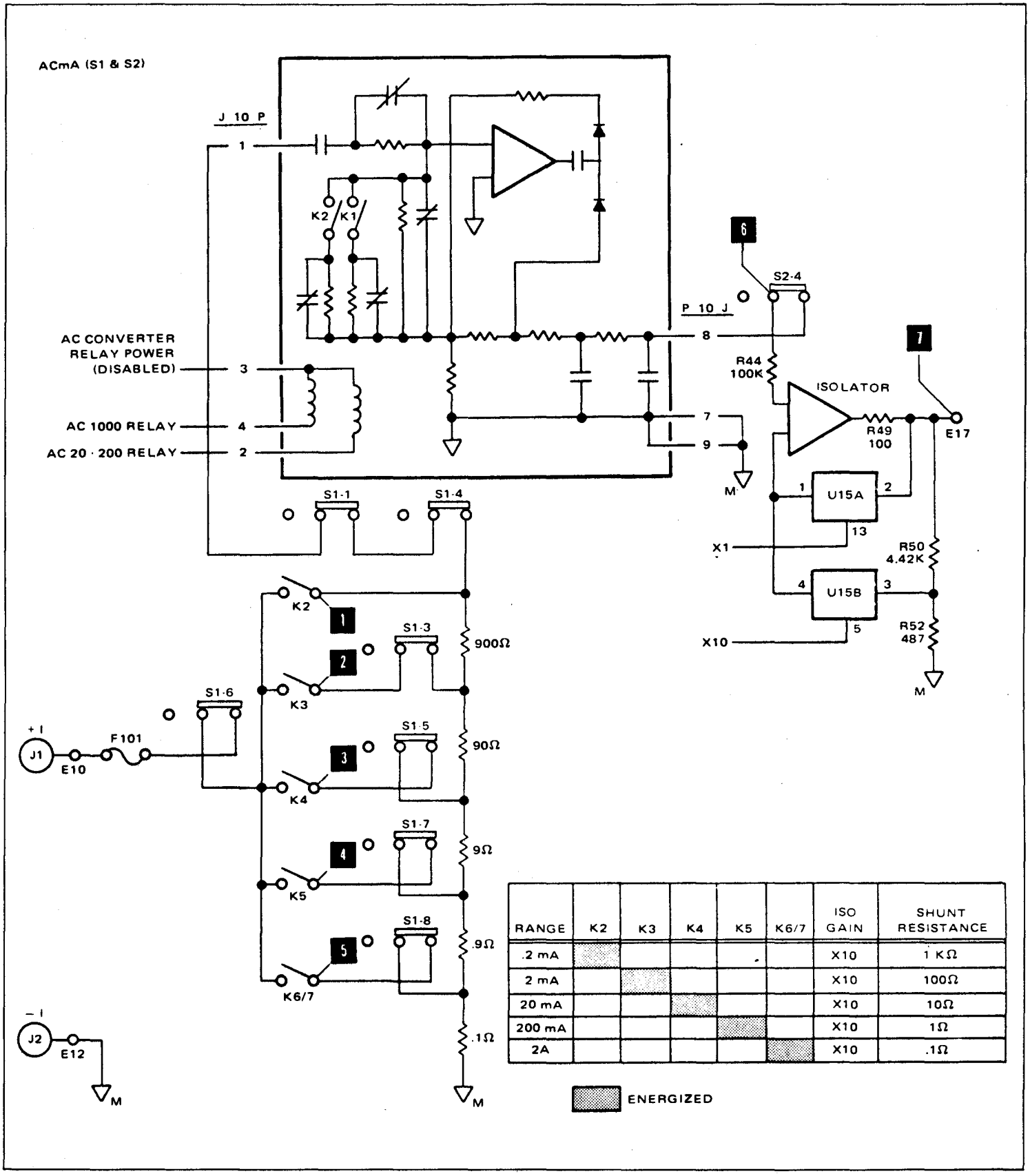
RANGE	K2	K3	K4	K5	K6/7	ISO GAIN	SHUNT RESISTANCE
.2 mA	■					X10	1 KΩ
2 mA		■				X10	100Ω
20 mA			■			X10	10Ω
200 mA				■		X10	1Ω
2A					■	X10	.1Ω

■ ENERGIZED

Figure 5.5 - DCmA Single Thread Diagram

Table 5.14 - ACmA Unit Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: AC & mA Range: .2 (Manual) Input Terminals: J1 (Hi) and J2 (Lo) connected to an AC current standard set to 199 μA					NOTE: All measurements are referenced to TP1 (MECCA)
	AC Converter Input	K2	1	Fig. 5.6	0.1990V AC ± Tol.
	Isolator Input	S2-4 (COM)	6	Fig. 5.6	–0.1990V DC ± Tol.
	Isolator Output	E17	7	Fig. 5.6	–1.990V DC ± Tol.
Range: 2 (Manual) Set AC current standard to 1.99 mA	AC Converter Input	K3	2	Fig. 5.6	0.1990V AC ± Tol.
	Isolator Input	S2-4 (COM)	6	Fig. 5.6	–0.1990V DC ± Tol.
	Isolator Output	E17	7	Fig. 5.6	–1.990V DC ± Tol.
Range: 20 (Manual) Set AC current standard to 19.9 mA	AC Converter Input	K4	3	Fig. 5.6	0.1990V AC ± Tol.
	Isolator Input	S2-4 (COM)	6	Fig. 5.6	–0.1990V DC ± Tol.
	Isolator Output	E17	7	Fig. 5.6	–1.990V DC ± Tol.
Range: 200 (Manual) Set AC current standard to 199 mA	AC Converter Input	K5	4	Fig. 5.6	0.1990V AC ± Tol.
	Isolator Input	S2-4 (COM)	6	Fig. 5.6	–0.1990V DC ± Tol.
	Isolator Output	E17	7	Fig. 5.6	–1.990V DC ± Tol.
Range: 2000 (Manual) Set AC current standard to 1.99A	AC Converter Input	K6/K7	5	Fig. 5.6	0.1990V AC ± Tol.
	Isolator Input	S2-4 (COM)	6	Fig. 5.6	–0.1990V DC ± Tol.
	Isolator Output	E17	7	Fig. 5.6	–1.990V DC ± Tol.



RANGE	K2	K3	K4	K5	K6/7	ISO GAIN	SHUNT RESISTANCE
.2 mA	■					X10	1 KΩ
2 mA		■				X10	100Ω
20 mA			■			X10	10Ω
200 mA				■		X10	1Ω
2A					■	X10	.1Ω

■ ENERGIZED

Figure 5.6 - ACmA Single Thread Diagram

5.4.10 Subassembly Performance Tests.

5.4.11 Subassembly performance tests are designed to isolate a malfunction to a small group of components or a single functional group of components. Once the trouble is narrowed down to a small area the technician should resort to conventional troubleshooting techniques such as checking individual components such as resistors, capacitors, semiconductors and applying heat and cold to individual components. Each of the subassembly performance tests is accompanied by performance standards for each step of the test. These performance standards are in the form of static dc voltages or waveform pictures.

In the case of the main printed circuit board, the largest and most complex of the PCB's, several performance tests have been provided. These tests are segregated because the main PCB contains a number of separate functional circuits such as the clock, isolator, range control and null detector. Separate performance tests are provided for each of the remaining smaller boards.

5.4.12 Note that the test points in the performance test tables refer to the performance standard or waveforms in the test and to the test point shown on the assembly drawings and schematic drawings in section 6 of this manual. The presentation of assembly drawings in the troubleshooting section and again in the drawing section of the manual is redundant but it provides the necessary continuity and makes the technicians troubleshooting job easier.

WARNING

Removal of covers exposes potentially lethal voltages. On units equipped with battery pack option the power supply charges the batteries even though the power switch is in the off position. Avoid contact with internal AC primary circuits when instrument is connected to the AC line.

Table 5.15 - Main PCB, Power Supply (Line Only) Subassembly Performance Test

AC line (only) Power Supply

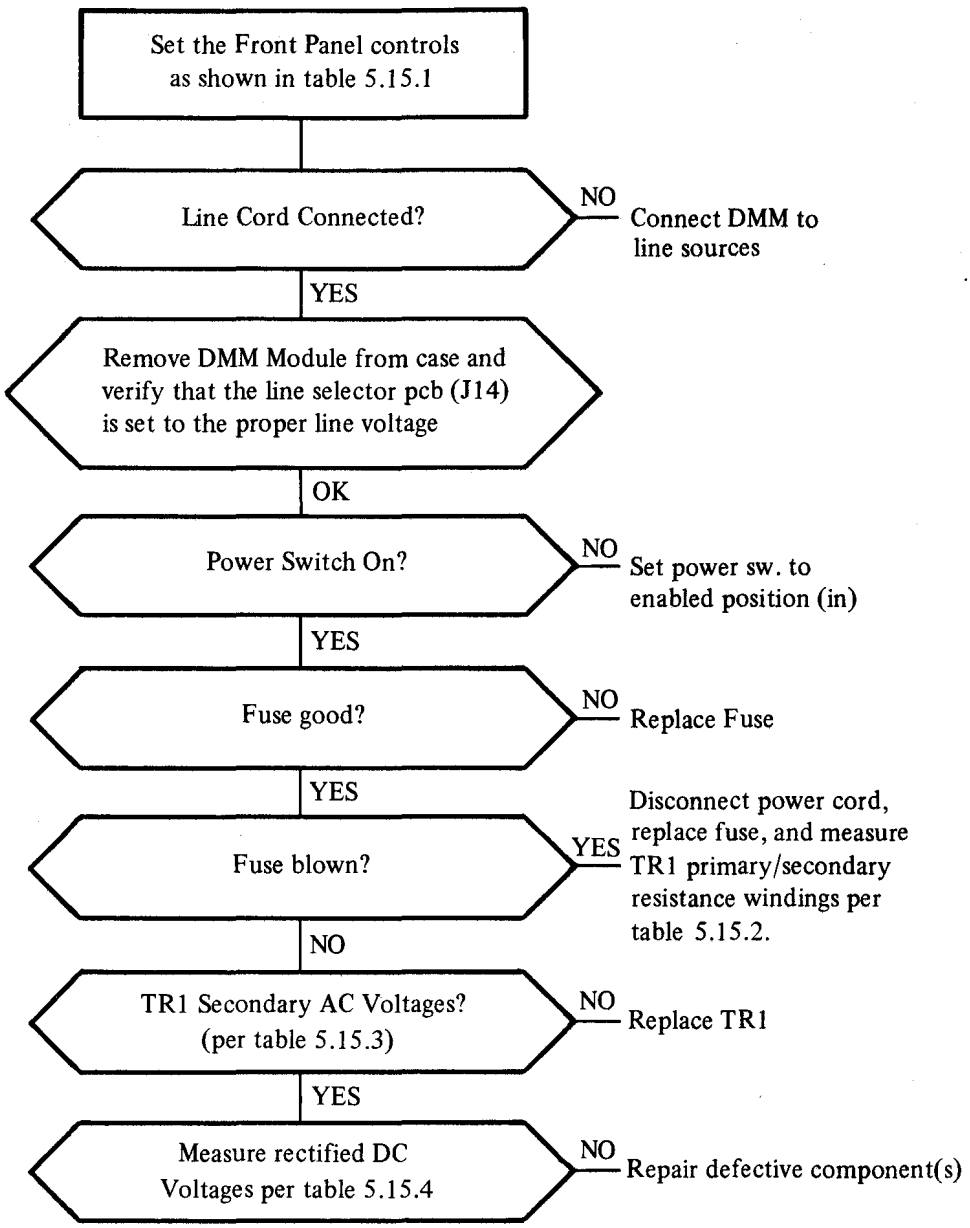


Table 5.15.1

Control	Position
mA	OUT
ACV	OUT
KΩ	OUT
DC	IN (enabled)
UP	OUT
DWN	OUT
AUTO	IN (enabled)
J3 (AC·DC·Ω Hi) jumpered to J4 (AC·DC·Ω Lo)	

Table 5.15.2

Primary Resistance of TR1	
J14 Setting	J201 Line (L) to neutral (N)
100 VAC	40Ω ± 2Ω
120 VAC	42Ω ± 2Ω
220 VAC	142Ω ± 5Ω
240 VAC	154Ω ± 5Ω
Secondary Resistances	
E43 to E47	16 to 16.5Ω
E43 to E46	16 to 16.5Ω
E46 to E47	32 to 33Ω
E42 to E44	0.8 to 0.9Ω
E42 to E45	0.8 to 0.9Ω
E44 to E45	1.6 to 1.8Ω
P8-1 to P8-2	2.6 to 2.75Ω
P8-1 to P8-3	2.6 to 2.75Ω
P8-2 to P8-3	5.2 to 5.5Ω

Table 5.15.3

TR1 Secondary AC Voltages	
E43 to E47	18.0 to 18.5 VAC
E43 to E46	18.0 to 18.5 VAC
E46 to E47	36.0 to 37.0 VAC
E42 to E44	7.8 to 8.3 VAC
E42 to E45	7.8 to 8.3 VAC
E44 to E45	15.5 to 16.5 VAC
P8-1 to P8-2	7.5 to 7.8 VAC
P8-1 to P8-3	7.5 to 7.8 VAC
P8-2 to P8-3	15.0 to 15.6 VAC

Table 5.15.4

DC Voltages Referenced to TP1 (Mecca)	
CR26/27 Cathodes	+21.0 to +22.0 Vdc
CR24/25 Anodes	−21.0 to −22.0 Vdc
VR12 Cathode	+15.5 to +16.0 Vdc
VR11 Anode	−15.5 to −16.0 Vdc
VR13 Anode	−17.8 to −18.1 Vdc
VR14 Cathode	+4.6 to +4.8 Vdc
Q12 Emitter	+15.0 to +15.2 Vdc
Q11 Emitter	−15.0 to −15.2 Vdc
Q13 Emitter	−17.1 to −17.3 Vdc
DC Voltages Referenced to E21 (digital common)	
CR22/23 Cathode	+9.0 to +9.1 Vdc
VR10 Cathode	+5.5 to +5.7 Vdc
Q10 Emitter	+4.9 to +5.1 Vdc

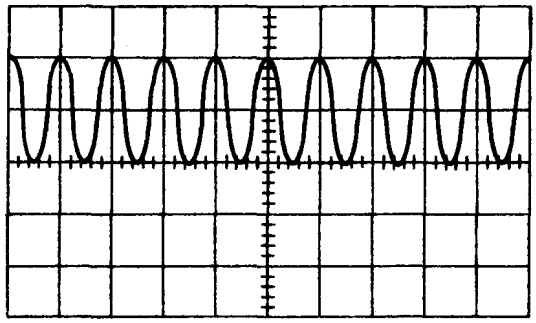
Table 5.16 - Main PCB, Oscillator/Clock Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: Auto Input Terminals: J3 (Hi) and J4 (Lo) connected with a copper jumper					NOTE: All measurements referenced to digital common
	Crystal Oscillator Output	U7-13	A	Fig. 5.7	Waveform No. 1
	Oscillator Output	U7-10	B	Fig. 5.7	Waveform No. 2
	Clock Output	U8-9	C	Fig. 5.7	Waveform No. 3

Waveforms for Table 5.16

1 (NO.) CRYSTAL OSCILLATOR OUTPUT

U7-13 200 kHz



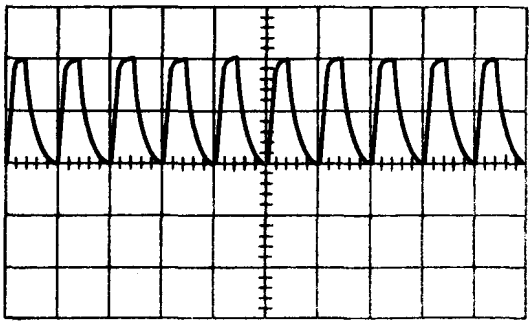
1.V (V/DIV)

5 μS (S/DIV)

DC COUPLED

2 (NO.) OSCILLATOR OUTPUT

U7-10 200 kHz



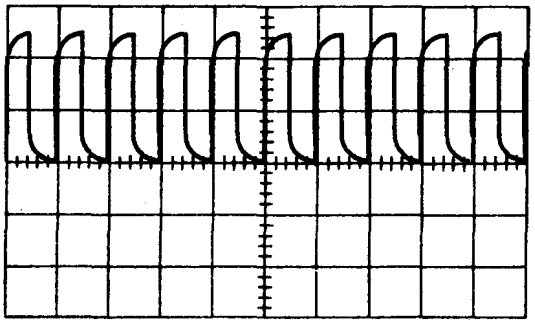
2.V (V/DIV)

5 μS (S/DIV)

DC COUPLED

3 (NO.) CLOCK OUTPUT

U8-9 100 kHz



2.V (V/DIV)

10 μS (S/DIV)

DC COUPLED

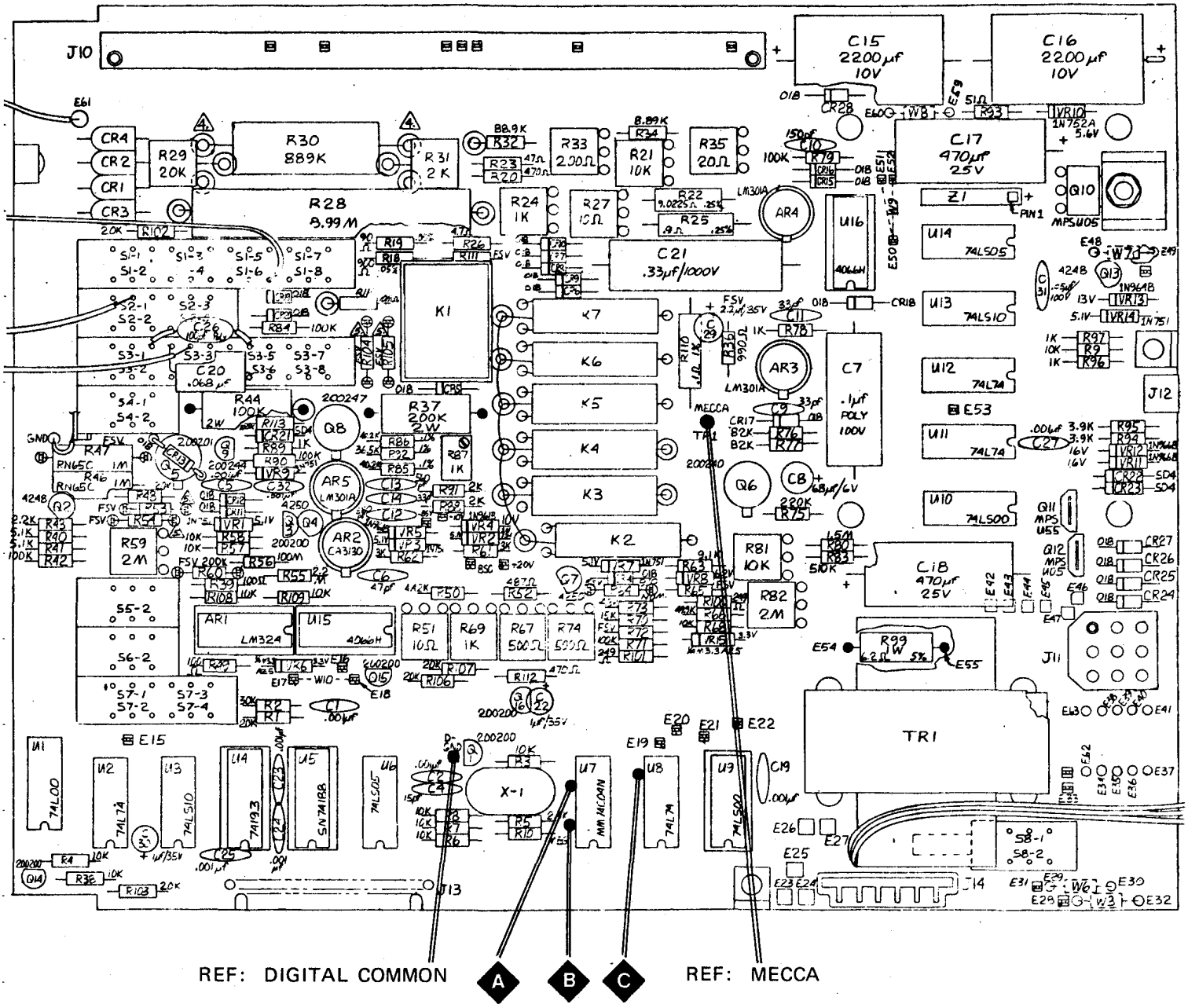


Figure 5.7 - Main PCB Oscillator/Clock Test Point Locations

Table 5.17 - Main PCB, Reference Voltage Generator Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: Auto Input Terminals: J3 (Hi) and J4 (Lo) connected with a copper jumper					NOTE: All measurements are referenced to TP1 (Mecca)
	Current Generator bias voltage	CR14 (Cathode)	1	Fig. 5.8	+9.5 to 9.9 Vdc
	Current Generator bias voltage	R64	2	Fig. 5.8	+10.1 to +10.6 Vdc
	Reference Zener voltage	VR8 (Cathode)	3	Fig. 5.8	+6.2 to +6.4 Vdc (refer to voltage on zener tag)
	–1V Reference Output voltage	AR1b – 14	4	Fig. 5.8	–0.9999 to –1.0001 Vdc
	+1V Reference Input	AR1c – 10	5	Fig. 5.8	+1.0005 to +1.0015 Vdc
	+1V Reference Output	AR1c – 8	6	Fig. 5.8	+0.9999 to +1.0001 Vdc
	+1V Ohms Reference Input	AR1d – 3	7	Fig. 5.8	+1.0010 to +1.0025 Vdc
	+1V Ohms Reference Output	AR1d – 1	8	Fig. 5.8	+1.0005 to +1.0015 Vdc

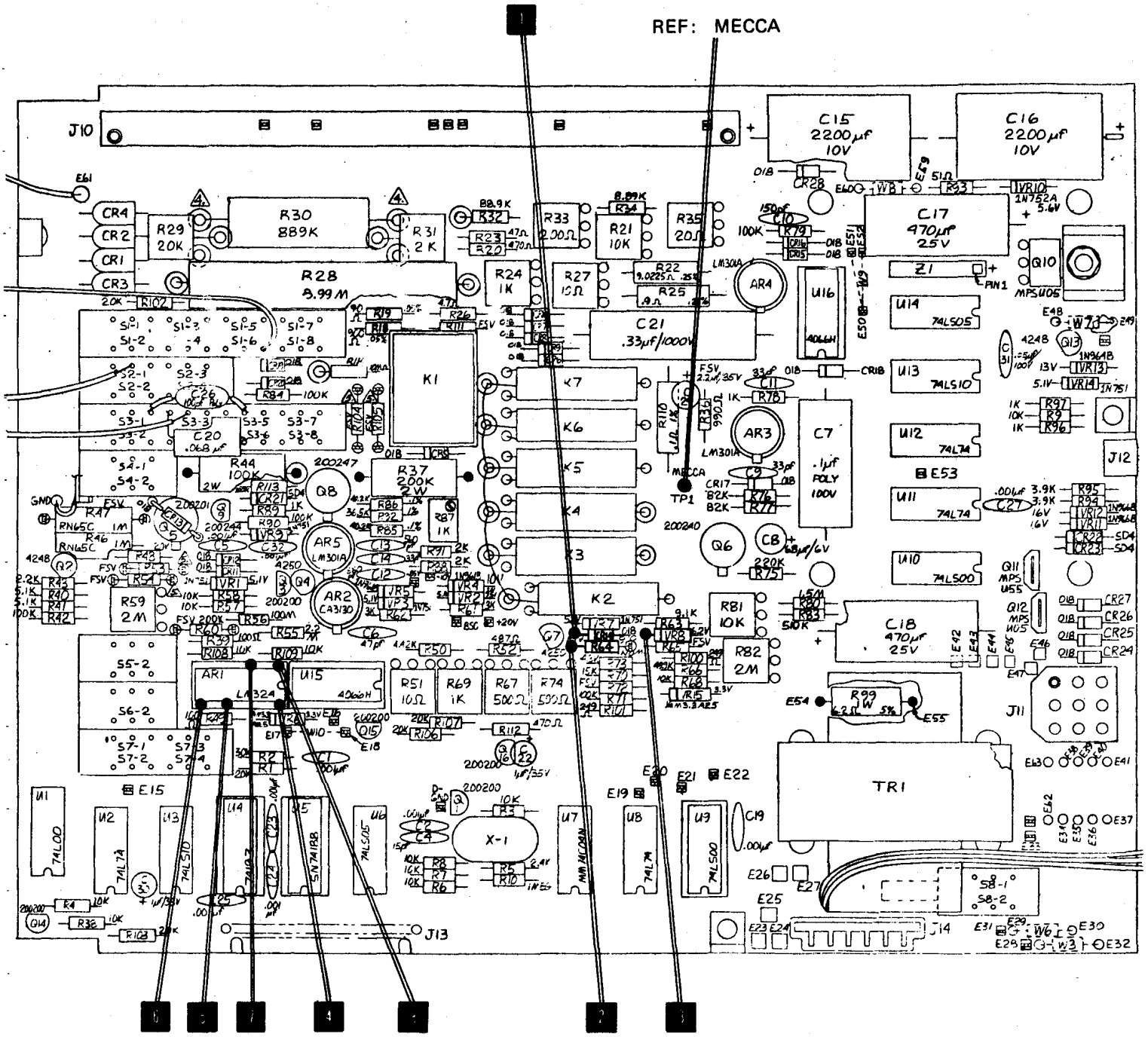


Figure 5.8 - Main PCB Reference Voltage Generator Test Point Locations

Table 5.18 - Main PCB, Timing and Control Logic Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: Auto Input Terminals: J3 (Hi) and J4 (Lo) connected with a copper jumper					NOTE: All measurements are referenced to digital common NOTE: Ext. trig. scope at S7-3 N/O
	Counter Output, Q_{e1}	U9-2	D	Fig. 5.9	Waveform No. 4
	Counter Output, Q_{e2}	U9-1	E	Fig. 5.9	Waveform No. 5
	$\overline{\text{Signal Integrate}}$	U9-3	F	Fig. 5.9	Waveform No. 6
	$\overline{\text{Reset}}$	U9-6	G	Fig. 5.9	Waveform No. 7
	Signal Switch Output	U14-2	H	Fig. 5.9	Waveform No. 8
	– Reference Switch Output	U14-10	I	Fig. 5.9	+ Polarity (Display) Waveform No. 9
	+ Reference Switch Output	U14-12	J	Fig. 5.9	– Polarity (Display) Waveform No. 9
	Reset Switch Output	U14-4	K	Fig. 5.9	Waveform No. 10
Check $\overline{\text{Transfer}}$ at $0V_{in}$, H/S (half scale) and F/S (full scale)	$\overline{\text{Transfer}}$	U10-8	L	Fig. 5.9	Waveform No. 11

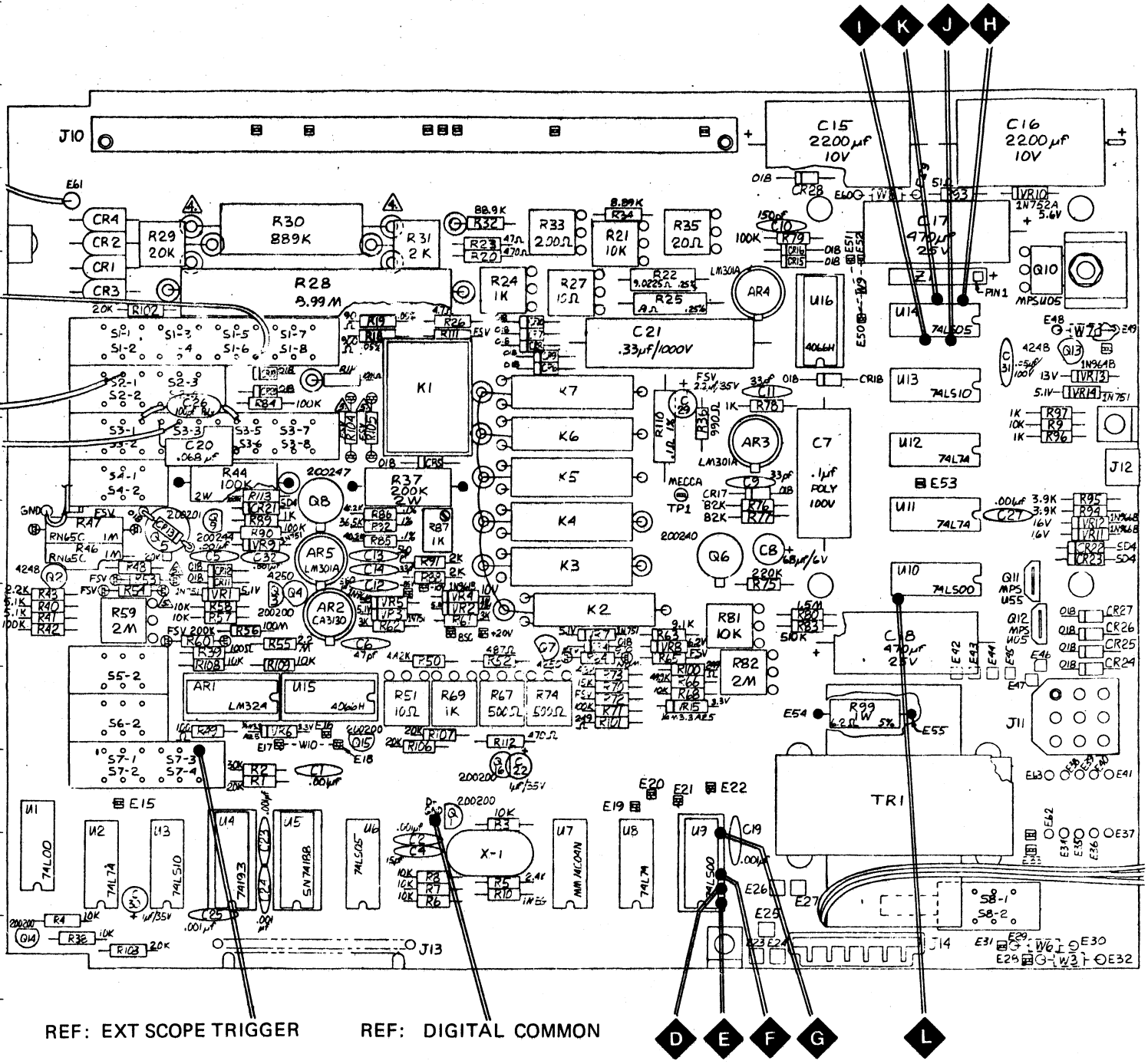
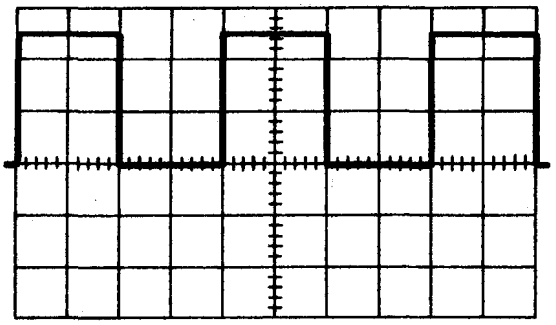


Figure 5.9 - Main PCB Timing and Control Logic Test Point Locations

4 (NO.) Q_{e1}

U9-2



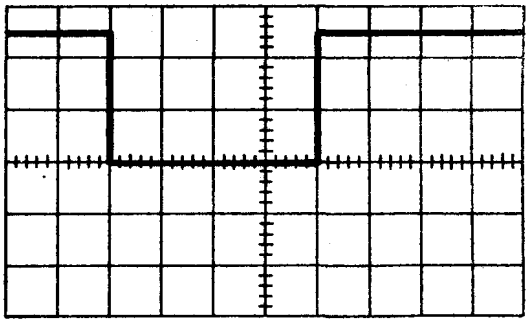
2.0V (V/DIV)

50 MS (S/DIV)

DC COUPLED

5 (NO.) Q_{e2}

U9-1



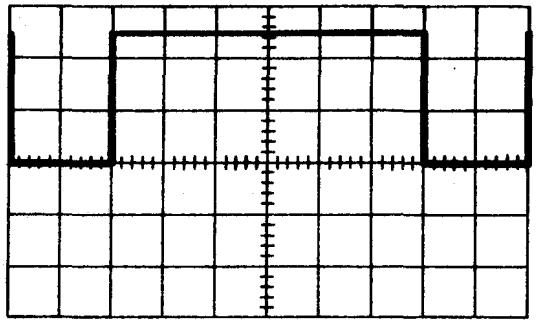
2.0V (V/DIV)

50 MS (S/DIV)

DC COUPLED

6 (NO.) $\overline{\text{SIGNAL INTEGRATE}}$

U9-3



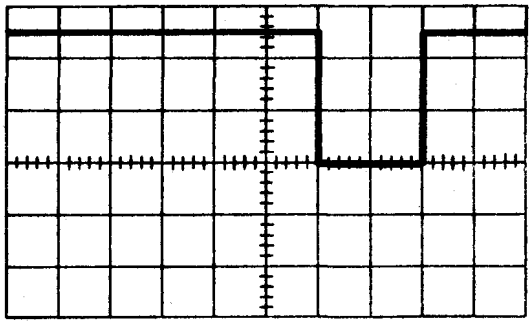
2.0V (V/DIV)

50 MS (S/DIV)

DC COUPLED

7 (NO.) $\overline{\text{RESET}}$

U9-6



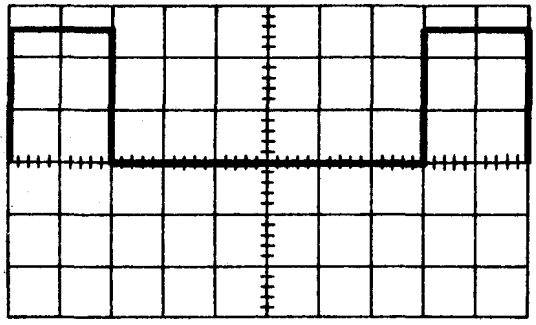
2.0V (V/DIV)

50 MS (S/DIV)

DC COUPLED

8 (NO.) SIGNAL SWITCH

U14-2



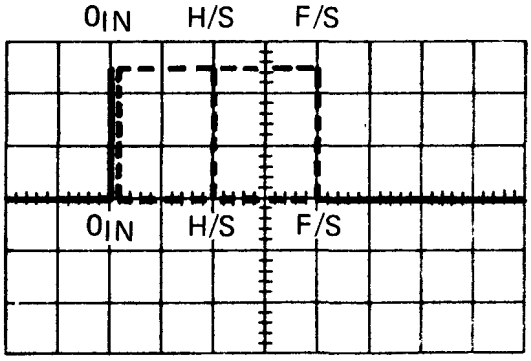
2.0V (V/DIV)

50 MS (S/DIV)

DC COUPLED

9 (NO.) MINUS REFERENCE SWITCH

U14-10



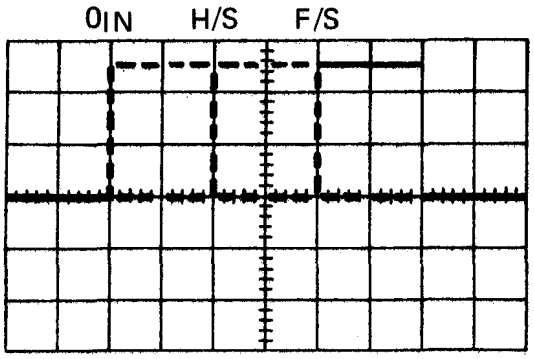
2.0V (V/DIV)

50 MS (S/DIV)

DC COUPLED

Waveforms for Table 5.18

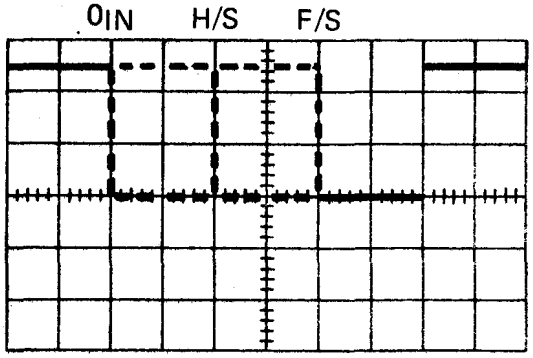
10 (NO.) RESET SWITCH
U14-4



2.0V (V/DIV)

DC COUPLED
50 MS (S/DIV)
REF: DIGITAL COMMON

11 (NO.) $\overline{\text{TRANSFER}}$
U10-8



2.0V (V/DIV)

DC COUPLED
50 MS (S/DIV)
REF: DIGITAL COMMON

Table 5.19 - Main PCB, Range and Relay Logic Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: .2 manual Input Terminals: J3 (Hi) and J4 (Lo) connected with a copper jumper			See paragraph 5.4.13 below.		NOTE: All measurements referenced to digital common
Range: .2	ROM inputs/outputs	U5			
Range: 2.	ROM inputs/outputs	U5			
Range: 20.	ROM inputs/outputs	U5	9	Fig. 5.10	Fig. 5.11(A)
Range: 200.	ROM inputs/outputs	U5			
Range: 1000.	ROM inputs/outputs	U5			
Function: ACV	ROM inputs/outputs	U5			
Range: 200.	ROM inputs/outputs	U5			
Range: 20.	ROM inputs/outputs	U5	9	Fig. 5.10	Fig. 5.11(B)
Range: 2.	ROM inputs/outputs	U5			
Range: .2	ROM inputs/outputs	U5			
Function: KΩ	ROM inputs/outputs	U5			
Range: 2.	ROM inputs/outputs	U5			
Range: 20.	ROM inputs/outputs	U5	9	Fig. 5.10	Fig. 5.11(C)
Range: 200.	ROM inputs/outputs	U5			
Range: 2000.	ROM inputs/outputs	U5			
Range: 20,000.	ROM inputs/outputs	U5			
Function: DCmA	ROM inputs/outputs	U5			
Range: 200.	ROM inputs/outputs	U5			
Range: 20.	ROM inputs/outputs	U5	9	Fig. 5.10	Fig. 5.11(D)
Range: 2.	ROM inputs/outputs	U5			
Range: .2	ROM inputs/outputs	U5			
Function: ACmA	ROM inputs/outputs	U5			
Range: 2.	ROM inputs/outputs	U5			
Range: 20.	ROM inputs/outputs	U5	9	Fig. 5.10	Fig. 5.11(E)
Range: 200.	ROM inputs/outputs	U5			
Range: 2000.	ROM inputs/outputs	U5			

5.4.13 The test point 9 specified in table 5.19 refers to the ROM input and output pins on ROM U5 shown in figure 5.10. For the specific pin to be used for testing refer to figure 5.11. For example when performing the DCV check presented in table 5.19 the performance standard column refers to figure 5.11A. At the top of figure 5.11A logic level "checkerboards" are provided to indicate the logic level of each input and output pin of the ROM U5. Note also that every range of the DC function is shown. For example to check the ROM input for the 2 volt range refer to the "IN" checkerboard. In the 2 column all input pins are shown to be logic zero (.1V dc) except pin 12 which is logic level 1 (4.1V dc). Thus it is a simple matter to determine the proper ROM state from figure 5.11 for any function and range combination.

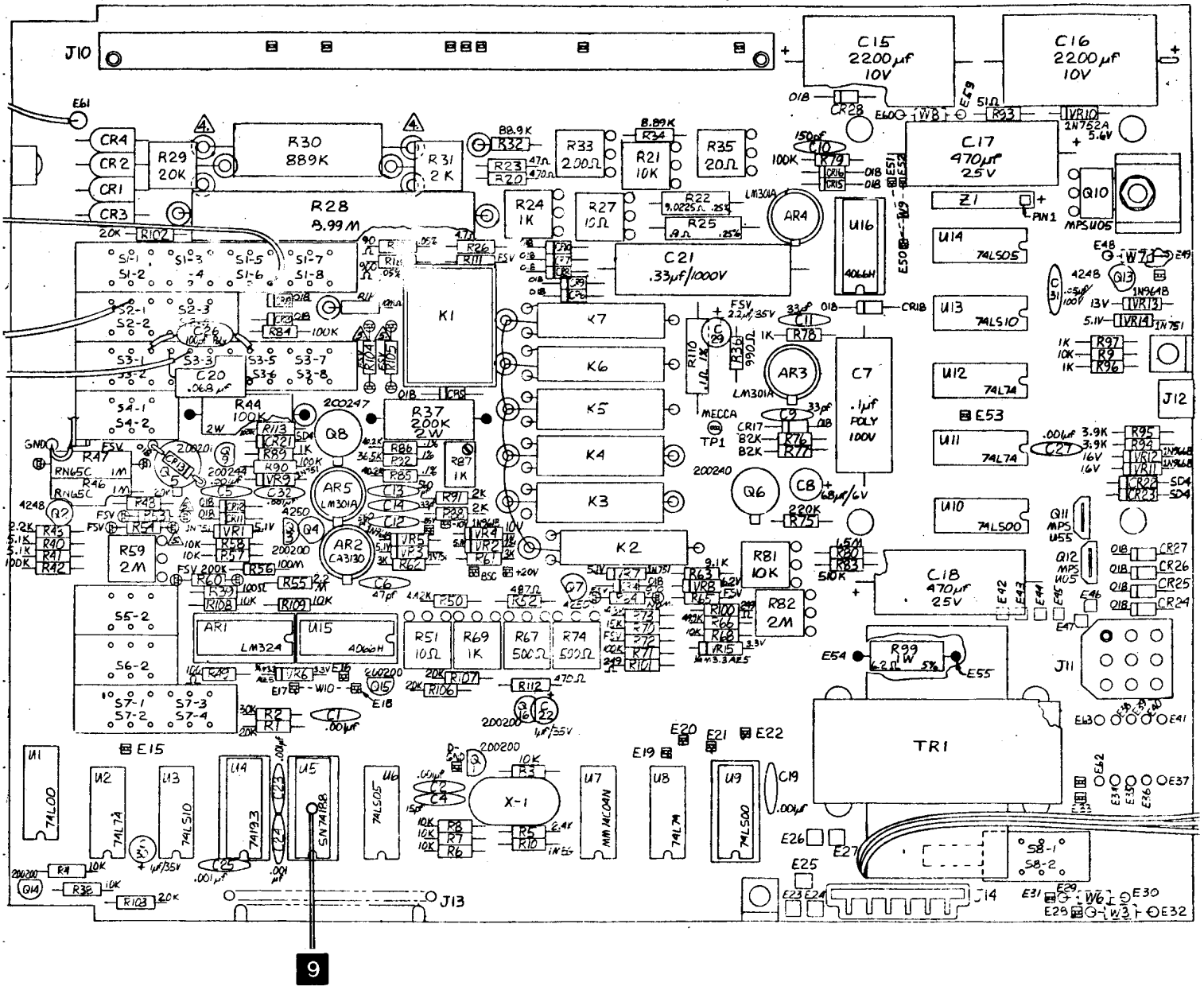


Figure 5.10 - Range and Relay Logic Test Points

ROM INPUT | ROM OUTPUT

= 0.1 Vdc

= 4.1 Vdc

Dig. Com. = Ref

= .085 to .145

= 5.26 to 5.3

A

DC

U5 PIN		IN .2	2	20	200	1K
A	10					
B	11					
C	12		■		■	
D	13			■	■	
E	14					■

U5 PIN		OUT .2	2	20	200	1K
Y1	1	■	■			
Y2	2					
Y3	3			■		
Y4	4				■	
Y5	5					■
Y6	6					
Y7	7					■
Y8	9					

B

AC

Typical for all Inputs

AC · CURRENT

KΩ · CURRENT

R1

R2

R4

U5 PIN		IN .2	2.	20	200	1K
A	10	■	■	■	■	■
B	11					
C	12		■		■	
D	13			■	■	
E	14					■

U5 PIN		OUT .2	2	20	200	1K
Y1	1					
Y2	2					
Y3	3	■	■			
Y4	4			■		
Y5	5				■	
Y6	6					■
Y7	7					■
Y8	9					

Typical for all Outputs

Base of Q1 (K1)

U4-11 ($\overline{\text{LOAD}}$)

K3

K4

K5

K6/K7

$\overline{\text{UPLIMIT}}$

K2

C

KΩ

U5 PIN		IN .2	2.	20	200	2K	20K
A	10						
B	11	■	■	■	■	■	■
C	12		■		■		■
D	13			■	■		
E	14					■	■

U5 PIN		OUT .2	2.	20	200	2K	20K
Y1	1						
Y2	2						
Y3	3					■	
Y4	4				■		
Y5	5			■			
Y6	6	■	■				
Y7	7						■
Y8	9						

D

DCmA

U5 PIN		IN .2	2.	20	200	2K
A	10	■	■	■	■	■
B	11	■	■	■	■	■
C	12		■		■	
D	13			■	■	
E	14					■

U5 PIN		OUT .2	2.	20	200	2K
Y1	1					
Y2	2					
Y3	3		■			
Y4	4			■		
Y5	5				■	
Y6	6					■
Y7	7					■
Y8	9		■			

E

ACmA

U5 PIN		IN .2	2	20	200	2K
A	10	■	■	■	■	■
B	11	■	■	■	■	■
C	12		■		■	
D	13			■	■	
E	14					■

U5 PIN		OUT .2	2	20	200	2K
Y1	1					
Y2	2					
Y3	3		■			
Y4	4			■		
Y5	5				■	
Y6	6					■
Y7	7					■
Y8	9		■			

Figure 5.11 - Range Relay Logic Level Performance Standard

			Relays							ISO Gain		Divider Range Current Source	Current Shunt Resistor	AC Conv ATTN
			K1	K2	K3	K4	K5	K6	K7	X10	X1			
(a)	DC	.2								■				
		2									■			
		20	■		■						■	÷10		
		200	■			■					■	÷100		
		1K	■				■				■	÷1000		
(b)	KΩ	.2						■	■	■		1 mA		
		2						■	■		■	1 mA		
		20					■				■	100 μA		
		200				■					■	10 μA		
		2K			■						■	1 μA		
		20K									■	100 nA		
(c)	AC	.2			■					■				
		2			■						■			
		20				■				■				÷100 K1
		200					■				■			÷100 K1
		1K						■	■		■			÷1000 K2
(d)	DC mA	.2		■						■			909Ω	
		2			■					■			90.9Ω	
		20				■				■			9.09Ω	
		200					■			■			.909Ω	
		2K						■	■	■			.1Ω	
(e)	AC mA	.2		■						■			909Ω	
		2			■					■			90.9Ω	
		20				■				■			9.09Ω	
		200					■			■			.909Ω	
		2K						■	■	■			.1Ω	

□ = OFF

■ = ON

Figure 5.12 - Range Relay Status Chart

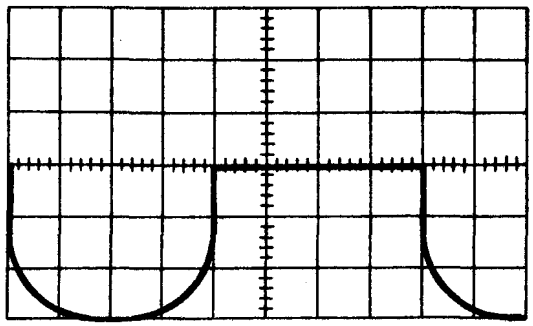
Table 5.20 - Main PCB, Null Detector Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: Auto Input Terminals: J3 (Hi) and J4 (Lo) connected to a +.1 Vdc source					NOTE: All measurements are referenced to TP1 (Mecca). Scope Ext. trig. at S7-3 (N/O)
	Null detector input	CR15 (Cathode)	M	Fig. 5.11	Waveform No. 12
	Null detector output	R79	N	Fig. 5.11	Waveform No. 13
J3 (Hi) and J4 (Lo) connected to a –.1 Vdc source	Null detector input	CR15 (Cathode)	M	Fig. 5.11	Waveform No. 14
	Null detector output	R79	N	Fig. 5.11	Waveform No. 15

Waveforms for Table 5.20

12 (NO.) NULL DETECTOR IN (PLUS SIGNAL)

CR15 (CATHODE)



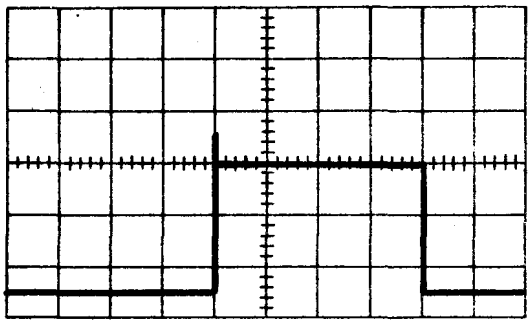
0.2V (V/DIV)

50 MS (S/DIV)

DC COUPLED
REF: MECCA

13 (NO.) NULL DETECTOR OUTPUT

R79



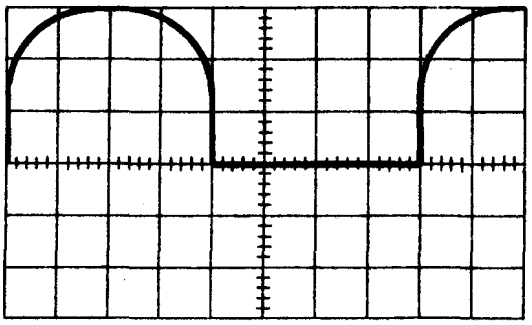
2.0V (V/DIV)

50 MS (S/DIV)

DC COUPLED
REF: MECCA

14 (NO.) NULL DETECTOR IN (MINUS SIGNAL)

CR15 (CATHODE)



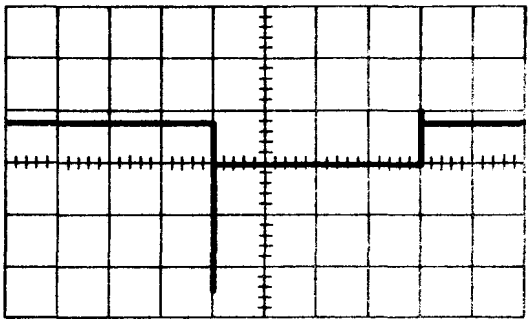
0.2V (V/DIV)

50 MS (S/DIV)

DC COUPLED
REF: MECCA

15 (NO.) NULL DETECTOR OUTPUT

R79



2.0V (V/DIV)

50 MS (S/DIV)

DC COUPLED
REF: MECCA

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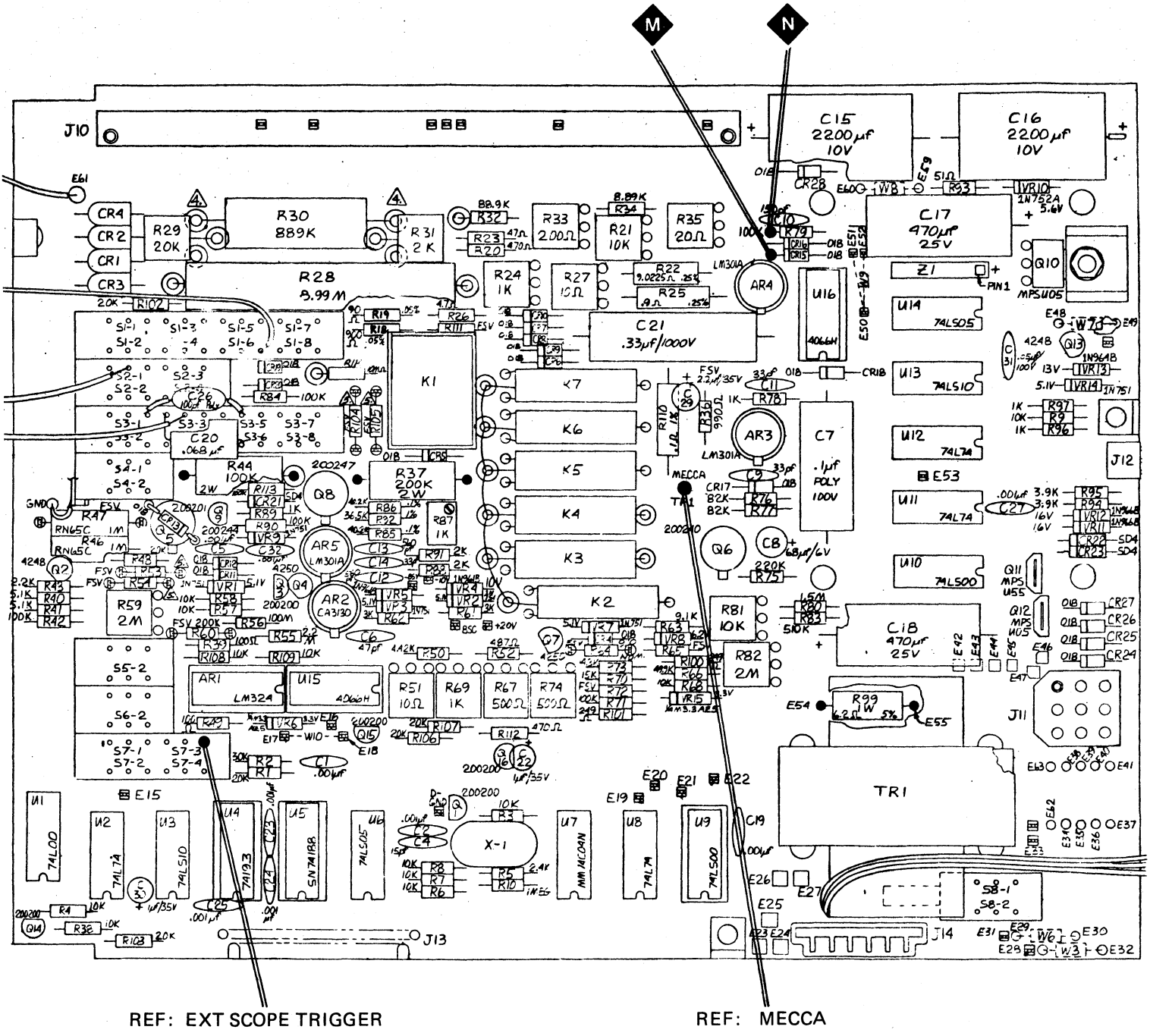


Figure 5.13 - Main PCB Null Detector Test Points

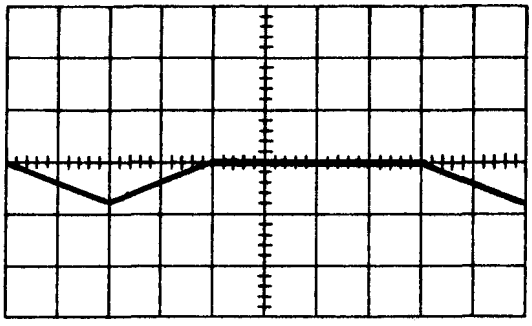
Table 5.21 - Main PCB, Integrator Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: Auto Input Terminals: J3 (Hi) and J4 (Lo) connected to a +.1 Vdc source	Integrator Op Amp non-inverting input	R77	10	Fig. 5.14	NOTE: All measurements are referenced to TP1 (Mecca). Scope Ext. trig. at S7-3 (N/O) +2.5 to +2.7 Vdc
	Integrator Op Amp inverting input	R76	11	Fig. 5.14	+2.5 to †2.7 Vdc
	Integrator Op Amp output	C7	◆	Fig. 5.14	Waveform No. 16
Connect J3 and J4 to a –.1 Vdc source	Integrator Op Amp output	C7	◆	Fig. 5.14	Waveform No. 17

Waveforms for Table 5.21

16 (NO.) INTEGRATOR OUT

C7

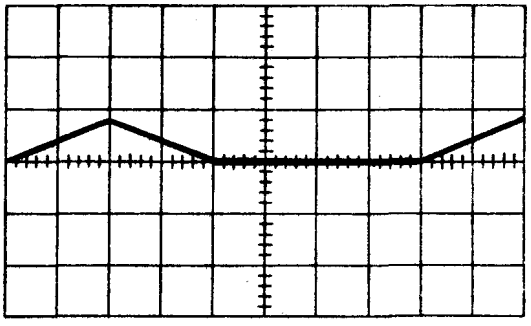


5.0V (V/DIV)

EXT TRIG: S7-3 (N/O)
DC COUPLED
REF: MECCA

50 MS (S/DIV)

17 (NO.)



5.0V (V/DIV)

EXT TRIG: S7-3 (N/O)
DC COUPLED
REF: MECCA

50 MS (S/DIV)

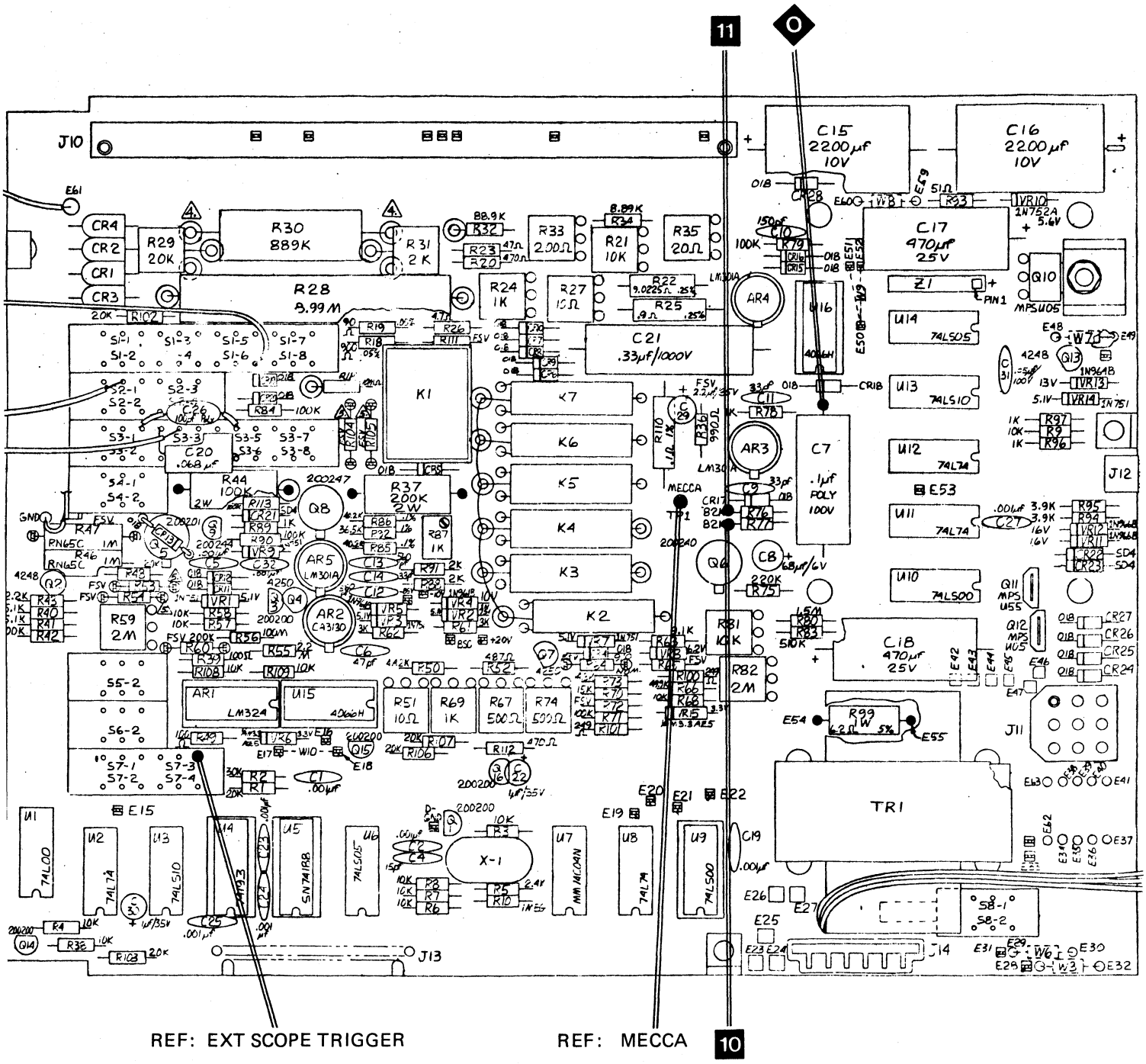


Figure 5.14 - Main PCB Integrator Test Points

Table 5.22 - Main PCB, Isolator/Bootstrap Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: Auto Input Terminals: J3 (Hi) and J4 (Lo) connected with a copper jumper					NOTE: All measurements are referenced to TP1 (Mecca)
	Isolator input	R44	12	Fig. 5.15	+0.0001 to –0.0001 Vdc
	Isolator emitter bias	R55	13	Fig. 5.15	–0.43 to –0.45 Vdc
	Isolator op amp non-inverting input	AR1a – 5	14	Fig. 5.15	+3.75 to +3.85 Vdc
	Isolator op amp inverting input	AR1a – 6	15	Fig. 5.15	+3.75 to +3.85 Vdc
	Isolator op amp output	AR1a – 7	16	Fig. 5.15	+0.00003 to –0.00003 Vdc
	Bootstrap amp output	VR2 (anode)	17	Fig. 5.15	+0.004 to –0.004 Vdc
	+ Bootstrap voltage	VR2 (cathode)	18	Fig. 5.15	+4.90 to +5.10 Vdc
	– Bootstrap voltage	VR3 (anode)	19	Fig. 5.15	–4.90 to –5.10 Vdc
Range: .2	Isolator X10 switch control voltage (on)	U15b – 5	20	Fig. 5.15	+4.7 to +4.8 Vdc
	Isolator X1 switch control voltage (off)	U15a – 13	21	Fig. 5.15	–5.04 to –5.08 Vdc
Range: 2.	Isolator X10 switch control voltage (off)	U15b – 5	20	Fig. 5.15	–5.04 to –5.08 Vdc
	Isolator X1 switch control voltage (on)	U15a – 13	21	Fig. 5.15	+4.7 to +4.8 Vdc
Connect J3 and J4 to a +1 Vdc source	Isolator input	R44	12	Fig. 5.15	+0.9999 to +1.0001 Vdc
	Isolator op amp output	AR1a – 7	16	Fig. 5.15	+1.0190 to +1.0210 Vdc
	+ Bootstrap voltage	VR2 (cathode)	18	Fig. 5.15	+5.870 to +5.880 Vdc
	Bootstrap amp output	VR2 (anode)	17	Fig. 5.15	+1.0030 to +1.0040 Vdc
	Isolator output	e17	22	Fig. 5.15	+0.9999 to +1.0001 Vdc

Table 5.22 continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Connect J3 and J4 to a –0.1 Vdc source, range to .2	Isolator input	R44	12	Fig. 5.15	–0.0999 to –0.1001 Vdc
	Isolator op amp output	AR1a – 7	18	Fig. 5.15	–1.0190 to –1.0210 Vdc
	– Bootstrap voltage	VR3 (anode)	19	Fig. 5.15	–4.99 to –5.2 Vdc
	Bootstrap amp output	VR2 (anode)	17	Fig. 5.15	–0.0950 to –0.0970 Vdc
	Isolator output	e17	22	Fig. 5.15	–0.9998 to –1.0002 Vdc

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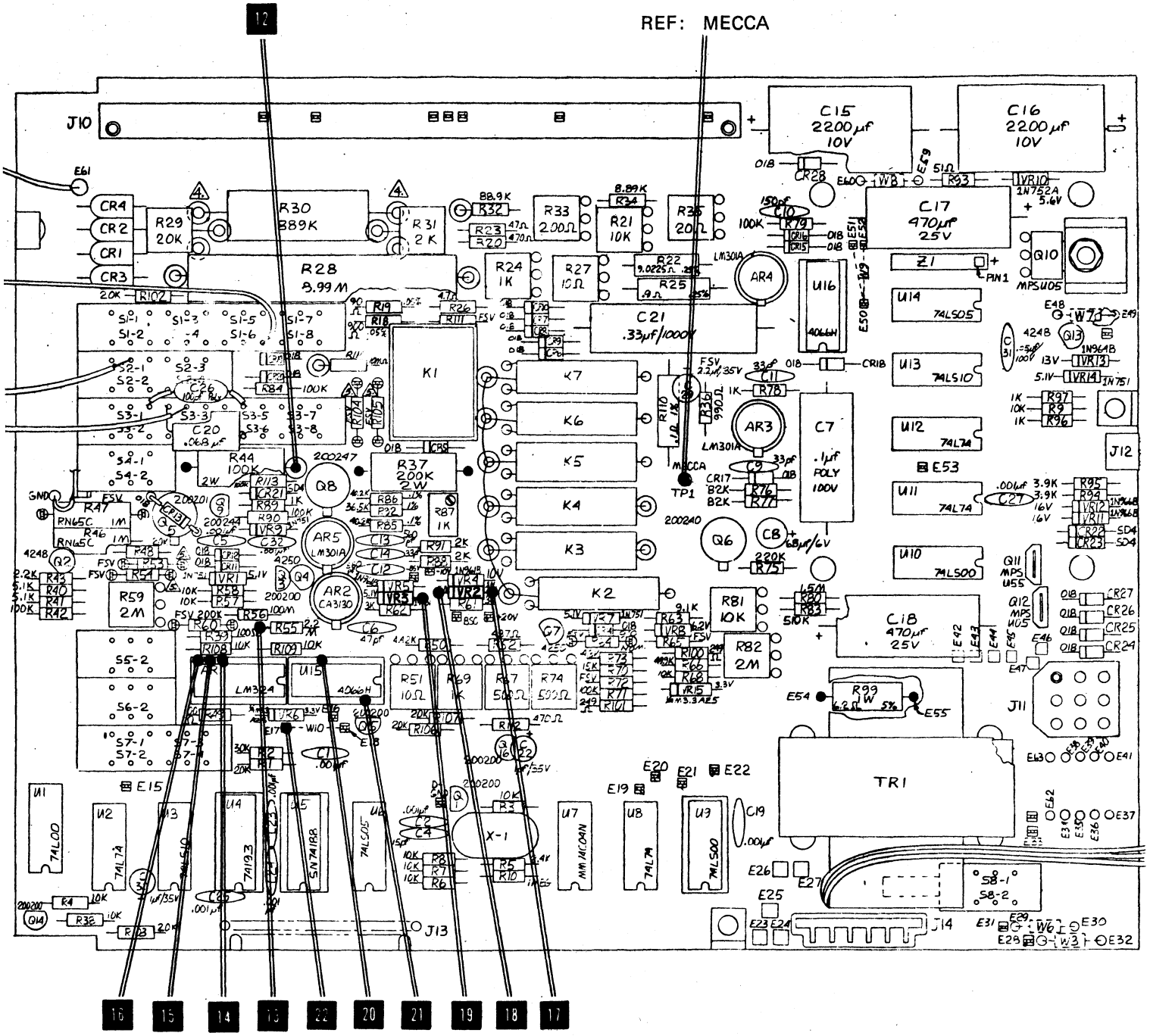


Figure 5.15 - Main PCB Isolator/Bootstrap Test Points

Table 5.23 - Main PCB, KOhms Amplifier Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: Kohms Range: Auto Input Terminals: J3 (Hi) and J4 (Lo) connected with a copper jumper					NOTE: All measurements are referenced to TP1 (Mecca)
	Ohms op amp non-inverting input	R85	23	Fig. 5.16	+8.175 to +8.185 Vdc
	Ohms op amp inverting input	R86	24	Fig. 5.16	+8.175 to +8.185 Vdc
	Ohms op amp output	R89	25	Fig. 5.16	–3.730 to –3.740 Vdc
	Ohms protection bias	R89 (Q9 emitter)	26	Fig. 5.16	–2.560 to –2.580 Vdc
	Ohms protection bias	VR9 (anode)	27	Fig. 5.16	–1.940 to –1.960 Vdc
	Ohms protection bias	CR21 (cathode)	28	Fig. 5.16	–0.550 to –0.570 Vdc
	Ohms output drive	CR21 (anode)	29	Fig. 5.16	+0.0001 to –0.0001 Vdc
	Ohms reference voltage	R36	30	Fig. 5.16	+1.0005 to +1.0020 Vdc
Remove jumper from J3 and J4, set range to .2 – manual	Ohms op amp non-inverting input	R85	23	Fig. 5.16	+2.69 to +2.71 Vdc
	Ohms op amp inverting input	R86	24	Fig. 5.16	+13.38 to +13.41 Vdc
	Ohms op amp output	R89	25	Fig. 5.16	–12.83 to –12.85 Vdc
	Ohms protection bias	R89 (Q9 emitter)	26	Fig. 5.16	–5.97 to –6.00 Vdc
	Ohms protection bias	VR9 (anode)	27	Fig. 5.16	–5.15 to –5.25 Vdc
	Ohms protection bias	CR21 (cathode)	28	Fig. 5.16	–5.95 to –6.00 Vdc
	Ohms output drive	CR21 (anode)	29	Fig. 5.16	–5.46 to –5.48 Vdc

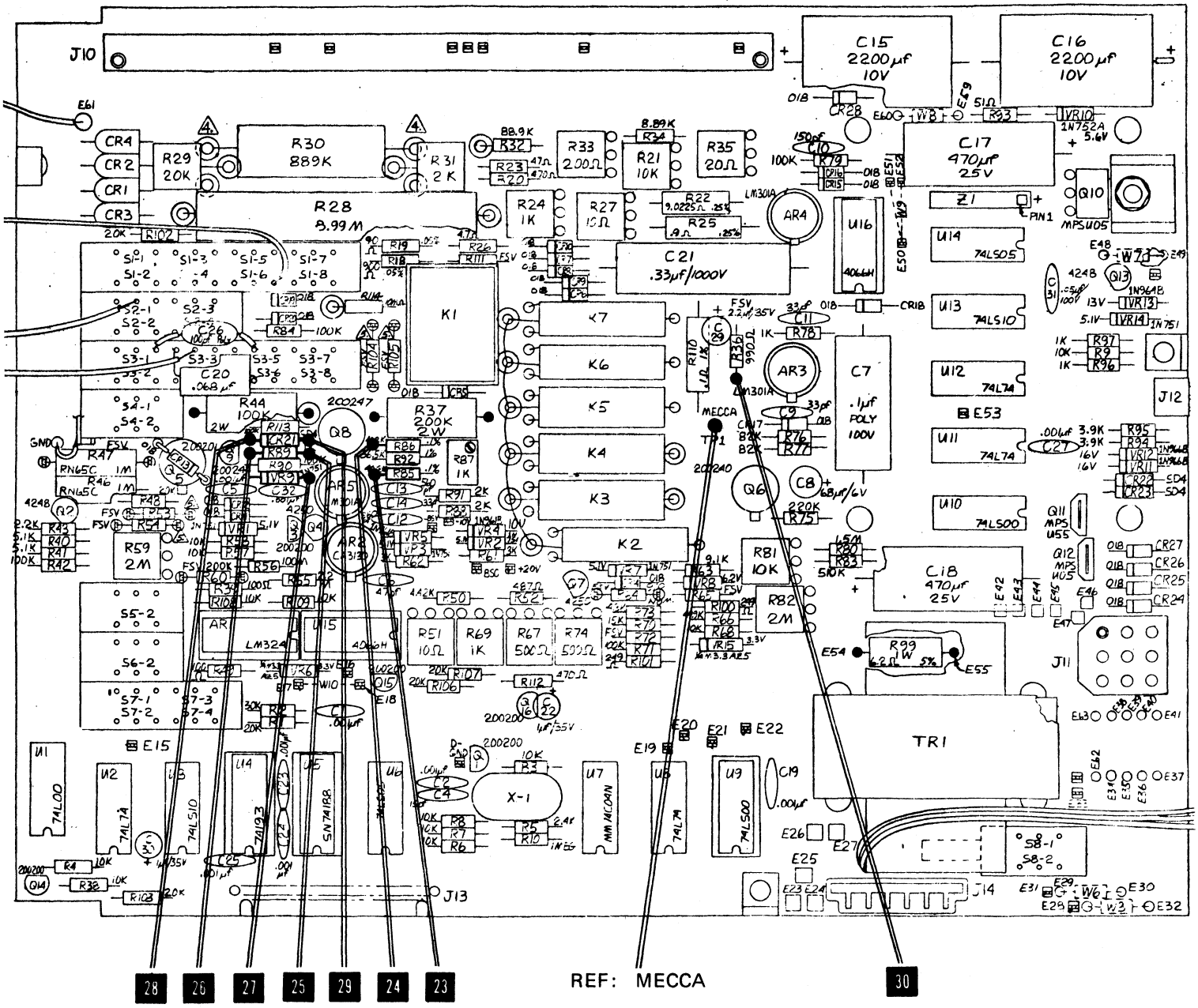


Figure 5.16 - Main PCB KOhm Amplifier Test Points

Table 5.24 - Display Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: Manual .2 Input Terminals: J3 (Hi) and J4 (Lo) connected with a copper jumper					NOTE: All measurements are referenced to digital common scope ext. trig. at S7-3 (N/O)
	+5V	U2-24	1	Fig. 5.17	+4.95 to +5.05 Vdc
	–12V	U2-15	2		–11.95 to –12.05 Vdc
	Clock	U2-1	A	Fig. 5.15	Waveform No. 1
	Q_{e1}	U2-18	B		Waveform No. 2
	Q_{e2}	U2-16	C		Waveform No. 3
Set function to Kohms – open input terminals	$Q_{e2}L$ (O/L)	U2-9	■	Fig. 5.15	low until overrange
	÷100 (step)	U2-11/20/E9	D	Fig. 5.15	Waveform No. 4
	÷2K	U2-19	E		Waveform No. 5 50 Hz ± 5 Hz
	$\overline{\text{Transfer}}$	U2-2	F		Waveform No. 6
	O_A	U2-8	G		Waveform No. 7
	O_B	U2-7	H		Waveform No. 8
	O_C	U2-17	I		Waveform No. 9
	O_D	U2-22/E14	J		Waveform No. 10
	O_E	U2-21	K		Waveform No. 11
	Q_1	U2-4/E5	L		Waveform No. 12
	Q_2	U2-5/E6	M		Waveform No. 13
	Q_4	U2-6/E7	N		Waveform No. 14
	Q_8	U2-10/E8	O		Waveform No. 15
Change input to display + & – polarity	+ Pol	E4	4		Hi = +4.5Vdc = + Pol Lo = +0.25Vdc = –Pol
Manually change ranges in the Kohms function (Range 0 to 5)	R1	E3 (See range and relay	5		High for range 2, 200, & 20,000
	R2	E2 performance - Check)	6		High for range 20 & 200
	R4	E1	7		High for range 2000 & 20,000

Table 5.24 continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	LED 5 Strobe	Q1 collector	P	Fig. 5.15	Waveform No. 17
	LED 4 Strobe	Q2 collector	Q		Waveform No. 18
	LED 3 Strobe	Q3 collector	R		Waveform No. 19
	LED 2 Strobe	Q4 collector	S		Waveform No. 20
	LED 1 Strobe	Q5 collector	T		Waveform No. 21

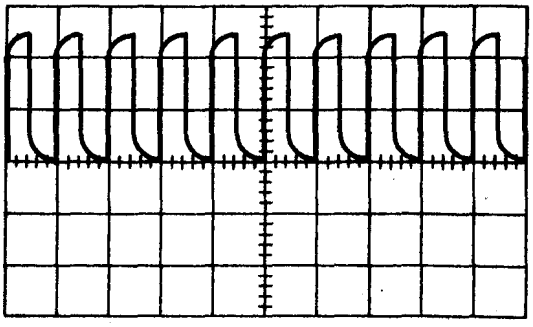
NOTE

To derive counter content connect oscilloscope probe to TP12 and record the HI/LO logic levels as shown in Waveform 12. Then connect the oscilloscope probe to test points 13 through 15 and record the HI/LO content shown for each point. Add the values as shown within waveform grid 16 and the total is the content of the counter.

Waveforms for Table 5.24

1 (NO.) CLOCK

U2-1

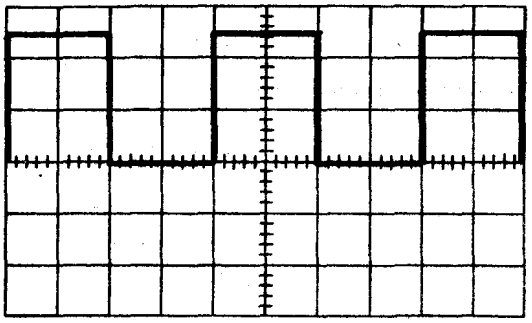


2.0V (V/DIV)

10 μSEC (S/DIV)

2 (NO.) Q_{e1}

U2-18

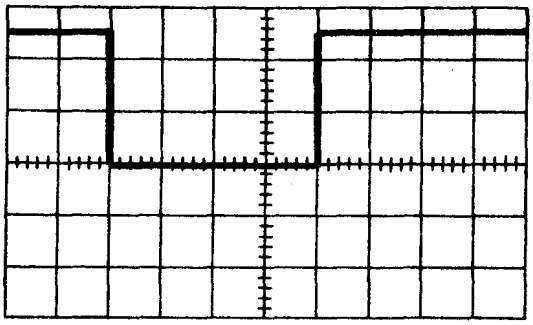


2.0V (V/DIV)

50 MSEC (S/DIV)

3 (NO.) Q_{e2}

U2-16

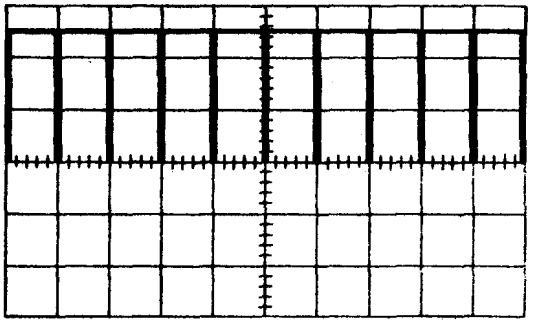


2.0V (V/DIV)

50 MSEC (S/DIV)

4 (NO.) ÷ 100 (STEP)

U2-11/20 or E9

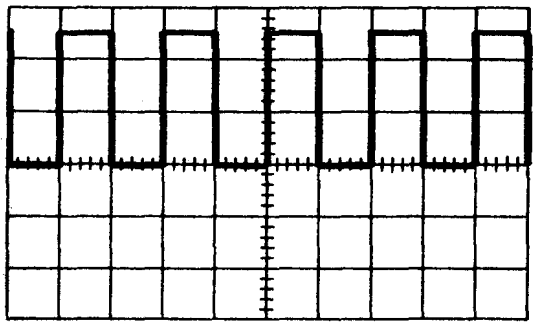


2.0V (V/DIV)

1 MSEC (S/DIV)

5 (NO.) ÷ 2K

U2-19



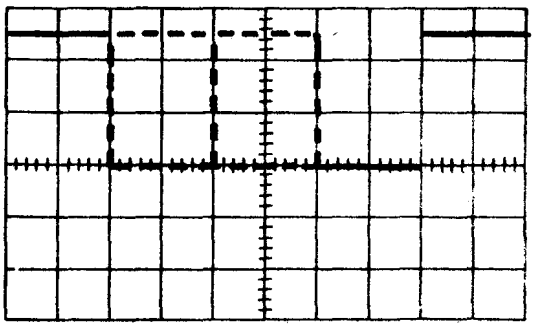
2.0V (V/DIV)

10 MSEC (S/DIV)

6 (NO.) TRANSFER

U2-2

0_{IN} H/S F/S

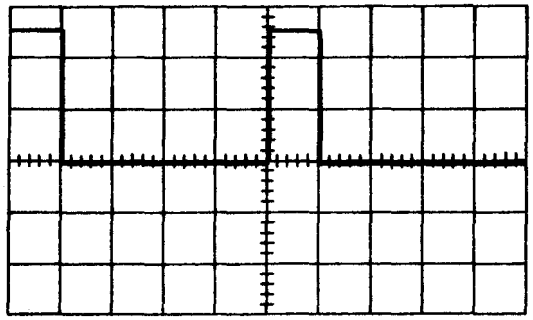


2.0V (V/DIV)

50 MSEC (S/DIV)

7 (NO.) 0_A

U2-8

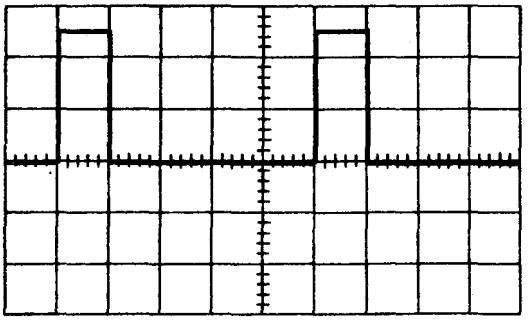


2.0V (V/DIV)

1 MSEC (S/DIV)

8 (NO.) 0_B

U2-7

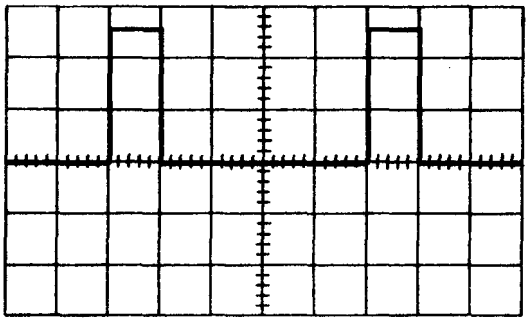


2.0V (V/DIV)

1 MSEC (S/DIV)

9 (NO.) 0_C

U2-17

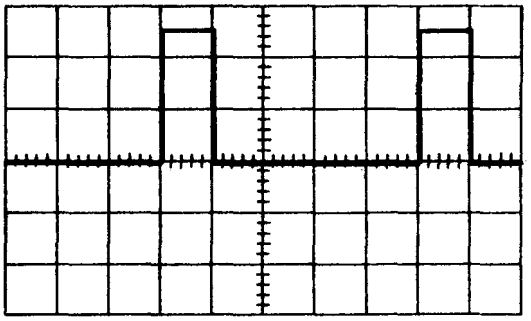


2.0V (V/DIV)

1 MSEC (S/DIV)

10 (NO.) 0_D

U2-22 or E14

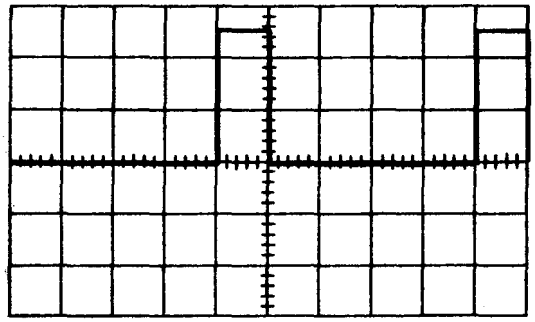


2.0V (V/DIV)

1 MSEC (S/DIV)

11 (NO.) 0_E

U2-21



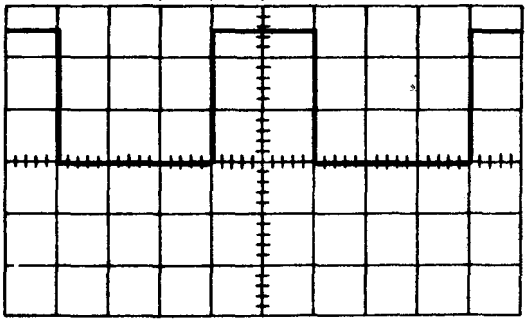
2.0V (V/DIV)

1 MSEC (S/DIV)

EXAMPLE: DIGITAL DISPLAY .18229 KOHMS

12 (NO.) Q_1 (DECIMAL WEIGHT OF 1) U2-4/E5

LSD TO MSD → 1 | 0 | 0 | 0 | 1 ← SINGLE SCAN



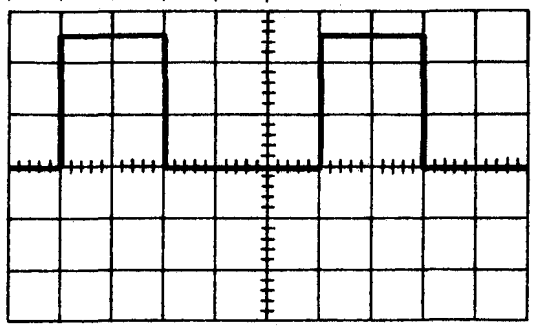
2.0V (V/DIV)

1 MSEC (S/DIV)

EXAMPLE: DIGITAL DISPLAY .18229 KOHMS

13 (NO.) Q_2 (DECIMAL WEIGHT OF 2) U2-5/E6

LSD TO MSD → 0 | 1 | 1 | 0 | 0 ← SINGLE SCAN



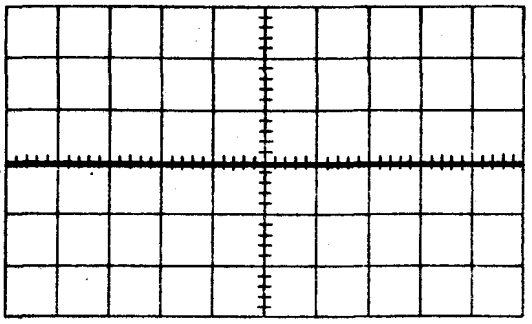
2.0V (V/DIV)

1 MSEC (S/DIV)

EXAMPLE: DIGITAL DISPLAY .18229 KOHMS

14 (NO.) Q_4 (DECIMAL WEIGHT OF 4) U2-6/E7

LSD TO MSD → 0 | 0 | 0 | 0 | 0 ← SINGLE SCAN



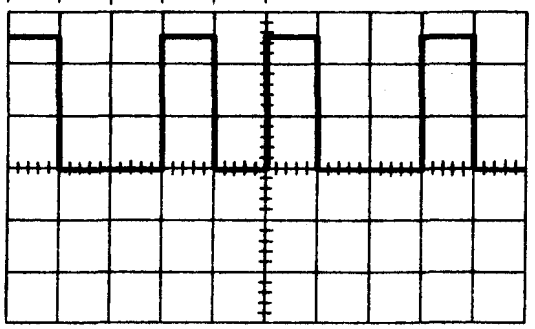
2.0V (V/DIV)

1 MSEC (S/DIV)

EXAMPLE: DIGITAL DISPLAY .18229 KOHMS

15 (NO.) Q_8 (DECIMAL WEIGHT OF 8) U2-10/E8

LSD TO MSD → 1 | 0 | 0 | 1 | 0 ← SINGLE SCAN



2.0V (V/DIV)

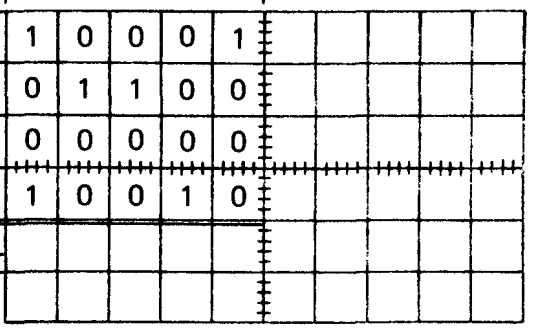
1 MSEC (S/DIV)

SUM OF 12 TO 15

16 (NO.) DIGITAL DISPLAY .18229 KOHMS

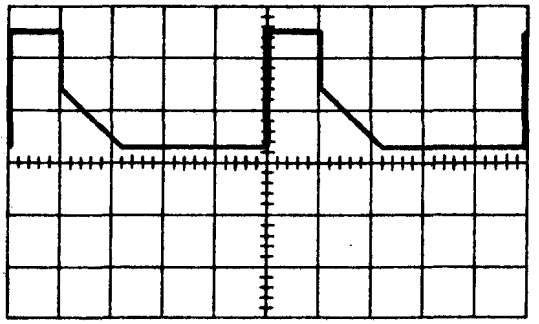
LSD TO MSD → ← SINGLE SCAN

Q_1	1	0	0	0	1
Q_2	0	1	1	0	0
Q_4	0	0	0	0	0
Q_8	1	0	0	1	0
TOTAL					



1M (S/DIV)

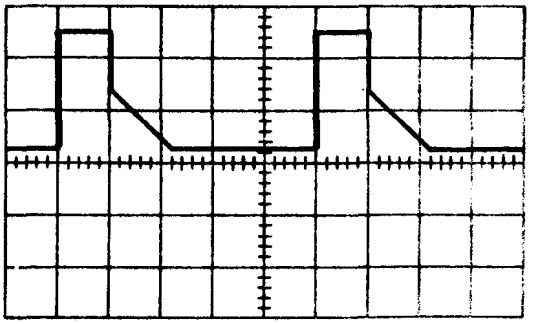
17 (NO.) Q_1 (COLLECTOR) LED 5 STROBE



2.0V (V/DIV)

1 MSEC (S/DIV)

18 (NO.) Q_2 (COLLECTOR) LED 4 STROBE

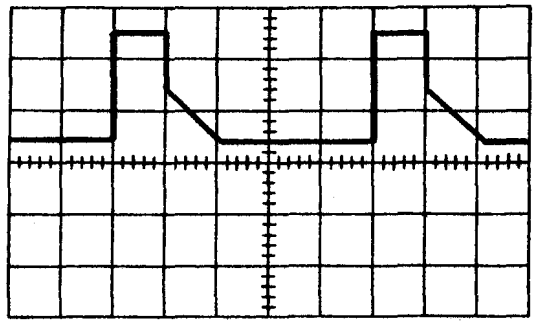


2.0V (V/DIV)

1 MSEC (S/DIV)

Waveforms for Table 5.24 continued

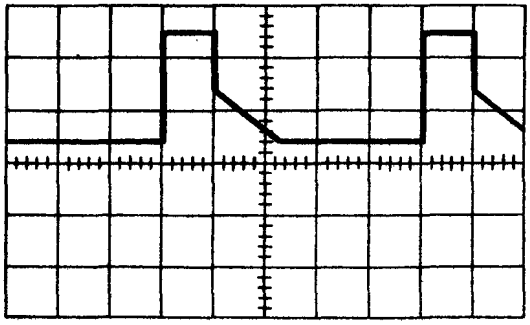
19 (NO.) Q_3 (COLLECTOR) LED 3 STROBE



2.0V (V/DIV)

1 MSEC (S/DIV)

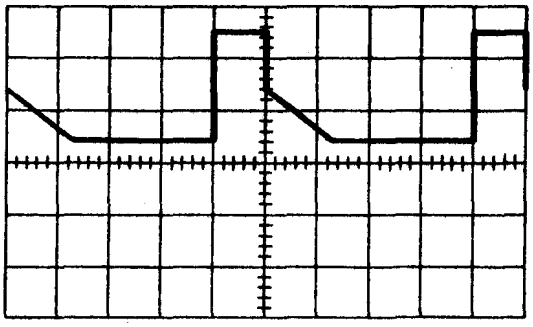
20 (NO.) Q_4 (COLLECTOR) LED 2 STROBE



2.0V (V/DIV)

1 MSEC (S/DIV)

21 (NO.) Q_5 (COLLECTOR) LED 1 STROBE



2.0V (V/DIV)

1 MSEC (S/DIV)

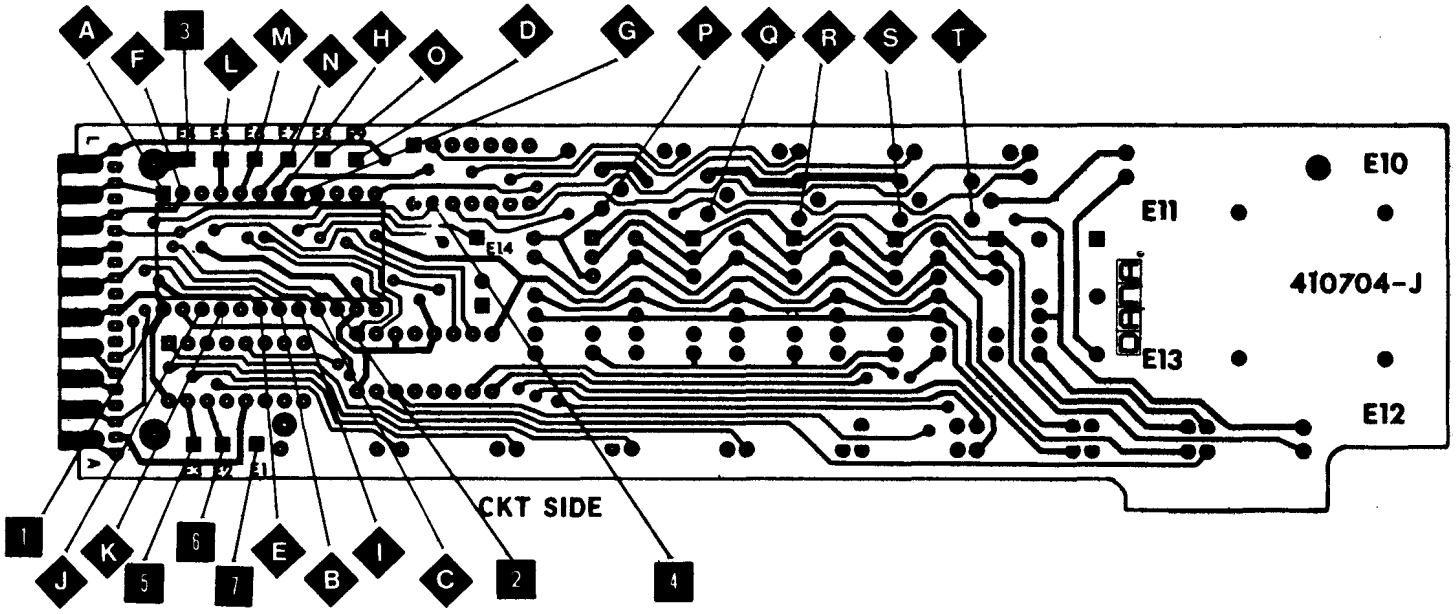


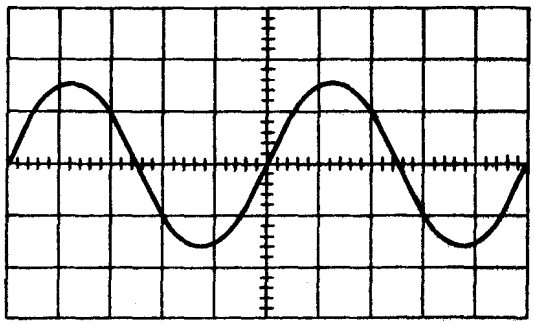
Figure 5.17 - Display Subassembly Test Points

Table 5.25 - AC Converter Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: ACV Range: Auto Input Terminals: J3 (Hi) and J4 (Lo) are connected with a copper jumper					NOTE: All measurements are referenced to TP1 (Mecca)
	Op amp non-inverting input	R11	1	Fig. 5.18	+1.59 to +1.61 Vdc
	Op amp inverting input	R12	2	Fig. 5.18	+1.59 to +1.61 Vdc
	Op amp output	R15/16 junction	3	Fig. 5.18	–0.02 to –0.03 Vdc
	+ Output driver bias	R13/15 junction	4	Fig. 5.18	+13.4 to +13.6 Vdc
	– Output driver bias	R16/17 junction	5	Fig. 5.18	–13.4 to –13.6 Vdc
	Driver output	C15 (minus)	6	Fig. 5.18	–0.85 to –0.95 Vdc
Connect J3 (Hi) and J4 (Lo) to a 1 RMS ACV @ 1 kHz source (2. range)	Op amp output	R15/16 junction	A	Fig. 5.18	Waveform No. 1
	+ output driver signal	R13/15 junction	B	Fig. 5.18	Waveform No. 2
	– output driver signal	R16/17 junction	C	Fig. 5.18	Waveform No. 3
	Driver output	C15 (minus)	D	Fig. 5.18	Waveform No. 4
	+ Rectified output	CR5 (cathode)	E	Fig. 5.18	Waveform No. 5
	– Rectified output	CR6 (anode)	F	Fig. 5.18	Waveform No. 6
	AC Converter output	C17	7	Fig. 5.18	–0.9999 to –1.0001 Vdc

1 (NO.) OP AMP OUTPUT

R15/R16 JUNCTION



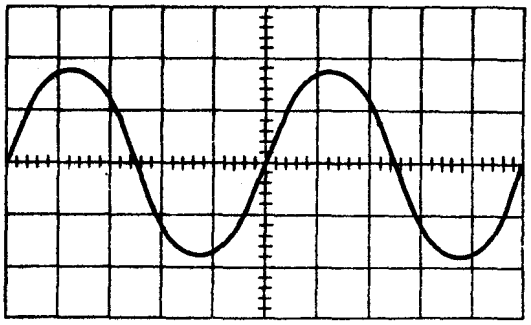
1.0V (V/DIV)

200 µSEC (S/DIV)

AC COUPLED

2 (NO.) POSITIVE OUTPUT DRIVE

R13/R15 JUNCTION



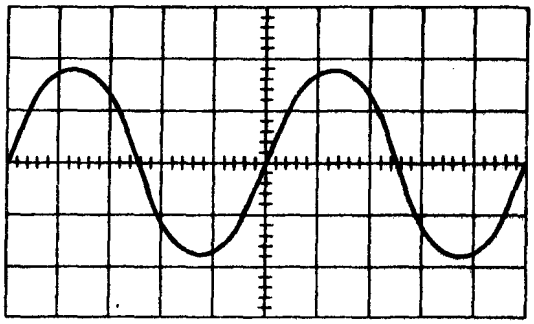
100 MV (V/DIV)

200 µSEC (S/DIV)

AC COUPLED

3 (NO.) NEGATIVE OUTPUT DRIVE

R16/R17 JUNCTION



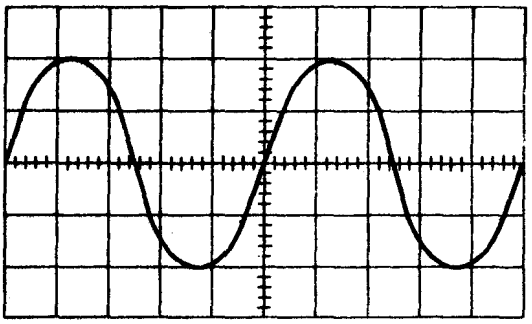
100 MV (V/DIV)

200 µSEC (S/DIV)

AC COUPLED

4 (NO.) DRIVER OUTPUT

C15 (MINUS SIDE)



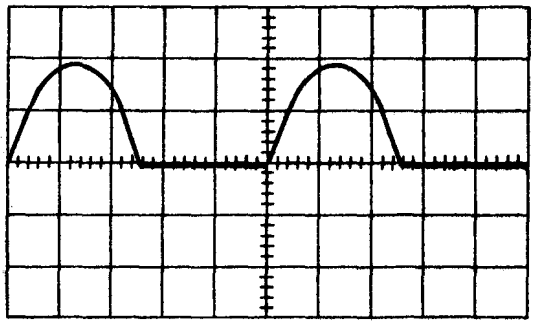
2.0V (V/DIV)

200 µSEC (S/DIV)

AC COUPLED

5 (NO.) POSITIVE RECTIFIED OUTPUT

CR5 (CATHODE)



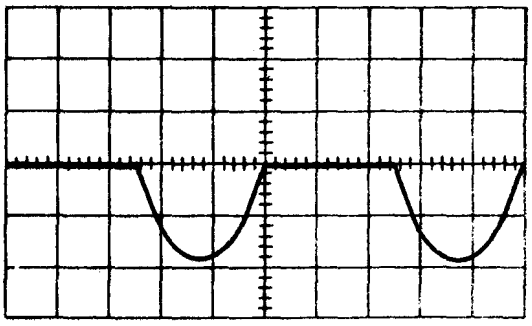
2.0V (V/DIV)

200 µSEC (S/DIV)

DC COUPLED

6 (NO.) NEGATIVE RECTIFIED OUTPUT

CR6 (ANODE)



2.0V (V/DIV)

200 µSEC (S/DIV)

DC COUPLED

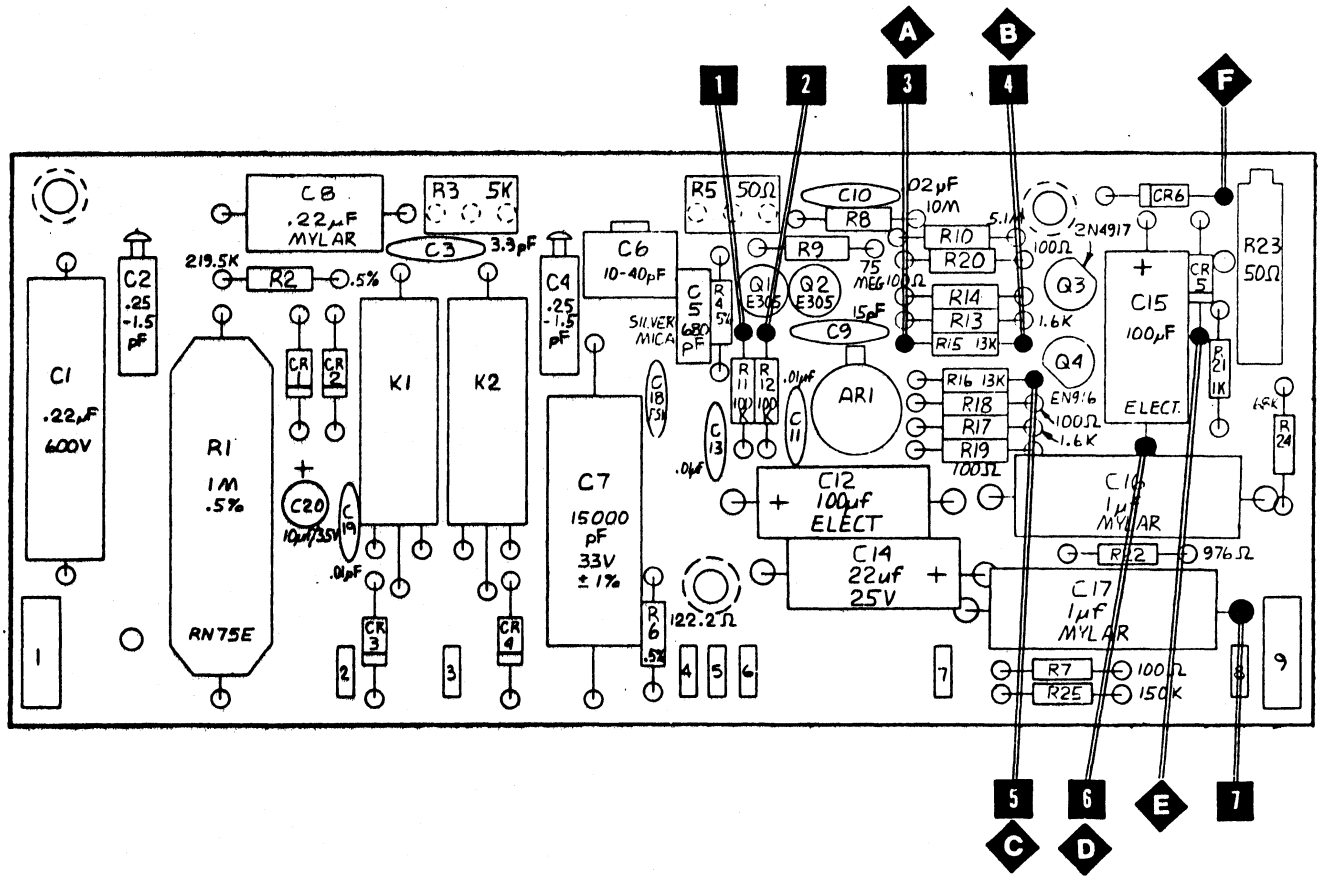


Figure 5.18 - AC Converter Subassembly Test Points

Table 5.26 - Data Output (Opt. 51) Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: Manual (.2) Input Terminals: J3 (Hi) and J4 (Lo) connected with a copper jumper					

Check that all connections to the Data Output PCB are made as shown below.

"E" Term		Color	J1-Pin	Name
Display PCB	Main PCB			
	E22	BLU	9	Transfer
E1		GRN	8	R4
E2		YEL	10	R2
E3		ORG	7	R1
E9		RED	11	÷100 (MUX CLK)
E4		BRN	6	+ Pol
E7		BLK	12	D4
E6		WHT	5	D2
E14		GRY	13	O_D (1K MUX DR)
E8		VIO	4	D_8
E5		BLU	14	D_1
	E15	GRN	3	$\overline{\text{Kohms}}$
	E16	YEL	15	$\overline{\text{ACV}}$
	E20	ORG	2	$\overline{\text{I}}$ (CURRENT)
	E19	RED	16	+5V DC
	E21	BRN	1	DIG. COM.

Connect P8 on Main PCB to J8 on Data Output PCB (isolated supply)

Check following voltage levels, referenced to "–" of C6

Rectified voltage	CR1/CR2 (cathode)	1	Fig. 5.20	+7.9 to +8.2 Vdc
Zener voltage	VR3 (cathode)	2	Fig. 5.20	+5.5 to +5.7 Vdc
Isolated regulator voltage	Q3 (emitter)	3	Fig. 5.20	+4.9 to +5.1 Vdc

Change reference to Digital Common

MUX Clock	U2 pin 1	A	Fig. 5.20	Waveform No. 1
O_D (1K MUX DR)	C3	B	Fig. 5.20	Waveform No. 2
Transfer	C1	C	Fig. 5.20	Waveform No. 3
Data Transfer	U3 pin 6	D	Fig. 5.20	Waveform No. 4
Data Strobe	OCI – 5 pin 1	E	Fig. 5.20	Waveform No. 5

Table 5.26 continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Change reference to (isolated) BCD Common, J202 pin 2, and check:					
	Serial data strobe	U7-5/J202-C	F	Fig. 5.20	Waveform No. 6
	Inhibit parallel data	U7-13/J202-F	G	Fig. 5.20	Waveform No. 7
	Serial data strobe	U7-12/J202-E	H	Fig. 5.20	Waveform No. 8
	Parallel data valid	U7-4/J202-D	I	Fig. 5.20	Waveform No. 9

Check the function code as shown below.

	F_1	F_2	F_4	F_8	Wght
+DCV	0	0	0	0	0
–DCV	1	0	0	0	1
ACV	1	1	0	0	3
+DCI	0	0	1	0	4
–DCI	1	0	1	0	5
ACI	1	1	1	0	7
KΩ	1	0	0	1	9
	18	V	10	L	
	J202				

PCB locations are:
F_1 – U10-4
F_2 – U11-4
F_4 – U12-4
F_8 – U13-4

Check the range code as shown below.

	Range Code			
	R_1	R_2	R_4	Wght
.2	0	0	0	0
2	1	0	0	1
20	0	1	0	2
200	1	1	0	3
2000	0	0	1	4
20,000	1	0	1	5
	19	W	11	
	J202			

PCB locations are:
R_1 – U10-3
R_2 – U11-3
R_4 – U12-3

Table 5.26 continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard

Check the decade numerical code as shown below.

Units		Tens		Hundreds		Thousands		10 Thousands	
1	J202-22	10	J202-20	100	J202-21	1K	J202-16	10K	J202-17
2	J202-Z	20	J202-Y	200	J202-X	2K	J202-T	20K	J202-U
4	J202-14	40	J202-13	400	J202-12	4K	J202-9		
8	J202-8	80	J202-P	800	J202-N	8K	J202-K		

Check the serial 1 output at J202-S or U10-1 (Ext. trig. @ U10-8)
Check the serial 2 output at J202-15 or U11-1 (Ext. trig. @ U11-8)
Check the serial 4 output at J202-8 or U12-1 (Ext. trig. @ U12-8)
Check the serial 8 output at J202-J or U13-1 (Ext. trig. @ U13-8)

} as shown in figure 5.19

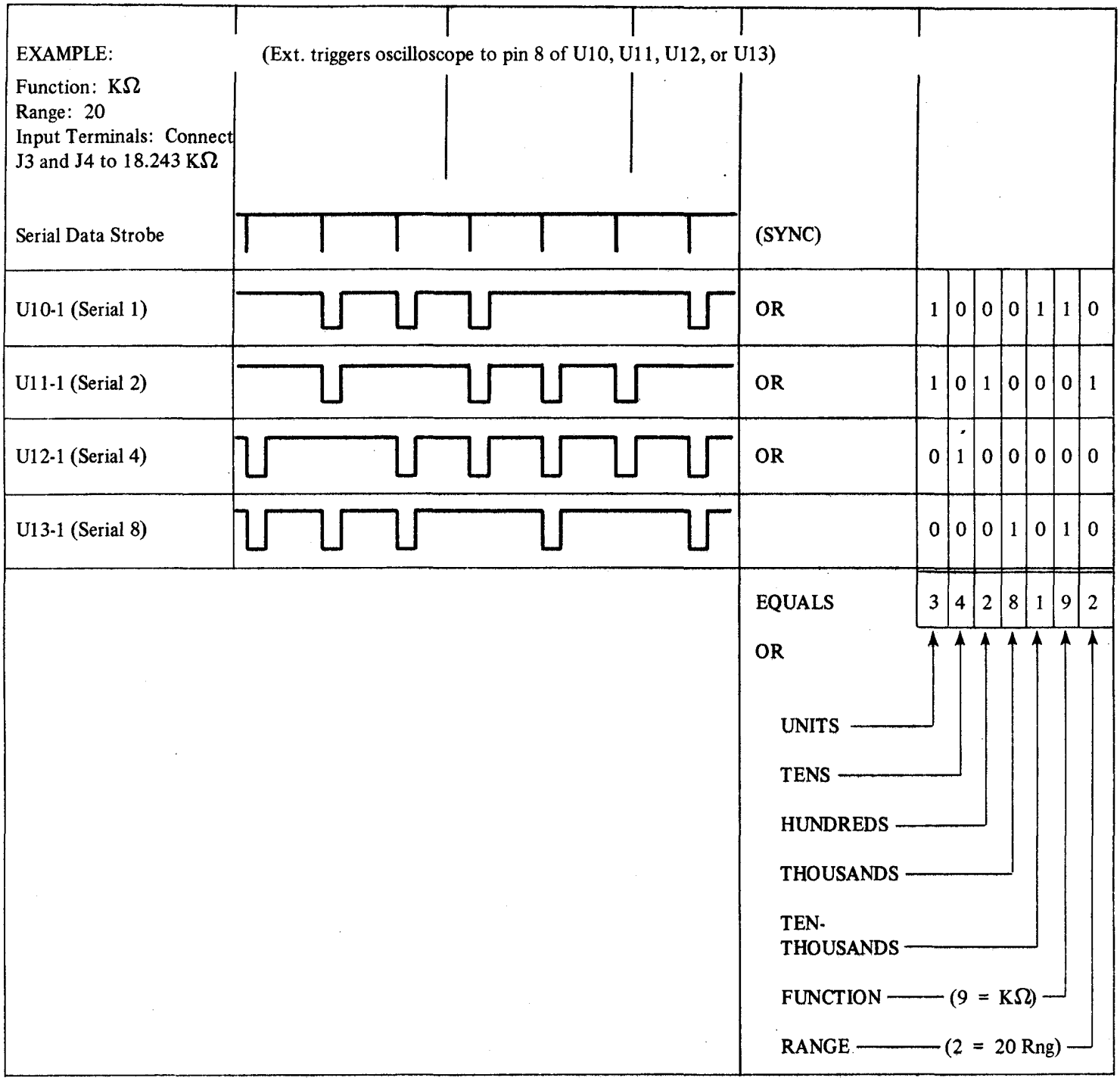
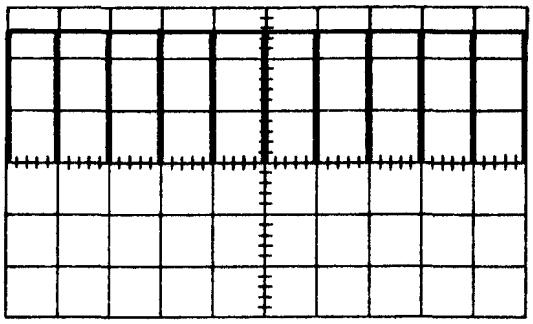


Figure 5.19 - Serial Output Codes

1 (NO.) MUX CLOCK

U2-1



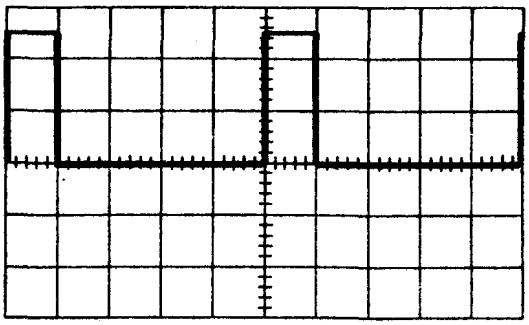
2.0V (V/DIV)

DC COUPLED
REF: DIGITAL COMMON

1 MS (S/DIV)

2 (NO.) 0_D (1 kHz MUX DRIVE)

C3



2.0V (V/DIV)

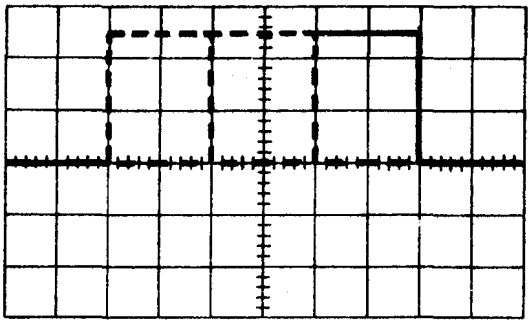
EXT TRIG: S7-3 (N/O)
DC COUPLED
REF: DIGITAL COMMON

1 MS (S/DIV)

3 (NO.) TRANSFER

C1

0V H/S F/S



2.0V (V/DIV)

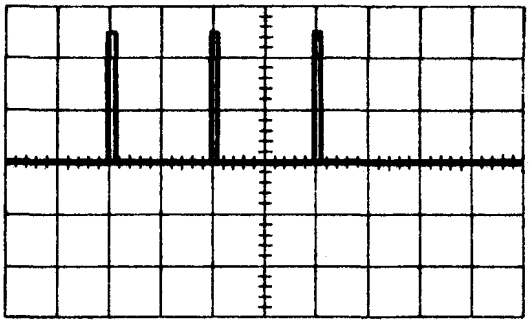
EXT TRIG: S7-3 (N/O)
DC COUPLED
REF: DIGITAL COMMON

50 MS (S/DIV)

4 (NO.) DATA TRANSFER

U3-6

0V H/S F/S



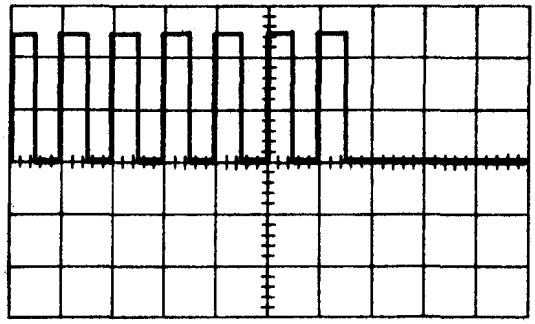
2.0V (V/DIV)

EXT TRIG: S7-3 (N/O)
DC COUPLED
REF: DIGITAL COMMON

50 MS (S/DIV)

5 (NO.) DATA STROBE

OCI-5 PIN 1



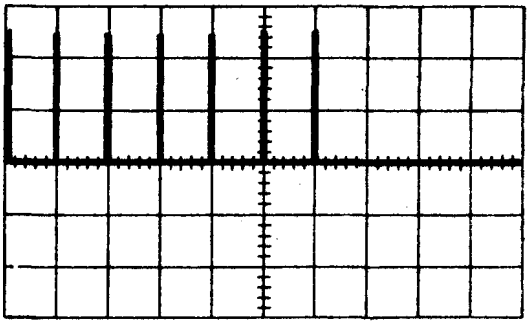
2.0V (V/DIV)

EXT TRIG: S7-3 (N/O)
DC COUPLED
REF: DIGITAL COMMON

1 MS (S/DIV)

6 (NO.) SERIAL DATA STROBE

U7-5 (AT END OF DIGITIZING)
PULSE WIDTH = 40 μS



2.0V (V/DIV)

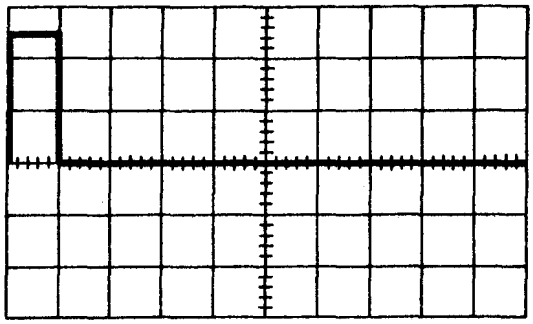
EXT TRIG: S7-3 (N/O)
DC COUPLED
REF: OUTPUT COMMON

1 MS (S/DIV)

Waveforms for Table 5.26

7 (NO.) INHIBIT PARALLEL DATA

U7-3 (AT END OF DIGITIZING)



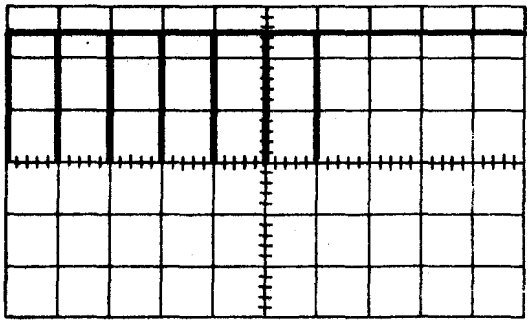
2.0V (V/DIV)

EXT TRIG: S7-3 (N/O)
DC COUPLED
REF: OUTPUT COMMON

10 MS (S/DIV)

8 (NO.) SERIAL DATA STROBE

U7-12 (AT END OF DIGITIZING)
PULSE WIDTH = 40 μS



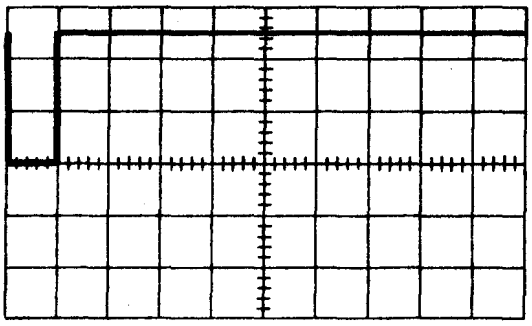
2.0V (V/DIV)

EXT TRIG: S7-3 (N/O)
DC COUPLED
REF: OUTPUT COMMON

1 MS (S/DIV)

9 (NO.) PARALLEL DATA VALID

U7-4 (AT END OF DIGITIZING)



2.0V (V/DIV)

EXT TRIG: S7-3 (N/O)
DC COUPLED
REF: OUTPUT COMMON

10 MS (S/DIV)

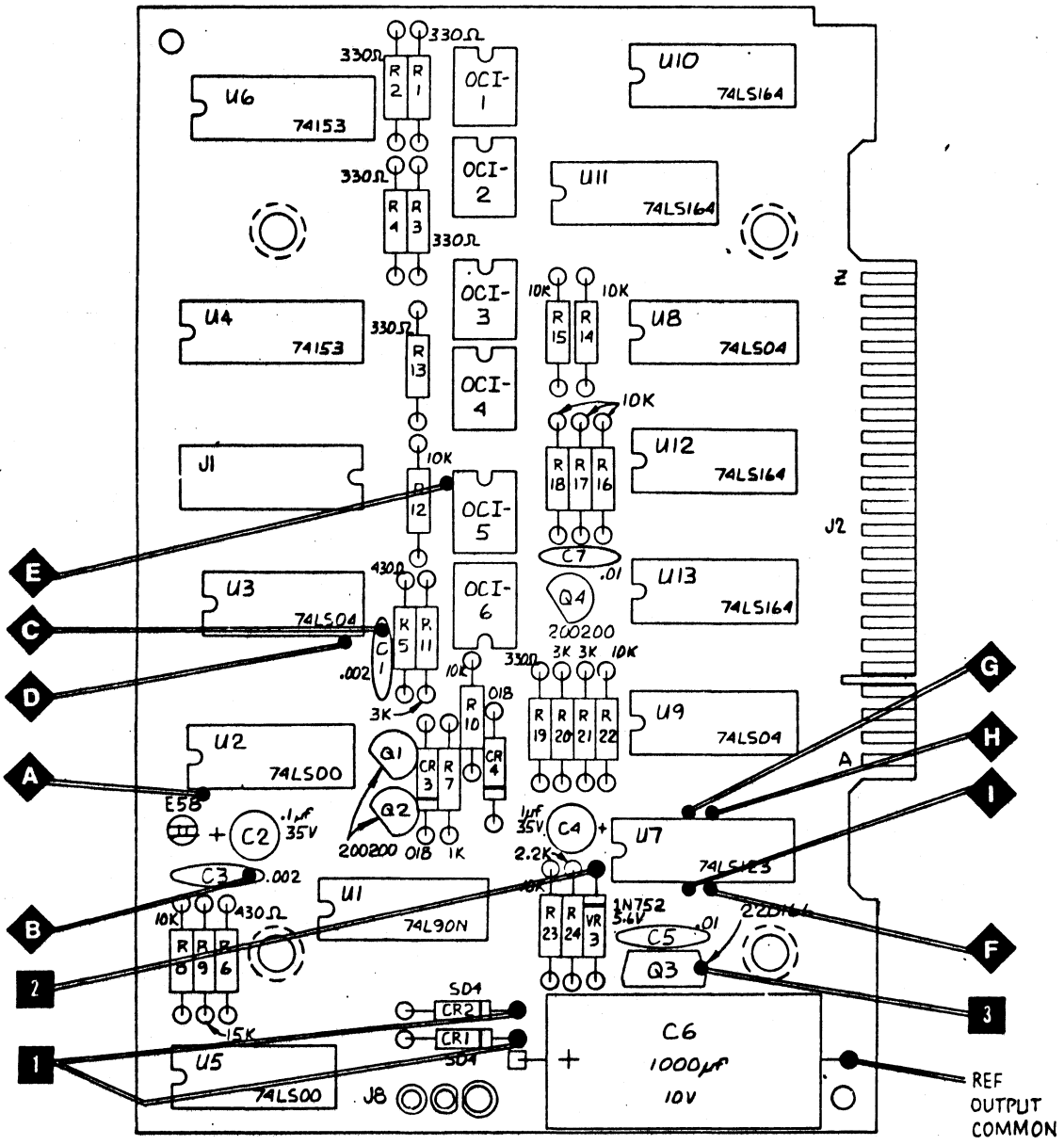


Figure 5.20 - Data Output Subassembly Test Points

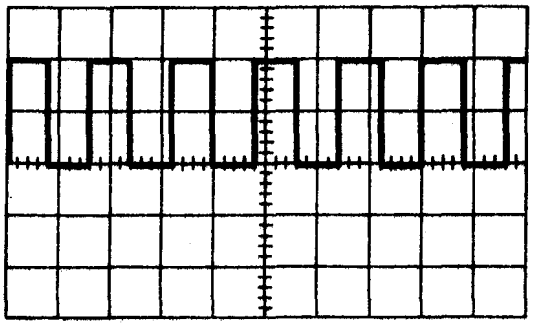
Table 5.27 - Battery Pack (Opt. 70) Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: Auto Input Terminals: J3 (Hi) and J4 (Lo) connected with a copper jumper. Connect power input terminal to line voltage. Power sw. to "on" position.					NOTE: All measurements are referenced to digital common, unless otherwise specified
	Check for normal power supply operating voltages and normal operation on all functions per range.				
Remove power cord from DMM line connector (battery operation)	Mecca	J11 pin 1	1	Fig. 5.21	+4.8 to +5.0 Vdc
	+22 Vdc (ref: mecca)	J11 pin 2	2	Fig. 5.21	+24.0 to +26.0 Vdc
	Battery voltage	J11 pin 3	3	Fig. 5.21	+6.3 to +6.7 Vdc
	Battery voltage switched	J11 pin 4	4	Fig. 5.21	+6.3 to +6.7 Vdc
	–22 Vdc (ref: mecca)	J11 pin 5	5	Fig. 5.21	–15.0 to –16.0 Vdc
	Battery circuit bias	J11 pin 6	6	Fig. 5.21	+6.3 to +6.7 Vdc
	Dig. Com/mecca bias	J11 pin 7	7	Fig. 5.21	+5.5 to +5.8 Vdc
	Dig. Common	J11 pin 8	8	Fig. 5.21	+0.020 to –0.020 Vdc
	Battery "Lo" voltage	J11 pin 9	9	Fig. 5.21	±0.000 Vdc
*Battery Pack PCB Assy.	*Switching transistors	Q4/Q5 collectors	A B	Fig. 5.22	Waveform No. 1
	*Battery pack rectifier Drive	CR4 (cathode) CR6/CR7 (anode)	C D	Fig. 5.22	Waveform No. 2
Set power sw. to "off" and connect power cord to line voltage	Dig. Common rectifier Voltage	CR22/23 (cathode)	10	Fig. 5.21	+9.0 to +9.2 Vdc
	Battery charge voltage	J11 pin 3	3	Fig. 5.21	+5.2 to 8.2 Vdc Voltage drop depends upon battery charge.

Waveforms for Table 5.27

1 (NO.)

SWITCHING TRANSISTORS
Q4 & Q5 (COLLECTORS)
f = 8.8 kHz



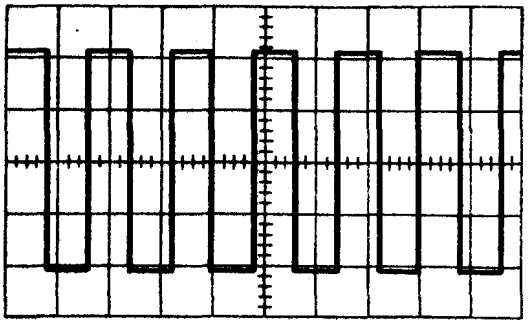
5.0V (V/DIV)

50 µS (S/DIV)

DC COUPLED
REF: DIGITAL COMMON

2 (NO.)

BATTERY PACK RECTIFIER DRIVE
CR4/5 (CATHODES)
CR6/7 (ANODES)



10.V (V/DIV)

50 µS (S/DIV)

DC COUPLED
REF: MECCA

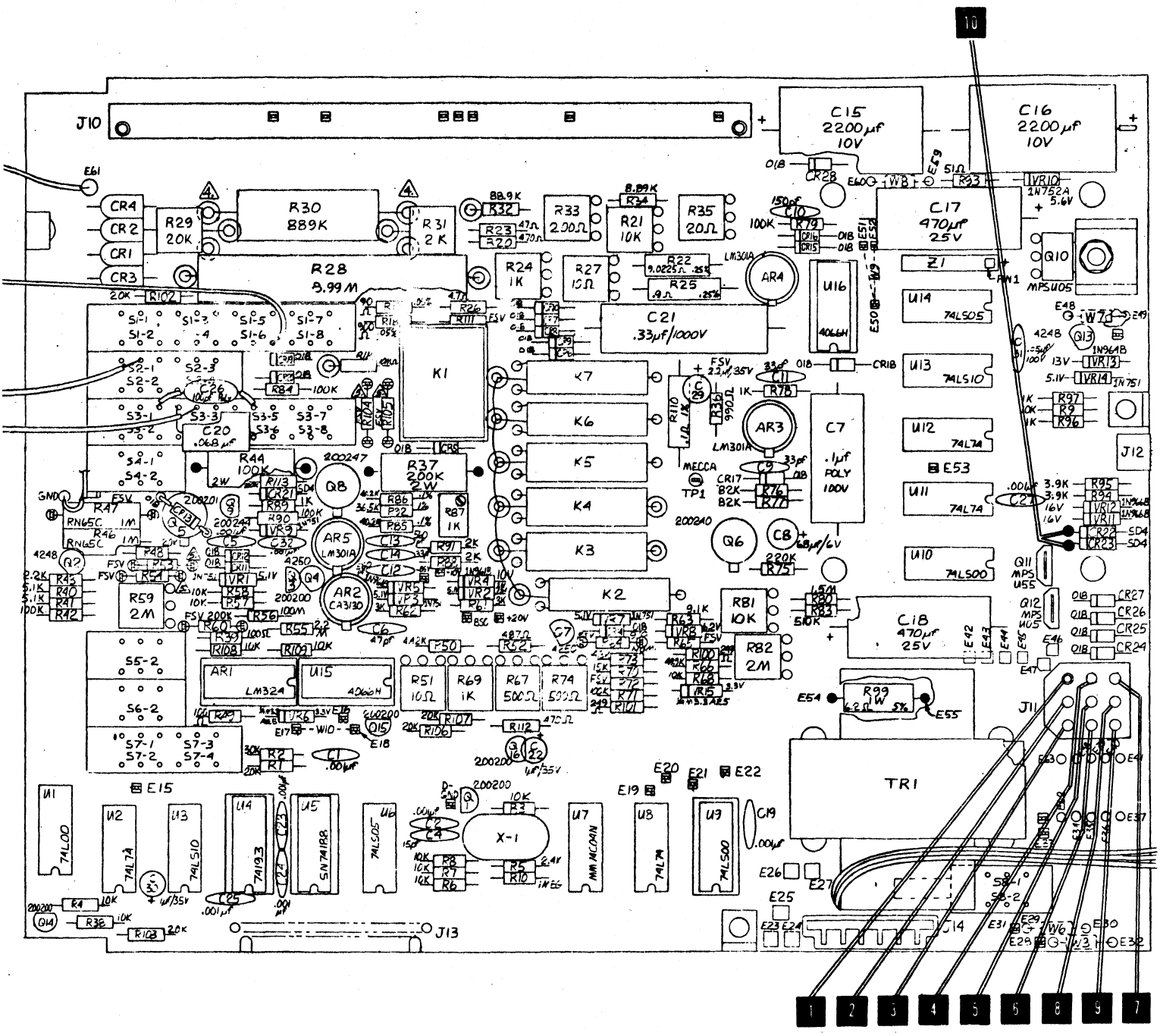


Figure 5.21 - Battery Pack Subassembly Test Points

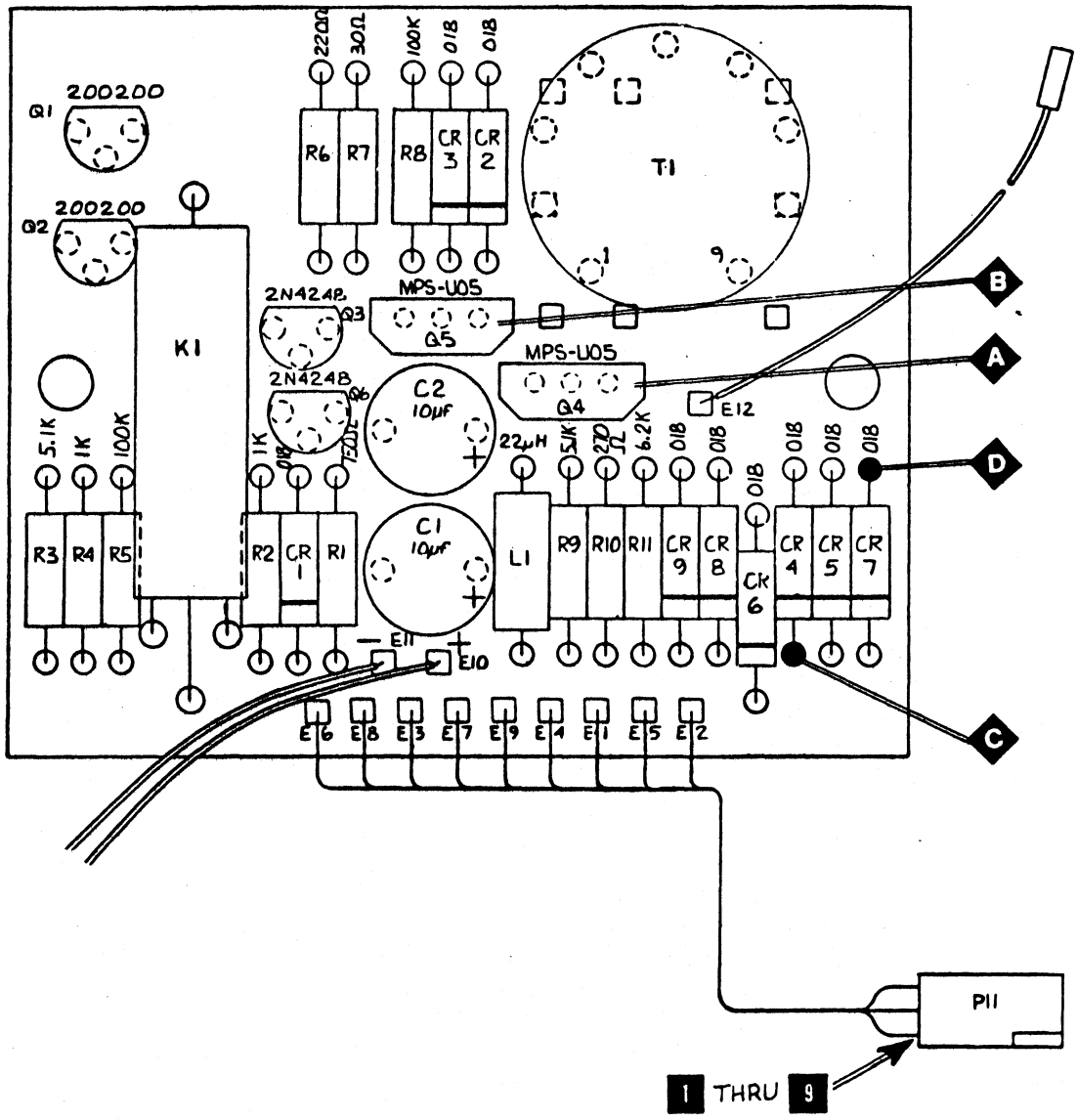


Figure 5.22 - Battery Pack Subassembly Test Points

E		
1	–	R4 DISPLAY INTERCON TO D/O
2	–	R2 DISPLAY INTERCON TO D/O
3	–	R1 DISPLAY INTERCON TO D/O
4	–	+ POL DISPLAY INTERCON TO D/O
5	–	Q1 DISPLAY INTERCON TO D/O
6	–	Q2 DISPLAY INTERCON TO D/O
7	–	Q4 DISPLAY INTERCON TO D/O
8	–	Q8 DISPLAY INTERCON TO D/O
9	–	÷100/STEP DISPLAY INTERCON TO D/O
10	–	+ CURRENT
11	–	+ INPUT
12	–	– CURRENT
13	–	– INPUT
14	–	0_D STROBE DRIVE-DISPLAY
15	–	KOHMS
16	–	AC
17	–	ISOLATOR OUTPUT (TO E18)
18	–	INTEGRATOR INPUT (TO E17)
19	–	+5V (REF: DIG COM)
20	–	I (CURRENT-BAR)
21	–	DIGITAL COMMON
22	–	TRANSFER
23	–	PRIMARY BLK
24	–	PRIMARY BRN
25	–	PRIMARY ORG
26	–	PRIMARY RED
27	–	PRIMARY YEL
28	–	W3 (BATT OP "HI" INPUT (F201)
29	–	W6
30	–	W6
31	–	BATTERY OP "LO" INPUT
32	–	W3 (LINE OP)
33	–	LINE ONLY "HI" INPUT (F201)
34	–	W1 (BATT)
35	–	W2
36	–	W5 (BATT)
37	–	W4 (BATT)
38	–	W1 (BATT)
39	–	W2
40	–	W5 (BATT)

E		
41	–	W4 (BATT)
42	–	DIGITAL COM V10
43	–	MECCA COM BLK
44	–	DIGITAL SEC BLU
45	–	DIGITAL SEC BLU
46	–	ANALOG POWER SEC GRY
47	–	ANALOG POWER SEC GRY
48	–	W7 (LINE OP)
49	–	W7 (LINE OP)
50	–	FEED FWD COMPENSATION (FROM E51/52)
51	–	+ REF SW DRIVE (TO E50)
52	–	– REF SW DRIVE (TO E50)
53	–	HOLD PROBE SW INPUT (TO E58 ON D/O)
54	–	R99
55	–	R99
56	–	R98
57	–	R98
58	–	HOLD ON DATA OUTPUT PCB (TO E53)
59	–	W8 (LINE OP)
60	–	W8 (LINE OP)
61	–	MECCA
62	–	W11 (BATT)
63	–	E63-W11 (BATT)

TP	–	(MAIN PCB)
1	–	MECCA
	–	"–" BSV
	–	"–" 10V
	–	BSC
	–	"+" 20V
	–	DIGITAL COMMON

E	–	(BATTERY PACK ASSY.)
1	–	(P11-1) MECCA
2	–	(P11-2) +22V
3	–	(P11-3) (E10) + BATT VOLTS
4	–	(P11-4) SWITCHED BATT VOLTS
5	–	(P11-5) –22V
6	–	(P11-6) BATT CKT BIAS VOLTS
7	–	(P11-7) DIGITAL VOLTS BASE BIAS
8	–	(P11-8) (E11) DIGITAL COM/BATTERY "–"
9	–	(P11-9) BATT "LO" CONTROL BIAS
10	–	(E3) + BATTERY TERMINAL
11	–	(E8) – BATTERY TERMINAL
12	–	RELAY SWITCH CONTROL (TO E49 M/B)

1. POWER SUPPLY VOLTAGE DEFINITIONS
2. "J" NO. IDENTIFICATIONS
3. "E" NO. IDENTIFICATIONS
4. "TP" NO. IDENTIFICATIONS
5. ERRATA SHEET TO COVER ALL PREVIOUS MANUALS

J		
1	–	"+" CURRENT INPUT (AC & DC)
2	–	"–" CURRENT INPUT (AC & DC)
3	–	NON-EXISTENT
4	–	NON-EXISTENT
5	–	NON-EXISTENT
6	–	NON-EXISTENT
7	–	NON-EXISTENT
8	–	DATA OUTPUT POWER CONN
9	–	INTERCONNECT TO MAIN PCB CONN.
10	–	AC CONVERTER CONN
11	–	BATTERY PACK CONN
12	–	HOLD PROBE CONN
13	–	INTERCONNECT TO DISPLAY CONN
14	–	LINE SELECT JUMPER CONN
201	–	AC LINE CORD CONN
202	–	DATA OUTPUT CONN

F		
101	–	FRONT PANEL mA FUSE CONN
201	–	REAR PANEL LINE FUSE CONN

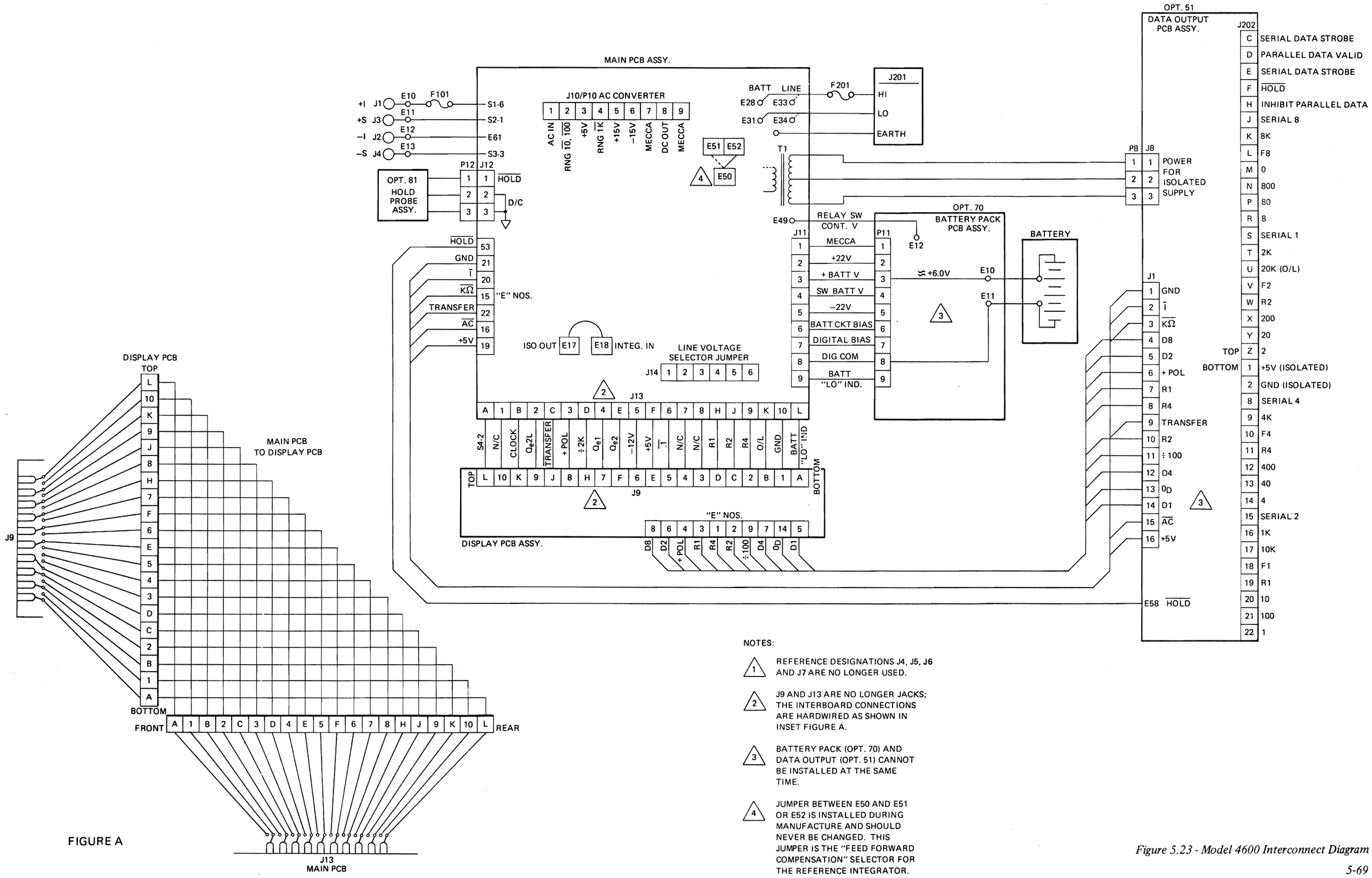


FIGURE A

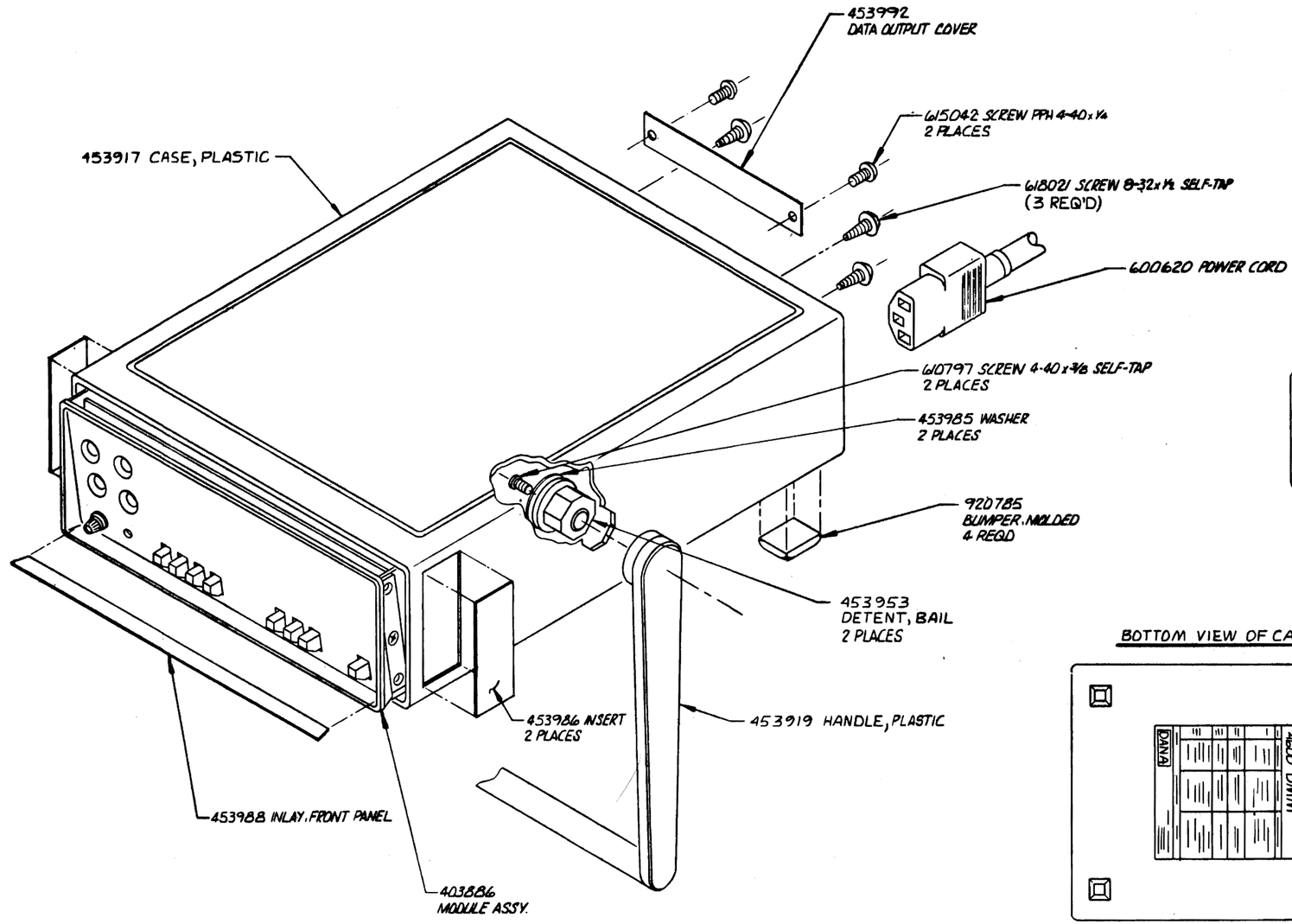
NOTES:

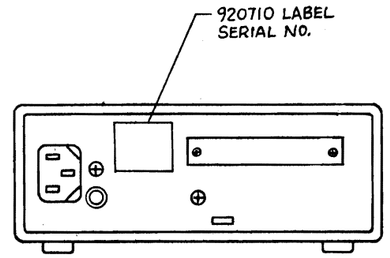
1. REFERENCE DESIGNATIONS J4, J5, J6 AND J7 ARE NO LONGER USED.
2. J9 AND J13 ARE NO LONGER JACKS; THE INTERBOARD CONNECTIONS ARE HARDWIRED AS SHOWN IN INSET FIGURE A.
3. BATTERY PACK (OPT. 70) AND DATA OUTPUT (OPT. 51) CANNOT BE INSTALLED AT THE SAME TIME.
4. JUMPER BETWEEN E50 AND E51 OR E52 IS INSTALLED DURING MANUFACTURE AND SHOULD NEVER BE CHANGED. THIS JUMPER IS THE "FEED FORWARD COMPENSATION" SELECTOR FOR THE REFERENCE INTEGRATOR.

Figure 5.23 - Model 4600 Interconnect Diagram

SECTION 6 DRAWINGS

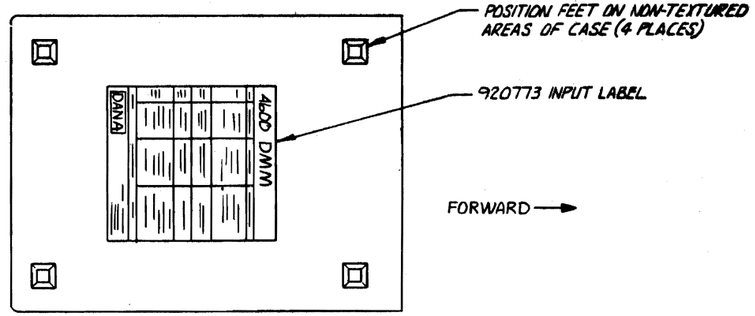
REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPD
A	RELEASED PER DRN # 1113	1/3/76		
B	REVISED PER E.O.# 10039	3/29/76	5-5-76	
C	REVISED PER E.O.# 10211	4-19-76		
D	EO 10444			





REAR VIEW OF CASE

BOTTOM VIEW OF CASE



NEXT DWG	USED ON	NEXT DWG	FINAL ASST	
APPLICATION		QTY REQD		

UNLESS OTHERWISE SPECIFIED DIMENSIONS IN MILLIMETERS AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
.X ±.5 .XX ±.25	0° 30' FORMED 1° 0'	+.10 −.05

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL

FINISH

DRAWN	R Henderson	7/3/75
CHECK		
DESIGN	R Henderson	7/3/75
MECH ENGR		
PROJ ENGR		7/3/75
MFG ENGR		4-5-76
Xc		

DANA® DANA LABORATORIES INC.
IRVINE, CALIFORNIA

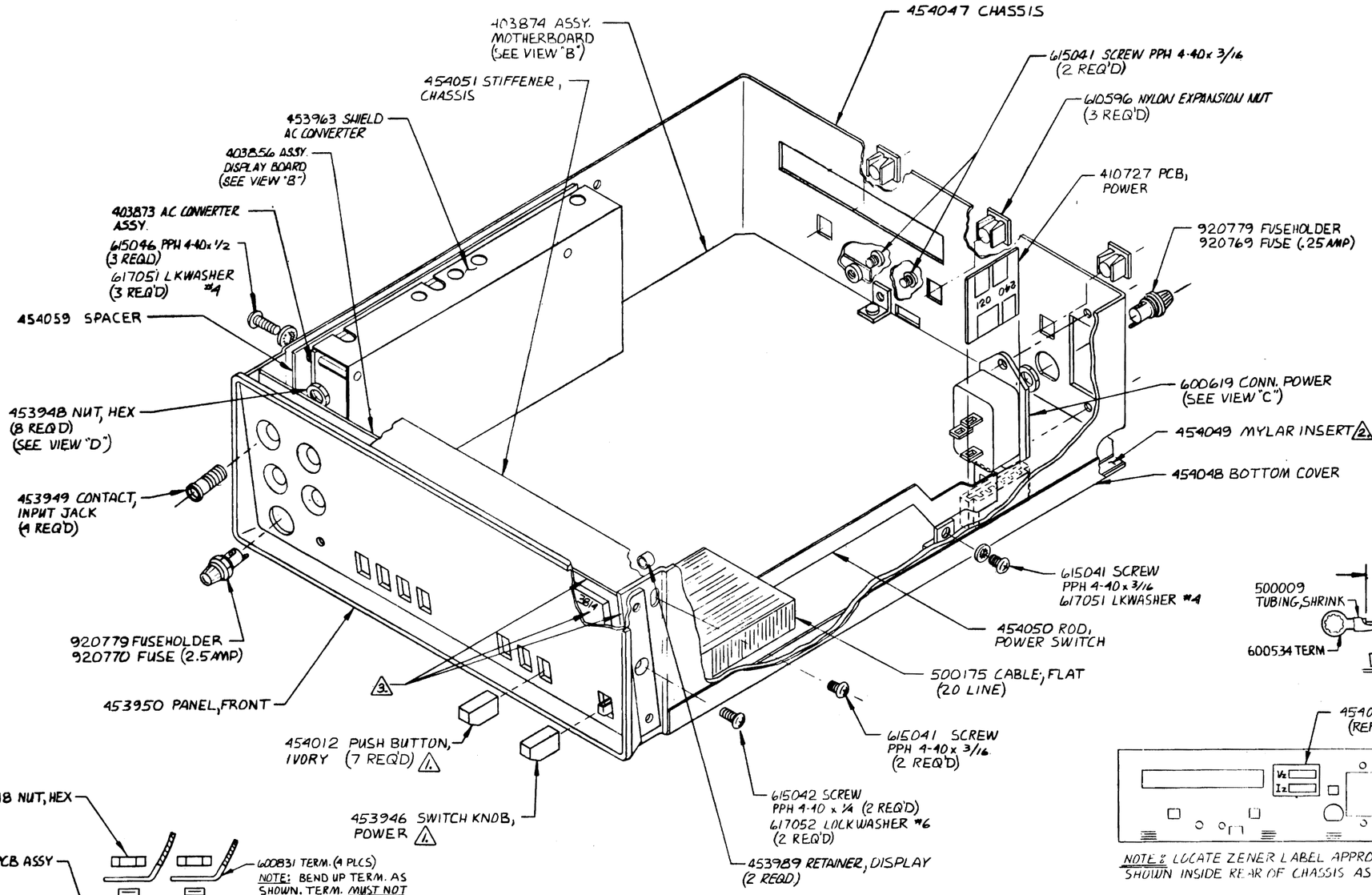
TOP ASSEMBLY
4600

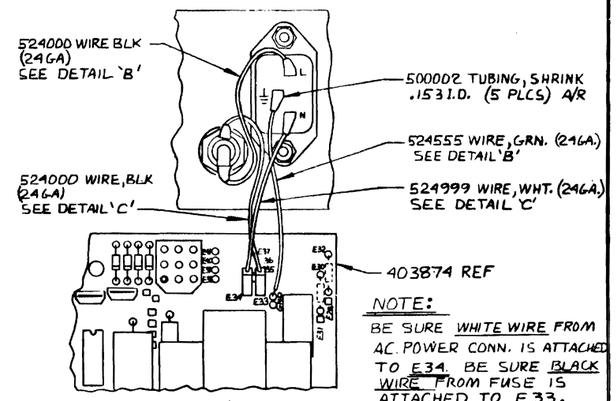
SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	400977	D

SCALE NONE | SHEET 1 OF 2

T	REVISED PER E.O.# 10472	RLH 8-31-76	DCP 9-7-76	
U	REVISED PER E.O. # 10494	RLH 9-1-76	DCP 9-20-76	
V	REVISED PER E.O. # 10536	RLH 9-27-76	DCP 11-4-76	

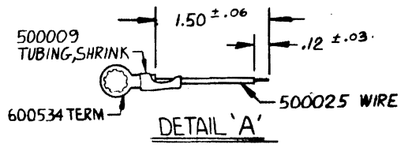
REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPD
C	RELEASED PER DRN # 1113 (orig)	1/31/74		
D	REVISED PER E.O. # 9890	1/29/74 A.L.H.	2/6/74	
E	REVISED PER E.O. # 9946	2/6/74 RLH	2/11/74	
F	REVISED PER E.O. # 9987	2/19/74 RLH	2/22/74	
H	REVISED PER E.O. # 10039	4/26/74 RLH	5-2-74 DCP	DCP 5/14/74
J	REVISED PER E.O. # 10090	4-29-74 RLH	5-2-74 DCP	DCP 5/14/74
K	REVISED PER E.O.# 10196	RLH 5-23-74		DCP 6/13/74
L	REVISED PER E.O.# 10211	RLH 5-21-74		DCP 6/13/74
M	REVISED PER E.O.# 10221	RLH 5-23-74		
N	REVISED PER E.O.# 10251	RLH 5-23-74		DBC 6/14/74
P	REVISED PER E.O.# 10269	RLH 6-11-74		6/15/74
R	REVISED PER E.O.# 10291	DCP 7-1-74		DBC 7/1/74
S	REVISED PER E.O.# 10359	DCP 8-1-74		DBC 8/1/74





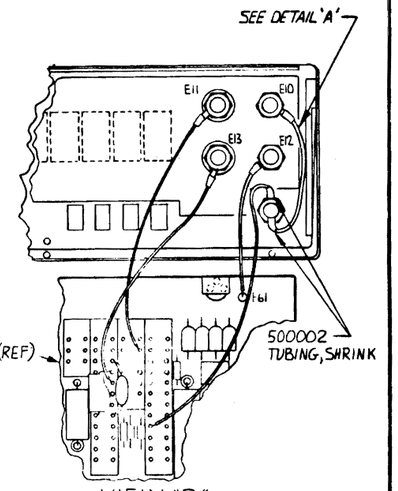
VIEW "C"

NOTE:
BE SURE WHITE WIRE FROM AC POWER CONN. IS ATTACHED TO E34. BE SURE BLACK WIRE FROM FUSE IS ATTACHED TO E33. FOR LINE OPERATED DMM'S ONLY.

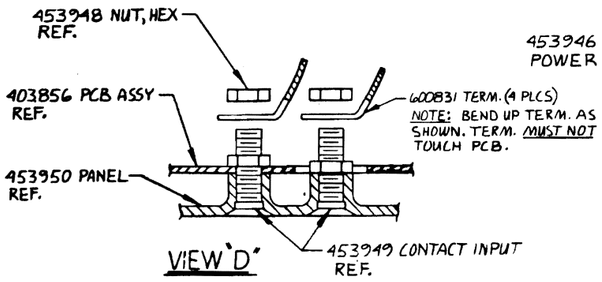


DETAIL 'A'

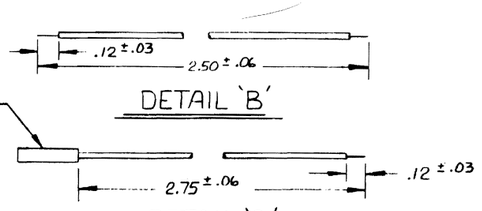
NOTE 2. LOCATE ZENER LABEL APPROX AS SHOWN INSIDE REAR OF CHASSIS AS SHOWN.



VIEW "B"



VIEW "D"



DETAIL 'B'

DETAIL 'C'

2. MYLAR INSERT TO BE GLUED TO BOTTOM COVER USING 920789 SPRAY ADHESIVE.

1. BUTTONS TO BE GLUED TO SWITCHES USING 920504 (4475 SCOTCH GRIP) CEMENT.

3. USE A BLACK "MARKS-A-LOT" TO BLACKEN THE LEADING EDGE OF STIFFENER & THE LEADING EDGES OF CHASSIS & THE 3814 CHIP ON THE DISPLAY BOARD.

400977	4600	1	1
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS X.030 XX.020 XXX.010 | ANGLES 0° 30' FORMED 1° 0' | HOLE DIAMETERS +.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL

FINISH

DRAWN	R. Henderson	7/24/75
CHECK		
DESIGN	R. Henderson	7/24/75
MECH ENGR	DICK PAYNE	7/12/74
PROJ ENGR		7/18/76
MFG ENGR		7/23/76

Xc

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

MODULE ASSY. 4600

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403886	V

SCALE NONE | SHEET 1 OF 4

ARTEKMEDIA => 2012

610234 BIF. TERM. (14 REQD)
500060 SLEEVING 18GA. A/R
600747 SOCKET, RELAY
610744 STANDOFF, HEX
600750 CLIP, GROUND
600786 POST, MACHINE APPLIED (7 REQ'D)
453900 GUIDE PIN
SEE DETAIL "E"
610234(2) BIFURCATED TERMINALS
920482 SOCKET 8-PIN 4 REQD (AR2,3,4,5)
600786 POST (E50,51,52)
SEE DETAIL "C"
500060, SLEEVING (18GA) A/R
454046 HEATSINK
600766 TEFLON TERM. (19 REQD)
500025 WIRE (20GA) LENGTH 2.0 IN. SEE DETAIL "A"
E12 DISPLAY PCB
600831 TERM. (2)
920781 PAD, TRANS
500025 WIRE (20GA.) LENGTH 2.5 IN. SEE DETAIL "A"
FUSE FR. PANEL
500009 TUBING, SHRINK (3 PLCS)
454065 SWITCH ASSY, (FUNCTION)
E11 DISPLAY PCB
600831 TERM. (2)
E13 DISPLAY PCB
500025 WIRE (20GA.) LENGTH 2.5 IN. SEE DETAIL "A"
524999 WIRE LENGTH .75 IN. SEE DETAIL "A"
SEE DETAIL "B"
454067 SWITCH ASSY, (RANGE)
920734 SOCKET (14-PIN) 4 REQ'D (AR1, U15, U16, U9)
524999 WIRE LENGTH 2.0 IN. SEE DETAIL "A"
600786 POST
600829 CONNECTOR (4 REQ'D)
600828 CONTACT (4 REQ'D)
410711 PCB (REF.)
DETAIL "C"
615044 SCREW 4-40 x 1/4
617004 NUT, HEX
617102 WASHER, FLAT
(INSERT SCREW FROM BOTTOM OF PCB)
600245 JUMPER 4 REQD
(W3, W6, W7, W8)
(INSTALL JUMPERS ON BOTTOM OF PCB)
600786 POST
453402 BRKT RT. ANGLE
610177 RIVET
600789 CONN. (3 PIN)
CEMENT CR13 TO TOP OF Q5 USING 920540 (SCOTCH 4475) CEMENT.
500060 18GA. SLEEVING A/R
DETAIL "B"
NOTE: THE GLASS BODY OF CR13 MUST MAKE CONTACT WITH METAL CAN OF Q5.
600786 POST
410711 PCB
FEMALE PIN
600656 CONN. (MOLEX 9-PIN)
454038 SPACER
SEE SHT. 2 FOR WIRING LIST FOR TR1.
600786 POST
600380 PIN, MALE
600379 CONN. (3 PIN MOLEX)
VIO
BLU
BLU
600381 PIN, FEMALE 2 REQ'D
SEE DETAIL "H" FOR SECURING CABLE ASSY.
600778 SWITCH, POWER (DO NOT USE SPACER UNDER SWITCH.)
W3, W6 TO BE INSTALLED ON BOTTOM OF P.C.B.
600821 CONN.
600786 POST
453402 BRACKET
610077 RIVET
610080 WASHER
(SEE DETAIL "F") Pg. 2
920735 SOCKET, 16-PIN (2 REQD)
SEE DETAIL "C"
600786 POST
(FOR PIN DESCRIP.) (SEE PAGE 5-69)
J13
DETAIL "A"
.25 ±.03 IN. (TYP.)
LENGTH SPECIFIED ± .25 IN.

PCB REV	LTR	DESCRIPTION	DR	CHK	APPD
	D	RELEASED PER DRN # 1113			
	E	REVISED PER E.O. # 9889			
	F	REVISED PER E.O. # 9946			
	H	REVISED PER E.O. # 9968			
	J	REVISED PER E.O. # 10018			
	K	REVISED PER E.O. # 10038			
M	L	REVISED PER E.O. # 10075			
M	M	REVISED PER E.O. # 10090			
N	N	REVISED PER E.O. # 10102			
N	P	REVISED PER E.O. # 10165			
P	R	REVISED PER E.O. # 10221			
R	S	REVISED PER E.O. # 10250			
S	T	REVISED PER E.O. # 10268			
S	U	REVISED PER E.O. # 10310			
S	V	REVISED PER E.O. # 10380			
T	W	# 10425			
T	Y	# 10450			
T	Z	# 10468			
T	AA	# 10469			
T	AB	# 10470			
T	AC	# 10471			
T	AD	# 10534			
T	AE	# 10548			

3. ●-THIS SYMBOL ON COMP. LEADS INDICATES COMP. IS TO BE RAISED .125 IN. ABOVE PCB.
2. USE PANDUIT CRIMPING TOOL NO. CT-100.
1. SCHEMATIC REF. 432087
NOTES: UNLESS OTHERWISE SPECIFIED.

5. USE 600245 JUMPER (4 PLCS) R53, 54, 104, 105 T/C FSV ESTABLISHED.
4. HOOKSPLICE BUSSWIRE TO MIDDLE LEAD OF R29 & R30 PRIOR TO STUFFING.
6. ADD BACK TO BACK CAPS BETWEEN BSC AND MECCA (R52) 2.2μFD, 35V, P/N 110125. MAY NOT BE ON ALL ASSEMBLYS. THEY ARE DESIGNATED C33 AND C34.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING
TOLERANCES
DECIMALS X.030 XX.020 XXX.010
ANGLES 0° 30' FORMED 1° 0'
HOLE DIAMETERS +.004 −.001
DIMENSIONS AND TOLERANCES PER USAS Y14.15
MATERIAL
FINISH

DRAWN	R. Henderson	10/27/75	
CHECK			
DESIGN	R. Henderson	10/27/75	
MECH ENGR			
PROJ ENGR		11/3/76	
MFG ENGR		11/3/76	
Xc			

403886	4600-D24	1	1
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

DANA DANA LABORATORIES INC. IRVINE, CALIFORNIA

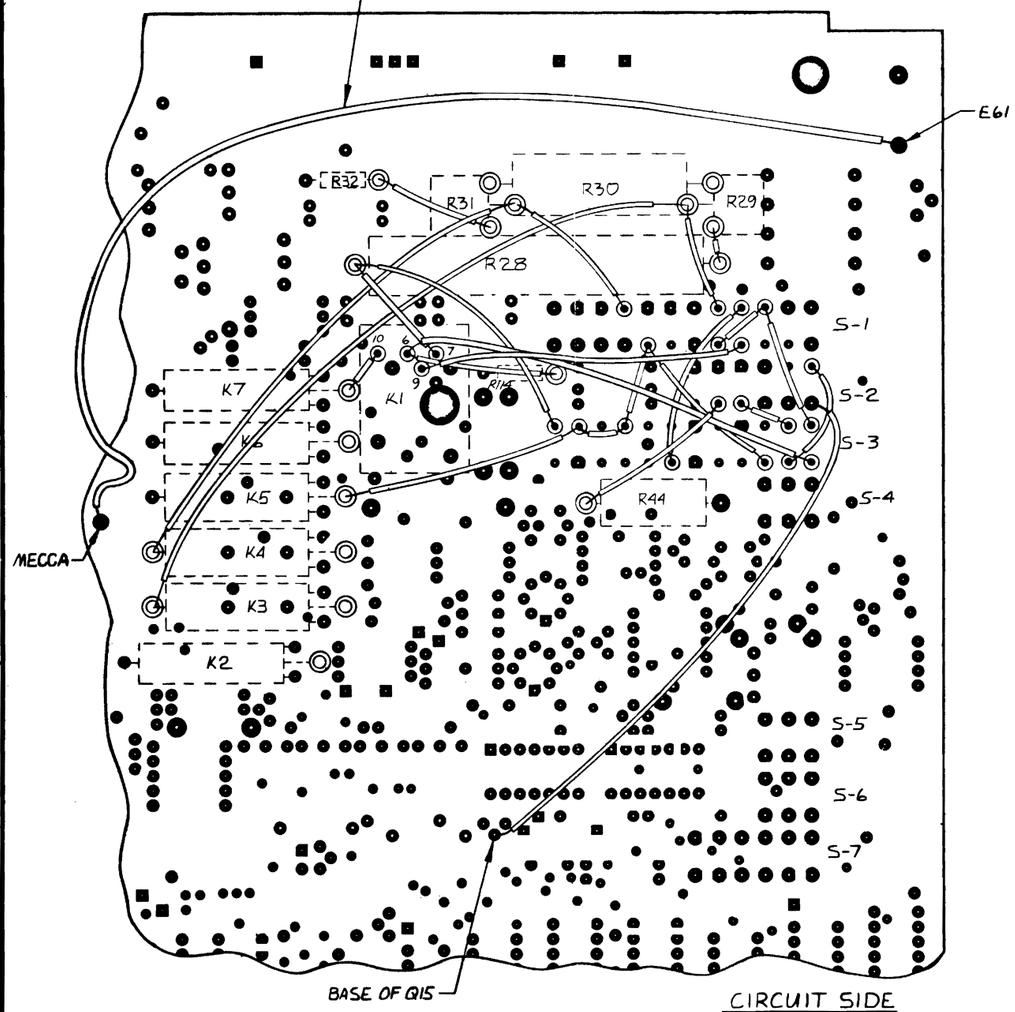
PCB ASSY., MOTHERBOARD 4600-D24

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403874	AS

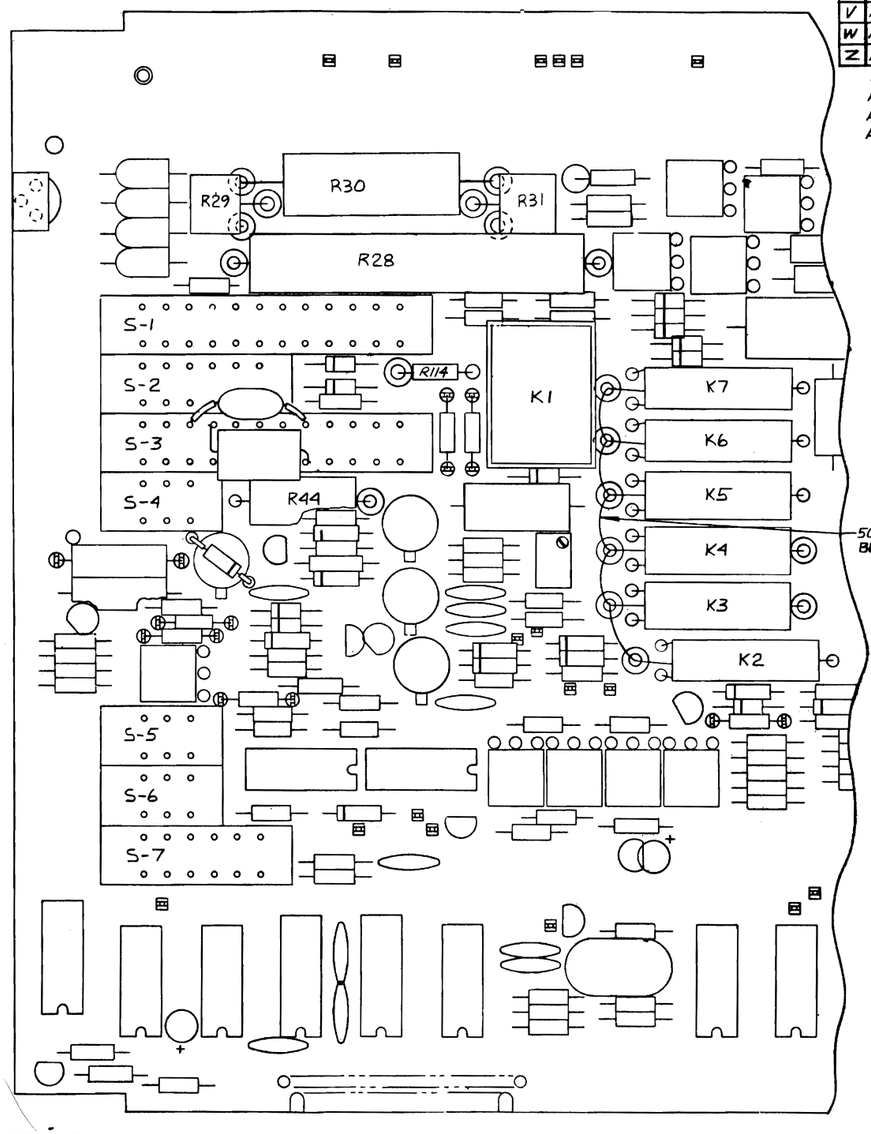
SCALE 2/1 SHEET 1 OF 11

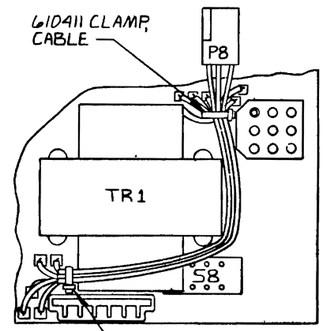
NOTE: POSITION OF WIRE TO BE ADJUSTED FOR MINIMUM NOISE AS MEASURED AT PIN "a" OF AR4. FIX POSITION WITH HOT-MELT GLUE. (OR EQUIV.)

500061 WIRE 18GA. (7.0" LENGTH)

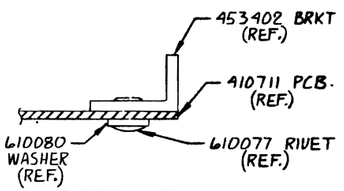


CIRCUIT SIDE

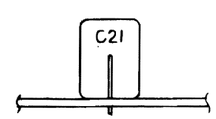




DETAIL "H"



DETAIL "F"



DETAIL "E"

WIRING LIST FOR TR1

COLOR	E#'S	LENGTH
GREEN	GND	2 3/8"
BROWN	24	2 3/4"
BLACK	23	2 3/4"
RED	26	3"
YELLOW	27	3"
ORANGE	25	3"
TOP GREY	46	3"
BOTTOM GREY	47	3"
TOP BLUE	45	3"
BOTTOM BLUE	44	3"
BLACK	43	3"
VIOLET	42	3"

REVISIONS				
PCB REV	LTR	DESCRIPTION	DR	CHK	APPD
		RELEASED PER DRN #			
U	AF	REVISED PER EO # 10549	REV 11-16-76		11-17-76 3 CKT
V	AH	# 10613			
V	AJ	# 10629			
V	AK	# 10646			
W	AL	# 10664			
Z	AM	# 10665	REV 4-26-76		11-17-76 3 CKT
	AN	EO 10862			
	AP	EO 10887			
	AR	EO 10904			
	AS	EO 11003			

403886	4600-D24	1	1	
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY	
APPLICATION		QTY REQD		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL

FINISH

DRAWN	K. Henderson	7/24/75
CHECK		
DESIGN	R. Thompson	7/24/75
MECH ENGR		
PROJ ENGR		12/2/76
MFG ENGR		1-13-77

Xc

DANA DANA LABORATORIES INC.
IRVINE, CALIFORNIA

PCB ASSY., MOTHERBOARD
4600 - D24

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403874	AS

SCALE | SHEET 2 OF 11

PCB REV	REVISIONS				
	LTR	DESCRIPTION	DR	CHK	APPD
	Z	REDRAWN WITH REVISIONS PER EO	R. MAYS		

AC CONV SIG IN

mA S1

I ENABLE

J1 +I IN — E10

FI01 2.5A

CR1 CR3 CR2 CR4

(3E1) AC CONV RLY PWR

J3 +IN — E11

AC CONV RLY ENABLE

ACV S2

ISO GAIN DISABLE (AC)

$\overline{AC}$

J10-8 AC CONV OUT

J4 −IN — E13

KΩ S3

J2 −I IN — E12 — E61

$\overline{K\Omega}$

C20 .068

(2A1) +1V Ω REF

R114 10M

K1

R37 2M 2W

C21 .33 1KV

R28 8.99M

R29 20K 1/2W

R30 889K

R31 2K 1/2W

R32 88.9K

R33 200

R34 8.89K

R35 20 1/2W

R36 990

30

R18 900 .05%

R19 90 .05%

R20 470

R22 9.0225 .25% 1/2W

R21 10K

R23 47

R24 1K

R25 0.9 .25% 3W

C29 FSV 2.2 35V NOM

R110 0.1 1% 3W

R111 FSV

R26 4.7

R27 10 1/2W

K7 K6 K5 K4 K3 K2

RLY COILS SHOWN AT 3D2,34

DCV S4

R39 100

DC

+5V

FUNCTION CONTROLS

ATTENUATOR/ SHUNT

(3D8) ISO X1 SW

(3D8) ISO X10 SW

ISO/BOOTSTRAP AMPL

R45 20K

R46 1M 1% — R47 FSV 1M NOM 1%

C5 .001 — R48 20K

ARI-A LM324

R49 100

R44 100K 2W

Q3 Q4 2N4250

Q5 200201

X1 U15A

R54 FSV 1%

R53 FSV 1%

X10 U15B

R50 4.42K .5%

R51 10 1/2W

R52 487 .5%

M

+15V

R56 100M

R58 10K

CR11

VR1 5.1V

CR12

R57 10K

R60 FSV 200K NOM

R55 2.2M

R59 2M 1/2W

CR13

VR4 10V

R61 3K

C6 47pF

AR2 CA3130

VR2 5.1V

BSC

-BSV

VR3 5.1V

VR5 10V

R62 3K

-15V

K OHMS AMPL

R87 1K

C12 560pF

R85 40.2K .1% 1/10W

R86 40.2K .1% 1/10W

R88 2K

C14 33pF

AR5 LM301A

R84 100K

Q8 200199

C13 560pF

R91 2K

R89 1K

CR19 CR20

R104 FSV

R105 FSV

VR9 5.1V

Q9 SEL MPS-A42

C26 100pF POLY

R113 100K

R92 36.5K 1% 1/10W

C32 .001

R90 100K 1/2W

CR21 IN4004A

I ENABLE (3E8)

ISO GAIN DISABLE(AC) (3D8)

$\overline{AC}$ (3D8)

$\overline{K\Omega}$ (3D8)

INTEGRATOR IN (2D8)

E17 W10 E18

YR6 3.3V

VR15 3.3V

J10 AC CONV SIG IN 1

AC CONV RLY ENABLE 3

DC J13-A

9. TRANSISTORS ARE 200200

8. RESISTOR MAY BE OMITTED ON LATER PRODUCTION MODELS

7. +10V LEVELS ARE 5V ABOVE MECCA REF TO DIG COM

6. +5V LEVELS ARE MECCA REF TO DIG COM

5. SEE NOTE REGARDING TP9 UNDER TABLE 5-10, PAGE 5.10

4. RELAYS ARE .310125

3. DIODES ARE IN916

2. CAPACITORS ARE IN µF

1. RESISTORS ARE IN OHMS, ±5%, 1/4W

NOTES: UNLESS OTHERWISE SPECIFIED

10. GRID C-2 SHT. 1 ADD BACK TO BACK CAPS BETWEEN BSC AND MECCA (R52) 2.2µFD, 35V. MAY NOT BE ON ALL ASSEMBLYS. THEY ARE DESIGNATED C33 AND C34.

403874	4600		
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	−.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	Rich Mays	2-1877
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

DANA LABORATORIES INC. IRVINE, CALIFORNIA

SCHEMATIC-4600 DMM MAIN LOGIC PCB

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	432087	Z

SCALE — SHEET 1 OF 4

PCB REV	REVISIONS				
	LTR	DESCRIPTION	DR	CHK	APPD
		RELEASED PER DRN # SEE SH 1			

INTEGRATOR/NULL DETECTOR

(1D1) — U16A SIG SW — R75 220K — C8 68 6V TANT — Q6 2N5240 — C7 .1 100V POLY — C9 33 pF — AR3 LM301A — R78 1K — R81 10K — CR16 — CR15 — AR4 LM301A — C11 3.3pF — CR17 — CR18 — ND

U16B RESET SW — R76 82K — R77 82K — C10 150pF — R79 100K — CR28

R80 1.5M — R82 2M 1/2W — R83 510K — U16D

REFERENCE VOLTAGE GENERATOR

VR7 5.1V — CR14 — R64 FSV — Q7 2N4250 — R63 9.1K — VR8 FSV 6.2V — R65 FSV — R71 100K — R72 FSV 1% 14.3K — R73 — R74 500 — ARI-B LM 324 — ~REF SW — U15C

R66 49.9K 1% — R100 24.9 1% 1/10W — R67 500 — R69 1K — R101 24.9 1% 1/10W — R68 10K 1% — R70 15K — ARI-C LM 324 — +REF SW — U15D — R108 10K — ARI-D LM 324 — R109 10K — 1V Ω REF

E52 W9 E50 E51

HOLD PROBE INPUT

J12 E53 — R9 10K — U11

TIMING/CONTROL LOGIC

U10 74LS00 — U11 PST CLK 74L74 CLR — +ND F/F — U13 74LS10 — U14 74LS05 — RESET SW — R14 15K — R16 15K — R15 15K — R17 15K — +10V

U12 — -ND F/F — +REF SW — -REF SW — SIG SW

U7 74C04 — SIG INT — (3B8)

RESET — POL F/F — C27 .001 — (3D8)

RESET — (3B8)

SIG INT — (3C8)

U9 74LS00 — C19 .001

INT RESET — U8 — POL DR F/F — TRANSFER — E22 — TRANSFER — (3A8)

Qe1 (O/L) — (3C8)

J13 O/L +POL TRANSFER

+IV Ω REF — (1B8)

J13 4 Qe1 — E Qe2 — 2 Qe2 (O/L)

U15

SEE SH 1

NOTES: UNLESS OTHERWISE SPECIFIED

403874	4600		
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

ARTEKMEDIA A

Digitally signed by ARTEKMEDIA
DN: cn=ARTEKMEDIA, o, ou, email=Manuals@ArtekmMedia.com, c=US
Date: 2012.06.24 03:41:28 -05'00'

DRAWN	Rich Mays	2-22-77
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

DANA LABORATORIES INC. IRVINE, CALIFORNIA

SCHEMATIC-4600 DMM MAIN LOGIC PCB

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	432087	Z

SCALE — SHEET 2 OF 4

6-7

PCB REV	REVISIONS LTR	DESCRIPTION	DR	CHK	APPD
		RELEASED PER DRN # SEE SH 1			

RANGE & RELAY LOGIC

(1D1) I ENABLE — R102 20K, R38 10K, Q14

(1D1) ISO GAIN DISABLE (AC) — Q15

J13-6 .1

(1D1) AC

(1D1) KΩ

(2C1) RESET

E16, E20, E15

R103 20K, R42 100K, R43 2.2K, Q2 2N4248

R12 15K, R13 15K

ISO X10 SW

ISO X1 SW

R40 5.1K, R106 20K, R41 5.1K

R4 10K, R3 10K, R5 10K, Q1, K1 310128, K2

R6 10K, R7 10K, R8 10K

CR 5, CR 6, CR 7, CR 8, CR 9, CR 10, K3, K4, K5, K6, K7

AC CONV RLY PWR (1D8)

ISO X10 SW (1D8)

ISO X1 SW (1D8)

U1 74LS00, U10 74LS00, U14 74LS05, U5 74188, U6 74LS05

J10: AC 10V-100V RLY <2, AC 1000V RLY <4

R1 <H, R2 <J, R4 <9

C25 .001, C24 .001, C23 .001

UP LIMIT

C2 .001

U4 74L192, U3 74LS10, U2 74L74

RANGE CONTROLS

UP — S5 — STEP UP

DWN — S6 — STEP DOWN

AUTO — S7

(2C1) SIG INT

(2B1) Q_{e2} (O/L)

(2C1) SIG INT

(2C1) RESET

J13-D ÷2K

(2B1) TRANSFER

R107 20K, C22 1 35V TANT, Q16

U7 74C04

R1 20K, R2 30K, C1 .001, R112 470, C30 1 35V

CLOCK <8

OSCILLATOR/CLOCK

C4 15pf, R10 1M, U7 74C04, U8 74L74, Y1 200 KHz

NOTES: UNLESS OTHERWISE SPECIFIED

403874	4600		
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	−.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	Rich Mays	2-22-77
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

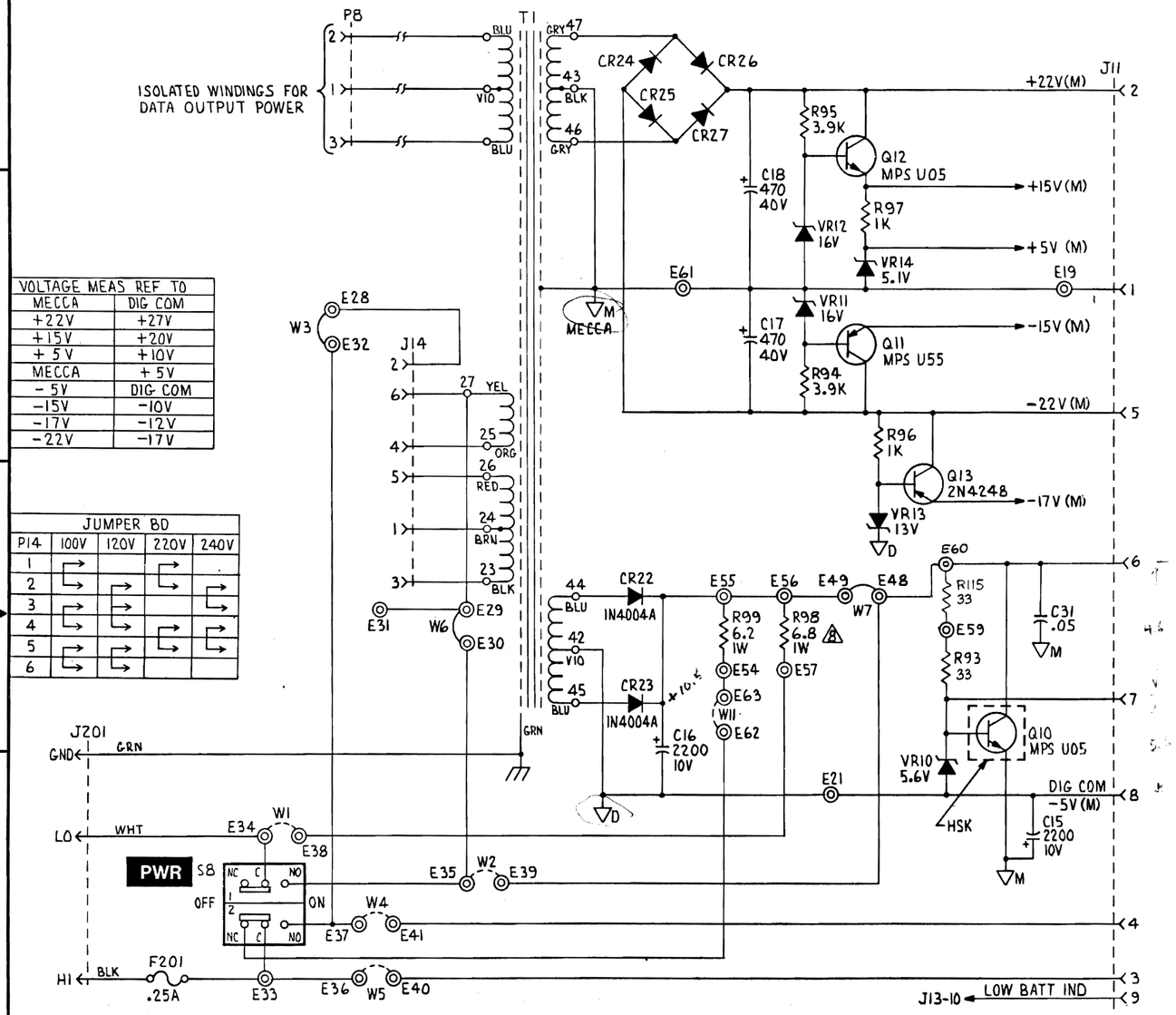
DANA LABORATORIES INC. IRVINE, CALIFORNIA

SCHEMATIC-4600 DMM MAIN LOGIC PCB

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	432087	Z

SCALE — SHEET 3 OF 4

PCB REV	REVISIONS				
	LTR	DESCRIPTION	DR	CHK	APPD
		RELEASED PER DRN # SEE SH 1			



VOLTAGE MEAS REF TO	
MECCA	DIG COM
+22V	+27V
+15V	+20V
+5V	+10V
MECCA	+5V
-5V	DIG COM
-15V	-10V
-17V	-12V
-22V	-17V

JUMPER BD				
P14	100V	120V	220V	240V
1	→		→	
2	→	→	→	→
3	→	→		→
4	→	→	→	→
5	→	→	→	→
6	→	→		

Note! some models are missing R115, R93 has been replaced with 51Ω 1/4W - R93 runs very hot may have to increase to 1/2W max

6MA 1/4 Amp line fuse seems to blow excessively

SEE SH 1

NOTES: UNLESS OTHERWISE SPECIFIED

403874	4600	—	—
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	Rich Mays	1-11-77
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

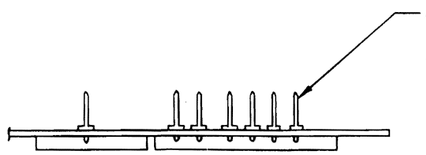
DANA® DANA LABORATORIES INC. IRVINE, CALIFORNIA

SCHEMATIC-4600 DMM MAIN LOGIC PCB

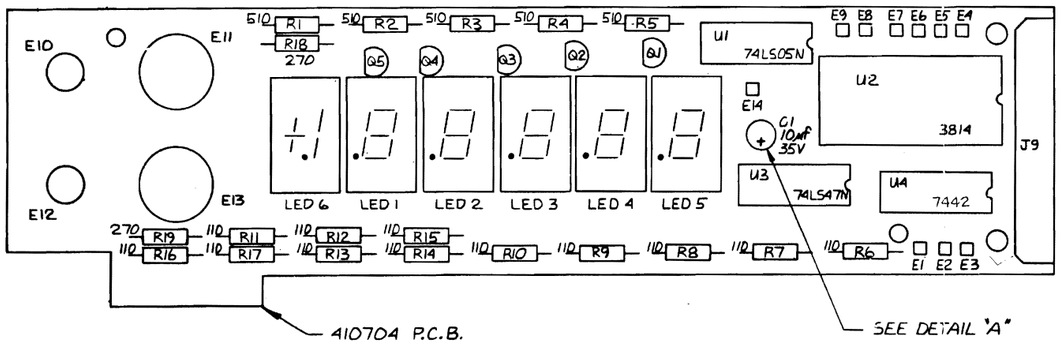
SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	432087	Z

SCALE — SHEET 4 OF 4

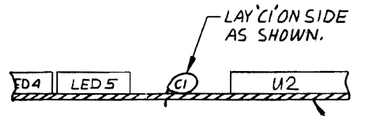
PCB REV	LTR	DESCRIPTION	DR	CHK	APPD
	C	RELEASED PER DRN # 1113	11/3/76		
	D	REVISED PER EO # 9887	11/8/76 RLH		
	E	REVISED PER EO # 9943	2/5/76 RLH		
	F	REVISED PER E.O. # 10220	6-7-76 RLH		
J	H	ADDED NOTE 3 PER E.O 10289	KRM 6-16-76	RLH 7-14-76	7-27-76
	J	EO 10611			
	K	EO 11012			



600786 POST, MACHINE APPLIED 10 PLACES, INSTALL FROM CIRCUIT SIDE AT SQUARE PADS THAT ARE DESIGNATED AS FOLLOWS: E1, E2, E3, E4, E5, E6, E7, E8, E9, E14.



SEE PAGE 5-69 FOR J9 PIN DESIGNATIONS



DETAIL "A"

3. MATCHING ± LED LIGHT INTENSITY CODE TO OTHER LED'S IS NOT MANDATORY.
2. ALL TRANSISTORS MPSA55 TYPE.
1. SCHEMATIC REF. 432084.

NOTES: UNLESS OTHERWISE SPECIFIED

403886	4600-D24	1	1
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030 XX.020 XXX.010	0° 30' FORMED 1° 0'	+.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

PCB REV. "F" OR LATER

DRAWN	R. Henderson	11/14/75
CHECK		
DESIGN	R. Henderson	11/14/75
MECH ENGR		
PROJ ENGR		1/12/76
PROD ENGR		1-5-76

DANA® DANA LABORATORIES INC. IRVINE, CALIFORNIA

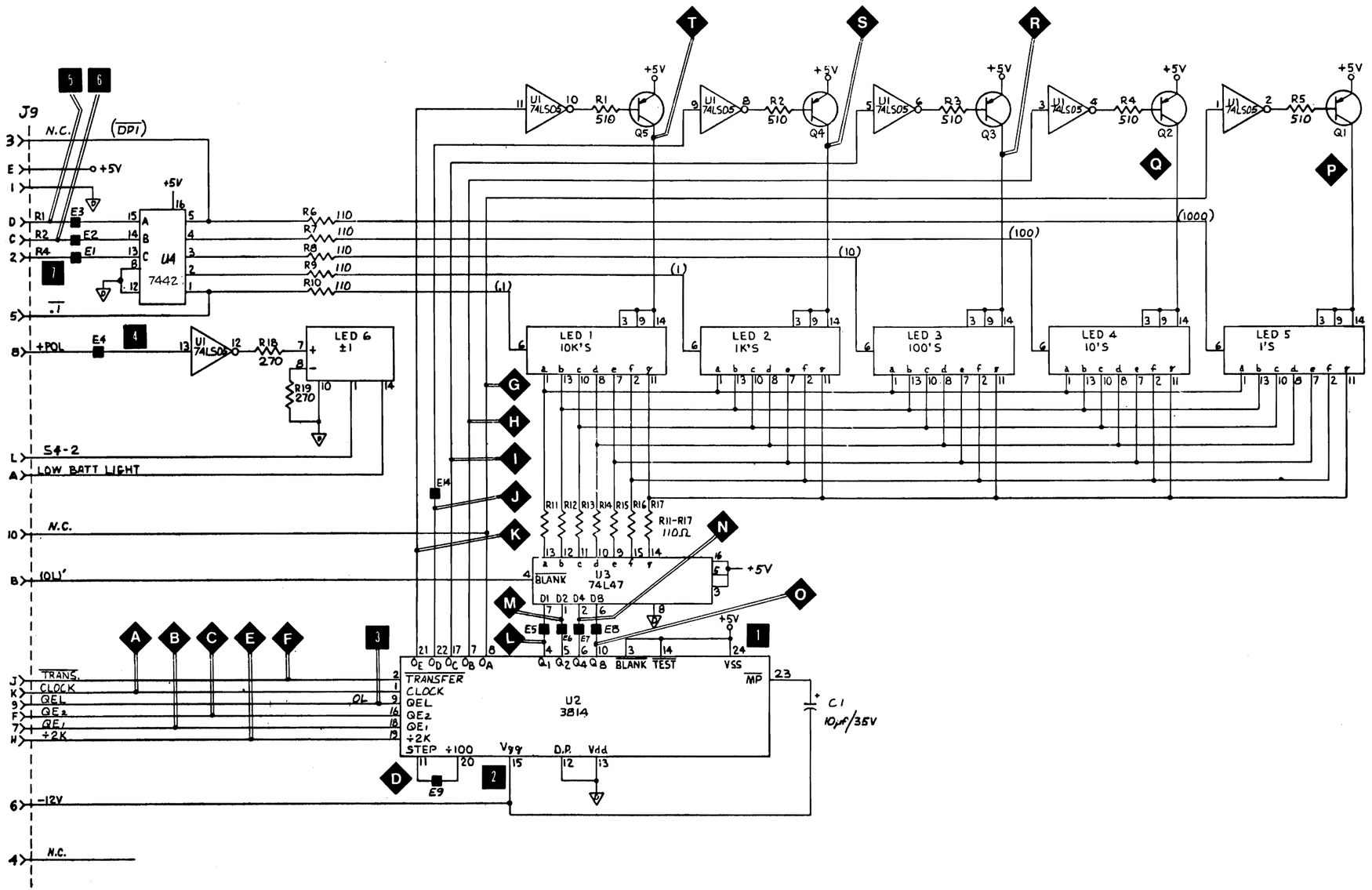
PCB ASSY, DISPLAY BOARD 4600 - D24

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403856	K

SCALE 3/1 SHEET 1 OF 2

REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPD
D	RELEASED PER DRN # 1113 Wayne	11/3/74		
E	REVISED PER E.O.# 9887	1/28/76 R.L.H.	1/28/76	
F	REVISED PER E.O.# 9913	2/4/76 R.L.H.	2/11/76	
H	REVISED PER E.O.# 10220	6-3-76 R.L.H.		6/4/76

J EO 11012



"E" NO'S

E1 - R4
E2 - R2
E3 - R1
E4 - +POL
E5 - D1
E6 - D2
E7 - D4
E8 - D8
E9 - +100
E14 - O_D

4. ⏚ ALL GROUNDS ARE DIGITAL COMMON.
3. —■— THIS DENOTES A PAD FOR CONNECTION OF DATA OUTPUT OPTION.
2. TRANSISTORS ARE MPS-A55.
1. RESISTORS ARE IN OHMS ±5%, 1/4W

NOTES: UNLESS OTHERWISE SPECIFIED

403856	4600-D24	1	1
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	Rich Mayo	9-15-75
CHECK	Kor H	
DESIGN	KOCH	
MECH ENGR		
PROJ ENGR	L.E.	1/12/76
PROD ENGR	[illegible]	10-76

JK

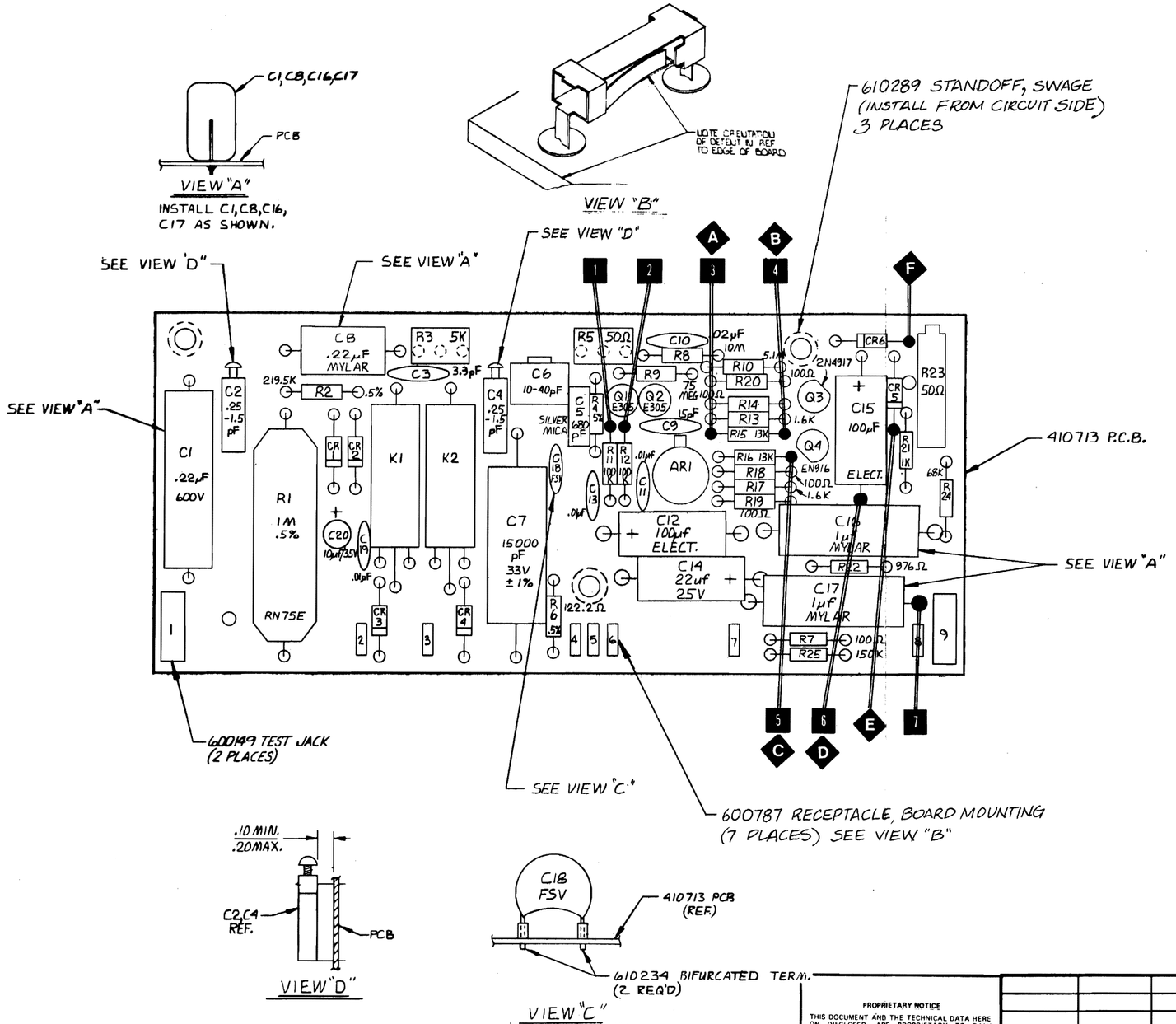
DANA DANA LABORATORIES INC. IRVINE, CALIFORNIA

SCHEMATIC— DISPLAY BOARD, D24

SIZE	CODE IDENT NO.	DWG. NO.	REV
D	21793	432084	J

SCALE | SHEET 1 OF 1

REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPD
A	RELEASED PER DRN # 1113	1/3/75		
B	REVISED PER E.O.# 10074	RLH 5-16-76		5/18/76
C	REVISED PER E.O.# 10101	RLH 5-16-76		5/18/76
D	REVISED PER E.O.# 10135	RLH 5-16-76		5/19/76



VIEW "D"

VIEW "C"

2. ALL DIODES 018 TYPE.
1. SCHEMATIC REF. 432083

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
403886	4600 - D24	1	1
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030 XX.020 XXX.010	0° 30' FORMED 1° 0'	+.004 -.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL

FINISH

DRAWN	R. Henderson	4/24/75
CHECK		
DESIGN	R. Henderson	4/24/75
MECH ENGR		
PROJ ENGR	D. Liggo	4/28/75
MFG ENGR		5-13-76

Xc

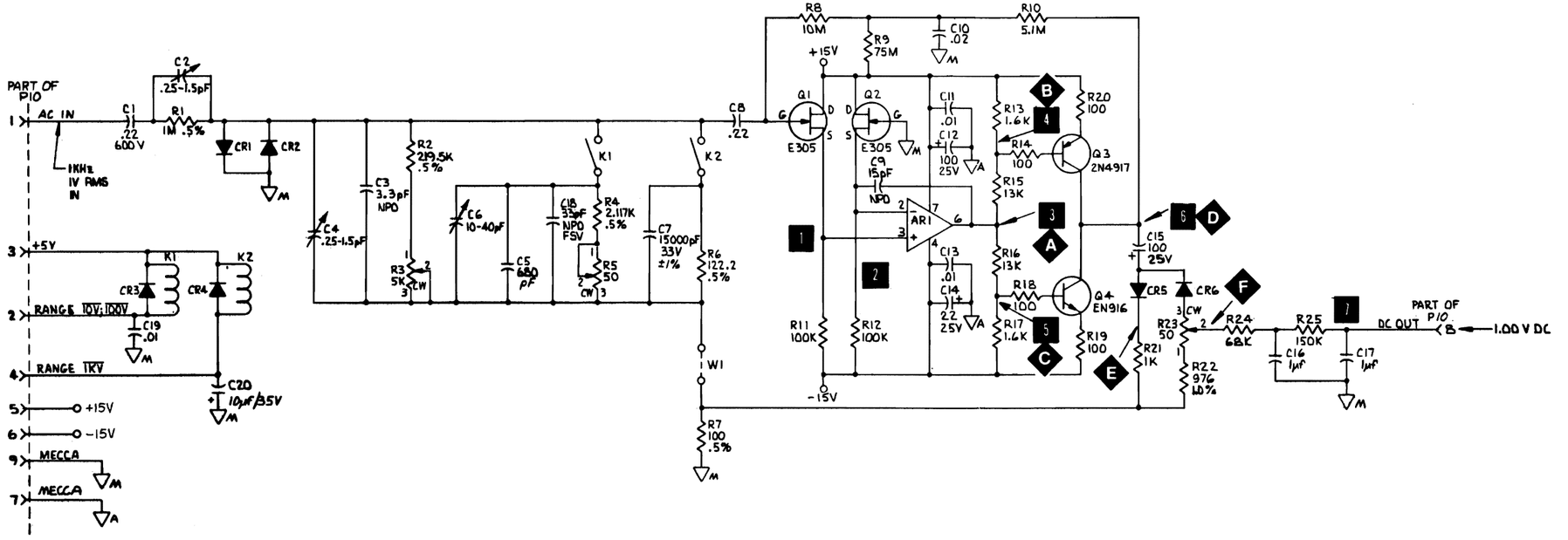
DANA® DANA LABORATORIES INC. IRVINE, CALIFORNIA

PCB ASSY., A.C. CONVERTER 4600A-D24

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403873	D

SCALE NONE SHEET 1 OF 4

REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPD
A	RELEASED PER DRN # 1113	1/13/76		
B	REVISED PER E.O.# 10074	RLH 5-18-76		
C	REVISED PER E.O.# 10101	RLH 5-28-76		
D	REVISED PER E.O.# 10135	RLH 6-8-76		



AC CONVERTER ATTENUATION CHART

RANGE SELECTED	AC CONVERTER			150 GAIN
	RELAY	AC IN	DC OUT	
.2V	–	.2V	-.2V	X10
2V	–	2V	-2V	X1
20V	K1	20V	-.2V	X10
200V	K1	200V	-2V	X1
1KV	K2	1KV	-1V	X1

6. ALL VOLTAGES ARE APPROXIMATE LEVELS AND SHOWN WITH DMM IN 1V-AC, 1V RMS AT 1KHz APPLIED TO INPUT.
5. ▽A - ANALOGUE COMMON GROUND.
4. ▽M - MECCA GROUND.
3. DIODES ARE 018
2. CAPACITORS ARE IN µF EXCEPT AS NOTED.
1. RESISTORS ARE IN OHMS ±5%, 1/4W

NOTES: UNLESS OTHERWISE SPECIFIED

403886	4600	1	1
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

MODIFIED BY PUBLICATIONS DEPT.

DRAWN	Rich Maya	9-2-75
CHECK	J. KOCH	9-22-75
DESIGN	J. KOCH	9-25-75
MECH ENGR		
PROJ ENGR		10/6/75
PROD ENGR		10/15/76

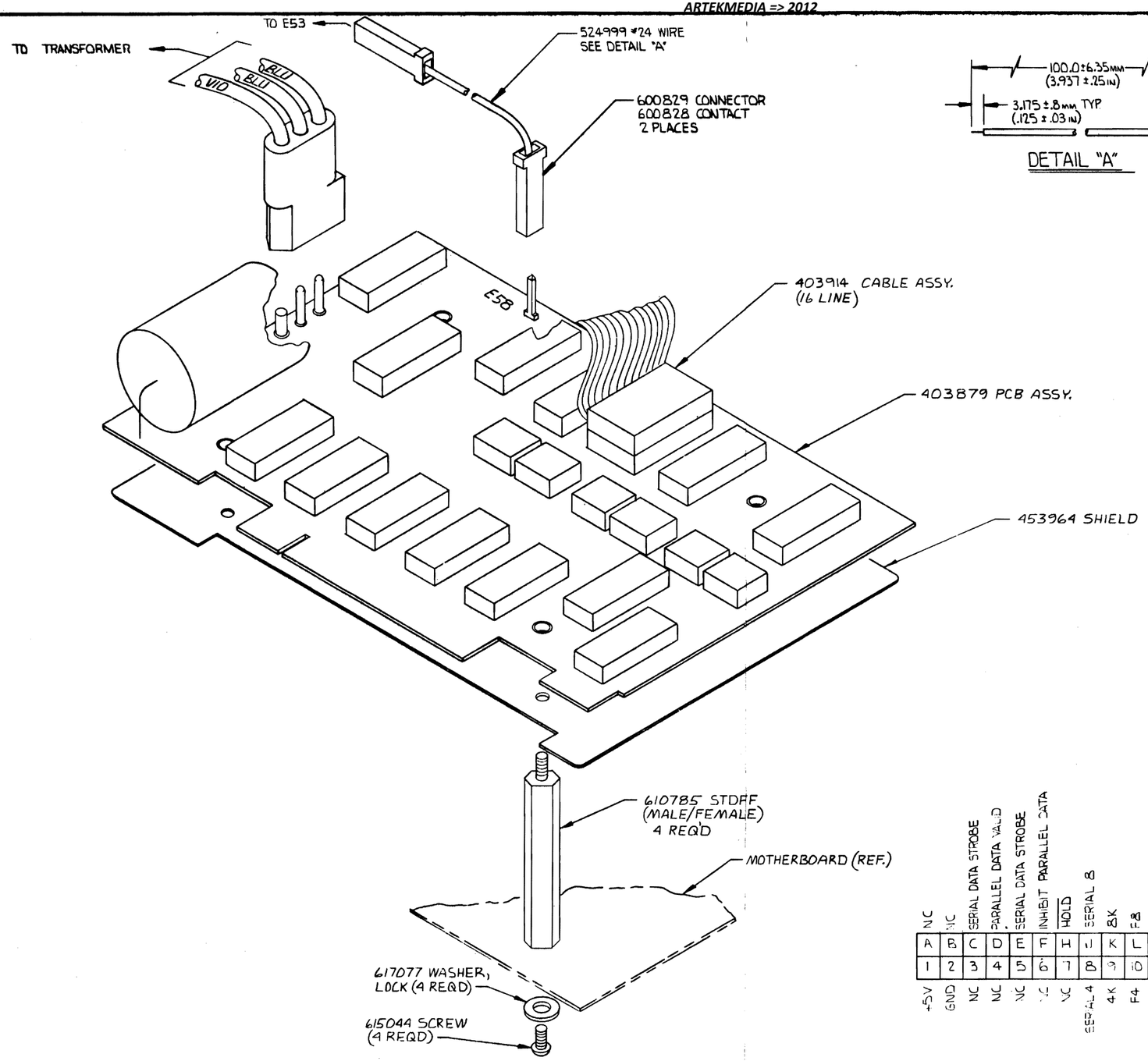
DANA DANA LABORATORIES INC. IRVINE, CALIFORNIA

SCHEMATIC — AC CONVERTER

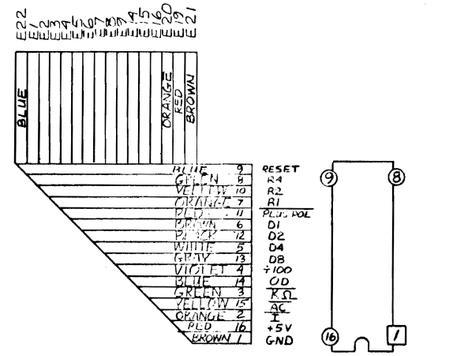
SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	432083	D

SCALE | SHEET 1 OF 1

REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPD
A	RELEASED PER DRN # 1113	1/3/76		



DETAIL "A"



403914 CABLE ASSY.

	A	B	C	D	E	F	H	J	K	L	M	N	P	R	S	T	U	V	W	X	Y	Z	
	NC	NC	SERIAL DATA STROBE	PARALLEL DATA VALID	SERIAL DATA STROBE	INHIBIT PARALLEL DATA	HOLD	SERIAL 8	8K	F8	0	800	80	8	SERIAL 1	2K	20K (2L)	F2	R2	200	20	2	COMPONENT SIDE
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	CIRCUIT SIDE
	+5V	GND	NC	NC	NC	NC	NC	SERIAL 4	4K	F4	R4	400	40	4	SERIAL 2	1K	10K	F1	R1	100	10	1	

				UNLESS OTHERWISE SPECIFIED DIMENSIONS IN MILLIMETERS AND INCLUDE THICKNESS OF PLATING	
				TOLERANCES	
				DECIMALS .X ±.5 .XX ±.25 .XXX ±.010	ANGLES 0° 30' FORMED 1° 0'	HOLE DIAMETERS +.10 −.05
				DIMENSIONS AND TOLERANCES PER USAS Y14.15	
	4600			MATERIAL	
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY	FINISH	
APPLICATION		QTY REQD			

DRAWN	J. Henderson	7/1/75
CHECK		
DESIGN	R. Henderson	7/1/75
MECH ENGR		
PROJ ENGR		7/21/76
MFG ENGR		10/76
Xc		

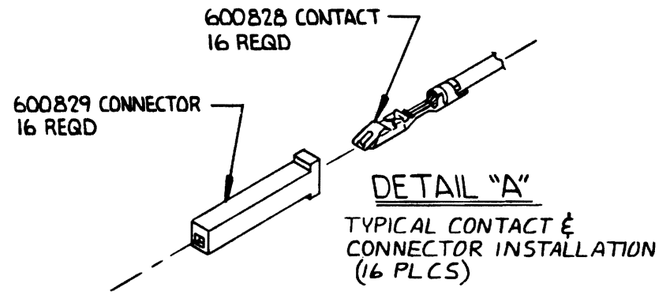
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

DATA OUTPUT OPTION 4600

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403894	A

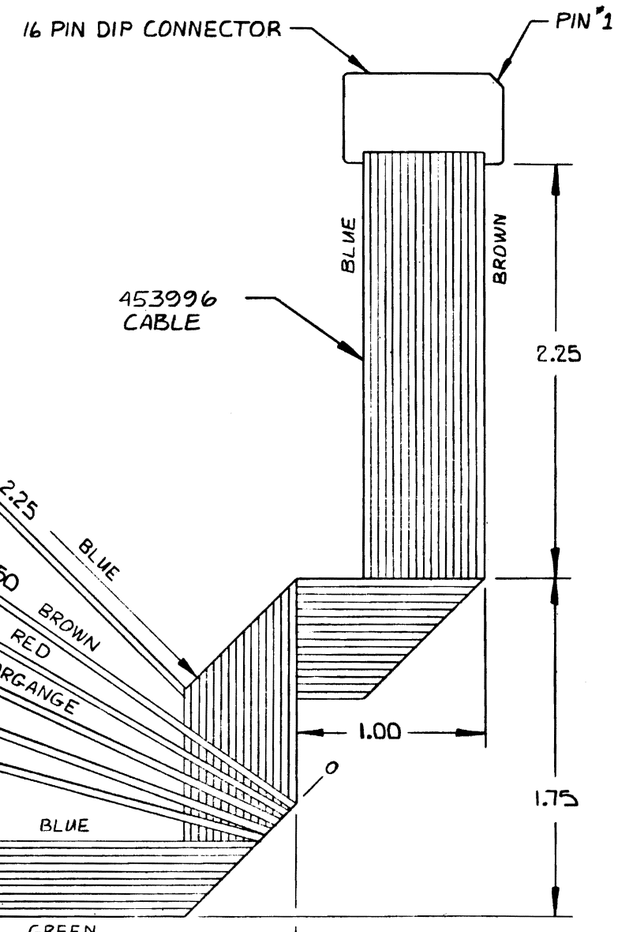
SCALE NONE | SHEET 1 OF 2

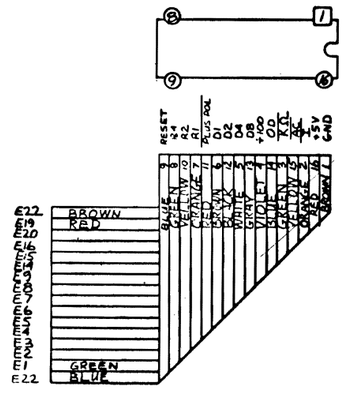
REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPD
A	RELEASED PER DRN # 1113	11/3/76		



DETAIL "A"

TYPICAL CONTACT & CONNECTOR INSTALLATION (16 PLCS)





NOTES: UNLESS OTHERWISE SPECIFIED

403894	4600	1	1
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
XX.06 XXX.010	0° 30' FORMED 1° 0'	+.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL | FINISH

DRAWN	R. Henderson	10/9/75
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		10/9/75
MFG ENGR		1-13-76
Xc		

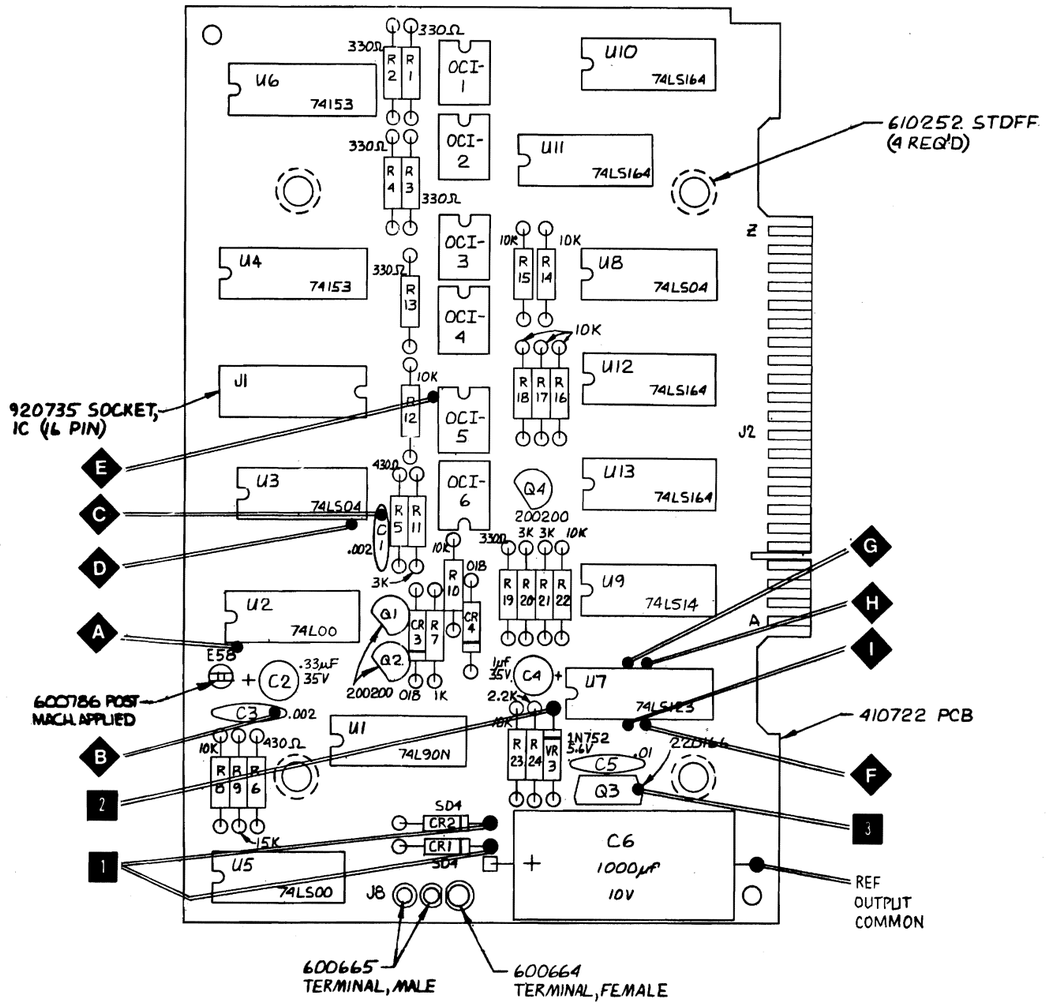
DANA® DANA LABORATORIES INC.
IRVINE, CALIFORNIA

CABLE ASSY, DATA OUTPUT OPTION

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	403914	A

SCALE NONE | SHEET 1 OF 2

PCB REV	LTR	DESCRIPTION	DR	CHK	APPD
	A	RELEASED PER DRN # 1113	11/3/76		
E	B	REVISED PER E.O.# 10076	3/2/77	3/2/77	
F	C	REVISED PER E.O.# 10195	4/13/78		
D	EO 10956				



1. SCHEMATIC REF. 432085

403894	4600						
NEXT DWG	USED ON	NEXT DWG	FINAL ASST				
APPLICATION		QTY REQD					

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL

FINISH

DRAWN	R. Henderson	6/29/75
CHECK		
DESIGN	R. Henderson	6/29/75
MECH ENGR		
PROJ ENGR	D. Wing	10/3/75
MFG ENGR	[illegible]	1-13-76

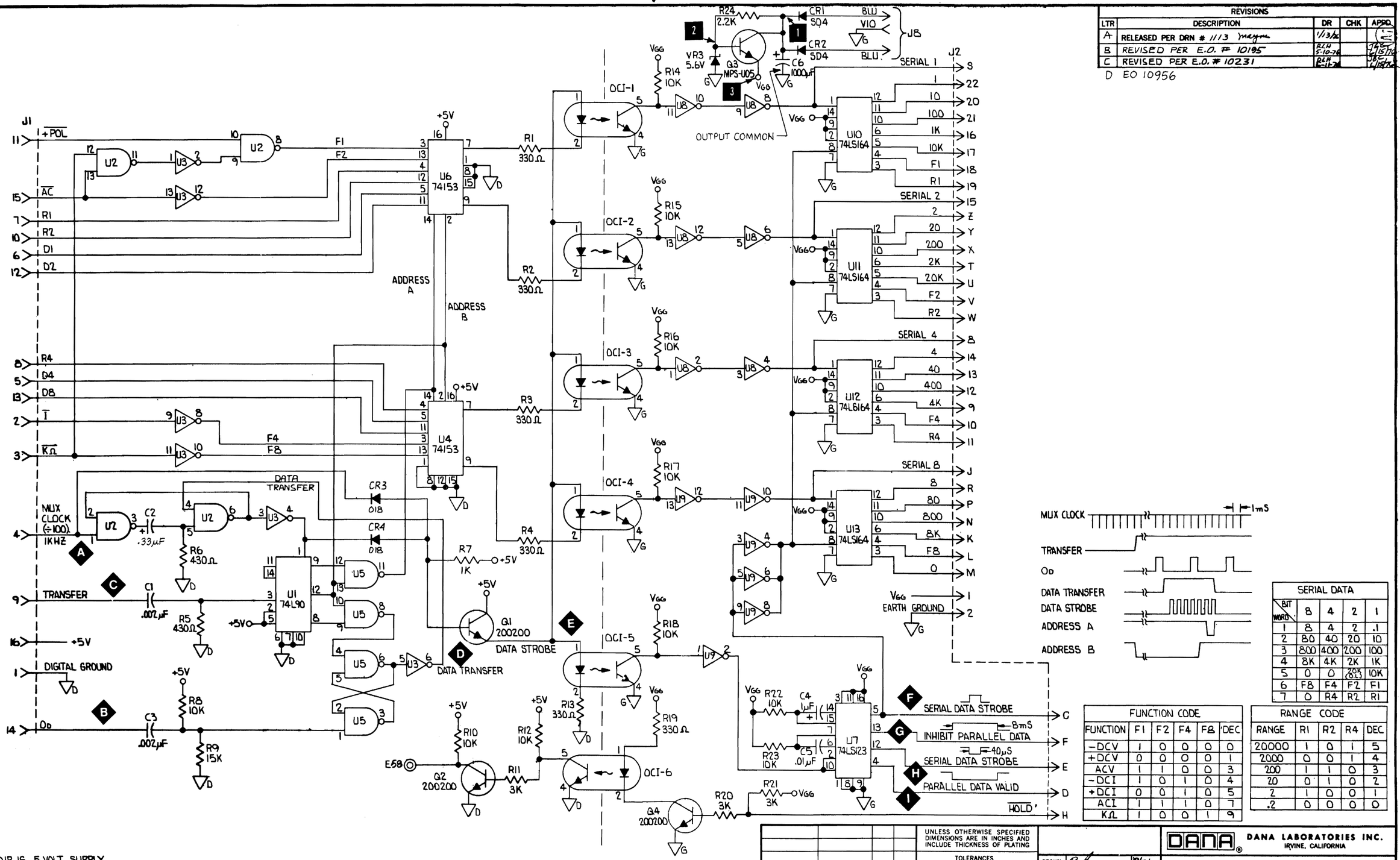
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

PCB ASSY DATA OUTPUT OPT.
4600A - D24

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403879	D

SCALE NONE | SHEET 1 OF 3

REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPD
A	RELEASED PER DRN # 1113	11/3/76		
B	REVISED PER E.O. # 10195	RLH 5-10-76		
C	REVISED PER E.O. # 10231	RLH 6-16-76		
D	EO 10956			



SERIAL DATA				
BIT / WORD	8	4	2	1
1	8	4	2	.1
2	80	40	20	10
3	800	400	200	100
4	8K	4K	2K	1K
5	0	0	20K (8.L.S.)	10K
6	F8	F4	F2	F1
7	0	R4	R2	R1

FUNCTION CODE					
FUNCTION	F1	F2	F4	F8	DEC
-DCV	1	0	0	0	0
+DCV	0	0	0	0	1
ACV	1	1	0	0	3
-DCI	1	0	1	0	4
+DCI	0	0	1	0	5
ACI	1	1	1	0	7
KΩ	1	0	0	1	9

RANGE CODE				
RANGE	R1	R2	R4	DEC
20000	1	0	1	5
2000	0	0	1	4
200	1	1	0	3
20	0	1	0	2
2	1	0	0	1
.2	0	0	0	0

6. PIN 14 ON DIP IS 5 VOLT SUPPLY.
5. PIN 7 ON DIP IS COMMON.
4. VGG IS A GROUNDED 5 VOLT SUPPLY.
3. U3, U8 & U9 ARE 74LS04.
2. U2 & U5 ARE 74LS00.
1. ALL RESISTORS ARE IN OHMS ±5%, ¼ W.

NOTES: UNLESS OTHERWISE SPECIFIED

403879	4600		
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL | FINISH

DRAWN	B Benson	10/2/75
CHECK	Tim O	—
DESIGN		
MECH ENGR		
PROJ ENGR	DP	10/8/75
PROD ENGR		11/5/75

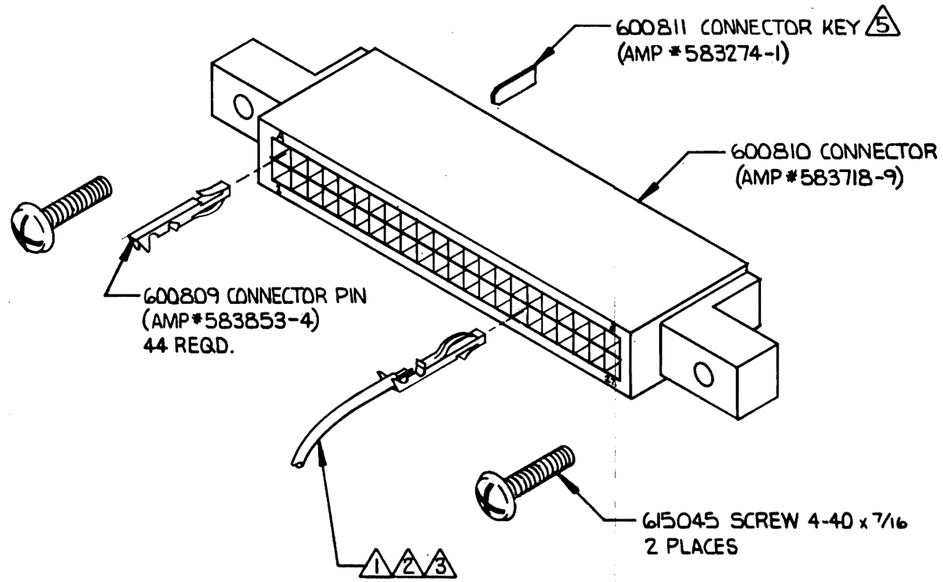
DANA® DANA LABORATORIES INC. IRVINE, CALIFORNIA

SCHEMATIC, DATA OUTPUT OPTION 4600

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	432085	D

SCALE NONE | SHEET 1 OF 2

REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPD
A	RELEASED PER DRN # 1113 mwynn	1/13/76		



6. PACKAGE ALL ITEMS IN A 5"x 7" POLY BAG.
(5) INSERT KEY 600811 BETWEEN CONNECTOR POSITIONS D & E.
4 FOR EXTRACTING CONNECTOR PINS USE TOOL NO. 453997 SUPPLIED.
(3) WIRE MAY BE ATTACHED TO CONNECTOR PIN USING AMP HAND TOOL NO. 90272-1 NOT SUPPLIED WITH KIT.
(2) SOLDER WIRE TO CONNECTOR PIN (600809), TABS MUST BE EITHER STRAIGHT UP OR CRIMPED OVER BEFORE INSERTING INTO CONNECTOR (WIRE NOT SUPPLIED).
(1) WIRE RANGE OF CONNECTOR PIN (600809) IS 24-20 AWG.
NOTES: UNLESS OTHERWISE SPECIFIED

403894	4600		
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	J. Benson	11/4/75
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		1/12/76
PROD ENGR		1/13/76

DANA® DANA LABORATORIES INC.
IRVINE, CALIFORNIA

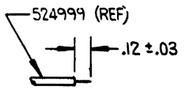
SHIPPING KIT-DATA OUTPUT
4600

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	403920	A

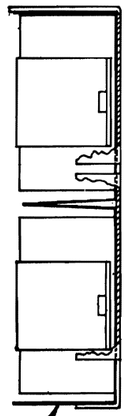
SCALE NONE | SHEET 1 OF 2

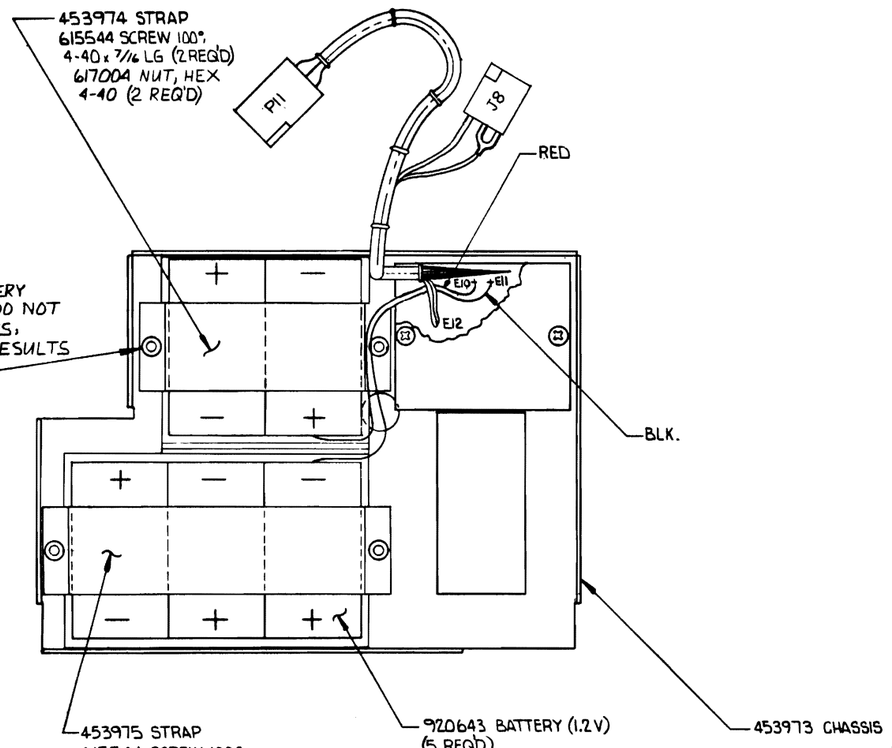
DIETZGEN 980337 DIETZGEN-POST CLEARPRINT 1020

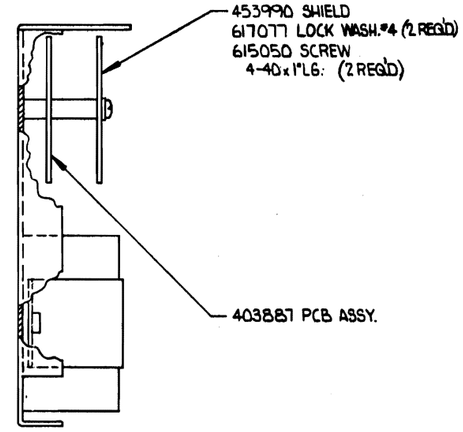
REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPD
A	RELEASED PER DRN # 1113	11/3/76		
B	REVISED PER E.O. # 9891	1/26/76 R.L.N.	1/27/76	
C	REVISED PER E.O. # 10511	R.L.N. 2-4-76	2-06-76 9-10-76	
D	E.O. 10948			

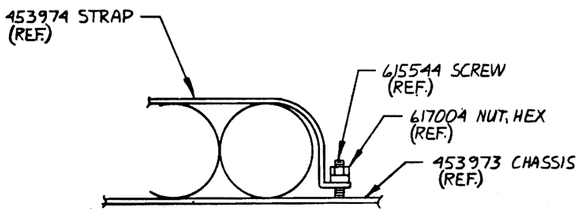


DETAIL "A"

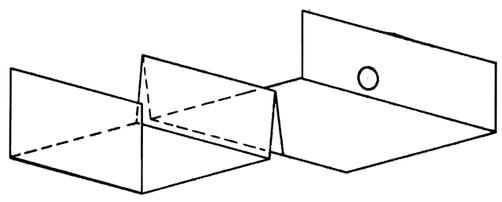






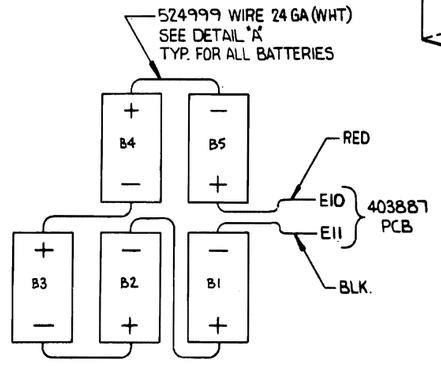


DETAIL "B"



VIEW "Z"

FOLD INSULATOR AS SHOWN (453991)



WIRING DIAGRAM

1. CHASSIS WARPAGE OF .030 IS ACCEPTABLE.

NOTES: UNLESS OTHERWISE SPECIFIED

403889	4600		
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030 XX.020 XXX.010	0° 30' FORMED 1° 0'	+.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

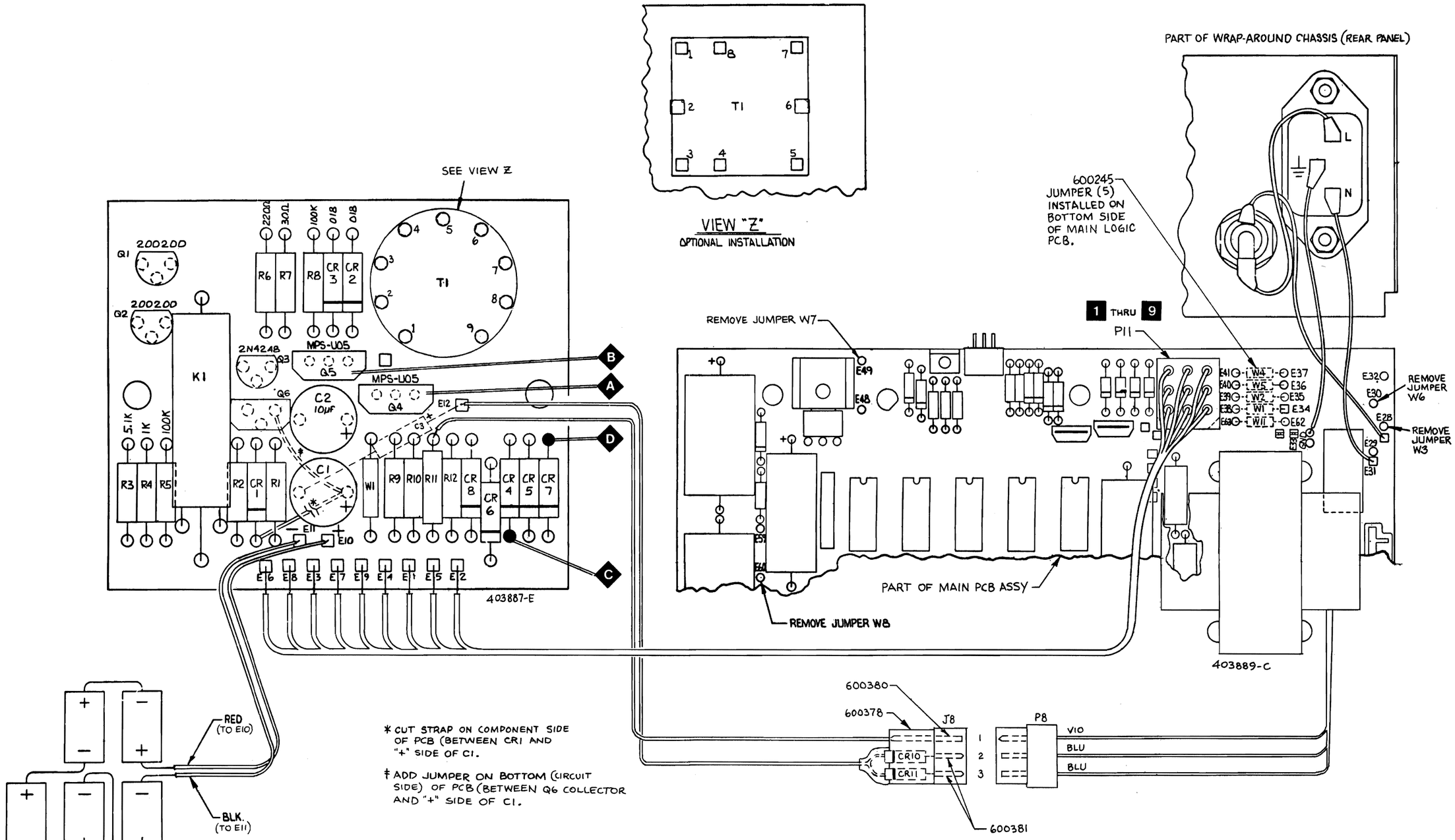
DRAWN	J. Benson	9/24/75
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR	O'Boyle	9/9/75
PROD ENGR		11-5-76

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

MODULE ASSEMBLY-
BATTERY PACK (4600)

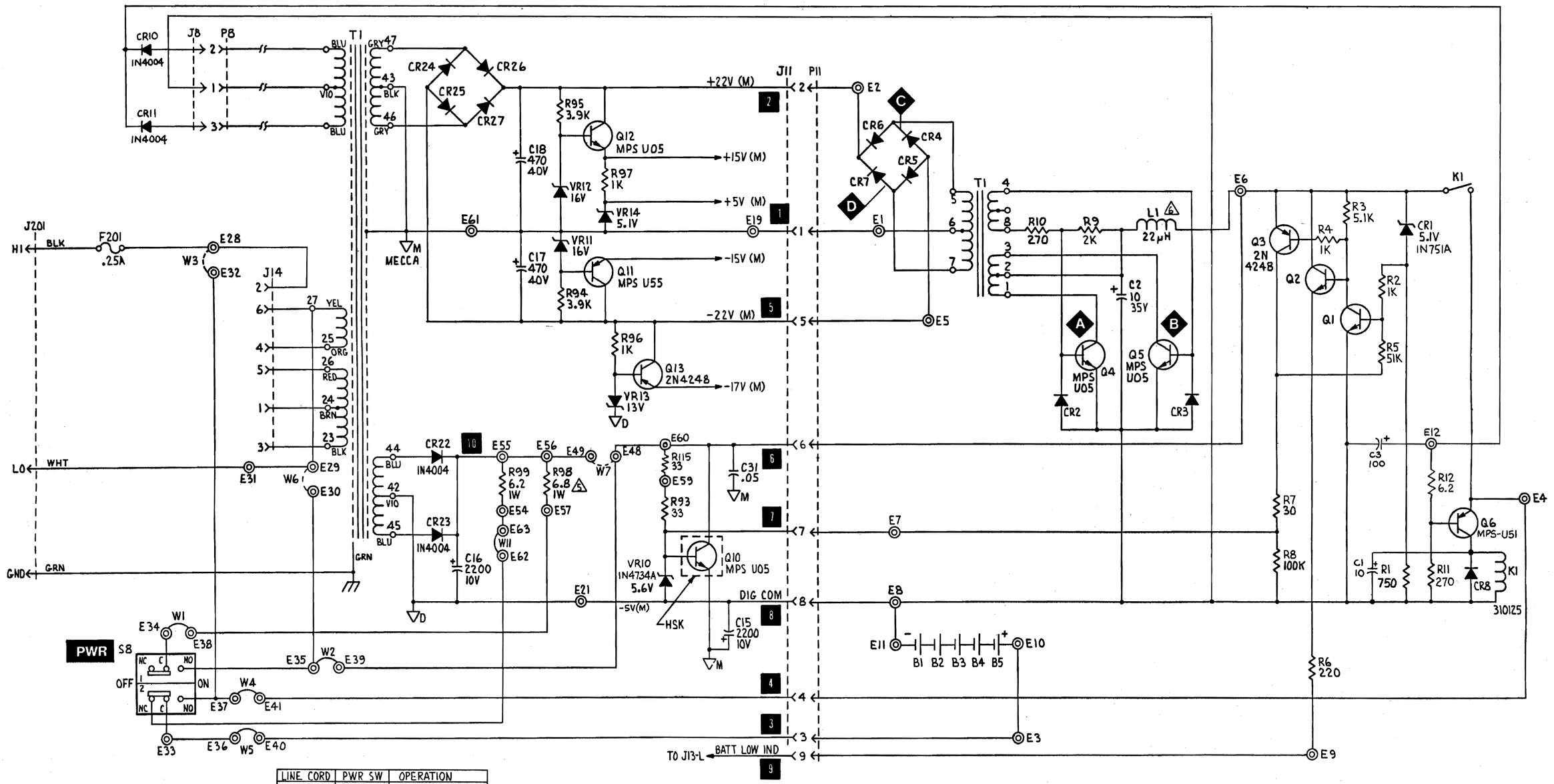
SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403888	D

SCALE 1/1 SHEET 1 OF 2



Schematic, Battery Pack/Main Logic PCB Interconnection

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
		RELEASED PER DRN #			



LINE CORD	PWR SW	OPERATION
OUT	ON	BATTERY OPERATION
OUT	OFF	INOPERATIVE
IN	ON	LINE OPERATION
IN	OFF	BATTERY CHARGE

VOLTAGE MEAS REF TO	
MECCA	DIG COM
+22V	+27V
+15V	+20V
+5V	+10V
MECCA	+5V
-5V	DIG COM
-15V	-10V
-17V	-12V
-22V	-17V

JUMPER BOARD				
P14	100V	120V	220V	240V
1	→		→	
2	→	→	→	→
3	→	→		→
4	→	→	→	→
5	→	→	→	→
6	→	→		

△6 L1 MAY BE REPLACED WITH A JUMPER ON LATER PRODUCTION MODELS
△5 RESISTOR MAY BE OMITTED ON LATER PRODUCTION MODELS
4. TRANSISTORS ARE 2N2200
3. DIODES ARE IN916
2. CAPACITORS ARE IN µF
1. RESISTORS ARE IN OHMS, ±5%, 1/4W
NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
	4600		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030	0° 30'	+.004
XX.020	FORMED	-.001
XXX.010	1° 0'	

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL / FINISH

DRAWN	Rich Mays	2-18-77
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

DANA DANA LABORATORIES INC. IRVINE, CALIFORNIA

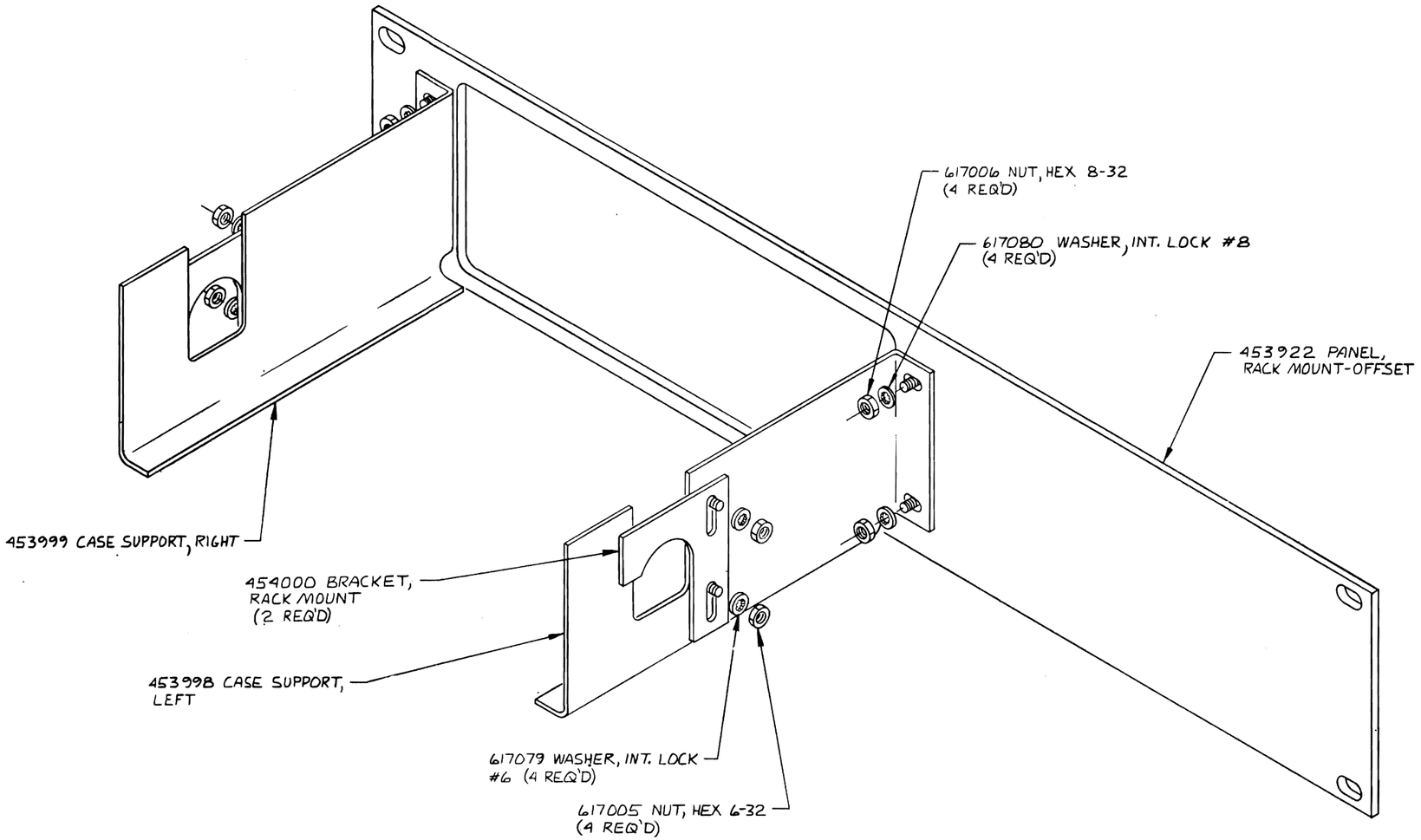
SCHEMATIC 4600 DMM MAIN LOGIC PCB-PWR SUPP & BATT PACK INTERCONNECT

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793		1

SCALE | SHEET 1 OF 1

6-21

REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPD
A	RELEASED PER DRN # 1114 1/27/76	Mayer		



RIGHT HAND MOUNTING SHOWN

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
	4600		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030 XX.020 XXX.010	0° 30' FORMED 1° 0'	+.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL	FINISH

DRAWN	R. Henderson	1/15/76
CHECK		
DESIGN		
MECH ENGR	J. Guercio	1-16-76
PROJ ENGR		1/16/76
PROD ENGR		1-23-76

DANA® DANA LABORATORIES INC.
IRVINE, CALIFORNIA

RACK MOUNTING OPTION
4600

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403892	A

SCALE 1/1 SHEET 1 OF 2

SECTION 7 PARTS LIST

7.1 This section contains lists of replaceable parts arranged in the order of the following subassemblies:

7.2 Manufacturers are identified by FSC numbers listed in table 7.2, "List of Suppliers". The code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1, H4-2, and their supplements.

7.3 Certain parts having 21793 (Dana) listed in the "FSC" column are specially-selected semiconductors. For some of these, standard commercial parts will serve as satisfactory replacements. These Dana parts are identified in table 7.1 along with the commercial equivalent.

Table 7.1

Semiconductor Type:	Equivalent:
018 Diode	Fairchild 1N916B

Table 7.2 - List of Suppliers

FSC	NAME	FSC	NAME
01121	ALLEN BRADLEY CO. MILWAUKEE, WISCONSIN	05397	UNION CARBIDE CORP. (Materials Systems Division) CLEVELAND, OHIO
01295	TEXAS INSTRUMENTS, INC. DALLAS, TEXAS	07263	FAIRCHILD (Semiconductor Division) MOUNTAIN VIEW, CALIFORNIA
04404	HEWLETT-PACKARD CO. (Automatic Measurement Division) PALO ALTO, CALIFORNIA	08257	NPC ELECTRONICS CANOGA PARK, CALIFORNIA
04713	MOTOROLA, INC. (Semiconductor Products Division) PHOENIX, ARIZONA	11237	CTS KEENE, INC. PASO ROBLES, CALIFORNIA

Table 7.2 - List of Suppliers continued

FSC	NAME
12406	ELPAC, INC. IRVINE, CALIFORNIA
21793	DANA LABORATORIES, INC. IRVINE, CALIFORNIA
22045	JORDAN ELECTRIC CO. VAN NUYS, CALIFORNIA
27014	NATIONAL SEMI-CONDUCTOR CORP. SANTA CLARA, CALIFORNIA
27264	MOLEX PRODUCTS CO. DOWNERS GROVE, ILLINOIS
27556	IMB ELECTRONIC PRODUCTS, INC. SANTA FE SPRINGS, CALIFORNIA
31741	GOULD-NATIONAL BATTERIES ST. PAUL, MINNESOTA
32293	INTERSIL, INC. CUPERTINO, CALIFORNIA
32997	BOURNS (Trimpot Products Division) RIVERSIDE, CALIFORNIA
34553	AMPEREX/MEPCO-ELECTRA (Component Division) HAUPPAUGE, NEW YORK
50434	HEWLETT-PACKARD CO. (HPA Division) PALO ALTO, CALIFORNIA
52763	STETTNER-TRUSH CAZENOVIA, NEW YORK
56289	SPRAGUE ELECTRIC CO. (Pacific Division) LOS ANGELES, CALIFORNIA
71471	AEROVOX CORP. (Cinema Plant) MONCKS CORNER, SOUTH CAROLINA
71590	CENTRALAB ELECTRONICS MILWAUKEE, WISCONSIN
73138	BECKMAN INSTRUMENTS, INC. FULLERTON, CALIFORNIA
73445	AMPEREX ELECTRONIC CORP. HICKSVILLE, LONG ISLAND, NEW YORK
74970	E. F. JOHNSON CO. WASECA, MINNESOTA
75915	LITTELFUSE, INC. DES PLAINES, ILLINOIS
80131	ELECTRONICS INDUSTRIES ASSOC. WASHINGTON, D.C.
80294	BOURNS, INC. RIVERSIDE, CALIFORNIA
81349	MILITARY SPECIFICATION
82389	SWITCHCRAFT, INC. CHICAGO, ILLINOIS
91419	RADIO MATERIALS CO. CHICAGO, ILLINOIS
91637	DALE ELECTRONICS, INC. COLUMBUS, NEBRASKA
99800	AMERICAN PRECISION INDUSTRIES, INC. (Delevan Division) EAST AURORA, NEW YORK

403886 – Assy., MODULE

REF DES	DANA P/N	DESCRIPTION			FSC	MANU P/N
F101	920770	FUSE, FAST BLOW	2.5 AMP	250 V	75915	21202.5
F201	920769	FUSE, FAST BLOW	.25 AMP	250 V	75915	212.250
J201	600619	CONNECTOR, RECEPTACLE			82389	EAC-301

403874 – Assy., PCB, MAIN LOGIC

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
AR1	230298	INTEGRATED CIRCUIT					27014	LM324
AR2	230242	INTEGRATED CIRCUIT					21793	230242
AR3	230054	INTEGRATED CIRCUIT					27014	LM301A
AR4	230054	INTEGRATED CIRCUIT					27014	LM301A
AR5	230054	INTEGRATED CIRCUIT					27014	LM301A
C1	100071	CAP	CERAM	.001 MFD	1000 V	20%	56289	C023B102E102M
C2	100071	CAP	CERAM	.001 MFD	1000 V	20%	56289	C023B102E102M
C4	100060	CAP	CERAM	15 PFD	1000 V	5%	56289	C030B102E150J
C5	100071	CAP	CERAM	.001 MFD	1000 V	20%	56289	C023B102E102M
C6	101182	CAP	CERAM	47 PFD	500 V	10%	71471	TCD-DI-2(N750)
C7	120236	CAP	POLY	0.1 MFD	100 V	5%	27556	PA2B104J
C8	110154	CAP	TANTA	68 MFD	6 V	20%	05397	T368B686M006AS
C9	100012	CAP	CERAM	33 PFD	500 V	10%	71471	TCD-DI-1(N750)
C10	101642	CAP	CERAM	150 PFD	500 V	10%	71471	SCD1X5F
C11	100072	CAP	CERAM	3.3±.5 PFD	1000 V		56289	C030B102E3R3D
C12	100038	CAP	CERAM	560 PFD	500 V	10%	71590	DD561
C13	100038	CAP	CERAM	560 PFD	500 V	10%	71590	DD561
C14	100012	CAP	CERAM	33 PFD	500 V	10%	71471	TCD-DI-1(N750)
C15	110121	CAP	ELECT	2200 MFD	10 V		34553	ET222X010A03
C16	110121	CAP	ELECT	2200 MFD	10 V		34553	ET222X010A03
C17	110112	CAP	ELECT	470 MFD	40 V		34553	ET471X040A02
C18	110112	CAP	ELECT	470 MFD	40 V		34553	ET471X040A02
C19	100071	CAP	CERAM	.001 MFD	1000 V	20%	56289	C023B102E102M
C20	120284	CAP	MYLAR	.068 MFD	100 V	20%	73445	C281AH/A68K
C21	120342	CAP	MYLAR	.33 MFD	1 KV	10%	27556	ZA2334K
C22	110143	CAP	TANTA	1 MFD	35 V	20%	05397	T368A105M035AS
C23	100071	CAP	CERAM	.001 MFD	1000 V	20%	56289	C023B102E102M
C24	100071	CAP	CERAM	.001 MFD	1000 V	20%	56289	C023B102E102M
C25	100071	CAP	CERAM	.001 MFD	1000 V	20%	56289	C023B102E102M
C26	120034	CAP	POLY	100 PFD	630 V	5%	08257	KSO Series
C27	100071	CAP	CERAM	.001 MFD	1000 V	20%	56289	C023B102E102M
C29	110125	CAP	TANTA	2.2 MFD	35 V	20%	05397	T368B225M035AS
C30	110143	CAP	TANTA	1 MFD	35 V	20%	05397	T368A105M035AS
C31	100080	CAP	CERAM	.05 MFD	100 V	20%	56289	C023A101L503M
C32	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C33 *	110125	CAP	TANTA	2.2 MFD	35 V	20%	05397	T368B225M035AS
C34 *	110125	CAP	TANTA	2.2 MFD	35 V	20%	05397	T368B225M035AS
CR1	210085	DIODE	RECT	SELECTED	3 AMP		21793	210085
CR2	210068	DIODE		SELECTED	3 AMP		21793	210068
CR3	210085	DIODE	RECT	SELECTED	3 AMP		21793	210085
CR4	210068	DIODE		SELECTED	3 AMP		21793	210068
CR5	211083	DIODE	SILICO		018		21793	211083
CR6	211083	DIODE	SILICO		018		21793	211083
CR7	211083	DIODE	SILICO		018		21793	211083

*May not be on all assemblies.

403874 – Assy., PCB, MAIN LOGIC *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
CR8	211083	DIODE SILICO 018	21793	211083
CR9	211083	DIODE SILICO 018	21793	211083
CR10	211083	DIODE SILICO 018	21793	211083
CR11	211083	DIODE SILICO 018	21793	211083
CR12	211083	DIODE SILICO 018	21793	211083
CR13	211083	DIODE SILICO 018	21793	211083
CR14	211083	DIODE SILICO 018	21793	211083
CR15	211083	DIODE SILICO 018	21793	211083
CR16	211083	DIODE SILICO 018	21793	211083
CR17	211083	DIODE SILICO 018	21793	211083
CR18	211083	DIODE SILICO 018	21793	211083
CR19	211083	DIODE SILICO 018	21793	211083
CR20	211083	DIODE SILICO 018	21793	211083
CR21	210004	DIODE SILICO SD-4	81349	1N4004
CR22	210004	DIODE SILICO SD-4	81349	1N4004
CR23	210004	DIODE SILICO SD-4	81349	1N4004
CR24	211083	DIODE SILICO 018	21793	211083
CR25	211083	DIODE SILICO 018	21793	211083
CR26	211083	DIODE SILICO 018	21793	211083
CR27	211083	DIODE SILICO 018	21793	211083
CR28	211083	DIODE SILICO 018	21793	211083
K1	310128	RELAY, 2 FORM C 1 KV 5V COIL	21793	310128
K2	310125	RELAY, REED , 1 FORM A 5 V	21793	310125
K3	310125	RELAY, REED , 1 FORM A 5 V	21793	310125
K4	310125	RELAY, REED , 1 FORM A 5 V	21793	310125
K5	310125	RELAY, REED , 1 FORM A 5 V	21793	310125
K6	310125	RELAY, REED , 1 FORM A 5 V	21793	310125
K7	310125	RELAY, REED , 1 FORM A 5 V	21793	310125
Q1	200200	TRANS NPN	21793	200200
Q2	200088	TRANS SILICO PNP	80131	2N4248
Q3	200200	TRANS NPN	21793	200200
Q4	200068	TRANS PNP	80131	2N4250
Q5	200201	TRANS DUAL NPN	21793	200201
Q6	200240	TRANS DUAL FET	21793	200240
Q7	200068	TRANS PNP	80131	2N4250
Q8	200247	TRANS DUAL FET	21793	200247
Q9	200244	TRANS High Voltage NPN	04713	MPS-A42 Series
Q10	200166	TRANS NPN	04713	MPSU05
Q11	200167	TRANS PNP	04713	MPSU55
Q12	200166	TRANS NPN	04713	MPSU05
Q13	200088	TRANS SILICO PNP	80131	2N4248
Q14	200200	TRANS NPN	21793	200200
Q15	200200	TRANS NPN	21793	200200

403874 – Assy., PCB, MAIN LOGIC *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
Q16	200200	TRANS NPN	21793	200200
R1	000203	RES CARBON 20 K 5% 1/4W	81349	RC07GF203J
R2	000303	RES CARBON 30 K 5% 1/4W	81349	RC07GF303J
R3	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R4	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R5	000242	RES CARBON 2.4 K 5% 1/4W	81349	RC07GF242J
R6	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R7	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R8	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R9	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R10	000105	RES CARBON 1 M 5% 1/4W	81349	RC07GF105J
R12	080012	RES MODULE, 8 PIN 15 K 2%	21793	080012
R13	080012	RES MODULE, 8 PIN 15 K 2%	21793	080012
R14	080012	RES MODULE, 8 PIN 15 K 2%	21793	080012
R15	080012	RES MODULE, 8 PIN 15 K 2%	21793	080012
R16	080012	RES MODULE, 8 PIN 15 K 2%	21793	080012
R17	080012	RES MODULE, 8 PIN 15 K 2%	21793	080012
R18	020690	RES WW 900 OHM .05% 50 PPM	22045	J-110
R19	020691	RES WW 90 OHM .05% 50 PPM	22045	J-110
R20	000471	RES CARBON 470 OHM 5% 1/4W	81349	RC07GF471J
R21	040197	POT CERMET 10 K 20%	11237	360T103B
R22	020692	RES WW 9.0225 OHM .25% 1/2W	22045	M-16
R23	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R24	040196	POT CERMET 1 K 20%	11237	360T102B
R25	020671	RES WW .9 OHM FSV .25% 3 W	21793	020671
R26	001878	RES CARBON 4.7 OHM 5% 1/4W	81349	RC07GF4R7J
R27	040243	POT CERMET 10 OHM 20% .5 W	73138	72PX10
R28	010938	RES METAL SET, ATTENUATOR	21793	010938
R29	040263	POT CERMET 20 K 20% .5 W	73138	72XW20K
R30	010938	RES METAL SET, ATTENUATOR	21793	010938
R31	040261	POT CERMET 2 K 20% .5 W	73138	72XW2K
R32	010938	RES METAL SET, ATTENUATOR	21793	010938
R33	040221	POT CERMET 200 OHM 20%	11237	360T Series
R34	010938	RES METAL SET, ATTENUATOR	21793	010938
R35	040244	POT CERMET 20 OHM 20% .5 W	73138	72PX20
R36	010938	RES METAL SET, ATTENUATOR	21793	010938
R37	001806	RES CARBON 200 K 5% 2 W	01121	See Descrpt.
R38	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R39	000101	RES CARBON 100 OHM 5% 1/4W	81349	RC07GF101J
R40	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J

403874 – Assy., PCB, MAIN LOGIC *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
R41	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J
R42	000104	RES CARBON 100 K 5% 1/4W	81349	RC07GF104J
R43	000222	RES CARBON 2.2 K 5% 1/4W	81349	RC07GF222J
R44	030005	RES CARBON 100 K 5% 2 W	81349	RC42GF104J
R45	040299	POT CERMET 20 K	32997	3386H-W79-203
R46	010111	RES METAL 1 M T-2 1% 1/4W	81349	RN65C1004F
R47	012011	RES METAL 1 M (NOM) FSV 1%	21793	012011 (RN55C)
R48	000203	RES CARBON 20 K 5% 1/4W	81349	RC07GF203J
R49	000101	RES CARBON 100 OHM 5% 1/4W	81349	RC07GF101J
R50	010998	RES SET, ISOLATOR .5%	21793	010998
R51	040243	POT CERMET 10 OHM 20% .5 W	73138	72PX10
R52	010998	RES SET, ISOLATOR .5%	21793	010998
R53	010802	RES METAL FSV 1%	21793	010802
R54	010802	RES METAL FSV 1%	21793	010802
R55	000225	RES CARBON 2.2 M 5% 1/4W	81349	RC07GF225J
R56	000107	RES CARBON 100 M 5% 1/4W	81349	RC07GF107J
R57	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R58	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R59	040254	POT CERMET 2 M 20% .5 W	73138	72PX2M
R60	001737	RES CARBON FSV 5% 1/4W	21793	001737
R61	000302	RES CARBON 3 K 5% 1/4W	81349	RC07GF302J
R62	000302	RES CARBON 3 K 5% 1/4W	81349	RC07GF302J
R63	000912	RES CARBON 9.1 K 5% 1/4W	81349	RC07GF912J
R64	000911	RES CARBON 910 OHM 5% 1/4W	81349	RC07GF911J
R65	403891	ZENER KIT	21793	403891
R66	010987	RES METAL SET, POSITIVE REF	21793	010987
R67	040187	POT CERMET 500 OHM 20% 3/4W	11237	360T501B
R68	010987	RES METAL SET, POSITIVE REF	21793	010987
R69	040196	POT CERMET 1 K 20%	11237	360T102B
R70	000153	RES CARBON 15 K 5% 1/4W	81349	RC07GF153J
R71	010986	RES METAL SET, NEGATIVE REF	21793	010986
R72	403891	ZENER KIT	21793	403891
R73	010986	RES METAL SET, NEGATIVE REF	21793	010986
R74	040187	POT CERMET 500 OHM 20% 3/4W	11237	360T501B
R75	000224	RES CARBON 220 K 5% 1/4W	81349	RC07GF224J
R76	000823	RES CARBON 82 K 5% 1/4W	81349	RC07GF823J
R77	000823	RES CARBON 82 K 5% 1/4W	81349	RC07GF823J
R78	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R79	000104	RES CARBON 100 K 5% 1/4W	81349	RC07GF104J
R80	000155	RES CARBON 1.5 M 5% 1/4W	81349	RC07GF155J
R81	040197	POT CERMET 10 K 20%	11237	360T103B
R82	040254	POT CERMET 2 M 20% .5 W	73138	72PX2M

403874 – Assy., PCB, MAIN LOGIC *continued*

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
R83	000514	RES	CARBON	510 K	5% 1/4W	81349	RC07GF514J
R84	000104	RES	CARBON	100 K	5% 1/4W	81349	RC07GF104J
R85	012023	RES	METAL	40.2 K	.1% 1/10W	81349	RN55E4022B
R86	012023	RES	METAL	40.2 K	.1% 1/10W	81349	RN55E4022B
R87	040270	POT	CERMET	1 K		80294	3299W
R88	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R89	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R90	001718	RES	CARBON	100 K	5% 1/2W	81349	RC20GF104J
R91	000202	RES	CARBON	2 K	5% 1/4W	81349	RC07GF202J
R92	010790	RES	METAL	36.5 K	1% 1/10W	81349	RN55E3652F
R93	001775	RES	CARBON	33 OHM	5% 1/2W	81349	RC32GF330J
R94	000392	RES	CARBON	3.9 K	5% 1/4W	81349	RC07GF392J
R95	000392	RES	CARBON	3.9 K	5% 1/4W	81349	RC07GF392J
R96	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R97	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R99	001883	RES	CARBON	6.2 OHM	5% 1 W	81349	RC32GF6R2J
R100	010600	RES	METAL	249 OHM	1% 1/10W	81349	RN55C2490F
R101	010600	RES	METAL	249 OHM	1% 1/10W	81349	RN55C2490F
R102	000203	RES	CARBON	20 K	5% 1/4W	81349	RC07GF203J
R103	000203	RES	CARBON	20 K	5% 1/4W	81349	RC07GF203J
R104	001737	RES	CARBON	FSV	5% 1/4W	21793	001737
R105	001737	RES	CARBON	FSV	5% 1/4W	21793	001737
R106	000203	RES	CARBON	20 K	5% 1/4W	81349	RC07GF203J
R107	000203	RES	CARBON	20 K	5% 1/4W	81349	RC07GF203J
R108	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R109	000103	RES	CARBON	10 K	5% 1/4W	81349	RC07GF103J
R110	020664	RES	WW	.1 OHM	1% 3 W	91637	RS-2B
R111	001737	RES	CARBON	FSV	5% 1/4W	21793	001737
R112	000471	RES	CARBON	470 OHM	5% 1/4W	81349	RC07GF471J
R113	000104	RES	CARBON	100 K	5% 1/4W	81349	RC07GF104J
R114	000106	RES	CARBON	10 M	5% 1/4W	81349	RC07GF106J
R115	001775	RES	CARBON	33 OHM	5% 1/2W	81349	RC32GF330J
S1	454065	SWITCH	FUNCTION			21793	454065
S2	454065	SWITCH	FUNCTION			21793	454065
S3	454065	SWITCH	FUNCTION			21793	454065
S4	454065	SWITCH	FUNCTION			21793	454065
S5	454067	SWITCH	RANGE			21793	454067
S6	454067	SWITCH	RANGE			21793	454067
S7	454067	SWITCH	RANGE			21793	454067
S8	600778	SWITCH	PUSHBUTTON			71590	PBI Series
TR1	300082	TRANSFORMER				21793	300082

403874 – Assy., PCB, MAIN LOGIC *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
U1	230076	INTEGRATED CIRCUIT, PLASTIC	07263	74L00
U2	230141	INTEGRATED CIRCUIT	01295	SN74L74N
U3	230248	INTEGRATED CIRCUIT	01295	SN74LS10N
U4	230312	INTEGRATED CIRCUIT	01295	SN74193N
U5	230240	INTEGRATED CIRCUIT PROM 74188	32293	1M5600CPE
U6	230192	INTEGRATED CIRCUIT, 14 DIP, INVERTER	01295	SN74LS05N
U7	230195	INTEGRATED CIRCUIT	27014	CMOS74C04N
U8	230141	INTEGRATED CIRCUIT	01295	SN74L74N
U9	230193	INTEGRATED CIRCUIT, 14 DIP, NAND GATE	01295	SN74LS00N
U10	230193	INTEGRATED CIRCUIT, 14 DIP, NAND GATE	01295	SN74LS00N
U11	230141	INTEGRATED CIRCUIT	01295	SN74L74N
U12	230141	INTEGRATED CIRCUIT	01295	SN74L74N
U13	230248	INTEGRATED CIRCUIT	01295	SN74LS10N
U14	230192	INTEGRATED CIRCUIT, 14 DIP, INVERTER	01295	SN74LS05N
U15	230247	INTEGRATED CIRCUIT	21793	230247
U16	230247	INTEGRATED CIRCUIT	21793	230247
VR1	220007	DIODE SILICO ZENER	81349	1N751A
VR2	220007	DIODE SILICO ZENER	81349	1N751A
VR3	220007	DIODE SILICO ZENER	81349	1N751A
VR4	220004	DIODE SILICO ZENER	81349	1N961B
VR5	220004	DIODE SILICO ZENER	81349	1N961B
VR6	220031	DIODE SILICO ZENER 3.3 V	04713	1/4M3.3AZ5
VR7	220007	DIODE SILICO ZENER	81349	1N751A
VR8	403891	ZENER KIT	21793	403891
VR9	220007	DIODE SILICO ZENER	81349	1N751A
VR10	220083	DIODE SILICO ZENER 5.6 V	04713	1N4734A
VR11	220035	DIODE ZENER 16 V 5%	81349	1N966B
VR12	220035	DIODE ZENER 16 V 5%	81349	1N966B
VR13	220016	DIODE SILICO ZENER	81349	1N964B
VR14	220007	DIODE SILICO ZENER	81349	1N751A
VR15	220031	DIODE SILICO ZENER 3.3 V	04713	1/4M3.3AZ5
W3	600245	JUMPER INSULATED		L-2007-1LP
W6	600245	JUMPER INSULATED		L-2007-1LP
W7	600245	JUMPER INSULATED		L-2007-1LP
W8	600245	JUMPER INSULATED		L-2007-1LP
X1	920772	RESONATOR, CERAMIC 200 kHz	91419	RMC-CR10-Fa-200kHz ± 1 kHz
Z1	080012	RESISTOR MODULE, 8 PIN 15 K 2%	21793	080012

403873 – Assy., AC CONVERTER

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
AR1	230180	INTEGRATED CIRCUIT OP AMP	27014	LM318H
C1	120007	CAP MYLAR .22 MFD 600 V 20%	27556	ZA1101
C2	130146	CAP TRIMMER .25-1.5 PFD	74970	273-0001-002
C3	100072	CAP CERAM 3.3±.5 PFD 1000 V	56289	C030B102E3R3D
C4	130146	CAP TRIMMER .25-1.5 PFD	74970	273-0001-002
C5	130159	CAP MICA 680 PFD 500 V 5%		FC681J03
C6	130127	CAP TRIMMER 10-40 PFD	52763	10S-TRIKO-24N750
C7	120230	CAP POLY .015 MFD 33 V 1%	12406	PD8458
C8	120290	CAP MYLAR .22 MFD 100 V 20%	73445	C281AH/A220K
C9	100060	CAP CERAM 15 PFD 1000 V 5%	56289	C030B102E150J
C10	100068	CAP CERAM .02 MFD 100 V 20%	56289	C023B101H203M
C11	100017	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C12	111148	CAP ELECT 100 MFD 25 V	34553	ET101X025A5
C13	100017	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C14	110043	CAP ELECT 22 MFD 25 V	34553	ET220X025A3
C15	111148	CAP ELECT 100 MFD 25 V	34553	ET101X025A5
C16	120298	CAP MYLAR 1.0 MFD 100 V 20%	73445	C281AH/A1M
C17	120298	CAP MYLAR 1.0 MFD 100 V 20%	73445	C281AH/A1M
C18	100100	CAP CERAM FSV	21793	100100
C19	100017	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C20	110151	CAP TANTA 10 MFD 35 V 20%	05397	T362C106M035A
CR1	211083	DIODE SILICO 018	21793	211083
CR2	211083	DIODE SILICO 018	21793	211083
CR3	211083	DIODE SILICO 018	21793	211083
CR4	211083	DIODE SILICO 018	21793	211083
CR5	211083	DIODE SILICO 018	21793	211083
CR6	211083	DIODE SILICO 018	21793	211083
K1	310125	RELAY, REED 1 FORM A	21793	310125
K2	310125	RELAY, REED 1 FORM A	21793	310125
Q1	200230	TRANS FET N-CHAN, SIL JUNCTION		E305
Q2	200230	TRANS FET N-CHAN, SIL JUNCTION		E305
Q3	200096	TRANS PNP	81349	2N4917
Q4	200163	TRANS SILICO NPN	07263	EN916

403873 – Assy., AC CONVERTER *continued*

REF DES	DANA P/N	DESCRIPTION				FSC	MANU P/N
R1	010996	RES	METAL	1 MEG	.5% 1 W	81349	RN75E1004D
R2	010994	RES	METAL	219.5 K	.5% 1/10W	81349	RN55E
R3	040262	POT	CERMET	5 K	20% .5 W	73138	72XW5K
R4	010993	RES	METAL	2.117 K	.5% 1/10W	81349	RN55E
R5	040257	POT	CERMET	50 OHM	20% .5 W	80294	3389S-500
R6	010995	RES	METAL	122.2 OHM	.5% 1/10W	81349	RN55E
R7	010992	RES	METAL	100 OHM	.5% 1/10W	81349	RN55E1000D
R8	000106	RES	CARBON	10 M	5% 1/4W	81349	RC07GF106J
R9	000756	RES	CARBON	75 M	5% 1/4W	81349	RC07GF756J
R10	000515	RES	CARBON	5.1 M	5% 1/4W	81349	RC07GF515J
R11	000104	RES	CARBON	100 K	5% 1/4W	81349	RC07GF104J
R12	000104	RES	CARBON	100 K	5% 1/4W	81349	RC07GF104J
R13	000162	RES	CARBON	1.6 K	5% 1/4W	81349	RC07GF162J
R14	000101	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R15	000133	RES	CARBON	13 K	5% 1/4W	81349	RC07GF133J
R16	000133	RES	CARBON	13 K	5% 1/4W	81349	RC07GF133J
R17	000162	RES	CARBON	1.6 K	5% 1/4W	81349	RC07GF162J
R18	000101	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R19	000101	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R20	000101	RES	CARBON	100 OHM	5% 1/4W	81349	RC07GF101J
R21	000102	RES	CARBON	1 K	5% 1/4W	81349	RC07GF102J
R22	010771	RES	METAL	976 OHM	1% 1/10W	81349	RN55E9760F
R23	040225	POT	CERMET	50 OHM	20%	73138	89PR50
R24	000683	RES	CARBON	68 K	5% 1/4W	81349	RC07GF683J
R25	000154	RES	CARBON	150 K	5% 1/4W	81349	RC07GF154J

403856 – Assy., DISPLAY

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
C1	110125	CAP TANTA 2.2 MFD 35 V 20%	05397	T368B225M035AS
LED 1	210074	DIODE, LED 7 Segment Display, YELLOW	04404	HP5082-7660
LED 2	210074	DIODE, LED 7 Segment Display, YELLOW	04404	HP5082-7660
LED 3	210074	DIODE, LED 7 Segment Display, YELLOW	04404	HP5082-7660
LED 4	210074	DIODE, LED 7 Segment Display, YELLOW	04404	HP5082-7660
LED 5	210074	DIODE, LED 7 Segment Display, YELLOW	04404	HP5082-7660
LED 6	210082	DIODE, LED DISPLAY	50434	HP5082-7662
Q1	200184	TRANS PNP	04713	MPSA55
Q2	200184	TRANS PNP	04713	MPSA55
Q3	200184	TRANS PNP	04713	MPSA55
Q4	200184	TRANS PNP	04713	MPSA55
Q5	200184	TRANS PNP	04713	MPSA55
R1	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R2	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R3	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R4	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R5	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R6	000111	RES CARBON 110 OHM 5% 1/4W	81349	RC07GF111J
R7	000111	RES CARBON 110 OHM 5% 1/4W	81349	RC07GF111J
R8	000111	RES CARBON 110 OHM 5% 1/4W	81349	RC07GF111J
R9	000111	RES CARBON 110 OHM 5% 1/4W	81349	RC07GF111J
R10	000111	RES CARBON 110 OHM 5% 1/4W	81349	RC07GF111J
R11	000111	RES CARBON 110 OHM 5% 1/4W	81349	RC07GF111J
R12	000111	RES CARBON 110 OHM 5% 1/4W	81349	RC07GF111J
R13	000111	RES CARBON 110 OHM 5% 1/4W	81349	RC07GF111J
R14	000111	RES CARBON 110 OHM 5% 1/4W	81349	RC07GF111J
R15	000111	RES CARBON 110 OHM 5% 1/4W	81349	RC07GF111J
R16	000111	RES CARBON 110 OHM 5% 1/4W	81349	RC07GF111J
R17	000111	RES CARBON 110 OHM 5% 1/4W	81349	RC07GF111J
R18	000271	RES CARBON 270 OHM 5% 1/4W	81349	RC07GF271J
R19	000271	RES CARBON 270 OHM 5% 1/4W	81349	RC07GF271J
U1	230192	INTEGRATED CIRCUIT 14 DIP, INVERTER	01295	SN74LS05N
U2	230120	INTEGRATED CIRCUIT	07263	3814
U3	230236	INTEGRATED CIRCUIT 16-DIP	01295	SN74LS47N
U4	230074	INTEGRATED CIRCUIT PLASTIC	07263	7442

403879 – Assy., PCB, DATA OUTPUT

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	100019	CAP	CERAM	.002 MFD	1000 V	10%	56289	C023B102F202M
C2	110162	CAP	TANTA	.33 MFD	35 V	5%	05397	T368A334J035AS
C3	100019	CAP	CERAM	.002 MFD	1000 V	10%	56289	C023B102F202M
C4	110143	CAP	TANTA	1 MFD	35 V	20%	05397	T368A105M035AS
C5	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C6	110100	CAP	ELECT	1000 MFD	10 V		34553	ET102X010A01
CR1	210004	DIODE	SILICO	SD-4			81349	1N4004
CR2	210004	DIODE	SILICO	SD-4			81349	1N4004
CR3	211083	DIODE	SILICO	018			21793	211083
CR4	211083	DIODE	SILICO	018			21793	211083
OCI-1	250005	OPTO-ISOLATOR, LOGIC DRIVE					21793	250005
OCI-2	250005	OPTO-ISOLATOR, LOGIC DRIVE					21793	250005
OCI-3	250005	OPTO-ISOLATOR, LOGIC DRIVE					21793	250005
OCI-4	250005	OPTO-ISOLATOR, LOGIC DRIVE					21793	250005
OCI-5	250005	OPTO-ISOLATOR, LOGIC DRIVE					21793	250005
OCI-6	250005	OPTO-ISOLATOR, LOGIC DRIVE					21793	250005
Q1	200200	TRANS		NPN			21793	200200
Q2	200200	TRANS		NPN			21793	200200
Q3	200166	TRANS		NPN			04713	MPSU05
Q4	200200	TRANS		NPN			21793	200200
R1	000331	RES	CARBON	330 OHM		5% 1/4W	81349	RC07GF331J
R2	000331	RES	CARBON	330 OHM		5% 1/4W	81349	RC07GF331J
R3	000331	RES	CARBON	330 OHM		5% 1/4W	81349	RC07GF331J
R4	000331	RES	CARBON	330 OHM		5% 1/4W	81349	RC07GF331J
R5	000431	RES	CARBON	430 OHM		5% 1/4W	81349	RC07GF431J
R6	000431	RES	CARBON	430 OHM		5% 1/4W	81349	RC07GF431J
R7	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R8	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R9	000153	RES	CARBON	15 K		5% 1/4W	81349	RC07GF153J
R10	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R11	000302	RES	CARBON	3 K		5% 1/4W	81349	RC07GF302J
R12	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R13	000331	RES	CARBON	330 OHM		5% 1/4W	81349	RC07GF331J
R14	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R15	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J

403879 – Assy., PCB, DATA OUTPUT *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
R16	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R17	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R18	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R19	000331	RES CARBON 330 OHM 5% 1/4W	81349	RC07GF331J
R20	000302	RES CARBON 3 K 5% 1/4W	81349	RC07GF302J
R21	000302	RES CARBON 3 K 5% 1/4W	81349	RC07GF302J
R22	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R23	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R24	000222	RES CARBON 2.2 K 5% 1/4W	81349	RC07GF222J
U1	230121	INTEGRATED CIRCUIT 14 PIN	01295	SN74L90N
U2	230076	INTEGRATED CIRCUIT PLASTIC	07263	74L00
U3	230234	INTEGRATED CIRCUIT 14 DIP, HEX INVERTER	01295	SN74LS04N
U4	230239	INTEGRATED CIRCUIT	01295	SN74153
U5	230193	INTEGRATED CIRCUIT 14 DIP, NAND GATE	01295	SN74LS00N
U6	230239	INTEGRATED CIRCUIT	01295	SN74153
U7	230237	INTEGRATED CIRCUIT PLASTIC	01295	SN74LS123N
U8	230234	INTEGRATED CIRCUIT 14 DIP, HEX INVERTER	01295	SN74LS04N
U9	230336	INTEGRATED CIRCUIT	01295	74LS14
U10	230238	INTEGRATED CIRCUIT	01295	74LS164
U11	230238	INTEGRATED CIRCUIT	01295	74LS164
U12	230238	INTEGRATED CIRCUIT	01295	74LS164
U13	230238	INTEGRATED CIRCUIT	01295	74LS164
VR3	220019	DIODE SILICO ZENER	81349	1N752A

403889 – Assy., BATTERY PACK OPTION

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
A1	403888	MODULE ASSY., BATTERY PACK	21793	403888
W1	600245	JUMPER INSULATED		L-2007-1LP
W2	600245	JUMPER INSULATED		L-2007-1LP
W3	600245	JUMPER INSULATED		L-2007-1LP
W4	600245	JUMPER INSULATED		L-2007-1LP
W5	600245	JUMPER INSULATED		L-2007-1LP

403888 – Assy., MODULE, BATTERY PACK

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
A1	403887	PCB ASSY, BATTERY PACK OPTION	21793	403887
B1 to B5	920643	BATTERY (5*) Rechargeable 1.2 V	31741	4.0SCL - Size D

403887 – Assy., PCB, BATTERY PACK

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
C1	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C2	110151	CAP	TANTA	10 MFD	35 V	20%	05397	T362C106M035A
C3	110006	CAP	TANTA	100 MFD	10 V	10%	05397	T310C107K010AS
CR1	220007	DIODE	SILICO	ZENER			81349	1N751A
CR2	211083	DIODE	SILICO		018		21793	211083
CR3	211083	DIODE	SILICO		018		21793	211083
CR4	211083	DIODE	SILICO		018		21793	211083
CR5	211083	DIODE	SILICO		018		21793	211083
CR6	211083	DIODE	SILICO		018		21793	211083
CR7	211083	DIODE	SILICO		018		21793	211083
CR8	211083	DIODE	SILICO		018		21793	211083
CR10	210004	DIODE	SILICO		SD4		81349	1N4004
CR11	210004	DIODE	SILICO		SD4		81349	1N4004
K1	310125	RELAY	REED		1 FORM A	5 V	21793	310125
P11	600655	RECPTLE, HOUSING					27264	1292R-2
Q1	200200	TRANS		NPN			21793	200200
Q2	200200	TRANS		NPN			21793	200200
Q3	200088	TRANS	SILICO	PNP			80131	2N4248
Q4	200166	TRANS		NPN			04713	MPSU05
Q5	200166	TRANS		NPN			04713	MPSU05
Q6	200115	TRANS	POWER	PNP			04713	MPSU51
R1	000751	RES	CARBON	750 OHM		5% 1/4W	81349	RC07GF751J
R2	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R3	000512	RES	CARBON	5.1 K		5% 1/4W	81349	RC07GF512J
R4	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R5	000513	RES	CARBON	151 K		5% 1/4W	81349	RC07GF513J
R6	000221	RES	CARBON	220 OHM		5% 1/4W	81349	RC07GF221J
R7	000300	RES	CARBON	30 OHM		5% 1/4W	81349	RC07GF300J
R8	000104	RES	CARBON	100 K		5% 1/4W	81349	RC07GF104J
R9	000202	RES	CARBON	4 2 K		5% 1/4W	81349	RC07GF202J
R10	000271	RES	CARBON	270 OHM		5% 1/4W	81349	RC07GF271J
R11	001812	RES	CARBON	270 OHM		5% 1/2W	01121	See Descrpt.
R12	001781	RES	CARBON	6.2 OHM		5% 1/4W	81349	RC07GF6R2J
T1	300084	TRANSFORMER, INVERTER					21793	300084
W1	600245	JUMPER, INSULATED						L-2007-1LP