NOTE

This manual documents the Model 8502A Digital Multimeter and its assemblies at the revision levels shown in Appendix 7A. If your instrument contains assemblies with different revision letters, it will be necessary for you to either update or backdate this manual. Refer to the supplemental change/errata sheet for newer assemblies, or to the backdating sheet in Appendix 7A for older assemblies.

8502A Digital Multimeter

Instruction Manual

P/N 471466
March 1978

FLUKE®

WARRANTY

Notwithstanding any provision of any agreement the following warranty is exclusive:

The JOHN FLUKE MFG. CO., INC., warrants each instrument it manufactures to be free from defects in material and workmanship under normal use and service for the period of 1-year from date of purchase. This warranty extends only to the original purchaser. This warranty shall not apply to fuses, disposable batteries (rechargeable type batteries are warranted for 90-days), or any product or parts which have been subject to misuse, neglect, accident, or abnormal conditions of operations.

In the event of failure of a product covered by this warranty, John Fluke Mfg. Co., Inc., will repair and calibrate an instrument returned to an authorized Service Facility within 1 year of the original purchase; provided the warrantor's examination discloses to its satisfaction that the product was defective. The warrantor may, at its option, replace the product in lieu of repair. With regard to any instrument returned within 1 year of the original purchase, said repairs or replacement will be made without charge. If the failure has been caused by misuse, neglect, accident, or abnormal conditions of operations, repairs will be billed at a nominal cost. In such case, an estimate will be submitted before work is started, if requested.

THE FOREGOING WARRANTY IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS, OR ADEQUACY FOR ANY PARTICULAR PURPOSE OR USE. JOHN FLUKE MFG. CO., INC., SHALL NOT BE LIABLE FOR ANY SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER IN CONTRACT, TORT, OR OTHERWISE.

If any failure occurs, the following steps should be taken:

1. Notify the JOHN FLUKE MFG. CO., INC., or nearest Service facility, giving full details of the difficulty, and include the model number, type number, and serial number. On receipt of this information, service data, or shipping instructions will be forwarded to you.

2. On receipt of the shipping instructions, forward the instrument, transportation prepaid. Repairs will be made at the Service Facility and the instrument returned, transportation prepaid.

SHIPPING TO MANUFACTURER FOR REPAIR OR ADJUSTMENT

All shipments of JOHN FLUKE MFG. CO., INC., instruments should be made via United Parcel Service or "Best Way" prepaid. The instrument should be shipped in the original packing carton; or if it is not available, use any suitable container that is rigid and of adequate size. If a substitute container is used, the instrument should be wrapped in paper and surrounded with at least four inches of excelsior or similar shock-absorbing material.

CLAIM FOR DAMAGE IN SHIPMENT TO ORIGINAL PURCHASER

The instrument should be thoroughly inspected immediately upon original delivery to purchaser. All material in the container should be checked against the enclosed packing list. The manufacturer will not be responsible for shortages against the packing sheet unless notified immediately. If the instrument is damaged in any way, a claim should be filed with the carrier immediately. (To obtain a quotation to repair shipment damage, contact the nearest Fluke Technical Center.) Final claim and negotiations with the carrier must be completed by the customer.

The JOHN FLUKE MFG. CO., INC, will be happy to answer all applications or use questions, which will enhance your use of this instrument. Please address your requests or correspondence to: JOHN FLUKE MFG. CO., INC., P.O. BOX 43210, MOUNTLAKE TERRACE, WASHINGTON 98043, ATTN: Sales Dept. For European Customers: Fluke (Holland) B.V., P.O. Box 5053, 5004 EB, Tilburg, The Netherlands.

*For European customers, Air Freight prepaid.

John Fluke Mfg. Co., Inc., P.O. Box 43210, Mountlake Terrace, Washington 98043

Rev. 4/80

Section 1
Introduction & Specifications

1-1. INTRODUCTION

1-2. This manual comprises eight modular sections. You will find herein up-to-date information for installing, operating and maintaining the Fluke Model 8502A Digital Multimeter. Generally, complete descriptions and instructions are provided for the 8502A mainframe, modules necessary for DC Volts and DC Ratio measurement, and for any optional modules (AC Converter, Ohms Converter, etc.) that you may have ordered with your 8502A. Specifically, each section contains:

1. Section 1 – General description, specifications.

2. Section 2 – Operating instruction, capabilities.

3. Section 3 – Theory of operation, including simplified schematic and functional block diagrams.

4. Section 4 – Maintenance, adjustments and troubleshooting.

5. Section 5 – List of replaceable parts, with parts locators.

6. Section 6 – Option and accessory information, including complete information on any option ordered with the 8502A. As the need arises to broaden your 8502A's capabilities, the most recent information will be included with any options you order.

7. Section 7 – General information (list of abbreviations, federal supply codes, Service Centers, and Sales Respresentatives).

8. Section 8 – Schematic diagrams.

1-3. DESCRIPTION

1-4. The Model 8502A Digital Multimeter is a 6 1/2 digit instrument employing microprocessor control and a bus structure. Memory programming either from the front panel or through a remote interface permits a number of operations to be performed on the measured input before it is displayed. The standard configuration allows for measurement of dc volts in 5 ranges. Four ranges are available for ac volts when either optional ac converter is installed. Resistance can be measured in 8 ranges. Current can be measured in 5 ranges.

1-5. Modular Construction

1-6. Considerable versatility is realized through the 8502A's unique construction. All active components are contained in modules which plug into a mainframe motherboard. This module-motherboard mating, combined with bus architecture and microprocessor control, yields both ease of option selection and reduced downtime.

1-7. Microprocessor Control

1-8. All modules function under direct control of a microprocessor based controller. Each module is addressed by the controller as a memory location. External reference values and offsets can be applied separately, stored in memory, and automatically used as factors in all subsequent readings. Digital filtering utilizes averaged samples for each reading.

1-9. Recirculating Remainder A/D Conversion

1-10. The 8502A adapts Fluke's patented recirculating remainder (R^2) A/D conversion technique to microprocessor control. This combination provides fast, accurate linear measurements and long-term stability.

1-11. Options and Accessories

1-12. Remote interfaces, AC converters, a current converter and an ohms converter are among the numerous options and accessories available for the 8502A. Refer to Tables 1-1 and 1-2 for complete listings. AC conversion can be accomplished with either an ac averaging module (–01) or a true RMS module (–09A). Any one of three remote interface modules (–05, –06, –07) may be installed at one time; the isolator module (–08A) must then be installed to maintain guarding of analog and high quality busses during remote operations. Maximum interfacing with digital systems is thus realized. Calibration downtime is reduced through the use of a calibration memory module (–04); correction factors may be entered from the front panel, providing automatic correction for further measurements. Analog inputs from a remote position are permitted when Rear Input (Option–17) is installed. Selectable front or rear analog inputs are available with Option –16.

1-13. SPECIFICATIONS

1-14. Mainframe specifications with DC Volts and DC Ratio measurement capability are presented in Table 1-3. Optional function specifications are supplied with the respective option modules and included in Section 6. The table of specifications presented here is divided into three parts:

1. General Specifications.
2. Accuracy.
3. Instrument Operating Characteristics.

Table 1-1. 8502A Options

Option No.	Name	Notes
01	AC/DC Converter (Averaging)	1, 3
02	Ohms Converter	
03	Current Shunts	3
04	Calibration Memory	
05	IEEE Standard 488–1975 Interface	2
06	Bit Serial Asynchronous Interface	2
07	Parallel Interface	2
08A	Isolator	4
09A	AC/DC Converter (True RMS)	1, 3
16	Front–Rear Switchable Input	5
17	Rear Input	

1) Options 01 and 09A cannot be installed simultaneously.
2) Only one of Options 05, 06, and 07 can be installed at any time.
3) For the AC portion of Option 03 to operate, either Option 01 or 09A must be installed.
4) Option 08A must be installed for remote operations.
5) Option 16 must be factory installed.

Table 1-2. 8502A Accessories

Model or Part No.	Name
M04-205-600	Rack Ear Mounting Assembly
M00-260-610	18-inch Rack Slides
M00-280-610	24-inch Rack Slides
80F-5	High Voltage Probe
80F-15	High Voltage Probe
81RF	High Frequency Probe
82RF	High Frequency Probe
KDM1	Keyboard Display Module w/Cable
Y8001	IEEE Std. Cable, 1 Meter Length
Y8002	IEEE Std. Cable, 2 Meter Length
Y8003	IEEE Std. Cable, 4 Meter Length
MIS-7011K*	Extender Assembly
MIS-7190K*	Static Controller
MIS-7191K*	Test Module
MIS-7013K*	Bus Interconnect and Monitor

*For use during service or repair

Table 1-3. Specifications

GENERAL SPECIFICATIONS

DIMENSIONS

	H		L		W
cm	10.8	x	42.5	x	43.2
Inches	4.25	x	16.75	x	17

WEIGHT

	Basic	Fully Loaded
kg	9.1	10.92
Lbs	20	24

OPERATING POWER

Basic Instrument	12 watts	115V ac or 230V ac ±10%
Fully Loaded	24 watts	50–60 Hz

WARM-UP

1 hour to rated accuracy

SHOCK AND VIBRATION

Meets requirements of MIL-T-28800 for Class 5 style E equipment.

TEMPERATURE RANGE

Operating	0°C to 50°C
Non Operating	–40°C to 70°C*

**0°C to 50°C operating and non-operating with calibration memory option (–04) installed.*

HUMIDITY RANGE

(Operating to Full Accuracy)

0°C to 18°C	80% RH
18°C to 40°C	75% RH
40°C to 50°C	60% RH

OVERLOAD

LO to Guard	127V max
Guard to Chassis	1000V max
HI Sense to HI Source	127V max
LO Sense to LO Source	127V max
HI Sense to LO Sense	1000V max
HI Source to LO Source	280V max

ACCURACY

Note

The stated accuracies are valid under the following environmental conditions.

Temperature: 18°C to 28°C (Except 24 hour: 22°C to 24°C)

Humidity: ≤75%

Line Regulation: 90V to 110V, 103.5V to 126.5V, or 207V to 253V @ 45 to 66 Hz

DC Volts

Normal Resolution (5 1/2 digits)

Range	Full Scale	Resolution	Accuracy ± (% of Input + Number of Digits)		
			24 Hours	90 Days	1 Year
100 mV	312 mV	1 uV	0.002 + 4	0.003 + 5	0.005 + 8
1 V	2.5 V	10 uV	0.001 + 1	0.002 + 1	0.004 + 1
10 V	20 V	100 uV	0.001 or 1*	0.001 + 1	0.002 + 1
100 V	160 V	1 mV	0.001 + 1	0.002 + 1	0.004 + 1
1000 V	1200 V	10 mV	0.001 + 1	0.002 + 1	0.004 + 1

**Whichever is greater.*

Table 1-3. Specifications (cont)

ACCURACY (Continued)

DC Volts (Continued)

High Resolution (HI RES or CAL — 6 1/2 digits)

Range	Full Scale	Resolution	Accuracy ± (% of Input + Number of Digits)		
			24 Hours	90 Days	1 Year
1 V	2.5 V	1 uV	0.001 + 6	0.002 + 8	0.004 + 9
10 V	20 V	10 uV	0.001 or 6*	0.001 + 8	0.002 + 9
100 V	160 V	100 uV	0.001 + 6	0.002 + 8	0.004 + 9
1000 V	1200 V	1 mV	0.001 + 6	0.002 + 8	0.004 + 9

**Whichever is greater.*

DC Ratio

Ext. Ref. Voltage	Accuracy
±20V to ±40V	±(A + B + 10 ppm)
$\pm V_{min.}$* to ±20V	$\pm\left(A + B + \frac{200\text{ ppm}}{\lvert V_{xref}\rvert}\right)$

A =10V dc Range Accuracy
B =Input Signal Function and Range Accuracy
V_{min} =Minimum Allowable External Reference Voltage
$|V_{xref}|$ =Absolute Value of External Reference Voltage

**The formula for determining V_{min} is included in Instrument Operating Characteristics*

Example Calculations for External Reference Accuracy:

1. Input = + 90.000V, Ext. Ref. Input = 30.000V (+ 15V to Ext. Ref. HI, −15V to Ext. Ref. LO)
   A = .001% + 1 Digit B = .001% + 1 Digit
   Ratio Accuracy = ±(A + B + 10 ppm) = ±(.001% + 1 Digit + .001% +1 Digit + .001% = ±(.003% +2 Digits)
   Reading may be between 3.0003 and 2.9997

2. Input = 1.20000V, Ext. Ref. Input = .12000 (V_{min} for 1V Range)
   A = .001% + 1 Digit, B = .001% + 1 Digit, $\frac{200\text{ ppm}}{V_{xref}} = \frac{.02\%}{.12} = .1667\%$

   Ratio Accuracy = ±.001% + 1 Digit + .001% +1 Digit + .1667%) = ±(.1687% + 2 Digits)
   Reading may be between .998313 and 1.001686.

INSTRUMENT OPERATING CHARACTERISTICS

DC Volts

TEMPERATURE COEFFICIENT (0°C to 18°C and 28°C to 50°C)

Range	Temperature Coefficient
100 mV	± (3 ppm/reading + 0.5 digit)/°C
1V	±(3 ppm/reading +0.1 digit)/ °C
10 V	± (2 ppm/reading + 0.05 digit)/°C*
100 V	± (3 ppm/reading + 0.1 digit)/°C*
1000 V	± (3 ppm/reading + 0.05 digit)/°C*

**For High Resolution Multiply Digits by 10.*

INPUT IMPEDANCE

Range	Input Impedance
100 mV	>10,000 MΩ
1V	>10,000 MΩ
10 V	>10,000 MΩ
100 V	10 MΩ
1000 V	10 MΩ
Guard to Chassis	∞

INPUT BIAS CURRENT

	At time of Cal	30 Days (23°C ± 1°C)	Temperature Coefficient
Bias Current	<± 5 pA	<± 50 pA	± 3 pA/°C

Table 1-3. Specifications (Cont)

INSTRUMENT OPERATING CHARACTERISTICS (Continued)

DC Volts (Continued)

RESPONSE TIME

Digitizing Time			Analog Settling Time Within Voltmeter		
Reading Rate*		Digitizing Time	Filter Mode	Step Input to 0.01% of Change	Step Input to 0.001% of Change
50 Hz line	4 Samples/Rdg	22 ms	Filter, Fast	40 ms	50 ms
	32 Samples/Rdg	162 ms	Bypass	2 ms	20 ms
	128 Samples/Rdg	642 ms	Bypass	2 ms	20 ms
60 Hz line	4 Samples/Rdg	18 ms	Filter, Slow	400 ms	500 ms
	32 Samples/Rdg	136 ms	Bypass	2 ms	20 ms
	128 Samples/Rdg	546 ms	Bypass	2 ms	20 ms

**Number of samples per reading is programmable from 1 (2^0) to 131,072 (2^{17}) in 18 binary steps.*

ZERO STABILITY

Better than 5 μV for 90 days after a one hr. warm-up. Front Panel pushbutton auto zero is provided. The zero correction is stored in memory until power is interrupted or the 8502A is RESET. If calibration memory Option –04 is installed, the zero correction is retained.

OVERLOAD

±1200V DC, 1200V peak to 60 Hz, or 1400V peak above 60 Hz may be applied continuously to any dc range without permanent damage. Maximum common mode rate of voltage rise is 1000V/μsec.

NOISE REJECTION

	Normal Mode			Common Mode	
Line/Filter Frequency	4 Samples/ Rdg	32 Samples/ Rdg	128 Samples/ Rdg	True	Effective
50 Hz Fast Filter	60 dB	70 dB	75 dB	100 dB at 60 Hz for 1 KΩ unbalance	Sum of Common Mode Rejection and Normal Mode Rejection
50 Hz Slow Filter	85 dB	90 dB	95 dB		
60 Hz Fast Filter	60 dB	70 dB	75 dB		
60 Hz Slow Filter	90 dB	95 dB	100 dB		

128 SAMPLES/READING

Typical Performance with 60 Hz Line
(Combined digital and analog filtering)

Cusps shown are at multiples of 60 Hz line frequency. Similar cusps (not shown) occur every 7½ Hz.

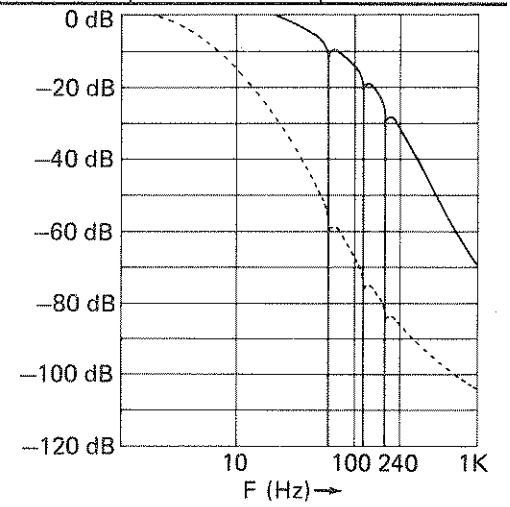


Table 1-3. Specifications (Cont)

INSTRUMENT OPERATING CHARACTERISTICS (Continued)

DC Ratio

INPUT IMPEDANCE	SOURCE IMPEDANCE
Ext Ref HI or LO > 10,000 MΩ relative to Ohms Guard* or Sense LO	Resistive Unbalance (Ext Ref HI to LO) <4 kΩ Total Resistance Sense LO from either HI or LO <20 kΩ
BIAS CURRENT	**OVERLOAD (Ext Ref HI or LO)**
Ext Ref HI or LO relative to Ohms Guard* or Sense LO <5 nA	±180 volts peak , 127V rms (relative to Ohms Guard* or Sense LO) X (360V peak HI to LO)

** Ohms Guard available through rear input (−16 or −17 Option)*

NOISE REJECTION

Normal Mode	Common Mode, All Inputs Driven
Sense Input—Same as dc volts **Ext Ref Input**—dc, line frequency and 2x line frequency >100 dB	**Sense Input**—Same as dc volts **Ext Ref Input**—Line frequency and 2x line frequency, 75 dB

RESPONSE TIME

Settling Time

Sense Input Fast Filter < 50 ms to 0.001% of change
Sense Input Slow Filter < 500 ms to 0.001% of change

Digitizing Time

NOTE

The Sense Input is measured prior to measuring Ext Ref HI and LO.

Ext Ref Input—Each input HI and LO

90 ms at 60 Hz line frequency
107 ms at 50 Hz line frequency

Ext Ref Calibration—12 ms

Sense Input		
Line Volt	Approx. Rdg. Rate	Digitizing Time
60 Hz	4½ rdg/s	136 ms
	1½ rdg/s	536 ms
50 Hz	3½ rdg/s	162 ms
	1¼ rdg/s	642 ms
60 Hz	4 samples/rdg	18 ms
50 Hz	4 samples/rdg	22 ms

EXT REF VOLTAGE RANGE

Maximum Ext Ref Voltage = ±40V between Ext Ref HI and LO terminals, providing neither terminal is greater than ±20V relative to the Sense LO or Ohms Guard terminals.

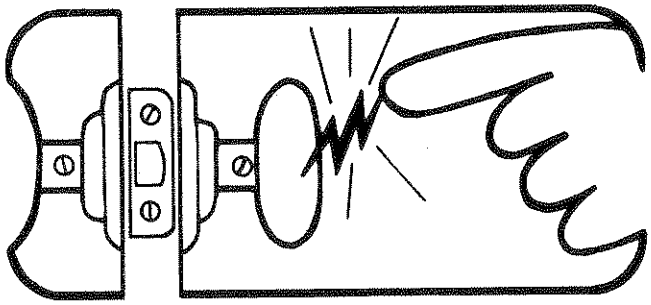
Minimum Ext Ref Voltage = ±0.0001V, or $\frac{V_{input}}{10^9}$ (whichever is greater)

MAXIMUM DISPLAY— Ratio, Scaling or Offset Mode = ±1.00000 x 10^9 in all Ranges

static awareness

A Message From

John Fluke Mfg. Co., Inc.

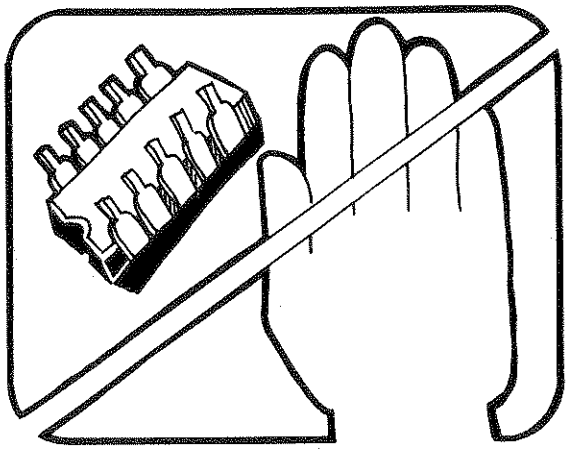


Some semiconductors and custom IC's can be damaged by electrostatic discharge during handling. This notice explains how you can minimize the chances of destroying such devices by:

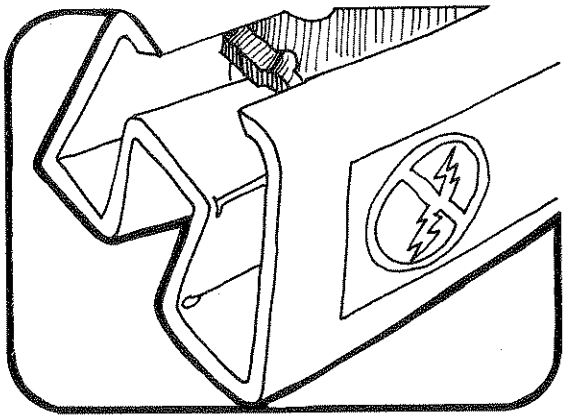
1. Knowing that there is a problem.
2. Learning the guidelines for handling them.
3. Using the procedures, and packaging and bench techniques that are recommended.

The Static Sensitive (S.S.) devices are identified in the Fluke technical manual parts list with the symbol "⊗".

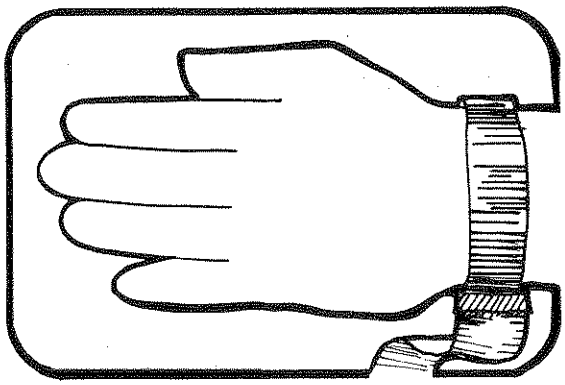
The following practices should be followed to minimize damage to S.S. devices.



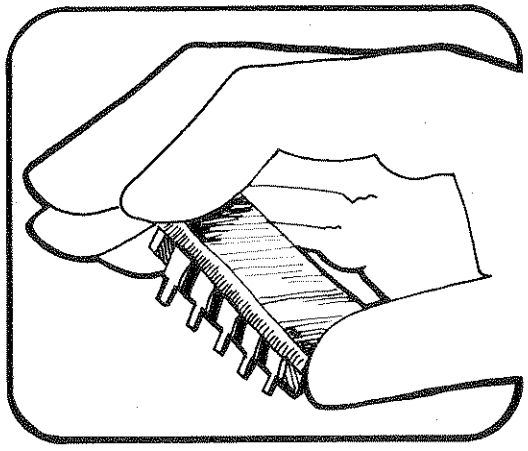
1. MINIMIZE HANDLING



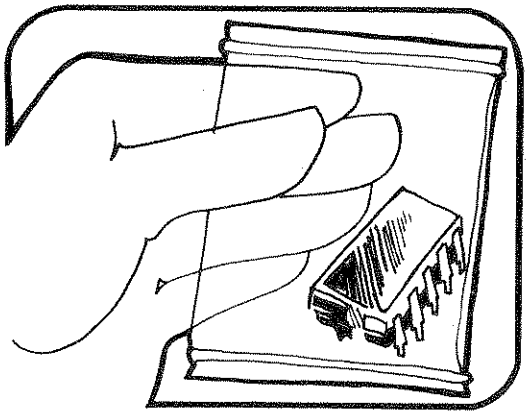
2. KEEP PARTS IN ORIGINAL CONTAINERS UNTIL READY FOR USE.



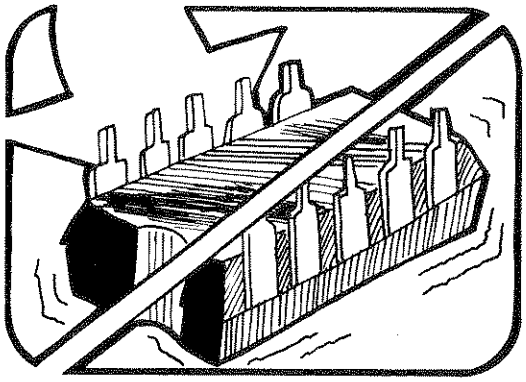
3. DISCHARGE PERSONAL STATIC BEFORE HANDLING DEVICES



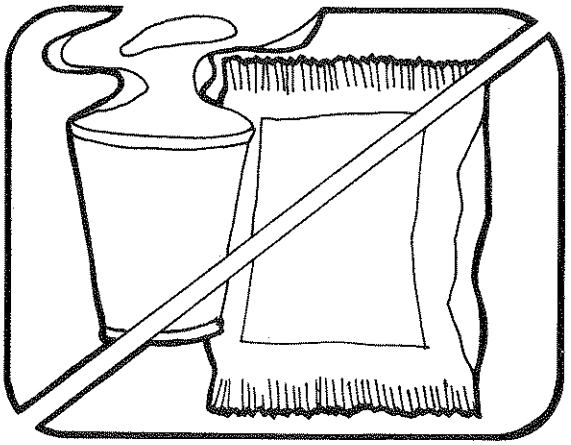
4. HANDLE S.S. DEVICES BY THE BODY



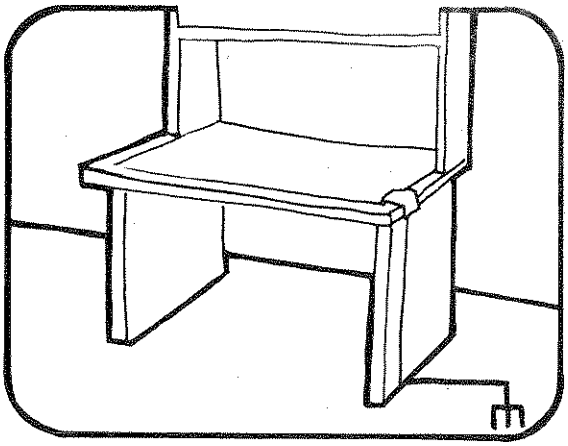
5. USE ANTI-STATIC CONTAINERS FOR HANDLING AND TRANSPORT



6. DO NOT SLIDE S.S. DEVICES OVER ANY SURFACE



7. AVOID PLASTIC, VINYL AND STYROFOAM IN WORK AREA



8. HANDLE S.S. DEVICES ONLY AT A STATIC-FREE WORK STATION

9. ONLY ANTI-STATIC TYPE SOLDER-SUCKERS SHOULD BE USED.

10. ONLY GROUNDED TIP SOLDERING IRONS SHOULD BE USED.

Anti-static bags, for storing S.S. devices or pcbs with these devices on them, can be ordered from the John Fluke Mfg. Co., Inc.. See section 5 in any Fluke technical manual for ordering instructions. Use the following part numbers when ordering these special bags.

John Fluke Part No.	Bag Size
453522	6" x 8"
453530	8" x 12"
453548	16" x 24"
454025	12" x 15"

Section 2
Operating Instructions

2-1. INTRODUCTION

2-2. Installation and operation of the 8502A Digital Multimeter are explained in this section. The 8502A's full capabilities may be realized by thoroughly reading and understanding these operating instructions. Explanations and applications are provided for all standard functions and operations. Read them. Should any difficulties arise, contact your nearest Fluke Sales Representative (list in Section 7), or the John Fluke Mfg. Co., Inc. (P.O. Box 43210, Mountlake Terrace, Wa., 98043; tel. 206 774-2211).

2-3. SHIPPING INFORMATION

2-4. The 8502A is packaged and shipped in a foam-packed container. Upon receipt of the instrument, a thorough inspection should be made to reveal any possible shipping damage. Special instructions for inspection and claims are included with the shipping container.

2-5. If reshipment is necessary, the original container should be used. If the original container is not available, a new container can be obtained from John Fluke Mfg. Co., Inc. Please reference the instrument model number when requesting a new shipping container.

2-6. INSTALLATION

2-7. Non-marring feet and a tilt-down bail are installed on the instrument for field or bench use. A rack-mounting kit and rack slides are available for use with standard 19-inch equipment racks. Information regarding installation or rack-mounting accessories is contained in Section 6.

2-8. The 8502A operates from either 115V ac ±10% or 230V ac ± 10%, 50 or 60 Hz (10% tolerance translates to high and low limits of: 103.5 to 126.5V ac, 207 to 253V ac).

WARNING

TO AVOID ELECTRICAL SHOCK, PROPERLY GROUND THE CHASSIS. A GROUND CONNECTION IS PROVIDED IN THE THREE-PRONG POWER CONNECTOR; IF PROPER GROUND IN YOUR POWER SYSTEM IS IN DOUBT, MAKE A SEPARATE GROUND CONNECTION TO THE REAR PANEL CHASSIS BINDING POST. OTHERWISE, THE POSSIBILITY OF ELECTRICAL SHOCK MAY EXIST IF HIGH VOLTAGE IS MEASURED WITH THE LEADS REVERSED (INPUT HI GROUNDED).

2-9. OPERATING FEATURES

2-10. Display, control, and terminal locations on the 8502A can be found in Figure 2-1. Table 2-1, will then detail respective functions. In addition, a convenient set of condensed operating instructions is provided under the instrument's front right side. Just pull out the tab.

2-11. OPERATING NOTES

2-12. Input Power

2-13. A binding post on the rear panel has been provided as an earth ground connection. Power supply switching (115V or 230V ac) is explained in Section 4. With the exception of slower reading rates and filter time outs, operation at 50 Hz is identical to that at 60 Hz.

2-14. The line fuse (.5A MDL Slow Blow) is located on the rear panel, near the heatsink. The current protection fuse (1.5A AGC) is located in the lower right-hand corner of the front panel.

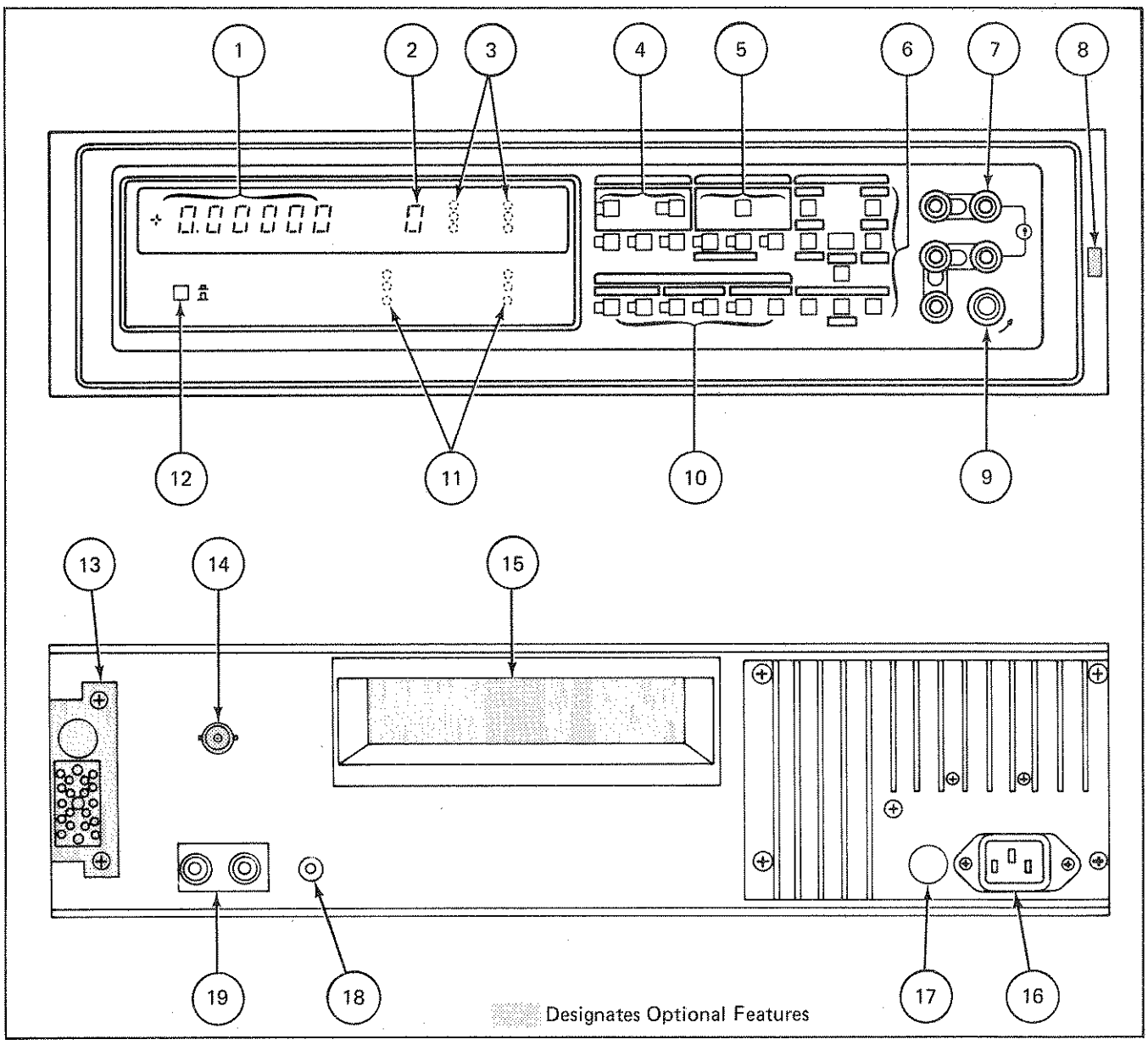


Figure 2-1. 8502A Controls and Indicators

Table 2-1. 8502A Controls and Indicators

REF. NO.	NAME	FUNCTION
1	Digit Display	Displays 5 1/2 digits with polarity and properly positioned decimal point. When instrument is in Hi Res mode, the exponent display will be used as an extra digit (for 6 1/2 digits).
2	Exponent Display	Displays polarity and value of exponent for engineering notation.
3	Range and Function Indicators	LED's illuminate to identify function and autoranging selection.
4	FUNCTION Controls	Push to select volts (VDC, VAC), current (A DC, A AC), or OHMS. Serve as dual function controls for numeric entries.

Table 2-1. 8502A Controls and Indicators (cont)

REF. NO.	NAME	FUNCTION
5	RANGE Controls	Manually shift range up or down. Enter high resolution mode. Select auto or manual ranging. Recall (HI, LO) peak or limit. Store (HI, LO) limit values. Serve as dual function controls for numeric entries.
6	MEMORY Controls	Toggle into/out of LIMITS, PEAK, CAL, OFFSET or SCALING. RECALL Memory values. Manual TRIGGER. STORE applied values, numerics. ENTER or clear (CE) numerics.
7	INPUT Terminals	SENSE INPUT HI and LO for volts, ohms. INPUT SOURCE HI and LO for amps, ohms. Guard Current protection fuse. GUARD.
8	(REAR INPUT IN)	Optional (−16)
9	Current Fuse	Use AGC 1.5A
10	MODIFIER Controls	RESET RESUME REMOTE EXT REF FILTER SAMPLE Numerics
11	Status Display	LED's light for: Slow filter Sample (flashes at reading rate) SCALING selected REMOTE selected OFFSET selected PEAK selected LED's flash if CAL or EXT REF selected
12	Power Switch	Push on/Push off
13	(Rear Input Connector and Fuse)	Optional connections for remote input and external reference terminals (−16, −17).
14	(External Trigger Input)	Optional (−08A)
15	(Interface Connectors and Switches)	Optional remote interface module accessible in this area (−05, −06, −07)
16	Power Connector	Three-prong connector accepting line cord with ground wire.
17	Line Fuse	Use MDL .5A (slow blow).
18	Chassis Ground	Binding post for ground interconnections.
19	External Reference Terminals	Apply external reference voltage. (40V max between HI and LO).

2-15. Display

2-16. DESCRIPTION

2-17. The 8502A's display consists of a digit readout, exponent, and LED annunciators for indication of instrument function and status. Specifically, these features provide:

1. 5 1/2 or 6 1/2 digit display with polarity, automatic reading and decimal placement.

2. Exponent display with polarity for readings in engineering notation. Serves as an extra digit of resolution in Hi Res and Cal modes.

3. Function and autoranging indicators light for function selected and for autoranging.

4. Status indicators give a constant illumination to signify selection of REMOTE, OFFSET, PEAK, SCALING, slow FILTER. Dual function LED's will flash to indicate selection of CAL or EXT REF. SAMPLE LED will flash at the reading rate selected (with more than 128 samples per reading, the LED will flash at the same rate to denote a reading in progress).

5. Power ON LED.

2-18. WARNING INFORMATION

2-19. The digit and exponent displays will provide warning indications and error codes.

1. "HHHHHH" will flash at the reading rate if the input voltage exceeds the full scale value for the range selected. Full scale values are included with the specifications in Section 1.

2. "H" will flash in the exponent display should an input voltage greater than 40V occur when in the Scaling, External Reference or Offset modes.

3. These flashing indications will not be seen when in the Cal mode.

NOTE

Flashing indicators in the digit or exponent display are a warning only; they have no effect on instrument operation.

4. Error codes will be provided in the digit and exponent displays when appropriate. Consult Table 2-2 for applicable meanings.

NOTE

Error codes will not be displayed in Cal mode. Random readings will then be the only indication of an invalid function or faulty module.

Table 2-2. Error Codes

CODES	FAULT
Error	System error – if this error message appears prior to the introductory messages at power initialization or reset, the problem is with the calibration memory module.
Error 0	VDC/Ohm Zero Error – either a VDC/Ohm Zero was attempted in a range other than 100 mV or 10 ohms, or an overrange was entered.
Error 1	Store during overload condition attempted.
Error 2	Filter module error – the module is faulty or not installed.
Error 3	DC Signal Conditioner error – the module is faulty or not installed.
Error 4	Ohms or Current error – excessive voltage applied to the selected module, shorting links not properly connected, or the selected module is faulty.
Error 5	R^2 A/D error – the recirculating remainder analog to digital converter module is faulty or not installed.
Error 6	Numeric display overflow error.
Error 7	External Reference error – the magnitude of one of the external reference inputs is greater than 20V dc.
Error 8	Controller error – the module is faulty or not installed.
Error 9	Function Selection error – the function module selected, other than dc volts, is faulty or not installed.
Error C	Invalid switch sequence during Recall or Store operations.

2-20. SPECIAL CONSIDERATIONS

2-21. Cal

2-22. Use of the Cal mode will significantly change normal display indications. As noted above, no warning indications will be displayed. Further, the exponent display will now serve as an extra digit of resolution (yielding 6 1/2 digit resolution).

2-23. Hi Res

2-24. The exponent display will be used as an extra digit of resolution in the High Resolution mode (not used in the 100 mV or 100 uA ranges). No exponent will be displayed.

Although not visible in Hi Res, the exponent remains in effect; care should be exercised when interpreting readings. To avoid confusion, remember that an exponent in the exponent display will always have its own polarity sign; a high resolution digit will not.

2-25. Input Terminals

2-26. TERMINAL INTERCONNECTIONS

2-27. For dc voltage measurements, both INPUT HI terminals may be left strapped together, The INPUT LO terminals may likewise remain strapped. For most measurements, it is sufficient to strap GUARD to INPUT LO. Refer to Figure 2-2, for recommended input terminal strapping.

CAUTION

The guard terminal should not be left disconnected. Instrument damage can occur if common mode voltage exceeds the LO to GUARD maximum voltage rating (127V).

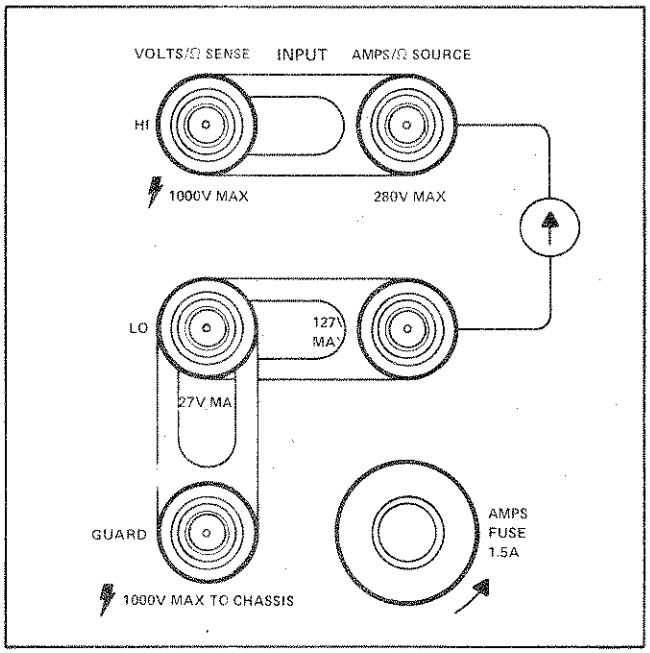


Figure 2-2. Front Panel Terminal Interconnections

2-28. GUARDING

2-29. Common mode voltages, resulting from currents and voltage drops between two points otherwise electrically common, may produce significant errors. Proper use of a floating, guarded voltmeter will minimize these errors and allow representative reading of normal mode voltages (actual source voltage and noise).

2-30. Correct use of the 8502A's guard terminal will both protect the instrument and provide more accurate readings. Since the LO to GUARD maximum voltage rating is 127V, the guard terminal should always be connected either to the INPUT LO terminal or to a point in the source circuit to be measured. For accurate readings, connect the guard to minimize common mode currents flowing through any resistance which helps determine the voltage being measured. See Figure 2-3, for suggested guard connections.

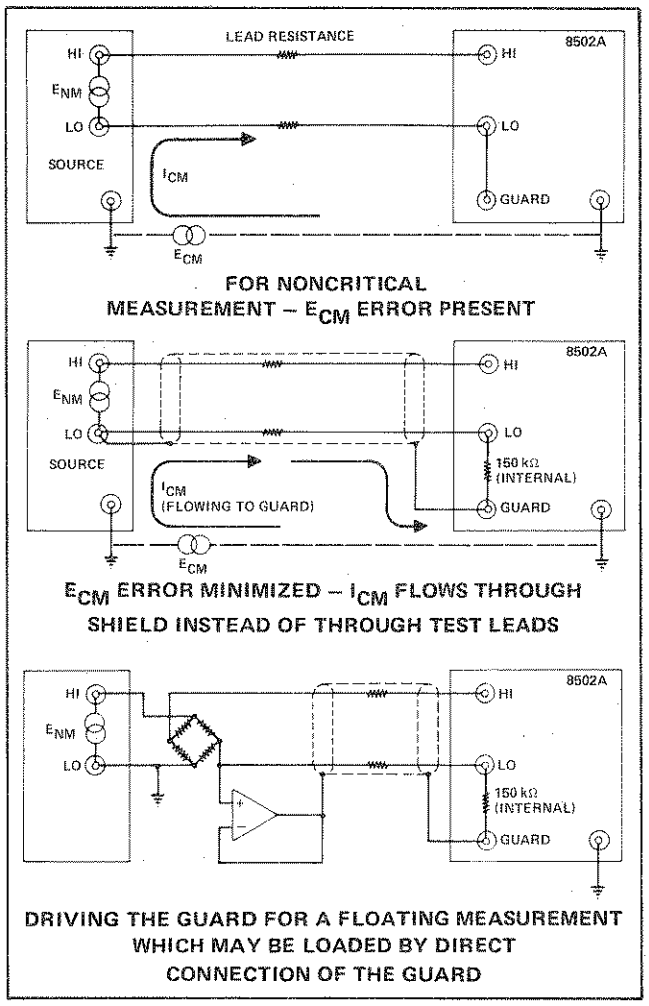


Figure 2-3. Guard Connections

2-31. Generally, guarding should be used in the following situations:

1. When long signal leads are used.
2. When signal source impedance is high.
3. When making measurements near high-level radiated noise, particularly at the power line frequency.
4. When making floating measurements.

NOTE

Errors due to thermal EMF's should be considered when making low level, high resolution measurements. Thermal EMF's (voltages produced by temperature differences between contacts of two dissimilar metals or by temperature gradients along a length of material) may cause differences in potential of several microvolts. Since the 8502A utilizes gold-plated input terminals, the use of low EMF, shielded cables with gold-plated spade lugs will minimize thermal EMF errors.

2-32. Front Panel Controls

2-33. Most front panel controls are momentary contact switches. If held in continuously, such switches will be read only one time. In addition, some of these switches will hold a particular reading in the 8502A's display for as long as they are held depressed. Front panel switches may have 1, 2, or 3 functions; switch sequencing will determine which function is in effect for multi-function switches. Refer to "OPERATING DIRECTIONS" later in this section for detailed front panel control procedures.

2-34. Function

2-35. The DC volts function is standard with this instrument; optional modules must be included for all other functions. Complete information for any options included with your 8502A can be found in Section 6 of this manual. If a function is selected for which the appropriate module is not installed, "Error 9" will appear in the display.

2-36. Range

2-37. DC volts can be measured on five successive ranges from 100 mV to 1000V. Respective resolutions vary from 1 uV to 1 mV. Input impedance on the 100V and 1000V ranges is 10 Mohms. On the lower three ranges it is greater than 10,000 Mohms. Overrange capabilities, DC voltage accuracies, and overload protection conditions are detailed in Section 1 of this manual.

2-38. Modifiers

2-39. FILTER

2-40. The 8502A has five filter modes.

1. F – slow filter, no time out – FILTER LED on.
2. F0 – fast filter, no time out.
3. F1 – filter bypass.
4. F2 – slow filter, with time out (550 msec, settling time) – FILTER LED on.
5. F3 – fast filter, with time out (50 msec, settling time).

("Fast" and "slow" refer to the respective filter's settling time.)

2-41. The slow filter will provide better line frequency rejection; the fast filter discriminates against higher frequency and harmonically related line noise. Time outs are always inserted before the first reading is taken in a newly selected function or range. With F2 or F3 selected, time outs will always be inserted before each subsequent reading in that function or range.

2-42. SAMPLE

2-43. Samples taken in the 8502A can be synchronous or asynchronous to the line frequency. Line frequency noise rejection can be increased by averaging more samples per displayed reading (refer to NOISE REJECTION specifications in Table 1-3 of this manual.) Provision is therefore made to change the number of samples taken for each reading (display update). Setting the samples per reading will yield a specific reading time. Additional time per reading will be necessary whenever memory operations (Offset, Scaling, etc.) are involved. Ohms measurements will also require more time due to the multiple readings involved.

2-44. For example, if rate 7 is selected, 128 samples will be taken and averaged per reading. With no memory operations involved, digitizing time for a dc volts reading will therefore take 533 ms. Sample rate designations (such as 7) are actually the number of samples per reading expressed as exponents of 2; rate $7 = 2^7 = 128$ samples per reading.

2-45. EXTERNAL REFERENCE

2-46. An external reference dc voltage can be used to divide the inputs in any function. A true ratio measurement is then computed by the Controller.

$$\text{Reading} = \frac{\text{Input}}{\text{dc Ext. Ref. Input}}$$

2-47. A pair of external reference terminals will be found either separately on the rear panel or together in the optional rear input connector.

1. The applied external reference voltage may be a maximum of ±20V at either external reference HI or LO or 40V between HI and LO, with respect to SENSE LO (or to Ohms Guard in the rear input connector).

2. The minimum voltage applicable to the external reference terminals is the greater of either ±100 uV, or a value found with the following formula:

$$V_{min} = \frac{\pm \ |V_{in}|}{10^9}$$

3. The resistance between either EXT REF terminal and INPUT LO should be less than 20 Kohms. Normally, EXT REF LO will be tied to INPUT LO.

2-48. REMOTE

2-49. If an optional remote interface is installed, the REMOTE switch may be used to toggle into or out of remote control. With the IEEE (Option –05) Interface installed, only toggling out of remote control is permitted from the front panel. When in remote control, only the remote switch and the power switch will have any effect on the instrument's operation. A reset caused by power interruption will return the instrument to local control.

2-50. Remote control does not affect analog inputs on the High Quality Bus. With Rear Input (Option –17) or Switchable Front - Rear Inputs (Option –16), separate Sense Hi and Lo, Source Hi and Lo, Guard, Ohms Guard, and External Reference connections must be made remotely.

2-51. Memory

2-52. The 8502A provides considerable versatility in measurement manipulations through both front panel and remote programming. Displayed numbers are computed from measured data according to the following general equation, where:

y = the displayed number

m = the scaling factor or external reference

x = the actual input (averaged samples)

b = the offset factor (subtracted)

Thus:

$$\left[y = \frac{x}{m} - b\right]$$

2-53. Either displayed values or numeric sequences may be stored as memory factors.

NOTE

Storing a value in memory does not select a mathematical operation. The operation must be selected separately before or after the value is stored.

2-54. LIMITS

2-55. Any currently displayed value may be stored as a limit value. With such values stored as references, the 8502A (toggled into the Limits mode) will yield a display of:

1. HI if the reading is greater than the high limit.

2. PASS if the reading is less than or equal to the high limit and greater than or equal to the low limit.

3. LO if the reading is less than the low limit.

NOTE

HI, LO, and PASS describe the normally displayed reading, with all math operations completed, relative to the limit values.

2-56. Only one set of limits may be stored at a time. A function change will exit the Limits mode but retain stored values.

2-57. PEAK

2-58. Highest and lowest values displayed in any series of measurements may be stored when in the Peak mode. Toggle in and out of this mode by depressing the PEAK switch. Peak values will be retained after the mode is deactivated but lost should the instrument be reset or the mode reselected.

2-59. CALIBRATION MODE

2-60. The CAL switch will be found on the front panel behind a small plastic cover which pulls out and hinges down. Sliding the switch down places the 8502A in the Calibration mode. This mode is designed primarily to be used with the Calibration Memory (Option –04). When this module is installed and the instrument is in the Calibration mode, correction factors can be stored at the decade point for each range and function. Refer to Section 6 of this manual for complete Calibration Memory procedures.

2-61. If the Calibration Memory is installed, inadvertent use of the STORE switch will store the last reading as a calibration factor and erase calibration factors for the function and range in use at the time. To correct this possible mistake without a calibration standard, disconnect the input, short the input terminals, and press STORE again.

2-62. Whether or not the Calibration Memory module is installed, entry into the Calibration mode (CAL LED flashes) necessitates consideration of the following alterations to the 8502A's display:

1. The exponent is replaced with an extra digit of resolution.

2. Error codes are disabled. Only spurious readings will now denote selection of an invalid function.

3. The overrange indication is disabled.

NOTE

When changing from one function to another, or upon entering the Cal mode, memory modes will be deactivated. Stored values will be retained. Use of RESET or interruption of power to the 8502A will erase memory entries.

2-63. OFFSET

2-64. The Offset mode can be used to automatically subtract a number from the measured input and display the result. The subtracted offset number may be:

1. Any currently displayed value.

2. A programmed numeric entry (ranging from $+10^9$ to -10^9).

2-65. The displayed reading in Offset mode will exhibit no increase in digit resolution. Only one offset factor at a time can be stored. A function change will deactivate Offset mode; the stored value will be retained. A flashing H will appear in the exponent display should more than 40V appear between the input terminals when in Offset mode.

2-66. SCALING

2-67. The Scaling mode may be used to automatically divide a measured input by a programmed number or by an applied value. This feature essentially provides the ability to program an external reference without standard external reference limitations in range. In fact, scaling values may range from $+10^9$ to $+10^{-9}$ and from -10^9 to -10^{-9}. A scaling factor of 0 is not allowed. Scaled readings will contain 3 significant digits if the original reading had 3 or less significant digits. For more than 3 significant digits in the original reading, the scaled reading will display the same number of significant digits. Only one scaling factor may be stored at a time. A function change will deactivate the Scaling mode but retain the stored factor.

NOTE

If the 8502A is in both Scaling and Offset, the scaling factor will be applied first; the scaled displayed values will then be offset.

2-68. ZEROING

2-69. There are two methods of zeroing the 8502A. Either method may be used in the 100 mV range or the 10 ohm range.

2-70. VDC/Ohms Zero

2-71. Correction for internal dc drift can be made by applying a good quality, low thermal short between HI and LO terminals (not between test leads). If necessary, repeat this operation once the instrument has warmed up. Only dc volts zero factors may be recalled.

2-72. Zeroing with OFFSET

2-73. After zeroing for internal drift, separate dc volts and 2-wire ohms measurement corrections can be made by shorting the test leads and storing the reading as an offset factor.

2-74. Systems Use of the 8502A

2-75. The availability of optional interface modules makes the 8502A adaptable to a large variety of digital systems. Operating and programming instructions related to remote operation are included with the appropriate optional module. Overall information on remote interfacing can be found in Fluke Application Bulletin –25 "System Use of the Fluke Model 8500A", Specific information about the IEEE interface (–05 Option) may be found in Fluke Application Bulletin –36. Application Bulletin –37 "Unique Measurements Using the 8500 Series Digital Voltmeter" will also be useful for both local and systems use of the 8502A.

2-76. OPERATING DIRECTIONS

2-77. Initial Settings

2-78. Upon applying power to the 8502A, the display will read:

"HI – 2.0.Y"

("Y" will be the number of the software version employed in your instrument.) Then:

"CXXXXX"

("X" will be identifying numbers for installed options.)

The instrument will now assume the following status:

1. V DC function

2. 1000V range

3. Slow reading rate (7)

4. Fast filter (F0)

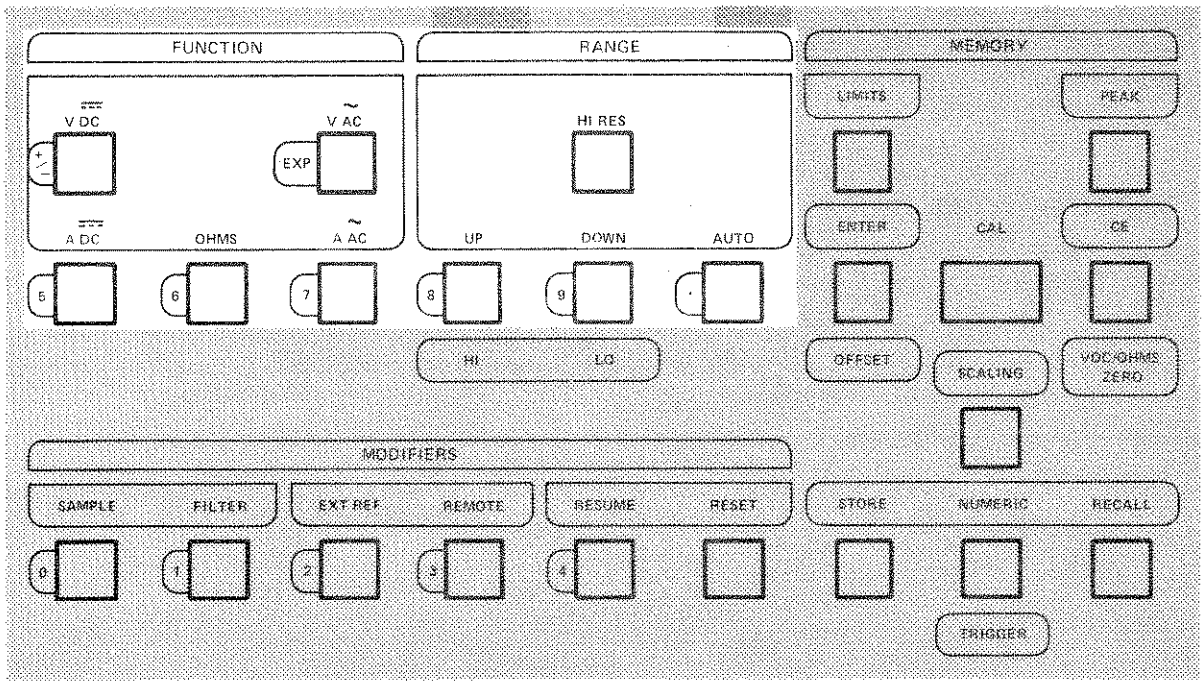
5. Offset – off and zeroed
Scaling – off and set to 1
Peaks – off and set to 0
Ext Ref – off
Trigger – Auto
VDC/Ohmx Aero – zeroed
Remote – out, in local.

2-79. Allow a 1 hour warm-up to insure rated accuracy.

2-80. Front Panel Control Usage

2-81. Figures 2-4, 2-5, 2-6, and 2-7 will describe 8502A front panel control usage. When initially setting these controls, use the following grouping sequence:

FUNCTION → RANGE → MODIFIERS → MEMORY



FUNCTION

Depress the switch for the desired function. The 8502A will assume autoranging (AUTO LED on) and retain any modifier (sample, filter, etc.) or memory (scaling, offset, etc.) mode already in use. If a function is selected for which the module is either faulty or not installed, Error 9 will appear in the display. Press RESET or select another function to clear this error indication. Otherwise, the appropriate function LED will come on when one of the following functions is selected:

1. DC VOLTS (V DC) – Standard, 5 ranges.
2. AC VOLTS (V AC) – Optional, 4 ranges.
3. DC CURRENT (A DC) – Optional, 5 ranges.
4. AC CURRENT (A AC) – Optional, 5 ranges.
5. Resistance (OHMS) – Optional , 8 ranges.

Figure 2-4. Function and Range

RANGE

Range switching in the 8502A can be either manual or automatic.

☐ UP ☐

Advances 8502A to the next higher range with each application. UP will have no effect at the top of the range. If the 8502A is in autoranging, application of UP will both shift to manual range and change the range.

☐ DOWN ☐

Steps 8502A to the next lower range each time it is depressed. DOWN will have no effect at the bottom of the range.

☐ AUTO ☐

Toggles the 8502A into/out of the Autoranging mode.

☐ HIGH RESOLUTION ☐

Depress the HI RES switch to enter this mode (not available in 100 mV DC or 100 mA range). Depress it a second time to exit the mode. Don't forget that, although the exponent is not displayed, it does remain in effect.

Figure 2-4. Function and Range (cont)

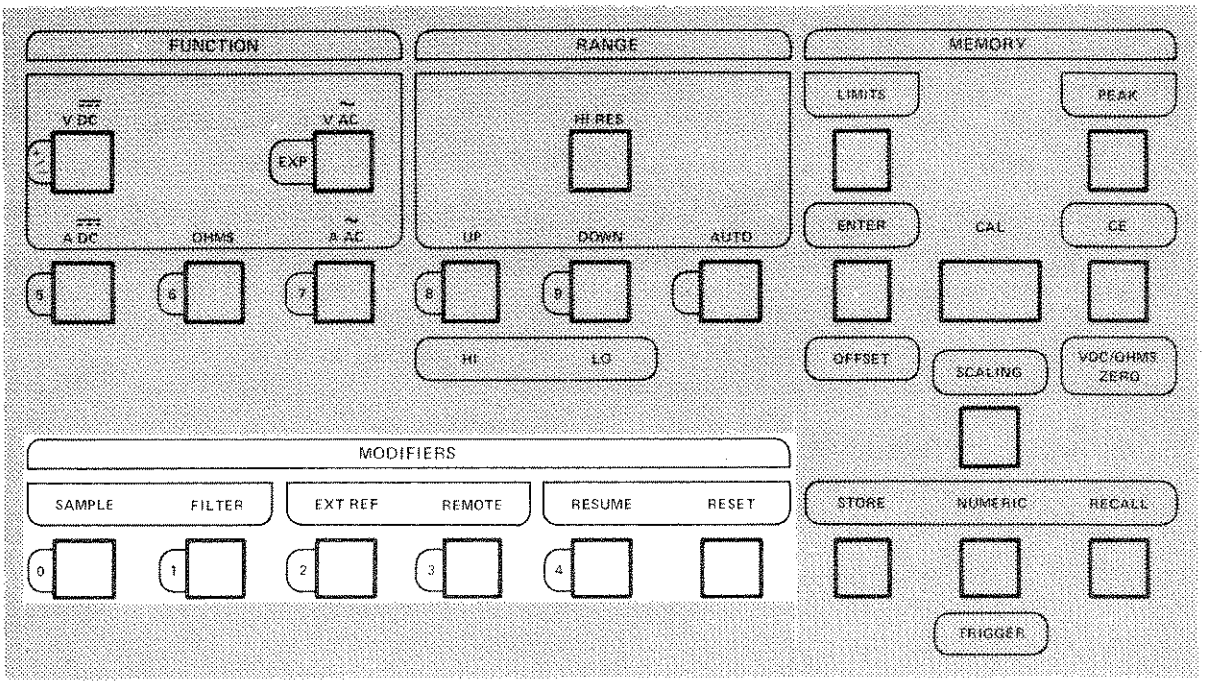


Figure 2-5. Modifiers

☐ SAMPLE ☐

1. Press SAMPLE to toggle between samples/reading rates 5 and 7.

2. Alternately, any rate between 0 and 17 may be programmed from the front panel. Press:

   STORE → NUMERIC → SAMPLE → (rate number) → ENTER

   The new rate will go into effect as soon as ENTER is pressed.

3. To display the samples/reading rate, press:

   RECALL → SAMPLE

   The rate will be displayed as long as SAMPLE is held depressed.

4. The SAMPLE LED will flash at the samples/reading rate selected. With more than 128 samples/reading (rate 7) there will be no distinguishable rate difference from the LED's indications at rate 7.

☐ FILTER ☐

1. Press FILTER to toggle between filter modes F and F0. The FILTER LED will come on for F (slow filter).

2. Use the following switches to select filter modes F1, F2, or F3:

   STORE → NUMERIC → FILTER → (1, 2, or 3) → ENTER

3. Display the filter mode in effect by pressing:

   RECALL → FILTER

   The mode will be displayed as long as FILTER is held depressed.

4. If modes F1 or F3 are in effect, subsequent use of FILTER will toggle the 8502A back to mode F. If mode F2 is in effect, pressing FILTER will toggle back to mode F0.

☐ EXTERNAL REFERENCE ☐

1. Press EXT REF to enter the External Reference mode (EXT REF LED will flash). The external reference voltage applied at the rear panel terminals will be displayed as long as EXT REF is held depressed. Release of the switch enters the 8502A into the External Reference mode.

2. For proper external reference operation; the resistance between SENSE LO on the front panel and external reference HI or LO on the rear panel must be less than 20 Kohms. Apply a direct connection between these two points to insure correct operation.

☐ REMOTE ☐

1. Use REMOTE to toggle between local and remote operation with either the RS 232 (Option –06) or or the Parallel (Option –07) Interface installed.

2. Use REMOTE to toggle into local only if in remote with the IEEE (Option –05) installed.

Figure 2-5. Modifiers (cont)

☐ RESUME ☐

Use RESUME to exit Manual or External Triggering modes.

☐ RESET ☐

Use RESET to put the 8502A back to the power on status:

1. V DC function.
2. 1000V range.
3. F0 filter.
4. 7 sample.
5. No other modifiers or memory modes in effect.
6. Memory entries lost. (Calibration Memory (Option –04) entries will not be lost.)

Figure 2-5. Modifiers (cont)

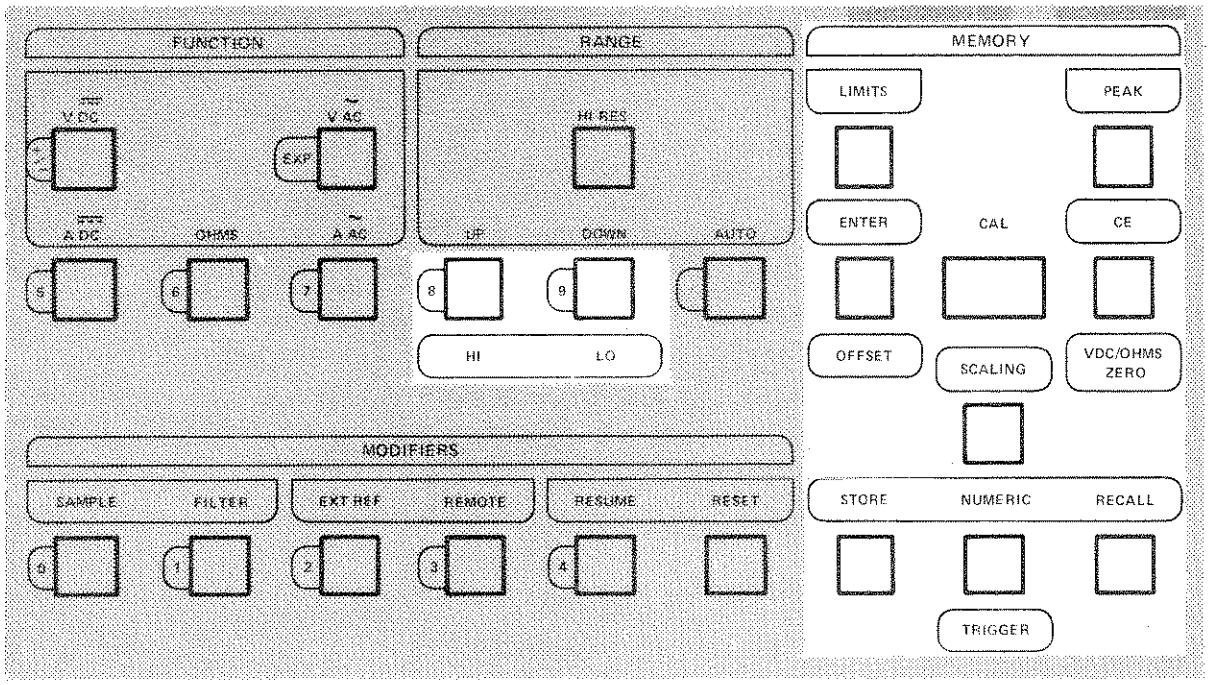


Figure 2-6. Memory

DISPLAY INDICATIONS WHEN PROGRAMMING THE 8502A

The display will respond to memory programming as in the following example:

PRESS	DISPLAY RESPONDS
STORE	"?"
NUMERIC	YES?
OFFSET	Go
(numbers)	1, 2, 3 . . .
ENTER	Return to normal display.

☐ LIMITS ☐

1. Select the Limit mode by depressing the LIMIT switch. A display of HI, LO, or PASS will indicate that the mode has been entered. Depress LIMIT a second time to exit the mode.

2. To store any displayed value as a limit value; use the following sequence:

   STORE → HI

   STORE → LO

   The value being entered will be displayed as long as HI or LO are held depressed. Release of either switch will enter the value as the respective limit. LIMIT must be separately depressed before or after entering values to enter the Limit mode.

3. To enter numeric values as limit values, press:

   STORE → NUMERIC → HI or LO → (value numbers) → ENTER

   LIMIT must be depressed to enter the mode.

4. To display the stored limits, press:

   RECALL → HI or LO → LIMIT

   The respective value will be displayed as long as LIMIT is held depressed.

☐ PEAK ☐

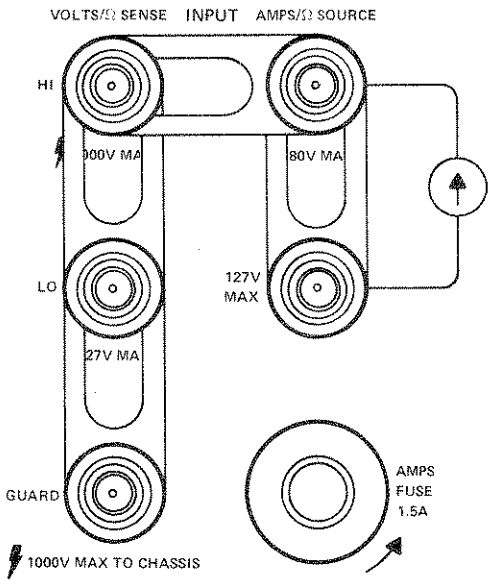
1. Press PEAK to toggle into or out of the Peak mode (PEAK LED will come on).

2. To display the readings recorded in this mode, use the following sequence:

   RECALL → HI or LO → PEAK

Figure 2-6. Memory (cont)

☐ VDC/OHM ZERO ☐



1. Correct for internal drift by shorting the input terminals as illustrated. Use a good quality, low thermal short. The instrument must be in the 100 mV or 10 ohm range.

Now use the switches:

STORE → VDC/OHM ZERO

The value will be displayed as long as VDC/OHM ZERO is held depressed. The display will be zeroed once VDC/OHM ZERO is released.

2. To display the stored zero correction (for dc volts only), press:

RECALL → VDC/OHM ZERO

The value will be displayed as long as VDC/OHM ZERO is held depressed.

☐ OFFSET ☐

1. Enter the Offset mode by pressing OFFSET (OFFSET LED will come on). Exit this mode by again depressing OFFSET.

2. Store any currently displayed value with the following procedure:

STORE → OFFSET

3. To enter a programmed numeric value as an offset, use the following procedure:

STORE → NUMERIC → OFFSET → (numbers) → ENTER

4. To use OFFSET as a zeroing feature, first perform VDC/OHM ZERO. Then, short test leads used in dc volts or 2-wire ohms measurements. Press:

STORE → OFFSET

The value will be displayed as long as OFFSET is held depressed. Push OFFSET a second time to enter Offset mode.

Figure 2-6. Memory (cont)

☐ SCALING ☐

1. Press SCALING to enter this mode (SCALING LED will come on). Pressing the switch a second time will exit the mode.

2. Store any currently displayed value as a scaling factor by pressing:

   STORE → SCALING

   Read the value as long as SCALING is held depressed. Enter the mode by again depressing SCALING.

3. Enter a programmed numeric as a scaling factor by pressing:

   STORE → NUMERIC → SCALING → (numbers) → ENTER

   Press SCALING to enter the mode.

4. Display a stored scaling factor by pressing:

   RECALL → SCALING

☐ CAL ☐

1. Enter the Cal mode by sliding the CAL switch down (the CAL LED will flash). This switch will be found behind a small plastic cover which pulls out and hinges down. Use a small screwdriver or equivalent to slide the switch.

2. To enter calibration factors for each range and function, the optional Calibration Memory must be installed. Refer to Section 6 for applicable operating instructions.

☐ TRIGGER ☐

1. Press TRIGGER to activate both manual triggering mode and external triggering operation (–08A Option installed). The 8502A will now accept either:

   a. A manually triggered reading with each subsequent depression of TRIGGER, or

   b. An external trigger applied through the rear panel connector (part of Option –08A).

   Manual triggering from the front panel will take precedence if a simultaneous external trigger is received.

2. Exit manual/external triggering by pressing RESUME.

3. When you press a switch it is acted upon immediately, and the reading is aborted. Thus, if the instrument is in manual trigger and a switch is pressed during the reading, the 8502A will halt. It will then be necessary to press TRIGGER again to take the reading.

☐ CE ☐

Use this switch to clear a numeric entry prior to entry into memory.

Figure 2-6. Memory (cont)

☐ ENTER ☐

Use this switch to enter a numeric into memory.

☐ STORE ☐

Use to initiate a numeric entry sequence.

☐ RECALL ☐

Use to initiate recall and display of stored values.

CORRECTING ENTRY ERRORS

There are a number of methods to correct memory entry errors. Choices include staying in the entry sequence, exiting the sequence and retaining memory, or exiting the sequence and losing memory.

1. Stay in sequence: CE – erases only numbers before entry.

2. Exit sequence, retain memory: Generate any invalid switch sequence that will result in "Error C",

3. Exit sequence, lose memory: RESET or power interruption causes 8502A to assume V DC 1000V, F0, sample 7, blank memory (optional Calibration Memory not affected).

Figure 2-6. Memory (cont)

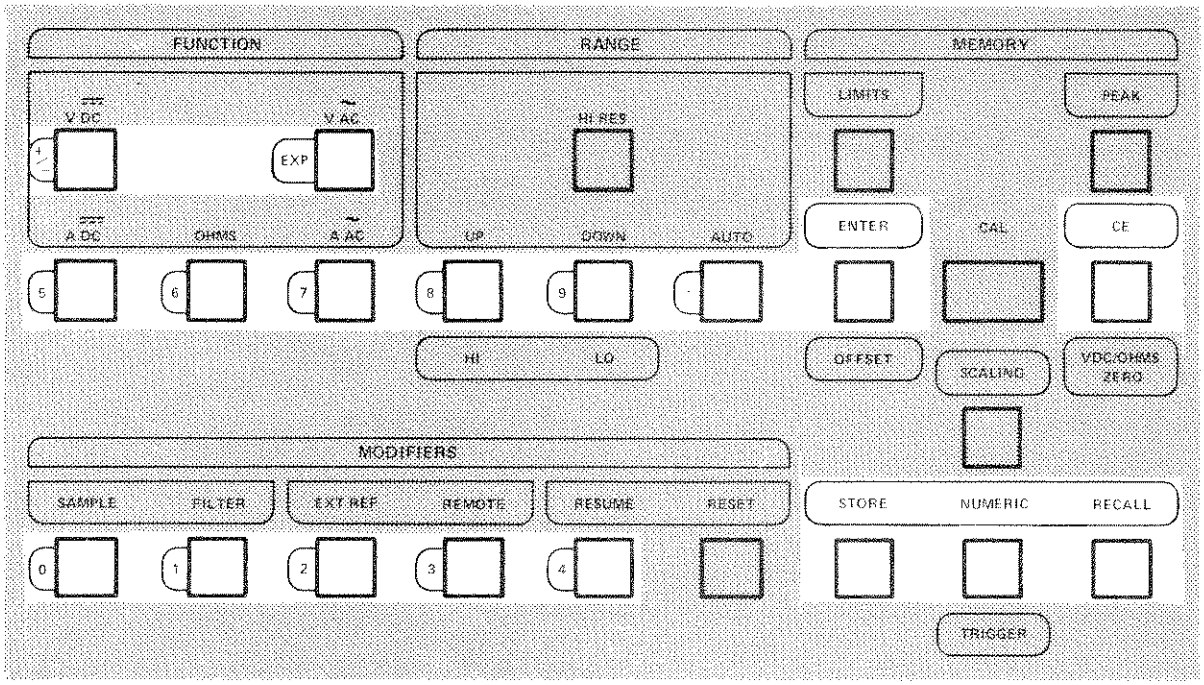


Figure 2-7. Numerics

☐ STORE ☐

Use the numeric sequence whenever entering a value (as in Offset) or a particular mode (as in Filter) into the 8502A's memory. Use the following procedural steps:

1. Initiate the numeric entry. Press:

STORE	("?" appears in display)
NUMERIC	(YES? appears in display)

2. Select the desired use for the numeric entry. Press:

OFFSET	(Go appears in display)
(SCALING FILTER, SAMPLE, HI or LO for LIMITS).	

3. Select the desired numbers. Numbers will appear in the display from left to right as they are entered.

NOTE: Press CE if an error is made during the following number, polarity and exponent entry steps. The 8502A will then display Go. Start entries again from this point.

   a. For Filter, enter the mode number (–, 0, 1, 2, or 3).

   b. For Sample, enter the exponent of 2 for samples averaged in each reading (0 through 17).

   c. For Offset, enter the number(s) for the offset factor.

   d. For Scaling, enter the number(s) for the scaling factor.

   e. For Limits (HI, LO), enter the numeric values desired.

4. To change the polarity of the numeric entry, press:

   +/–

5. To add an exponent to the numeric entry, press:

   EXP

6. To change polarity for the exponent, now press:

   +/–

7. To finalize storing of the entry and exit the numeric sequence, press:

   ENTER

8. The value is now stored. For Filter or Sample entries, the value is now also in effect. For Offset, Scaling or Limits, the value will not become effective until the appropriate mode is selected.

Figure 2-7. Numerics (cont)

2-82. Measurement Instructions

2-83. DC VOLTAGE (V DC)

2-84. Use the following procedure when measuring dc volts:

1. Select the VDC function.
2. The 8502A will go to autoranging. If desired, select manual ranging and one of the five available ranges (1000V, 100V, 10V, 1V, or 100 mV).
3. Perform DC Zero, if needed (100 mV range only).
4. Select desired modifiers and memory operations.
5. Connect the dc voltage to the HI and LO SENSE INPUT terminals.
6. A dc voltage reading should now appear in the display.

2-85. DC ZERO

2-86. For dc zeroing, use the following steps:

1. Select the V DC function and either autoranging or the 100 mV manual range.
2. Place a good quality, low thermal short across the HI and LO INPUT terminals.
3. Depress the STORE switch. "?" will appear in the display.
4. Depress the VDC/OHMS ZERO switch; value applied to input terminals will now be displayed as long as the switch is held depressed.
5. Release of the switch will activate V DC/Ohms Zero mode, applying the value read in step 4 as a zero reference for subsequent readings.

2-87. AC VOLTAGE (V AC)

2-88. Use the following procedure when measuring ac volts:

1. An AC Converter module must be installed (Option –01, or –09A).
2. Select the VAC function.
3. The 8502A will go to autoranging; manual ranging can be selected if necessary. There are four available ranges: 1000V, 100V, 10V, 1V.
4. Perform DC ZERO, if necessary. No additional zero procedure is needed for ac voltage.
5. Select desired modifiers and memory operations.
6. The slow filter (FILTER LED illuminated) must be selected for full accuracy below 400 Hz.
7. Connect the ac voltage to the HI and LO SENSE INPUT terminals.
8. The ac voltage should be read in the display.

2-89. AC VOLTAGE ON A DC LEVEL (V DC and V AC)

2-90. Use the following procecure when measuring ac and dc voltage:

1. The RMS AC Converter module must be installed.
2. Depress both V DC and V AC awitches simultaneously.
3. The 8502A will go to autoranging; manual ranging can be selected if necessary. There are four available ranges: 1000V, 100V, 10V or 1V.
4. Select desired modifiers and memory operations.
5. Connect the unknown voltage to the HI and LO SENSE INPUT terminals. The reading displayed will be the rms value of the two voltages combined.

2-91. DC CURRENT (A DC)

2-92. Use the following procedure when measuring dc current:

1. The Current Shunts module must be installed.
2. Select the A DC function.
3. The 8502A will go to autoranging; manual ranging can also be utilized to select one of five available ranges (100 uA, 1 mA, 10 mA, 100 mA, or 1A).
4. Select desired modifiers and memory operations.
5. Connect dc current to HI and LO INPUT SOURCE terminals.

2-93. AC CURRENT (A AC)

2-94. Use the following procedure when measuring ac current:

1. The Current Shunts module must be installed.

2. Select the A AC function.

3. Follow steps 3-5 listed for DC Current measurements.

2-95. OHMS

2-96. Use the following procedure for resistance measurements:

1. The Ohms Converter module must be installed.

2. Select the OHMS function.

3. The 8502A will go to autoranging; manual ranging can be selected if necessary. There are eight resistance ranges available: 100M, 10M, 1M, 100K, 10K, 1K, 100 and 10 ohms.

4. If necessary, perform the ohms zero procedure described below (10 ohm range only).

5. Select desired modifiers and memory operations.

6. Connect the unknown resistance to the HI and LO INPUT terminals (see Section 6 for 2-wire and 4-wire connection methods).

2-97. OHMS ZERO

2-98. For ohms zeroing, use the following steps:

1. The Ohms Converter module must be installed.

2. Select the Ohms function.

3. Select the 10 ohms range.

4. Short input terminals as described in zeroing instructions.

5. Depress the STORE switch; "?" will appear in the display.

6. Depress the V DC/OHMS ZERO switch; the value of residual resistance will be displayed for as long as the switch is held depressed.

7. Release of the zero switch will activate the Ohms Zero mode.

2-99. APPLICATIONS

2-100. The applications presented in Table 2-3 presuppose an initial power on or reset instrument status, i.e.,

1. V DC function.

2. 1000V range.

3. Sample – 7.

4. Filter – F0.

5. No stored values (excepting the Calibration Memory).

Table 2-3. Applications

STORING A DISPLAYED VALUE	
STORE →	OFFSET VDC/OHM ZERO SCALING HI LO
APPLICATION 1	
REQUIREMENT:	Monitor the stability of a power supply in terms of its deviation in volts from a present output of +5.03V.
METHOD:	Store the present output as an offset. Press: STORE → OFFSET → OFFSET Initial use of OFFSET places the displayed value into memory (value will be viewed as long as switch is held depressed). The second use of OFFSET places the instrument in Offset mode. The display will now read only the deviation from +5.03V.

Table 2-3. Applications (cont)

APPLICATION 2

REQUIREMENT: Monitor the stability of a power supply as a decimal ratio to its present reading of −20.08V. DC zeroing appears to be necessary.

METHOD: Perform V DC Zeroing for internal drift. Apply low thermal short between INPUT HI and LO (at the terminals). Press:

STORE → VDC/OHMS ZERO

The value stored will be displayed as long as VDC/OHMS ZERO is held depressed. Release of the switch will activate the Zero mode. Revise terminal interconnections for dc volts measurements. Connect the dc voltage.

Apply power supply reading of −20.08V as a scaling factor. Press:

STORE → SCALING → SCALING

Initial use of SCALING places the displayed value (which is seen as long as the switch is held depressed) into memory. The second use of SCALING places the 8502A into Scaling mode.

Display will now yield the ratio of subsequent readings to the scaling factor, e.g., an input of 22.08V yields a ratio of:

$$\frac{22.088}{20.08} = 1{:}1$$

STORING A NUMERIC ENTRY

STORE → NUMERIC → { OFFSET, SCALING, HI, LO → (value number) → ENTER; FILTER → (−, 0, 1, 2, 3) → ENTER; SAMPLE → (0 thru 17) → ENTER }

APPLICATION 3

REQUIREMENT: Determine which of a group of power supplies have a tolerance of 15V ± 100 mV.

METHOD: Set high and low limits. Press:

STORE → NUMERIC → HI → 1 → 5 → . → 1 → ENTER

STORE → NUMERIC → LO → 1 → 4 → . → 9 → ENTER

Select LIMITS. The 8502A will now display "HI", "LO", or "PASS" for each power supply.

Table 2-3. Applications (cont)

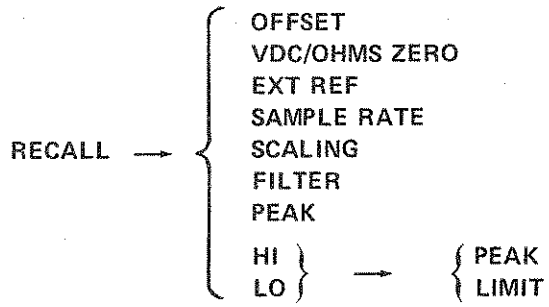
APPLICATION 4	
REQUIREMENT:	For a group of 20V power supplies, determine the deviation in volts.
METHOD:	Offset the displayed reading by 20. Press: STORE → NUMERIC → OFFSET → 2 → 0 → ENTER Select OFFSET. Any value displayed now will equal the deviation from 20V.

APPLICATION 5	
REQUIREMENT:	Display the input error voltage for an operational amplifier by measuring the dc output error. Gain = 2.6847×10^4.
METHOD:	Divide the measured dc output error by a scaling factor (the op amp gain). Press: STORE → NUMERIC → SCALING → 2 → → 6 → 8 → 4 7 → EXP → 4 → ENTER Select SCALING. The 8502A will now divide the measured input by the gain of the op amp and display the input error voltage.

APPLICATION 6	
REQUIREMENT:	Make a series of measurements in a noisy environment. Speed of measurement is not important. Display only the deviation in volts.
METHOD:	Allow for extra settling between readings. Press: STORE → NUMERIC → FILTER → 3 → ENTER Increase digital filtering (average more samples per reading). Press: STORE → NUMERIC → SAMPLE → 9 → ENTER Offset by the nominal output (e.g., 15V). Press: STORE → NUMERIC → OFFSET → 1 → 5 → ENTER Select OFFSET

Table 2-3. Applications (cont)

RECALLING



APPLICATION 7

REQUIREMENT: Determine the highest and lowest readings encountered in measuring a group of 28V power supplies.

METHOD: Press PEAK to record measurement extremes. When required measurements are complete, use the following sequence to recall high and low values. Press:

RECALL → LO → PEAK

RECALL → HI → PEAK

(Hold PEAK in to read the recorded values.)

Section 3
Theory of Operation

3-1. INTRODUCTION

3-2. This section of the manual describes the theory of operation for the 8502A mainframe, which includes the modules necessary for DC Volts and DC Ratio measurements. Block Diagram descriptions give an overview of the operation of the modules and an explanation of the bus structure. Circuit Analyses give a more detailed description of the circuitry. Optional modules are described in Sect. 6.

3-3. BLOCK DIAGRAM DESCRIPTION

3-4. Bus Structure

3-5. The 8502A is constructed with a bus architecture similar to a computer. Figure 3-1 is an overall block diagram of the instrument with optional modules drawn in dashed lines. Figure 3-2 is a block diagram illustrating signal flow. A microprocessor-based controller module controls information flow on the three buses. The controller sets up each of the analog modules for a measurement by addressing the modules as memory locations. An unguarded digital interbus is used to connect the controller to the front panel and to digital option modules such as the calibration memory and a remote I/O (input/output) interface.

3-6. The unguarded digital bus consists of the following lines:

1. Address/Control (IC) lines –7.
2. Bidirectional data (ID) lines –8.
3. Real time (RT) lines –7.
4. Handshake lines (INT–interrupt, ACK–acknowledge, INA–interrupt acknowledge).
5. Power Supply lines.

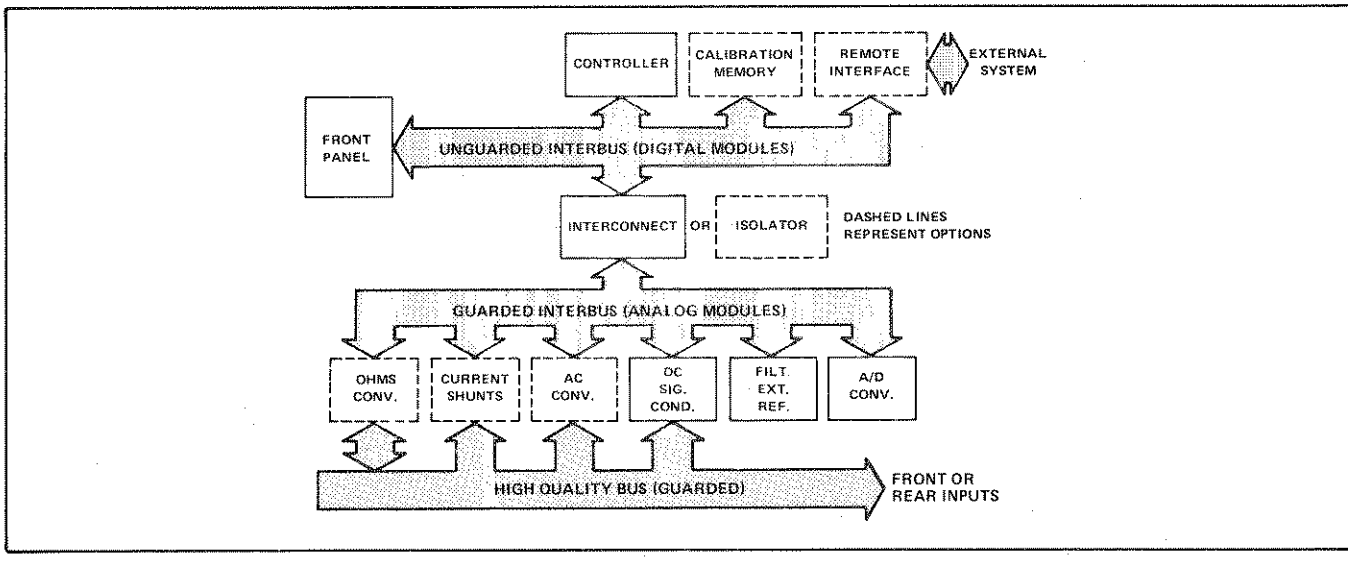


Figure 3-1. 8502A Block Diagram

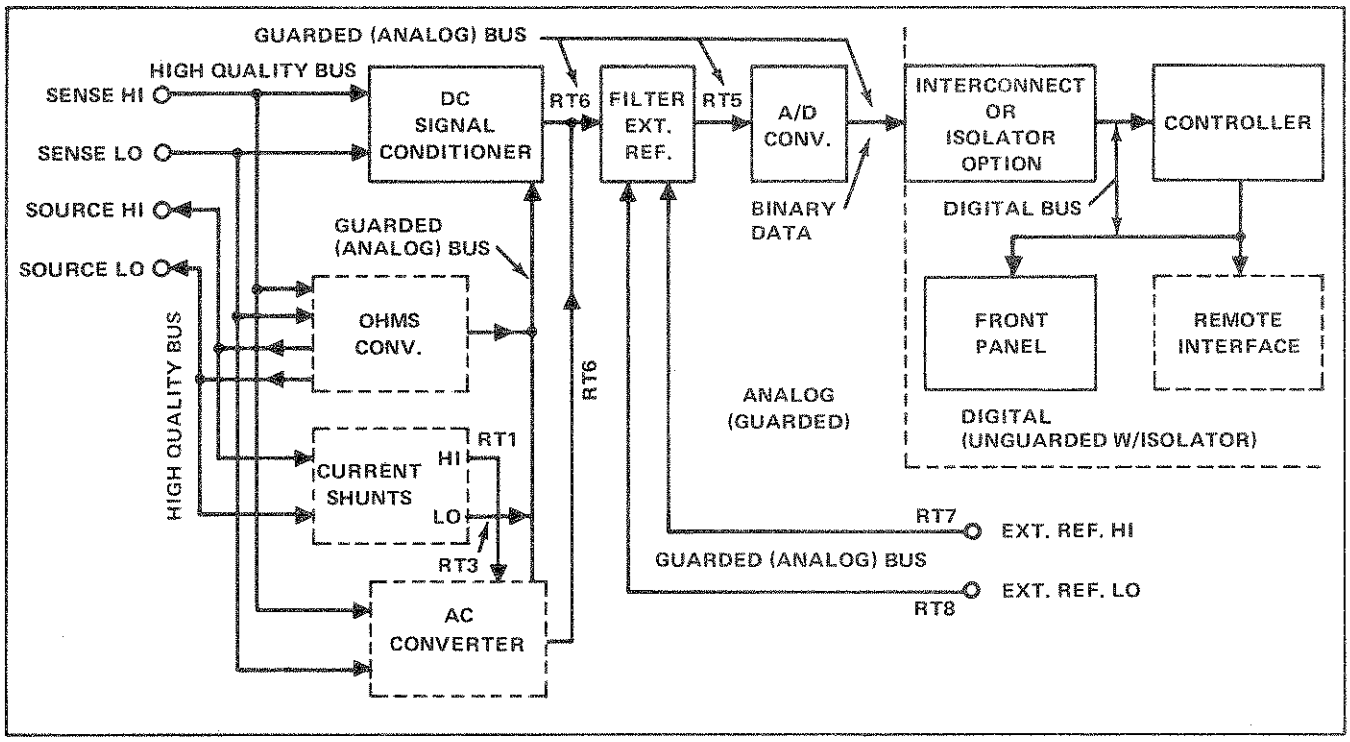


Figure 3-2. 8502A Analog Signal Flow

3-7. The guarded bus connects the controller to the analog modules through the Bus Interconnect Board or through the optional Isolator module; the Isolator must replace the Interconnect Board if an optional remote interface is installed. The guarded bus consists of the following lines:

1. Address/Control (IC) lines –7.

2. Bidirectional data (ID) lines –8.

3. Real time lines –9.

4. Handshake line (ACK) –1.

5. Power Supply lines.

3-8. The address, handshake, and data lines of the two buses serve the same functions. The real time and power supply lines may have differing functions. For example, the RT lines in the unguarded bus are unused except for RT5 (frequency reference). The RT lines in the guarded bus form an analog bus which carries all the conditioned and converted analog signals between the analog modules. The external reference input lines are part of the analog bus (RT7 and RT8). Logic supply lines (Vcc and Vss) will be different in the two busses if an isolator option is installed. In the guarded bus, Vcc and Vss are always –15V and –20V with respect to analog common. In the unguarded bus with an interconnect pcb installed Vcc and Vss are diode coupled to the guarded bus. But with the isolator option installed, Vcc and Vss are isolated from analog common.

3-9. The high quality bus consists of lines connecting the input switch (Sense HI and LO, source HI and LO, Guard, Ohms Guard) to the signal conditioning and converting modules (AC converters, Ohms converter, etc.). Ohms guard is only available through the rear inputs.

3-10. Controller

3-11. Under the direction of the software program, the controller addresses and sets up each of the modules necessary to perform a function. Two types of addresses are used: direct and indirect. An indirect address requires a previous direct address to set up the indirect address response logic. Data transfers are accomplished with a handshake between the address (IC) lines and the acknowledge (ACK) line. When the controller addresses a module, it places data on the data (ID) lines or receives data from the addressed module. The addressed module must respond with an ACK signal signifying that it is receiving or sending data.

3-12. The controller directs the R^2 A/D converter in taking a sample and receives the sample data from the converter. The controller stores range and function information for application to the sample data. Using the arithmetic capability of the microprocessor, the software processes the data to arrive at a binary 2's complement number which represents the polarity and value of the measurement. This number is made available to an optional remote interface either as is or after further processing to ASCII code. The number is further processed by the controller for application to the front panel display in a seven segment LED format.

3-13. The software program consists of two parallel processes. A background process (Figure 3-3) is responsible for interrupt driven activities such as updating the display digits and directing the A/D converter in taking a sample. The foreground process (Figure 3-4) is responsible for the measurement cycle including accumulating data from the background process and performing required calculations.

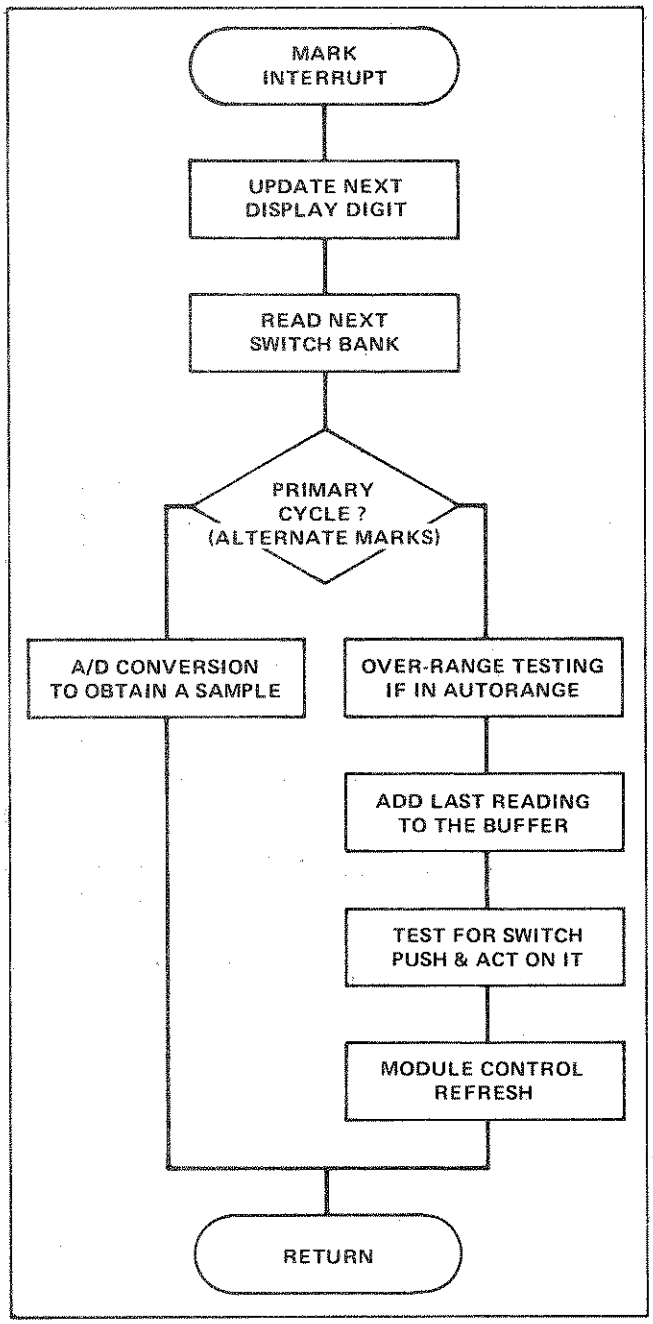


Figure 3-3. Background Software Process

3-14. The controller is structured around the Intel 8080 microprocessor. Figure 3-5 is a block diagram of the controller module. Hardware control functions have been minimized by careful software design. Sequences of events are timed from two sources. Basic operations of the microprocessor are run from a 1.7 MHz clock. The other source is generated by shaped line frequency pulses, which are applied to a phase-locked loop. The phase-locked loop multiplies the line frequency by eight. This signal is used to generate mark interrupts which time the background process.

3-15. Software for the 8502A is stored in five ROM's. These read only memories are mounted on a "piggy-back" board, which is connected to the main controller pcb at the socket for U25. Four RAMs (random access memory) are used for temporary storage of data by the microprocessor. Data lines (DB0–DB7) are used for bidirectional data flow. Address lines (A0–A15) determine the source or storage location of data. Since other modules of the 8502A system are addressed as memory locations, address and data I/O controls are used for access to the external bus structure.

3-16. Interrupts are used to divert the microprocessor from the main program to service other routines. Interrupts are synchronized to an appropriate time in the microprocessor cycle through interrupt control, where assigned priorities vector module identity data onto the data bus. Module identity data words direct the microprocessor to the memory location containing the next instruction. Two interrupts are internally generated: ACK INT and MARK INT (priorities one and six respectively). ACK INT is generated when an acknowledge signal is not returned. MARK INT is used to synchronize A/D samples and display digit updates to the line frequency.

3-17. An interrupt may be externally requested by pulling the INT line low. When the microprocessor is ready to accept the interrupt, the interrupt acknowledge (INA) signal is generated. The requesting module must respond with an ACK and a data bit (on ID1–ID4) which is used as a priority vector by INT CONTROL.

3-18. Two types of resets may occur: software and hardware. Software resets are a result of front panel or remote requests. Hardware resets occur at power up or power down. Line frequency pulses from RT5 are sensed by the reset logic. At power up the reset signal assures that the microprocessor will start from program location zero. At power down the reset signal assures that the controller will not call up wrong modules.

3-19. The microprocessor control logic is responsible for latching up a status word at the beginning of each instruction cycle and for telling the microprocessor when to enter and exit wait states. Microprocessor sequences are divided into machine states (one clock period, 588 nsec), machine cycles (from three to five states) and instruction cycles (from one to five machine cycles). Status words are used to control and synchronize data I/O, memory read/write, and some of the interrupt control signals. The microprocessor must be instructed to enter a wait state after addressing an external module and after being interrupted to allow the external module time to respond.

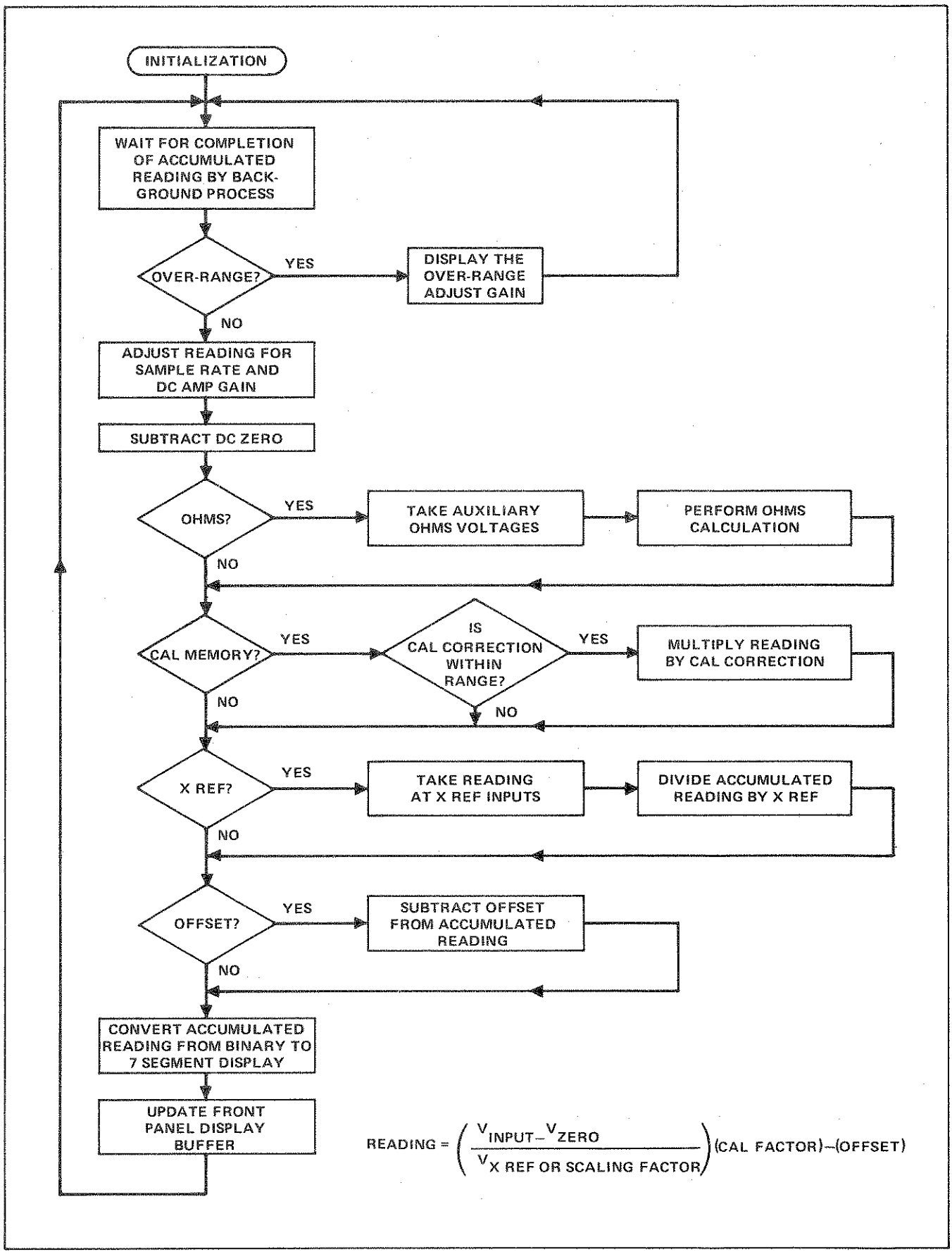


Figure 3-4. Foreground Software Process

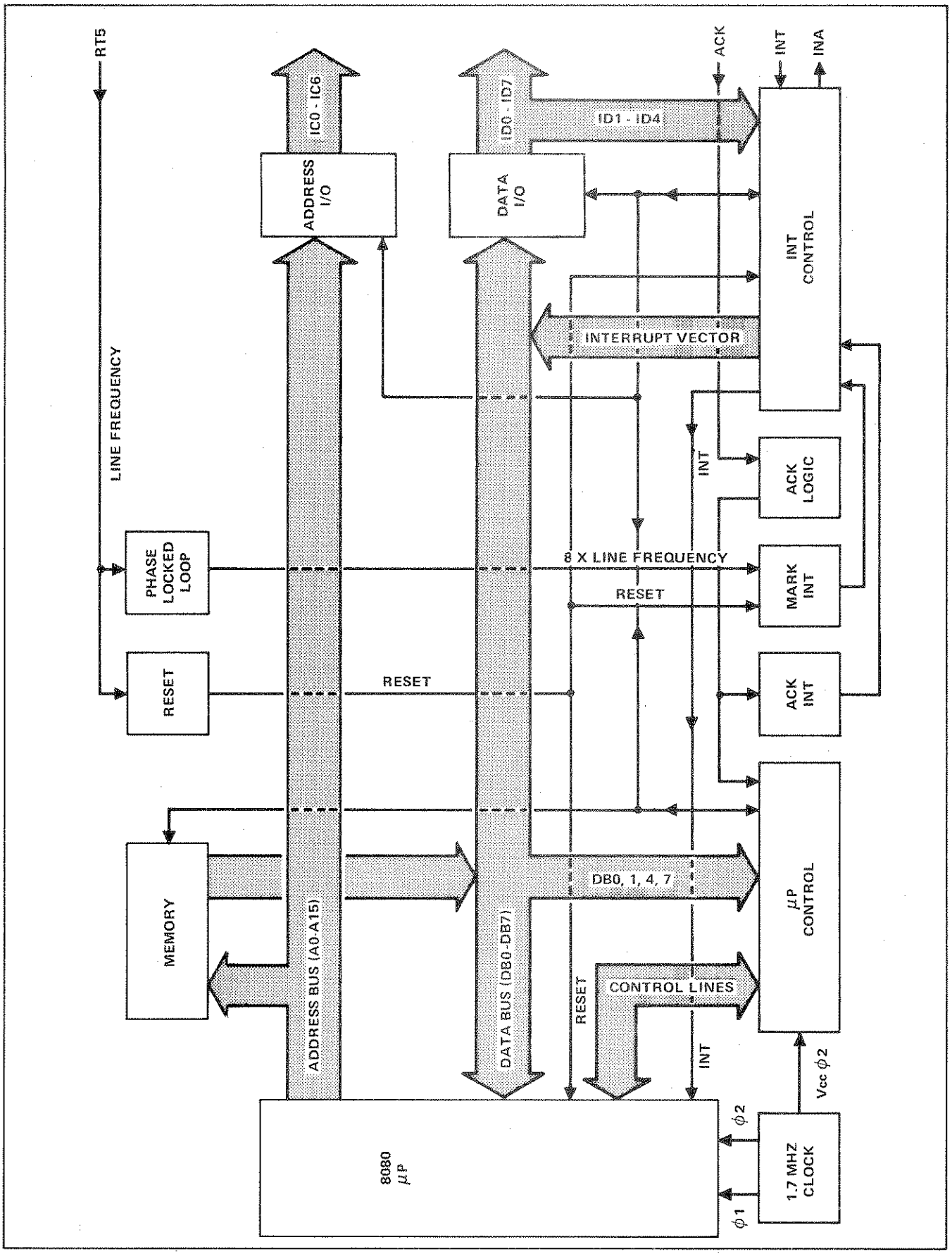


Figure 3-5. Controller Block Diagram

3-20. Front Panel

3-21. The front panel serves as an interface between the operator and the 8502A controller. The display is multiplexed by the controller by means of addressing the front panel for each digit. One direct address, two indirect addresses, and the accompanying data determine which digit or annunciator and which segments will light. An indirect address requires a previous, valid direct address to set up the indirect response. Another direct address enables the switch matrix to be read to determine if any function changes are desired. The cycle of updating each digit and annunciator and reading the switch matrix requires approximately 28 msec and is a continual cycle. Input terminals, J1–J5, are physically located on the front panel but have no electrical interaction with the front panel.

3-22. DC Signal Conditioner

3-23. DC signals from either the input terminals or optional signal conditioners (Ohms or Current Shunts) are routed through the DC Signal Conditioner to be brought within the range of the A/D Converter (± 20V). Figure 3-6 is a block diagram of the DC Signal Conditioner. For ease in arithmetic manipulations in the microprocessor, all gains and attenuations in the 8502A are powers of eight. Gain or attenuation factors are selected by the microprocessor addressing the module. Data from the data bus is latched into the control circuitry and used to select relays in the attenuator and switches in the amplifier feedback circuit. The combination of the attenuator and feedback-controlled amplifier give gain or attenuation factors of one, eight, or sixty-four.

3-24. Active Filter

3-25. The purpose of the Active Filter module is to multiplex dc signals to the A/D Converter and to switch analog filters into the signal conditioner inputs. Figure 3-7 is a block diagram of the Filter/External Reference module. Five filter modes may be selected from the front panel. For external reference measurements, the signal

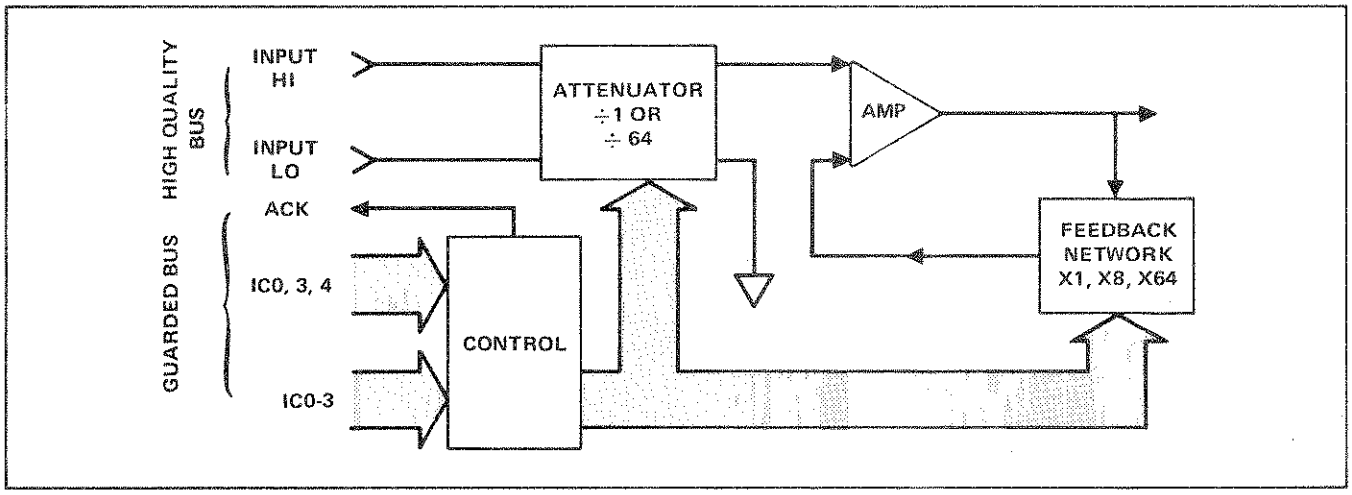


Figure 3-6. DC Signal Conditioner Block Diagram

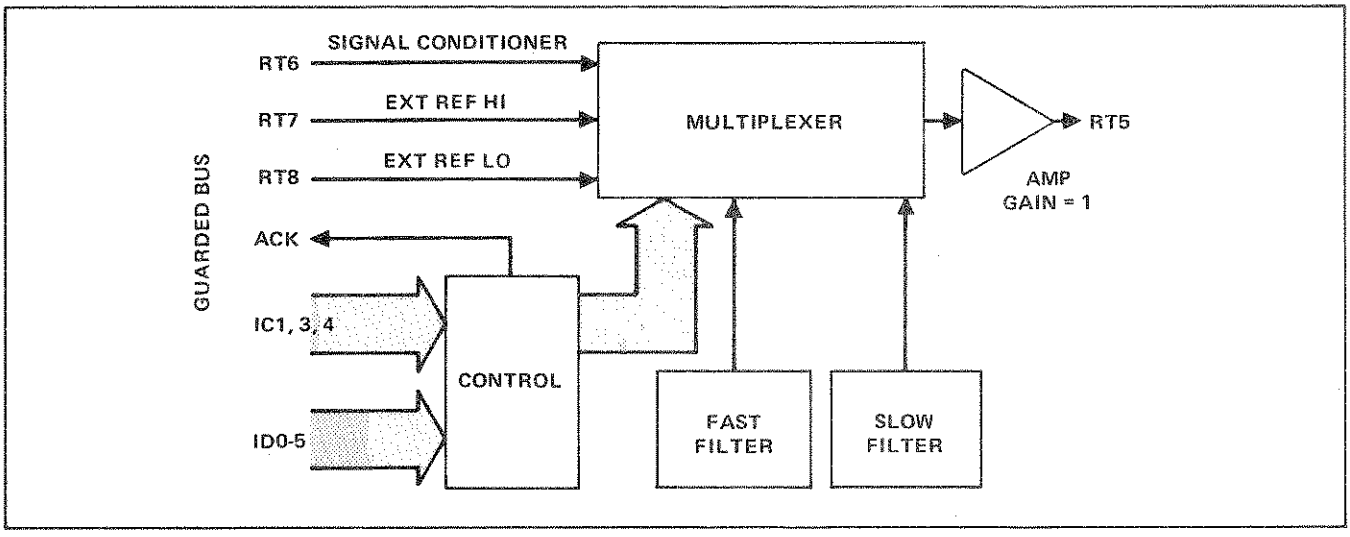


Figure 3-7. Active Filter Block Diagram

conditioner input, the External Reference HI input and the External Reference LO input are multiplexed to the A/D Converter. Samples are taken of each input and arithmetically manipulated by the Controller to arrive at a reading. Outputs from the optional AC converter modules are applied to the Active Filter module, bypassing the DC Signal Conditioner.

3-26. Fast R^2 A/D Converter

3-27. The Fast R^2 A/D Converter employs Fluke's patented recirculating remainder (R^2) technique for converting a dc input signal into a binary, bit-serial data stream. The R^2 technique has been modified for microprocessor control. Obtaining a sample is a five-step process. Each step consists of a decision period of five decisions and a subtraction period. Set-up of the converter, decisions, and reset are initialized by the Controller addressing the A/D Converter. Figure 3-8 is a block diagram of the R^2 A/D Converter.

3-28. During the first step, the input signal is applied to the Summing Node. The polarity of the input is detected and the resulting bit of information is transmitted to the Controller. On the basis of the returned polarity, the A/D module selects which reference polarity is required: positive for negative inputs, negative for positive inputs. The first of five precision currents is switched into the Summing Node and a polarity bit returned. If the polarity is changed, the first current is switched off. If not, it is left on. Then the next current is switched into the Summing Node and another polarity bit returned. Another decision is made and so on until all five currents have been switched into the Summing Node and five decisions have been made. This completes the first decision period. The five precision currents are related by powers of two. The fifth current has a resolution of thirty-two.

3-29. Following the decision period is a subtraction period. Feedback through the Remainder Storage nulls whatever remainder was left after the five currents have been switched into the summing node. The remainder is amplified by 16 in the Remainder Amp and is stored on a capacitor in Remainder Storage. This completes the first step. The input is now switched out of the Summing Node and the amplified remainder switched in for the next step. There are two remainder channels in Remainder Storage and they are alternated in the four subsequent steps. Since the fifth current has a resolution of thirty-two and the Remainder Amp has a gain of 16, the first bit of a step has the same significance as the last bit of the previous step.

3-30. Of the five steps required to complete a sample, the first uses the input signal for decision and subtraction periods. The four subsequent steps alternate remainder channels to use the amplified remainder of the preceding step for decision and subtraction periods. Polarity bits

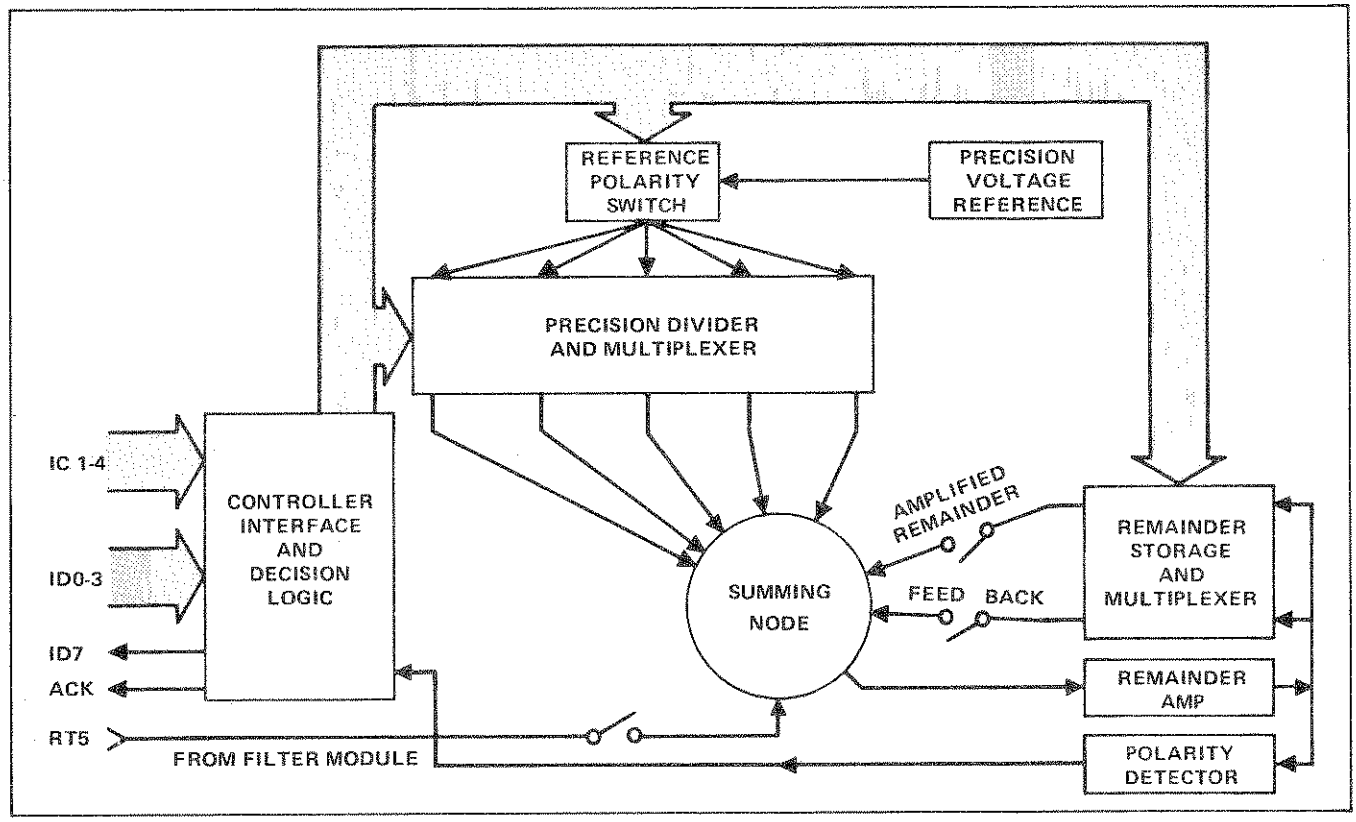


Figure 3-8. R^2 A/D Converter Block Diagram

returned at each decision are accumulated by the Controller and assembled into a 24-bit word describing the polarity and magnitude of the input.

3-31. CIRCUIT ANALYSIS

3-32. Introduction

3-33. Detailed circuit descriptions for each module in the standard 8502A mainframe will be presented in the following paragraphs. Optional modules are covered in Section 6. Block Diagram Description should be read first to get an understanding of the overall functioning of the instrument. Simplified schematic diagrams are located in Section 8 (Section 6 for optional modules). Table 3-1 is a list of mnemonic definitions used in the Controller schematic.

3-34. Controller

3-35. TIMING

3-36. The 8080 microprocessor requires two 12V clock inputs whose phase relationship must fall within certain limits (Figure 3-9). The period of the $\phi 1$ clock (588 nsec) governs the duration of a machine state (3 to 5 states required for a machine cycle, 1 to 5 machine cycles required for an instruction cycle). A 1.7 MHz crystal oscillator is RC coupled through buffers and gates to provide the two-phase clock signal. R1 controls the positioning of the $\phi 1$ clock pulse (with respect to time) during the $\overline{\phi 2}$ pulse. The $\phi 2$ clock pulse is inverted and translated to 5 volt TTL levels for other timing functions in the control circuitry.

3-37. Shaped line pulses are applied to a phase-locked loop (U26) which runs at 8 times the line frequency 480 Hz for 60 Hz line, 400 Hz for 50 Hz line). The output of U26 is divided by 8 (U34) and applied to a phase comparator (U26). Line synchronization is achieved using the output of the phase-locked loop to time the internal interrupt, MARK INT.

3-38. ADDRESS and DATA BUSSES

3-39. Sixteen address lines are used for addressing memory locations and external modules. Refer to the Controller schematic in Section 8. Internal scratch pad memory locations use A0-A7, with A8, 9, 11, 12, 13 decoded as a RAM chip select. Internal ROM locations use A0-A10, A11, 12, 13 decoded as a ROM chip select. ROM/RAM select uses A14 for RAM (high for RAM). External addresses use A8-A14 with A15 used as external/internal select (high for external). These address lines are inverted when driving the IC lines on the Interbus. The data bus is eight lines (DB0-7) connected directly to memory and to the external data bus (ID0-7) through tristate I/O buffers.

Table 3-1. Mnemonic Definitions

ACK	— acknowledge
ACK LAT	— acknowledge late
AR	— analog return
DB	— data bus
DBIN	— data bus input signal (from μP)
DLD ACK	— delayed ACK
EN INT	— enable interrupt
HLDA	— hold acknowledge
IB ADX	— interbus address
IBIN	— interbus input signal
IC	— interbus control
ID	— interbus data
IINT	— internal interrupt
INA	— interrupt acknowledge (from controller)
INT	— interrupt
INTA	— Interrupt acknowledge (status word from μP)
INTE	— interrupt enable (from μP)
MEM RD	— memory read
MS ADDR BYTE	— memory select address byte
$\phi 1$	— clock pulse
$\phi 2$	— clock pulse
ϕLL	— phase-locked loop
RAM	— random access memory
ROM	— read only memory
RRDY	— reset ready
RST	— reset
RT	— real time
R/$\overline{W}$	— read/$\overline{\text{write}}$
μP	— microprocessor
VA	— analog supply voltage
V_{CC} $\phi 2$	— 5V clock pulse
V_{DD} $\phi 2$	— 12V clock pulse
SRDY	— set ready
SYN IINT	— synchronized internal interrupt
TTL PU	— TTL pull-up
WO	— write out
WR	— write

3-40. RESET

3-41. Shaped line frequency pulses are applied to U36 and U34 to provide a reset on power up or power down (Figure 3-10). U36 is a retriggerable one-shot multivibrator which is cleared on power up by Delayed Vcc. Clearing U36 sets U35 to the Reset condition. After the clear on

U36 is removed (Delayed Vcc high), U34 clocks U35 out of the reset condition on the eighth line pulse. At power down, U36 changes state at a time determined by R18 and C22, setting U35 to the reset state.

3-42. STATUS LATCH

3-43. During the first state of every machine cycle, the microprocessor sends a status word out on the data bus. This is at the same time and duration as the SYNC output. SYNC $\overline{\phi 2}$ clocks the status word into a hex "D" latch, U18. Outputs from U18 (Figure 3-11) are used in various portions of the control circuitry.

3-44. WAIT LOGIC

3-45. When the microprocessor addresses an external module (A15 high) or is interrupted, the WAIT logic causes the microprocessor to enter a wait state by pulling the ready (RDY) line low (Figure 3-12). Set Ready (SRDY), normally high, is pulled low to exit the wait state. Reset ready (RRDY), normally low, goes high to enter the wait state. For an external address, A15 TTL is high; therefore RRDY will go high at SYNC TTL (derived from the microprocessor). For interrupts, the interrupt enable (INTE) signal is inverted for application to U8. INTE enables INT and is removed before INT falls low (due to an RC delay in the INT CONTROL circuit) so the INT and INTE are high long enough to clock U1 for a wait signal.

3-46. Three possible combinations will cause the microprocessor to exit a wait state. If an ACK signal is missing, ACK INT TTL will pull $\overline{\text{SRDY}}$ low. For external addresses, and external interrupts, A15 + INTA and ACK LAT will pull $\overline{\text{SRDY}}$ low. For internal interrupts SYN IINT and

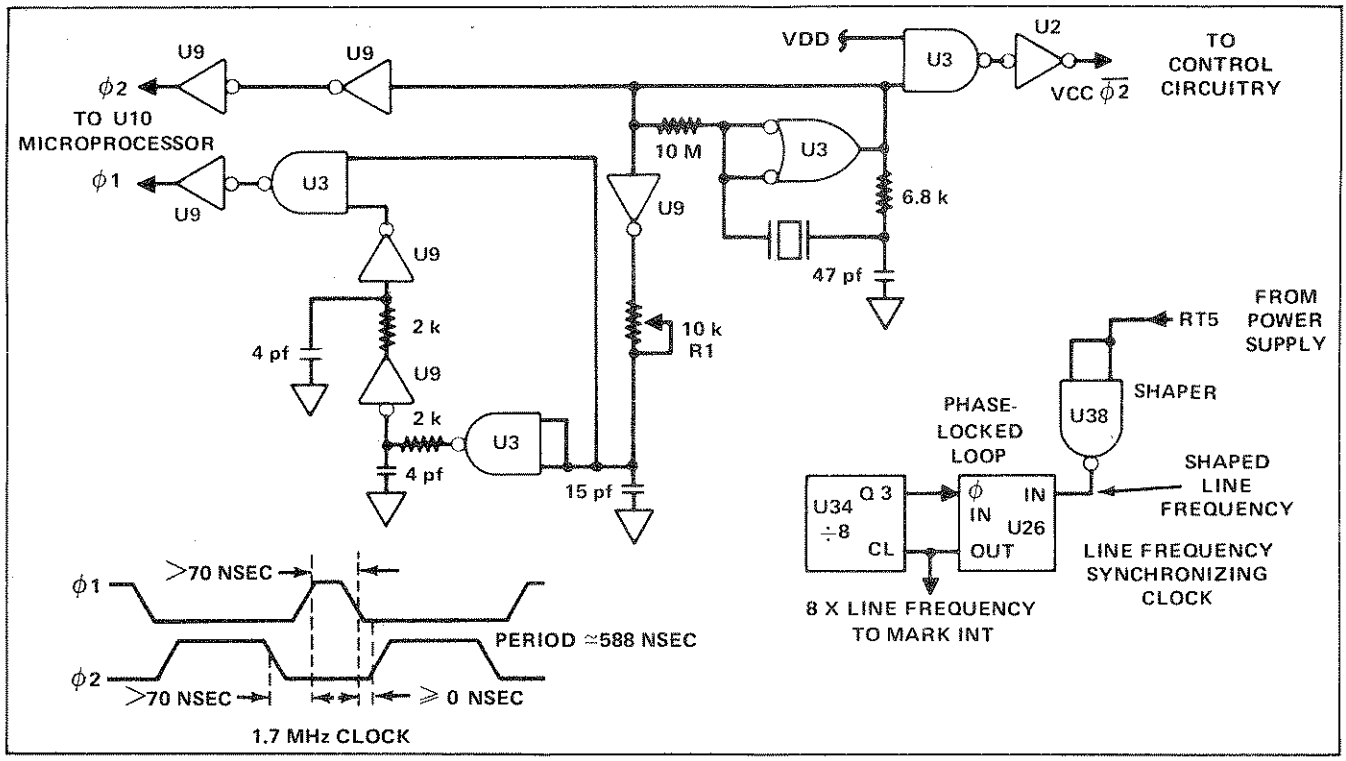


Figure 3-9. Timing Circuits

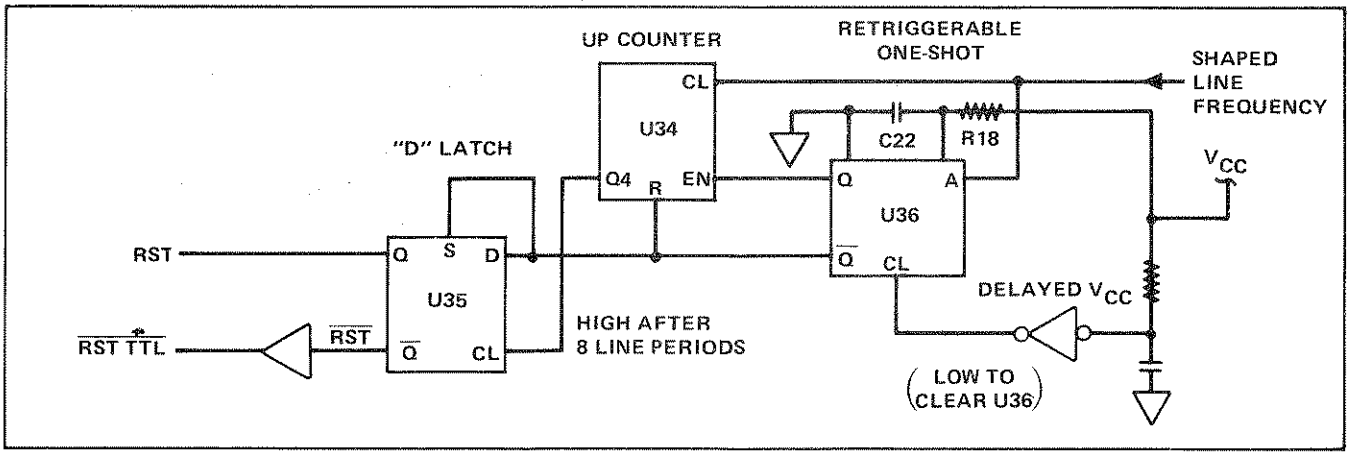


Figure 3-10. Reset Logic

INTA remove the wait state limiting the wait time to a single machine state.

3-47. ACK LOGIC

3-48. When a module is addressed by the Controller, or enabled for interrupt identification by INA from the Controller, it must return an ACK (high) signal. Refer to Figure 3-13. Either INTA (for interrupts) or A15 (for external addresses) together with the delayed ACK signal produce $\overline{\text{DLD ACK}}$ for U38. $\overline{\text{DLD ACK}}$ resets the ACK interrupt logic, which is timing the wait for ACK, and produces the ACK LAT signal through U15 and U27. RRDY must be low to get ACK LAT. This synchronizes ACK LAT to the SYNC TTL signal. ACK LAT (or $\overline{\text{ACK INT TTL}}$ if an ACK is missing) causes the microprocessor to exit the wait state.

3-49. INTERUPTS

3-50. Two internal interrupts and four possible external interrupts are applied to the interrupt (INT) control logic (Figure 3-13). A low on OR gate U17 places a high on NAND gate U38. When INTE is high from the microprocessor (during the last state of an instruction cycle), U38 outputs a low through an RC delay network to U32. U32 inverts the signal and places a high on the INT line to interrupt the microprocessor. The microprocessor drops INTE low, then puts out an interrupt acknowledge (INTA) as a status word which is latched up in the Status Latch, U18. Then the microprocessor enters a wait state until the interrupt and its priority are identified through INT VECTOR, U28 (Controller schematic, Section 8).

3-51. Internal interrupts are ACK INT and MARK INT (Figure 3-14). ACK INT logic consists of a retriggerable

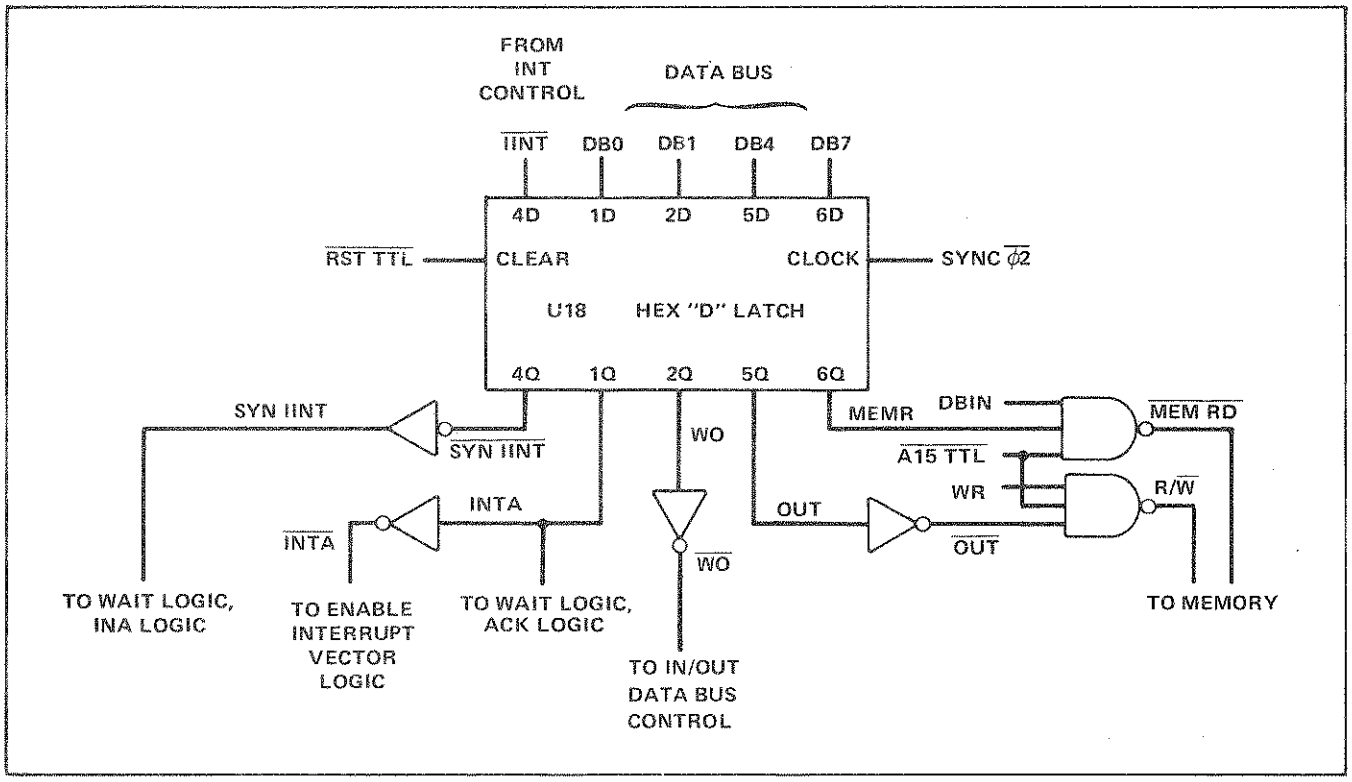


Figure 3-11. Status Latch

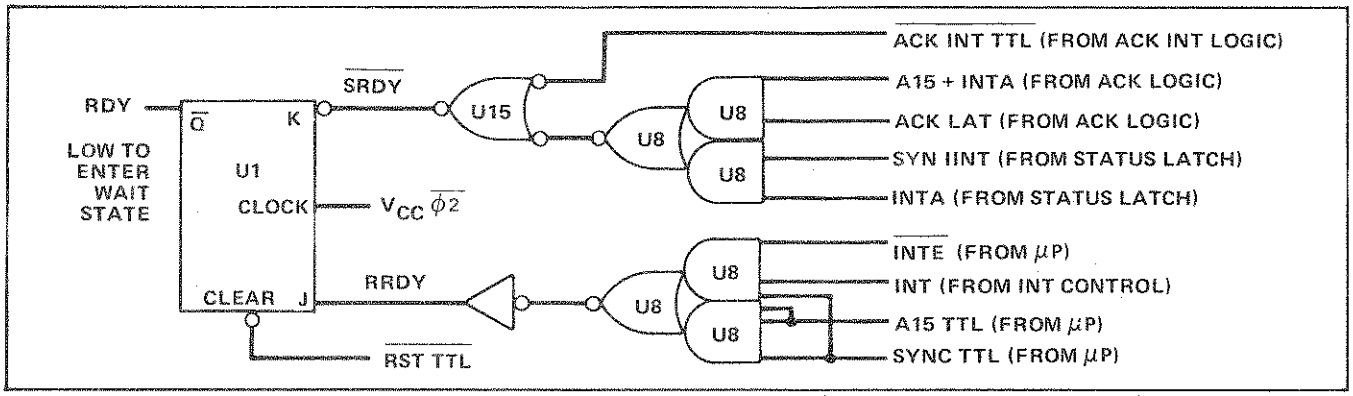


Figure 3-12. Wait Logic

monostable multivibrator, U36, and a "D" type flip-flop, U14. U36 is triggered by A15 TTL and SYNC $\overline{\phi 2}$. If DLD ACK does not occur within the time constant of U36, U36 will clock U14 to generate ACK INT. ACK INT TTL is also generated by U14 to end the wait state resulting from the external address.

3-52. The MARK INT logic is armed by an internal address keyed to RAM. A15 TTL is high indicating an internal address. DB4 is high as part of the status word indicating an address to an output device. A15 TTL and DB4 (both high) with SYNC $\overline{\phi 2}$ clock U1 through U31-12. A14 is low for a RAM address so U1-7 is clocked high. Although the address which arms the mark is keyed to RAM, no data transfer takes place between the microprocessor and RAM. The write signal (R/W) is disabled by OUT from the STATUS LATCH. MEM RD (memory read) is disabled by DBIN (from the microprocessor) and MEMR (from the STATUS LATCH) both being low. After ARM MARK (U1-7) is clocked high, the next pulse from the phase-locked loop timing circuit clocks U14 to generate the MARK INT signal.

3-53. Interrupts are prioritized through INT VECTOR (refer to Controller schematic, Section 8). Before entering a wait state after an interrupt, the microprocessor puts out a DBIN signal, signifying that it is ready to receive data. DBIN and INTA produce EN INT through U37 to enable the Interrupt Vector (U28). Internal interrupts are applied directly to U28 and have priorities of one (highest) for ACK INT and six (lowest) for MARK INT. For an internal interrupt, IINT is generated by one section of U38 (Figure 3-13) and, when latched into the Status Latch (U18), is used to end the wait state. For an external interrupt, SYN IINT is low and with EN INT low, INA is generated on the interbus. The interrupting module must respond with an

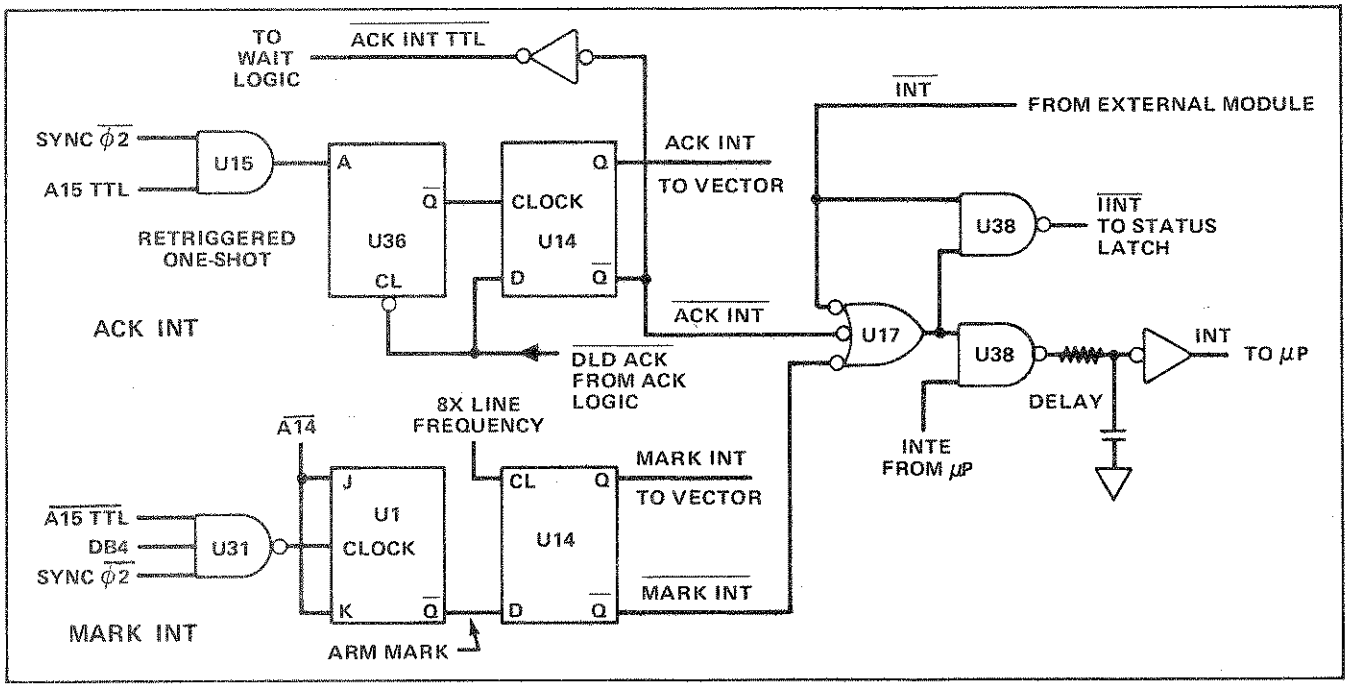


Figure 3-13. Internal Interrupts and INT Control

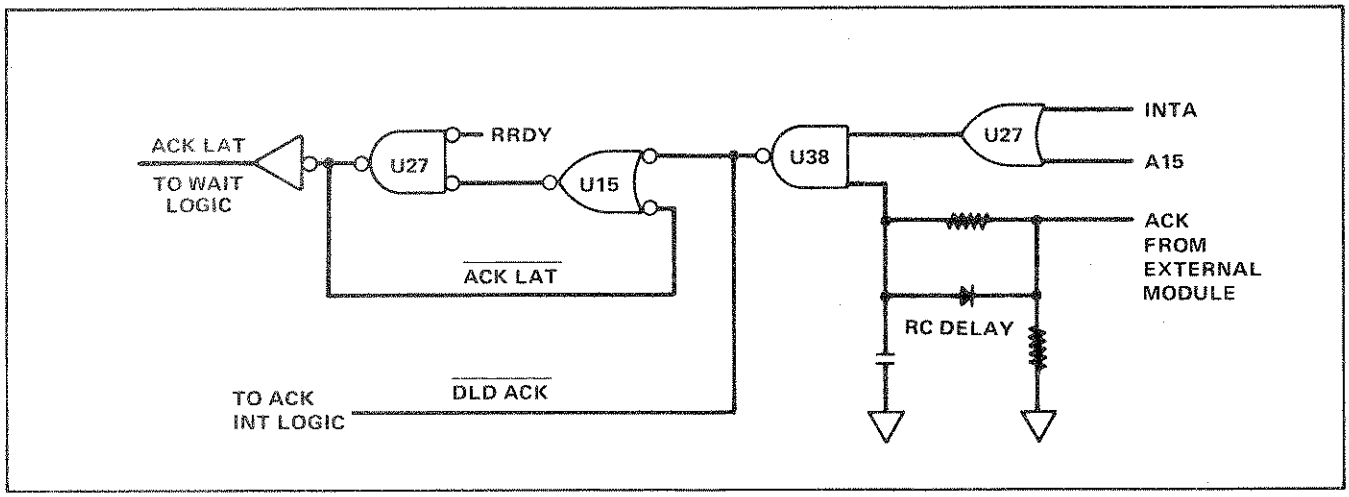


Figure 3-14. ACK Logic

ACK and a data bit on ID1-4. The returned ACK ends the wait state and the data bit is applied to INT VECTOR, U28. The complement of the output from U28 is placed on the data bus to instruct the microprocessor where to go for the next instruction.

3-54. Front Panel

3-55. Annunciator segment data is clocked into register one by the direct address, IC0, 1, 5 high. Refer to Figure 3-15. Data output from the switch matrix is also a direct address–IC0, 1, 6 high. For either direct address, the condition of ID7 (high for disable) is latched into U23 to enable an indirect address. Digit segment address–IC1, 5 high, and digit-annunciator select address–IC0, 5 are both indirect addresses. Data is clocked into the registers upon termination of the address. An update sequence is as follows:

1. Register one is addressed with all data lines low to blank the annunciator display and enable indirect addressing.
2. Register two is addressed indirectly with data lines low to blank the digit display.
3. Register three is addressed indirectly with all data lines high to turn off all LEDs, disable the switch matrix, and disable indirect addressing.
4. Register one is addressed with ID7 low to enable indirect addressing and with annunciator segment data on ID0-6. The data is latched and applied to the annunciator LEDs.
5. Register two is addressed with digit segment data on ID0-7 (U23 is not clocked by this address so ID7 may be high without disabling indirect addressing). The data is latched and applied to the digit LEDs.
6. Register three is addressed with ID7 high (disable indirect addressing) and one of the data lines, ID0-6, low to enable one digit LED and one annunciator LED. One bank of the switch matrix is also enabled.
7. The output buffer is addressed enabling the data from the previously enabled switch bank to be placed on the data bus. One or more lines low indicates a change is desired. This address also keeps the kill circuit charged.

3-56. The seven steps just outlined are required for one digit-annunciator-switch bank update. The process is repeated seven times for a complete update. The kill circuit is used to blank the display if the Controller discontinues addressing the front panel. Otherwise, segments would be left on continuously and would soon burn out.

3-57. DC Signal Conditioner

3-58. Relays K1 and K2 control the input to the DC Signal Conditioner and the attenuation of the input (Figure 3-16). If both relays are energized, the input is from the Volt/Ω input terminals with ÷ 64 attenuation. If just K1 is energized, the input is from the Volt/Ω input terminals with no attenuation. If just K2 is energized, the input is from RT1 (optional signal conditioners). Q10, Q11, CR3, and CR4 provide overvoltage protection.

3-59. A differential amplifier (Q18, Q19) drives U3. FET switches (Q14, Q15, Q16) control the gain of Q18, and Q37. An output voltage swing of ±20V is achieved through bootstrapping; U4 provides a bootstrap for Q33 and Q37, and U3 and U4 provide a bootstrap for U5 and U6. Current sink and source for Q18 and Q19 are provided by Q33 and Q37 respectively.

3-60. The DC Signal Conditioner is addressed by IC0, 3, 4 high. Data on ID0-3 is latched up and decoded to determine which switches and relays will be energized. Figure 3-16 includes an example of the relay driver used to minimize thermal changes in the relays between the on and off states. RC coupling between the decoder and the relay driver provide voltage swings up to 4V or down to 0V to ensure positive relay action. Steady state voltages of 1.45V (off) and 2.75V (on) minimize current differences between the on and off states while maintaining the relay state under all conditions.

3-61. Filter/External Reference

3-62. All inputs to the A/D Converter are routed through the Filter/External Reference module. Refer to Figure 3-17. External reference measurements are made by multiplexing the three Filter module inputs to the A/D Converter. Q18, Q19, and Q20 switch the signal conditioner input, the external reference LO input, and the external reference HI input respectively. Data controlling the switches is latched into U1 upon termination of the address (IC1, 3, 4 high).

3-63. Three-pole, active Bessel filters (U3 and U4) have different settling times and cut-off points. Either filter may be selected from the front input panel for application to the signal conditioner input. Bypass is automatically selected for external reference inputs or may be remotely selected for signal conditioner inputs. The combination of Q32, Q25, Q23, Q24, or Q21, Q22 is turned on to select a filter mode.

3-64. A dual, super-beta transistor in a differential configuration (Q27) drives U5. A current source (Q26) and sink (Q30) bias Q27. Enough current is drawn through R19 by Q26 to bootstrap the input amplifier, Q27, 5V above the output. Gain of the amplifier is set at one by the combination of R21 and the input resistors. The external reference inputs have additional series resistors located at the rear panel terminals.

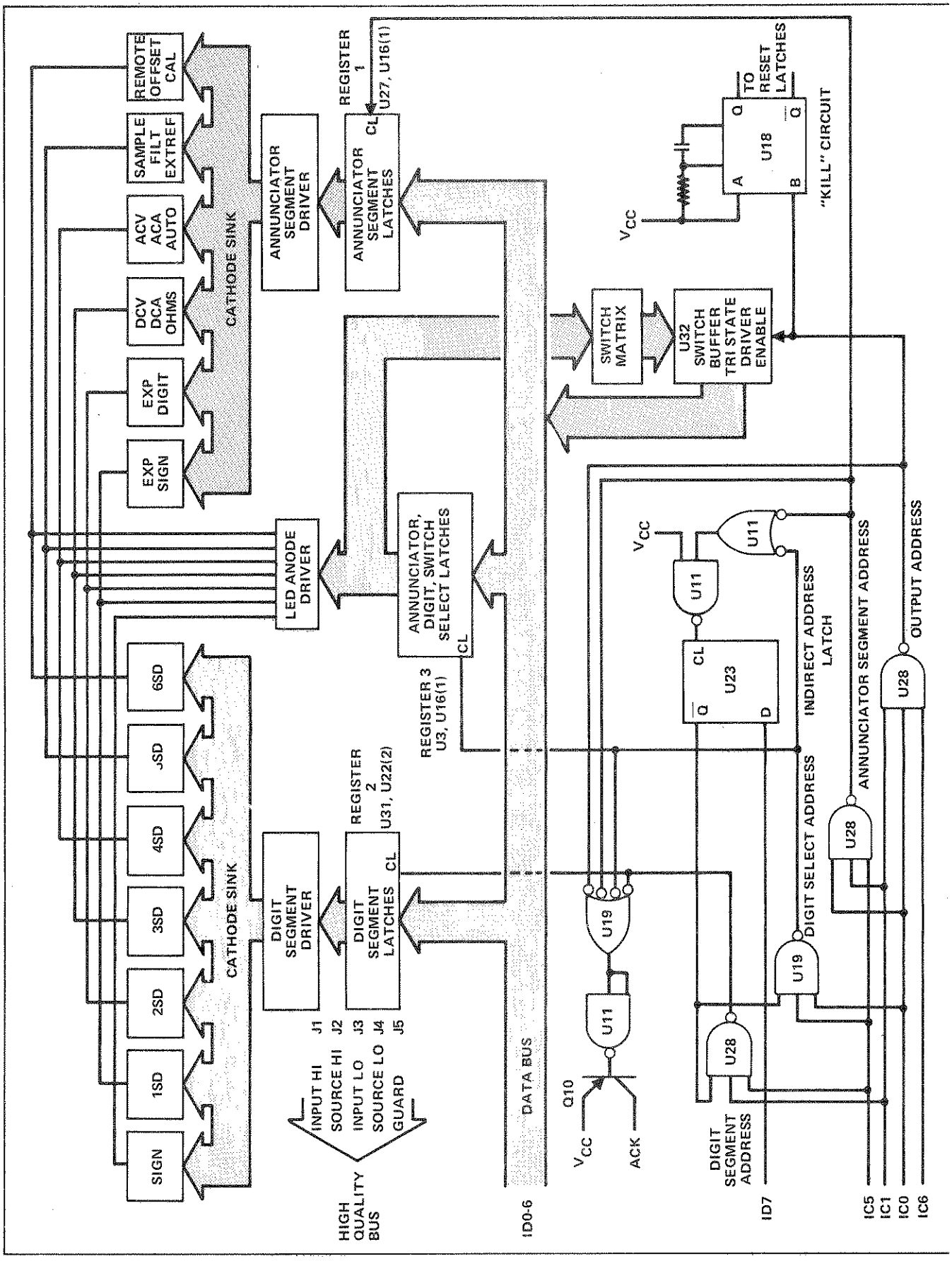


Figure 3-15. Front Panel

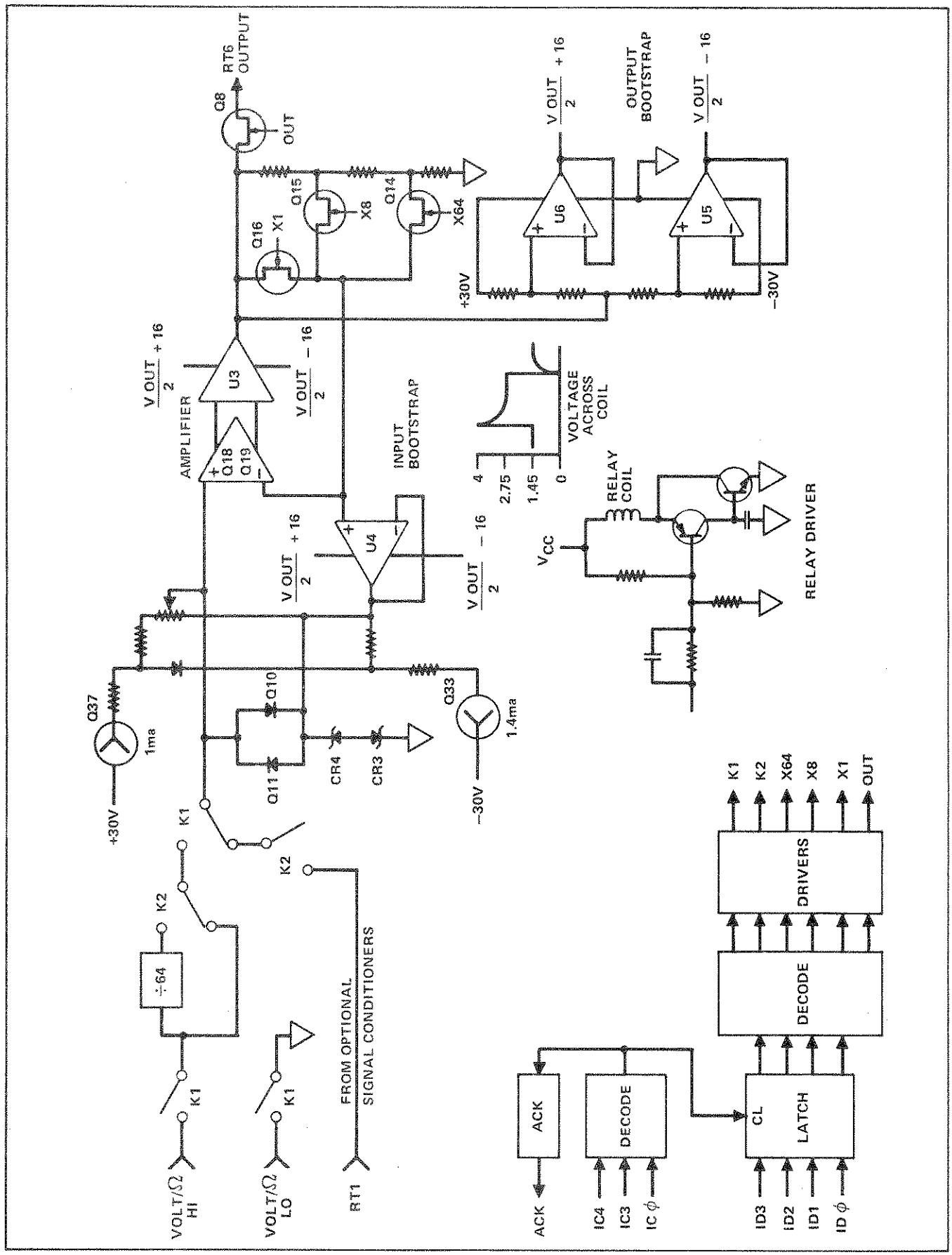


Figure 3-16. DC Signal Conditioner

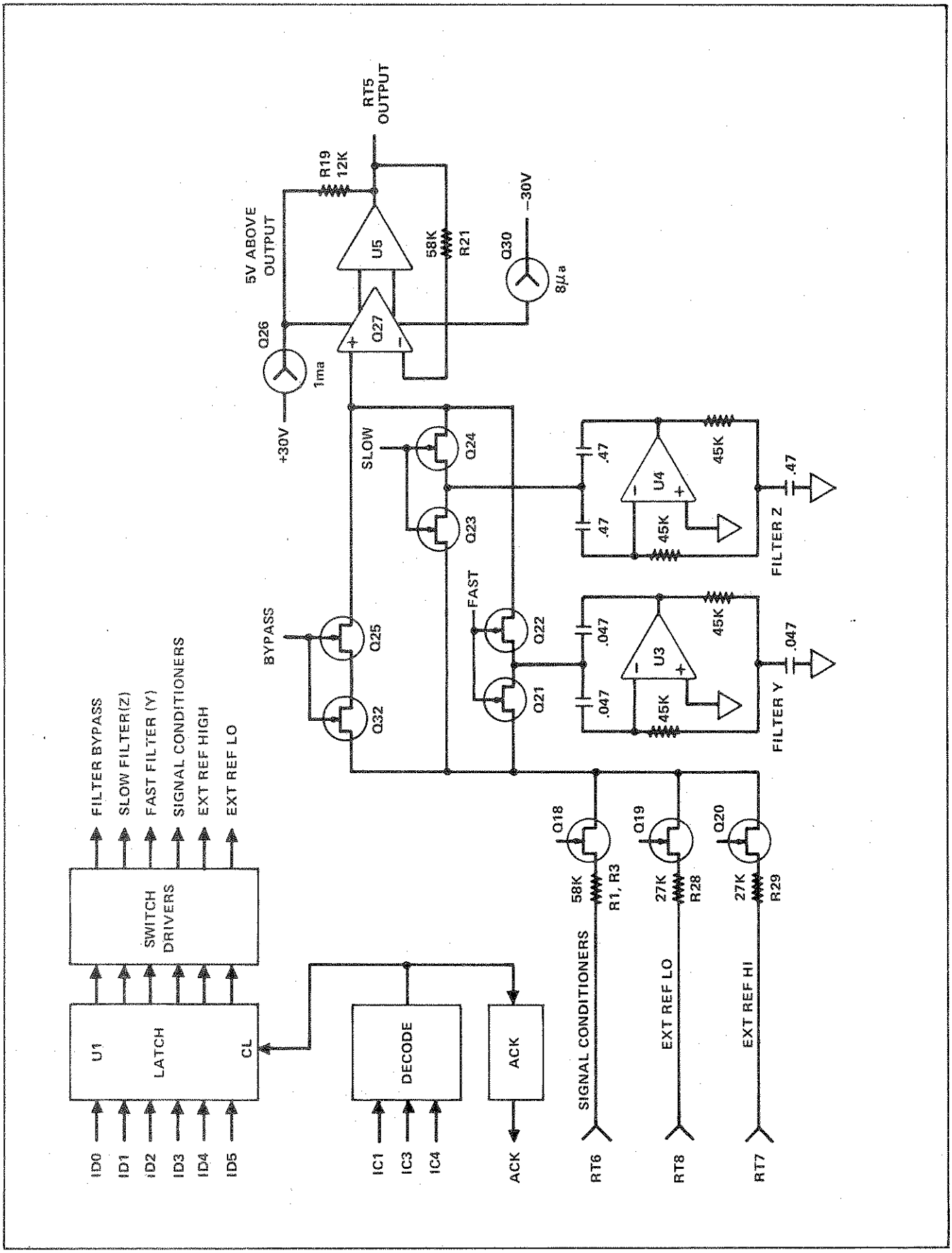


Figure 3-17. Filter/External Reference

3-65. Fast R^2 A/D Converter

3-66. The Fast R^2 A/D Converter may be separated for analysis into two component groups: Analog and Digital. Analog circuitry is responsible for producing a voltage reference, for summations, and for remainder amplification and storage. Digital circuitry interfaces the analog circuitry to the Controller and is responsible for reference selection, decisions in the summation process, remainder channel control, and autozeroing. Since functions within the A/D Converter are either directly controlled by the Controller module via the data bus or are clocked through their operations by the Controller addressing the A/D module, the A/D conversion program could be considered a functional part of the A/D Converter.

3-67. ANALOG

3-68. Figure 3-18 is a simplified schematic of the analog portion of the A/D Converter. For clarity, switches are shown as a circle enclosing a letter designator. U1 is a reference and reference amplifier controlling U2, a current source. The −7V reference is set by R9 and R14. U3 serves as a highly regulated collector and zener supply for U1. Operation of the D/A Converter requires both a positive and negative reference (for negative and positive inputs, respectively). Q9 and U4 are a precision unity gain amplifier whose input is controlled by switches A1 and A2. With A1 open and A2 closed, Q9 and U4 are configured as an inverting amplifier producing a positive reference. With A1 closed and A2 open, Q9 and U4 are a noninverting amplifier.

3-69. An input signal is applied to the summing node of the remainder amplifier (Q27, U7) through switch I. Q27 and U7 are an inverting amplifier with two gain configurations. During the decision period, switch G is closed, applying the output of U7 to polarity detector Q28 and forming a feedback path through CR5 and CR6. Q28 sends a polarity bit to the digital portion of the circuitry. On the basis of this first polarity bit, a reference polarity is selected.

3-70. Switches B, C, D, E, and F are closed, one at a time, to switch a precise amount of current into the summing node. When a switch is closed, the opposite switch is opened and vice versa. For example, when D is closed, $\overline{D}$ is opened. After a switch is closed, a polarity bit is returned. If the polarity changed with respect to the original polarity selected for a step, the switch is opened; otherwise it is left closed. The next switch is closed, a polarity bit returned and a decision made, and so on until all five switches have been closed (and possibly opened again). This constitutes a decision period.

3-71. Following the decision period is the subtraction period. Switch G is opened and switches X and SX are closed to form a feedback path for the remainder amplifier through the X channel. A 400K resistor, R35, sets the gain of Q27 and U7 at sixteen. The feedback current completes the summation process and the amplified remainder is stored on C10 in the X channel.

3-72. For the next decision period switches SX and X are opened and switches RX and G are closed. Since Q27 and U7 form an inverting amplifier, the opposite polarity reference (from the original selection) is automatically selected. The amplified remainder is applied to the summing node through U6 and R34. Five decisions are made, followed by a subtraction period using channel Y for feedback and remainder storage. The first decision-subtraction period applies the input signal to the summing node. The four following steps apply an amplified remainder, alternating between channel X and channel Y.

3-73. When a sample is complete, the circuits are autozeroed. U8 zeros the remainder amplifier through channel X. Any offset is stored on C13 at the noninverting input of Q27. The switching reference, Q9 and U4, is zeroed by first closing A1 and opening A2 to decrease settling time. Then A1 and A2 are both opened and the Z1 and Z2 switches are closed, storing any offset error on C5.

3-74. DIGITAL

3-75. For the following discussion, refer to the Digital Fast R^2 A/D schematic in Section 8. Direct address IC2, 3, 4 latches data into U34 and U35 controlling input switch I, remainder channel switches, autozero, and reset (digital). U31, a ring counter, is clocked to the C1 state enabling the indirect address decoder (U33) and the polarity detector (switch G). A polarity bit is returned and applied to U6.

3-76. Indirect address IC1, 2 latches the polarity bit in U6, enables the tristate transmitter, U5, and clocks U31 to the C2 state. The transition of U31 from C1 to C2 clocks the polarity into U11 (the uppermost section) whose output determines whether switch A1 or A2 will be closed (reference polarity). At the same time, U1 (uppermost section) is clocked to set the other section of U11, closing the first reference switch, B, of the D/A Converter. The next indirect address clocks a new polarity bit (a result of closing the first reference switch B) into U6. If the polarity changed, the output of U6 will cause a reset of the previous switch latch, opening the previous switch. At termination of the address the next switch is closed. One direct address and six indirect addresses are required to complete a step. The last indirect address resets the control logic to the C0 state.

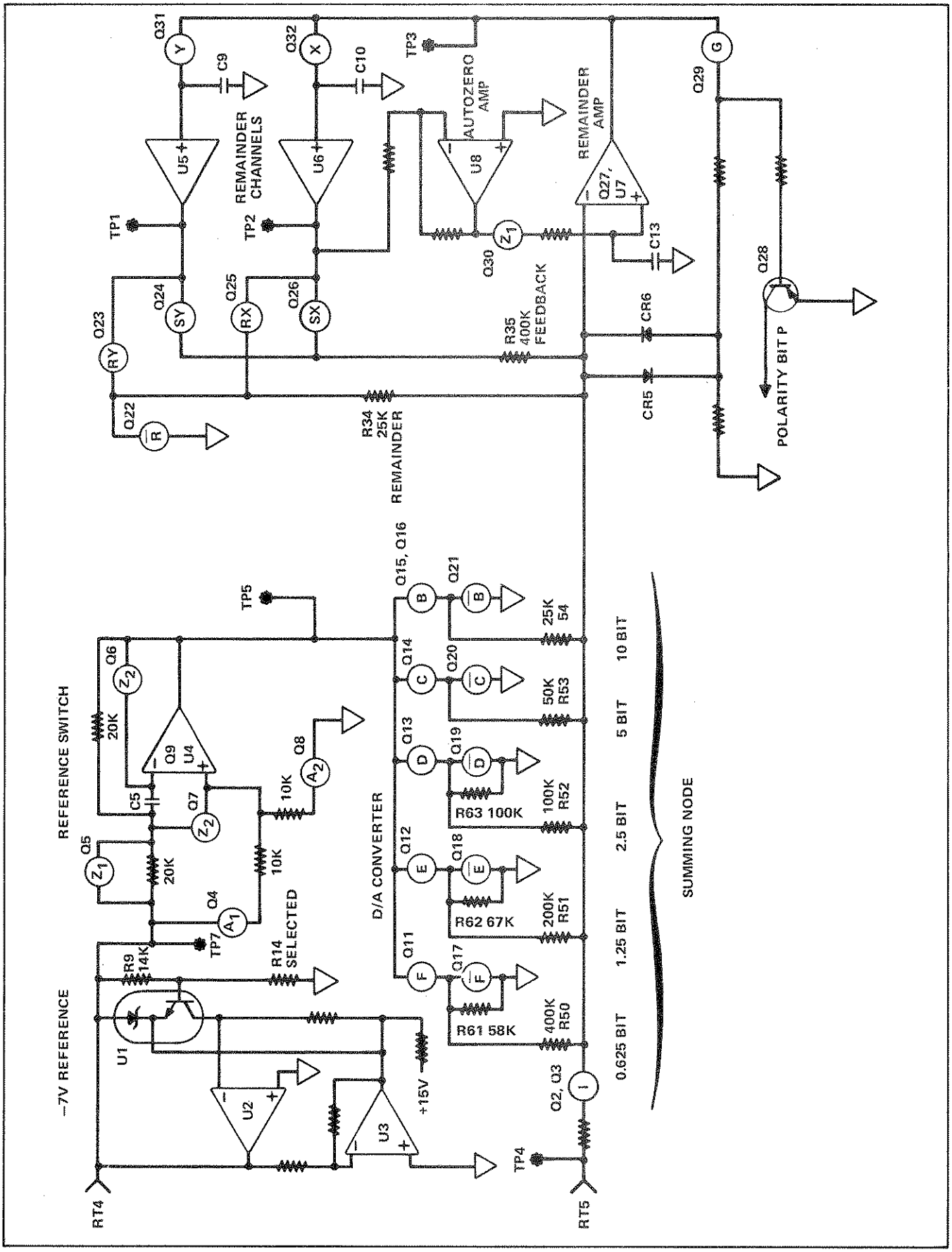


Figure 3-18. Fast R^2 A/D Converter (Analog)

3-77. Switch selections are made through switch drivers which rely on Vcc and Vss being at −15V and −20V with respect to analog common. This allows simple transition from TTL levels to FET off voltages. D/A Converter switches are selected on transition of U31 from one state to the next. The transition clocks the first of two "D" flip-flops which sets the second. The output of the second latch resets the first and selects the switch. If the polarity does not change after closing a switch, the output of U6 plus the output of U11 (reference select) will place two highs on the input of one section of AND gate U25. Through OR gate, U16, a one will be applied to the D input of that switch latch. The next transition of U31 will clock the latch, keeping the switch closed. If the polarity had changed, a zero would be applied to the D input, opening the switch.

3-78. After the last step, at completion of a sample, the Controller addresses the A/D Converter for autozero. U31 is clocked to the C7 state causing a digital reset. When U6, storage capacitor disable, is reset, autozero is enabled. RC coupled gates delay the zero switch controls so that switch A1 may be closed and A2 opened in the reference switching circuit. This provides a faster settling time for the reference switching amplifier. Both A1 and A2 are opened during the autozero time.