Option —04
Calibration Memory

604-1. INTRODUCTION

604-2. Installation of the Calibration Memory module permits extended calibration intervals while maintaining the accuracy of the instrument. A calibration factor is entered into memory with a single keystroke. Calibration factors are determined by comparison to a standard at the cardinal point for each function and range. An input of +1.000000V dc would be the cardinal point for the 1V dc range. A non-volatile memory allows storage of calibration factors for at least one year or until the instrument is completely recalibrated.

604-3. SPECIFICATIONS

604-4. DC Zero, Ohms Zero, and calibration factors for the cardinal points of every range and function will be maintained for at least one year with no power applied to the instrument.

604-5. INSTALLATION

604-6. Refer to Section 4 of this manual under Module Installation and Removal for installation procedures. The interconnect diagram in Section 8 contains a table listing permissible and preferred slots.

604-7. OPERATING NOTES

604-8. When the Calibration Memory module is installed, care must be exercised when using the instrument in the high resolution mode. Inadvertently depressing the STORE switch while in the high resolution mode will erase the cal factor for that function and range from memory and enter an erroneous factor. Use the following procedure to enter calibration factors.

1. Ensure that the DC Zero and Ohms Zero procedures have been performed.
2. Verify that the EXT REF and OFFSET indicators are extinguished.
3. Select the Cal mode (CAL indicator illuminated).
4. Select the desired function and range.
5. Apply an input from a calibration source equal to the value of the cardinal point at the function and range selected (e.g., with 10V dc selected apply +10.000000V dc).
6. Depress the STORE switch. The reading displayed should be equal to the value of the input ± the listed specification as long as the switch is held in.
7. Repeat steps 4, 5 and 6 for each applicable function and range.
8. Depress the RECALL switch to display the last uncorrected reading taken while in the Cal Memory mode. The reading is displayed until the switch is released.
9. To remove Calibration factors from the Cal Memory, use the foregoing procedure, except in step 5 use a short (an open for current factors) at the input terminals instead of the calibration source.

NOTE

Correction factors entered for the V ac rms feature automatically correct any reading in dc coupled ac.

604-9. THEORY OF OPERATION

604-10. The Calibration Memory module provides non-volatile read/write memory used to store calibration constants and dc and ohms zero factors. When the dc or ohms functions are selected, the appropriate zero factor (if one was entered) is brought out by the instrument controller for storage within the controller module. Likewise, when a new function or range is selected, calibration constants are read from and stored for immediate use within the controller module.

604-11. This module was designed for use in more than one instrument, so there are land patterns and some devices which are not used in this particular instrument on the pcb. The following discussion is keyed to the schematic, Figure 604-1.

604-12. RAM Location Addresses

604-13. RAM location addresses are sent to the Calibration Memory module on the instrument data bus, ID0-7. Address IC1, 2, 6 clocks the data into U23 through U15-10, and U14-12. Outputs from U23 determine the location in the RAMs that data will be written or read.

604-14. Write Operation

604-15. Addresses used in both read and write operations are true 3 of 7 codes in which three IC lines must be high and four low to obtain a response. Writing data into memory first requires an address (IC3, 4, 5 high) and a data key (ID 0, 3, 5, 6 high, ID 1, 2, 4, 7 low) to set the circuitry into the write mode. The address is decoded by U15-9, U14-1 ANDed by U13-3 (VA1). The data key is decoded by U24-13, U24-1 ANDed by U13-4 (KEY). VA1 and KEY are ANDed by U2-11 to produce the ACK response (U17, Q1) and to set U12-2 low (WRITE) through U25-10. The module is now set into the write mode.

604-16. The next address (IC0, 2, 6 high) is decoded by U15-6, U14-13 ANDed by U13-10 (VA2). VA2 triggers a one-shot multivibrator, U1-4, so U2-5, 6 are both low and VA2·WRITE is true (low) which sets the RAMs into the write mode. U12-1 is high so U2-3 is high which disables the outputs of the RAMs (OD). Data to be written into the RAMs accompanies this address and is stored in the memory location previously clocked into U23. At termination of the address, VA2 goes high clocking U12-1 low and U12-2 high, which sets the module into the read mode.

604-17. Read Operations

604-18. The module stays in the read mode unless set into the write mode. Read operations require the address resulting in VA2 as previously explained. This time U12-1 is low (READ). U2-3 goes low enabling the RAM outputs. U2-4 is high setting the RAMs (R/W) into the read mode. The desired memory location must have been clocked into U23 prior to the READ address.

604-19. TROUBLESHOOTING

604-20. Problems in the Calibration Memory can cause apparent problems in all functions of the instrument. The most common problem is wrong values entered. The recall feature may be used to determine the value of the stored correction factor. Since correction factors are multipliers, the stored value will be close to one and consequently difficult to display meaningfully. Instead, the last uncorrected reading is displayed when in the CAL mode, and the RECALL switch is depressed. Dividing the cardinal value for the selected range into the last uncorrected reading results in the stored constant. By using the recall feature, it is fairly easy to determine if a reasonable cal constant is stored.

604-21. The three following checks may be made to determine if the Calibration Memory is functioning properly.

1. Store zeros for all functions and ranges, then recall the zero values.

2. Store cardinal points for all functions and ranges, then recall for the last uncorrected reading.

3. Remove power for two or more hours (to ensure that the RAMs have discharged C7 to the battery level), then reapply power and recall as in 1 and 2. This checks the shift of RAM power supply from Vcc to battery and back to Vcc. The purpose of C7 is to remove glitches in the RAM supply which can scramble entries stored in RAM.

604-22. Table 604-1 lists the test points found on the Calibration Memory module. Table 604-2 gives a symptom analysis approach to troubleshooting.

604-23. PARTS LIST

604-24. Table 604-3 gives a parts breakdown for the Calibration Memory module. Refer to Section 5 of this manual for ordering and use code information.

Table 604-1. Test Points

TP1 – Vss; logic return, use as LO return for test instrument
TP2 – VA2 · READ; low for the controller to read from cal memory goes low 3 or 4 times every 200 msec
TP3 – VA2 · WRITE; low for the controller to write into cal memory goes low 4 times for every STORE switch push
TP4 – RAM Supply Voltage; when power is on =Vcc – .6V when power is off = battery voltage
TP5 – Negative Battery Terminal
TP6 – Vcc; Logic Supply
TP7 – ACK; acknowledge signal returned when module addressed

Table 604-2. Symptom Analysis

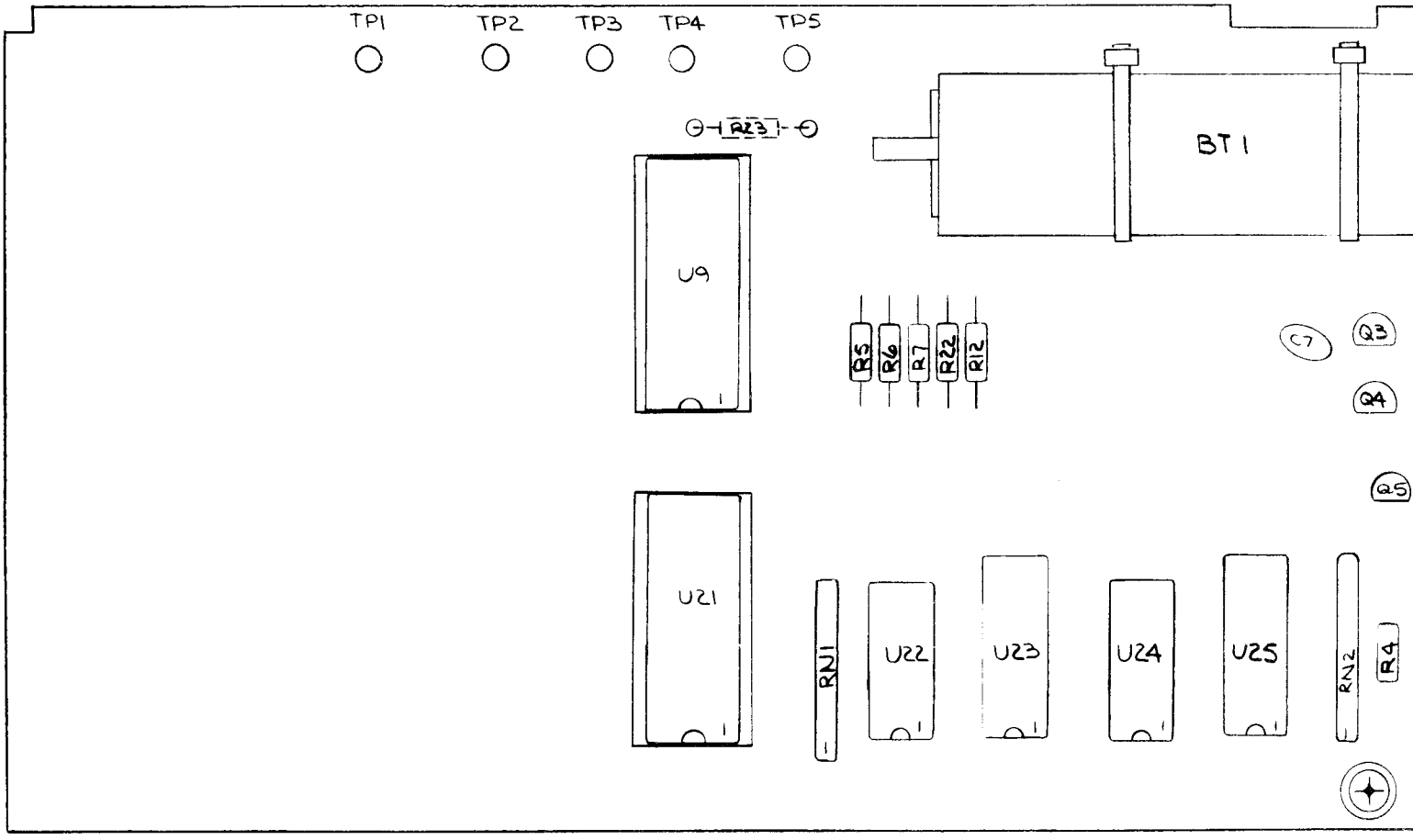
SYMPTOM	POSSIBLE FAILURE
Won't Store	VA2 · WRITE missing; check TP3
Won't Read	VA2 · READ missing; check TP2
Error at Turn-On	Battery voltage bad at TP4, RAM defective, not reading
Wrong Readings	U23 (RAM address latch), RAM defective, wrong data stored

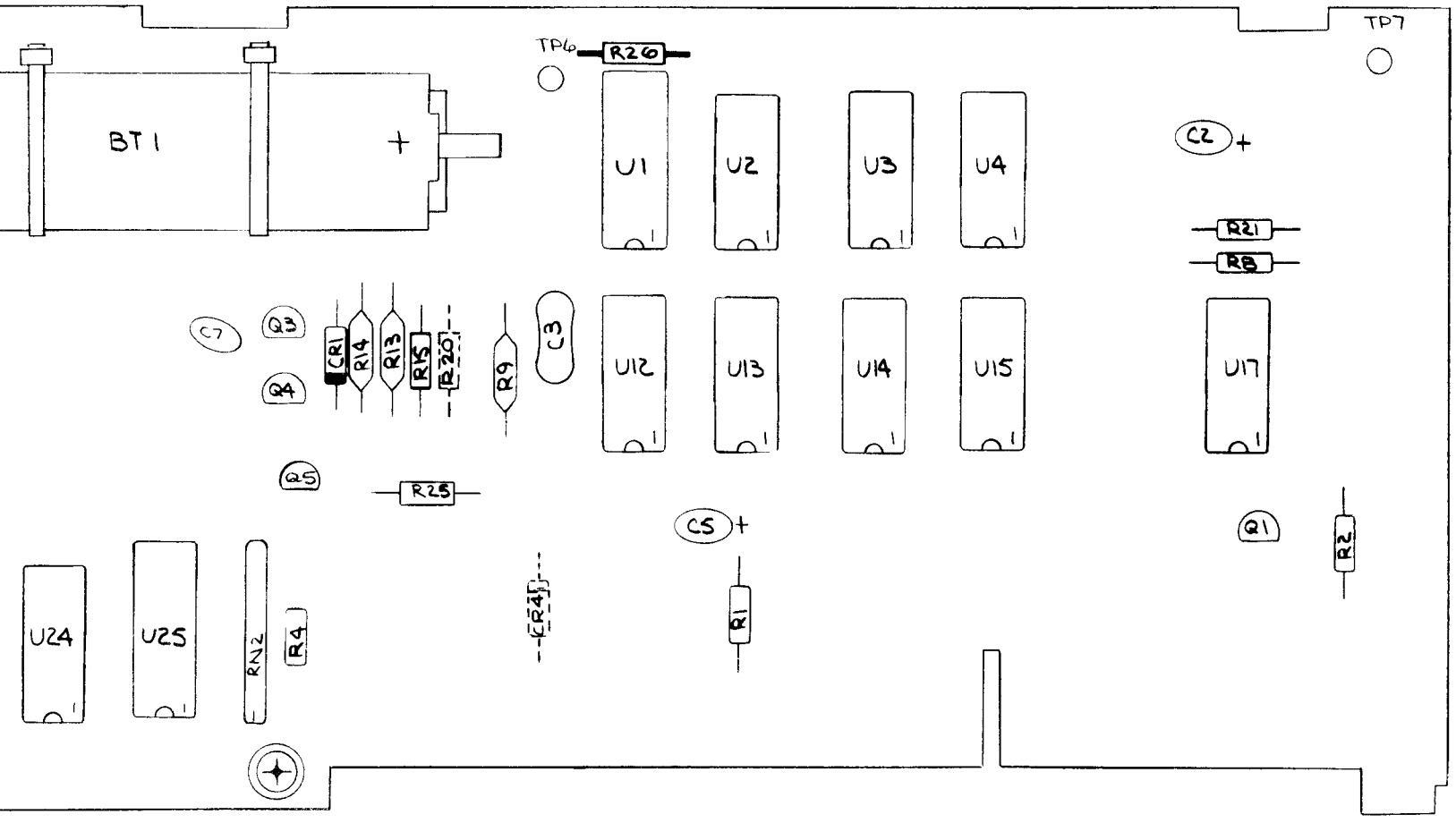
Table 604-3. Calibration Memory Assembly

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
Ⓧ	**CALIBRATION MEMORY ASSEMBLY** **Figure: 604-1**						
BT1	Battery Lithium (use when R20 & CR4 are not installed)	408286	89536	408286	1		G
BT1	Battery Lithium (see above)	448498	89536	448498			H>
BT1	Battery Ni-cad (use when R20, CR4 and U9, U21 P/N 408757 are installed)	412890	06001	PPS2092	1		
C2	Cap, Ta, 0.47 uF ±20%, 35V	161349	56289	196D474X0035 HA1	1		
C3	Cap, mica, 180 pF ±5%, 500V	284786	72136	DM15F181J	1		
C4	Cap, Ta, 0.33 uF ±20%, 35V	408690	56289	196D334X0035 HA1	1		
C5	Cap, Ta, 1 uF ±20%, 35V	161919	56289	196D105X0035 JA1	1		
C6	Cap, mica, 390 pF ±5%, 500V	148437	72136	DM15F391J	1		
C7	Cap, Ta, 10 μF ±20%, 15V	193623	56289	1960106X 0015KA1	1		
CR1, CR2	Diode Hi-speed switching	203323	07910	1N4448	3	1	
CR4	Diode, Hi-speed switching (use with U9, U21 when P/N408757 installed)	203323	07910	1N4448	REF		
Q1	Xstr, Si, PNP	226290	04713	MPS3640	1	1	
Q3	Xstr, Si, NPN	168716	89536	168716	1	1	
Q4	Xstr, FET, N-channel	370072	89536	370072	1	1	
Q5	Xstr, Si, PNP	195974	04713	2N3906	1	1	
R1	Res, car, dep, 150 ±5%, 1/4W	343442	80031	CR251-45P151T	1		
R2, R11	Res, car, dep, 47k ±5%, 1/4W	348896	80031	CR251-45P473T	1		
R4 thru R8, R12, R15, R16, R21, R22, R24, R25	Res, car, dep, 100k ±5%, 1/4W	348920	80031	CR251-45P101T	12		
R9	Res, mf, 10k ±1%, 1/8W	168260	91637	MFF1-81002F	1		
R10	Res, mf, 130k ±1%, 1/8W	221648	91637	MFF1-81303F	1		
R13	Res, mf, 34k ±1%, 1/8W	261602	91637	MFF1-83402F	1		

Table 604-3. Calibration Memory Assembly (Concluded)

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
R14	Res, mf, 6.04k ±1%, 1/8W	285189	91637	MFF1-86041F	1		
R20	Res, car, dep, 1k ±5%, 1/4W (use with U9, U21 when P/N 308757 is installed)	343426	80031	CR251-45P102T	1		
RN1, RN2	Res Network	412908	89536	412908	2	1	
U1	⊗IC, Dgtl, TTL, lo-pwr Schottky	404186	01295	SN74LS123N	1	1	
U2	⊗IC, Dgtl, C-MOS, quad, 2-input OR gates	408393	18725	CD4071BE	1	1	
U3, U4	⊗IC, Dgtl, C-MOS, dual complimentary pair plus inverter	408013	02735	CD4007AE	2	1	
U9, U21	⊗IC, Dgtl, C-MOS, 1024 bit, static RAM (use with 408286)	429860	34649	P5101L	2	1	
U9, U21	⊗IC, Dgtl, C-MOS, 1024 bit, static RAM (use with 412890)	408757	34649	P5101L-3	2	1	
U12, U22	⊗IC, C-MOS, dual "D" type, flip-flop	340117	02735	CD4013AE	2	1	
U13	⊗IC, Dgtl, C-MOS, quad, 2-input NAND gates	355198	02735	CD4011AE	1	1	
U14	⊗IC, COS/MOS, dual 4-input NOR gates	363820	02735	CD4002AE	1	1	
U15	⊗IC, Dgtl, C-MOS, triple, 3-input AND gate	408807	02735	CD4073B	1	1	
U17, U24	⊗IC, Dgtl, C-MOS, dual 4-input AND gate	408799	02735	CD4082B	2	1	
U23	⊗IC, Dgtl, C-MOS, hex "D" flip-flop	404509	12040	MM74C174N	1	1	
U25	⊗IC, Dgtl, C-MOS, hex, inverter/buffer	381848	02735	CD4049AE	1	1	
U26	⊗IC, Dgtl, COS/MOS quad exclusive OR gate	355222	02735	CD4030AE	1	1	
	Case half, module	402990	89536	402990	2		
	Cover Module Case	402974	89536	402974	1		
	Decal, cal. memory	413484	89536	413484	1		
	Guard, front	383356	89536	383356	1		
	Guard, rear	383364	89536	383364	1		
	Shield, cover	411975	89536	411975	1		
	Socket, component lead	343285	00779	2-331272-6	2		
	Socket, IC, 22 pin	453126	91506	322-AG39D	2		

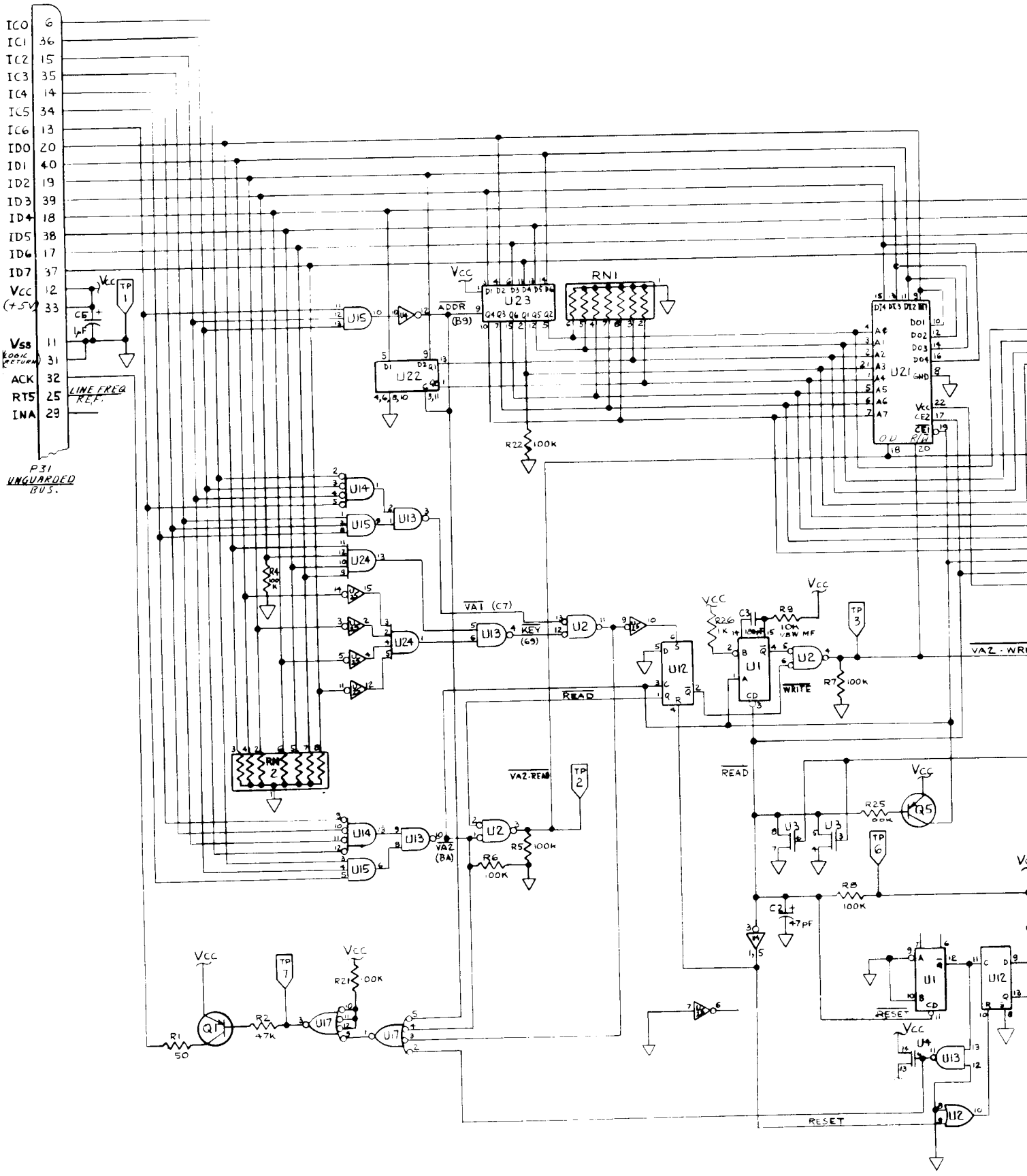

TP1
TP2
TP3
TP4
TP5
R23
BT1
U9
R5
R6
R7
R22
R12
C7
Q3
Q4
Q5
U21
RN1
U22
U23
U24
U25
RN2
R4

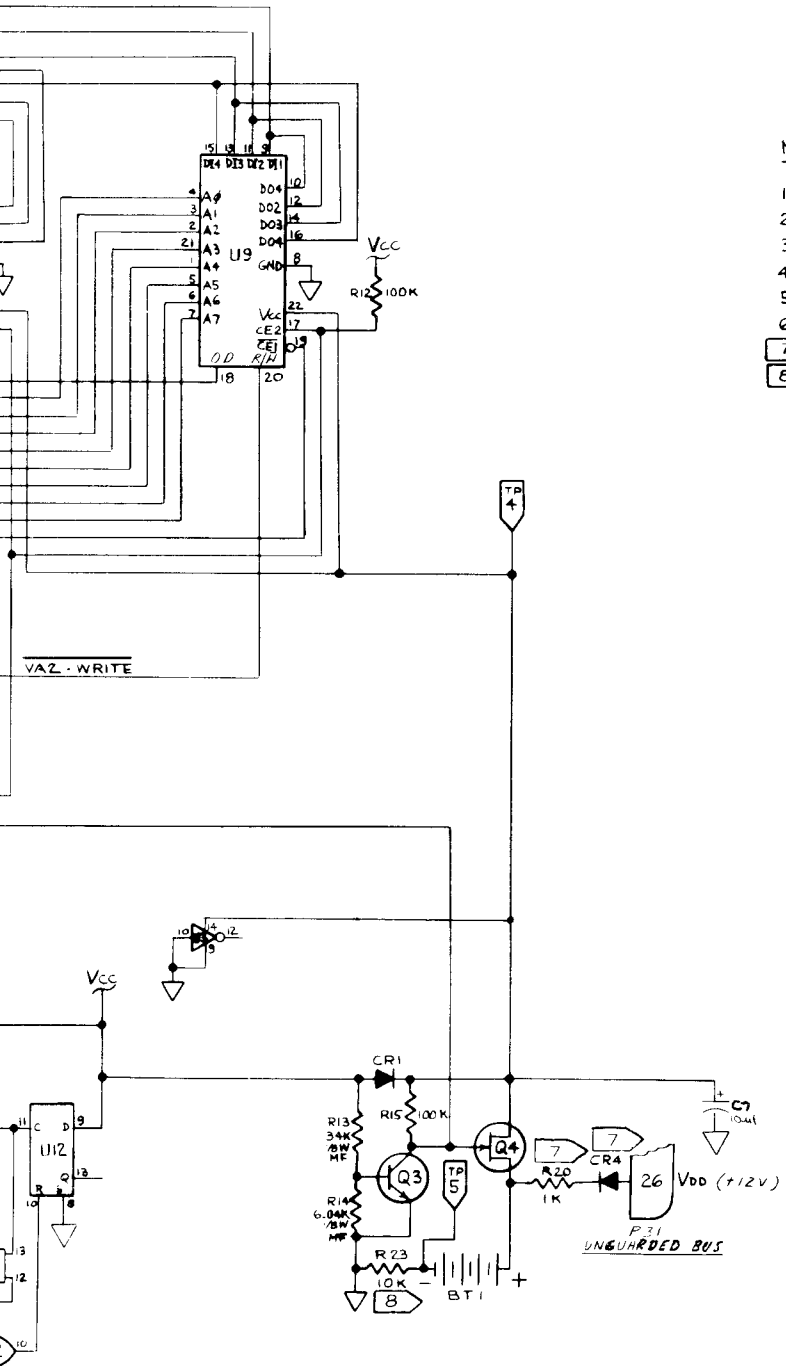


NOTES:

1. FOR SCHEMATIC DIAGRAM SEE 8500A-1160.
2. FOR P.C.B. SEE M.I.S.-3160.
3. FOR ASSY. DRAWING SEE 8500A-4160.
4. R 20 & CR4 WILL ONLY BE INSTALLED WHEN A NI-CAD BATTERY IS INSTALLED.
5. R21 WILL BE REPLACED BY A JUMPER WHEN A NI-CAD BATTERY IS INSTALLED.

Figure 604-1. Calibration Memory Assembly (850


IC0 6
IC1 36
IC2 15
IC3 35
IC4 14
IC5 34
IC6 13
ID0 20
ID1 40
ID2 19
ID3 39
ID4 18
ID5 38
ID6 17
ID7 37
Vcc (+5V) 12 33
Vss (LOGIC RETURN) 11 31
ACK 32
RTS 25
INA 29
P31 UNGUARDED BUS.
LINE FREQ REF.
TP 1
C5 1μF
RN1
U23
U22
U21
ADDR (B9)
R22 100K
U14
U15
U13
U24
R4 100K
VA1 (C7)
KEY (69)
U2
U12
U1
R26 1K
R9 10K 1/8W MF
R7 100K
WRITE
READ
VAZ·WR
TP 3
RN 2
VAZ·READ
TP 2
VAZ (BA)
R5 100K
R6 100K
R25 100K
Q5
TP 6
R8 100K
C2 47pF
TP 7
R21 100K
Q1
R1 50
R2 47K
U17
RESET
U4



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTOR ¼W, CC, ALL RESISTANCE IN OHMS.
2. FOR REF. DESIGNATION SEE 8500A-1760
3. FOR PCB DETAIL SEE MIS-3160
4. FOR ASSY. DWG. SEE 8500A-4160.
5. LAST REF. DES. NO'S USED: U25, Q5, CR4, C7, RN2, R23, BT1.
6. REF. DES. NO'S NOT USED: U5-U8, U10, U11, U16, U18-U20, R3, R17-R19, CR3, C1, R10, R11, R16, R22, CR2, C4 AND C6
7. CR4 & R20 ARE ONLY USED WHEN NICKEL CADMIUM BATTERY (BT1) IS INSTALLED.
8. R23 WILL BE INSTALLED WHEN USING LITHIUM BATTERY. A JUMPER WILL BE INSTALLED WHEN USING NI-CAD BATTERY.

CAUTION — THIS ITEM SHOULD BE INSTALLED DURING TEST TO AVOID CURRENT DRAIN FROM BATTERY, WHICH COULD OCCUR DUE TO INSTALLATION OF FAULTY COMPONENTS.

Figure 604-2. Calibration Memory (8500-1160)