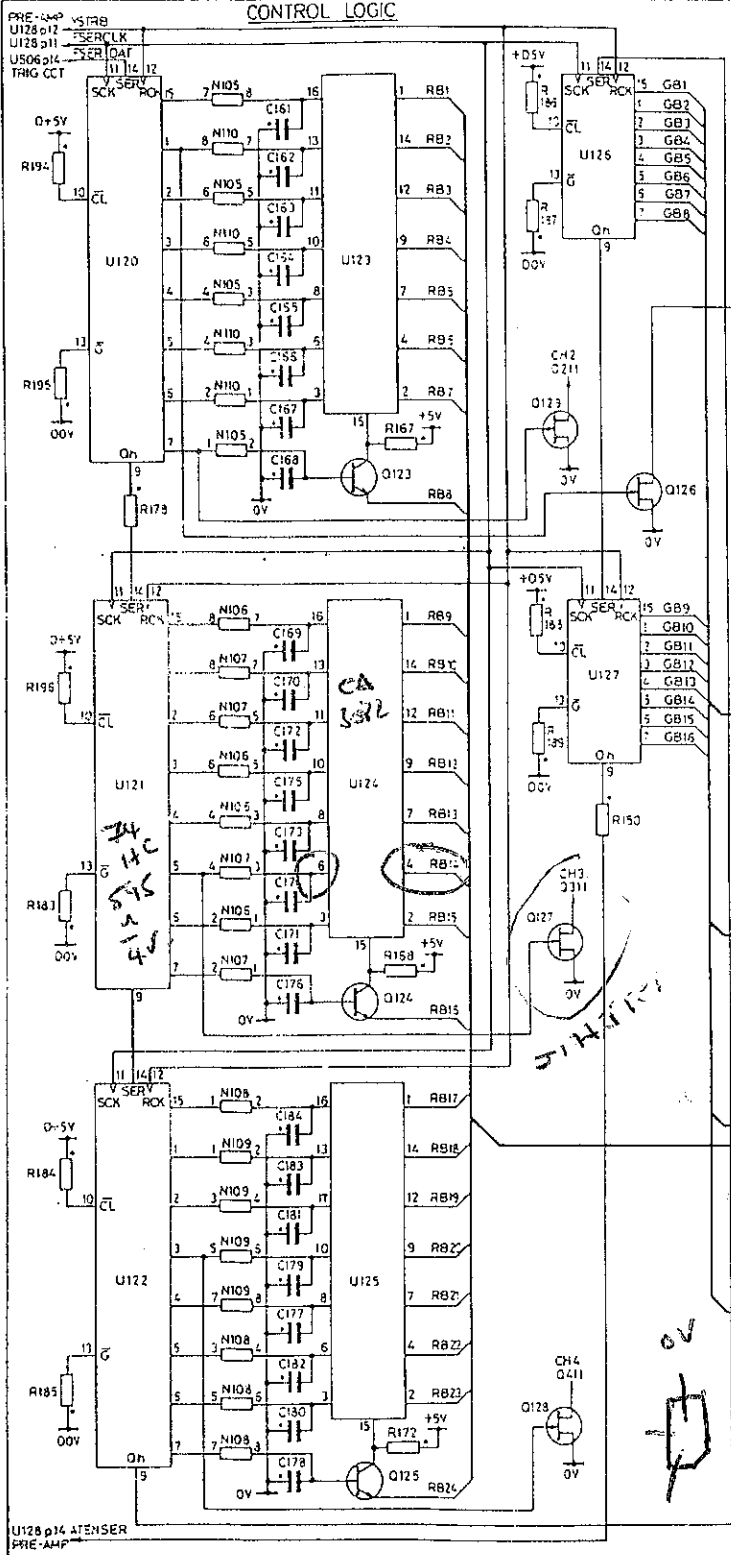


CH1 457001

CH2 457502

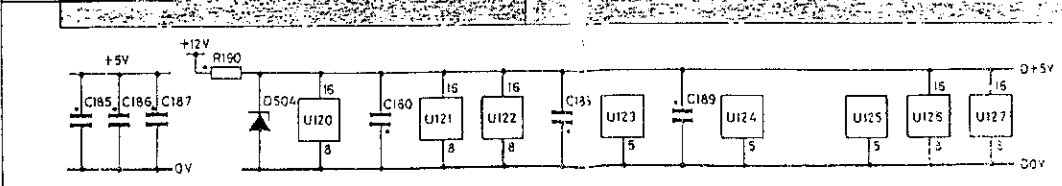
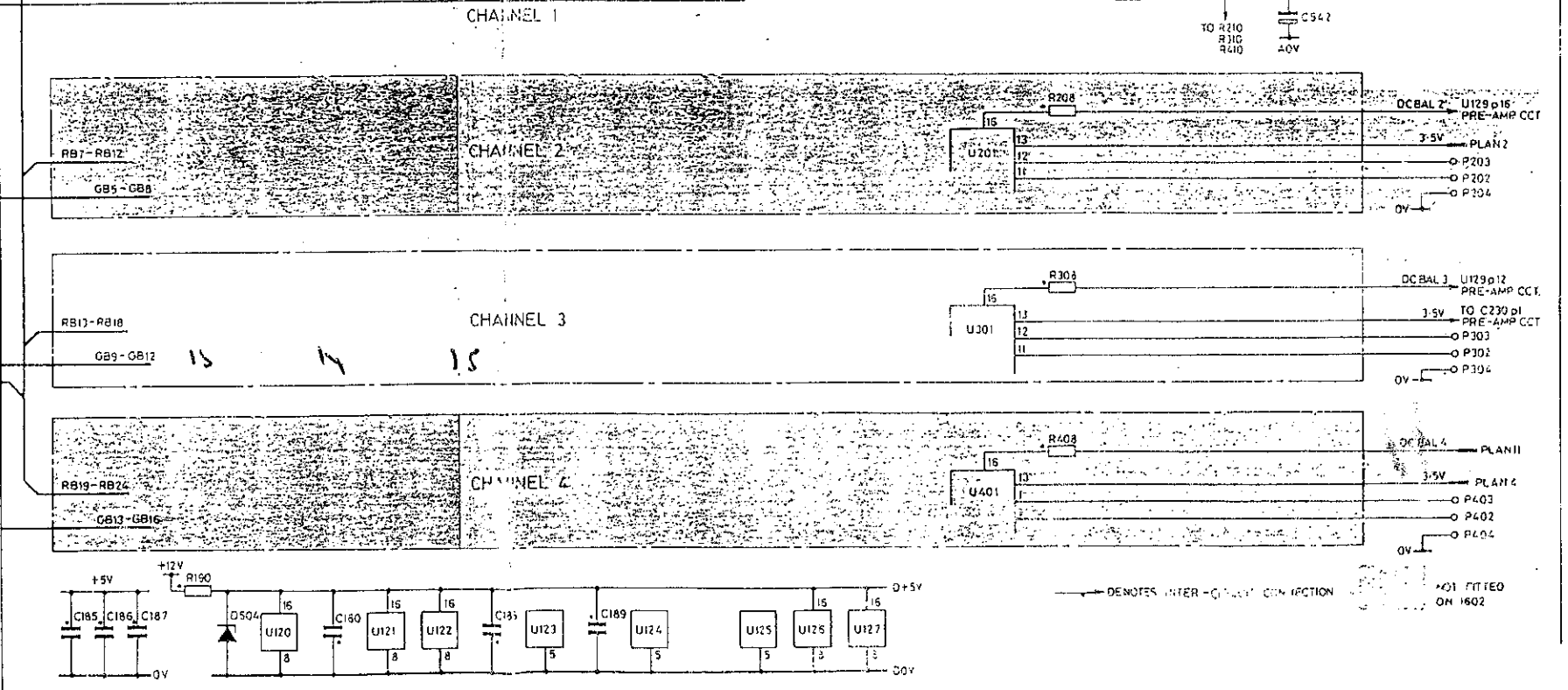
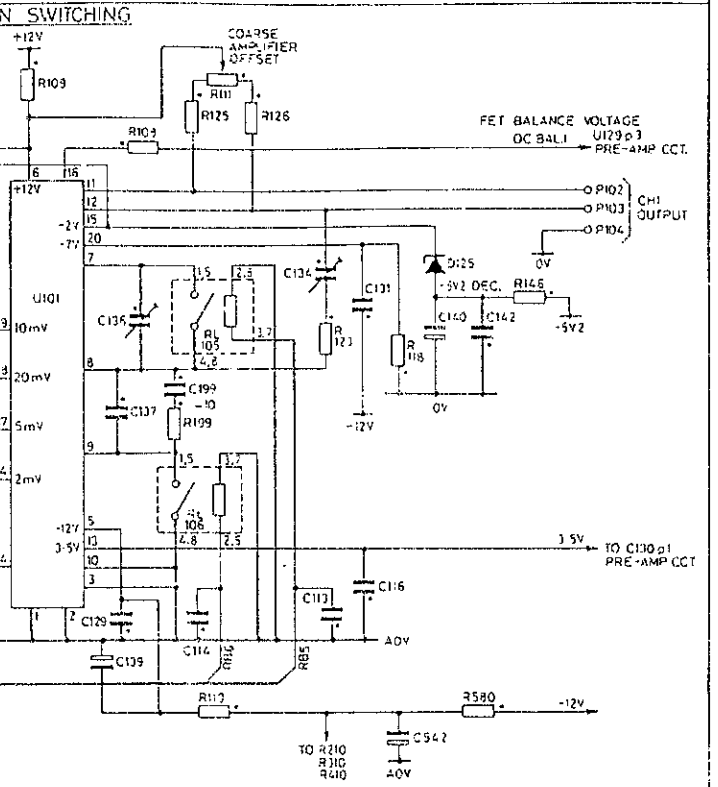
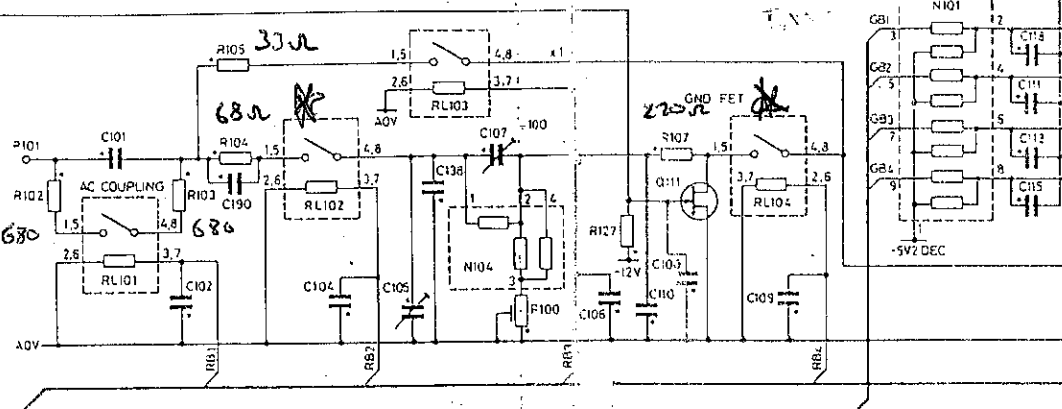
Wrona

RES.	R178	N105 N106 N107 N108 N109	R167 R168 R172	R134 R137 R138 R139	R150	R102	R103 R104	R105 R104	R100	R127	R107	N101	R109	R108 R109 R110	R125 R111 R126	R123	R118	R146	
CAPS.		C151 C184				C101	C190	C104	C105 C160	C107	C106	C110	C109	C135 C136 C137 C138 C139	C199 C114	C134 C113	C131 C116	C146	C142
MISC.	U120 U121 U122		U123 U124 U125	U127 U128	U126 U127								U101 U201 U301 U401		RL105 R105			D125	R580



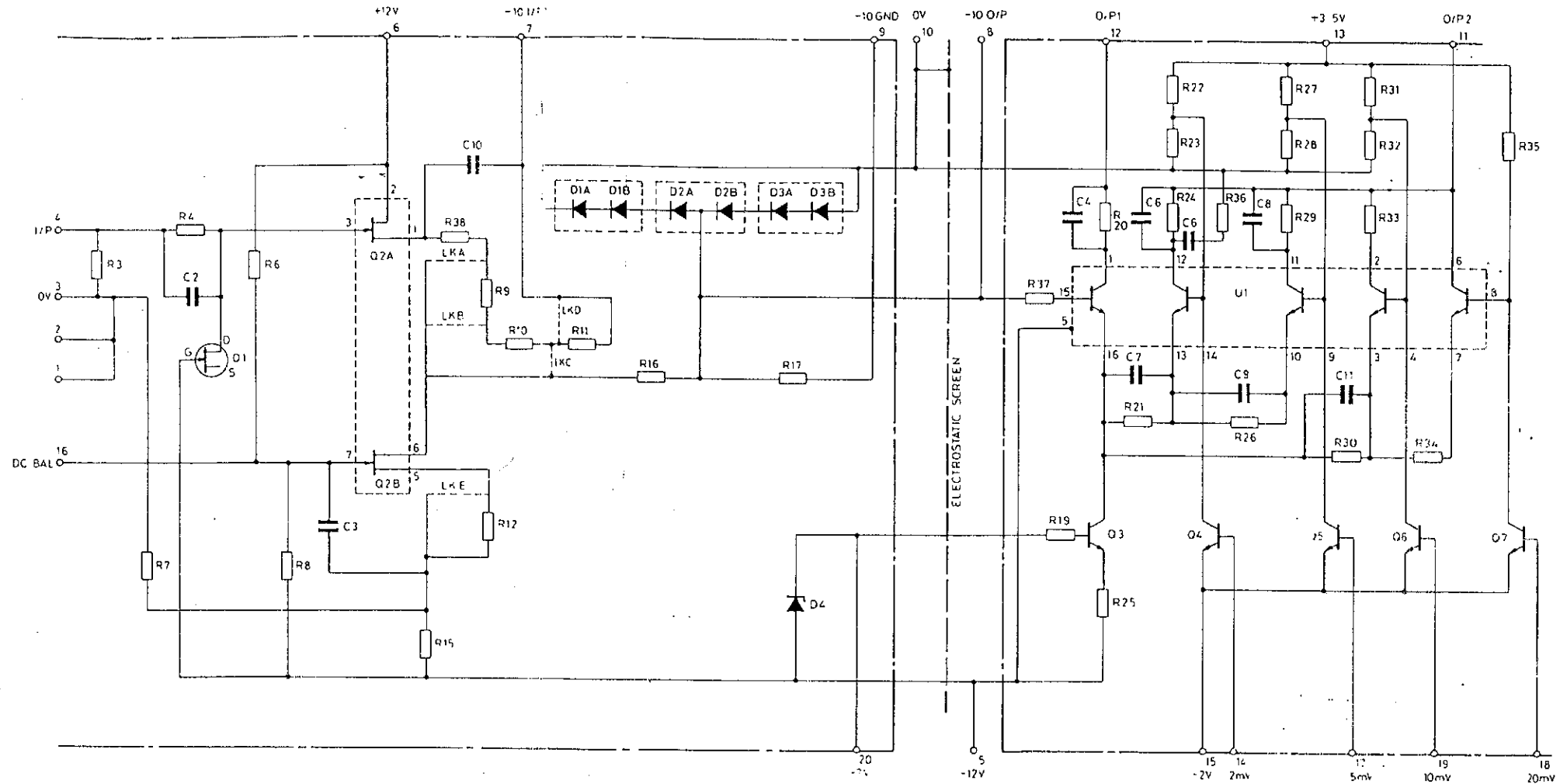
0.2V RANGE = OK.  
0.1V " " "  
0.5 OFF SCREEN  
See page 43 CHART.

4.3v dc  
ON 11/12.  
NOISE LEVEL  
ON 11/12.



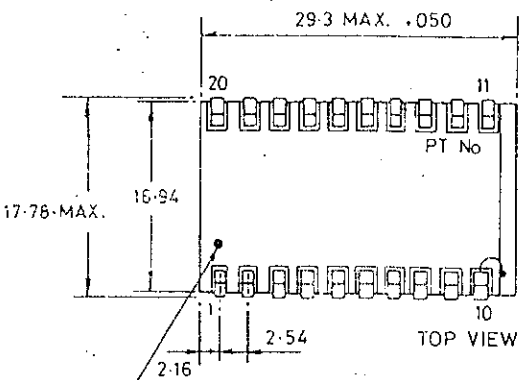
→ DENOTES INTER-CIRCUIT CONNECTION \*01 FITTED ON 1602

Fig. 6-2 Attenuator Circuit Diagram



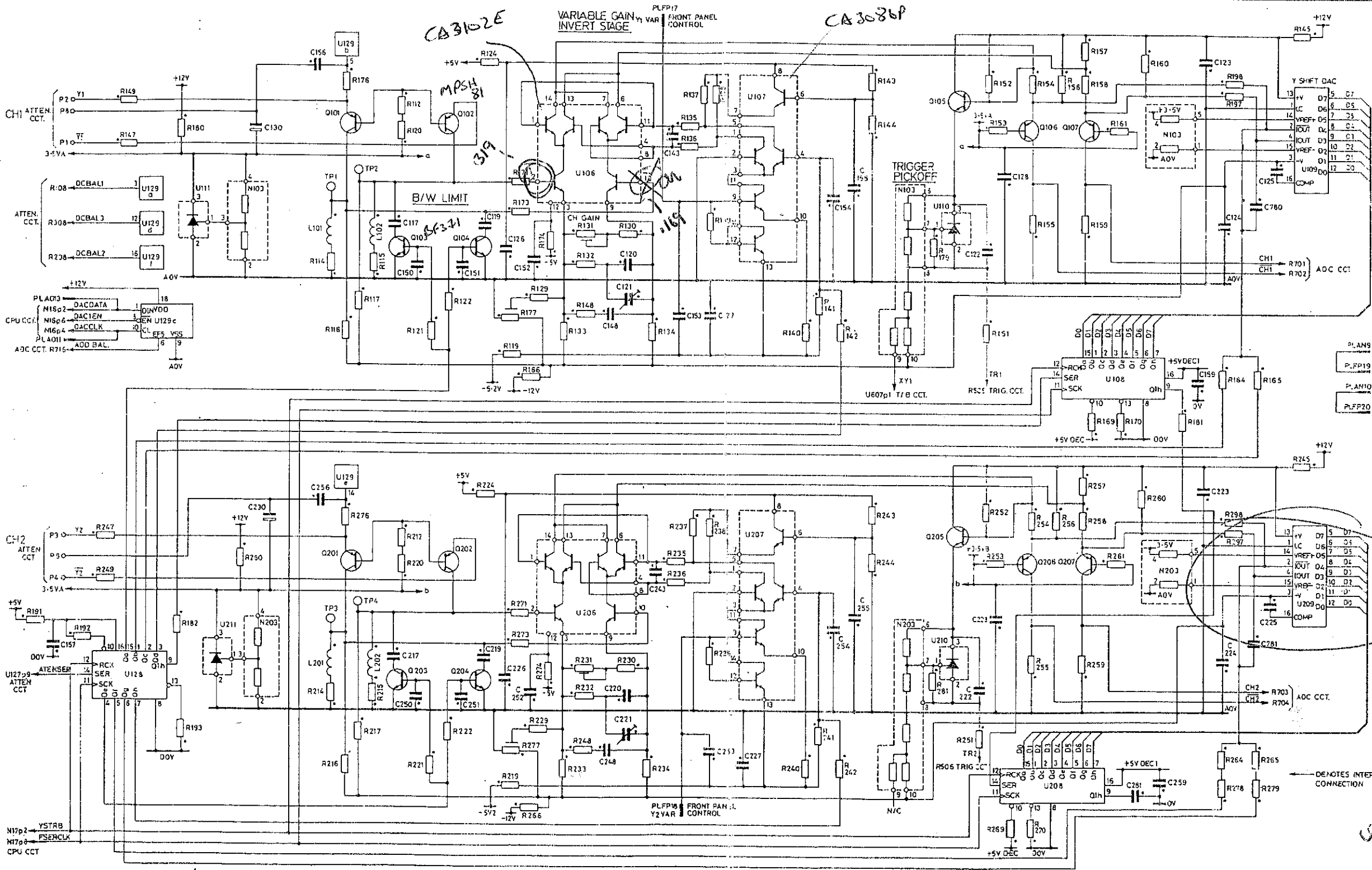
CIRCUIT OF SIDE 1 (TOP)

CIRCUIT OF SIDE 2



PIN 1

RES.	R149 R147 R217 R213	R180 R182 R193	N103 R280 N203	R114 R216 R217 R215	R116 R217 R215	R117 R218 R221	R115 R217 R221	R112 R120 R121	R122 R224 R227 R273 R219	R124 R173 R177 R176 R119 R229 R233 R231 R232 R248	R129 R133 R131 R132 R128 R236	R130 R134 R135 R137 R136	R140 R141 R142	R143 R144 R243 R244	N103 N203	R179 R281	R152 R153 R151 R252 R253 R251 R257	R154 R155 R156 R159 R257 R258 R259	R157 R161 R169 R170	R160 R260 N203	R198 R197 R154 R165	R199 R264 R265 R278 R279	R165 R265 R279	R145 R215		
CAPS.	C157	U106 U129a,c,d,f	U111 U211	C130 C230	C156	C117 C150 C151 C19	C217 C250 C251 C219	C103 C102 C104	C122 C252	C120 C14 C121 C248 C220 C221	C154 C143 C253 C243	C177 C227	C154 C155	C222 C228	C122 C128	C206 C107 U108	C281 C259	C123 C124 C780 C125	C224 C224	C781 C225						
MISC.	U206 U129	U106 U129a,c,d,f U111 U211	U101 Q201 L201	Q101 U129b L102	Q103 Q203	Q102 Q202	Q104 Q204	U106 U206	U107 U207	U105 U111 Q205 U210	Q106 Q107 U108	Q206 Q207	U208	U209	U209											



2 = -4  
4 = +0.24

100%  
FR  
DIL

12.0 ✓  
0 0 X

U206  
1 + 2.36  
2 - 0.518  
3 - 1.08

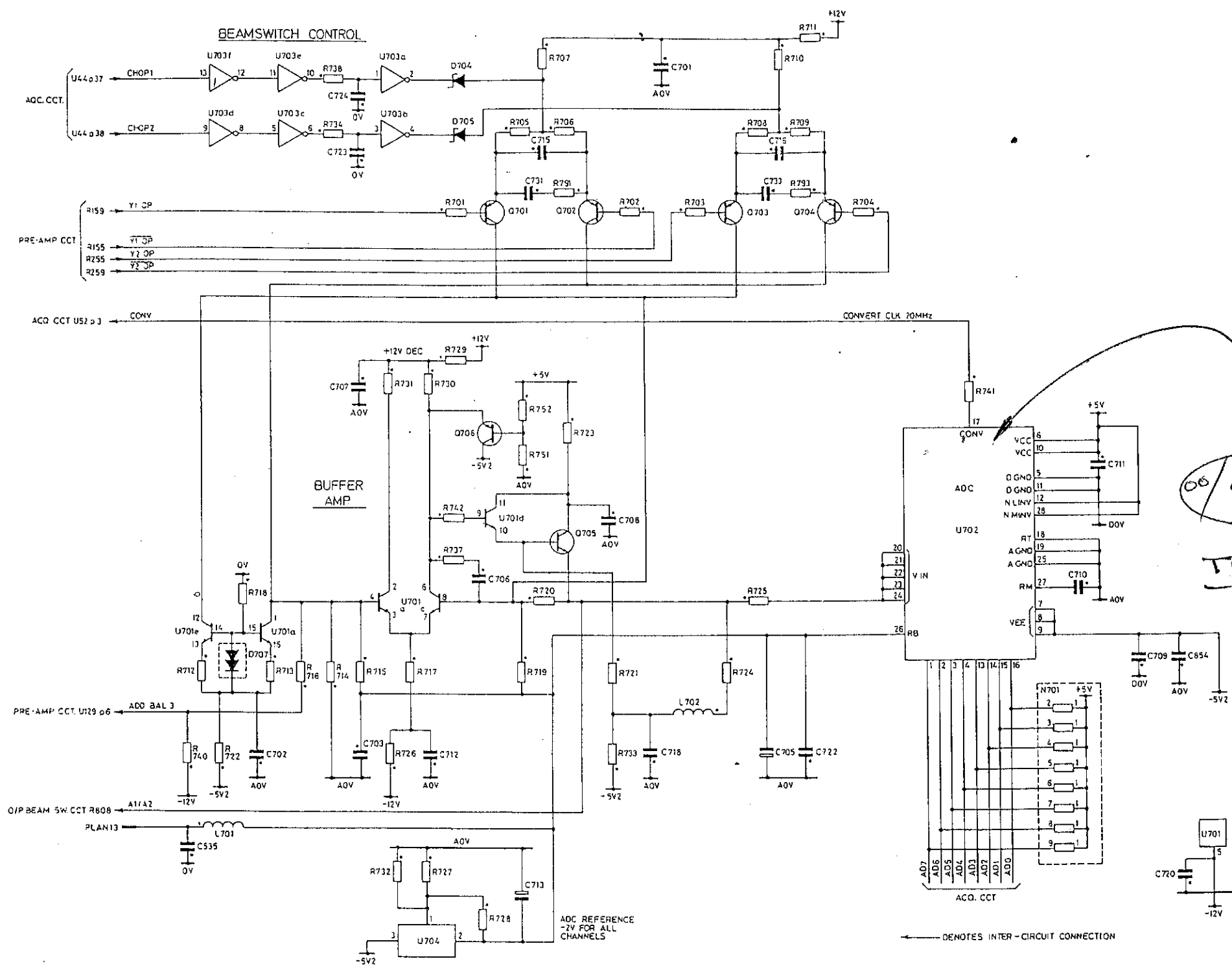
8 + 2.57  
9 - 0.95

U106  
1 - 2.79  
2 - 1.096  
3 - 0.87

8 + 2.59  
9 - 0.87  
12 - 1.098

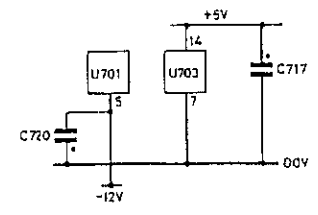
Fig. 6.4 Pre-amp Main Board

RES.	R712 R740	R718 R713 R716 R714 R734	R738 R715	R731 R717 R728 R727 R731	R701 R729 R730 R742 R757	R705 R752 R791 R751 R720 R728 R719	R706 R791 R773	R702 R721 R733	R701	R708 R724 R725	R710 R711 R709 R713	R704	R741	N701		
CAPS.	C535	C702	C707 C703	C724 C723	C712	C706	C731 C713	C708	C701 C718	C733	C716 C705	C712	C711 C710	C709	C854 C720	C717
MISC.	U703d,f D707 U701e L701	U703c,e U701a	U703a,b U701b,c	U704 D705 U701d	Q701 Q706 U701d	Q702 Q705	Q703 Q704	Q704 Q705	Q701 Q702	Q703 Q704	Q703 Q704	Q703 Q704	Q703 Q704	Q703 Q704	Q703 Q704	Q703 Q704



00/455,496

TOC 1048  
(TRW 1048) 2x SPARES.



← DENOTES INTER-CIRCUIT CONNECTION

Fig. 6.5 ADC Beamswitch Main Board

RES	R850	R802 R803	R876	R806 R836 R847 R848	R804 R844 R851	R807 R808	R843 R850	R809 R875 R842	R842	R846 R837	R874 R834	R857 R871 R842	R835	R811 R873 R838	R301	R881 R841 R840 R864	R827 R826 R870	R820 R828 R884	R880	R813 R829	R814	R883 R856 R815 R862	R821 R818	R816 R832	R822	R817 R824 R825	
CAPS	C811		C827		C817		C809	C810			C840	C820	C818 C806	C352	C821 C850 C828 C805	C801	C851		C814	C815	C804	C813			C816		
MISC	U804a,d	U804b,c	U803	U802d,e	D804		Q813	U802a,b	D810			U801c	U802c	Q816 Q815	Q812		Q803	Q814			U801a,b		U817		U801e		U801d

BEAMSWITCH BETWEEN CH1/CH2, CH3/CH4 DIGITAL Y

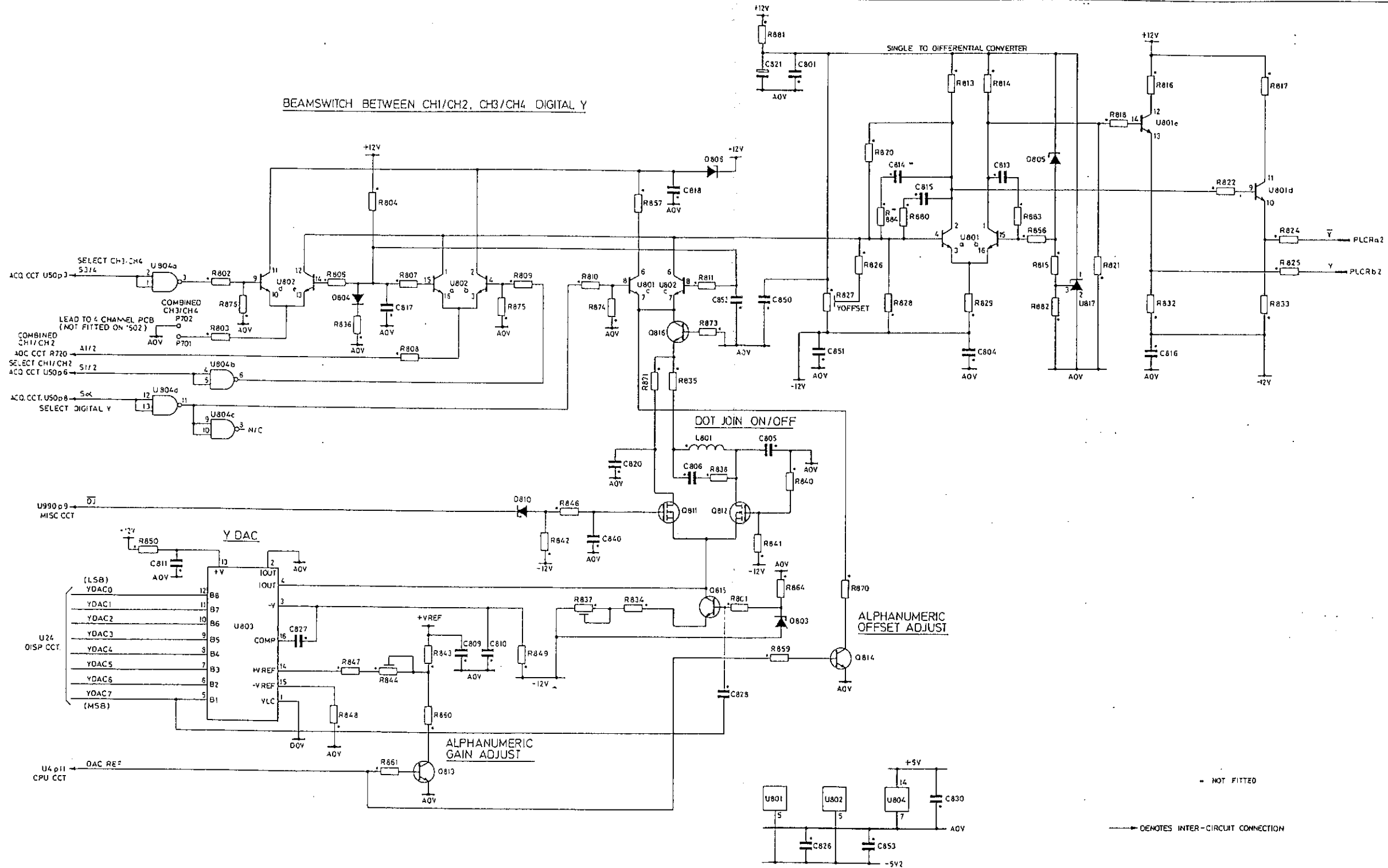


Fig. 6.6 O/P Beamswitch & Y-DAC

RES	R530	R514	R515 R516	R518 R517	R504	R519 R503	R523 R527 R564 R520 R505 R507 R501 R502	R525 R512	R528 R511	R510	R533 R566	R534 R535	R556	R524	R577 R537	R538 R539	R579	R541	R542	R559 R560 R552	R540	R544 R543	R584 R571 R569 R567 R578	R546	R565 R549	R583 R582 R581	R561 R562	R529 R585	
CAPS			C541	C516 C503 C502	C528	C517	C501	C520	C519 C508	C505 C507	C540 C590	C504 C551	C518	C513					C500 C527			C523 C531 C524 C553	C552	C545			C521		
MISC	Q506	Q502	D503	U512a			Q507 L502		Q507 U503 L504		L501		C510	C512	C511	C526		Q508	U504a U505 U508			U510c,d Q505	C542	C543	C545		U511a,c Q511 U509		U505b U502b

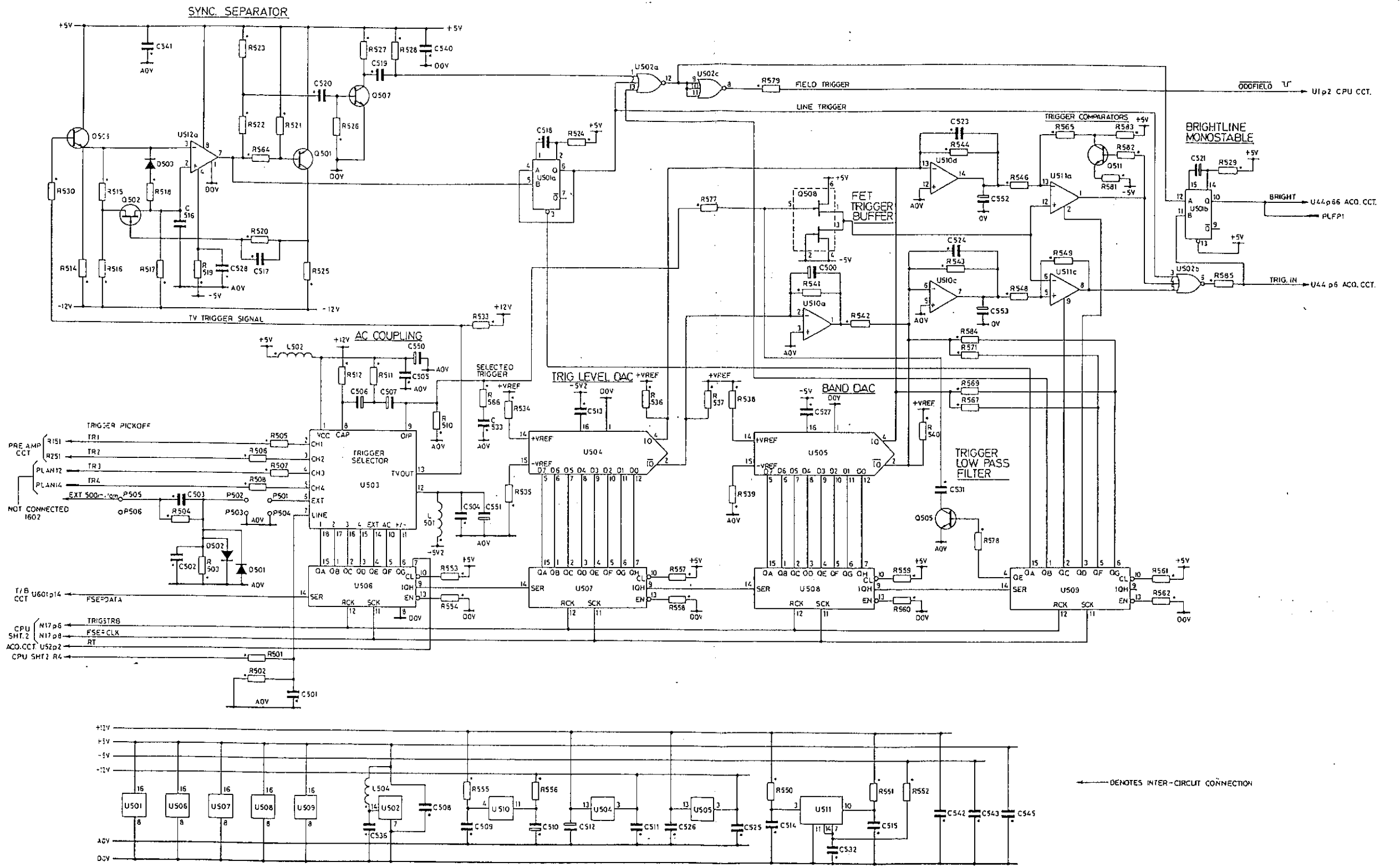


Fig. 6.7 Trigger

RES.	R175	R663	R643	R646	R650	R645	R602	R620	R623	R661	R660	R626	R662	R625	R627	R615	R609
	R612	R611	R640	R673	R674	R643	R644	R610	R631	R621	R632	R622	R603	R604	R670	R671	R605
	R601		R675	R672	R677	R648	R634	R653									R608
				R602	R636	R635		R654									R606
CAPS.		C511	C609	C620	C601		C610	C619	C611	C612	C613		C608	C610	C632	C603	C607
				C601			C622			C621	C614	C605		C610	C632	C603	C604
				C601							C615	C616			C602		C604
MISC			U603	U605c		O601	O601	O601	O602	O603	O603	U605a	D602		U606a		U9401
			U601			U605b,d			U609			U607a	U602	U604	L602	O620	L601
														Q605		U607	

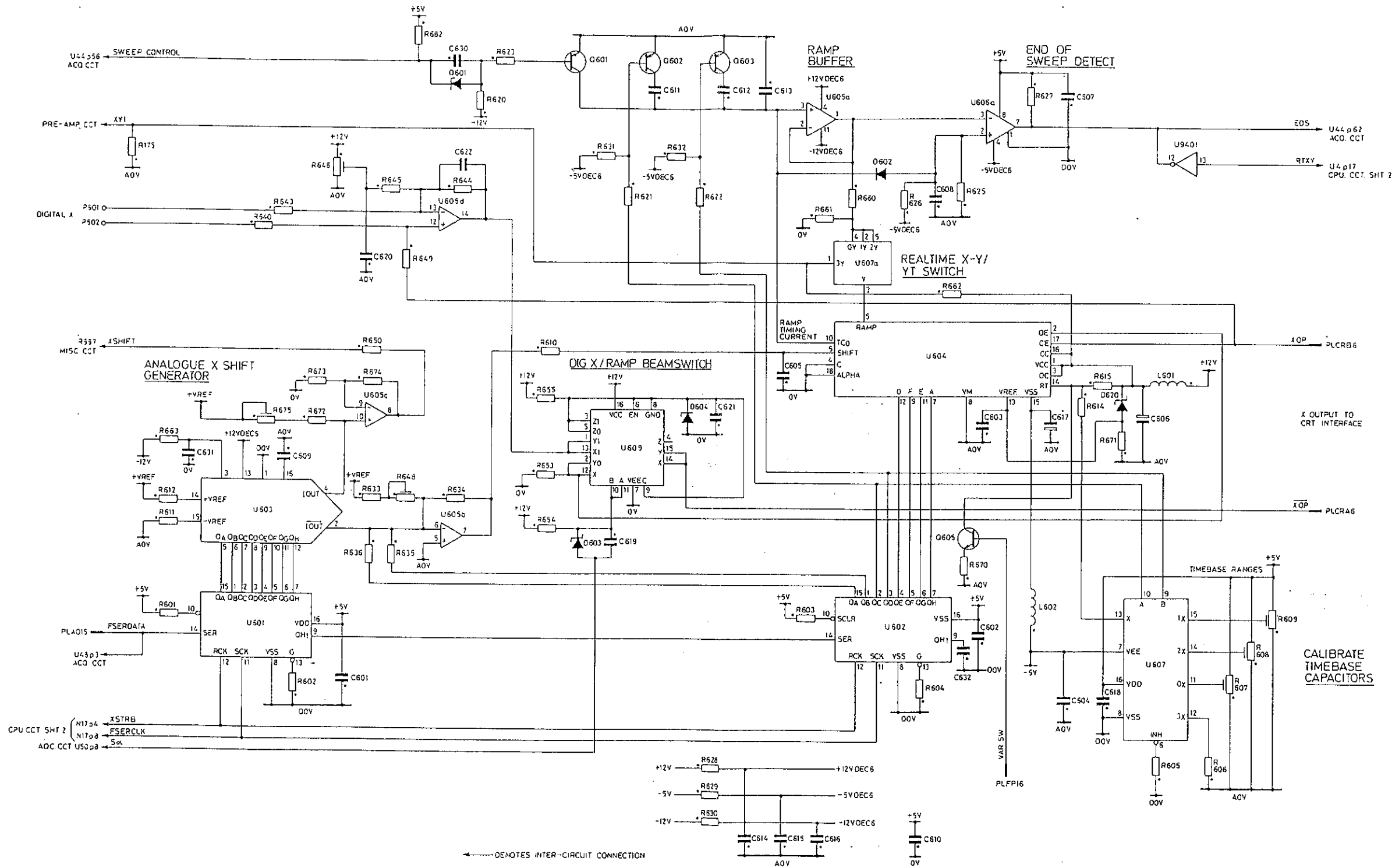


Fig. 6.8 Timebase

RES	R971 R973 R974	R975 R976 R977	R911 R912	R913	R970	R902	R914	R922 R930	R915	N905 N906	P920 R933	R991 R990 R923 R997	R959 R963 R964	R960	R954	R961	R996 R968 R967	R955 R953	R956 R952	R999 R958 R957 R951 R950 R969	R946 R947	R948	
CAPS			C951 C960	C925	C934 C935 C936 C937	C926 C927	C901		C929	C930		C932 C933 C953 C954	C950 C989		C944	C945	C948		C956 C949	C939	C990 C998	C952	C993
MISC	U28a,3,d U942c,3		U336 U337		U930		U933a,c U934a,c	U990c	U933b,d U934a,d		U942c U990b U912 U919	D910 D911 U935b	U52c	U50d	U910a	U940e U903 U904 U905	O992	U910b	U940a,b,c,d	U938	O920	O905 D906	Q902

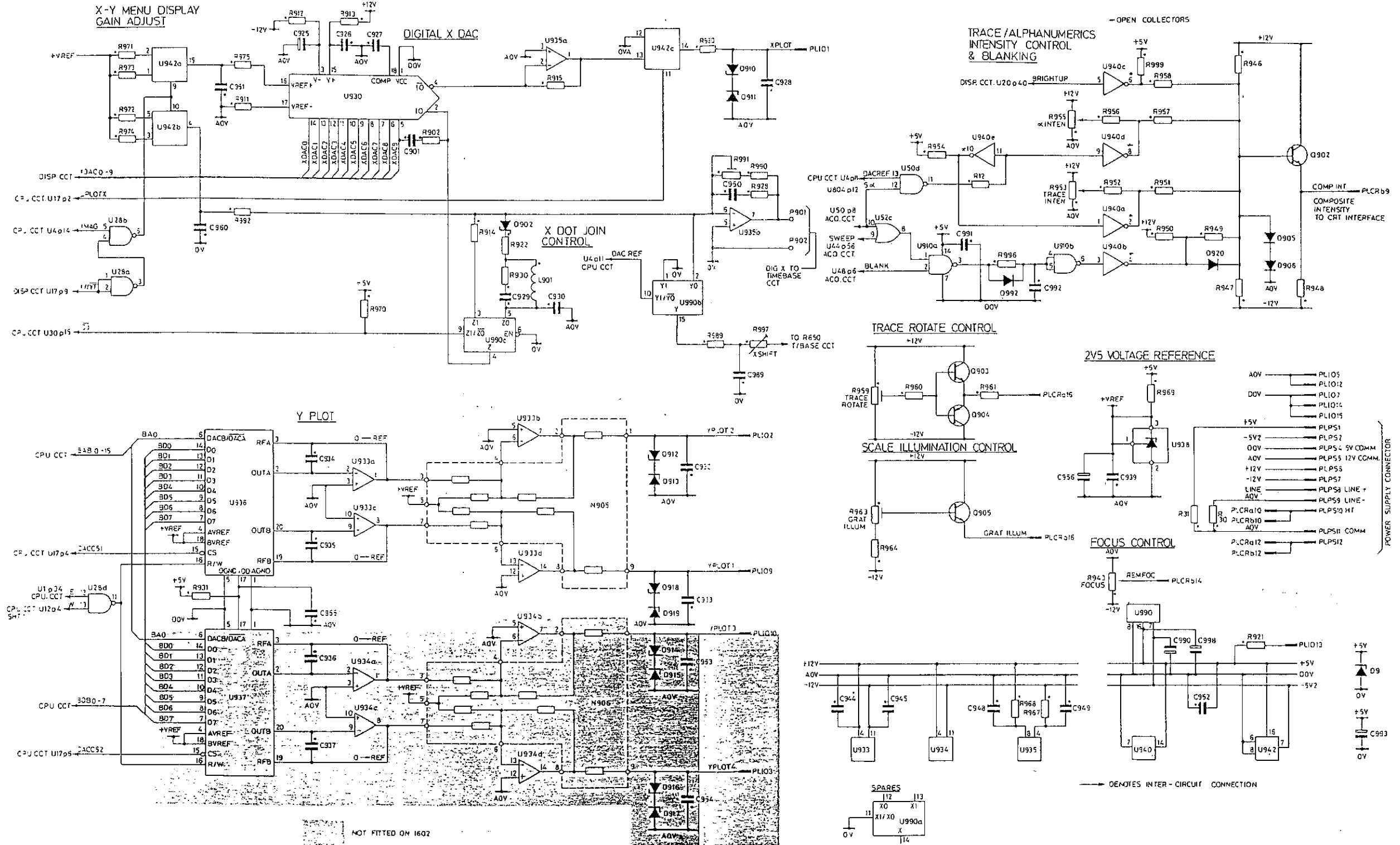


Fig. 6.9 Miscellaneous



RES.	N1 R11 R3	N2 R10	N10 N11	N1 N13	N2 R48	N15 N14														
CAPS.	C2																			
MISC.		U2 U9		U1	U3 U8	U13c U12b U12c	U29 U7			C30 C59										

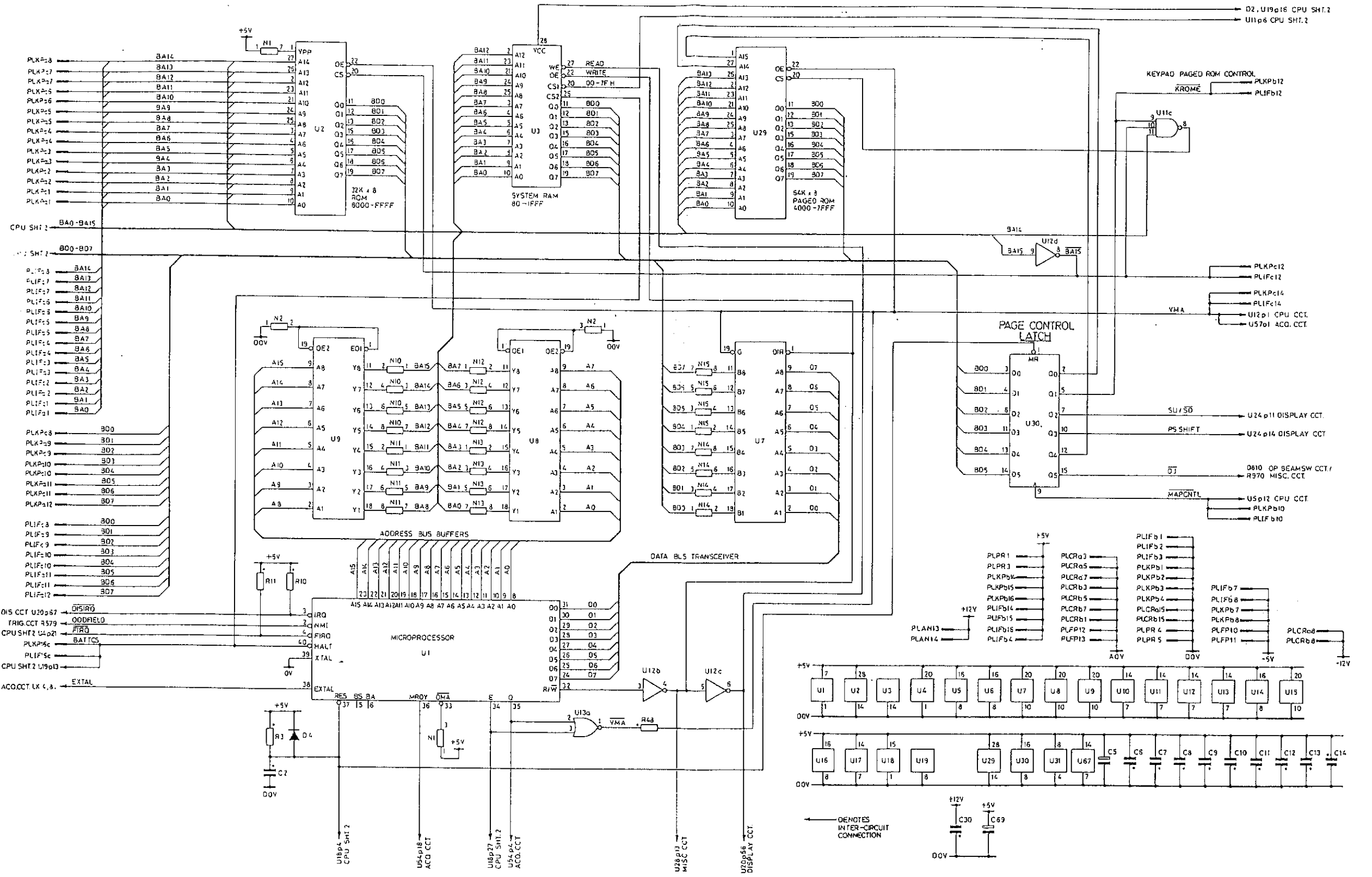


Fig. 6.10a CPU Circuit Diagram

RES.	R4	R23	N3	R5	R6	R20	R2	R1	R15	R18	R16	R17	R14	N1	R22	N2	N'	N2	N1	N2	R13	R21	N16	N17	R47											
CAPS.	C40C15		C1	C16		C17															C23															
MISC.	O5	O1	U19		O10	O7	O3	U10a, b, c		U13a	U13a	U13a	U13a	U18	U11a	U12a	U11b	U16		U15	U8	U5	U4	U67c	D20	O6	O2	O3	U141	U14a	U17a	U13b	U12e, f	U17b	U13a	U17c

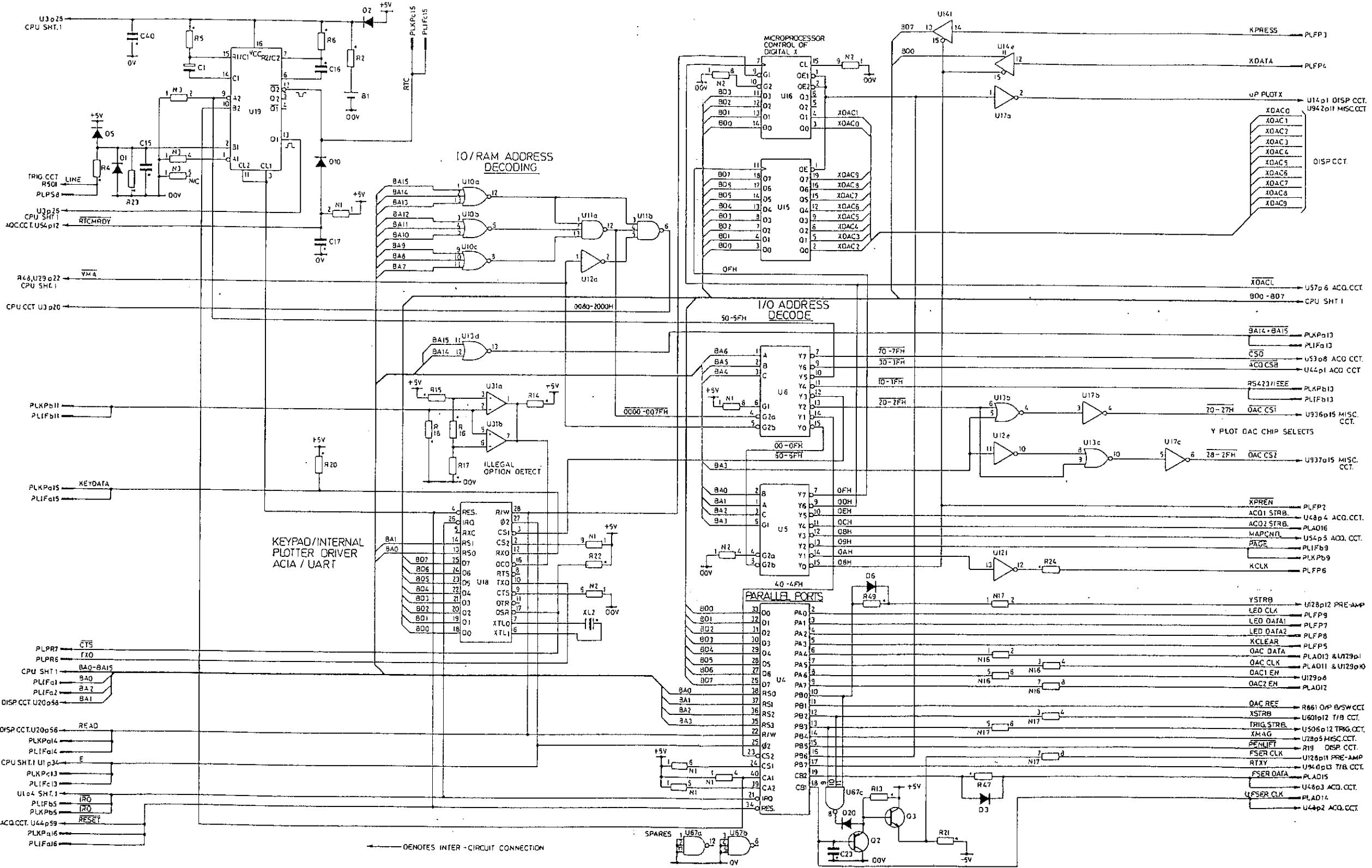


Fig. 6.10b CPU Circuit Diagram

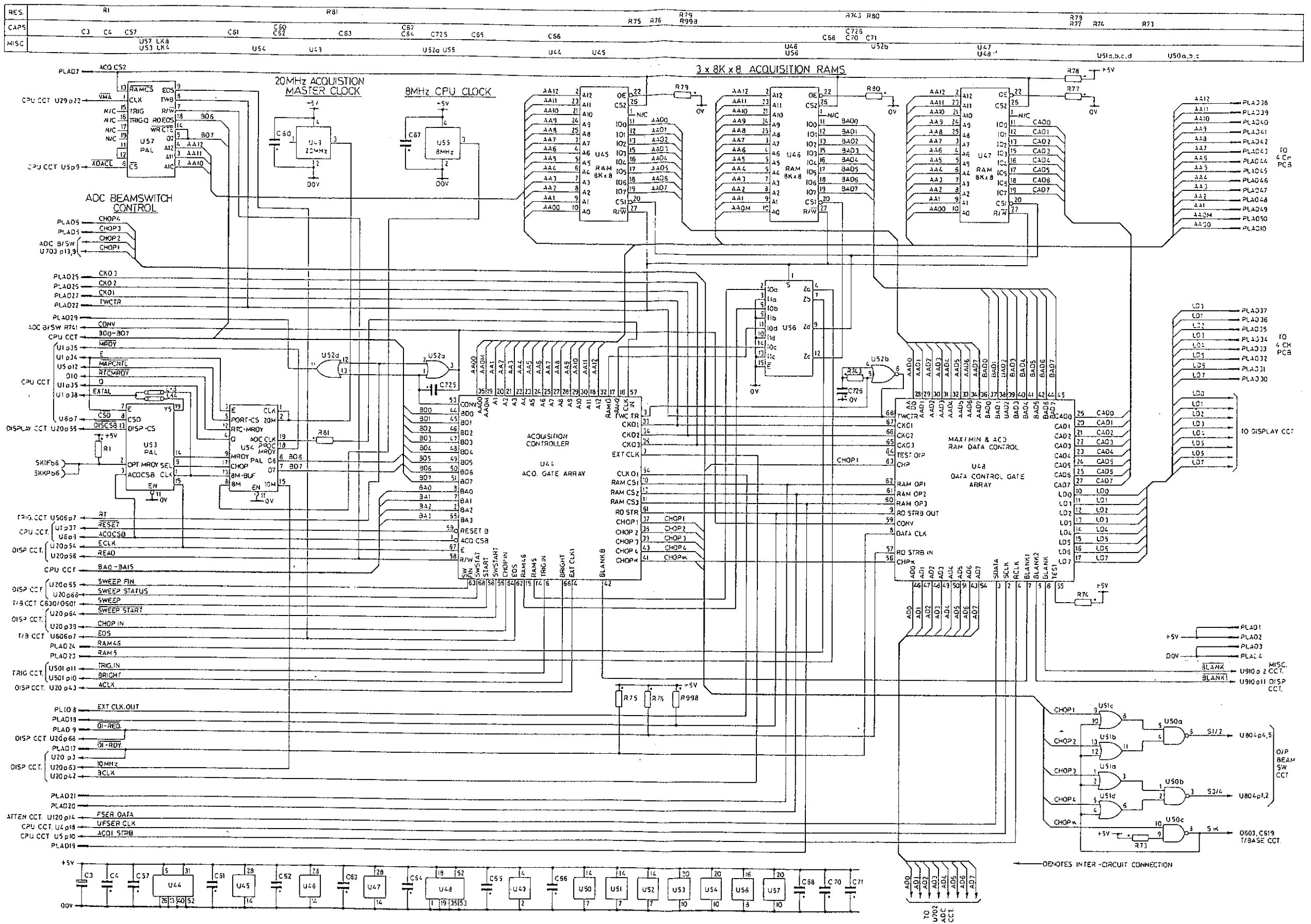


Fig. 6.11 Acquisition Main Board

RES.	R19	N4	R995	R901	R8	R900	N4	N4	N4	R7	R9						
CAPS.	C18	C19	C20	C994	C900	C21	C22										
MISC.	O1	RL1	U17e	U21	U20	U911a,b,U911	D901	D900	U17f	U28c	U27a	U25	U27b	U23	U17d	U24	U14a,b,c,d

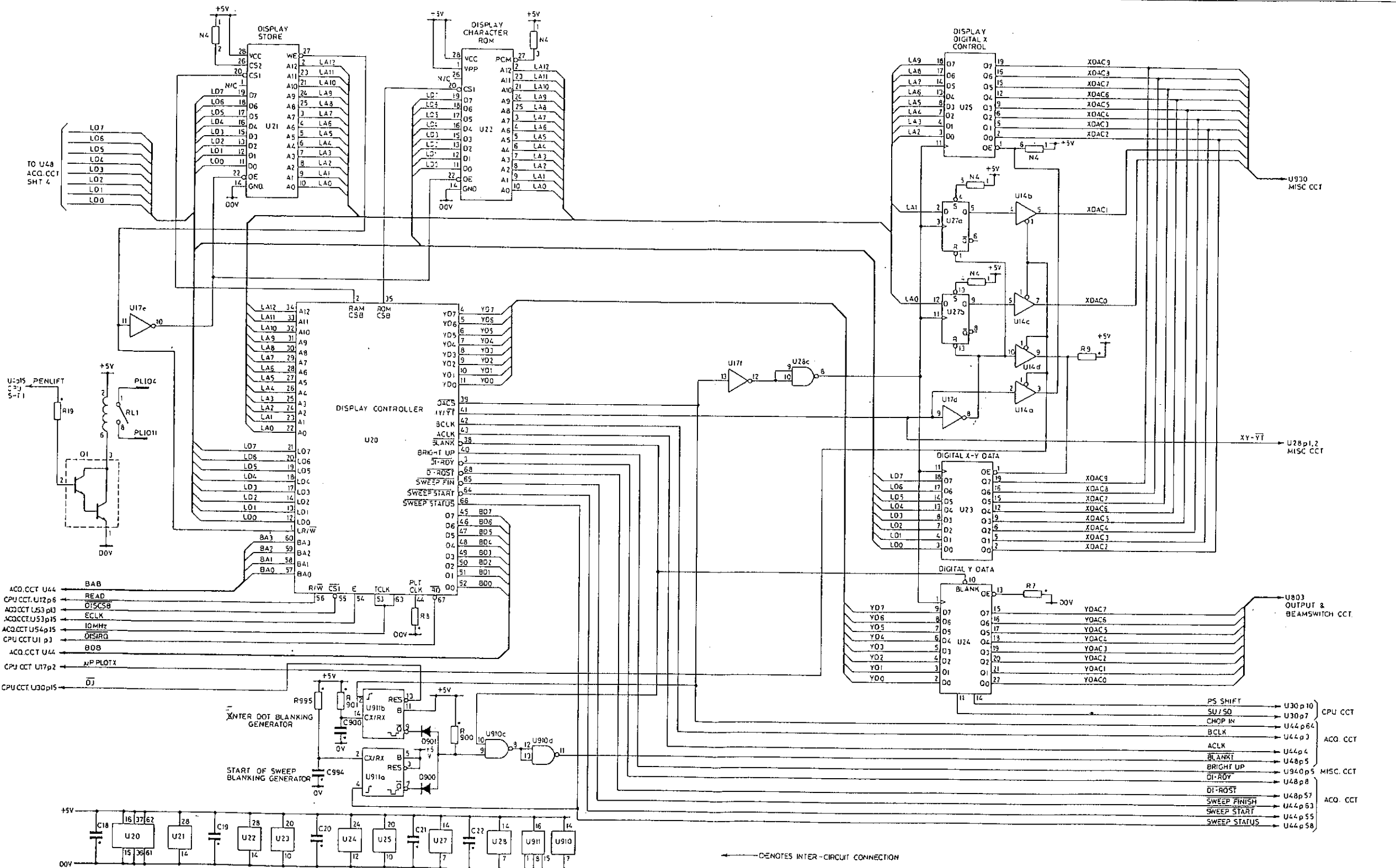


Fig. 6.12 Display

RES.	R149 R147 R249 R247	R180	N103	R175 R112 R115	R121	R122	R124 R171 R173 R177 R179 R183 R187 R188	R130	R134	R135 R137 R136	R138 R139	R140 R141 R142	R143 R144	N103	R179	R152 R153 R154 R155	R156 R157 R158 R159	R160	N103	R92	R194 R195 R196 R197 R198 R199 R200	R165	R145
CAPS.	C157	C56	C130	C156	C117 C250	C151	C119 C125 C252	C148 C120 C21	C143 C153	C243 C253	C22	C129	C254 C255	C222 C228	C127	C128	C129	C150	C123 C159 C213	C124 C224	C158 C258	C125	C225
IMSC.	U206 U123	U105 U129c,c,d,f	U111	L101 U129e L202	O103	O102 O203	O104 O204	U106	U107	U108	O105 U110 O205 U210	O106 O107	U109	O108	O109	U208	U207	U209	U210	U211 U210	U212	U213	U214

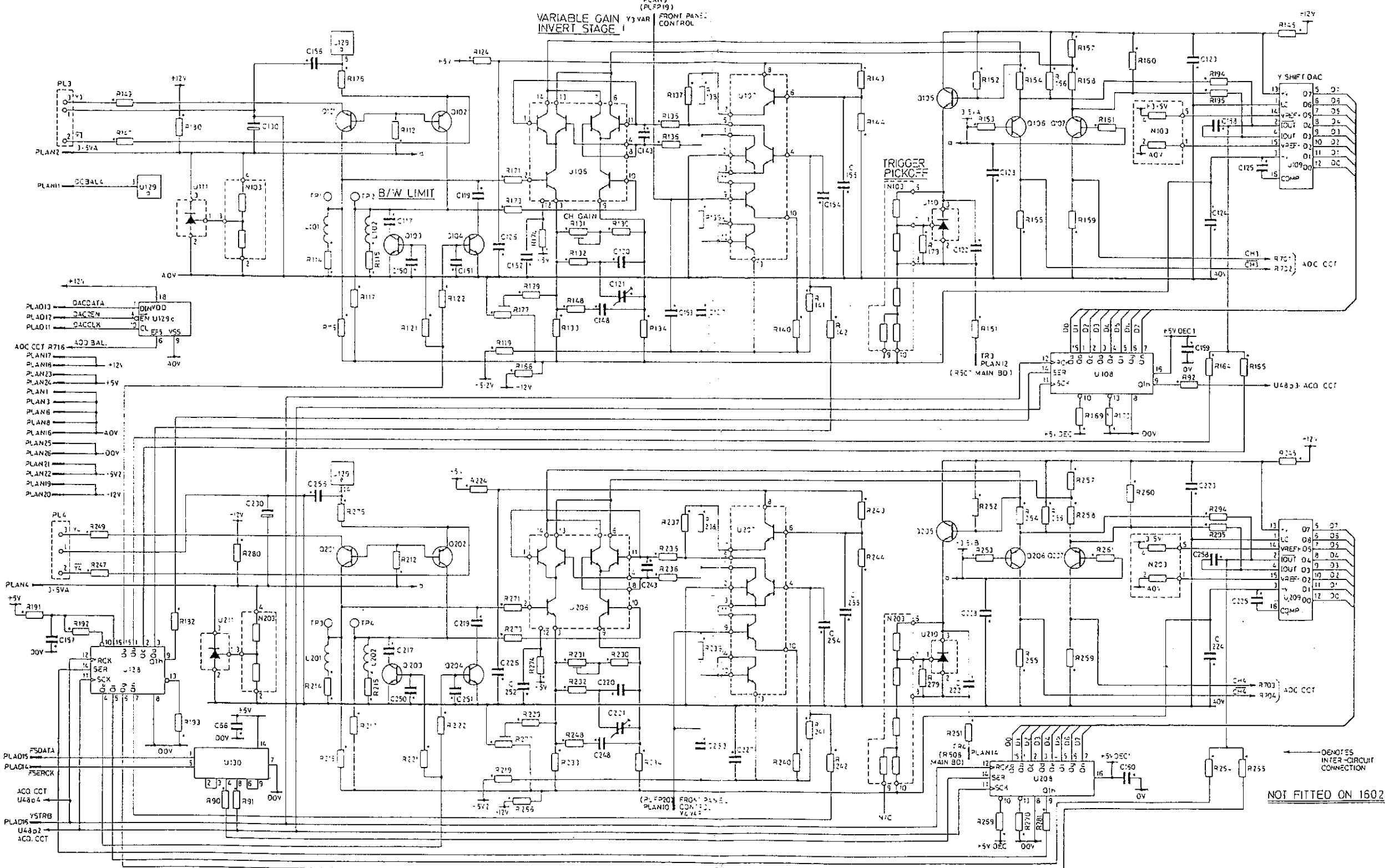


Fig. 6.13 Pre-amp 4 Channel Board

RES	R740	R738 R715 R714 R734	R715	R731 R717 R735 R727	R701 R723 R730 R742 R737	R705 R752 R791 R751 R723 R728 R719	R707 R706 R721 R733	R702 R721 R733	R703	R708 R774 R725	R710 R709 R793	R704	R741	N701	
CAPS	C535	C707 C703	C724 C723	C712	C706	C731 C713	C708 C718	C701	C733	C716 C705	C722	C711 C710	C709	C854 C720	C717
MISC	U703a U703b	U703c U703d	U703e U703f	U703g U703h	Q704 Q705	Q701 Q702	Q703 Q704	Q705	Q703	Q704	Q702	Q702	U702		

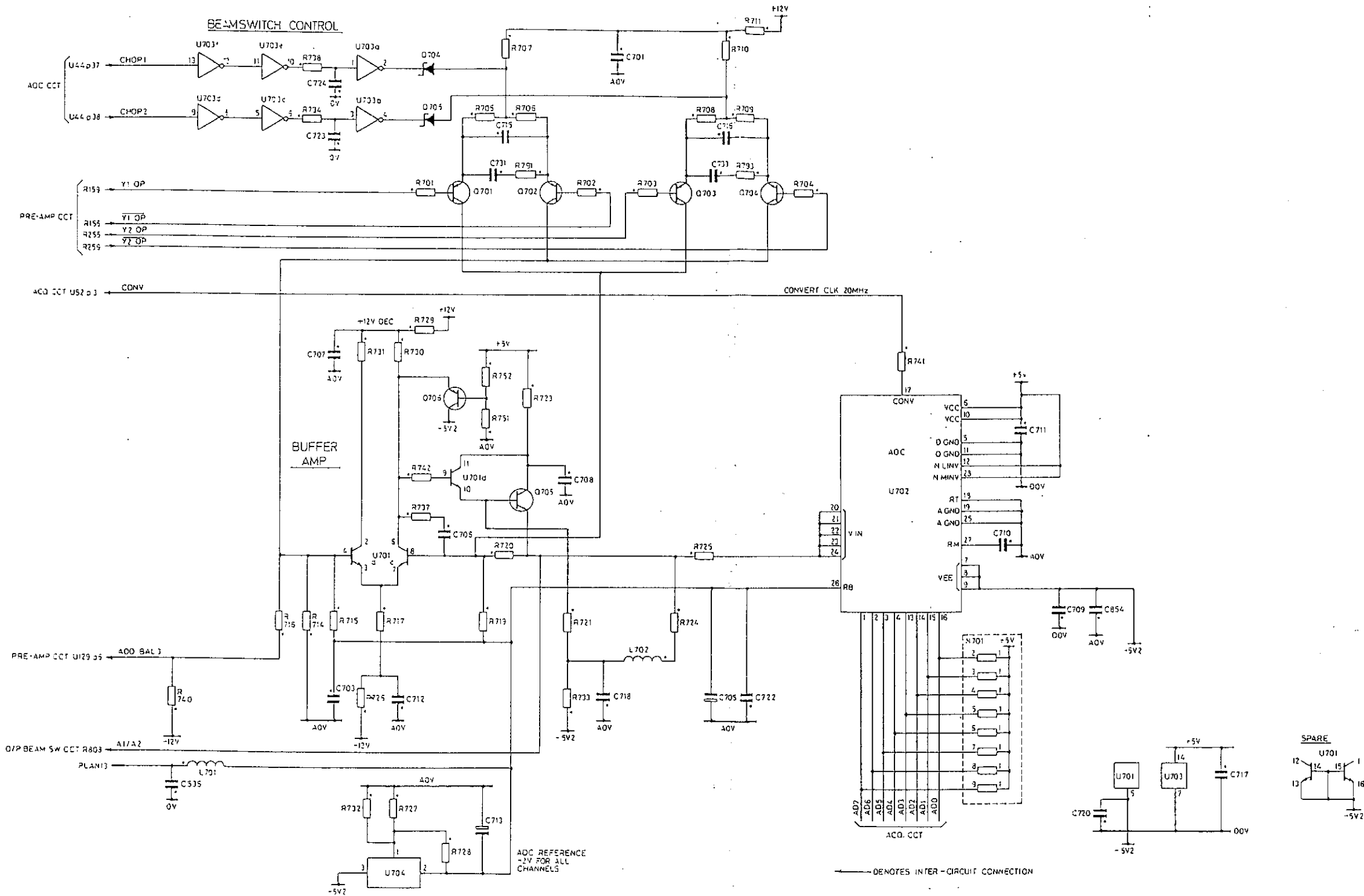


Fig. 6.14 ADC Beamswitch 4 Channel Board

RES				R72	R71	R70	R75	R79			R80	R74		R78	R77			
CAPS												C52	C63	C64	C65	C57	C58	C63
MISC					U45					U46	U43		U47					

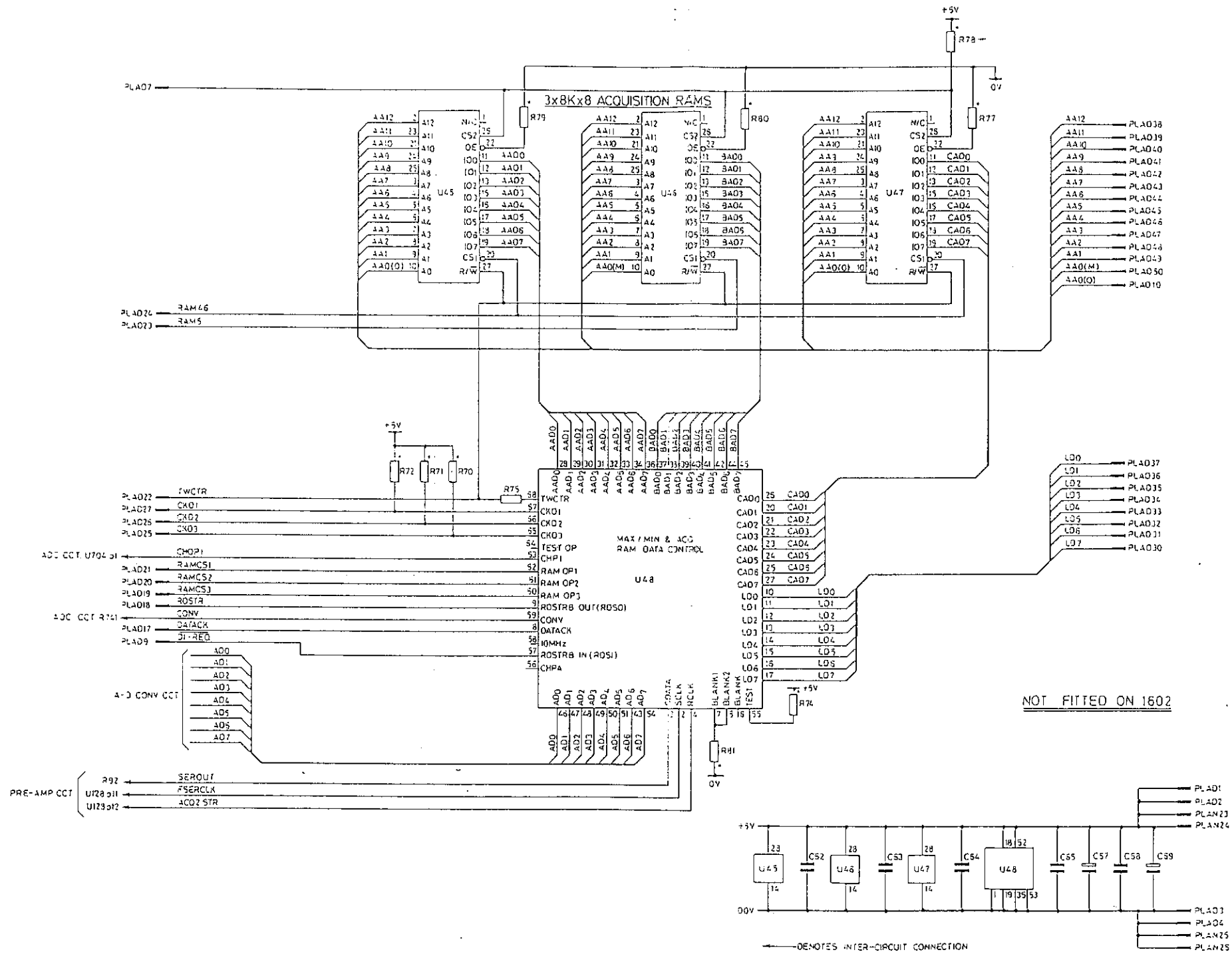


Fig. 6.15 Acquisition 4 Channel Board

RES.	R85 R90	R86 R88 R89	R87 R118 R112	R91	R92	R93	R94	R95	R103	R98 R97 R96	R104	R111 R99	R120 R121	R107	R102 R101 R108 R109	R110 R103	R119
CAPS.	C62 C63		C72	C60	C64	C65 C66		C67 C68	C53 C69 C54	C50	C51	C52	C70, C71				
MISC.		O15 D34	L1 D18 D16	O17 D17	O18	LK1 D19	T1 Q19	O20 O20	O21 O22	O24 O23	O25	MX6	O5		O27 D28 O30	O29 O30 O22	

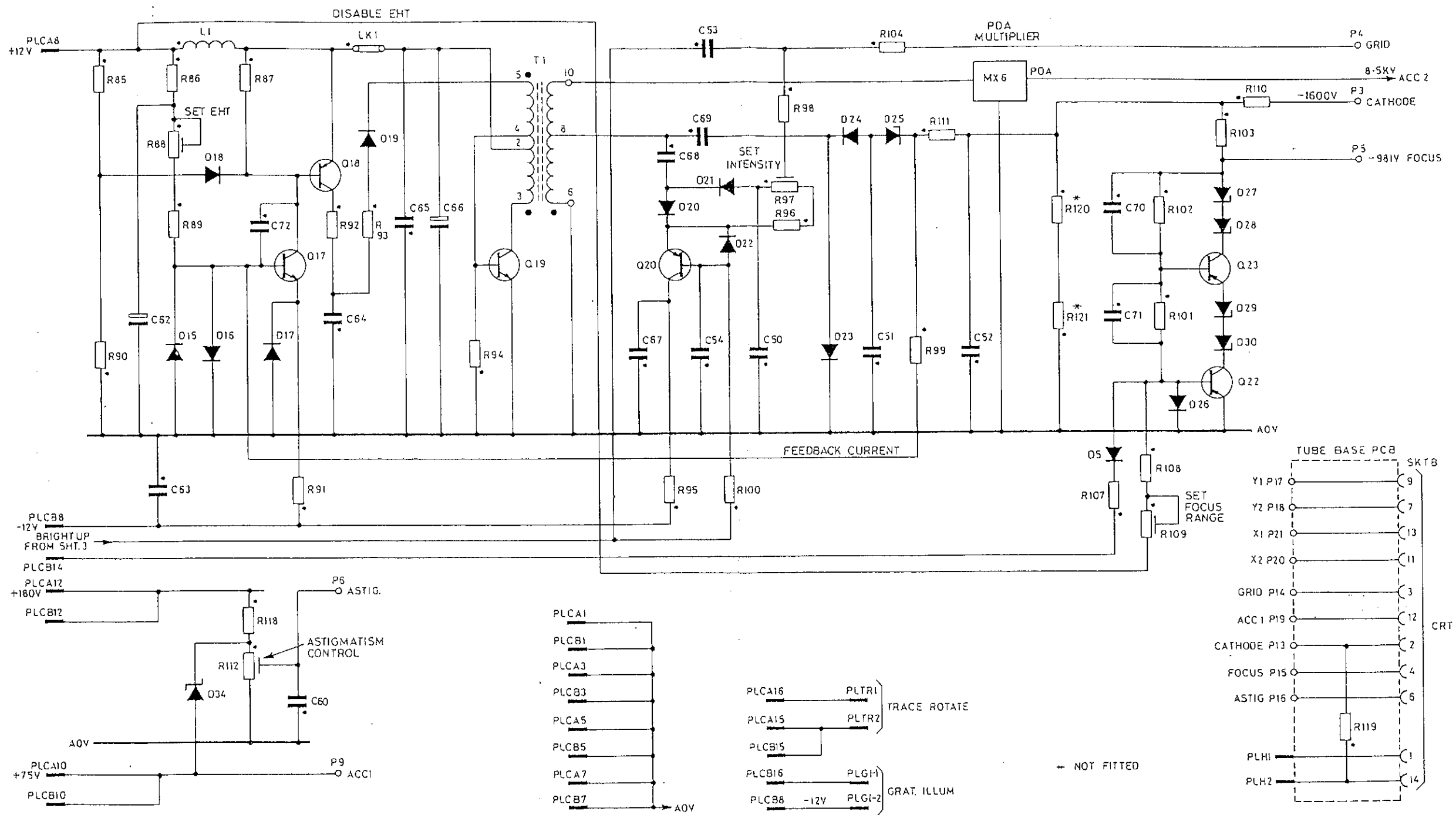
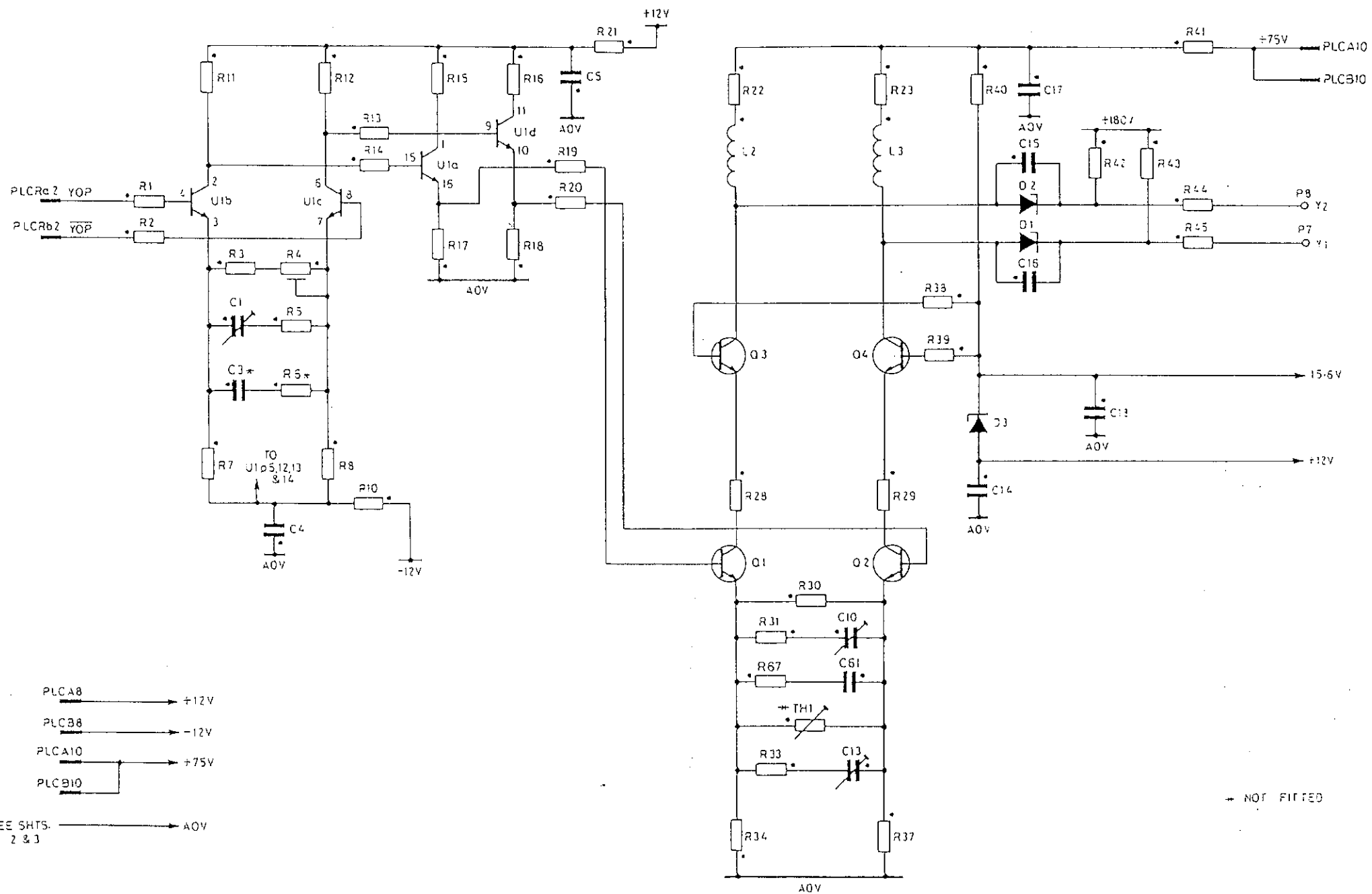


Fig. 6.16a CRT EHT Circuit Diagram



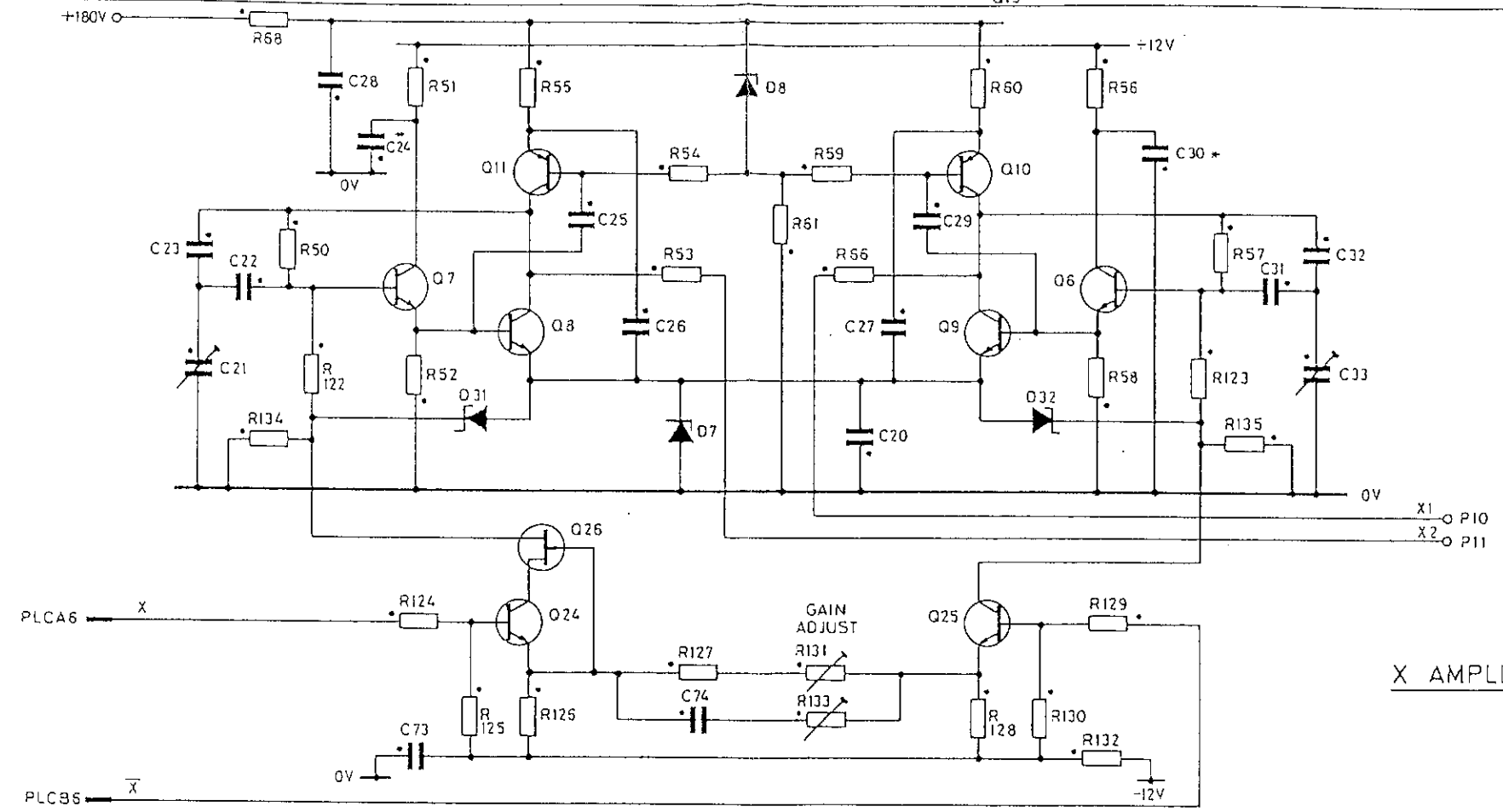
RES	R1 R2	R11 R7	R3 R6	R4 R5 R8	R12 R3	R13 R4 R10	R15 R17	R16 R18	R19 R20	R21	R22 R28 R34	R31 R57 R33	R30 TH1	R23 R29 R37	R38 R39	R40	R42 R-3	R41 R44 R45
CAPS.		C1 C3		C4				C5			C10 C61 C13			C14	C17 C15 C16		C18	
MISC.		U1b		U1c		U1a		U1d			L2 Q3 Q1		L3 Q4 Q2		D3	D2 D1		



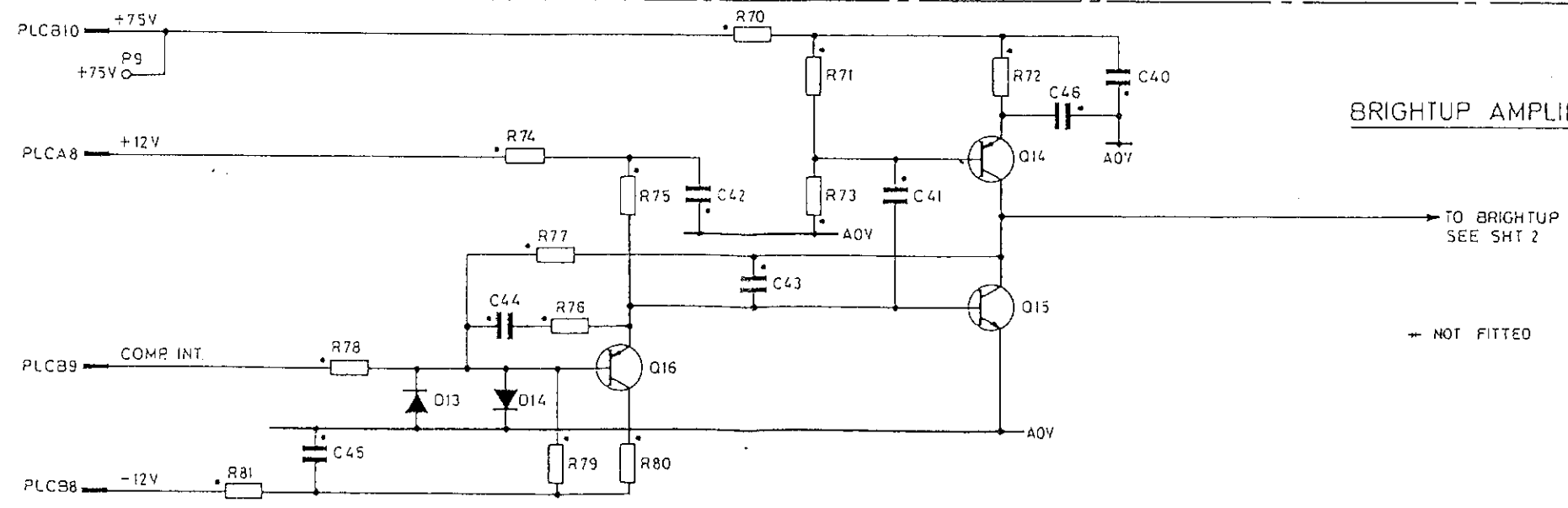
\* NOT FITTED

Fig. 6.16b Y-Amp Circuit Diagram

RES.	R68 R134 R81	R50 R122	R78	R51 R52 R124	R125	R55 R126 R74 R77	R76 R79	R75 R80	R54 R53 R127	R61 R70	R59 R131 R133	R66 R71 R73	R60 R128 R72	R130	R56 R58 R129 R132	R57 R123 R135	
CAPS.	C23 C21	C22	C28 C45	C24	C73	C44	C25	C26	C74 C42	C43	C20	C27	C29	C41	C46	C30 C40	C31 C32 C33
MISC.					Q7 D13	D31 D14	Q11 Q8 Q26 Q25 Q14 Q24	Q16	D7	D8			Q10 Q9 Q25 Q14 Q15	D32	Q6		



X AMPLIFIER

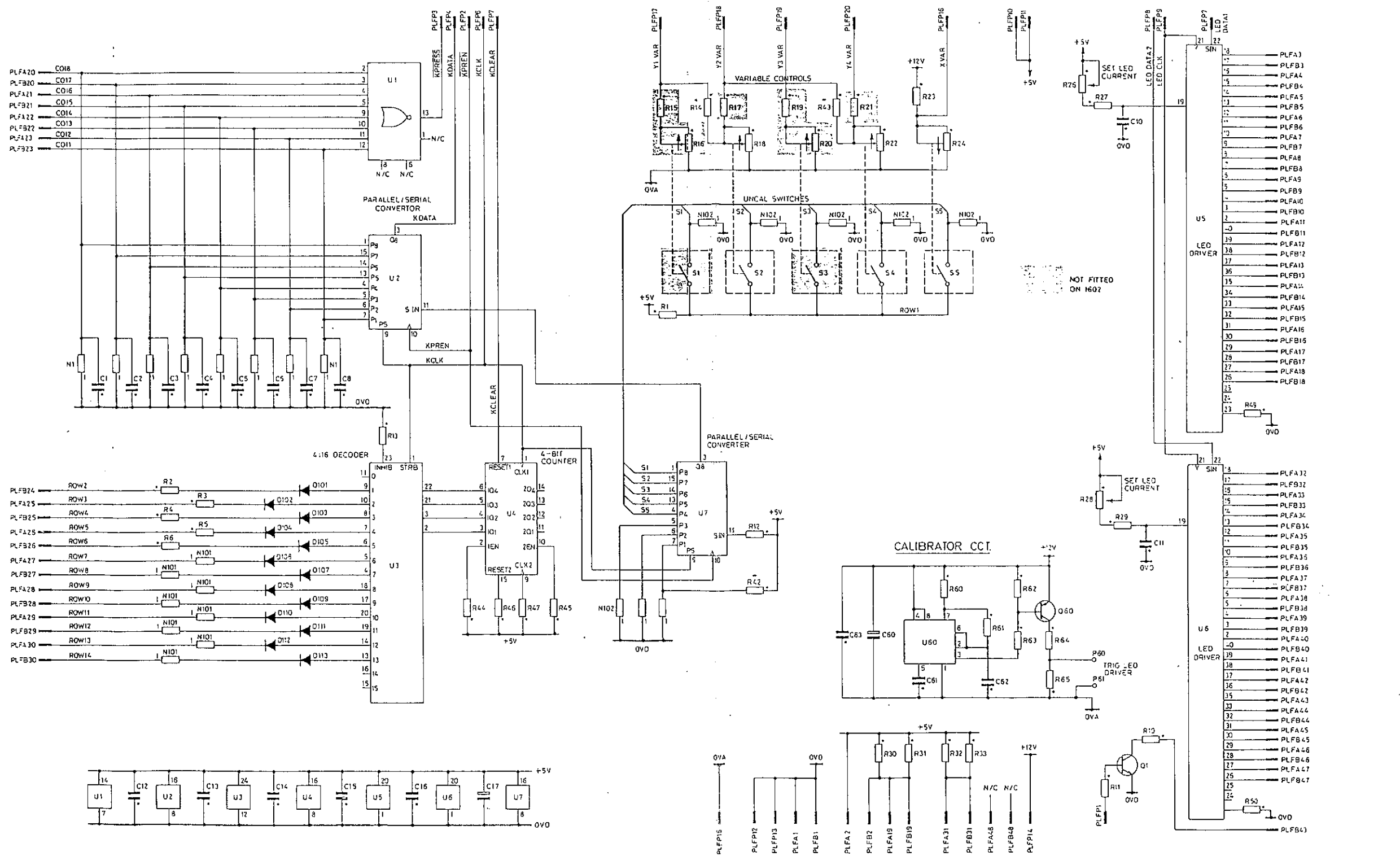


BRIGHTUP AMPLIFIER

⊛ NOT FITTED

Fig. 6.16c X-Amp & Bright-up Amp Circuit Diagram

RES.	N1	R2 R4 R6 N101	R3 R5 N101		R13										R15 R1	R16 R14	R17 N102	R18 R11 R42	R19	R20	R43 R21	R22	R23	R24	R60 R32	R33	R61 R62 R63	R64 R65	R26 R27 R28 R29	R11 R10		R49 R50
CAPS	C1	C2 C12	C3	C4 C13	C5	C6 C14	C7	C8 C15		C16	C17										C63	C60	C61		C62					C10 C11		
MISC							Q102 Q101 Q112 Q113	U1 U2 U3			U4			S1 U7	S2	S3	S4	S5									Q60	Q1		U5 U6		



550	551	560	554	56	514	070	522	530	538	07	071
552	553	562	559	57	515	R48	521	531	539	072	072
554	555	564	561	58	516		524	532	540	073	073
556	557	561	565	59	517		525	533	541	074	074
				60	518		526	534	542	075	075
				61	519		527	535	543	076	076
				62	520		528	536	544	077	077
				63	521		529	537	545	078	078
										079	079
										080	080

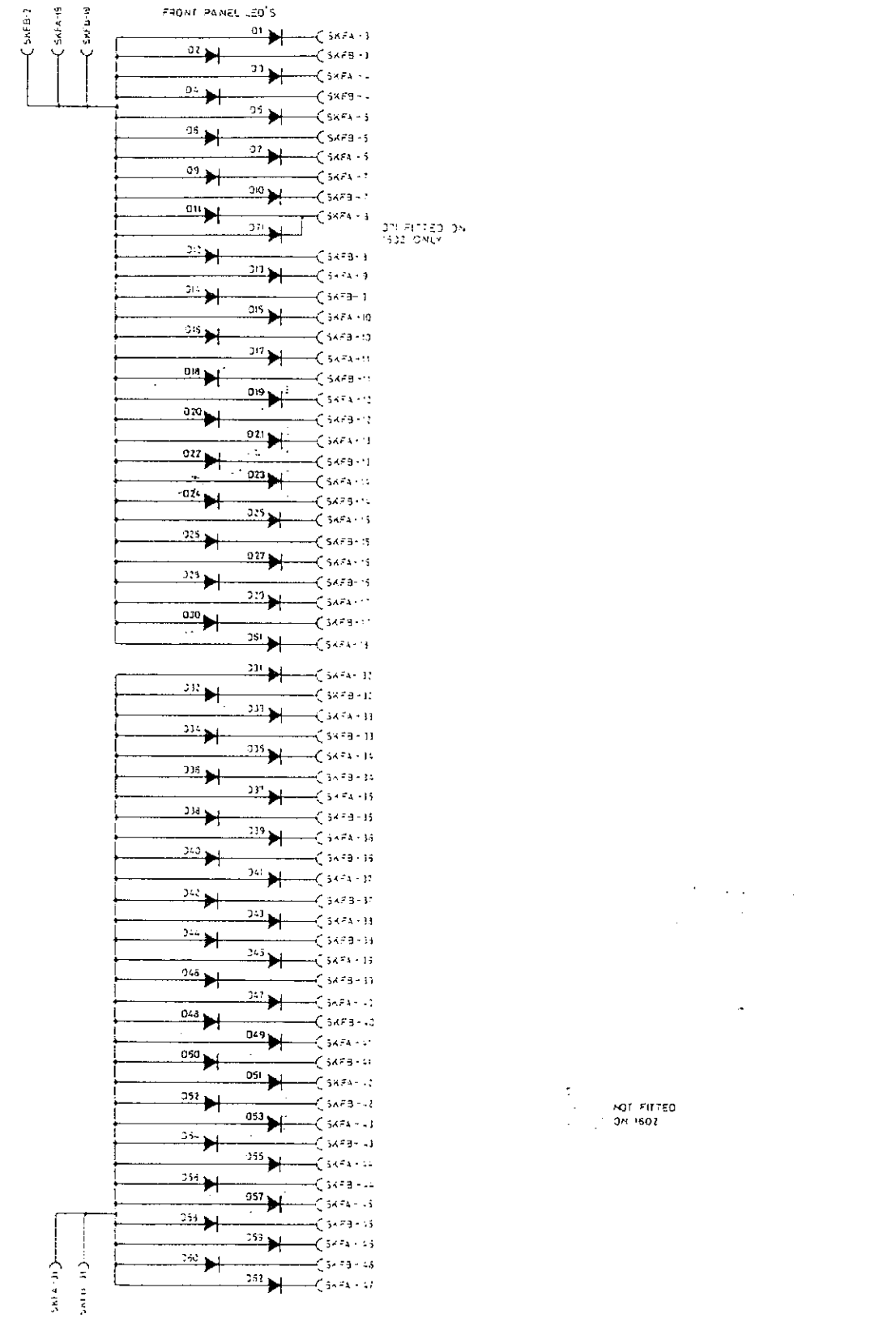
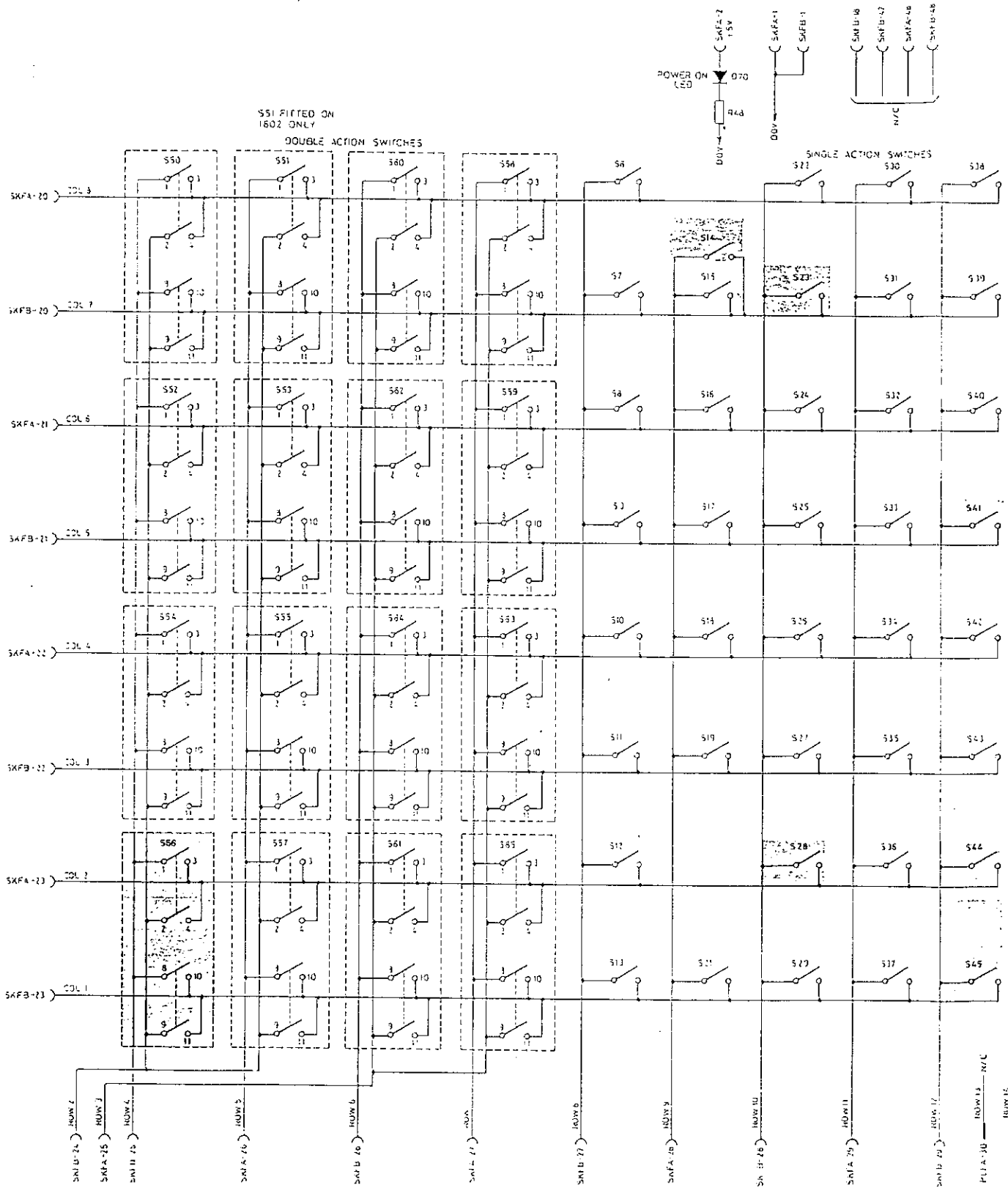


Fig. 6.17b Front Panel Circuit Diagram

RES	R19 R20	R13 R14	R8	R9 R15	R3 R4	R11 R7	R12 R7	R5 R6	R18	R1 R16 R2	R17	
CAPS.			C13 C6	C14 C20	C7	C3 C17	C9 C12	C23		C18 C10	C27 C23 C16	C11 C22
MSC.	F3 S1	T1	BR1 BR3 BR2	F2 F1	L2 U5 U4	Q2 Q1	U2 Q1		U1 U3	D2 L1		

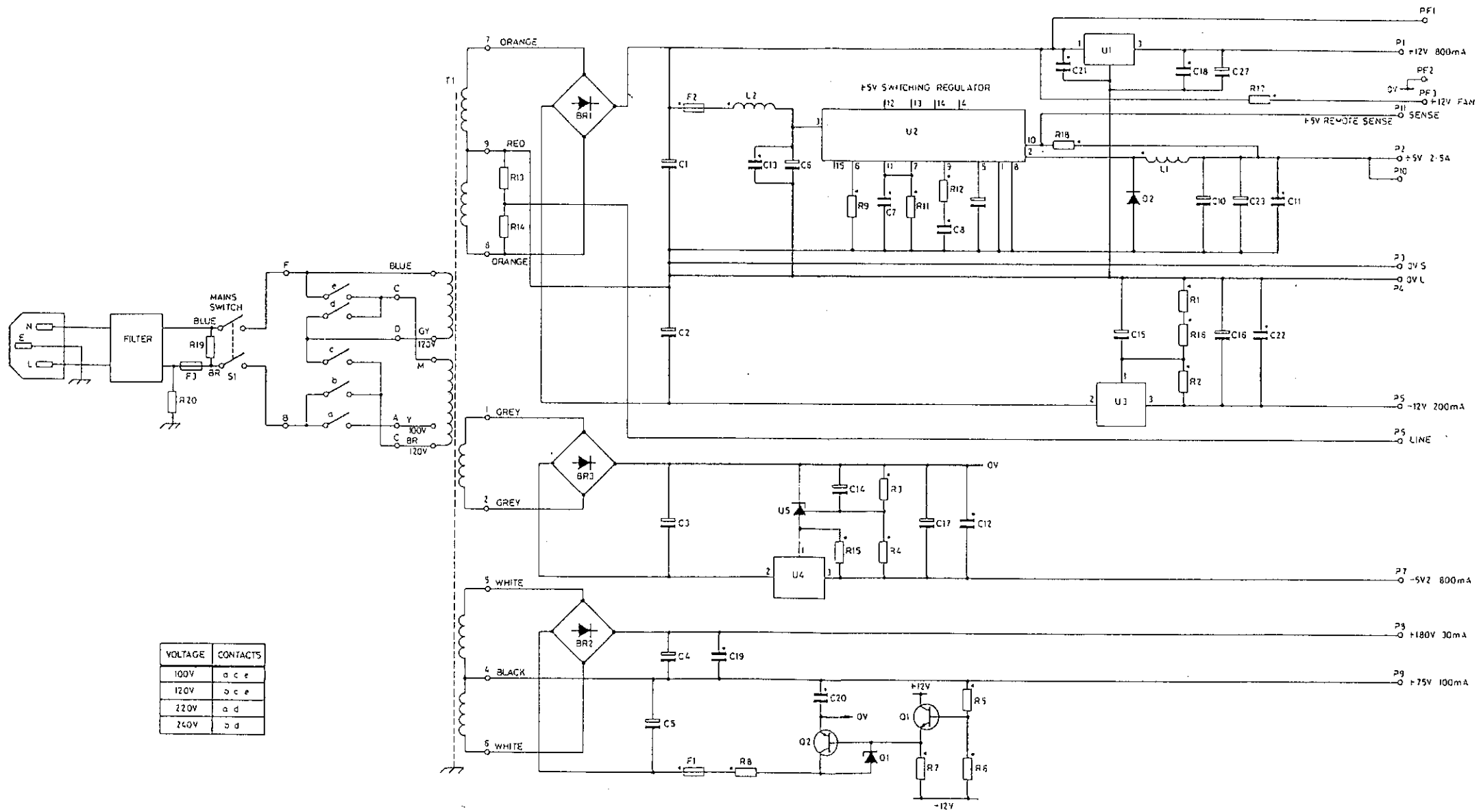
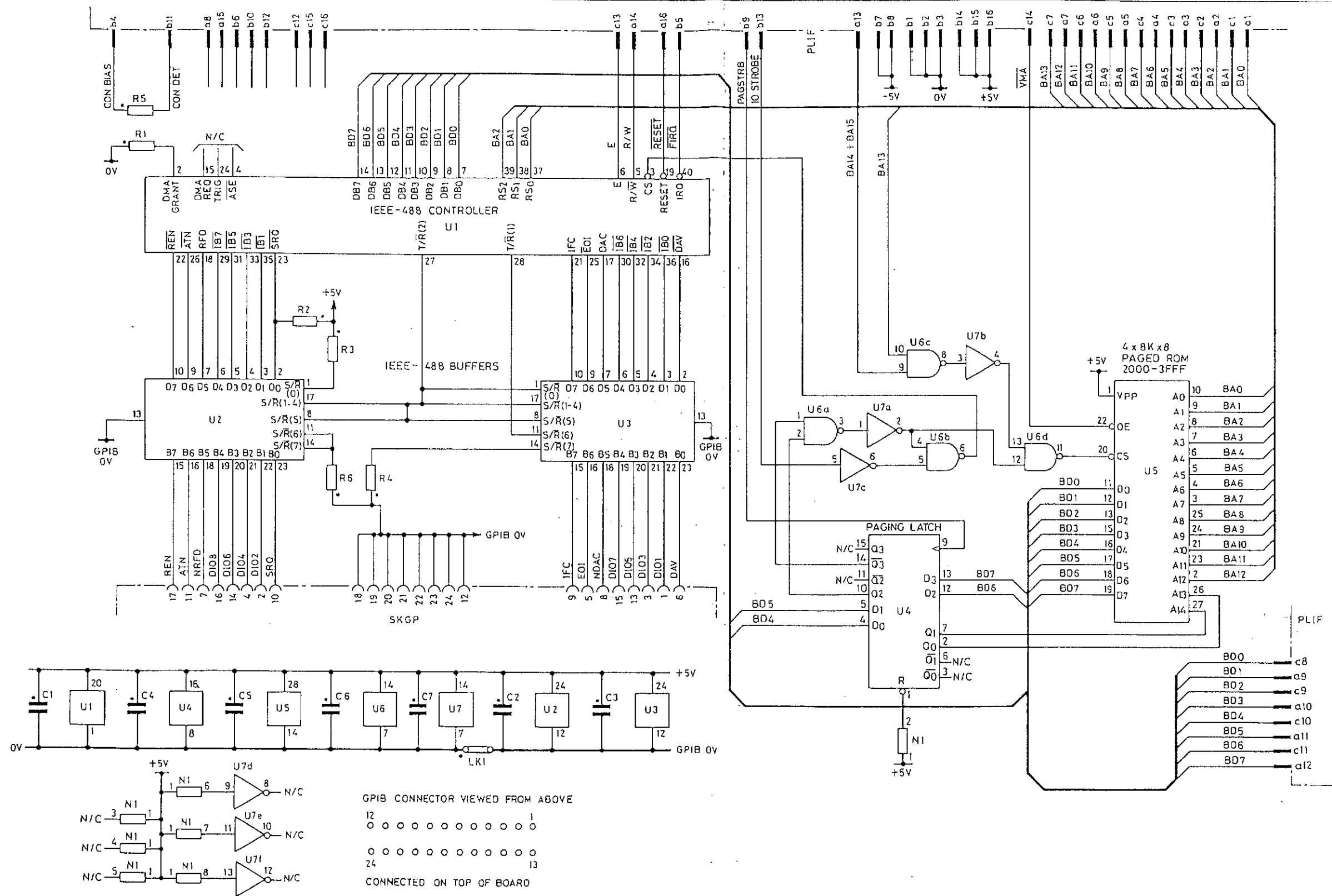


Fig. 6.18 Power Supply

RES.	R5 R1	N1	R2	R3 R6	R4	N1								
CAPS.	C1	C4	C5	C6	C7	C2	C3							
MISC.	U2		U7d,e,f		U1	U3		U6a	U7a,c	U6b,c	U7b	U6d	U5	



GPIB CONNECTOR VIEWED FROM ABOVE

```

12  O O O O O O O O O O O O
24  O O O O O O O O O O O O

```

CONNECTED ON TOP OF BOARD

Fig. 6.19 GPIB Option

RES.	R5 R5	N1 R10	N1 R11	R12	R13	R1 R3	N1	R4	R7 R8 R9	N1	R2										
CAPS		C10 C11					C1	C2	C3	C4	C5 C9	C6	C7	C8	C12	C13	C14				
MISC		XL1				U1	U3a	J5b	U3	U5c	U5d	U8a	U4e	U4f	U8b,c	U5e	U8d	U6	U4b,d	U5f	U7

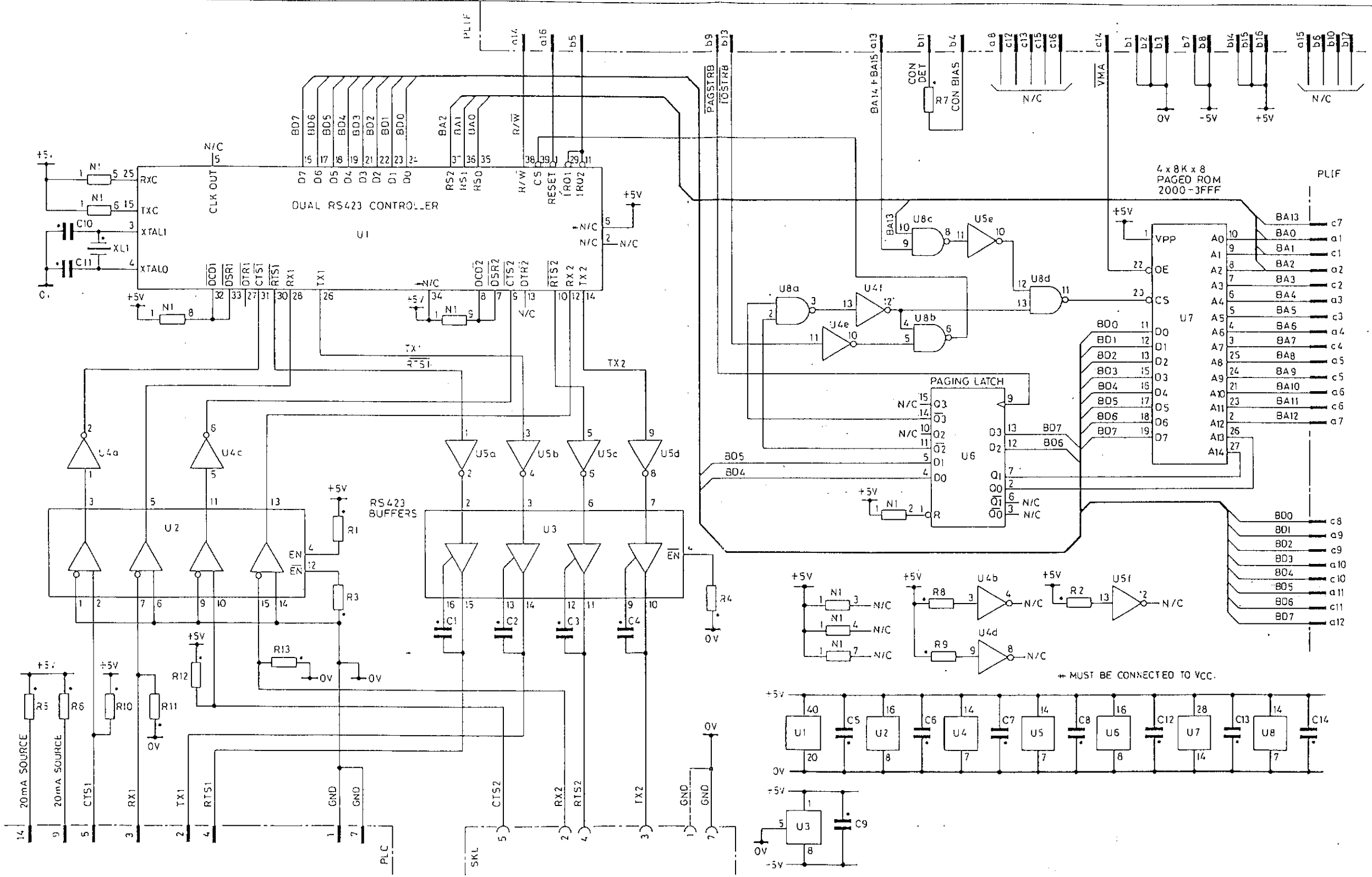


Fig. 6.20 RS423 Option

RES	N1 R5 R6	N1										R7	R1 R2	R3	R8	R4		
CAPS	C2	C3											C4 C6	C5	C1 C10 C9			
MISC	U6a D3	D2	U6b	U7 U2	U1 U5c	U3 U4						O1 O5	U5 O2	O4	B1	XL1 L2 L1	C8	C7

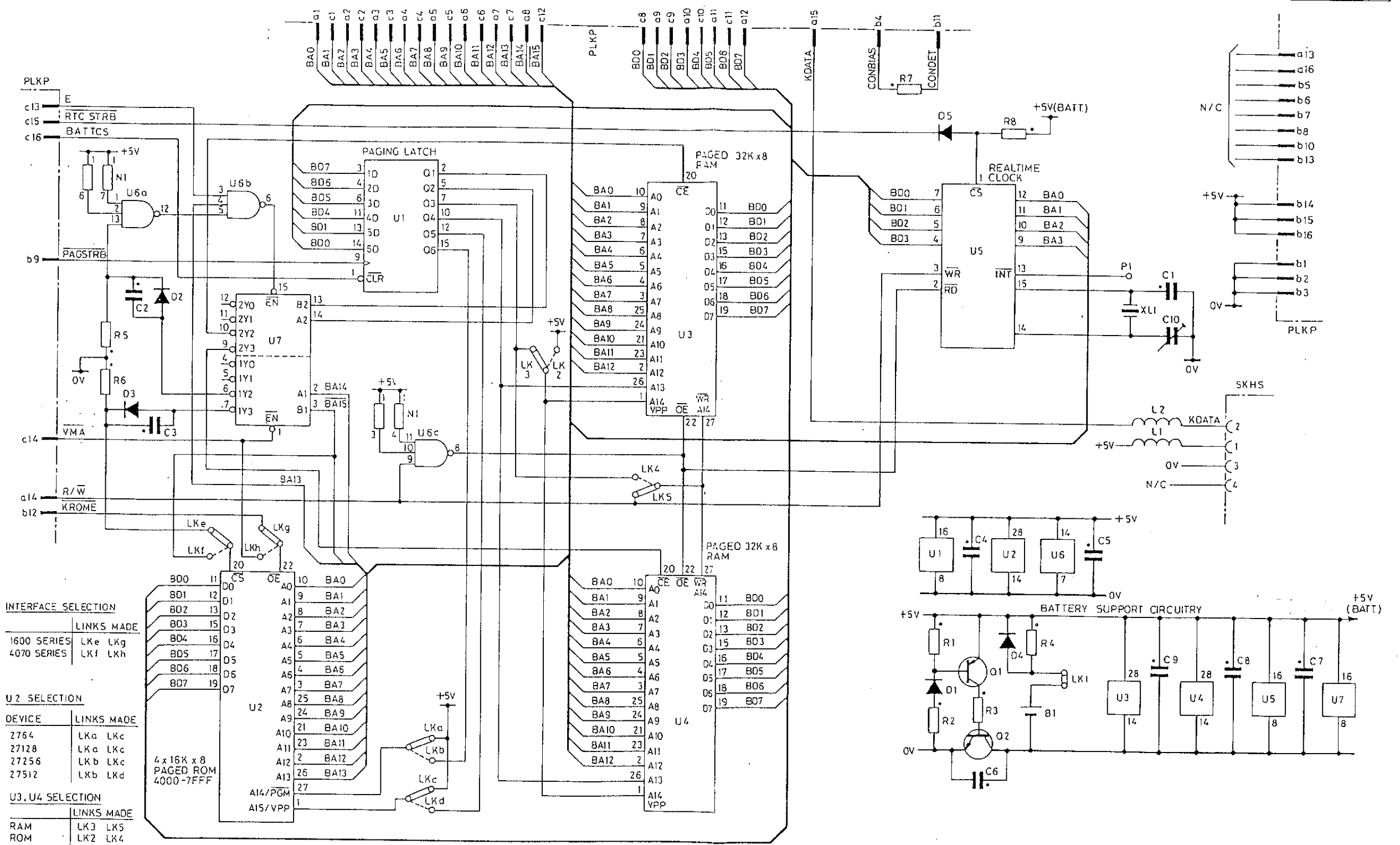


Fig. 6.21 Waveform Processor interface pod option



RES.	R1	R3	R2																	
CAPS.	C2	C4		C3	C1															
MISC		XL1	U2		U1	S16 S1	S17 S2	S18 S3	S19 S4	S26 S20 S10 S5	S15 S21 S11 S6	S22 S12 S7	S23 S13 S8	S24 S14	S25 S9					

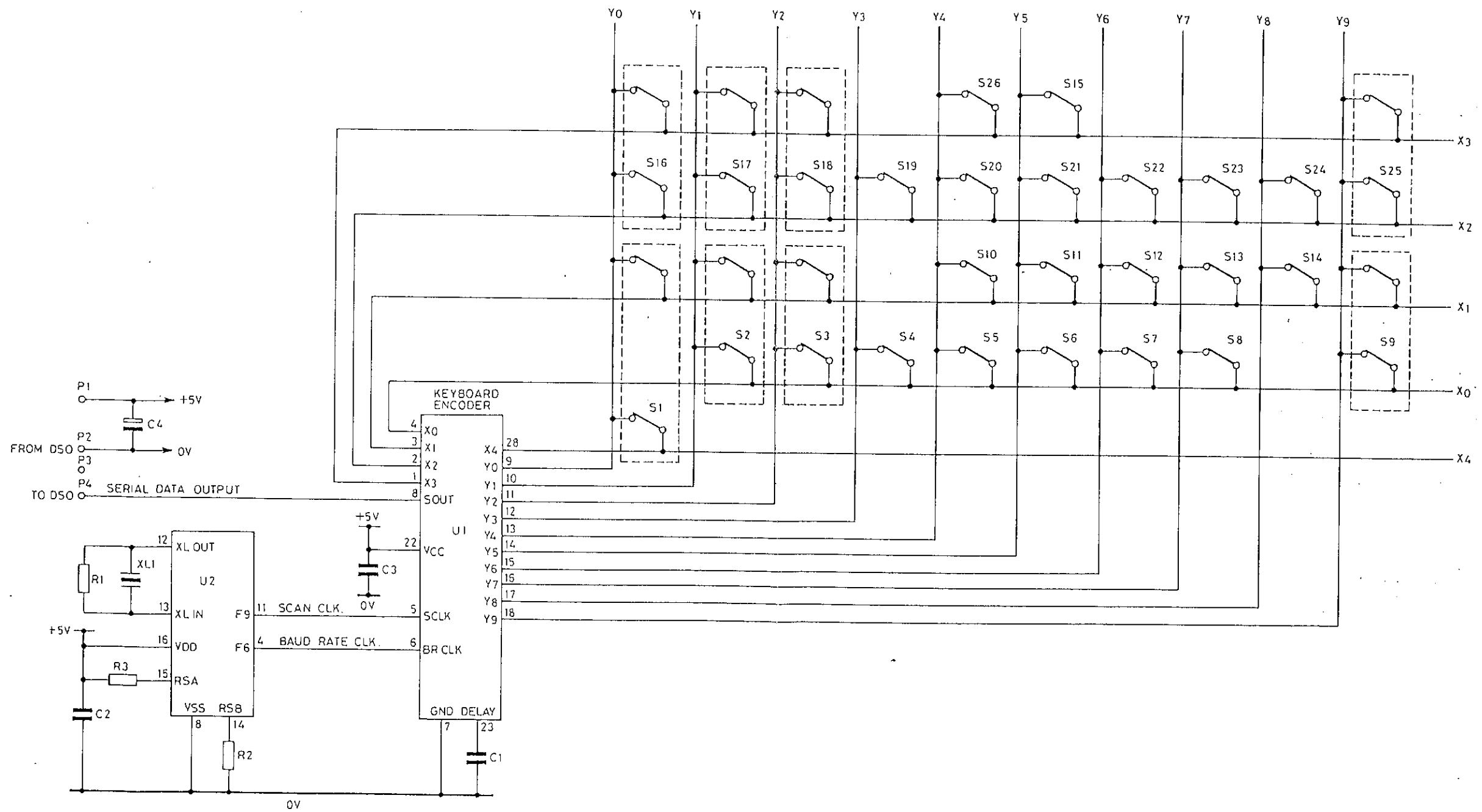


Fig. 6.22 160/170 Keypad

RES.		N1	R1 R2		R3 R4 R5	R12 N2	R6 R7	R8	R9 R10 R11		
CAPS.	C1 C4 C5 C6 C7	C2		C3	C9				C8		
MISC.			U3a b	U1		Q2 U3c d	U2	L1 Q5 Q7	Q6 Q8	Q2 Q3	S4 S5

