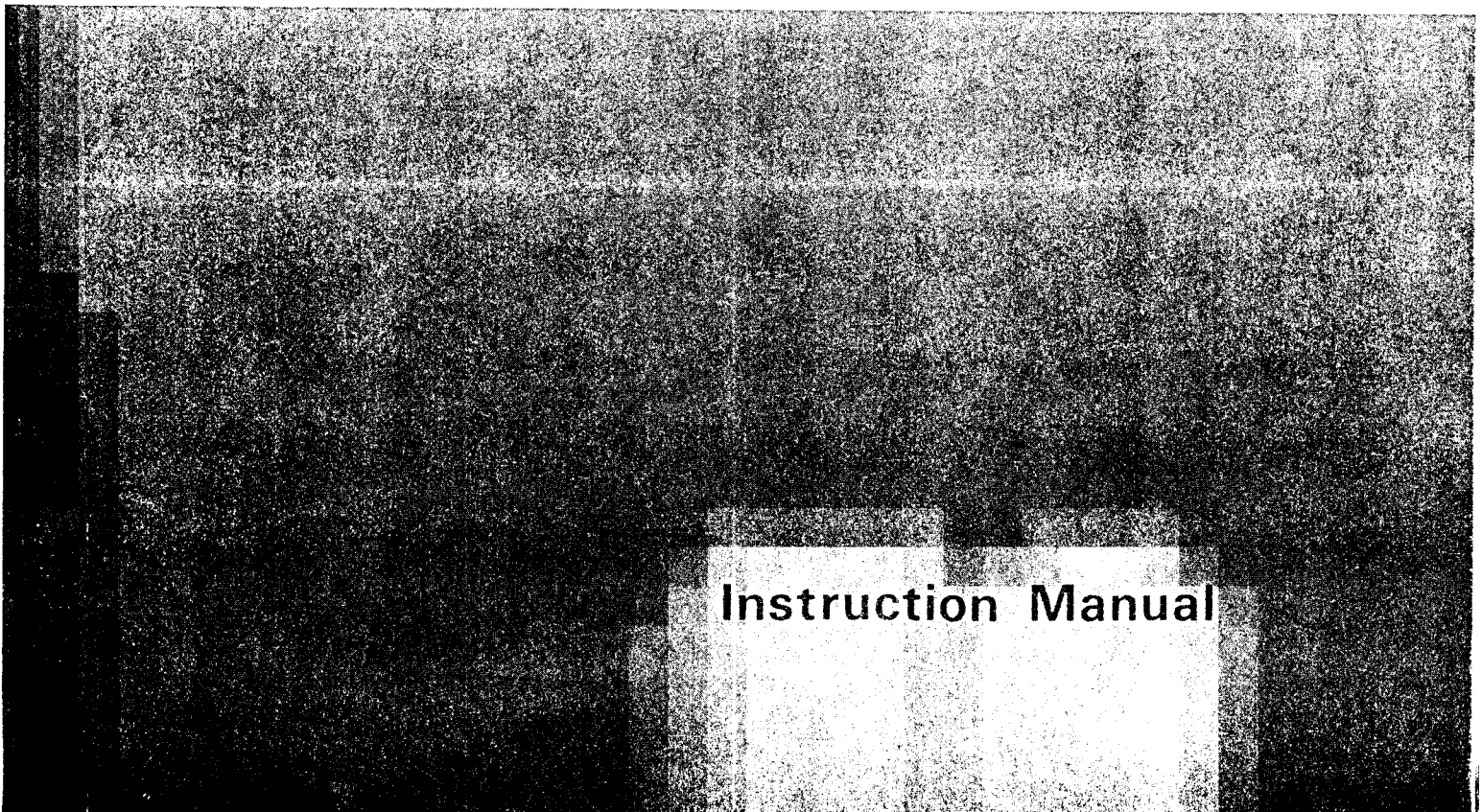
marconi
instruments

TF 2171

DIGITAL SYNCHRONIZER



Instruction Manual

Instruction Manual

No. EB 2171

for

Digital Synchronizer

TF 2171

Model No. 52171-900

MARCONI INSTRUMENTS LIMITED
ST. ALBANS HERTFORDSHIRE ENGLAND

Contents

Chapter 1

General information

1.1 INTRODUCTION

Digital Synchronizer TF 2171 is designed for use with Signal Generator TF 2015, to which it can be fitted as shown in Fig. 1.1. Together, the instruments provide a 10 to 520 MHz signal generator system with high discrimination tuning and very good frequency stability.

Warm-up drift is eliminated, so measurements can be commenced almost immediately after switching on. Incremental frequency control can be obtained digitally by adjusting the frequency switches of the synchronizer in increments of 100 Hz up to a maximum of 0.5% of the initially set frequency without any readjustment of the generator.

The synchronizer can also be switched to provide a 1 MHz standard frequency or to accept an external 1 MHz frequency standard.

The setting up procedure is extremely simple and calls only for the positioning of the synchronizer frequency switches and the tuning of the signal generator to obtain a 'locked-on' condition.

All the features of Signal Generator TF 2015 are fully maintained including the a.m. and f.m. facilities and the synchronizer can be switched to allow the generator to be used independently i.e. in the unlocked mode.

Fig. 1.1 Digital Synchronizer TF 2171 fitted below Signal Generator TF 2015

1.2 DATA SUMMARY

Characteristic	*Performance*
CARRIER FREQUENCY	
Range :	10 MHz to 520 MHz. (Specifically for use with Signal Generator TF 2015.)
Selection :	Seven decade switch controls in 100 Hz steps.
Incremental frequency control :	After synchronization, the decade controls may be used to digitally increment the generator carrier frequency over a range of typically ±0.5% without retuning the generator.
INTERNAL FREQUENCY STANDARD :	
Ageing rate :	Not greater than ±1 in 10^7 per month after 3 months continuous use.
Temperature coefficient :	Not greater than ±1 in 10^7 frequency change over the range 0 to 40°C. Adjustment by rear panel pre-set control.
Warm-up time :	Typically 10 minutes for the frequency to be within ±2 in 10^7 of final value.
Output level :	Not less than 2 V p-p square wave at 1 MHz.
RF INPUT	Compatible with counter output of Signal Generator TF 2015.
EXTERNAL STANDARD INPUT :	Switched socket provides internally generated 1 MHz standard signal at t.t.l. level or accepts 1 MHz input signal at t.t.l. level from external standard. Maximum input 5 V p-p, minimum input 2.5 V p-p.
LEAKAGE :	When used with Signal Generator TF 2015 and internal frequency standard, the r.f. leakage performance of the TF 2015 is maintained.
NON-HARMONICALLY RELATED COHERENT COMPONENTS :	None measurable on the output of TF 2015.

Power requirements

AC supply :	Any voltage within the limits 95 to 130 V and 190 V to 264 V; 45 Hz to 500 Hz.
Power consumption :	30 VA

Dimensions and weight

Height	*Width*	*Depth*	*Weight*
140 mm (5.5 in)	286 mm (11.25 in)	311 mm (12.25 in)	5.7 kg (12.5 lb)

1.3 ACCESSORIES

Supplied

Code No.	
43129-071	AC supply cable.
43129-063	Flexible coaxial cable, 50 Ω BNC plug to BNC plug.
43129-190	Semi-rigid coaxial cable, 50 Ω TNC plug to TNC plug.
46883-214	Mounting kit, for fitting to Signal Generator TF 2015.

Available

41690-044	Carrying case.	
43129-103	Coaxial cable, 50 Ω TNC plug to BNC plug.	
54127-231	Shelf rack mounting (Single)	Fitting instructions for these are included in the kit.
54127-241	Shelf rack mounting (Double)	

Chapter 2

Operation

2.1 FITTING TO SIGNAL GENERATOR

(1) Turn TF 2015 upside down and remove the bottom section of the case.

(2) Dismantle the tilt bar fitted at the front and discard the external plate with the two holes and two slots.

(3) Refit the tilt bar using one of the two latching plates supplied (joggled ends of plate inwards).

(4) Using the fixings supplied, fit the two plastic stands to clamp the latching plate.

(5) Remove the two rear stands and refit to clamp the second latching plate using existing fittings.

(6) Refit the bottom section of the case; then position TF 2015 on top of the synchronizer and clamp the two instruments together using the clips attached to each side of the synchronizer case.

2.2 CONNECTING TO SIGNAL GENERATOR

Only two connections, both at the rear, are required between the synchronizer and TF 2015.

(1) Using the flexible coaxial cable supplied, connect SYNC OUT on the synchronizer to SYNC/ SWEEP IN on TF 2015.

(2) Using the semi-rigid coaxial cable supplied, connect RF INPUT on the synchronizer to COUNTER OUT on TF 2015.

2.3 AC SUPPLY CABLE

The a.c. supply cable is fitted at one end with a female connector which mates with the a.c. input connector on the instrument. When fitting a supply plug ensure that the conductors are connected as follows :

Earth	- Green/Yellow
Neutral	- Blue
Live	- Brown

2.4 PRELIMINARY REQUIREMENTS

Prior to connecting the instrument to the a.c. supply :

(1) Check that the voltage selector switch is set to accept the local supply, i.e. set to 230 V for the range 190 to 264 V or to 110 V for the range 95 to 132 V. (Voltage regulation eliminates transformer tap changing except between the 95-130 V and 190-264 V ranges.)

To change the range, remove the locking plate, set the switch correctly, reverse the plate and refit.

(2) Check that the fuses are of the correct rating and type - see Section 2.5 - and secure in their holders.

2.5 FUSES

The instrument is normally supplied with fuses rated at 250 mA (slow-blow) and with the mains selector switch set for supply voltages of 190 to 264 V.

For supply voltages of 95 to 130 V change the fuses for those rated at 500 mA (slow-blow).

2.6 CONTROLS AND CONNECTORS

Front panel

(1) AC SUPPLY switch. Press up to switch on. Pilot lamp indicates presence of rectified supply.

(2) LOCK switch. Press up to operate generator in locked mode. With the switch down, the generator can be operated independently of the synchronizer.

(3) OUT OF LOCK lamp. Goes out when generator is correctly locked.

(4) SYNC OUTPUT meter. Indicates control signal level of synchronizer, i.e. the position of the generator frequency within the lock range.

(5) Frequency switches. Seven rotary decade switches to select the desired frequency. Minimum increment is 100 Hz.

Rear panel

(1) AC input connector. Mates with the connector fitted to the a.c. supply cable provided.

(2) Voltage selector switch. Selects either 95 to 132 V or 190 to 264 V to suit local a.c. supply.

(3) Fuses. AC input fuses rated at 250 mA (slow blow) for 190 to 264 V or 500 mA (slow-blow) for 90 to 132 V.

(4) RF INPUT connector (TNC 50 Ω). Accepts the COUNTER OUTPUT signal from TF 2015.

(5) SYNC OUT connector BNC 50 Ω). Provides the synchronizer control signal to SYNC/SWEEP IN on TF 2015.

(6) 1 MHz STANDARD connector (BNC 50 Ω). Provides or accepts a 1 MHz standard frequency signal depending on the setting of the associated switch - see (7).

(7) 1 MHz STANDARD switch. When positioned at INT OUTPUT a 1 MHz signal derived from the 5 MHz crystal controlled oscillator is available at the connector. When positioned at EXT INPUT an external 1 MHz standard can be applied to the connector to replace the internal crystal standard.

(8) INT.FREQ.STD. Adjusts the 5 MHz crystal controlled oscillator on Unit A2.

2.7 SETTING FREQUENCY

The setting up procedure is as follows :

(1) With both synchronizer and generator connected to the a.c. supply and switched on, check that both pilot lamps are lit.

(2) On the synchronizer, set the frequency switches as required and switch to LOCK ON.

(3) On the generator, set the function selector at CW and the CARRIER switch at ON. Select the appropriate carrier range and check that the pointer of the MOD & CARRIER LEVEL meter is within the white box on the meter scale.

(4) Using the TUNE control, and FINE TUNE control if necessary, carefully adjust the generator frequency to extinguish the LOCK lamp on the synchronizer. Check that the pointer of the SYNC OUTPUT meter is stationary. It is advisable, particularly if the incremental frequency facility is to be used, to adjust the FINE controls to bring the pointer of the SYNC OUTPUT meter to the centre of the white box.

The signal generator frequency is now locked to the frequency shown on the synchronizer.

2.8 INCREMENTAL FREQUENCY ADJUSTMENT

Accurate incremental frequency changes up to 0.5% from the initial frequency setting can be obtained by readjusting only the synchronizer decade switches. This feature is useful for quickly and accurately checking narrow bandwidths, response of highly selective tuned circuits, or the response of s.s.b. receivers.

Incremental changes using the synchronizer will cause the deflection of the SYNC OUTPUT meter pointer to change, but the signal generator will be locked to the changed frequency provided the LOCK lamp remains unlit.

2.9 INDEPENDENT USE OF SIGNAL GENERATOR

Signal Generator TF 2015 can be used as an independent instrument without disconnecting the synchronizer. To use the generator in this way press the LOCK switch down. The SUPPLY switch should be left at ON to maintain the operational levels of the synchronizer in a 'stand-by' condition.

2.10 1 MHz OUTPUT

When the 1 MHz STANDARD switch is set at INT OUTPUT a 1 MHz signal derived from the 5 MHz crystal oscillator is available from the 1 MHz STANDARD connector. This feature enables the synchronizer to provide a 1 MHz standard frequency for driving external equipment such as a frequency counter.

2.11 USING AN EXTERNAL 1 MHz SOURCE

With the 1 MHz STANDARD switch at EXT INPUT a 2 V to 5 V square wave output from an external 1 MHz source can be applied to the 1 MHz STANDARD connector as a substitute for the internal 5 MHz standard of the synchronizer. This feature enables a common 1 MHz standard to be used as the fundamental source for the synchronizer and any auxiliary equipment.

If the instrument is inadvertently switched to accept an external standard when no external standard is connected, an incorrect synchronized condition will be obtained since the signal generator will then lock to the secondary standard in TF 2171.

With this condition, errors up to 300 kHz from the setting shown on the digital switches can occur. It is therefore essential to ensure that the INTERNAL OUT/EXTERNAL IN switch at the rear of the instrument is in the correct position. When an external standard is used it is recommended to check that the standard signal is present at the input socket at the rear of TF 2171.

2.12 INTERNAL FREQUENCY STANDARD ADJUSTMENT

If required the frequency of the internal standard may be adjusted by use of the INT.FREQ.STD. adjustment control located on the rear panel. The frequency can be measured by connecting a suitable frequency counter to the 1 MHz standard output socket with the 1 MHz standard switch set to INTERNAL OUTPUT.

Coarse adjustment may also be carried out internally by means of a capacitance trimmer control. This can be located by removing the only counter sunk screw on the side of the crystal oven assembly.

Chapter 3

Technical description

3.1 INTRODUCTION

This chapter, which should be read with reference to the drawings, illustrations and circuit diagrams contained within this manual, outlines the function of the synchronizer when used with Signal Generator TF 2015 and describes the operation of the circuits employed.

3.2 MECHANICAL CHARACTERISTICS

The synchronizer is constructed to be easily fitted to Signal Generator TF 2015 and to provide easy access to all components for adjustment or repair.

All printed circuit boards and sub-assemblies in the instrument are allocated a unit identification number in the sequence A0 to A4 and where practical the assembly is marked with this number; silk screening is used to identify the components on the printed circuit boards.

Instrument construction consists of front and rear panels supported by side plates which are designed to support an r.f. box and to carry the mains transformer (T1) and two i.c. packages (IC1 and IC3). The rear panel is used as a heat-sink for power transistor A0TR1 and the i.c. package IC2.

The r.f. box contains units A1, A2 and the frequency switches SA to SG. Unit A1 consists of the input amplifier and diode shaper circuits, the prescaler and the variable ratio dividers. Unit A2 carries the 5 MHz and 10 MHz oscillator circuits and associated dividers, the ramp generators, the phase detectors, the sample and hold driver circuits and the lock indicator circuit. The rear of the r.f. box carries the RF INPUT connector, the 1 MHz STANDARD connector together with its associated switch. The underside of the r.f. box is used to mount the r.f. filter assembly, the interface circuit Unit A3, the power supply rectifier/regulator circuits Unit A4 and the associated capacitors C23, C24 and C26.

The instrument case, which is in two sections and easily removed by extracting six screws, is fitted with a carrying handle and a fold-away tilt bar. Clips are attached to the case and a mounting kit is supplied to enable the synchronizer to be quickly fitted to Signal Generator TF 2015. A clip-on cover is provided to protect the front panel controls.

3.3 BASIC PRINCIPLE

When a synchronizer is used with a signal generator as shown in the block diagram Fig. 3.1 the configuration can be considered as a phase locked frequency synthesizer.

Output from the crystal oscillator at a frequency fr is passed to a series of fixed dividers to produce a reference frequency fr/m which is applied to one input of a phase detector. Output from the signal generator at a frequency fo is passed to a series of variable ratio dividers to produce a signal frequency fo/n which is applied to a second input of the phase detector. When the frequency of the generator is set such that

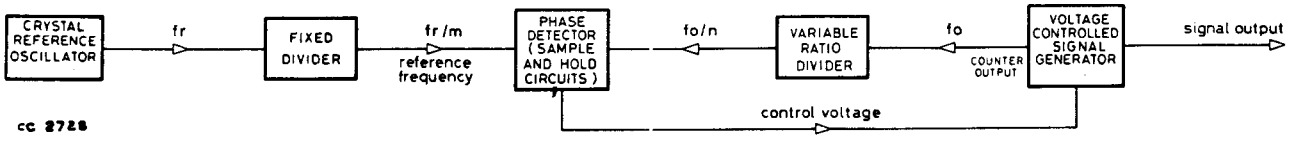


Fig. 3.1 Simplified functional diagram

fo/n is correctly related to fr/m the level of the control signal from the phase detector will be held constant. If the frequency of the generator drifts, the two frequencies will not be correctly related causing the control signal to vary in a manner such that the frequency of the generator is corrected.

The v.r.d. ratio (n) determines both the resolution (i.e. the smallest frequency increment that can be set) and the correction rate (i.e. the ability to deal with any rapid shifts in generator frequency). These two characteristics are conflicting since a high value of n is required for good resolution and a low value for high correction rate. In practice, this is overcome by including two phase locked loops: (i) a fast acting loop which provides large frequency increments and a high correction rate and (ii) a slow acting loop to provide the small increments.

3.4 CIRCUIT SUMMARY

The block diagram, Fig. 3.2, shows the functional arrangement of the synchronizer.

The input amplifier and the diode shaper provide a signal of the required form and amplitude to the prescaler which is included to ensure that the maximum operating frequency (40 MHz) of the variable ratio dividers is not exceeded.

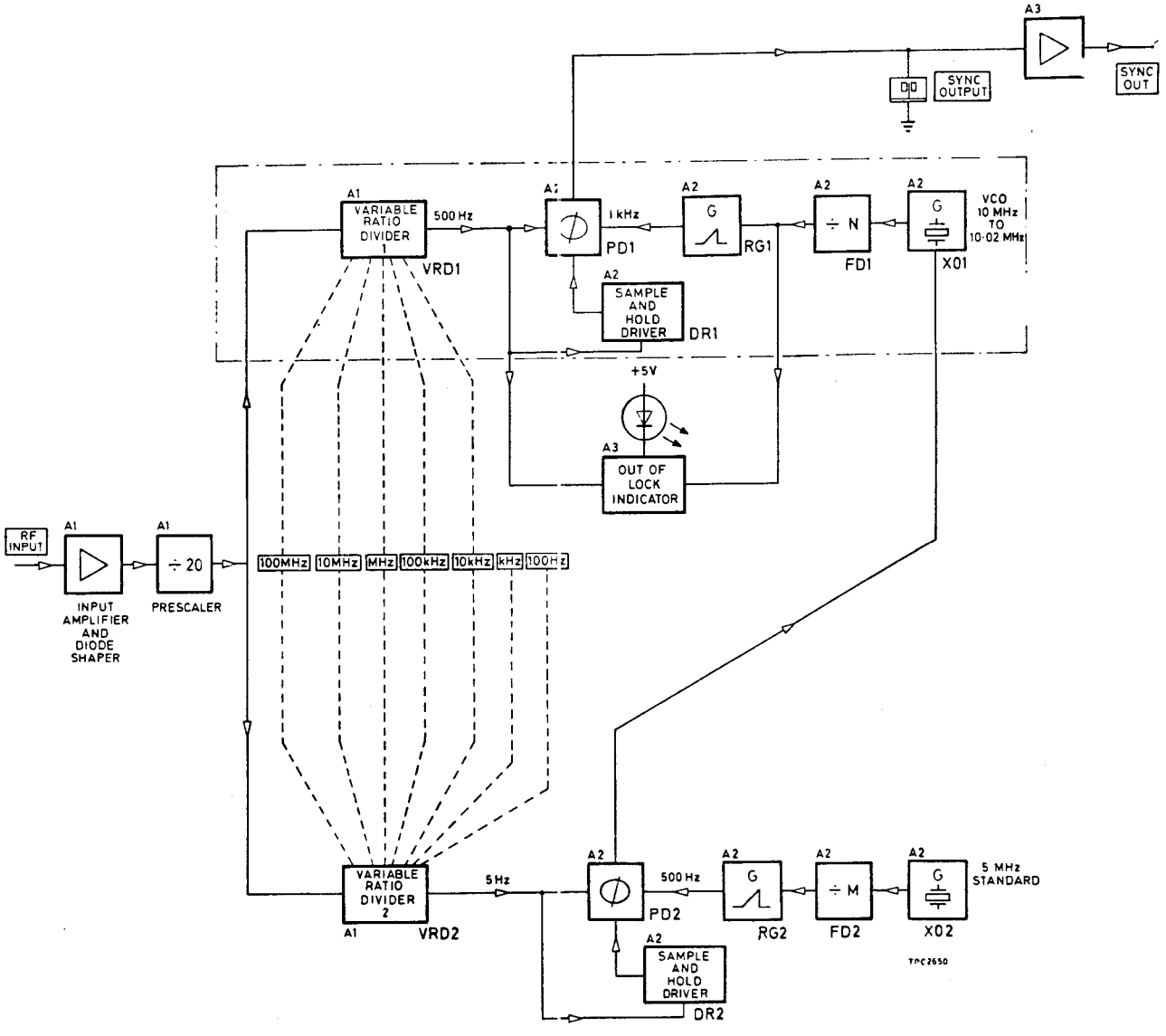


Fig. 3.2 Simplified block diagram

Output from the prescaler is passed to two variable ratio dividers VRD1 and VRD2.

Fast acting loop

VRD1, which forms part of the first phase locked loop consists of only five divider stages to provide the control necessary for fast correction of any frequency change occurring in the generator and to allow incremental settings to 10 kHz. When the signal generator frequency is locked to that set on the synchronizer, VRD1 produces a series of output pulses at a p.r.f. of 500 Hz. The 500 Hz pulses are applied to a phase detector PD1 where they sample a train of ramp waveforms produced by a voltage tuned crystal oscillator, X01, and a series of decade dividers, FD1, to provide a control signal to the generator.

If the frequency of the generator is suddenly changed the output p.r.f. from VRD1 will shift above or below 500 Hz. This causes a change in the sampling rate and consequently a change in the level of the control signal to the generator - see Fig. 3.3a - which rapidly corrects its frequency before the second (slow) loop has time to operate.

Slow acting loop

VRD2, which forms part of the second phase locked loop, consists of seven divider stages. When the 1 kHz and 100 Hz switches are each set at 0, VRD2 produces a series of output pulses at a p.r.f. of 5 Hz. The 5 Hz pulses are applied to a second phase detector PD2 where they sample a series of ramp waveforms produced by a 5 MHz crystal controlled oscillator X02 and a series of decade dividers FD2. The output of PD2 provides a control signal to the voltage tuned crystal oscillator X01 to set its frequency at 10 MHz.

To obtain increments of 1 kHz and 100 Hz the appropriate switches are moved to a number other than 0. This causes the output p.r.f. from VRD 2 to shift from 5 Hz so sampling occurs at a different position on the 500 Hz ramp, to consequently change the level of the control signal to the oscillator X01, as shown in Fig. 3.3b. The resulting slight change in the frequency of X01 increases the frequency of the ramp waveforms to PD1 such that the 500 Hz sampling pulses from VRD1 occur at a different position on the ramp. This causes the level of the control signal to the generator to change to provide the desired frequency increments.

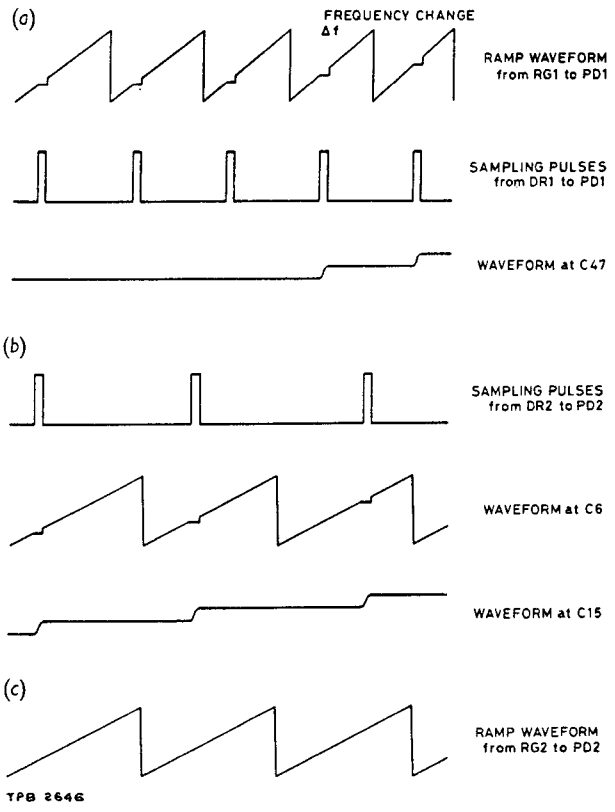


Fig. 3.3 Sampling and ramp waveforms

3.5 INPUT CIRCUIT

Circuit diagram Fig. 7.1

The amplifier consists of three common emitter stages TR1, TR2 and TR3 with the bias and gain of each stage set by the resistance/capacitance network connected between the collector and base of each transistor. To prevent a large signal causing overload and subsequent frequency doubling, the input to each stage incorporates a clamp diode D1, D2 and D3.

Output from the amplifier is applied to a clamping circuit D4 and D5. To ensure that the required signal level is passed to the prescaler the bias level to the diodes is preset by adjustment of R19.

Frequency division by a factor of twenty is obtained using a decade divider IC1 followed by a bistable IC2. Because the output of IC2 is at e.c.l. level it is passed to a common emitter amplifier TR4 to provide the voltage swing necessary to drive the t.t.l. circuits in the variable ratio dividers.

3.6 VARIABLE RATIO DIVIDERS

Circuit diagram Fig. 7.2

The two variable ratio dividers VRD1 and VRD2 differ only in the number of decade counters included in each, i.e. five and seven respectively. The two circuits which are interconnected as shown in Fig. 3.2 can be preset to any number from 0 to 9 to provide the desired overall division ratio.

When the digital switches are set at the required frequency, the counters will be preset to a number (X) equal to the complement of the desired division ratio (Y) with respect to the maximum content (Z) of the variable ratio divider, i.e. division ratio is Z-X. When input pulses are received from the prescaler the count will commence from X and continue to Z (counter full). The full condition is then detected and the signal is passed to the phase detector as a sampling pulse.

The overall function of the prescaler and the variable ratio dividers may be more clearly understood by reference to Fig. 3.4.

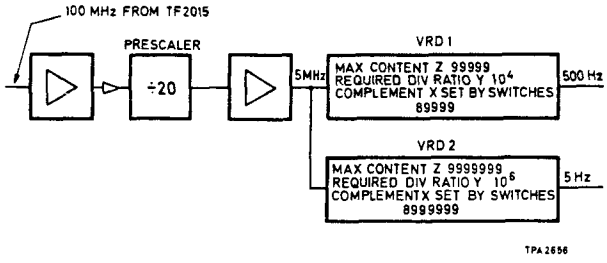


Fig. 3.4 Functional diagram of variable ratio dividers

Consider the operation of VRD2 (seven decade counters). The NAND gates IC6, IC5c3, IC7 and IC5a3 recognize when counters IC9 to IC14 are full, i.e. in the '9' state, and raise one input of the bistable IC3 to the high state. The remaining two inputs detect the '5' state of IC8 and allow IC3 and IC4 to count the following four clock pulses and provide a reset pulse to the counting chain as shown in Fig. 3.5.

The counting chain in VRD1 functions in exactly the same way.

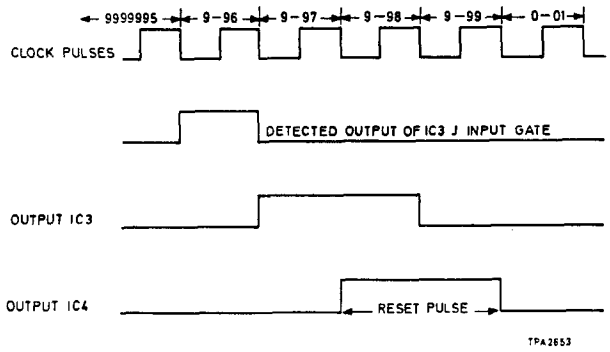


Fig. 3.5 Waveforms of reset system

3.7 STANDARD REFERENCE OSCILLATOR XO2

Circuit diagram Fig. 7.3

The fundamental reference frequency is provided by a 5 MHz temperature controlled crystal oscillator unit with an accuracy of 1 part in 10^7. To enable its frequency to be precisely set at 5 MHz, the unit has two controls (a) a trimmer which provides an initial adjustment and (b) an external control R5 for final adjustment.

Output from the oscillator is a 5 V square wave which is suitable for driving the t.t.l. circuits in the standard divider FD2.

3.8 FIXED FREQUENCY DIVIDERS

Circuit diagram Fig. 7.3

Two fixed divider chains are used in the instrument and the function of each is as follows.

Divider FD2, which is driven by the 5 MHz crystal controlled oscillator, consists of four decade counters IC4, IC5, IC6 and IC7 connected in cascade to provide an output frequency of 500 Hz. The square wave output from IC7 is applied to IC8 to produce a train of narrow positive going pulses at a p.r.f. of 500 Hz to the ramp generator RG2. Since each integrated circuit (IC4 to IC7) consists of two sections arranged to divide by five and two, an accurate 1 MHz output is available when the output of the 5 MHz reference oscillator has passed through the divide by five section of IC4.

The other fixed divider FD1, which is driven by the 10 MHz voltage tuned crystal oscillator, consists of four decade dividers IC15, IC16, IC17 and IC18 connected in cascade to provide an output of 1 kHz. The square wave output from IC18 is applied to IC19 to produce a train of narrow positive going pulses at a p.r.f. of 1 kHz to the ramp generator RG1.

3.9 RAMP GENERATORS

Circuit diagram Fig. 7.3

The two ramp generators RG1 and RG2 each consist of a constant current source, a transistor switch and a capacitor; their operation, which is explained with reference to RG2, is in principle the same.

During the interval between the 500 Hz pulses, transistor TR1 is non-conducting causing capacitor C2 to be linearly charged to the required level by the constant current source provided by the circuit of TR2. The arrival of a pulse at the base of TR1 causes this transistor to conduct and rapidly discharge C2. The generated waveform is as shown in Fig. 3.3(c).

3.10 SAMPLE AND HOLD PHASE DETECTORS

Circuit diagram Fig. 7.3

Since the two sample and hold phase detectors PD1 and PD2 are basically the same their operation can be explained with reference to the circuit of PD2.

During the interval between the sampling pulses from VRD2 transistor TR5 is on to allow the output from the ramp generator to charge the sampling capacitor C6 while TR7 is off, to isolate the hold capacitor C15 from the ramp input.

When the sampling pulse from the v.r.d. appears TR5 is switched off to isolate C6 which now holds a voltage at a level which has been determined by the position of the sampling pulse on the ramp. Transistor TR7 is now switched on for a short period to transfer the voltage at C6 to the hold capacitor C15. Since the voltage at C15 determines the level of the control signal to the voltage tuned crystal oscillator X01 and consequently its set frequency, it is monitored by the f.e.t. follower circuit TR8 to ensure that it is not discharged during the interval between sampling pulses.

3.11 SAMPLE AND HOLD DRIVER CIRCUITS

Circuit diagram Fig. 7.3

Operation of the phase detectors PD1 and PD2 is controlled by the sample and hold driver circuits DR1 and DR2. Except for the value of the components, the two circuits are similar so their function can be explained with reference to the circuit of DR2 which uses the three monostables IC1, IC2 and IC3. For sampling it is necessary to switch TR5 off just before TR7 is switched on to ensure that only a pure d.c. voltage is transferred to C15. To achieve this the output pulses from VRD2 are applied to the monostable IC1 to produce positive going pulses of the required duration to switch TR4 on and consequently TR5 off during the transfer periods.

Monostable IC2 provides a small delay before IC3 supplies the required negative going pulses to switch TR6 off and consequently TR7 on - see Fig. 3.6.

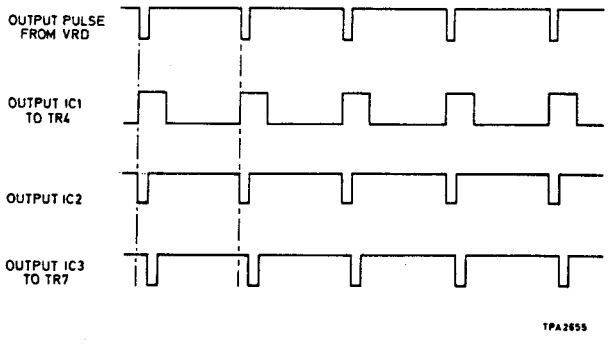


Fig. 3.6 Waveforms of sample and hold circuits

3.12 VOLTAGE TUNED CRYSTAL OSCILLATOR

Circuit diagram Fig. 7.3

Transistors TR9 and TR10 together with the crystal unit X01 and the circuit L1 D1 form an emitter coupled voltage tuned crystal oscillator which functions as follows:

The crystal, which operates as a series tuned circuit at 10.02 MHz, is connected in series with a second tuned circuit L1 and varactor D1 as shown in Fig. 3.7. The capacitive component Cx of the crystal is very small, being typically 0.01 pF, whilst its inductive component Lx is very large, i.e. several henries. Inductance L1 of the external circuit is very small compared with Lx whilst the capacitance of the varactor D1 is large compared with Cx. Since the capacitance of D1 is effectively in series with Cx its capacitive variations produce only small frequency changes within the tuned frequency range (10-10.02 MHz) of the oscillator. The capacitance of D1 and consequently the frequency of the circuit is determined by the d.c. output from PD1.

Output from the oscillator is passed to an amplifier TR11 to provide the signal level required to drive the t.t.l. circuits in the divider FD1.

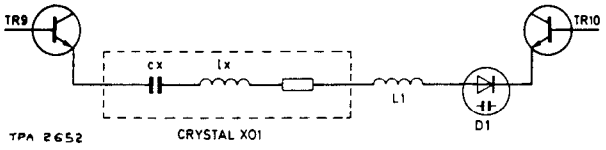


Fig. 3.7 Functional diagram of voltage tuned crystal oscillator

3.13 OUT-OF-LOCK INDICATOR CIRCUIT

Circuit diagram Fig. 7.3

Operation of the out-of-lock indicator circuits is best described with reference to the functional diagram Fig. 3.8 which identifies the circuits used and illustrates their performance when the signal generator is in the locked mode.

The 1 kHz pulses (b) from the fixed divider FD1 are applied to a bistable IC12 to provide a train of 500 Hz pulses (c) to the monostable IC14 which also receives the narrow 500 Hz pulses (a) from the variable ratio divider VRD1.

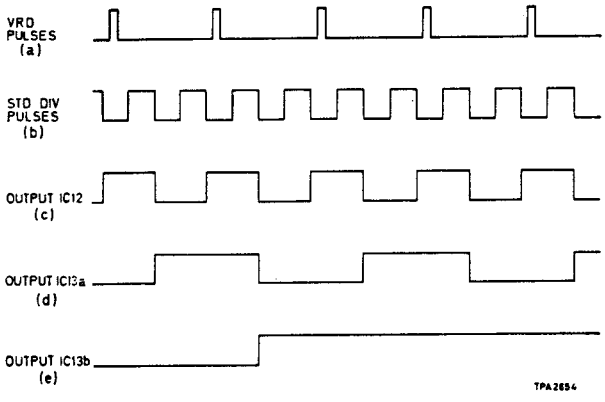


Fig. 3.8 Waveforms of out-of-lock indicator circuit

It is shown by relating waveforms (a) and (c) that when the signal generator is in the locked mode the v.r.d. pulses occur during the time that the output from IC12 is high. With this condition the two respective inputs to the monostable IC14 will be high, the monostable will not be triggered and the out-of-lock indicator will be unlit.

When the signal generator is not in lock the p.r.f. output from VRD1 is then not at 500 Hz so consequently the v.r.d. pulses do not always occur during the period when the output from IC12 is high. With this condition the respective inputs to the monostable will be received at different times and the monostable will be triggered causing the out-of-lock indicator to be lit.

To ensure that when the signal generator is in the locked mode the output pulses (b) from IC12 and the pulses (c) from the v.r.d. are maintained in phase a 'clear pulse' obtained from IC11 in the sample and hold driver circuit is applied to IC12 to immediately follow each v.r.d. pulse.

The circuit as described so far will not give an out-of-lock indication if the generator is at a sub-harmonic of that set on the synchronizer; therefore, to prevent false locking which could occur from this, a divide by four circuit IC13a and IC13b - see Fig. 3.9 - is included to produce waveforms (d) and (e). The inverted waveform

(e) from IC13b allows the monostable to trigger from the v.r.d. pulses despite the high level condition of waveform (c). It is also fed back to IC13a to prevent the circuits clocking so it is held in this state until the v.r.d. pulse is present and the following 'clear pulse' resets the circuits. The waveforms shown are those obtained in the absence of a 'clear pulse'.

TR20, D4, D5 and associated components ensure that when EXT STD is selected and no input is applied, the OUT OF LOCK lamp stays on.

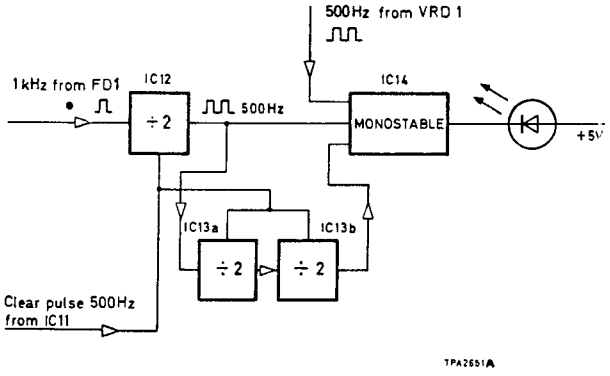


Fig. 3.9 Block diagram of false lock prevention circuits

3.14 INTERFACE AMPLIFIER

Circuit diagram Fig. 7.1

The interface amplifier circuit serves to convert the control voltage from the phase detector PD1 to a current drive for TF 2015. For voltage/current conversion transistors TR3 and TR6 form a long-tail pair with TR5 operating as a current inverter to add the current flowing through TR6 to that flowing through TR3. The circuit, which includes the temperature compensating diodes D3 and D4, has been balanced by selecting values for R13 and R17 such that no current flowed in a split load connected across the supply rails with the input connected to earth.

Because the tuning varactors in the TF 2015 oscillators have a non-linear voltage/capacitance characteristic the sensitivity of the synchronizer input on TF 2015 varies as the generator is tuned over each range. To maintain the loop gain within the desired limits the input signal to the interface is controlled by the circuit TR1, TR2 and the voltage/resistance converter APC1 consisting of the light emitting diode D2 and the light sensitive resistor PCC1, which functions as follows.

When the loop gain is high a large current flows through D2 causing it to be lit; this consequently lowers the resistance of PCC1 to accordingly reduce the signal level to the interface amplifier. With a lower loop gain the current flowing through D2 is not sufficient to cause it to be lit. The resistance of PCC1 is then increased such that the attenuator formed by R6 and PCC1 has little effect on the signal level to the interface amplifier.

3.15 POWER UNIT

Circuit diagram Fig. 7.4

The power unit, which operates from switch selected a.c. supplies of 95 to 130 V or 190 to 264 V, 45 to 500 Hz, consists of a mains transformer T1 with three secondary windings, three full wave rectifier circuits and four regulators to produce stabilized supplies of +24 V, +12 V, +5 V and -12 V. Connection to the a.c. supply is made through a three pin connector, a supply switch SH and fuses FS1 and FS2. The on/off indicator is a light emitting diode D2 which is operated from the +12 V supply.

The three voltage regulators IC1, IC2 and IC3, which provide stabilized supplies of +12 V, +5 V and +24 V respectively, also include protection against overload and external short circuit. The -12 V supply uses an operational amplifier IC4 with transistor TR1 as the regulating element. The reference is the 0V line and the sampling point is the junction of resistors R5 and R6 connected between the +12 V and -12 V rails.

The supply filters, which are contained in a screened box, are connected in series with various supply lines to minimize the introduction of any spurious r.f. Each consists of two screened sections using either a 6 or 10 μH inductor and lead-through capacitors.

RL1 ensures that when the TF 2171 is switched off no interaction will affect the accuracy of the TF 2015 if operating independent of the TF 2171.

Chapter 4

Maintenance

4.1 INTRODUCTION

This chapter contains information to enable the performance of the synchronizer to be maintained. It should be read with reference to Chapter 3 and the illustrations and circuit diagrams contained within this manual.

CAUTION

The instrument uses semiconductor devices which, although having inherent long term reliability, can be damaged by overloads, reverse polarity and excessive heat or radiation. Care should be exercised to ensure that d.c. supplies are not reversed and to avoid prolonged soldering and strong r.f. fields. Before applying continuity or insulation tests or before shorting or breaking a circuit refer to the circuit diagram to establish the effect on the bias arrangement of the devices employed.

NOTE (1). Test waveforms may vary slightly from the typical waveforms illustrated in Fig. 4.3 (a to y).

(2). The checks given in this section are simplified and of restricted range compared with those which would be needed to demonstrate complete compliance with the specification. They should be regarded only as providing a procedure, for routine maintenance, to determine whether adjustment or repair is necessary.

(3). Voltages given on the circuit diagrams approximate those which can be expected using a 20 kΩ/V meter on a typical TF 2171 connected to an a.c. supply of 240 V, 50 Hz. All voltage levels are with respect to chassis.

4.2 SCREW FASTENERS

The majority of screw threads are metric of various sizes but in some positions BA threads are used. All chromium plated screws and all screws tinted blue are metric.

Ensure that screws removed are refitted in original positions.

4.3 ACCESS TO SUB-ASSEMBLIES AND COMPONENTS

Removal of case

The case is in two sections. Remove the six screws (three each side) at the rear of the instrument then slide off the top and bottom sections.

Unit A1

To obtain access to Unit A1 shown in Fig. 4.1, remove the lid of the r.f. box. Unit A1 is hinged to provide access to Unit A2 and the frequency switches. It also enables direct connection to components for purpose of test and simplifies the replacement of a faulty component.

Unit A2

Direct access to Unit A2 is obtained by first removing the three holding screws at the rear of Unit A1 and then by folding Unit A1 back on its hinge. Unit A2 is also hinged as shown in Fig. 4.1 to provide access to inputs of the filter box and components. Prior to folding A2 back it is necessary that the push on connections to tags 11, 12, 13 with sleeves brown, red and orange respectively, be temporarily removed.

Units A3 and A4

These units are located on the underside of the instrument and are directly accessible as shown in Fig. 4.2.

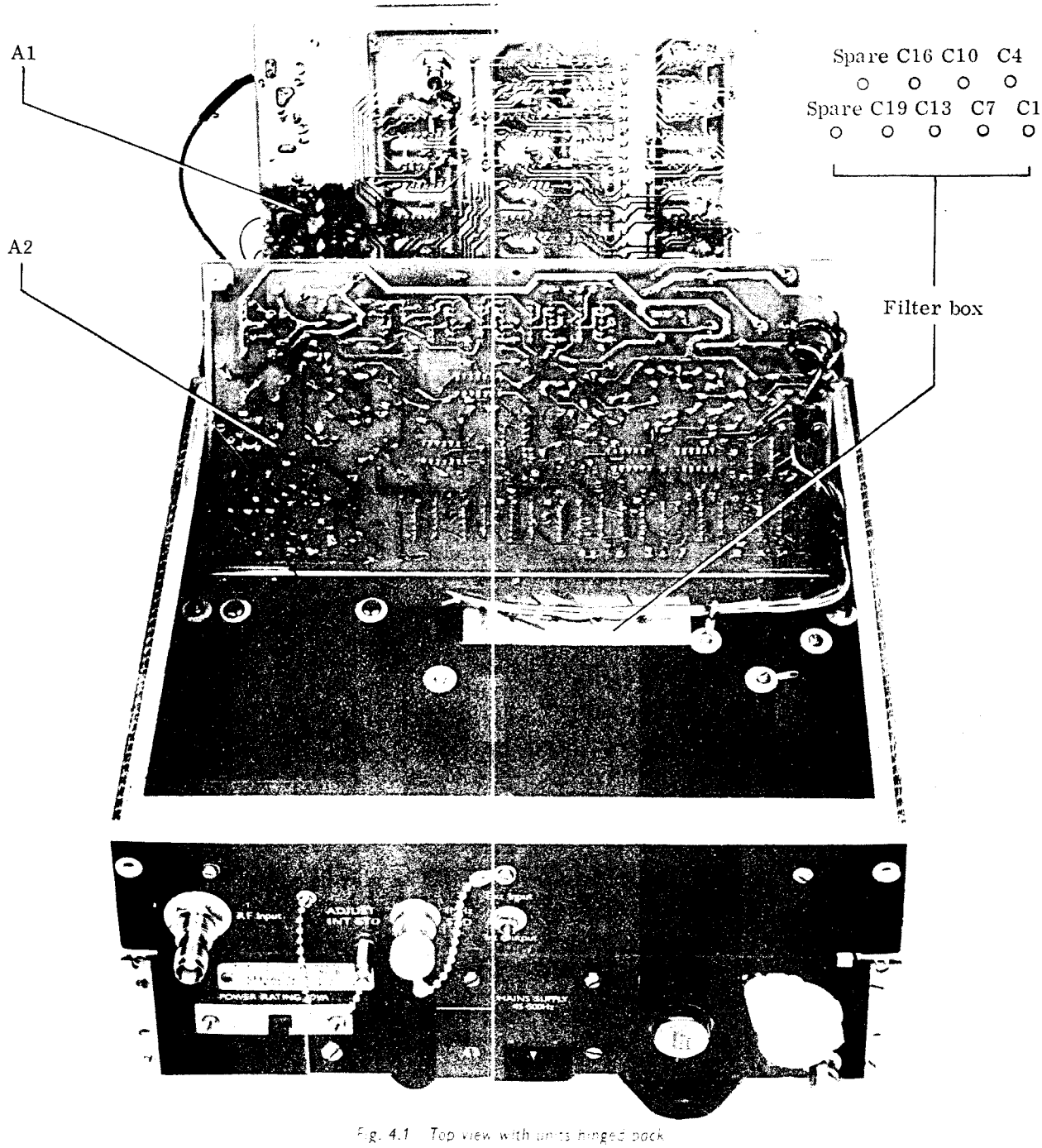


Fig. 4.1 Top view with units hinged back

Subsidiary assemblies

The location of subsidiary assemblies and various components is also shown in Figs. 4.1 and 4.2.

4.4 PRELIMINARY CHECKS

(1) Check to ensure that all switches are undamaged and operating correctly and verify that connectors are securely mated.

(2) Check that fuses are of the correct rating and type and fit correctly in the holder

(3) Check that the voltage selector switch is set to suit the local supply.

4.5 TEST EQUIPMENT

The test equipment required for maintenance and repair of the instrument is listed in Table 4.1.

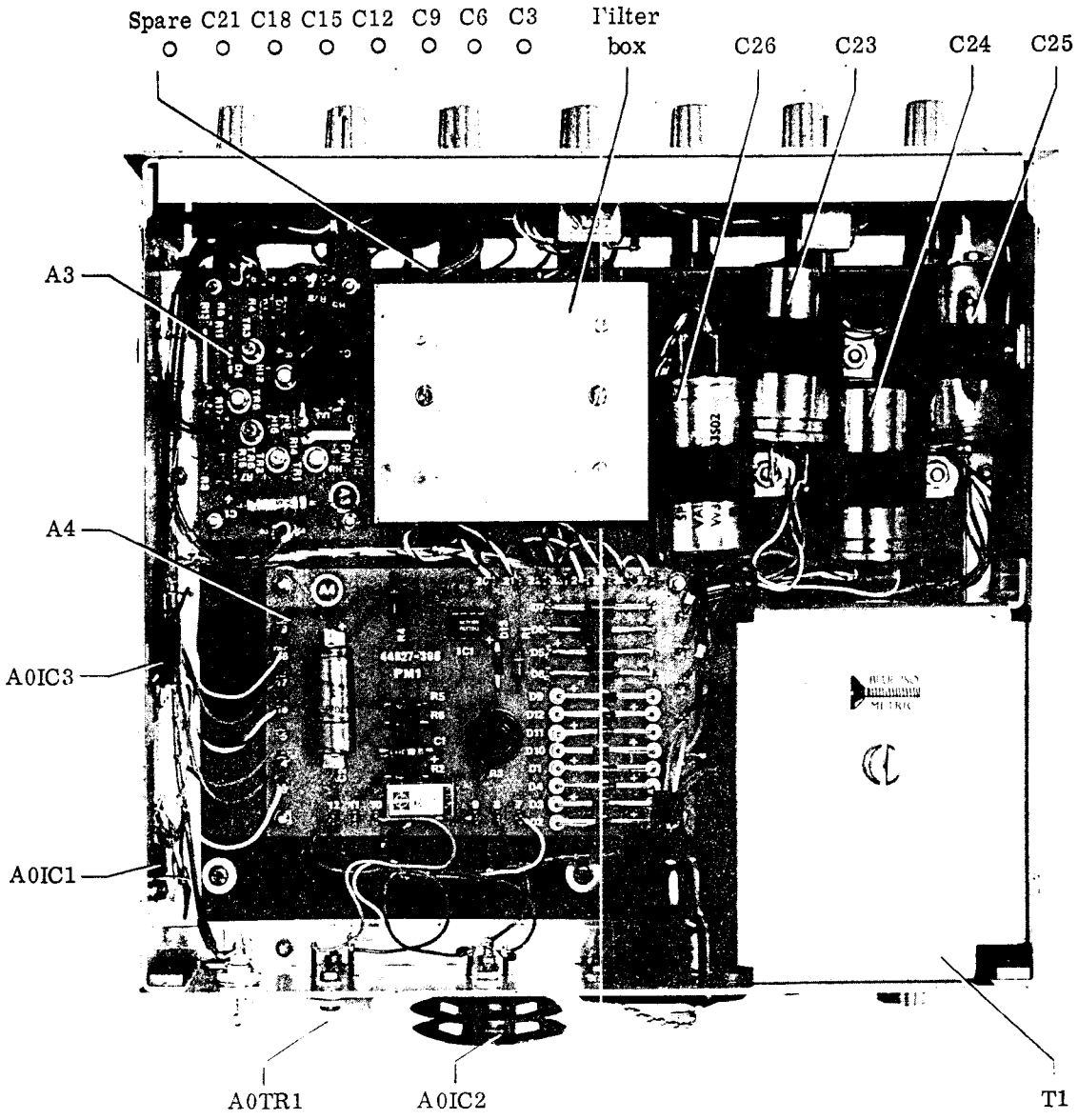


Fig. 4.2 Underside view

Table 4.1

Item	*Description*	*Recommended model*
a	Multimeter	GEC Selectest or Avometer Model 8
b	Oscilloscope	Minimum requirements : (a) Dual trace (b) Time base : 10 ns to 100 ms (c) Rise time : 2 ns (d) Amplitude measurement : 0 to 25 V
c	Input probe ($\div$ 10)	Suitable for above
d	Frequency counter	Marconi TF 2410 (standardized to 1 part in 10^8 at 5 MHz)
e	Variable voltage transformer	Variac or equivalent

4.6 OVERALL PERFORMANCE CHECK

Test equipment : item d.

With TF 2015 and TF 2171 connected together and switched on, correct performance can be quickly proved by the following test :

(1) Connect the frequency counter to the RF OUTPUT on TF 2015.

(2) Set TF 2171 at 100 MHz (1000000) and the LOCK switch at ON.

(3) Set TF 2015 at 100 MHz and carefully tune to extinguish the OUT OF LOCK lamp. Then check that the counter indicates 100 MHz.

(4) Set only TF 2171 at 100 MHz + 10 kHz (1000100) then check that the counter now indicates 100.01 MHz and that the OUT OF LOCK lamp remains unlit.

4.7 CIRCUIT CHECKS AND ADJUSTMENTS

The following functional checks should be performed to prove correct operation of the various circuits or to localize the cause of incorrect instrument performance. Where possible, adjustments are described for obtaining the required result.

4.7.1 Power supplies (A4)

Test equipment : items a, e.

(1) With TF 2171 disconnected from the a.c. supply remove connections to pins 14, 15, 17 and 18.

(2) With TF 2171 connected to the a.c. supply and switched on, connect the multimeter between pin 18 (positive) and pin 8 (negative) and check that the meter indicates 5.25 V. If necessary adjust R3 to obtain this voltage.

(3) Connect the multimeter in turn between pin 14 (positive) and pin 8 (negative) and pin 17 (positive) and pin 8 (negative) and check that the indicated voltages are 24 V ±1 V and 12 V ±0.5 V respectively.

(4) Connect the multimeter between pin 8 (positive) and pin 15 (negative) and check that the indicated voltage is 12 V ±0.5 V.

(5) Reconnect pins 14, 15, 17 and 18 and check that all voltage levels have remained the same.

(6) Connect the a.c. supply through the variable voltage transformer and check that with inputs to the power supply of between 190 and 260 V (or 95 and 130 V) the voltages as measured in (2), (3) and (4) remain within ±100 mV.

4.7.2 Input amplifier (A1)

Test equipment : items b, c.

(1) With TF 2015 connected to TF 2171 and switched ON set the generator frequency at 20 MHz and the RF OUTPUT controls fully clockwise, i.e. 0 and -7 dBm.

(2) Using the probe connect the oscilloscope to the junction of D4 and D5 and check that the waveform is as shown in Fig. 4.3 (a). If necessary adjust R19 to obtain the required amplitude.

(3) Set the r.f. output of TF 2015 at -13 dBm and check that the waveform shown is approximately the same, i.e. as Fig. 4.3 (a).

4.7.3 Prescaler unit (A1)

Test equipment : items b, c.

(1) With the frequency of TF 2015 at 20 MHz and the RF OUTPUT controls fully clockwise, connect the oscilloscope to the collector of TR4 and check that the waveform is as Fig. 4.3 (b).

(2) Set the frequency of TF 2015 at 500 MHz and the RF OUTPUT controls at -13 dBm and check that the waveform is as Fig. 4.3 (c).

4.7.4 Variable ratio dividers (A1)

Test equipment : items b, c.

(1) With the frequency of TF 2015 at 20 MHz and the RF OUTPUT controls fully clockwise set TF 2171 at 0000020.

(2) Connect the oscilloscope to pin 31 and check that the waveform is as Fig. 4.3 (d).

(3) Set TF 2171 at 0002000 then connect the oscilloscope to pin 32 and check that the waveform is the same i.e. as Fig. 4.3 (d).

4.7.5 5 MHz oscillator and divider FD2 (A2)

Test equipment : items b, c, d.

(1) Allow ten minutes from 'switch on' for the temperature of the crystal oven to stabilize then, using the oscilloscope probe, connect the counter to pin 1 on IC4 and check that the indicated frequency is 5 MHz ±0.5 Hz. If necessary carefully adjust R5 to obtain this requirement, (located on the rear panel). If the range of adjustment covered by R5 is insufficient to obtain the correct frequency, centre R5 travel and adjust the coarse capacitance trimmer. This can be located by removing the only counter sunk screw on the side of the crystal oven assembly.

(2) Remove the counter. Then, using the probe, connect the oscilloscope to pin 1 on IC4 and check that the waveform is as Fig. 4.3 (e).

(3) Connect the oscilloscope to pin 8 on IC8 and check that the waveform is as Fig. 4.3 (f).

4.7.6 Ramp generator RG2 (A2)

Test equipment : items b, c.

(1) Set TF 2015 and TF 2171 at 20 MHz and the RF OUTPUT controls on TF 2015 fully clockwise.

(2) Connect the oscilloscope to the collector of TR1 and check that the waveform is as Fig. 4.3 (g). If necessary adjust R3 to obtain the required ramp amplitude.

(3) Connect the oscilloscope to the emitter of TR3 and check that the waveform is as Fig. 4.3 (h).

4.7.7 Sample and hold driver circuit DR2 (A2)

Test equipment : items b, c.

(1) With TF 2015 and TF 2171 as in 4.7.6 (1) connect the oscilloscope in turn to the points listed below :

(a) pin 6 on IC1 for waveform Fig. 4.3 (i)
(b) pin 6 on IC2 for waveform Fig. 4.3 (j)
(c) pin 6 on IC3 for waveform Fig. 4.3 (k)
(d) collector of TR4 for waveform Fig. 4.3 (l)
(e) collector of TR6 for waveform Fig. 4.3 (m)

4.7.8 Voltage tuned crystal oscillator and divider FD1 (A2)

Test equipment : items b, c.

(1) With TF 2015 locked to TF 2171 at 10 MHz connect the oscilloscope to the source of TR7 and check by carefully triggering the oscilloscope that the waveform is as Fig. 4.3 (y). If necessary slightly adjust the core of L1 to position the step on the ramp at the required amplitude.

(2) Connect the oscilloscope in turn to the collectors of TR10 and TR11 and check that the waveforms are as Fig. 4.3 (n) and 4.3 (o) respectively.

(3) Connect the oscilloscope to pin 8 on IC19 and check that the waveform is as Fig. 4.3 (p).

4.7.9 Ramp generator RG1 (A2)

Test equipment : items b, c.

With TF 2015 and TF 2171 set at 20 MHz and with the TF 2015 RF OUTPUT controls fully clockwise, connect the oscilloscope to collector of TR12 and check that the waveform is as Fig. 4.3 (q).

4.7.10 Sample and hold driver circuit DR1 (A2)

Test equipment : items b, c.

(1) With TF 2015 and TF 2171 as in 4.7.9, connect the oscilloscope in turn to pin 6 on IC9,

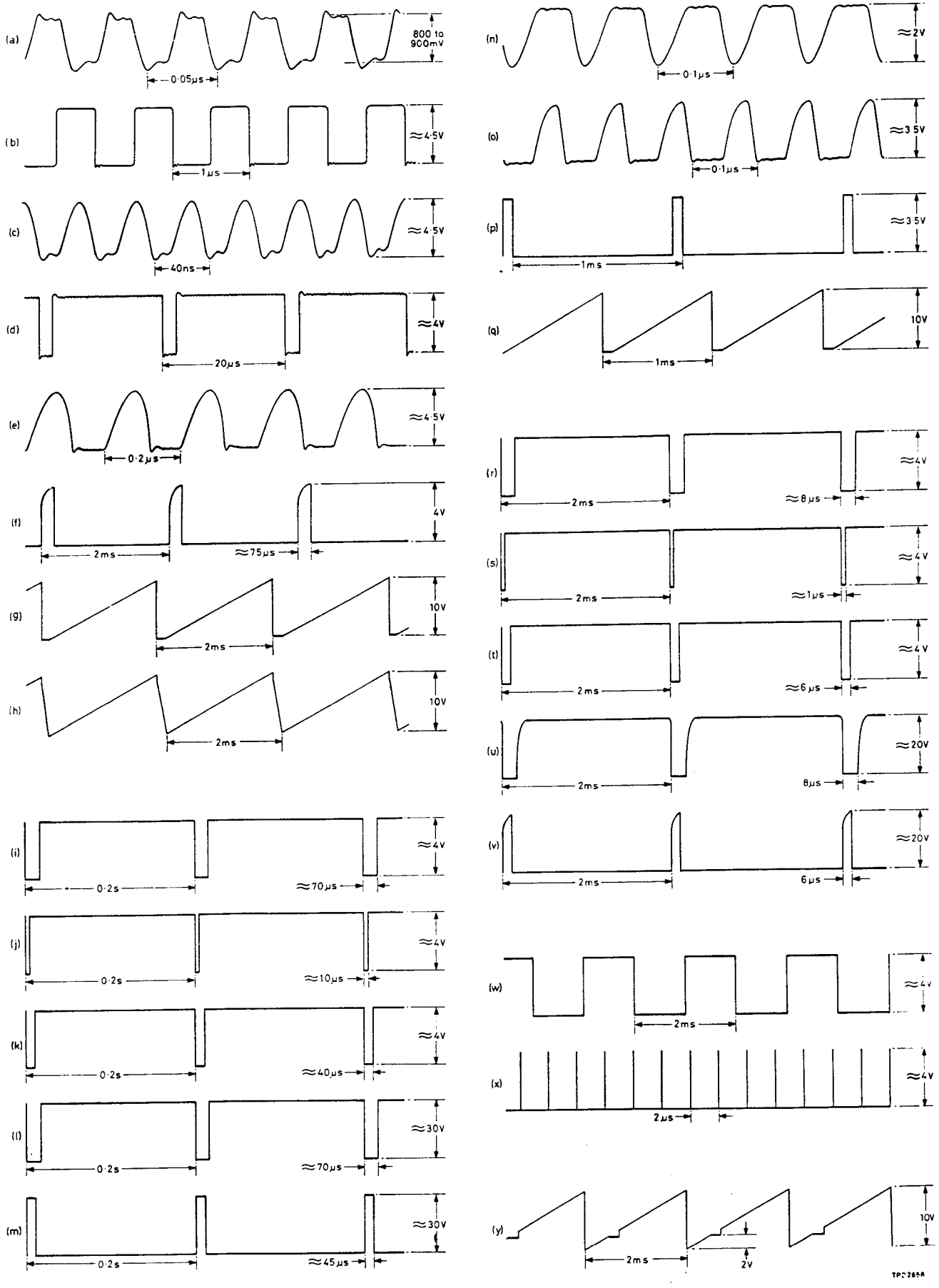


Fig. 4.3 Typical waveforms

pin 6 on IC10 and pin 6 on IC11 and check that the waveforms are as Figs. 4.3 (r), 4.3 (s) and 4.3 (t) respectively.

(2) Connect the oscilloscope in turn to collector of TR15 and TR17 and check that the waveforms are as Figs. 4.3 (u) and 4.3 (v).

4.7.11 Lock indicator circuits (A3)

Test equipment : items b, c.

(1) With TF 2015 locked to TF 2171 at any frequency connect the oscilloscope to pin 2 on IC12 and check that the waveform is as Fig. 4.3 (w).

(2) Connect the oscilloscope in turn to pin 6 on IC13, pin 3 on IC14 and pin 6 on IC14 and check that the waveform at each point is as Fig. 4.3 (x).

(3) Connect the oscilloscope to pin 2 on IC14 and check that this point is at low logic level.

4.7.12 Interface amplifier (A3)

Test equipment : item a.

(1) Disconnect the interconnecting cables between TF 2171 and TF 2015.

(2) Disconnect the coaxial cable from pin 9 and connect pin 9 to pin 8.

(3) Connect two 47 kΩ ±1% resistors in series between pins 1 and 5.

(4) Set the LOCK switch UP (lock) then with the multimeter set at 50 μA f.s.d. and connected between pin 2 and the junction of the 47 kΩ resistors, check that the multimeter indicates zero current. If necessary, change the value of either R13 or R17 to obtain a zero current result.

(5) Remove the resistors and the connection between pins 8 and 9 and reconnect the coaxial cable.

4.8 CLEANING ROTARY SWITCHES

These should be cleaned two or three times a year depending upon use. Only benzene or white spirit (not carbon tetrachloride) should be used. After cleaning, carefully wipe the contacts with a lubricant of 1% solution petroleum jelly in white spirit.

4.9 ADDITIONAL INFORMATION

If further information is required please write to or telephone Marconi Instruments Limited, Service Division - see address on back cover - or contact our nearest representative, quoting the type and serial number on the data plate on rear of the instrument.

If the instrument is being returned for repair please indicate clearly the nature of the fault or the work you require to be done.

Chapter 6

Replaceable parts

Introduction

Each sub-assembly or printed circuit board in this instrument has been allocated a unit identification in the sequence A0 to A4.

The complete component reference carries its unit number as a prefix e.g. A1C1 but for convenience in the text and on circuit diagrams the prefix is not used.

However, when ordering replacements or in correspondence the complete component reference must be quoted.

One or more of the components fitted in this instrument may differ from those listed in this chapter for any of the following reasons :

(a) Components indicated by a † have their value selected during test to achieve particular performance limits.

(b) Owing to supply difficulties, components of different value or type may be substituted provided the overall performance of the instrument is maintained.

(c) As part of a policy of continuous development, components may be changed in value or type to obtain detail improvements in performance.

When there is a difference between the component fitted and the one listed, always use as a replacement the same type and value as found in the instrument.

Ordering

When ordering replacements, address the order to our Service Division (address on rear cover) or nearest agent and specify the following for each component required.

(1) Type* and serial number of instrument.
(2) Complete circuit reference.
(3) Description.
(4) MI code.

* as given on the serial number label at the rear of the instrument; if this is superseded by a model number label, quote the model number instead of the type number.

Component references

The components are listed in alphanumerical order and the following abbreviations are used:

C	:	capacitor
Carb	:	carbon
Cer	:	ceramic
Cerm	:	cermet
D	:	semiconductor diode
Elec	:	electrolytic
FS	:	fuse
IC	:	integrated circuit (package)
L	:	inductor
Max	:	maximum
ME	:	meter
Met	:	metal
Mic	:	mica
Min	:	minimum value
Ox	:	oxide
PL	:	plug
Plas	:	plastic dielectric
R	:	resistor
S	:	switch
SK	:	socket
T	:	transformer
Tant	:	tantalum
TP	:	terminal
TR	:	transistor
Var	:	variable
WW	:	wirewound
XO	:	crystal oscillator
†	:	value selected during test; nominal value listed
Ø	:	feed-through component
W	:	watts at 70°C

Unit A0

When ordering, prefix circuit reference with A0

C1 to C21	Cer Ø 0.001μF -20+80% 500V		26373-733

Circuit reference	Description	M.I. code
C22	Elec 4.7μF -20+100% 63V	26415-801
C23	Elec 2200μF -10+100% 40V	26426-086
C24	Elec 2200μF -10+100% 40V	26426-086
C25	Elec 4700μF -10+50% 16V	26426-091
C26	Elec 1000μF -20+100% 63V	26426-081
C27	Tant 0.47μF 20% 35V	26486-207
C28	Tant 0.47μF 20% 35V	26486-207
C29	Plas 0.47μF 10% 100V	26582-215
C30	Tant 0.47μF 20% 35V	26486-207
C31	Tant 0.47μF 20% 35V	26486-207
C32	Tant 0.47μF 20% 35V	26486-207
C33	Elec 470μF -20+100% 25V	26415-822
D1	LED (on/off indicator)	28624-104
D2	LED (out of lock indicator)	28624-104
FS1	250mA (slow-blow) 190-264V	23411-045
	or 500mA (slow-blow) 95-130V	23411-046
FS2	250mA (slow-blow) 190-264V	23411-045
	or 500mA (slow-blow) 95-130V	23411-046
IC1	Regulator 12V	28461-708
IC2	Regulator 5V	28461-704
IC3	Regulator 24V	28461-710
L1	Filter coil 10μH	23642-555
L2	Filter coil 10μH	23642-555
L3	Filter coil 6μH	44290-023
L4	Filter coil 6μH	44290-023
L5	Filter coil 10μH	23642-555
L6	Filter coil 10μH	23642-555
L7	Filter coil 10μH	23642-555
L8	Filter coil 10μH	23642-555
L9	Filter coil 6μH	44290-023
L10	Filter coil 6μH	44290-023
L11	Filter coil 10μH	23642-555
L12	Filter coil 10μH	23642-555
L13	Filter coil 10μH	23642-555
L14	Filter coil 10μH	23642-555

Circuit reference	Description	M.I. code
R1	Met film 82Ω 2% ¼W	24773-247
R5	Var cermet 1kΩ 10% 1W	25748-499
ME1	Meter	44559-011
ME1	Meter board assembly consisting of	44828-285
R1	Met film 200Ω 2% ¼W	24773-256
R2	Met film 200Ω 2% ¼W	24773-256
R3	Var cermet 1kΩ 10% ½W	25711-503
SA	Frequency switch Hz x 100	44340-052
SB	Frequency switch kHz	44340-052
SC	Frequency switch kHz x 10	44340-052
SD	Frequency switch kHz x 100	44340-052
SE	Frequency switch MHz	44340-052
SF	Frequency switch MHz x 10	44340-052
SG	Frequency switch MHz x 100	44340-052
SH	Supply switch DPDT	23462-258
SJ	Voltage selector switch 230V/115V	23467-161
SK	Lock switch DPDT	23462-258
SL	1 MHz - STD switch DPDT	23462-331
T1	Mains transformer	43490-015
TR1	Transistor MJ 491	28435-876

Unit A1

When ordering, prefix circuit reference with A1

	Complete board	44827-303
C1	Cer 0.001μF -20+80% 500V	26383-242
C3	Cer 0.001μF -20+80% 500V	26383-242
C4	Cer 0.01μF -20+80% 100V	26383-055
C5	Cer 0.001μF -20+80% 500V	26383-242

For symbols and abbreviations see introduction to this chapter

Circuit reference	Description	M.I. code
C7	Cer 0.001μF -20+80%	26383-242
C8	Cer 0.01μF -20+80% 100V	26383-055
C9	Cer 0.001μF -20+80% 500V	26383-242
C11	Cer 0.001μF -20+80% 500V	26383-242
C12	Elec 220μF -20+100% 10V	26415-817
C13	Cer 0.001μF -20+80% 500V	26383-242
C14	Cer 6.8pF ±0.5pF 500V	26343-116
C15	Cer 0.001μF -20+80% 500V	26383-242
C16	Cer 0.001μF -20+80% 500V	26383-242
C17	Cer 0.001μF -20+80% 500V	26383-242
C18	Cer 0.01μF -20+80% 100V	26383-055
C19	Cer 0.01μF -20+80% 100V	26383-055
C20	Cer 0.01μF -20+80% 100V	26383-055
C21	Cer 0.01μF -20+80% 100V	26383-055
C22	Cer 0.01μF -20+80% 100V	26383-055
C23	Cer 82pF 10% 500V	26343-165
C24	Plas 0.22μF 10% 63V	26582-406
C25	Cer 0.01μF -20+80% 100V	26383-055
C26	Cer 0.01μF -20+80% 100V	26383-055
C27	Cer 0.01μF -20+80% 100V	26383-055
C28	Cer 0.01μF -20+80% 100V	26383-055
C29	Cer 0.01μF -20+80% 100V	26383-055
C30	Cer 0.01μF -20+80% 100V	26383-055
C31	Cer 0.01μF -20+80% 100V	26383-055
C32	Cer 0.01μF -20+80% 100V	26383-055
C33	Cer 0.01μF -20+80% 100V	26383-055
C34	Cer 0.01μF -20+80% 100V	26383-055
C35	Cer 0.01μF -20+80% 100V	26383-055
C36	Cer 0.01μF -20+80% 100V	26383-055
C37	Cer 0.01μF -20+80% 100V	26383-055
C38	Cer 0.01μF -20+80% 100V	26383-055
C39	Cer 0.01μF -20+80% 100V	26383-055
C40	Cer 0.01μF -20+80% 100V	26383-055
C41	Cer 0.01μF -20+80% 100V	26383-055
C42	Cer 0.01μF -20+80% 100V	26383-055
C43	Cer 0.01μF -20+80% 100V	26383-055
C44	Cer 0.01μF -20+80% 100V	26383-055
D1	Diode MBD 102	28349-004
D2	Diode MBD 102	28349-004
D3	Diode MBD 102	28349-004
D4	Diode MBD 102	28349-004
D5	Diode MBD 102	28349-004
D6	Diode Zener 156006A	28371-549
IC1	High speed counter	28464-007
IC2	JK bistable (120 MHz)	28462-006
IC3	High speed JK bistable	28462-014
IC4	High speed JK bistable	28462-014
IC5	Hex inverter	28469-159
IC6	8-input NAND gate	28466-330
IC7	8-input NAND gate	28466-330
IC8	High speed counter	28464-004
IC9	High speed counter	28464-004
IC10	High speed counter	28464-004
IC11	High speed counter	28464-004
IC12	High speed counter	28464-004
IC13	High speed counter	28464-004
IC14	High speed counter	28464-004
IC15	High speed counter	28464-004
IC16	High speed counter	28464-004
IC17	High speed counter	28464-004
IC18	High speed counter	28464-004
IC19	High speed counter	28464-004
IC20	High speed JK bistable	28462-014
IC21	High speed JK bistable	28462-014
IC22	8-input NAND gate	28466-330

For symbols and abbreviations see introduction to this chapter

Circuit reference	Description	M.I. code
R1	Met film 39Ω 2% ¼W	24773-239
R2	Met film 24 kΩ 2% ¼W	24773-306
R3	Met film 240Ω 2% ¼W	24773-258
R4	Met film 680Ω 2% ¼W	24773-269
R6	Met film 91Ω 2% ¼W	24773-248
R7	Met film 24kΩ 2% ¼W	24773-306
R8	Met film 240Ω 2% ¼W	24773-258
R9	Met film 680Ω 2% ¼W	24773-269
R11	Met film 91Ω 2% ¼W	24773-248
R12	Met film 24kΩ 2% ¼W	24773-306
R13	Met film 240Ω 2% ¼W	24773-258
R14	Met film 680Ω 2% ¼W	24773-269
R16	Met film 68Ω 2% ¼W	24773-245
R17	Met film 620Ω 2% ¼W	24773-268
R18	Met film 560Ω 2% ¼W	24773-267
R19	Cerm Var 100Ω 10% ½W	25711-545
R20	Met film 560Ω 2% ¼W	24773-267
R21	Cerm Var 1kΩ 10% ½W	25711-544
R22	Met film 390Ω 2% ¼W	24773-263
R23	Met film 3.3kΩ 2% ¼W	24773-285
R24	Met film 220Ω 270 ¼W	24773-257
R25	Met film 6.8kΩ 2% ¼W	24773-293
R26	Met film 430Ω 2% ¼W	24773-264
R27	Met film 10kΩ 2% ¼W	24773-297
R28	Met film 10kΩ 2% ¼W	24773-297
R29	Met film 10kΩ 2% ¼W	24773-297
R30	Met film 10kΩ 2% ¼W	24773-297
R31	Met film 10kΩ 2% ¼W	24773-297
R32	Met film 10kΩ 2% ¼W	24773-297
R33	Met film 10kΩ 2% ¼W	24773-297
R34	Met film 10kΩ 2% ¼W	24773-297
R35	Met film 10kΩ 2% ¼W	24773-297
R36	Met film 10kΩ 2% ¼W	24773-297
R37	Met film 10kΩ 2% ¼W	24773-297
R38	Met film 10kΩ 2% ¼W	24773-297
R39	Met film 10kΩ 2% ¼W	24773-297
R40	Met film 10kΩ 2% ¼W	24773-297
R41	Met film 10kΩ 2% ¼W	24773-297
R42	Met film 10kΩ 2% ¼W	24773-297
R43	Met film 10kΩ 2% ¼W	24773-297
R44	Met film 10kΩ 2% ¼W	24773-297
R45	Met film 10kΩ 2% ¼W	24773-297
R46	Met film 10kΩ 2% ¼W	24773-297
R47	Met film 10kΩ 2% ¼W	24773-297
R48	Met film 10kΩ 2% ¼W	24773-297
R49	Met film 10kΩ 2% ¼W	24773-297
R50	Met film 10kΩ 2% ¼W	24773-297
R51	Met film 10kΩ 2% ¼W	24773-297
R52	Met film 10kΩ 2% ¼W	24773-297
R53	Met film 10kΩ 2% ¼W	24773-297
R54	Met film 10kΩ 2% ¼W	24773-297
TR1	Transistor BFY 90	28452-157
TR2	Transistor BFY 90	28452-157
TR3	Transistor BFY 90	28452-157
TR4	Transistor BSX 20	28452-197

Unit A2

When ordering, prefix circuit reference with A2

	Complete board	44827-304
C1	Plas 0.01μF 10% 100V	26582-211
C2	Plas 0.047μF 10% 250V	26582-206
C3	Plas 0.01μF 10% 250V	26582-202
C4	Cer 0.01μF -20+80% 100V	26383-055
C5	Elec 4.7μF -20+100% 63V	26415-801
C6	Plas 0.1μF 10% 100V	26582-211
C7	Plas 0.0012μF 2% 125V	26516-512

For symbols and abbreviations see introduction to this chapter

Circuit reference	Description	M.I. code
C8	Cer 0.01μF -20+80% 100V	26383-055
C9	Cer 0.01μF -20+80% 100V	26383-055
C10	Plas 0.0068μF 2% 125V	26516-924
C11	Cer 0.01μF -20+80% 100V	26383-055
C12	Cer 0.01μF -20+80% 100V	26383-055
C13	Elec 4.7μF -20+100% 63V	26415-801
C14	Cer 0.01μF -20+80% 100V	26383-055
C15	Plas 0.022μF 10% 250V	26582-204
C16	Cer 0.01μF -20+80% 100V	26383-055
C17	Cer 0.01μF -20+80% 100V	26383-055
C18	Cer 0.01μF -20+80% 100V	26383-055
C19	Plas 18pF ±2pF 125V	26516-028
C20	Cer 0.01μF -20+80% 100V	26383-055
C21	Plas 1.0μF 10% 63V	26582-414
C22	Cer 0.01μF -20+80% 100V	26383-055
C23	Cer 0.01μF -20+80% 100V	26383-055
C24	Cer 0.01μF -20+80% 100V	26383-055
C25	Cer 0.1μF -25+50% 30V	26383-031
C26	Elec 470μF -20+100% 10V	26415-821
C27	Plas 0.1μF 10% 100V	26582-211
C28	Cer 0.01μF -20+80% 100V	26383-055
C29	Elec 220μF -20+100% 10V	26415-817
C30	Plas 0.002μF 10% 250V	26582-204
C31	Plas 0.0012μF 2% 125V	26516-512
C32	Cer 0.01μF -20+80% 100V	26383-055
C33	Cer 0.01μF -20+80% 100V	26383-055
C34	Plas 0.1μF 10% 100V	26582-211
C35	Cer 0.01μF -20+80% 100V	26383-055
C36	Plas 0.047μF 10% 250V	26582-206
C37	Plas 150pF ±2pF 125V	26516-287
C38	Plas 100pF ±2pF 125V	26516-241
C39	Cer 0.01μF -20+80% 100V	26383-055
C40	Cer 0.01μF -20+80% 100V	26383-055
C41	Cer 0.01μF -20+80% 100V	26383-055
C42	Plas 820pF ±2pF 125V	26516-462
C43	Elec 22μF -20+100% 25V	26415-805
C44	Cer 0.01μF -20+80%	26383-055
C45	Cer 0.01μF -20+80%	26383-055
C46	Plas 0.1μF 10% 100V	26582-211
C47	Plas 0.33μF 10% 100V	26582-213
C48	Plas 150pF ±2pF 125V	26516-287
C49	Cer 0.001μF -20+80% 500V	26383-242
C50	Elec 470μF -20+100% 10V	26415-821
C51	Cer 0.01μF -20+80% 100V	26383-055
C52	Cer 0.01μF -20+80% 100V	26383-055
C53	Cer 0.1μF -20+50% 30V	26383-031
C54	Cer 0.001μF -20+80% 500V	26383-242
C55	Cer 0.001μF -20+80% 500V	26383-242
C56	Cer 0.001μF -20+80% 500V	26383-242
C57	Cer 0.001μF -20+80% 500V	26383-242
D1	Diode Var carb BB105A	28381-096
D2	Diode Zener Z5B5-1	28371-403
D3	Diode 1N 4148	28336-676
D4	Diode 1N4148	28336-676
D5	Diode 1N4148	28336-676
IC1*	Monostable	28468-303
IC2*	Monostable	28468-303
IC3	Monostable	28468-303
IC4	Decade counter (2-5-10)	28464-002
IC5	Decade counter (2-5-10)	28464-002
IC6	Decade counter (2-5-10)	28464-002
IC7	Decade counter (2-5-10)	28464-002

* NOTE. Because of variation between batches of IC type 74122, giving rise to the risk of double triggering, a 1000 pF disc capacitor (MI code 26383-242) may be fitted between pins 6 and 7. If an IC with such a capacitor is replaced it is recommended that the capacitor should be transferred to the new IC.

Circuit reference	Description	M.I. code
IC8	Dual 4 input NAND gate	28466-324
IC9*	Monostable	28468-303
IC10*	Monostable	28468-303
IC11	Monostable	28468-303
IC12	Dual JK bistable	28462-013
IC13	Dual JK bistable	28462-013
IC14	Monostable	28468-303
IC15	Decade counter (2-5-10)	28464-002
IC16	Decade counter (2-5-10)	28464-002
IC17	Decade counter (2-5-10)	28464-002
IC18	Decade counter (2-5-10)	28464-002
IC19	Dual 4 input NAND gate	28466-324
L1	Inductor assembly	44278-217
L2	RF choke 330μH	23642-564
R1	Met film 100kΩ 2% ¼W	24773-321
R2 †	Met film 6.8kΩ 2% ¼W	24773-293
R3	Cerm Var 2.2kΩ 10% ½W	25711-547
R4	Met film 1.8kΩ 2% ¼W	24773-279
R6	Met film 1.8kΩ 2% ¼W	24773-279
R7	Met film 22kΩ 2% ¼W	24773-305
R8	Met film 1kΩ 2% ¼W	24773-273
R9	Met film 820Ω 2% ¼W	24773-271
R10	Met film 1.8kΩ 2% ¼W	24773-279
R11	Met film 3.9kΩ 2% ¼W	24773-287
R12	Met ox 2.7kΩ 2% ½W	24573-083
R13	Met ox 560kΩ 2% ½W	24573-139
R14	Met film 22kΩ 2% ¼W	24773-305
R15	Met film 22kΩ 2% ¼W	24773-305
R16	Met film 6.8kΩ 2% ¼W	24773-293
R17	Met ox 4.7kΩ 2% ½W	24573-089
R18	Met ox 560kΩ 2% ½W	24573-139
R19	Met film 3.3kΩ 2% ¼W	24773-285
R20	Met film 10kΩ 2% ¼W	24773-297
R21	Met film 4.7kΩ 2% ¼W	24773-289
R22	Met film 820Ω 2% ¼W	24773-271
R23	Met film 470Ω 2% ¼W	24773-265
R24	Met film 4.7kΩ 2% ¼W	24773-289
R25	Met ox 620kΩ 2% ½W	24573-140
R26	Met film 120kΩ 2% ¼W	24773-323
R27	Met film 120kΩ 2% ¼W	24773-323
R28	Met film 820Ω 2% ¼W	24773-271
R29	Met film 470Ω 2% ¼W	24773-265
R30	Met film 10kΩ 2% ¼W	24773-297
R31	Met film 4.7kΩ 2% ¼W	24773-289
R32	Met film 22kΩ 2% ¼W	24773-305
R33	Met film 1kΩ 2% ¼W	24773-273
R34	Met film 100kΩ 2% ¼W	24773-321
R35 †	Met film 6.8kΩ 2% ¼W	24773-293
R36	Cerm Var 2.2kΩ 10% ½W	25711-547
R37	Met film 22kΩ 2% ¼W	24773-305
R38	Met film 1kΩ 2% ¼W	24773-321
R39	Met film 470Ω 2% ¼W	24773-265
R40	Met film 1.2kΩ 2% ¼W	24773-275
R41	Met film 3.9kΩ 2% ¼W	24773-287
R42	Met ox 2.7kΩ 2% ½W	24573-083
R43	Met film 22kΩ 2% ¼W	24773-305
R44	Met film 22kΩ 2% ¼W	24773-305
R45	Met film 22kΩ 2% ¼W	24773-305
R46	Met film 10kΩ 2% ¼W	24773-321
R47	Met film 3.9kΩ 2% ¼W	24773-287
R48	Met ox 2.7kΩ 2% ½W	24573-083
R49	Met film 100Ω 2% ¼W	24773-249
R50	Met film 22kΩ 2% ¼W	24773-321
R51	Met film 3.3kΩ 2% ¼W	24773-285
R52	Met film 1kΩ 2% ¼W	24773-273
R53	Met film 1kΩ 2% ¼W	24773-273
R54	Met film 82Ω 2% ¼W	24773-247
R55	Met film 27kΩ 2% ¼W	24773-307
TR1	Transistor BC 107	28455-437
TR2	Transistor BF 244B	28459-011

For symbols and abbreviations see introduction to this chapter

Circuit reference	Description	M.I. code
TR3	Transistor BC 107	28455-437
TR4	Transistor BC 107	28455-437
TR5	Transistor BF 244B	28459-011
TR6	Transistor BC 107	28455-437
TR7	Transistor BF 244B	28459-011
TR8	Transistor BFW11	28459-012
TR9	Transistor BSX 20	28452-197
TR10	Transistor BSX 20	28452-197
TR11	Transistor BSX 20	28452-197
TR12	Transistor BC 107	28455-437
TR13	Transistor BF 244B	28459-011
TR14	Transistor BC 107	28455-437
TR15	Transistor BC 107	28455-437
TR16	Transistor BF 244B	28459-011
TR17	Transistor BC 107	28455-437
TR18	Transistor BF 244B	28459-011
TR19	Transistor BF 244B	28459-011
TR20	Transistor BC107	28455-437
X01	Crystal unit 10.02 MHz	28311-774
X02	Crystal oscillator 5MHz	44529-060

Unit A3

When ordering, prefix circuit reference with A3

	Complete board	44827-305
APC1	Analogue photo coupler	25687-501
C1	Elec 47μF -20+100% 40V	26415-810
C2	Plas 1μF 10% 100V	26582-217
D1	Diode 1N 4148	28336-676
D3	Diode 1N 4148	28336-676
D4	Diode 1N 4148	28336-676
R1	Met film 3.9kΩ 2% ¼W	24773-287
R2	Met film 220Ω 2% ¼W	24773-257
R3	Met film 68Ω 2% ¼W	24773-245
R4	Met film 15kΩ 2% ¼W	24773-301
R5	Met film 62kΩ 2% ¼W	24773-316
R6	Met film 4.3kΩ 2% ¼W	24773-288
R7	Met film 56kΩ 2% ¼W	24773-315
R8	Met film 56kΩ 2% ¼W	24773-315
R9	Met film 100kΩ 2% ¼W	24773-321
R10	Met film 20kΩ 2% ¼W	24773-304
R11	Met film 39kΩ 2% ¼W	24773-311
R12	Met film 100kΩ 2% ¼W	24773-321
R13* †	Met film 330kΩ 2% ¼W	24773-261
R14	Met film 20kΩ 2% ¼W	24773-304
R15	Met film 39kΩ 2% ¼W	24773-311
R16	Met film 100kΩ 2% ¼W	24773-321
R17* †	Met film 330kΩ 2% ¼W	24773-261
TR1	Transistor BCY 71	28435-235
TR2	Transistor BCY 71	28435-235
TR3	Transistor BC 109	28452-777
TR4	Transistor BC 109	28452-777
TR5	Transistor BCY 71	28435-235
TR6	Transistor BC 109	28452-777

* Only one SIC resistor, either R13 or R17, is required to be changed to obtain balance - see Sect. 4.7.12.

Unit A4

When ordering, prefix circuit reference with A4

	Complete board	44827-306
C1	Elec 4.7μF -20+100% 63V	26415-801
C2	Elec 470μF -20+100% 25V	26415-822
D1	Diode 1N 4004	28357-028
D2	Diode 1N 4004	28357-028
D3	Diode 1N 4004	28357-028

For symbols and abbreviations see introduction to this chapter

Circuit reference	Description	M.I. code
D4	Diode 1N 4004	28357-028
D5	Diode 1N 5401	28355-723
D6	Diode 1N 5401	28355-723
D7	Diode 1N 5401	28355-723
D8	Diode 1N 5401	28355-723
D9	Diode 1N 4004	28357-028
D10	Diode 1N 4004	28357-028
D11	Diode 1N 4004	28357-028
D12	Diode 1N 4004	28357-028
D13	Diode Zener Z5B18	28372-583
IC1	Operational amplifier μA 741	28461-304
R1	Met ox 390Ω 2% ½W	24573-063
R2	Met ox 330Ω 2% ½W	24573-061
R3	WW Var 47Ω 10% 1W	25811-011
R4	Met ox 470Ω 2% ½W	24573-065
R5	Met ox 10kΩ 2% ½W	24573-097
R6	Met ox 10kΩ 2% ½W	24573-097
RL1	Relay	23486-427

Circuit reference	Description	M.I. code
Miscellaneous items		
	Cap and chain BNC	23443-591
	Cap and chain TNC	23444-898
	Cap and chain Conhex	23444-304
	Case clip (four)	22315-098
	Frequency switch (seven)	
	Knob	22318-333
	Knob cap	22318-334
	Dial	22318-335
	Stator	22318-336
	Carrying handle	
	Handle liner	22315-572
	Handle section	22315-575
	Handle end cap (two)	22315-573
	Jack TNC (SKB)	23444-742
	Mains connector (PLA)	23423-159
	Plastic stand (two rear of case)	22315-663
	Socket BNC (SKC SKD)	23443-443

For symbols and abbreviations see introduction to this chapter

Index to Units

Unit number	M.I. code	Description	Circuit diagram Fig.	Parts list page
A0		Chassis and panel components	7.1 to 7.4	24
A1	44827-303	Input amplifier and diode shaper. Prescaler and amplifier.	7.1	24
		Variable ratio frequency dividers VRD1 and VRD2.	7.2	24
A2	44827-304	5 MHz crystal controlled oscillator and associated dividers XC2 and FD2. 10 MHz voltage tuned crystal oscillator and associated dividers XO1 and FD1. Ramp generators RG1 and RG2. Phase detectors PD1 and PD2. Sample and hold drivers DR1 and DR2. Lock indicator circuits.	7.3	26
A3	44827-305	Interface circuits	7.1	29
A4	44827-306	Power supplies	7.4	29

Chapter 7

Circuit diagrams

Circuit notes

1. COMPONENT VALUES

Resistors : No suffix = ohms, k = kilohms, M = megohms.

Capacitors : No suffix = microfarads, p = picofarads.

† value selected during test, nominal value shown.

2. VOLTAGES

Shown in italics adjacent to the point to which the measurement refers. See section 4.1 for conditions.

3. SYMBOLS


arrow indicates clockwise rotation of of knob.

etc., external front or rear panel marking.

tag on printed board.


other tag.


preset control.

unit identification number.

These symbols are used to identify branches of the power supply circuitry but have no particular physical reality on the printed boards.

point marked with this symbol is connected to and receives power from point marked with this symbol

4. CIRCUIT REFERENCES

These are, in general, given in abbreviated form - see Chapter 6.

5. SWITCHES

Rotary switches are drawn schematically.
Letters indicate control knob settings.
1F = 1st section (front panel), front
1B = 1st section, back
2F = 2nd section, front
etc.

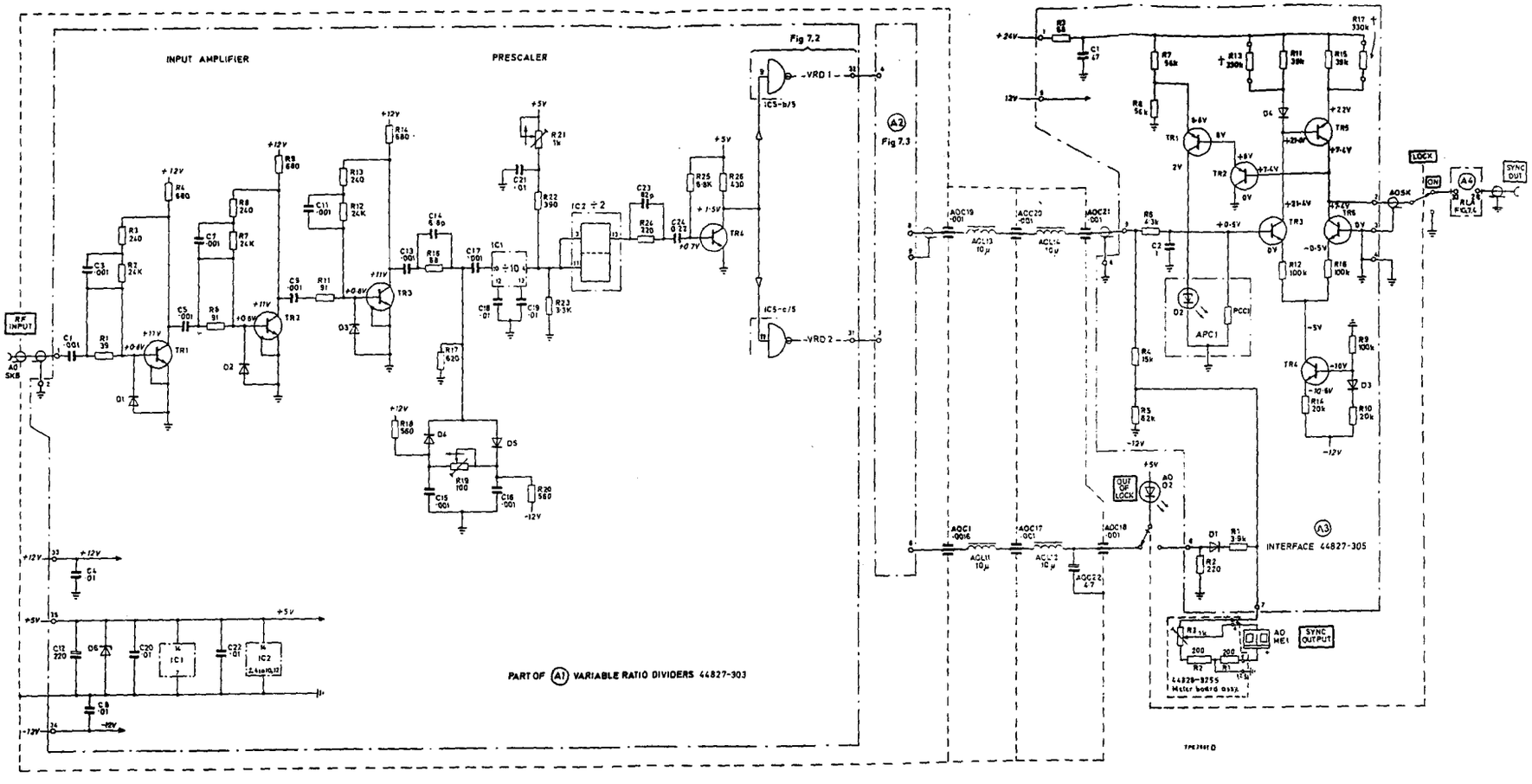


Fig. 7.1 Input amplifier, prescaler and interface

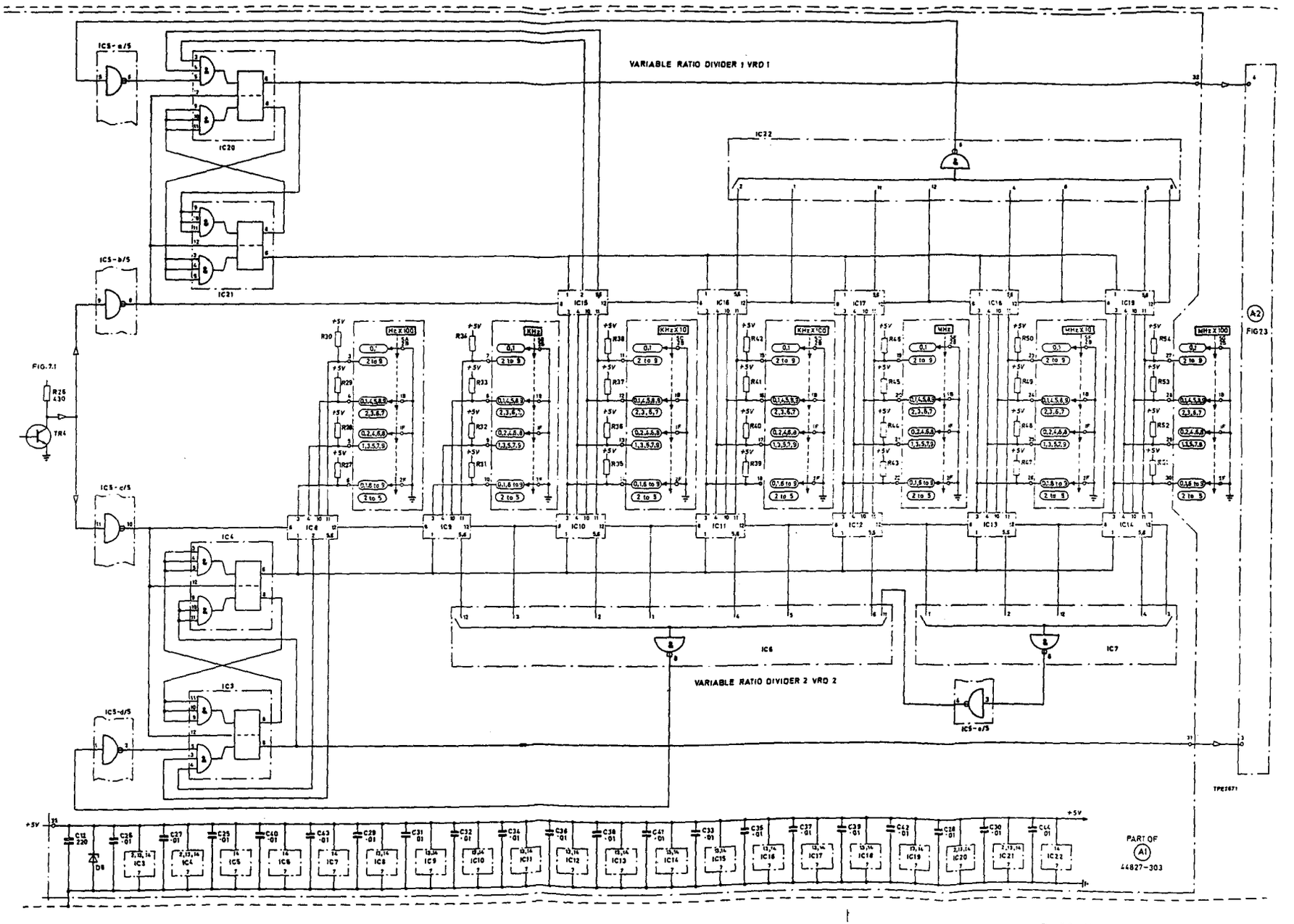


Fig. 7.2 Variable ratio dividers

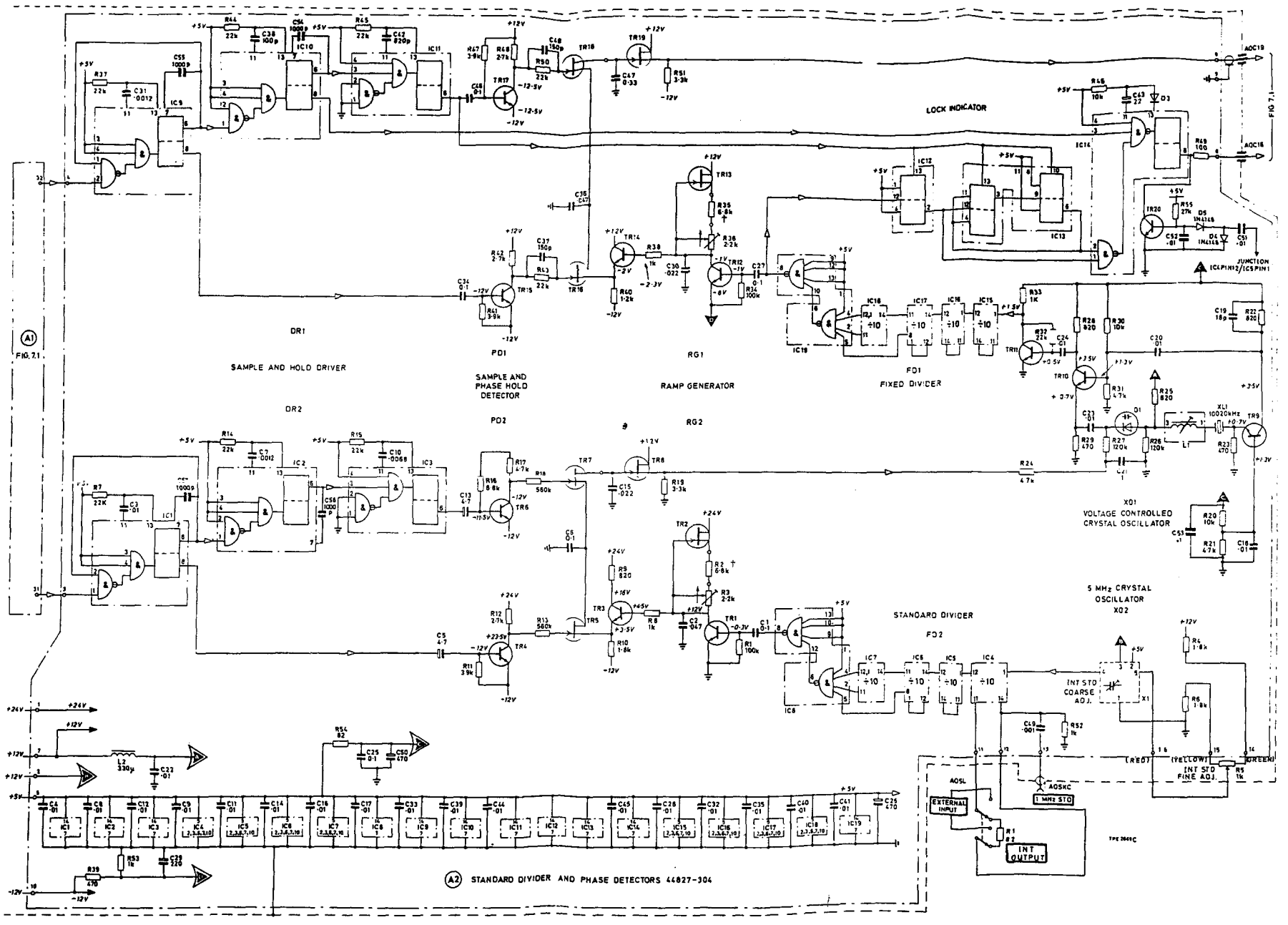


Fig. 7.3 Standard and fixed dividers and phase detector

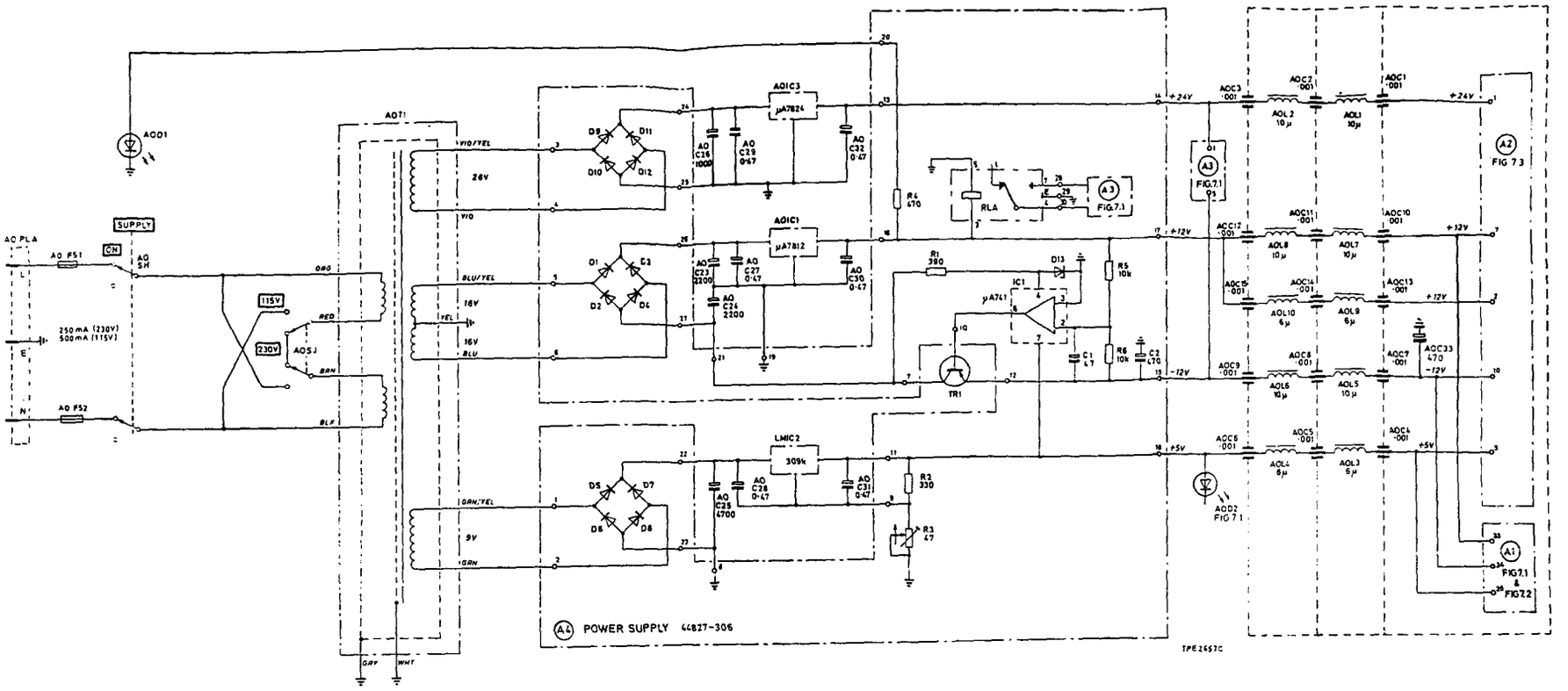


Fig. 7.4 Power supplies