2.4.9.5 Service Request (SRQ) when using the ZPV + TEK 4051/52

The ZPV can send an SRQ message if, for example, it is not in sync, the measurement range is exceeded, etc. To this end,

1) set switch S2.6 on the IEC interface board to OFF (cf. 2.4.5).

2) use the TEK to set the ZPV for external trigger operation ("TE") and to initiate a test cycle ("LR" or secondary address). Cf. 2.4.9.3.

Example: (TEK 4051/52)

```
100 ON SRQ THEN 2ØØ
110 PRINT @ 26: "TE"          External trigger operation
120 PRINT @ 26, 3: X1, X2     Initiate test cycle; output results
130 PRINT @ 26: "TI"          Internal trigger operation
140 END
:
200 POLL A, B; 26             Serial poll
210 PRINT A, B                Printout of device list number (A), and
                              status byte (B)
220 REM SRQ REMOVE FAULT      e.g., by altering test level
230 RETURN
```

NOTE: Relationship between status byte (B) after a SRQ, and the readout on the ZPV (cf. Table 2-7).

ZPV readout	Status byte (B) 4051/4052
A??	96
A>>	80
B>>	72
B<<	68
A<<	66 (ZPV-E1 only)

2.4.9.6 Increasing the Test Rate in Programmed Operation

The test rate of the ZPV can be increased by the commands

GØ	Tendency indication off
KØ	Recorder output off
SH	Fast test rate

Switchover to normal operation is achieved by the commands

G1	Tendency indication on
K1	Recorder output on
SL	Normal test rate

Example: Switching the ZPV over to fast test rate:

IECOUT 26, "GØKØSH" (PPC)

PRINT @ 26: "GØKØSH" (TEK 4051/52)

2.4.9.7 Input and Output of Reference Value for Relative Measurements

The reference value for the test result can be output from the ZPV in coded form (10 ASCII characters) and reentered in the ZPV.

Example:

Reference value output

IECOUT 26, "SR"	(PPC)	Preparation of reference value output
PRINT @ 26: "SR"	(TEK 4051/52)	
IECIN 26, A$	(PPC)	Output of reference value and storage in A$
INPUT @ 26: A$	(TEK 4051/52)	

or with a single command using secondary address 9:

IECIN 26; 9, A$ (PPC)

INPUT @ 26,9: A$ (TEK 4051/52)

Reentry of reference value in the ZPV

IECOUT 26, "TR"	(PPC)	PRINT @ 26: "TR"	(TEK 4051/52)
IECOUT 26, A$		PRINT @ 26: A$	

2.4.9.8 Phase Offset

In external trigger operation ("TE") it is possible to enter a phase value into the ZPV prior to the measurement, which is subtracted from the measured phase in the measurement. The phase offset holds only for one measurement command.

The phase offset is programmed by "POXXXX" with the value of XXXX ranging from 000.0 degrees to 360.0 degrees. The decimal point does not have to be used.

Example: (PPC)

IECOUT 26, "TEBA"	External triggering, mode B/A
IECOUT 26, "PO18ØØ"	Phase offset 180 degrees
IECIN 26;2, P	Result on lefthand readout (phase value P) P = measured phase - phase offset
IECIN 26;2, P	Result on lefthand readout (phase value P) P = measured phase since phase offset holds only for one measurement after "POXXXX" has been entered.

2.5 Measurement of Crystal Equivalent Circuit Parameters

2.5.1 General

The Vector Analyzer ZPV in conjunction with a frequency counter, an FM-DC signal generator, a control amplifier and a crystal adapter (π-network in accordance with IEC 444 or DIN 45 105) permits measurement of crystal equivalent circuit parameters.

The ZPV supplies a phase-proportional DC voltage which after amplification in the control amplifier pulls the signal generator to the series-resonance frequency of the crystal. The resonant frequency can be read off on the frequency counter.

If the keys Z and AUTO/XTRL are pressed the ZPV determines the resonant impedance of the crystal from the attenuation at resonance which is read out directly on the lefthand display.

Use of a desktop calculator with IEC-bus interface, such as Process Controller PPC, in the test assembly permits also the dynamic inductance L_1 and the dynamic capacitance C_1 to be determined.

To this end, the ZPV is programmed for a phase offset φ_o, i.e. the control loop locks at $\pm \varphi_o$. From the two frequencies at which the phase of the crystal is $\pm$ $_o$ and the resonant impedance, L_1 and C_1 are calculated by means of the desktop calculator.

To select the mode "measurement of crystal equivalent circuit parameters" press the button AUTO . Modes τ and $\Delta\tau$ must be switched off.

The following combinations can be selected:

A	AUTO	LIN/REF	Measurement of voltage in channel A relative to a reference value
B	AUTO	LIN/REF	Measurement of voltage in channel B relative to a reference value
B/A	AUTO	LIN/REF	Measurement of voltage ratio B/A relative to a reference value
Z	AUTO		Measurement of resonant impedance
Y	AUTO		Measurement of resonant admittance
S21, S12			Same as with B/A AUTO LIN/REF

The phase measurement range is limited to about $\pm 120^\circ$ in these modes .since only values between $\pm 90^\circ$ are required for measuring crystal equivalent circuit parameters.

2.5.2 Manual Measurement

2.5.2.1 Vector Measurement

Calibration

- Select B/A LIN/REF AUTO on the ZPV.
- Press the button r, φ on the ZPV.
- Adjust the nominal crystal frequency on the signal generator and select the test level.
- Press the button STOP AUTORANGING FREQ on the ZPV. The lamp lights up.
- Connect a shorting link into the $\overline{\pi}$ network in place of the crystal and press button LEVEL REF STORE . The lefthand display reads out 1.00.
- Connect a resistor into the $\overline{\pi}$ network, the resistance of which corresponds to about the resonant impedance of the crystal to be expected.
- Press the button φ, τ REF STORE on the ZPV. The righthand display reads out 0°.

Measurement

- Connect the crystal into the $\overline{\pi}$ network.
- Now the control loop pulls the crystal to the exact resonant frequency. The righthand display of the ZPV reads out 0°.
- The resonant frequency of the crystal can be read off on the frequency counter.
- The resonant impedance is given by the formula

$$Z_r = \left(\frac{1}{B/A} - 1 \right) \times 25 \qquad [\Omega]$$

where B/A is the attenuation read out on the lefthand display.

2.5.2.2 S-parameter and Z-measurement

The calibration and measurement procedures are basically the same as for the vector measurement (section 2.1). For calibration, the S21,S12 AUTO mode must however be used. The S21,S12 AUTO mode corresponds to the B/A AUTO LIN/REF. mode.

If the Z AUTO or Y AUTO mode is selected, the ZPV calculates the resonant impedance or admittance in accordance with the above formula and reads it out on the left-hand display.

2.5.3 Automatic Measurement

Program-controlled measurement is based on the same principle as manual measurement.

The controller sets the required button combinations via the IEC bus, stores the measured data and calculates from them the equivalent circuit parameters.

In automatic operation, a phase offset can be entered into the ZPV, say, for example, $\pm 45^{\circ}$, which causes the control loop to pull the signal generator to the frequency at which the phase of the crystal is not 0° but, for example, $\pm 45^{\circ}$. With the given resonant impedance Z_r, the controller can calculate the dynamic inductance L_1, the capacitance C_1 and the Q from the two 45° frequencies in accordance with the following formulae:

$$L_1 = \frac{(Z_r + 25\ \Omega) \cdot \tan\varphi}{2\pi\ (f_{+\varphi} - f_{-\varphi})}$$

$$C_1 = \frac{1}{4\pi^2 \cdot fr^2 \cdot L_1}$$

$$Q = \frac{2\pi \cdot fr \cdot C_1}{Z_r}$$

where f_r = resonant frequency

$f_{+\varphi}$ = frequency with positive phase offset

$f_{-\varphi}$ = frequency with negative phase offset

φ = phase offset (e.g. 45°)

Z_r = resonant impedance.

The IEC-bus instruction for programming a phase offset with the PPC reads

IECOUT@26: "PO....".

The decimal points stand for a figure each. For a 45° phase offset, for example, program

```
IECOUT   26 , "PØ45Ø"
```

and for -45°

```
IECOUT   26 , "P0315Ø".
```

2.5.4 Control Amplifier

Fig. 2-13 is an example of a simple control amplifier circuit. C_x, R_x, R_y, together with the deviation of the FM-DC signal generator, determine here the gain and the time constant of the control loop. In the case of high-Q crystals, the loop gain and the time constant should preferably be switch-selectable.

The control amplifier is driven from the signals obtained at the ZPV outputs CONTR. ΔF and SWEEP φ . The output voltage of the internal phase meter is available at the SWEEP φ output.

Scale: 0° corresponds to 0 V
-180° corresponds to approx. -0.5 V
$+180^{\circ}$ corresponds to approx. +0.5 V.

In addition, a reference voltage is available at the CONTR. ΔF output. This reference voltage is proportional to the reference value stored in the ZPV by means of the button φ , τ REF STORE .

Scale: 0° corresponds to 5 V
-179.9° corresponds to 0 V
$+179.9^{\circ}$ corresponds to 10 V.

If the two signals are taken to an amplifier which matches the scales to one another and subtracts the signals from one another, a voltage is obtained at its output corresponding to the phase readout in either the B/A LIN/REF AUTO or S21,S12 AUTO mode.

If a phase offset is programmed via an IEC bus instruction, the reference voltage at the CONTR. ΔF output changes accordingly, e.g. it falls by 1.25 V if an offset of 45° is programmed.

2.5.4.1 Hints for the Adjustment of the Potentiometers P1 and P2

Using a controller.
The adjustment is best made during operation, i.e. when measuring on a crystal.

If the control amplifier is not correctly adjusted, the control loop locks not exactly at 0° but, for example, at 1.3°.

Adjustment

- Adjust the potentiometer P2 (Fig. 1) so that the control loop locks exactly at 0°.
- Program a phase offset of 45°. The control loop will now lock not exactly at 45° but, for example, at 46°.
- Adjust P1 for 45°.
- Program a phase offset of 0° and adjust P2 again for 0°.
- Repeat this alternate adjustment until the control loop locks exactly at both 45° and 0°.

Without a controller
If no computer is available, proceed as follows:

- Switch the ZPV off and back on again.
- Select the B/Y LIN/REF AUTO mode.
- Shortcircuit the SWEEP φ input of the control amplifier.
- Connect the CONTR ΔF input of the control amplifier to the CONTR ΔF output of the ZPV.
- The voltage at this output is now 5.0 V.
- Vary P2 until the voltage at the output of the control amplifier is 0 V.
- Remove the shortcircuit at the SWEEP φ input and connect the input to the SWEEP φ output of the ZPV.
- Produce a phase shift of about 45° (watch the display on the ZPV), for example, by interconnecting the Group-delay cable 292.4000.00 (accessory supplied with the ZPV) at a frequency of about 2.5 MHz.
- Press the button STOP AUTORANGING FREQ. ; the associated lamp lights up.
- Adjust the output voltage of the control amplifier to 0 V by means of P1.

3. Maintenance and Repair

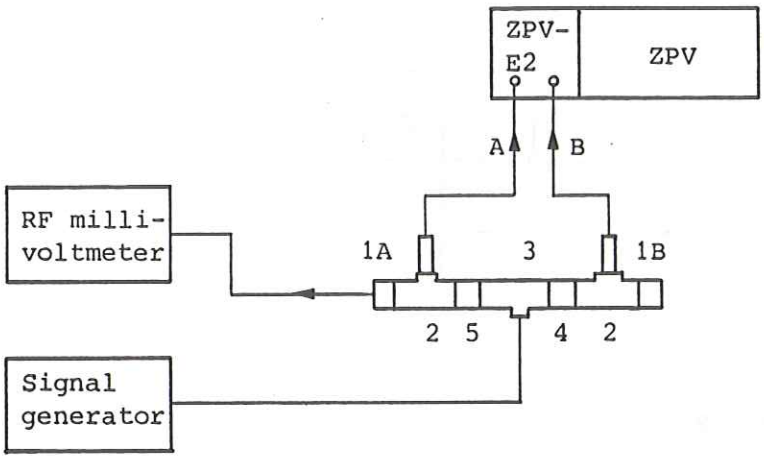
3.1 Required Measuring Equipment and Accessories

Item	○ Designation, required specifications ● Recommended R&S instrument	Type	Order No.	Use see section
1	○ Signal generator, 1 MHz, 2 V/50 Ω ● Signal generator, 10 Hz to 140 MHz	SMK	348.0010.03	3.2.1 to 3.2.4
2	○ Attenuator set 0 to 100 dB/50 Ω ● Programmable Attenuator	DPVP	214.8017.52	3.2.1 3.2.3
3	○ RF millivoltmeter 10 kHz to 10 MHz; error <1% ● RMS Voltmeter	URE	342.1214.02	3.2.1
4	○ 20-kHz signal generator with two output signals whose phase shift (-180^{o} to $+180^{o}$) is adjustable with an error of $<\pm 0.1^{o}$			3.2.3
5	○ Digital voltmeter ● Digital multimeter	UDL4	346.7800.02	3.2.4
6	○ 50-Ω termination ● Precision termination	RNA	272.4510.50	3.2.1 to 3.2.4
7	● Insertion adapter	ZPV-Z1	292.2713.50	3.2.1 to 3.2.4
8	● Feed unit	ZPV-Z2	292.2913.50	3.2.1 to 3.2.4
9	● Tuner 0.1 to 1000 MHz	ZPV-E2	292.0010.02	3.2.1 to 3.2.8
10	○ Attenuator 40 dB; 50 Ω (N) ● Attenuator (2x20 dB/50 Ω)	DNF	272.4310.50	3.2.1

3.2 Checking the Rated Specifications

3.2.1 Indication Error of Magnitude Range

Test setup



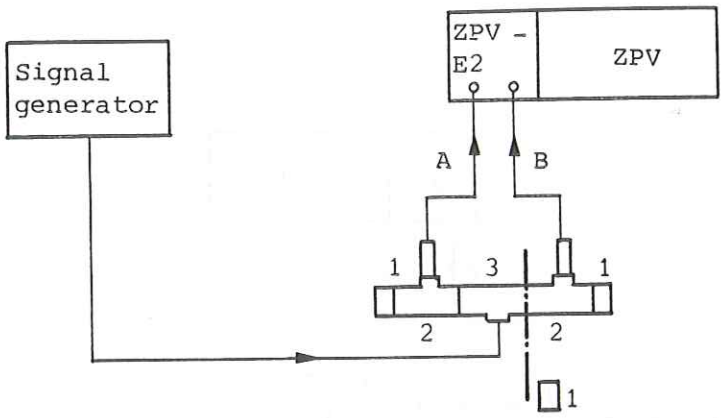
1A, 1B = 50-Ω termination
2 = insertion adapter UPV-Z1
3 = feed unit ZPV-Z2
4 = attenuator set
5 = attenuator 40 dB; 50 Ω

Select on the ZPV-E2 the frequency range 1-2 MHz and on the ZPV the operating mode A, LIN. Connect instead of the termination 1A the probe of the RF millivoltmeter (50 Ω). Adjust for an attenuation of 0 dB on the attenuator set. Set the generator frequency to 1 MHz and the level according to the RF millivoltmeter to 80 mV. The value indicated on the ZPV must not differ more than stated in the Specifications. Exchange the probes of the ZPV, select the operating mode B, LIN. and determine the deviation in the same way as in channel A.

Re-establish the initial test setup. Connect the insertion adapter A via the attenuator 5; adjust for 2 V, 50 Ω on the signal generator and 20 dB on the attenuator set. Select the operating mode B, LOG.-REF. and store the reference value in the ZPV (button LEVEL REF. STORE). Vary the attenuation of the attenuator set between 0 dB and 90 dB in 10-dB steps. The indicated values must not differ from the rating (n x 10 dB) more than stated in the Specifications (taking into account the calibration curve of the attenuator set).

3.2.2 Crosstalk Attenuation

Test setup



1 = 50-Ω termination

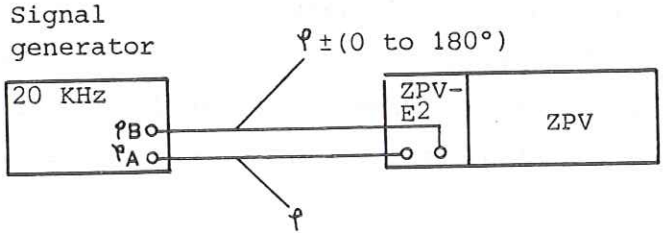
2 = insertion adapter ZPV-Z1

3 = feed unit ZPV-Z2

Select on the ZPV-E2 the frequency range 1-2 MHz and on the ZPV the operating mode B/A, LOG.-REF. Set the generator frequency to 1 MHz and the output level to 2 V/50 Ω (corresponding to 1 V at the ZPV). Store the magnitude by pressing the button LEVEL REF. STORE. The indicated magnitude should now be 0 dB. Disconnect the insertion adapter with the probe B and connect the feed unit with a termination (50 Ω). If required, terminate also the insertion adapter B. The indicated magnitude corresponds to the crosstalk signal in channel B, referred to the amplitude of the signal in channel A. The crosstalk attenuation is then equal to the absolute value of the magnitude indication and must not be smaller than stated in the Specifications.

3.2.3 Error of Phase Indication

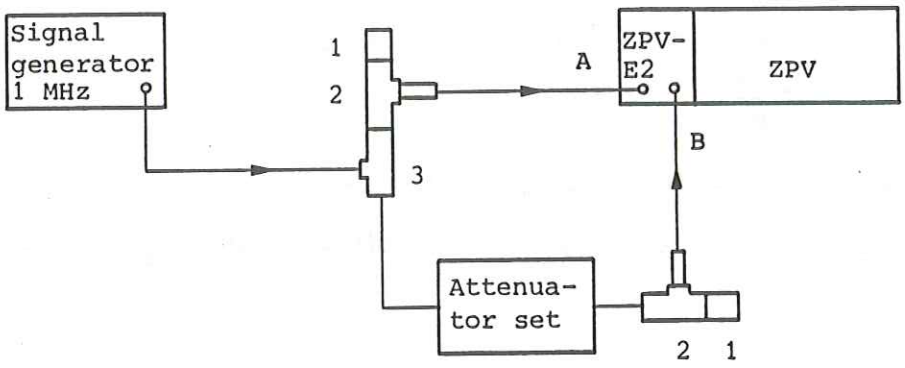
Test setup



Adjust the phase on the generator to 0° and store it on the ZPV. The indication should be 0°. Check the linearity in the entire range of indication from $+180^{\circ}$ to -180°.

Level dependence of phase indication

Test setup



1 = 50-Ω termination

2 = insertion adapter ZPV-Z1

3 = feed unit ZPV-Z2

Select on the ZPV-E2 the frequency range 1-2 MHz, set the transmitter frequency to 1 MHz and the level to ca. 1 V. Adjust 0 dB on the attenuator set and store the phase on the ZPV. The indication should be 0°. Increase the attenuation of the attenuator set in steps up to 90 dB. Taking into account the crosstalk attenuation and the variation of the electrical length of the attenuator set, the variation of the phase must not exceed the specified values.

3.2.4 Narrowband Sweeping

Test setup see 3.2.1

Set the signal generator to 1.5 MHz and vary the output level so, that the ZPV indicates 130 mV. Select on the ZPV-E2 the frequency range 1-2 MHz and switch on SWEEP. The output voltage at socket r 47 should be 730 mV ±30% (operating mode B/A). Reduce the output level of the signal generator to 40 mV (equivalent to an indication of 20 mV at the ZPV). The output voltage at socket r 47 must now be 300 mV ±30%.

The function of button 3 AMPL. STOP AUTORANGING is checked in that the ZPV signals that the minimum voltage in channel A is not reached when the signal-generator level is reduced even more.

Independent of the operating mode (A, B, B/A) the voltage +0.5 V ($+180^{\circ}$) to -0.5 V (-180°) proportional to the phase must be output at socket φ 48. In the other operating modes (SWEEP, OFF) the sockets are disconnected ($Z_{out} \rightarrow \infty$)

3.2.5 Basic Setting for Switching on AC Supply

Immediately after switching on the ZPV (button 18), the following instrument functions must be effective:

Operating mode vector measurement in channel A (A 26 lights),
dimension linear (LIN. 21 lights),
polar coordinates (r, φ 14 lights),
frequency and amplitude autoranging (4 and 6 do not light).

The readout panels 7 and 12 indicate the dimensions mV and angular degrees (φ BA).

3.2.6 Control of Analog Section

When performing the checks according to sections 3.2.1 to 3.2.4, the control of the analog section by the microcomputer is checked at the same time.

3.2.7 Operating and Indicating Elements

The instrument features 7 operating modes. In anyone mode, only a limited number of pushbuttons can be actuated, the other buttons being inhibited. The possibilities for the individual operating modes are shown below. Checking can be made by hand (switch 2 set to LOCAL or COMB.) or, if the IEC-bus option ZPV-B1 is incorporated, by means of the desktop calculator (switch 2 set to COMB. or REMOTE). The dimensions as selected by means of the respective buttons must be indicated on the display panels 7 and 12.

a) Vector measurements in channel A (button 26, control character CA)

Function	Button	Control character
Dimension linear, absolute	21	LI
Dimension linear, relative	22	ZY
Dimension logarithmic, absolute	23	DB
Dimension logarithmic, relative	24	DR
Input of reference voltage	9	LS
Input of reference phase, group delay	11	PS
Reference value indication	19	C1/CØ
Filter	20	I1/IØ
Crystal measurement	38	A1/AØ
Amplitude autoranging	3	M1/MØ
Frequency autoranging	5	Q1/QØ
Group-delay measurements	34 to 41	see Fig. 2-8

b) Vector measurements in channel B (button 25, control character CB)
see a)

c) Vector measurements, ratio B/A (button 27, control character BA)
see a)

d) s-parameters S11, S22 (button 32, control character S1)

Function	Button	Control character
Dimension linear, absolute	21	LI
Dimension linear, relative	22	ZY
Dimension logarithmic, absolute	23	DB
Reference input	10	PC
Directional coupler	31	R1/RØ
System impedance 50 Ω/75 Ω	29	05/07
Polar coordinates	15	RP
Cartesian coordinates	17	XY
Filter	20	I1/IØ
Amplitude autoranging	3	M1/MØ
Frequency autoranging	5	Q1/QØ

e) s-parameters S21, S12 (button 33, control character S2)
same as d), but without button 22.

f) Input impedance Z (button 30, control character Z1)
same as d), but without button 23.

g) Input admittance (button 28, control character Y1)
same as d), but without button 23.

The status selected in a particular operating mode remains stored when switching over to another operating mode and is restored when the original operating mode is selected again (see also section 2.3.1.2).

3.2.8 Calculator Routines

The calculator routines of the s-parameter measurement option ZPV-B2 and the group-delay measurement option ZPV-B3 are best checked with the aid of suitable test setups and some defined test items (e.g. short circuit, open circuit, termination, cable of known electrical length).

4. Circuit Description

4.1 Analog Section

The Vector Analyzer ZPV, in conjunction with the RF section, permits the measurement of the magnitude and the phase of two applied voltages in a wide frequency range. The instrument has two independent test inputs, to which the measured values can be applied and further processed. The measured values are evaluated at the fixed intermediate frequency of 20 kHz. This design features a high measuring sensitivity and phase measurement accuracy, but places exacting requirements on the frequency conversion with respect to linearity and delay in the entire frequency range. In order to meet these requirements, the ZPV is designed as an instrument with exchangeable RF sections (plug-ins).

The interface between the basic unit and the plug-in contains in addition to the necessary connections for the power supply and control of the plug-in also two independent IF inputs. This interface has also a connection for supplying the digital filter with the reference signal.

4.1.1 Amplitude Measurement

The IF signal of reference channel A is taken from the input (ST42.A4) directly to the PC board Y35, selectivity filter A, (see circuit diagram) 291.5319 S), where the signal, converted to the IF with correct phase and amplitude, is derived via the buffer stage R2-C2 and made available for monitoring purposes at the socket IF A on the rear panel.

In order to reduce the crosstalk between the reference channel A and the test channel B, the input of channel A is referred to the ground terminal of the IF input (ST42.A4). After filtering in the switch-selectable bandpass filter L1-C1 and buffering (B1) the signal is available at connector ST1.17a/b for phase and amplitude measurement.

The amplitude indication Y34 (see circuit diagram 291.5160 S) is a programmable AF millivoltmeter. The input can be electronically switched to reference channel A or test channel B. The necessary crosstalk attenuation of ca. 130 dB is obtained by the arrangement of the switching transistors T1 to T3 and T4 to

T6 and by suitable choice of levels (Fig. 4-3). Both input circuits are equipped with complementary transistors and can thus be controlled at a common point from the level converter B7.

The sensitivity is ca. 1 mV for full-scale deflection of 7.9 V and can be switch-selected in 10-dB steps up to 1 V for full-scale deflection. The two attenuator stages of 20 dB and 30 dB are designed as passive attenuator pads and are switched by T8 for 20 dB and T9 and T10 for 30 dB. A 10-dB switchover is already effected in the first amplifier stage B1 by T7. The necessary switching signal is processed by the level converter B7. The amplifier stages B1, B2, B3 are designed such that with automatic range selection by the microprocessor no dead times and delays occur. The coding of the TTL control signals for the channel and range selection can be taken from Table 4-4.

The 20-kHz IF signal from the output of B3 is applied to the full-wave rectifier B4, B5. The current of the negative halfwave is directly fed into B5. The positive halfwave is also fed into B5, but inverted by B4 and derived with double current. The main advantage of this rectifier is its good linearity and high slew rate. The other amplifier stages B6, used as active lowpass filters, provide for suppression of the spurious products of the rectification, permitting at the same time short transient response times. The DC offset can be adjusted with R32. R33 is intended for calibration of the amplitude. The analog signal is then routed via the electronic switch T1 and T2 in the selectivity filter A (Y35, circuit diagram 291.5319 S) together with the ground reference potential in order to avoid measuring errors. It is then applied to the D/A converter Y33.

The test signal of channel B is similarly processed as in the reference channel A in order to avoid any delay differences. The input signal of ST42.A1 is applied to the preamplifier B (Y24, circuit diagram 291.5219 S) and derived via the buffer stage R3-C1 for monitoring purposes. The signal is available at the socket IF B on the rear panel. The transistors T1, T2, T3, T4 form together with T11 and T12 in the digital filter (Y23, circuit diagram 291.5260 S) an electronic switch which is required for buffering the amplifier T11 to T16. Driving is made via T6 to T8.

T2 and T3 are through-connected for the voltage measuring ranges 0.3 mV to 1 mV; T1 and T4 remain inhibited. The signal is taken via the emitter follower T5 to the electronic switch T12 (Y23) and applied to the bandpass filter L1-C20 in the digital filter. The necessary isolation between the phase measuring branch and the amplitude measuring branch is provided by B4, which is used as impedance transformer and to whose output both measuring branches are connected. The amplifier B1, which is used as intermediate link and is switchable via B2, in the preamplifier B (Y24) provides for sufficient isolation of the amplitude measuring branch in the measuring ranges < 1 mV. R40 (Y24) is provided for compensating the tolerances between the two channels.

In the measurement ranges 100 µV and 30 µV the digital filter is cut in. The IF signal is now taken via the circuit C3-L1 and T1 and applied to the amplifier T11 to T16 (preamplifier Y24). At the same time T4 becomes conductive and T2 and T3 are inhibited in order to ensure sufficient isolation between the two branches. The output signal of the amplifier T11 to T16 is taken to the digital filter Y23. The operating principle of the digital filter is shown in Fig. 4-6. The input signal is applied via R and S to the storage capacitances C1 to C4. The switching frequency is identical with the frequency of the input signal. In this way the mean value of the applied voltage during a quarter period is formed at each capacitance. The fundamental wave is then derived again with the aid of the subsequent bandpass filter. The limit frequency f_T of the filter circuit and hence also the bandwidth of the digital filter with $B = 2 \times f_T$ are determined by the time constant R x C.

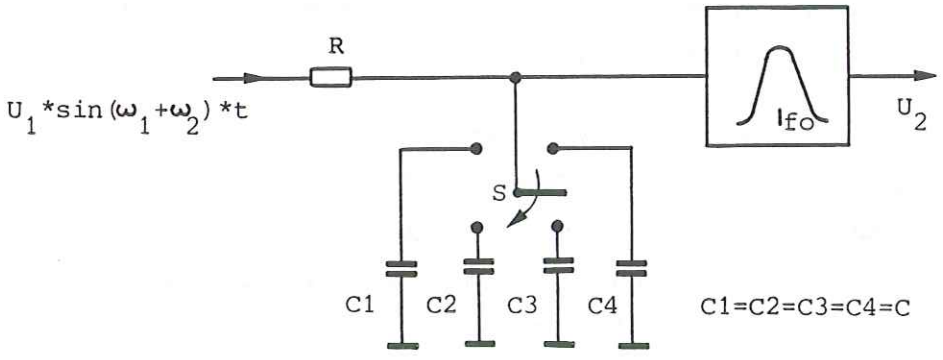


Fig. 4-6 Functional diagram of digital filter Y23

The switchover circuit is made up of T6 to T9 and a suitable drive (T1 to T5, B1, B2, B3). The transistors T3 and T4 form a multivibrator whose frequency is regulated by T2 to 160 kHz. This frequency is divided in B1 down to 20 kHz and the phase compared with the reference signal (T1). The voltage proportional to the phase deviation is filtered out at C1 and serves as control signal for the multivibrator T3, T4.

By logic operations, four successive pulses are generated which drive the switching transistors T6 to T9 (testpoints 9 to 12 and associated oscillograms in circuit diagram 291.5260 S).

A compensation network (R15, R16, C7, C12) is provided in order to suppress the crosstalk of the reference signal. The arrangement of the compensation network permits the generation of a voltage vector which has the same amplitude but opposite phase. The staircase signal from the digital filter is routed via the buffer stage T10 and T11 to the bandpass filter L1-C20, where the fundamental wave of the test signal is derived again. R24 permits exact calibration of the two measurement ranges 30 µV and 100 µV.

4.1.2 Phase Measurement

The phase meter consists of two identical channels, which convert the analog signal with variable amplitude and without phase distortion into a TTL signal. The phase information is then converted into an analog signal.
The amplitude of the test signal in each channel is kept constant by an AGC amplifier (Fig. 4-7).

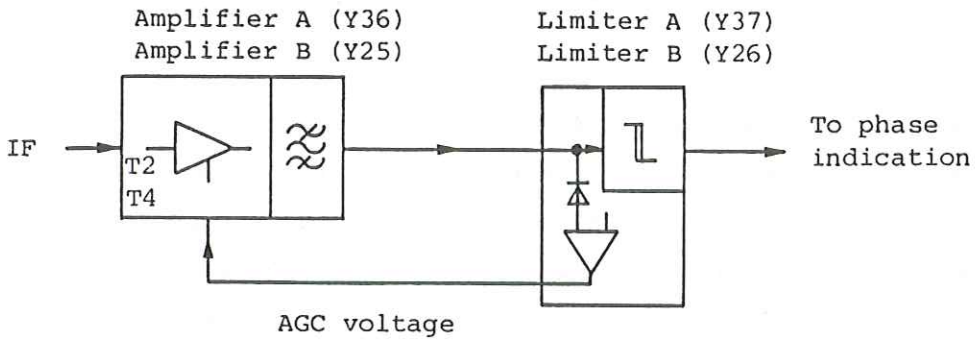


Fig. 4-7 Block diagram of phase meter

The test signal amplified by T2 and T4 and filtered out in the bandpass filter L1-C9 (see circuit diagram 291.5360 S and 291.5460 S) is further amplified in the limiter A (B) by T1 and T2 (see circuit diagram 291.5419 S and 291.5519 S). The symmetrical signal is then rectified (GL1 to GL4) and filtered. The actual voltage value is compared with the rated value at the non-inverting input of B2. The resulting deviation is linearized by T3, processed by B2 and taken back to the amplifier A (B). An attenuator pad (R3, T1) ensures a dynamic range of the amplifier of 100 dB. The amplitude of the IF signal of amplifier A (B) is thus constant and free from harmonics within the dynamic range. Phase distortions due to shifting of the zero-axis crossing are thus largely eliminated. The subsequent comparator B1 in the limiter A (B) converts the sinewave input signal into a TTL signal for the phase indicator Y27.

The phase indicator (see circuit diagram 291.5060 S) consists in principle of a phase meter with subsequent lowpass filter, a phase reset circuit and a calibration circuit, which permits calibration of the phase meter without an external standard.

The phase meter is equipped with the flipflop B5, which is set by the signal in channel A and reset by the signal in channel B. The mark-to-space ratio of the output pulses and hence also the mean value of the voltage with constant pulse amplitude is then proportional to the phase difference between the voltages in the reference and test channels. The constant amplitude of 6 V of the pulses is ensured by the switching transistors T1 and T2 and the use of the constant reference voltage of the D/A converter. The active low-pass filter B7, B8 derives then the mean value of the output voltage from the phase meter.

The phase of the two voltages in the channels A and B is additionally evaluated with the gate B4. For the automatic phase resetting the symmetrical characteristic of the phase meter is used by an exclusive OR gate (Fig. 4-8). With a phase difference of more than $\pm 100^{\circ}$ the switching threshold of the Schmitt trigger B6 is reached and the logic state of the storage flipflop B5 is changed. B4 inverts the reference signal, this corresponding to a phase offset of $\pm 180^{\circ}$.

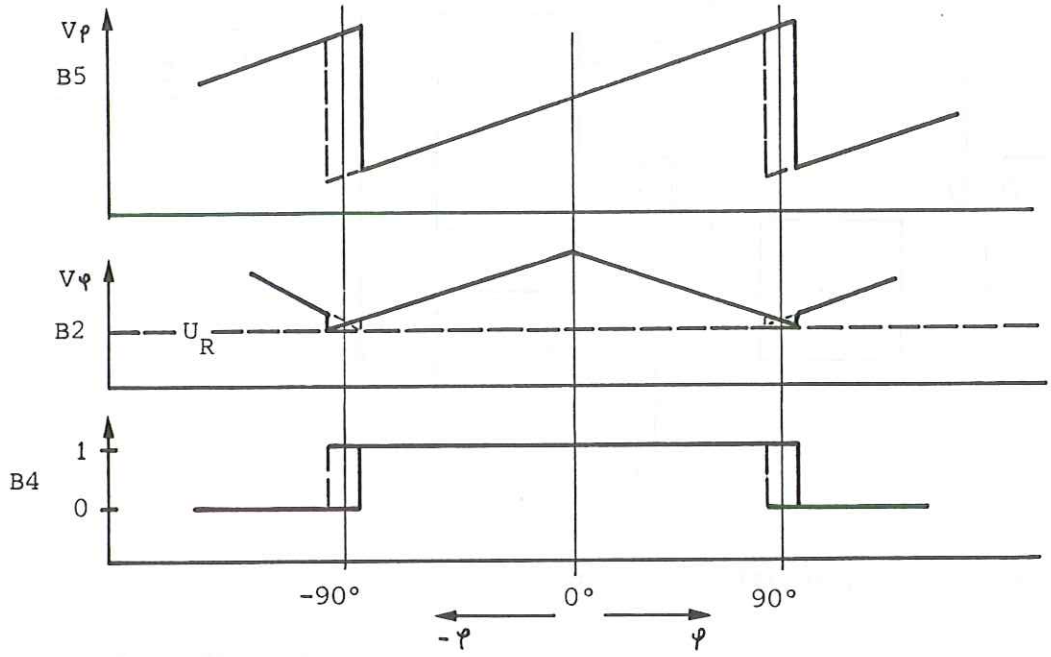


Fig. 4-8 Switching conditions of automatic phase resetting

The phase offset is then taken into in account in the built-in calculator when the phase value is output. In this way the otherwise negatively-sloped characteristic of the phase meter at a phase difference of $\pm 180^{\circ}$ and hence also the measuring inaccuracy is eliminated. In order to ensure proper functioning of the phase resetting and also for switchover from narrowband sweeping, the multivibrator T5, T6 delivers, if required, the missing reset pulses until the phase-proportional voltage at the input of the Schmitt trigger B6 reaches again the proper values.

The phase indicator Y27 permits in addition self-calibration of the phase meter, taking into account the error of the 180° phase offset. For this purpose the input B of the phase meter is supplied with the signal of channel A delayed by = 12.5 µs (Fig. 4-9). This delay corresponds to a phase shift of $\pm 90^{\circ}$, the polarity being dependent on the logic level at ST1.31b. As can be seen from Fig. 4-8, this phase shift is within the hysteresis of the phase resetting. Due to the forced switchover at ST1.17a it is then possible to cut in or out the 180° phase offset.

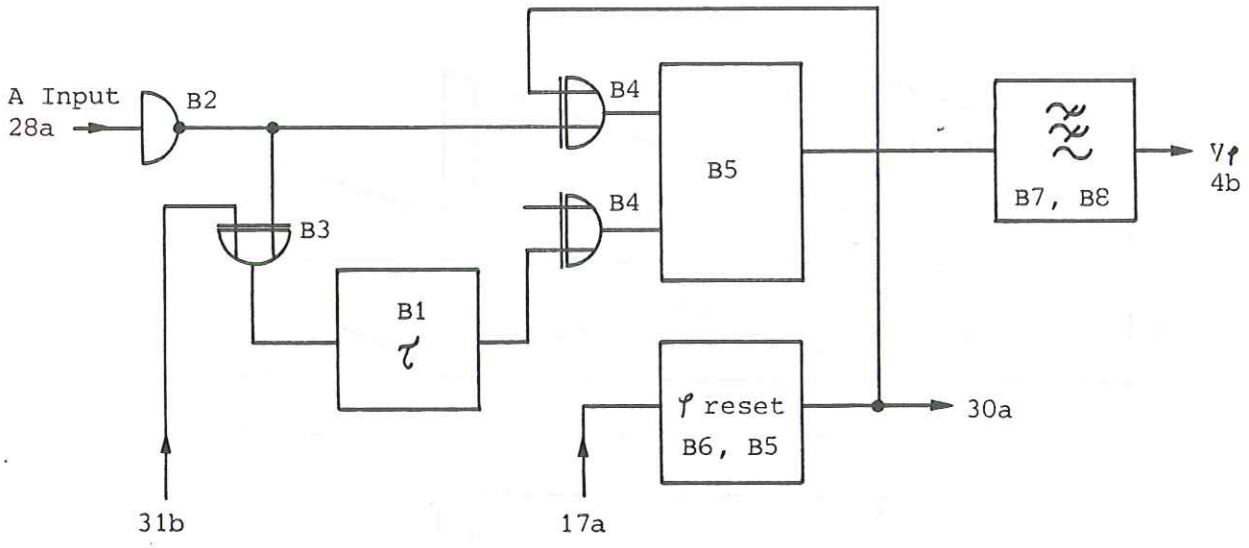


Fig. 4-9 Block diagram of self-calibration

The exact phase measure M and the phase offset O are determined from the four phase values and the corresponding analog voltages as follows:

$$M = \frac{|V_1 - V_2| + |V_3 - V_4|}{360} \frac{V}{\text{degree}}$$

$$O = \frac{|V_1 - V_2|}{M} \text{degree}$$

where

$V_1 = \varphi_1$

$V_2 = \varphi_2 = \varphi_1 - O$

$V_3 = \varphi_3 = -\varphi_1 - O$

$V_4 = -\varphi_1$

4.1.3 Narrowband Sweeping

In some cases a continuous display of the measured values, at least in a small frequency range, would be desirable, as is for instance required by crystal manufacturers or for measurement of narrowband filters. Such displays on the screen of an oscilloscope or in conjunction with an XY recorder are permitted by the operating mode SWEEP of the ZPV. A sweep rate of up to 300 MHz/s is possible with a sweep width corresponding to the holding range of the frequency synchronization.

Contrary to the other operating modes of the ZPV, in which the analog test values are digitized by the computer and output, the built-in computer monitors in the narrowband sweep mode the level in reference channel A. In this way accurate measurement without any additional adjustments is also possible in the SWEEP mode.

First condition for an accurate measurement is a constant signal at the input of the test item. In order to avoid exacting requirements on the signal generator used, the level at the input of the test item is measured in reference channel A and the value measured in channel B is corrected accordingly; the ratio of the two voltages is then formed.

The signal in reference channel A is further amplified in B1 on the PC board selectivity filter A (see circuit diagram 291.5319 S) and subsequently rectified by the operational rectifier B3. After filtering in the active lowpass filter B6 the measured DC voltage of the reference channel is applied to the multiplier B5. The measurement range of reference channel A is thus fixed to 0.05 to 0.5 V. At the same time, the voltage is taken via T2 to the computer. If the reference level leaves the particular range, a corresponding signal is delivered via the computer. The Zener diode GL3 ensures proper functioning of the instrument in the other operating modes.

The test signal of channel B is processed and measured like in the other operating modes of the ZPV (see section 4.1.1). With narrowband swept-frequency operation, the analog signal is applied via ST1.11a to the multiplier B5. The voltage ratio between channels A and B is formed and as analog voltage brought out via the switching transistor T4 at the socket r SWEEP on the rear panel of the set. Since the measurement range B can be switch-selected in 10-dB steps, swept-frequency measurements are possible in the entire dynamic range with a reference level of 0.03 to 0.3 V. The reference value 1 lies within the measurement range B = 0.1 to 0.3.

In addition to the possibility of forming the ratio B/A, a swept display of the values measured in channel B or A is also possible by switching off the voltage measurement in channel A by T3. The reference voltage REF. 1 routed via ST1.7a is used as reference potential. Switchover of the function is effected via the level converter B4 by applying a logic 1 to ST1.1b.

B4 also processes the signal required for switching the phase indicator Y27 (see circuit diagram 291.5060 S). When selecting the SWEEP mode, the phase is automatically output in analog form at the socket φ SWEEP on the rear

panel. The phase-proportional voltage is processed without phase resetting as used in point-for-point measurements. The phase resetting is disabled by applying the logic level 0 to B5.1 via R11. The amplitude of the phase-proportional voltage is reduced in B6 to ±0.5 V for full-scale deflection (±180°) and taken via the switching transistor T3 and R41 to the socket ℘ SWEEP. The output impedance is fixed at 100 Ω by R41.

4.1.4 Power Supply

The power supply Y2 (see circuit diagram 291.6015 S) is a self-contained module which is accommodated on the rear panel of the basic unit ZPV. Since the rear panel can be removed, measuring and checking the power supply is easy. The power supply is connected with the basic unit by means of two flat cables which are plugged into the motherboard and are part of the power supply. The power supply contains six supply units, which supply the ZPV basic unit and the plug-in with ±5 V, +12 V, ±15 V, ±20 V and +120 V.

The supply units for ±20 V and +12 V are of conventional design with fixed voltage regulators B1, B2, B3. R14 and R17 provide for exact setting of +20 V and -20 V. All three units have an internal current limiting and thermal overload protection and are therefore short-circuit-proof. Due to their low current load, the supply voltages of ±15 V are derived from ±20 V via the Zener diodes GL6 and GL9.

The +120-V unit is intended for the supply of the pulse generator in the tuner plug-in. The +20-V supply is used as reference voltage source. The amplifier T2, T3 is supplied from the -20-V unit. The overload protection of the series regulator T1 is ensured by the current limiting R2, GL2, GL3 and an additional fuse SI2.

The +5-V supply is a separate subassembly. The arrangement of the series regulator T4 permits driving into the saturation region of the collector-emitter voltage, thus ensuring less leakage power in the regulator. The -5-V supply with the fixed voltage regulator is used as reference voltage source. The deviation of the actual value from the rated value is amplified in B4 and via T5 applied to T4.

The voltage at R29, which is proportional to the current load, is compensated by the bias voltage at R27. In case of overload the sum of the voltages at R29 and at R27 becomes < 0. As a result the amplifier B4 takes over the driving via GL18 and adjusts for a smaller value of the output voltage. Thus

the bias voltage at R27 becomes smaller and also the maximum short-circuit current, which means a foldback current characteristics (Fig. 4-10).

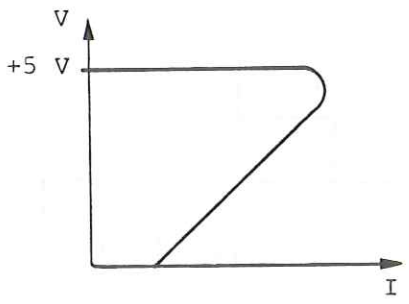


Fig. 4-10 Current characteristic of the +5-V supply

In order to keep the source impedance of the power supply small, separate sensor lines for measuring the +5-V voltage and the ground potential are brought out at BU15.11 and .1. The resistors R30 and R11 provide for a defined potential on the sensor lines for the case that the power supply should not be properly connected. The diodes GL17, GL21, GL7 and GL8 provide for a protection against overvoltage at the outputs of the power supply.

In addition to the analog and digital subassemblies of the ZPV the power supply also supplies the three-phase generator M01 of the blower. The power supply is designed for all usual AC supply voltages, which can be selected by means of the voltage selector on the rear panel of the ZPV. AC supply frequencies between 47 Hz and 420 Hz are permissible. A filter incorporated in the power cable provides for suppression of mains noise.

4.2 Digital Section

As can be seen from Fig. 4-1 in the appendix, the analog section of the ZPV is controlled by the digital section. The block diagram shows the internal structure of the digital section. The individual blocks represent the PC boards or subassemblies. The connecting lines within the digital section represent address bus, data bus and control lines.

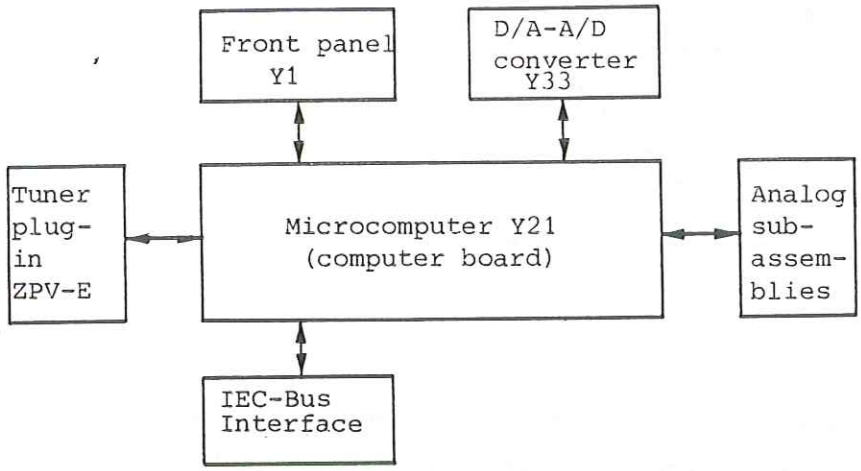


Fig. 4-11 Block diagram of digital section

The main part of the digital section is the PC board carrying the microcomputer. The front panel with pushbuttons and readouts serves for operation of the set and indication of the test results. The IEC-bus interface board enables remote control according to IEC standards. On the D/A converter board both digital values are converted into analog values (analog voltage outputs, tendency indication control) and analog values into digital values (test voltages). The connection between computer board and plug-in provides for the information about the synchronizing state and the possibility of automatic frequency range selection. The connection to the analog section of the basic unit is required for channel selection, automatic amplitude range selection, phase calibration, etc.

4.2.1 Computer Board Y21

See circuit diagram 291.4812 S

The microcomputer proper of the ZPV is accommodated on this PC board. The block diagram below shows the simplified design.

The heart of the microcomputer is the microprocessor, which mainly consists of the two-phase clock pulse generator B1, the central processing unit B3, the bus control module B6 and the address buffers B4 and B5. The program

commands and fixed information required for the microprocessor are available in ROMs B11 to B14. The decoder B10 in conjunction with the gates B7 and B2 serves for selecting the individual ROMs. The ROM capacity is 4 kbytes.

Variable data and return addresses are stored by the microcomputer in the RAMs B16 and B17. The inverter B2 and gate B15 provide for the selection of these RAMs. The available RAM capacity is 1 kbyte.

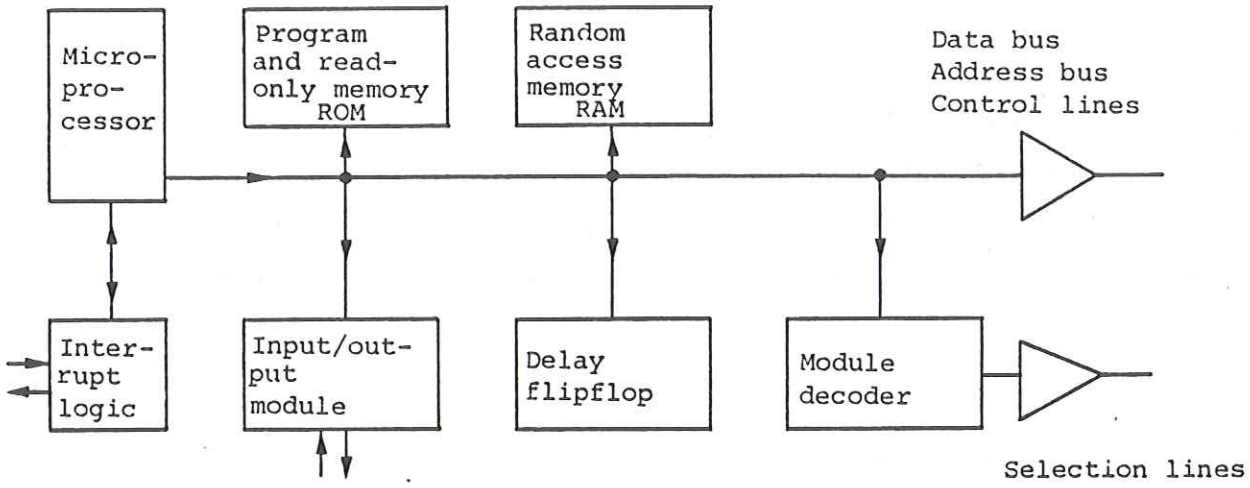


Fig. 4-12 Block diagram of computer board

An interrupt logic combines the three interrupt requests: keyboard interrupt, LACS and TACS (B7, B8, B9). Only one interrupt level is used (interrupt 7). The keyboard interrupt signal is emitted by the keyboard as soon as one button is pressed and sets the flipflop B9, whose output addresses the central processing unit and interrupts via B7 and B8 the keyboard clock signal, thus stabilizing the status. After processing of the interrupt the flipflop is reset and hence free for new interrupts.

The signals LACS and TACS come from the IEC interface board and mean a listener or a talker interrupt. The flipflop B9 is set and the central processing unit is addressed by the timing of signal SP15 and B7. A listener interrupt is stabilized by DAC via B8. After recognition of the cause of interrupt the flipflop is reset again and is free for a new interrupt.

The input/output module B23 is mainly used for controlling the analog section. In addition, it also controls the two monoflops B24, which are used for generating delays. The input/output module is selected by the input/output

decoder B20, B21, B22 like the other input/output modules on other sub-assemblies.
Parts of the address bus, the data bus and certain control lines are connected with the basic unit via the connector strips.

4.2.2 Front Panel Y1

See circuit diagram 291.4112 S

The front panel consists of the readout panel and the keyboard.
The following block diagram shows the individual functional groups.

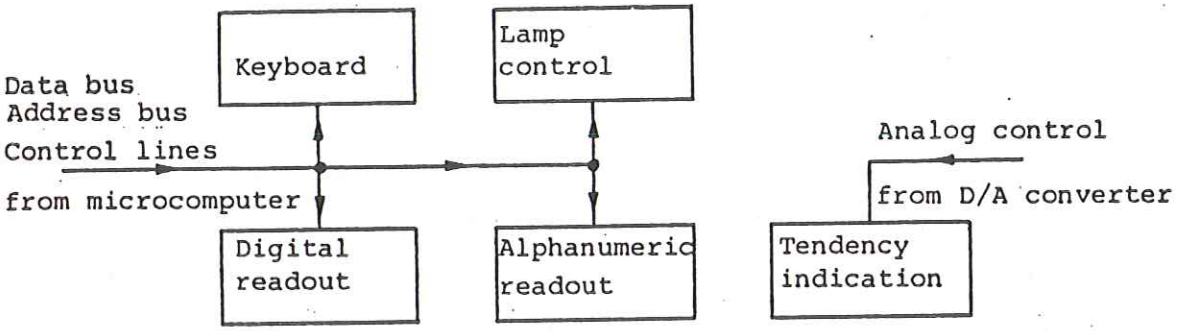


Fig. 4-13 Block diagram of front panel

All functional units, with the exception of the tendency indication, are connected to the address bus, the data bus and the input/output selection lines of the microcomputer. The keyboard operates with independent interrogation of the pushbuttons. The counter B43 is continuously switched by the keyboard clock signal. A level of 0 V is present only at one output line of the decoder B42 which is connected to B43. If a button is depressed, the 0 V-level is switched to one of the inputs of the B44. Consequently the counter disable line goes to +5 V and inhibits via the computer board the keyboard clock signal. After a certain delay, the keyboard interrupt signal

appears also and causes an interruption of the current computer program. The microcomputer reads in the gates B33, B34 and determines the depressed button. After releasing the button, the interrogation of the buttons is continued. The counter combination 15, which is not used for the pushbuttons, enables on the computer board an interruption by the IEC bus interface.

The flipflops B31, B41, B45 with the subsequent decoders B40, B50, B51, B52, B53 and the transistor array B46 drive the lamps in the luminous buttons as well as the LEDs GL4 to GL7. The selection for the data transfer to the individual flipflops is made via the decoder B32.

The hexadecimal components B2, B3, B4, B5 provide for the digital readout of the lefthand indication panel and B12, B13, B14, B15 for that of the righthand indication panel. The polarity signs of these digital readouts are produced by the overflow indicators B1 and B11. The sign and the decimal point of the lefthand digital readout are controlled via the flipflop B19, that of the righthand digital readout via the flipflop B21. The flipflop B211 provides for blanking of both digital readouts. The selection for the data transfer to the digital readouts and of the associated flipflops is made by the decoder B9.

The alphanumeric 5-by-7 dot matrices B6, B7, B8 are used for dimension indication of the lefthand readout and B16, B17, B18 for that of the right-hand readout. One column of the left and one of the right dimension indication is unblanked simultaneously with the contents of the RAMs B37, B47, B38 and B48. The column counter B54 in conjunction with its clock pulse generator B36 switches the RAM addresses synchronous with the column decoders B39 and B49. This is an automatic process. If the dimension changes, the microcomputer switches via the alpha write enable signal its address bus via the program switch to the address bus of these RAMs and resets at the same time the column counter. The new dimension pattern can be loaded in conjunction with the selection lines alpha output right and alpha output left.

The LED rows B26, B27 and B28, B29 enable quasi-analog display of the left-hand and the righthand readouts. Driving via B20 and B22 is purely analog by the reference voltage and the control voltages tendency left and tendency right from the D/A converter board.

4.2.3 D/A Converter Y32

See circuit diagram 291.5119 S

The D/A converter board serves both for converting digital into analog values and analog into digital values.

The core of this converter is the 12-bit D/A converter B2. It is driven by the microcomputer via the input/output module B1. Via its output amplifier T9, T10 it can quickly charge the capacitors C7 to C12, which are connected via one of the FET switches T3 to T8, to a certain voltage.

These voltages are then available via high-impedance emitter followers for digital output on the rear panel (X, r; Y, φ), for controlling the tendency indication (tendency left, tendency right) and for the deviation control output CONTR. ΔF on the rear panel (deviation control, γ).

The quad comparator B16 affords the comparison of analog voltages. Thus the voltage of the D/A converter can be compared with that of the A/D converter (from the socket ADC on the rear panel), with the voltage A, B (from the amplitude indication), with the voltage φ (from the phase meter) and with the output voltage of B15. By systematic comparison the microprocessor can thus approximate in 12 steps the voltage under observation and determine its digital value.

For increasing the resolution in the phase and group delay measurement the phase voltage at B8 can be compensated by a voltage at B9 and the difference amplified by B15 can be measured.

B17 buffers the two reference voltage outputs REF. 1 for the phase meter and REF. 2 for the tendency indication.

4.2.4 IEC Interface (Option ZPV-B1)

See circuit diagram 292.3632 S

The IEC interface board provides the ZPV with the interface functions SH1, AH1, T6, TE6, L4, SR1, DC1, DT1, RLØ, PPØ, CØ which comply with DIN-IEC 66.22 (IEEE 488). This PC board acts as data coupler between the external data bus DI/01 to DI/08 and the ZPV data bus DB0 to DB7. The IEC interface board performs pure interface functions such as handshake, addressing, unaddressing and last character coding completely independent, i.e. without any involvement of the microcomputer of the ZPV. This is shown in the following block diagram.