PUBLICATION NO. 980647

1991 AND 1992

UNIVERSAL TIMER/COUNTER

RACAL-DANA

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RACAL

PUBLICATION DATE: AUGUST 1987

AMENDMENT TO

THE FOLLOWING RACAL-DANA INSTRUCTION MANUALS

1991/2 Publication No. 980647
1991/2 Publication No. 980651
1992-02M Publication No. 980636
1994 Publication No. 980601

June 27, 1989

Page 6-15

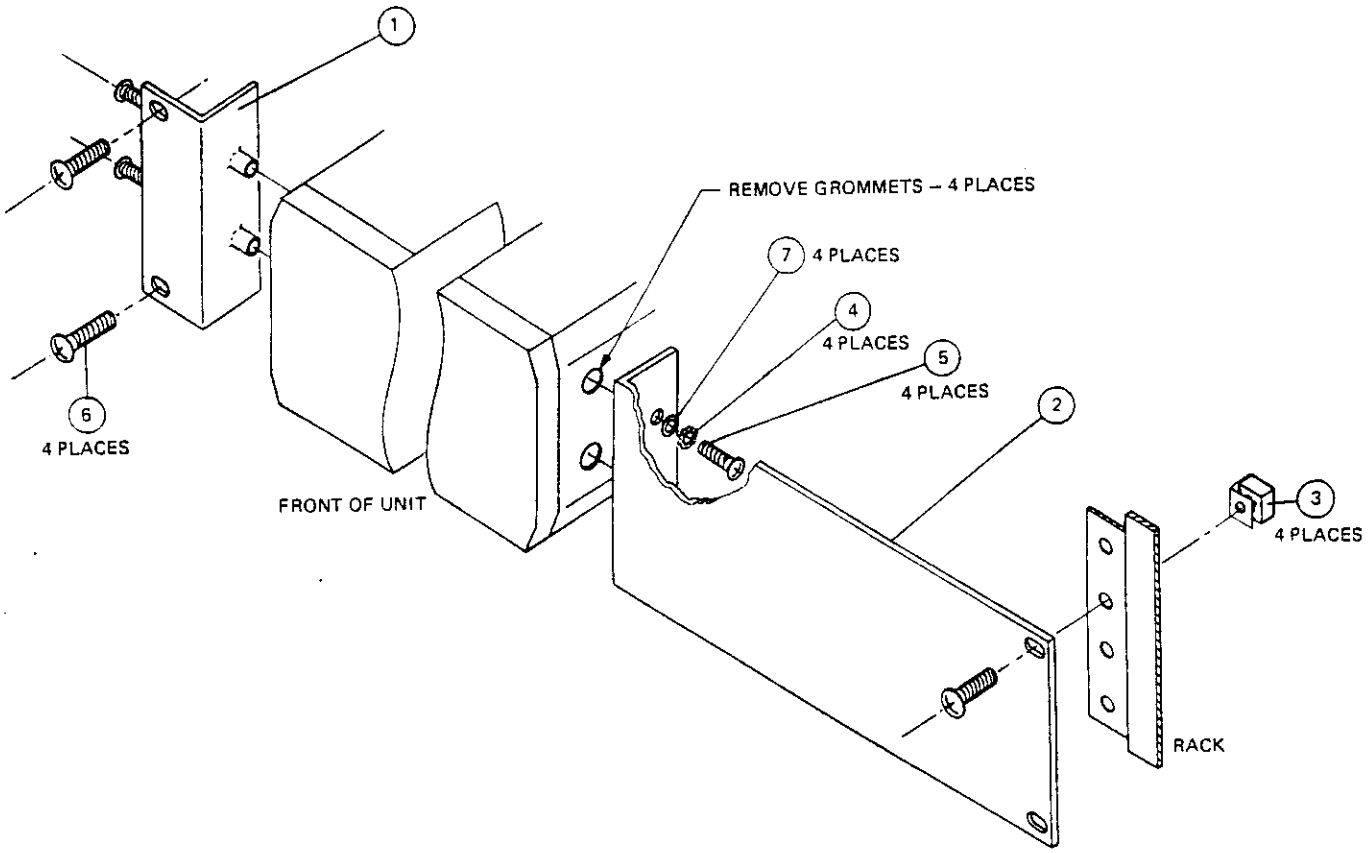
Special Function (SF) 76 should be: 74

1. Remove grommets - 4 places.

2. Attach rack mounting ear (1) and extension (2) to side of unit with screw (5) and crinkle washer (4) and flat washer (7) in 4 places.

3. Clip Tinnerman nuts (3) to rack in 4 places.

4. Attach unit to rack/nuts with screws (6) in 4 places.



CONTENTS OF KIT 404673)

ITEM NUMBER	RACAL-DANA P/N	DESCRIPTION (QTY.)		FSC	MANU P/N
1	455433	Rack Mounting Ear	(1)	21793	455433
2	455439	Mounting Ear Extension	(1)	21793	455439
3	610920	Nut, Retainer	(4)	21793	610920
4	R-24-2802	Washer, Crinkle, M4	(4)	21793	R-24-2802
5	616346	Screw, PPH, M4 x 16	(4)	---	----
6	615091	Screw, PPH, 10-32 x .500	(4)	---	----
7	617104	Washer, Flat #8 Light Series	(4)	---	----

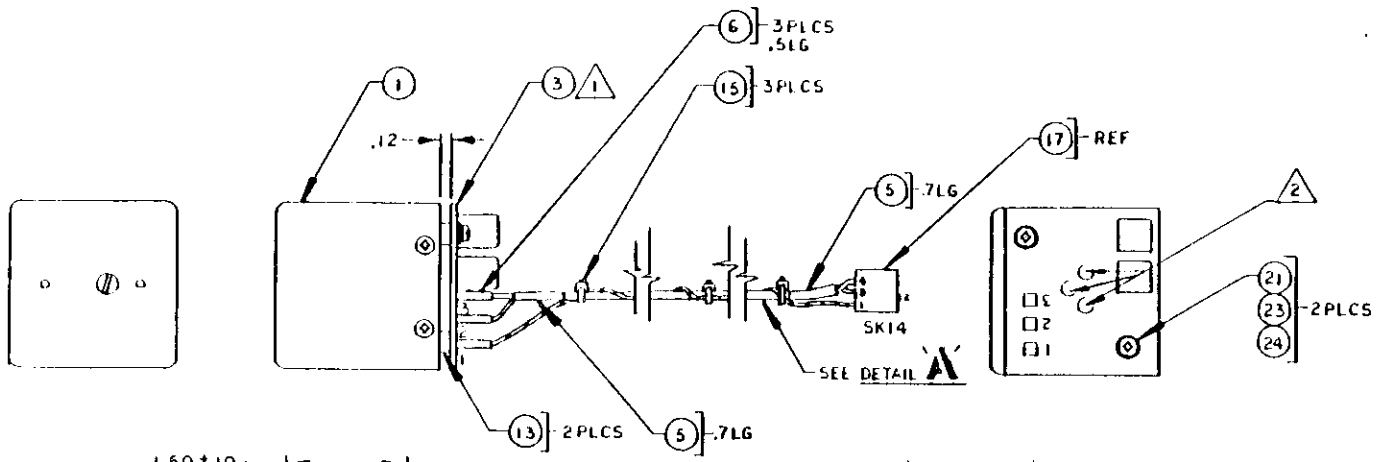
AMENDMENT TO

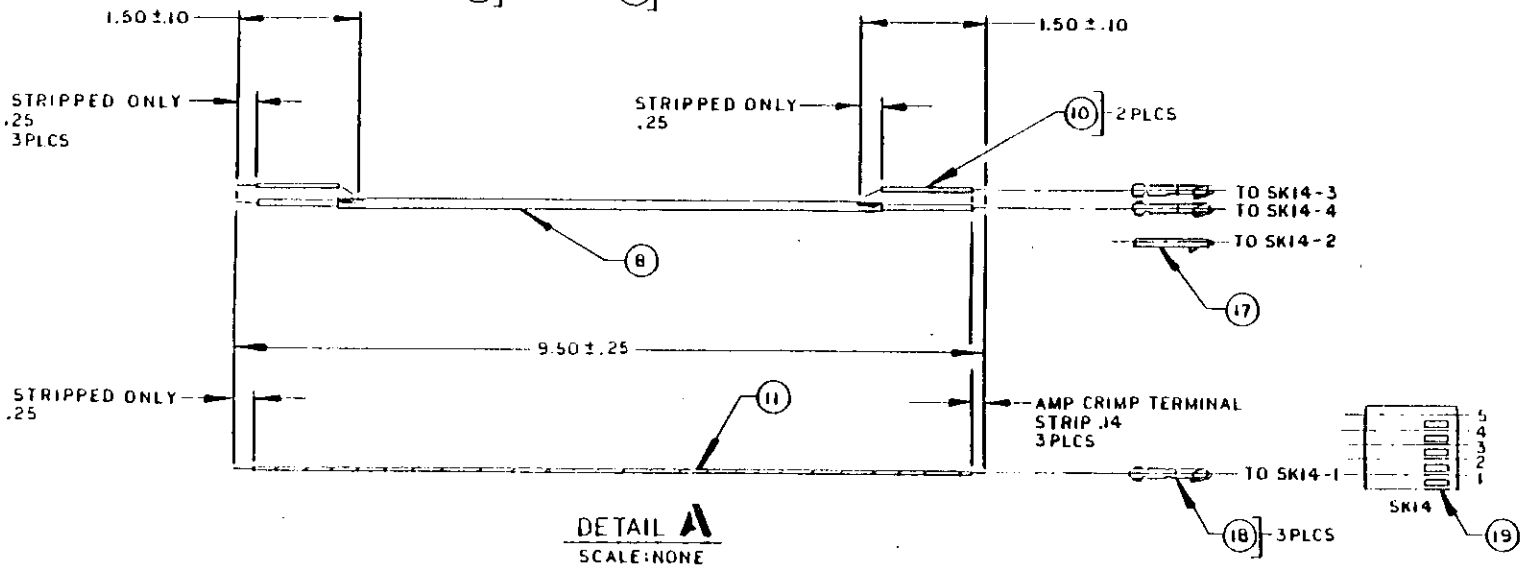
MODEL 1991/2 INSTRUCTION MANUAL
PUBLICATION NO.
980647 and 980651

April 28, 1989

1. Pages 1-11 and 1-20, Change the part number for Option 60A Rack Mounting Kit from 11-1648 to 404673.

2. Page 2-5 Replace Section 2.8.1 Option 60A Rack Mounting Instructions with the information provided in this amendment.





DETAIL A
SCALE: NONE

2 SOLDER AT ASSY.

1 REMOVE & DISCARD CABLE SUPPLIED WITH ITEM 3 & REPLACE WITH ITEMS 5,6,8,10,11,15, & 17-19.

NOTES: UNLESS OTHERWISE SPECIFIED

RACAL-DANA Instruments Inc.
4 GOODYEAR IRVINE CALIFORNIA 92714

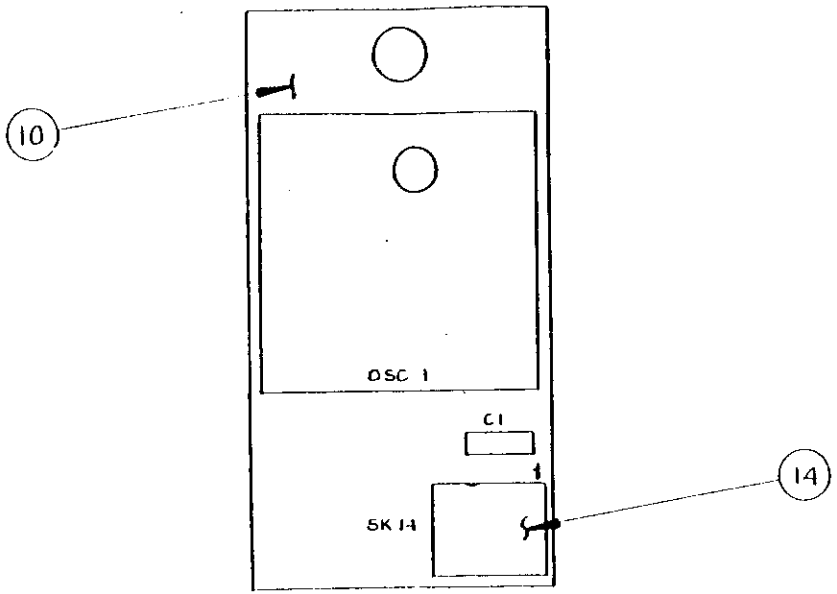
DOCUMENT TITLE
OVEN OSCILLATOR, 9444

SIZE	CODE IDENT NO	DWG NO	REV
C	21793	404397	A

SCALE — SHEET 1 OF 3

DWG 40404397

ECO No	USED ON 1991 , 1992 (11-1713)



RACAL-DANA INSTRUMENTS LTD	RACAL DRG No R-19-1208	REV A
TITLE PCB ASSY, 10 MHZ TCXO	DRAWING No SHEET 1 OF 2	

AMENDMENT

Racal-Dana Model 1991/2

Instruction Manual, Part Number 980651/980647

April 10, 1988

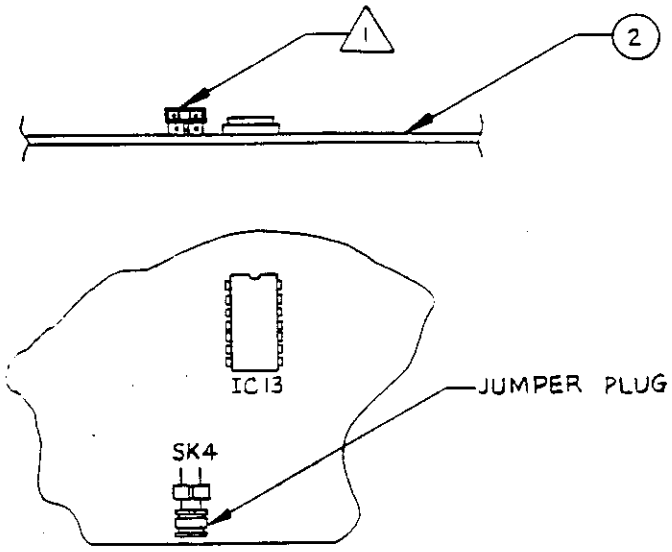
1. **Addition of GPIB Assembly**

   a. On page 7-1, add the following to the list of drawings:

      Figure 7.10A GPIB Assembly (404574)....7-22.

   b. On page 7-1, change the designation of Figure 7.10 to 7.10B. (Figure 7.10B is a subassembly of Figure 7.10A).

   c. On page 7-22, add Figure 7.10A, GPIB Assembly (404574) as shown below:



1 MAKE CERTAIN JUMPER PLUG IS INSTALLED IN UPPER TWO PINS OF SK4 AS SHOWN.

NOTES: UNLESS OTHERWISE SPECIFIED

   d. On page 7-22, change the designation of Figure 7.10 to 7.10B.

   e. On page 8-1, add the following to the listing of parts lists:
      GPIB Assembly (404574)....8-17

   f. On page 8-17, add the parts list for 404574-GPIB Assembly:

      Ref. Desig: {2} 1, Racal-Dana P/N: 401820, Description: PCB Assy, GPIB, FSC: 21793, Manu P/N: 401820

2. **Update of PCB Assembly, GPIB (401820) from Revision A to Revision B.**

   a. On page 7-22, delete item 50 from the drawing and add the following note:

      Trim lead length of SK4 connector so that lead protrusion on PCB circuit side does not exceed 0.072 inch.

   b. On page 8-17, delete item 50 (11-1603) from GPIB PCB Assy. parts list.

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LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont'd)

LIST OF TABLES

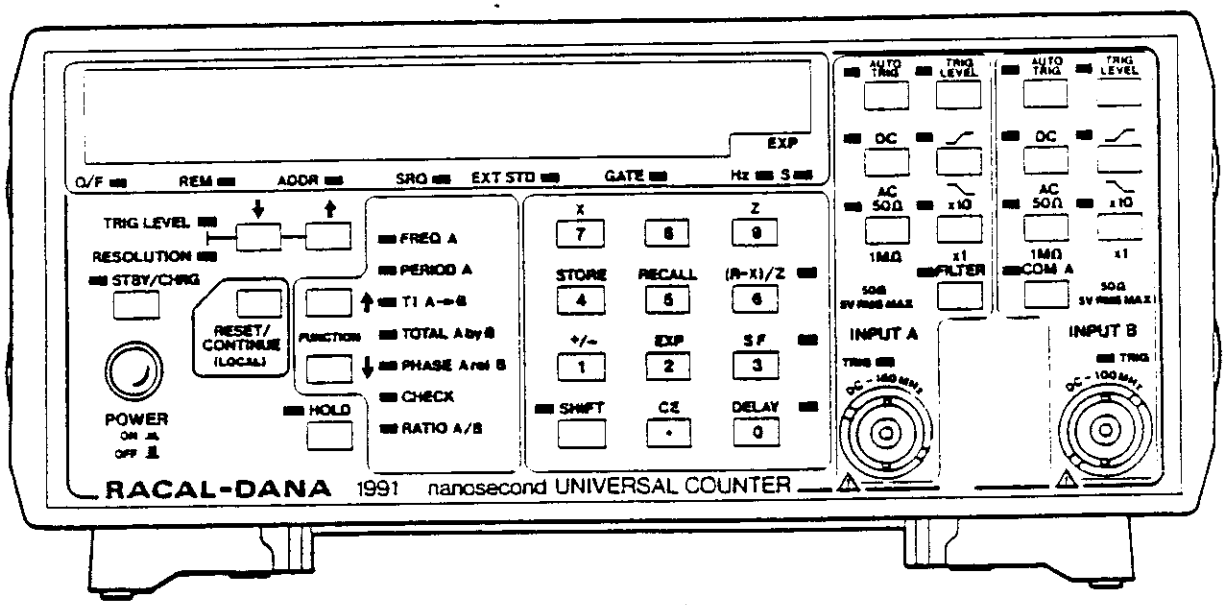


Figure 1.1 - Model 1991 Universal Timer/Counter

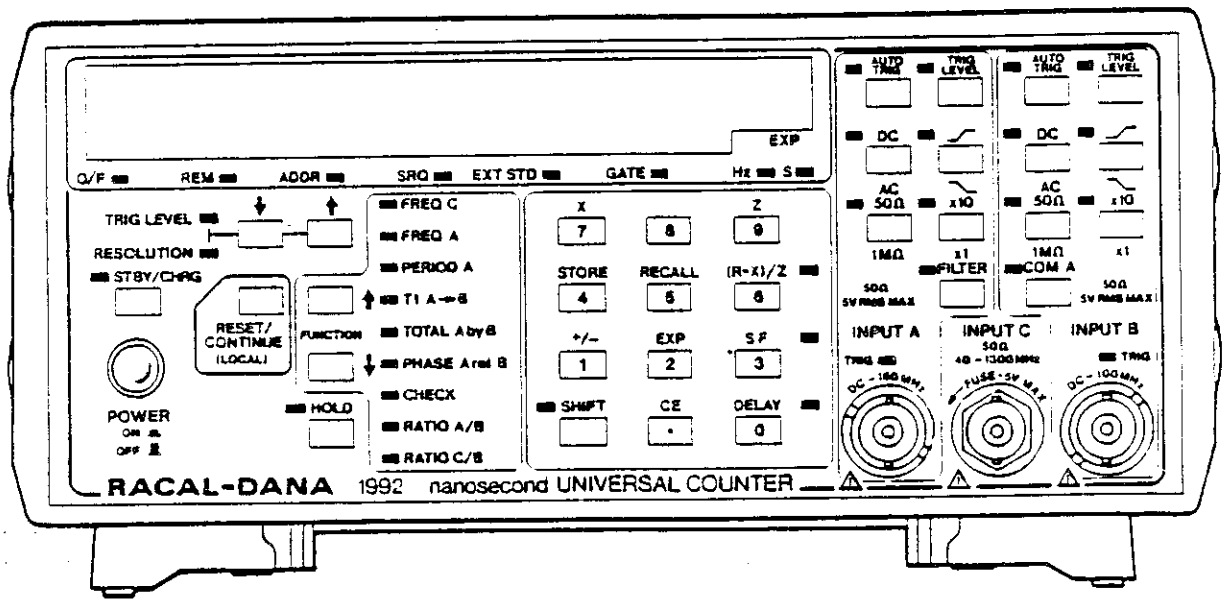


Figure 1.2 - Model 1992 Universal Timer/Counter

SECTION 1 GENERAL INFORMATION

1.1 INTRODUCTION

1.1.1 This Instruction Manual provides information for installing, operating, and servicing of Racal-Dana's 1991 and 1992 Universal Timer Counters. Figures 1.1 and 1.2 are front views of the 1991 and 1992. The 1991 offers universal counter functions using Inputs A and B. The 1992 also provides frequency measurements to 1.3 GHz using Input C.

1.2 SUMMARY

1.2.1 This manual is organized into the following eight sections:

SECTION 1. General Information:

a. Published Specifications

b. Safety

c. Product Support

d. General Description

SECTION 2. Installation and Preparation for Use:

a. Unpacking and Initial Inspection

b. Reshipment

c. Power Connections

d. Storage and Temperature

e. Functional Check

f. Miscellaneous Setup Procedures

g. Option Installation Instructions

SECTION 3. Local Operation:

a. Panel Descriptions

b. Operating Procedures

c. Trigger Level

d. Display Resolution

e. Gate Time

f. Stop Circuit Delay (Hold Off)

g. Special Functions

h. Error Codes

i. Math Function

j. External Arming

SECTION 4. GPIB Operation:

a. GPIB Description

b. GPIB Address Assignment

c. GPIB Functional Check

d. Interface Message Repertoire and Response

e. GPIB Operating Modes

f. Output Message Format

g. Service Request

h. Status Byte

i. Input Commands

SECTION 5. General Theory of Operation:

a. Functional Blocks

b. Theory of Operation by Block

SECTION 6. Maintenance:

a. PVP/Calibration Inspection Intervals

b. Required Test Equipment

c. Dismantling and Reassembly

d. Special Functions for Diagnostic Purposes

e. Troubleshooting

f. Post-Repair Setup

g. Internal Frequency Standard - Routine Calibration

h. Overall Performance Verification Procedure

SECTION 7. Drawings:

a. Assembly Drawings

b. Schematic Drawings

SECTION 8. Parts List:

a. Replaceable Parts and Assemblies

1.3 SPECIFICATIONS

1.3.1 Table 1.1 lists the 1991/1992 specifications. The specifications indicate the performance standards to which the instrument conforms at the time of shipment.

Table 1.1 - 1991/1992 Specifications

INPUT CHARACTERISTICS (MODEL 1991)	
Inputs A and B	
Frequency Range:	
Input A:	DC to 160 MHz DC-coupled 10 Hz to 160 MHz AC-coupled
Input B:	DC to 100 MHz DC-coupled 10 Hz to 100 MHz AC-coupled
Sensitivity:	
Sine Wave:	25 mV rms DC to 100 MHz 50 mV rms to 160 MHz
Pulse:	75 mV p-p, 5 ns min. width
Dynamic Range: **(x1 attenuation)**	75 mV to 5V p-p to 50 MHz 75 mV to 2.5V p-p to 100 MHz 150 mV to 2.5V p-p to 160 MHz
Signal Operating Range:	
x1 attenuation:	± 5.1V
x10 attenuation:	± 51V
Input Impedance (nominal):	
(x1 and x10 attenuation)	
Separate Mode:	50 ohms or 1 Megohm //≤45 pF
Common Mode:	50 ohms or 1 Megohm //≤55 pF
Maximum Input (without damage):	
50 ohms:	5V (DC + AC rms)
1 Megohm: **(x1 attenuation)**	260V (DC + AC rms), DC to 2 kHz Decreasing to 5V rms, at 100 kHz and above
1 Megohm: **(x10 attenuation)**	260V (DC + AC rms), DC to 20 kHz Decreasing to 50V rms at 100 kHz and above
Coupling:	AC or DC
Low Pass Filter:	50 kHz nominal (Input A selectable)
Trigger Slope:	+ve or -ve
Attenuator:	x1 or x10. In Auto Trigger mode, attenuator selected automatically if necessary

Table 1.1 - 1991/1992 Specifications (Cont'd)

Trigger Level Range:	
Manual:	± 5.1V in 20 mV steps
x1 attenuation:	± 51V in 200 mV steps
x10 attenuation:	± 51V
Automatic:	
Trigger Level Accuracy:	
Manual and Automatic:	± 30 mV ±1% of trigger level reading
x1 attenuation:	± 300 mV ±1% of trigger level reading
x10 attenuation:	
Auto Trigger:	
Frequency Range:	DC and 50 Hz to 100 MHz (Typically 160 MHz)
Min. Amplitude (AC):	Typically 150 mV p-p*
x10 attenuator	Automatically selected if input signal exceeds ± 5.1V or 5.1V p-p*
Trigger Level Outputs:	
(Rear Panel)	
Range:	± 5.1V
Accuracy (Relative to true trigger level)	
x1 attenuation:	± 1% V output ±10 mV
x10 attenuation:	± 1% V output ± 100 mV
Impedance:	10 kohm nominal

MODEL 1992: Specification for input characteristics is identical to that for the 1991 except for the following addition:

Input C	
Frequency Range:	40 MHz to 1.3 GHz
Sensitivity:	
Sine Wave:	<15 mV rms, 40 MHz to 1 GHz <75 mV rms to 1.3 GHz
Dynamic Range:	15 mV rms to 5V rms to 1 GHz 75 mV rms to 5V rms to 1.3 GHz
Input Impedance:	50 ohms nominal AC-coupled
VSWR:	≤2:1 at 1 GHz
Maximum Input:	7V rms (fuse-protected) Fuse located in BNC connector
Damage Level:	2.5W

*See Definitions

Table 1.1 - 1991/1992 Specifications (Cont'd)

MEASUREMENT MODES	
Frequency A	
Range:	DC to 160 MHz
Digits Displayed:	3 to 9 digits plus overflow
LSD Displayed (Hz):	$F \times 10^{-D}$ (D = No. of digits, F = Frequency rounded up to next decade)*
Resolution* (Hz):	± LSD† ± (Trig. Error* x Frequency) /Gate Time
Accuracy* (Hz):	± Resolution ± (Timebase Error x Frequency)
Frequency C (Model 1992 only)	
Range:	40 MHz to 1.3 GHz
LSD*:	As for Frequency A
Resolution* and Accuracy*:	As for Frequency A
Time Interval	
Range:	
Separate Mode:	0 to 8×10^5s Typically -2 ns to $+8 \times 10^5$s
Common Mode:	5 ns to 8×10^5s
Input:	
Common:	Input A START and STOP
Separate:	Input A START Input B STOP
Trigger Slopes:	+ve or -ve Selectable START and STOP
LSD Displayed:	1 ns min
Resolution* (sec):	± LSD ± 1 ns ± Trig Error*
Accuracy* (sec):	± Resolution ± (Timebase Error x T1) ± Trigger Level Timing Error* ± 2 ns**

*See Definitions
† 2 LSD for 6-9 digits displayed
**A differential delay which may be reduced by numerical offset or external compensation.

Table 1.1 - 1991/1992 Specifications (Cont'd)

Time Delay	
Available on Time Interval and Totalize	
Range:	200 µs to 800 ms nominal
Step Size:	25 µs nominal
Accuracy:	± 0.1% Rdg. ± 50 µs
Period A	
Range:	6.25 ns to 1.7×10^3s
Digits Displayed:	3 to 9 digits plus overflow
LSD Displayed (sec):	$P \times 10^{-D}$ (D = No. of digits, P = Period rounded up to next decade)*
Resolution* (sec):	± LSD† ± (Trig. Error* x Period) /Gate Time
Accuracy* (sec):	± Resolution ± (Timebase Error x Period)
Ratio A/B	
Specified for higher frequency applied to Input A	
Range:	DC to 100 MHz on both inputs
LSD Displayed: (for 6-9 digits selected)	$\left(\frac{10}{\text{Freq. B x Gate Time}}\right)$, rounded to nearest decade*
Resolution*:	± LSD ± (Trig. Error B*/Gate Time) x Ratio
Accuracy*:	± Resolution
Ratio C/B (Model 1992 only)	
Specified for higher frequency applied to Input C	
Range:	Input C 40 MHz to 1.3 GHz Input B DC to 100 MHz

*See Definitions
†2LSD for 6-9 digits displayed

Table 1.1 - 1991/1992 Specifications (Cont'd)

LSD Displayed: **(for 6-9 digits selected)**	$\left(\frac{640}{\text{Freq. B x Gate Time}}\right)$, rounded to nearest decade*
Resolution* and Accuracy*:	As for Ratio A/B
Totalize A by B	
Accumulative or single totalize	
Input:	Input A
Range:	10^{12}-1 (Max. 9 most significant digits displayed)
Maximum Rate:	10^{8} events/s
Minimum Pulse Width:	5 ns min. at trigger points
Accuracy:	± 1 count
Start/Stop:	Electrical (Input B) or Manual
Phase (A rel. to B)	
Range:	0.1° to 360°
LSD Displayed:	0.1° to 1 MHz 1.0° to 10 MHz 10° to 100 MHz
Resolution* (degrees):	± LSD ± (TI Resolution/Period A) x 360°
Accuracy* (degrees):	± LSD ± (TI Accuracy/Period A) x 360°
Amplitude Measurement	
Peak*	
Frequency Range:	50 Hz to 20 MHz
Amplitude Range:	160 mV p-p to 51V p-p
Resolution:	
x1 attenuation:	20 mV
x10 attenuation:	200 mV
Accuracy:	
x1 attenuation:	± 50 mV ± 6%V p-p (Typically ± 40 mV ± 2%V p-p)
x10 attenuation:	± 500 mV ± 10%V p-p (Typically ± 400 mV ± 3%V p-p)

*See Definitions

DC (<15 mV p-p AC)	
Amplitude Range:	± 51V
Resolution:	
x1 attenuation:	20 mV
x10 attenuation:	200 mV
Accuracy:	
x1 attenuation:	± 40 mV ± 1% Rdg.
x10 attenuation:	± 400 mV ± 1% Rdg.

Math

Available on all measurements except Phase and Check

Function:	(Result - X)/Z
Entry Range:	$\pm 1 \times 10^{-10}$ to $\pm 1 \times 10^{10}$ to 9 significant figures

EXTERNAL ARMING

A comprehensive external arming capability to determine the START and/or STOP point of a measurement. Available on all measurement functions except phase.

Input Signal: (via Rear Panel)	TTL compatible (min. pulse width 200 ns)
Slope:	+ve or -ve independently selectable on START or STOP arm
Impedance:	1 kohm nominal

BASIC FREQUENCY STANDARD

Internal Frequency:	10 MHZ
Adjustment Range:	± 5 ppm min. at shipment, by single turn trimmer via rear panel
Aging:	
Initial	1 ppm/month at shipment
Long Term	2 ppm/first year
Temperature Stability:	± 10 ppm over the range 0° to 50 °C, referenced to 25°C
Frequency Standard Output:	
Frequency:	10 MHz
Amplitude:	>600 mV p-p into 50 ohms
Impedance:	250 ohms nominal
External Standard Input:	
Frequency:	10 MHz
Signal Amplitude:	Min. 100 mV rms
(Sine Wave)	Max. 10V rms
Impedance:	1 kohm nominal at 1V p-p 500 ohms nominal at 10V p-p

Table 1.1 - 1991/1992 Specifications (Cont'd)

GENERAL SPECIFICATIONS	
Gate Time: **(Frequency, Period, and Ratio modes)**	Automatically determined by resolution selected (Range 1 ms - 10s)* Resolution Selected: / Gate Time: (seconds) 9 + overflow / 10 9 / 1 8 / 0.1 7 / 0.01 6,5,4,3 / 0.001
Single Cycle: **(Hold)**	Enables a single measurement to be initiated and held
Display:	9-digit, high brightness, 14 mm LED display in engineering format with exponent digit
Power Requirements:	
Voltage:	90-110 103-127 193-237 207-253 VAC
Frequency:	45-450 Hz
Rating:	35 VA max.
Environmental Requirements:	
Temperature, Storage:	-40°C to +75°C at 75%RH
Temperature, Operating:	0°C to +50°C
Relative Humidity:	95% to 30°C 75% to 40°C 45% to 50°C
Altitude, Storage:	12,000 meters
Altitude, Operating:	3,050 meters
Vibration:	2 g
Shock:	30 g
Safety:	Designed to meet the requirements of IEC 348 and follow the guidelines of UL1244
Weight:	Net 3.63 kg (8 lb) Shipping 5.5 kg (11 lb)
Dimensions, Instrument:	331 x 212 x 88 mm (13.03 x 8.35 x 3.46 in)

*See Definitions

OPTIONS

List of Options and Accessories

01*	Rear Panel Inputs	11-1709 (Model 1991) 11-1732 (Model 1992)
01*	Rear Panel Inputs	11-1713
04T**	Temperature Controlled Crystal Oscillator	11-1710
04A**	Oven Oscillator	404386
04E**	High Stability Oven Oscillator	11-1625
07†	Battery Pack	11-1645
10	Reference Frequency Multiplier	404574
55†	GPIB Interface	11-1730
60	Handles	11-1648
60A	Rack Mounting Kit (Fixed, Single)	11-1649
60B	Rack Mounting Kit (Fixed, Double)	15-0773
61	Carrying Case	15-0736
61M	Protectomuff Case	11-1716
65	Chassis Slides (incl. Rack Mounts)	11-0167
	Thru-line Connector	23-9020
	Telescopic Antenna	23-9104
	High Impedance Probe	11-1718
	1.3 GHz Fuse (Pkt. 5)	

*Installing Option 01 may affect certain specification parameters

**Only one frequency standard may be installed at any one time. The standard reference will be supplied unless Option 04T, 04A, or 04E is specified

† The battery pack and GPIB options cannot both be installed at the same time

Option 01 Rear Panel Inputs

A rear-panel input, factory-fitted option, is available for ATE applications. Inputs A and B are in parallel with those on the front panel while Input C (Model 1992 only) is fitted in place of the front panel input.

Option 04T Temperature Controlled Crystal Oscillator

Frequency:	10 MHz
Aging Rate:	$\leq 3 \times 10^{-7}$/month $\leq 1 \times 10^{-6}$ in the first year
Temperature Stability:	$\leq 1 \times 10^{-6}$ over the range 0°C to +40°C (Operable to +50°C)
Adjustment:	Via rear panel

Option 04A Ovened Oscillator

Frequency:	10 MHz
Aging Rate:	$\leq 3 \times 10^{-9}$/day averaged over 10 days after 3 months continuous operation
Temperature Stability:	$\leq 3 \times 10^{-9}$/°C averaged over range 0° to + 45° C (operable to +50° C)
Warm Up:	Typically $\pm 1 \times 10^{-7}$ within 6 minutes
Adjustment:	Via rear panel

Table 1.1 - 1991/1992 Specifications (Cont'd)

Option 04E High- Stability Ovened Oscillator	
Frequency:	10 MHz
Aging Rate:	$\leq 5 \times 10^{-10}$/day at shipment averaged over 10 days
Temperature Stability:	$\leq 7 \times 10^{-9}$ over the range 0°C to 50°C
Line Voltage Stability:	$\leq 5 \times 10^{-10}$ two minutes after a 10% line voltage change
Adjustment	Via rear panel
Option 07 Rechargeable Battery Pack and External DC Operation	
Battery Type:	Sealed lead-acid cells
Battery Life:	Typically 4 hours at 25°C (10 hrs on standby)
Battery Condition:	Display indicates battery low
External DC:	11-16V via socket on rear panel (-ve ground, not isolated)
Option 10 Reference Frequency Multiplier	
Input Frequency:	1,2,5 or 10 MHz ($\pm 1 \times 10^{-5}$)
Input Amplitude and Impedance:	As for external standard input
Option 55 GPIB Interface	Designed to comply with IEEE-STD-488 (1978) and to conform with the guidelines of IEEE-STD-728 (1982).
Control Capability:	All functions and controls are programmable except power on/off and standby charge
Output:	Engineering format (11 digits and exponent)
IEEE-STD-488 Subsets:	SH1,AH1,T5,TE0,L4,LE0,SR1,RL1,PP0,DC1, DT1,C0,E2
Handshake Time:	250µs to 1ms/character dependent on message content
Read Rate:	Typically 20/s dependent upon measurement function

SUPPLIED ACCESSORIES

Power Cord
Instruction Manual
Spare Fuse
Spare 1.3 GHz Fuse (Model 1992 only)

DEFINITIONS

LSD (Least Significant Digit)
In Frequency and Period modes, display automatically upranges at 1.1 x decade and downranges at 1.05 x decade, except on Input C for input frequency >1 GHz

Accuracy and Resolution is expressed as an RMS value

Table 1.1 - 1991/1992 Specifications (Cont'd)

Trigger Error RMS

$$\text{Trigger Error (seconds)} = \sqrt{\frac{(e_{i1}^2 + e_{n1}^2)}{S1^2} + \frac{(e_{i2}^2 + e_{n2}^2)}{S2^2}}$$

where e_i = input amplifier RMS noise (typically 150 µV RMS in 160 MHz bandwidth)
e_n = input signal RMS noise in 160 MHz bandwidth
S^n = Slew rate at trigger point V/s
Suffix 1 denotes START edge
Suffix 2 denotes STOP edge
In Frequency A, Period A, Frequency B, and Period B modes, triggering is always on positive-going edge

Trigger Level Timing Error

$$\text{Trigger Level Timing Error (seconds)} = 0.035\left(\frac{1}{S1} - \frac{1}{S2}\right)$$

$$\text{typically} = 0.018\left(\frac{1}{S1} - \frac{1}{S2}\right)$$

S1 = Slew rate on START edge V/s
S2 = Slew rate on STOP edge V/s

Gate Time

The nominal gate time indicated is set by the resolution selected in Frequency, Period, Ratio, and Check modes. It is the value which is used in the calculation of LSD and Resolution. The true gate time will be extended from this value by up to:

(a). One period of the input signal(s) on Frequency B, Period B, and Ratio A/B

(b). Two periods of the input signal on Frequency A and Period A

(c). One period of input signal B on Ratio C/B (Model 1992 only)

Peak and Peak-to-Peak Amplitudes

Peak is defined as being the highest or lowest point at which the signal width is 5 ns. Similarly, Peak-to-Peak is the difference between the highest and lowest points at which the signal width is 5 ns.

ORDERING INFORMATION

1991 160 MHz Universal Counter
1992 1300 MHz Universal Counter

1.4 SAFETY

1.4.1 The 1991/1992 incorporates a protective ground terminal and is designed to meet international safety requirements. Refer to the Safety Page "FOR YOUR SAFETY" immediately preceding the Table of Contents. Follow all **NOTES**, **CAUTIONS**, and **WARNINGS** to ensure personal safety and prevent damage to the instrument.

1.5 PRODUCT SUPPORT

1.5.1 Racal-Dana supports the 1991/1992 with Product Engineering, Service, and Parts Departments. A complete listing of service centers and field representatives is provided on the last two pages of the manual.

1.6 GENERAL DESCRIPTION

1.6.1 The 1991/1992 is a universal timer/counter designed for system or bench use. Basic measurement functions (described briefly in Subsection 1.6.2) include Frequency, Period, Time Interval, Totalize, Phase, and Ratio.

1.6.2 Measurement Functions

1.6.2.1 Frequency A Function

1.6.2.1.1 Frequency A function is used to measure the frequency of the signal applied to the Channel A input. A resolution of nine digits is available with a one-second gate time.

1.6.2.2 Frequency B Function

1.6.2.2.1 Special Function 21 (see Subsection 3.8 "Special Functions"), permits Frequency B measurements. Frequency B function is used to measure the frequency of the signal applied to the Channel B input. A resolution of nine digits is available with a one-second gate time.

1.6.2.3 Frequency C Function (Model 1992 only)

1.6.2.3.1 Frequency C function is used to measure the frequency of the signal applied to the Channel C input. A resolution of nine digits is available with a one-second gate time.

1.6.2.4 Period A Function (See Note below)

1.6.2.4.1 Period A function is used to measure the period of the waveform applied to the Channel A input. A number of periods, depending upon the resolution (and, therefore, the gate time) selected, are measured and the average value is displayed.

1.6.2.5 Time Interval A→B Function (See Note below)

1.6.2.5.1 Time Interval function is used to perform single-shot measurements of the time interval between:

a. An event occurring at the Channel A input and a later event at the Channel B input (using separate input channels)

b. Two events occurring at the Channel A input (using a common input channel)

1.6.2.5.2 The arming of the stop circuit can be delayed for a specific time set by the operator. This feature prevents the measurement interval being stopped prematurely by spurious pulses, such as those caused by relay contact bounce.

1.6.2.6 Total A Function (See Note below)

1.6.2.6.1 Total A function permits events occurring at the Channel A input to be totalized. The counting interval can be controlled by:

a. Electrical start and stop signals applied to the Channel B input (Total A by B)

b. Successive operations of a front-panel key (Manual Totalize)

1.6.2.6.2 Delayed arming of the stop circuit to prevent spurious triggering is available in the Total A by B measurement mode. The Manual Totalize mode provides the capability for totalizing cumulatively over a number of periods.

1.6.2.7 Phase A rel B Function (See Note below)

1.6.2.7.1 Phase A rel B function is used to measure the phase difference between the waveform applied to the Channel A input and that applied to the Channel B input. The phase difference is displayed in degrees, and indicates the phase lead at the Channel A input. The signals for phase measurement must be continuous and have the same frequency.

1.6.2.8 Ratio A/B Function

1.6.2.8.1 Ratio A/B function is used to measure the ratio of the frequency applied to the Channel A input to that applied to the Channel B input.

1.6.2.9 Ratio C/B Function (Model 1992 only)

1.6.2.9.1 Ratio C/B function is used to measure the ratio of the frequency applied to the Channel C input to that applied to the Channel B input.

NOTE:

Special Function 21 (see Subsection 3.8 "Special Functions") permits Period B, Time Interval B →A, Total B by A, and Phase B rel A. For these functions, note the following:

a. Period B is specified down to 10 ns

b. Total B by A operates for one complete cycle of the Channel A signal. The stop circuit delay is available on Channel A

1.6.3 Check Function

1.6.3.1 With the Check function selected, a number of functional tests of the instrument's circuits can be made without the use of additional test equipment. Although these tests do not check the instrument's performance to published specifications, they can be used to verify that the equipment is operating correctly following receipt or transportation to a new location. A brief, preliminary functional check procedure is given in Subsection 2.6.

1.6.4 Input Signal Channels

1.6.4.1 Inputs A and B are fully independent. However, provision is made for connection of the signal at the Channel A input into both channels. This is effected by selecting the COM(mon) A mode. When COM A is selected, Channel B's input socket is isolated from Channel B's circuitry.

1.6.4.2 Inputs A and B are provided with independent controls to permit the following selections:

a. AC or DC input coupling

b. 1MΩ or 50Ω input impedance

c. x1 or x10 input attenuation

d. Positive or negative-slope trigger

e. Manually or automatically-set input trigger level

1.6.4.2.1 The manually-set trigger level is entered as an internal store.

1.6.4.2.2 The auto-trigger level is derived by measuring the positive and negative peaks of the input signal. If the peak-to-peak value exceeds 5.1V or if either peak is outside the range ± 5.1V, the x10 attenuator is automatically switched in. The trigger level is then set to the arithmetic mean of the measured value.

1.6.4.2.3 When operating in the auto-trigger mode, with the x10 attenuator in circuit, the attenuator will be switched out if the peak-to-peak value is less than 4.6V and both peak values are within the range ± 4.6V.

1.6.4.2.4 The trigger levels in use are available at pins mounted on the rear panel of the instrument. The voltage range is ± 5.1V regardless of whether the attenuator is switched in or not, so the voltage should be multiplied by 10 when the x10 attenuator is selected.

1.6.4.3 Input C is available on the Model 1992 only. It has a nominal input impedance of 50Ω and is AC-coupled. Protection against excessive signal levels is provided by a fuse mounted in the input socket.

1.6.5 Low-Pass Filter

1.6.5.1 An internal low-pass filter can be introduced to reduce the bandwidth of Channel A to 50 kHz (nominal).

1.6.6 Math Function

1.6.6.1 When the math function is active, the displayed value is:

$$\frac{\text{Measurement Result} - X}{Z}$$

where X and Z are values entered into stores within the instrument by the operator. X is set to 0 and Z to 1 when the instrument is first switched on. By suitable choice of values for X and Z, ratio, offset (null), and percentage-difference displays can be obtained.

1.6.7 Special Functions

1.6.7.1 A number of special functions are available to the operator. These provide test procedures and operating facilities in addition to those available by operation of the front-panel controls. See Subsection 3.8 of this manual for further details.

1.6.8 Error Indication

1.6.8.1 When operating the 1991/1992, certain errors will result in displayed error codes. See Subsection 3.9 of this manual for further details.

1.6.9 External Arming

1.6.9.1 External arming of the start and stop circuits for the measurement interval can be carried out by means of signals connected to a rear-panel mounted socket. Any combination of internal and external arming can be selected by using the appropriate special function. For further details, refer to Subsections 3.8 and 3.11 along with Table 3.12 in this manual.

1.6.10 Display Format

1.6.10.1 The display uses an engineering format, with a nine-digit mantissa and one exponent digit. Overflow of the most significant digits can be used to increase the display resolution.

1.6.11 Hold Feature

1.6.11.1 The hold feature allows readings to be held indefinitely. A new measurement cycle is initiated using the RESET key.

1.6.12 Resolution and Gate Time

1.6.12.1 The counting interval (gate time) in the Total A by B mode is controlled by the time interval between the start and stop signals at the Channel B input. In the Manual Totalize mode, the gate time is determined by successive operations of the HOLD key. In the Frequency A, Frequency C, Period A, Ratio A/B, and Ratio C/B modes, the gate time is determined by the selected display resolution. In Phase mode, the gate time is fixed and the display resolution is determined by the input signal frequency. Details of the relationship between gate time and resolution for each measurement mode are provided in Subsection 3.6 of this manual.

1.6.13 External Frequency Standard Input

1.6.13.1 The 1991/1992 may be operated using an external frequency standard. The instrument will operate from the external standard whenever the signal at the EXT STD INPUT socket is of sufficient amplitude. The instrument will automatically revert to internal standard operation if the input from the external standard is removed.

1.6.14 Standby Mode

1.6.14.1 When the instrument is switched to standby, the internal frequency standard continues to operate, but the measuring circuits are disabled.

1.6.15 Initialization

1.6.15.1 When the 1991/1992 is first switched on or when it is initialized via the GPIB interface, it is set to the following conditions:

Measurement Function:	Frequency A
Display Resolution:	8 digits
Continuous Measurement Mode:	Enabled
Channel A and B Inputs:	Manual trigger AC coupling Positive-slope trigger 1MΩ input impedance Filter disabled Common input disabled
Trigger Level	0.00V
Delay:	Disabled
Delay Store:	200 µs
Math Function:	Disabled
X Store:	0
Z Store:	1
Hold:	Disabled
Special Functions:	Functions 10, 20, 30, 40, 50, 60, and 70 enabled
SRQ Message:	Generated upon error detection

1.6.16 **Options**

1.6.16.1 **Frequency Standards (04X Options)**

1.6.16.1.1 Frequency standard Options 04-T, 04-E, and 04-A are available. The technical specifications are given in Table 1.1 of this section. The frequency standard can be changed, if required, by the customer; instructions are provided in Section 2.

1.6.16.2 **Reference Frequency Multiplier (Option 10)**

1.6.16.2.1 The reference frequency multiplier is an internally-mounted, phase-locked multiplier, which permits the use of external frequency standard signals of 1 MHz, 2 MHz, 5 MHz or 10 MHz. The multiplier can be installed by the customer; instructions are given in Section 2.

1.6.16.3 **GPIB Interface (Option 55)**

1.6.16.3.1 An internally mounted interface to the IEEE-488-GPIB is available. This permits remote control of all the instrument's functions except the power ON/OFF and standby switching. The interface can be installed by the customer; instructions are given in Section 2.

1.6.16.3.2 The GPIB interface cannot be installed in an instrument already provided with the battery pack option. An adapter, Racal-Dana Part Number 23-3254, to convert the connector to the IEC 625-1 standard is available as an optional accessory.

1.6.16.4 **Battery Pack (Option 07)**

1.6.16.4.1 Installing the internal battery pack option permits the counter to be used in locations where no suitable AC supply is available. This option also allows operation from an external DC supply.

1.6.16.4.2 The battery is trickle-charged whenever the instrument is operated from an AC supply. Charging at the full rate is carried out when the instrument is switched to the standby mode. A full charge requires approximately 14 hours.

1.6.16.4.3 The counter will operate continuously for approximately 4 hours from a fully-charged battery. It will switch off automatically when the battery approaches the discharged condition. The STBY/CHRG LED starts to flash approximately 15 minutes before this occurs. The battery life can be extended by using the Battery-Save feature.

1.6.16.4.4 The battery pack option can be installed by the customer. Instructions are given in Section 2. The battery pack option cannot be installed to an instrument already provided with the GPIB interface option.

1.6.16.5 **Rack Mounting Kits**

1.6.16.5.1 The following kits, permitting the instrument to be mounted in a standard 19-inch rack, are available:

a. Single instrument, fixed-mount kit (Option 60A)
(Racal-Dana Part Number 11-1648)
The mounted instrument occupies half the rack width and is two rack units (3.5 inches) in height. The instrument is mounted offset in the rack and may be at either side.

b. Double instrument, fixed-mount kit (Option 60B)
(Racal-Dana Part Number 11-1649)
The panel of the mounting kit occupies the full-rack width and is two rack units (3.5 inches) in height. Two instruments can be mounted side-by-side.

1.6.16.5.2 All rack-mounting kits can be installed by the customer. Instructions are given in Section 2.

1.6.16.6 **Elapsed Time Indicator (Option ETI)**

1.6.16.6.1 A non-mercuric elapsed time indicator can be factory installed inside the instrument as an option. The elapsed time can be read by removing the instrument's top cover.

SECTION 2 INSTALLATION & PREPARATION FOR USE

2.1 INTRODUCTION

2.1.1 This section provides information on unpacking and inspection, reshipment, power connections, storage and temperature, functional checking, miscellaneous setup procedures, and option installation instructions for the 1991/1992.

2.2 UNPACKING AND INSPECTION

2.2.1 Before unpacking the counter, check the exterior of the shipping carton for any signs of damage. All irregularities should be noted on the shipping bill. Unpack and remove the instrument carefully from its carton, preserving the factory packaging as much as possible. Inspect the counter for any defect or damage. Notify the carrier immediately if any damage is apparent. Have a qualified person check the instrument for safety before use.

2.3 RESHIPMENT INSTRUCTIONS

2.3.1 Use the original packaging if it is necessary to return the counter to Racal-Dana for calibration and/or servicing. The original shipping carton and the instrument's plastic-foam form will provide the necessary support for safe reshipment. If the original packaging is unavailable, reconstruct it as much as possible. Wrap the counter in plastic; then use plastic spray foam to surround and protect the instrument. Reship in either the original or new, sturdy shipping carton.

2.4 POWER CONNECTIONS

2.4.1 Before operating the counter, verify that the AC voltage selector is correctly set for the local AC supply. The counter operates on 100, 120, 220, or 240 volts, 45 to 450 Hz. The present voltage range can be seen through the small open window in the rear panel to the left of the AC power plug.

2.4.2 Line Voltage Selection

2.4.2.1 The line voltage setting is easily changed by repositioning the small printed circuit card (voltage selector card) which is mounted horizontally in its slot and accessed via the small rear-panel window. Complete the following procedure to change the voltage setting:

a. Remove the AC power cord from the rear panel

b. Remove the keeper bracket with its one screw and washer from the voltage card window. This completely exposes the voltage selector card

c. Remove the voltage selector card via the small window; reposition it in its slot so that the desired line voltage designation is now visible through the window. (Using a small pair of needle-nose pliers in completing this last step is recommended.)

d. Securely replace the keeper bracket using its hardware

e. Connect the power cord to the counter again

2.4.3 Line Fuse

2.4.3.1 Verify that the rating of the line fuse is suitable for the AC voltage range selected. The fuse should be of the 1/4 in x 1- 1/4 in, glass cartridge, surge-resistant type. The required rating is:

90V to 127V: 500 mA (Racal-Dana P/N 920204)
123V to 253V: 250 mA (Racal-Dana P/N 920756)

2.4.4 Power Cord and Grounding

2.4.4.1 The front panel and instrument case meet the Type III grounding requirements of MIL-T-28800C, protecting the user from possible injury due to electrical shock.

NOTE:

The 1991/1992 is designed to meet IEC Publication 348, "Safety Requirements for Electronic Apparatus for Class I Instruments."

2.4.4.2 A protective ground terminal, forming part of the rear-panel power input socket, is provided. The 1991/1992 is supplied with a detachable 3-conductor power cord. Only this cord should be used.

2.4.4.3 Use only AC power outlets having a protective ground for connection to the counter. **DO NOT USE** 2-conductor extension cords or 3-prong to 2-prong adapters that don't provide a protective ground connection. Connection of the power cord to the power outlet must be made in accordance with the following standard color code:

	American	European
Live	Black	Brown
Neutral	White	Blue
Ground (Earth)	Green	Green/Yellow

2.5 STORAGE AND TEMPERATURE

2.5.1 The 1991/1992 can be stored at temperatures ranging from -40°C to 75°C at 75% relative humidity without adverse effects to PCBs or components. The counter must be brought within its specified operating range of 0°C to 50°C before power-on.

2.6 FUNCTIONAL CHECK

2.6.1 Introduction

2.6.1.1 The following procedure confirms whether or not the 1991/1992 is performing correctly by checking most of the counter's circuitry. The procedure should be conducted when the 1991/1992 is first put into service and after shipment to a new location. This procedure does not check that the instrument is operating to published specification. Detailed Performance Verification Procedures (PVPs) are given in Section 6 of this manual.

NOTE:

A 50 Ω coaxial test lead, fitted with BNC connectors, is required. This lead must be at least 60 cm, but not more than 1m long.

2.6.1.2 Perform the following procedure:

a. Connect the 1991/1992 to a suitable AC supply

b. Turn the instrument on. Verify that the instrument's model number appears in the display for approximately two seconds, followed by a number indicating the software version and issue numbers. The instrument should assume the following home state:

1. Display should be 00000000, providing a display resolution of 8 digits

2. Hz, RESOLUTION, FREQ A, INPUT A $\int$, and INPUT B $\int$ LEDs should be lit

3. INPUT A and B TRIG LEDs may or may not be lit

c. Press the FUNCTION ▼ key until the CHECK LED lights. Check that the display shows 10.0000000 E6 and that the GATE LED is flashing

d. Verify that the RESOLUTION LED is lit. Press the RESOLUTION ▼ key five times, ensuring that the resolution of the display is decreased by one digit each time

e. Press the RESOLUTION ▲ key to increase the display to nine digits

2.6.1.3 If required, the following additional checks may also be performed, using the instrument's special functions.

a. Complete the following key sequence:

[7] [1] [SHIFT] [STORE] [SF] [SHIFT] [SF]

Check that all LEDs, with the exception of TRIG A, TRIG B, GATE and STBY/CHRG flash on and off every two seconds. Verify that REM, ADDR, and SRQ LEDs are illuminated and do not flash

b. Connect the 10 MHz STD OUTPUT socket on the rear panel to the front panel INPUT A connector, using the coaxial test lead

c. Complete the following key sequence:

[7] [7] [SHIFT] [STORE] [SF]

Verify that the display shows *0.******* E0 Hz after about 6 seconds (where * indicates a blanked digit). The x10, 50 Ω, DC, FILTER and COM A LEDs for Channel A should light sequentially

d. Disconnect the coaxial lead from the INPUT A connector. The display should show an error number after a few seconds

e. Connect the coaxial lead to the INPUT B connector

f. Complete the following procedure:

[7] [8] [SHIFT] [STORE] [SF]

Check that the display shows *0.******* E0 Hz after about 4 seconds. The x10, 50 Ω and DC LEDs for Channel B should light sequentially

g. Disconnect the coaxial lead from the INPUT B connector and the 10 MHz STD OUT connector. The display should show an error number after a few seconds

h. Switch the instrument off

2.7 MISCELLANEOUS SETUP PROCEDURES

2.7.1 Frequency Standard

2.7.1.1 If it is intended to use an external frequency standard, the output of the frequency standard should be connected to the EXT STD INPUT connector on the rear panel of the instrument. The connection should be made using coaxial cable. Switch on the frequency standard and the instrument; check that the EXT STD LED on the front panel of the instrument lights.

2.7.1.2 A 10 MHz signal, derived from the internal frequency standard, is available at the 10 MHz STD OUT connector on the rear panel of the instrument. If this signal is used, the connection should be made using coaxial cable.

2.7.2 External Arming

2.7.2.1 If external arming is to be used, the arming signal should be connected to the EXT ARM INPUT connector on the rear panel.

2.7.3 Trigger Level Output

2.7.3.1 The trigger levels in use on Channels A and B are available via pins on the instrument's rear panel. If required, connection to the pins should be made using a clip-on probe or small alligator clip.

2.8 OPTION INSTALLATION INSTRUCTIONS

2.8.1 Single-Instrument Fixed-Rack Mounting Kit (Option 60A)

2.8.1.1 This kit comprises:

Item	Qty	Racal-Dana Part Number
Short mounting bracket	1	16-0643
Long mounting bracket	1	16-0644
Screw, M4 x 16	4	24-7733
Crinkle washer, M4	4	24-2802
Spacer, plain, M4 x 5	4	24-4112
Screw, M6 x 16	4	24-7995
Finishing washer, M6	4	24-2809
Captive nut, M6	4	24-2240

2.8.1.2 Assemble the kit to the instrument as follows:

a. Disconnect the AC power cord at the rear panel

b. Remove the two screws which secure the bezel to the rear panel; remove the bezel

c. Remove the bottom cover by sliding it towards the rear of the instrument

d. Remove the instrument's feet from the bottom cover

e. Replace the bottom cover. Replace and secure the bezel

f. Remove the four plugs from the sides of the instrument. This will reveal two threaded holes in each side frame

g. On one side of the instrument, secure a mounting bracket to the side frame using two spacers, M4 screws, and crinkle washers. Position the spacers between the mounting bracket and the side frame

h. Repeat step g on the other side of the instrument

i. Fit the finishing washers to the M6 screws. Hold the instrument up to the rack in the required position, and secure the brackets to the rack using the M6 screws and nuts

2.8.2 **Double-Instrument Fixed-Rack Mounting Kit (Option 60B)**

2.8.2.1 The kit comprises:

Item	Qty	Racal-Dana Part Number
Short mounting bracket	2	16-0643
Screw, M4 x 16	4	24-7733
Crinkle washer, M4	4	24-2802
Spacer, plain, M4 x 5	4	24-4112
Spacer, female	2	14-1583
Spacer, male	2	14-1584
Mating plate	1	13-2000
Rivet, plastic	4	24-3211
Screw, M6 x 16	4	24-7995
Finishing washer, M6	4	24-2809
Captive nut, M6	4	24-2240

2.8.2.2 Prepare both instruments as follows:

a. Disconnect the AC power cord at the rear panel

b. Remove the two screws which secure the bezel to the rear panel; remove the bezel

c. Remove the bottom cover by sliding it towards the rear of the instrument

d. Remove the instrument's feet from the bottom cover

e. Replace the bottom cover. Replace and secure the bezel

f. Remove the four plugs from the sides of the instrument. This will reveal two threaded holes in each side frame

g. Remove two buffers from the bezel at the side which is to be at the center of the rack

2.8.2.3 Assemble the kit to the instruments as follows:

a. At the sides which are to be at the center of the rack, secure the female spacers to one instrument and the male spacers to the other. The spacers screw into the threaded holes in the side frames

b. At the other side of each instrument, secure a mounting bracket to the side frame, using two plain spacers, M4 screws, and crinkle washers. Position the spacers between the mounting bracket and the side frame

c. Fit the male spacers on one instrument into the female spacers on the other

d. Position the mating plate to bridge the gap between the bezels. Secure it by pushing the plastic rivets through the plate into the buffer holes

e. Fit the finishing washers to the M6 screws. Hold the two instruments up to the rack in the required position, and secure the brackets to the rack using the M6 screws and nuts

2.8.3 PCB-Mounted Frequency Standard (Option 04T)

2.8.3.1 The kit comprises:

Item	Qty	Racal-Dana Part Number
Plate assembly	1	11-1610
Oscillator PCB	1	19-1208
Crinkle washer, M3	3	24-2801
Screw, M3 x 6	3	24-7721

2.8.3.2 Install the PCB-mounted frequency standard as follows:

a. Disconnect the AC power cord at the rear panel

b. Remove the two screws which secure the bezel to the rear panel; remove the bezel

c. Remove the top cover by sliding it towards the rear of the instrument

d. Remove the frequency standard already installed. Instructions are given in paragraphs 2.8.3.3 or 2.8.4.3, according to type

e. Secure the PCB to the plate assembly, using an M3 screw and washer from the kit. The screw should be passed through the mounting hole in the board and screwed into the threaded spacer of the plate assembly. The component side of the board should be towards the plate assembly

f. Connect the PCB to the motherboard at PL14, with the plate assembly towards the rear panel of the instrument

g. Secure the plate assembly to the rear panel, using two M3 screws and washers. The screws pass through the holes adjacent to the FREQ STD ADJUST aperture and screw into the plate assembly

h. Replace the top cover. Replace and secure the bezel

2.8.3.3 Remove the PCB-mounted frequency standard as follows:

a. Remove the two screws adjacent to the FREQ STD ADJUST aperture in the rear panel

b. Pull the PCB and plate assembly upwards until the board is disconnected from the motherboard

2.8.4 Ovened Frequency Standards (Options 04A and 04E)

2.8.4.1 The kit comprises:

Item	Qty	Racal-Dana Part Number
Oscillator assembly	1	11-1710 for 04A 404386 for 04E
Crinkle washer, M3	2	24-2801
Screw, M3 x 6	2	24-7721

2.8.4.2 Install the frequency standard as follows:

a. Disconnect the AC power cord at the rear panel

b. Remove the two screws which secure the bezel to the rear panel; remove the bezel

c. Remove the top cover by sliding it towards the rear of the instrument

d. Remove the frequency standard already installed. Instructions are given in paragraph 2.8.3.3 or 2.8.4.3, according to type

e. Connect the flying lead on the oscillator assembly to SK14 on the motherboard

f. Secure the oscillator assembly to the rear panel of the instrument, using the M3 screws and washers. The screws pass through the holes adjacent to the FREQ STD ADJUST aperture and screw into the oscillator assembly

g. Replace the top cover. Replace and secure the bezel

2.8.4.3 Remove the frequency standard as follows:

a. Remove the two screws adjacent to the FREQ STD ADJUST aperture in the rear panel

b. Lift the oscillator assembly out of the chassis and disconnect the flying lead from the motherboard at PL14

2.8.5 Reference Frequency Multiplier (Option 10)

2.8.5.1 The kit comprises:

Item	Qty	Racal-Dana Part Number
Frequency multiplier	1	19-1164
Crinkle washer, M3	2	24-2801
Screw, M3 x 6	2	24-7721

2.8.5.2 Install the reference frequency multiplier as follows:

a. Disconnect the AC power cord at the rear panel

b. Remove the two screws which secure the bezel to the rear panel; remove the bezel

c. Remove the top cover by sliding it towards the rear of the instrument

d. Remove the frequency standard if an ovened type is installed

e. Remove the shorting link from between pins 8 and 9 on PL16

NOTE:

This link should be stored in a safe and convenient place. It must be replaced if Option 10 is removed from the instrument

f. Connect the frequency multiplier PCB to the motherboard at PL16 and PL17, with the threaded spacers towards the right-hand side frame

g. Secure the PCB to the side frame, using the M3 screws and washers

h. Replace and secure the frequency standard if it was removed in step d

i. Replace the top cover. Replace and secure the bezel

2.8.6 GPIB Interface (Option 55)

2.8.6.1 The kit comprises:

Item	Qty	Racal-Dana Part Number
GPIB PCB assembly	1	19-1146
Lock washer, M3	2	24-2813
Screw, M3 x 6	2	24-7721

NOTE 1:

This option cannot be installed in an instrument already provided with the battery pack option.

NOTE 2:

The software version number (the first part of the decimal number) on the GPIB ROM (IC10) must be the same as that for the main instrument ROM (IC22 on the motherboard).

2.8.6.2 Install the GPIB interface option as follows:

a. Disconnect the AC power cord at the rear panel

b. Remove the two screws which secure the bezel to the rear panel; remove the bezel

c. Remove the top cover by sliding it towards the rear of the instrument

d. Remove the blanking plate from the rear panel by pushing out the plastic rivets from the inside of the instrument

e. Hold the GPIB PCB, component side down, with the GPIB connector towards the rear panel. Connect the ribbon cable to the motherboard at SK4

f. Tilt the board, and lower it into the instrument. Position it with the support brackets just below the top flanges of the side frames

g. Slide the board towards the rear panel so that the support brackets enter the grooves immediately below the top flanges of the side frames

h. Secure the bracket which carries the GPIB connector to the rear panel using the M3 screws and washers

NOTE:

The screws and washers provide the ground connection between the GPIB connector and the instrument chassis. Tighten the screws firmly to ensure that a good connection is obtained

i. Replace the top cover. Replace and secure the bezel

2.8.7 **Battery Pack (Option 07)**

2.8.7.1 The kit comprises:

Item	Qty	Racal-Dana Part Number
PCB assembly	1	11-1722
Mounting bracket	1	11-1599
Battery pack	1	11-1723
Cover plate	1	13-2040
Crinkle washers, M3	2	24-2801
Screws, M3	2	24-7721
Crinkle washers, M4	6	24-2802
Plain washers, M4	2	24-2705
Screws, M4	6	24-7730
Spare fuse, 3AT	1	23-0069

NOTE:

This option cannot be installed in an instrument already fitted with the GPIB interface option

2.8.7.2 Install the battery pack as follows:

a. Disconnect the AC power cord at the rear panel

b. Remove the two screws which secure the bezel to the rear panel; remove the bezel

c. Remove the top cover by sliding it towards the rear of the instrument

d. Remove the blanking plate from the rear panel by pushing out the plastic rivets from the inside of the instrument

e. If a PCB-mounted frequency standard is installed, remove the two screws adjacent to the FREQ STD ADJUST aperture

f. Remove the four screws which secure the rear panel to the side frames

g. Ease the rear panel away from the instrument until it disconnects from the motherboard at PL19 and PL20

h. Hold the PCB assembly with the switches towards the rear of the instrument and the PCB connector pointing downwards

i. Lower the PCB assembly into the chassis and connect the PCB to the motherboard at PL21, taking care that it mates correctly

j. Replace and secure the rear panel

k. If a PCB-mounted frequency standard is installed, secure it to the rear panel with the screws removed in step e

l. Position the cover plate over the switch protruding through the rear panel. Secure the cover plate and the rear panel to the PCB assembly using the M3 screws and washers

m. Secure the mounting bracket to the right-hand side frame using two M4 screws and washers. The horizontal flange should be towards the top of the instrument

n. Position the battery pack within the chassis using the supporting lugs resting on the mounting bracket. Secure the battery pack to the left-hand side frame using two M4 screws and washers

o. Secure the supporting lugs to the mounting bracket using M4 screws and washers

p. Connect the flying lead on the battery pack to the connector on the PCB assembly

q. Replace the top cover. Replace and secure the bezel

3.1 INTRODUCTION

3.1.1 This section contains information for operating the 1991/1992 as a bench instrument. It provides Front and Rear Panel Descriptions, Measurements Procedures, and Miscellaneous Operating Instructions.

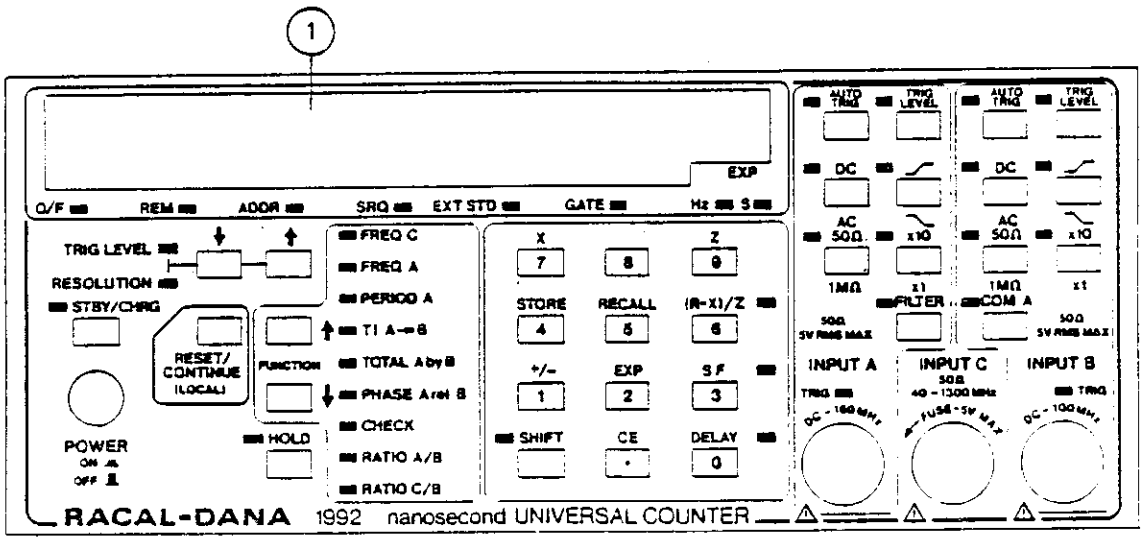
3.1.2 The instrument should be prepared for use in accordance with the instructions given in Section 2. If the instrument is being used for the first time or at a new location, ensure that the setting of the AC voltage selector is correct.

3.2 PANEL DESCRIPTIONS

3.2.1 Front Panel Features

3.2.1.1 Refer to Table 3.1 and the front-panel figures. They show and briefly describe the front-panel controls, indicators, and connectors.

Table 3.1 - Front-Panel Controls, Indicators, and Connectors

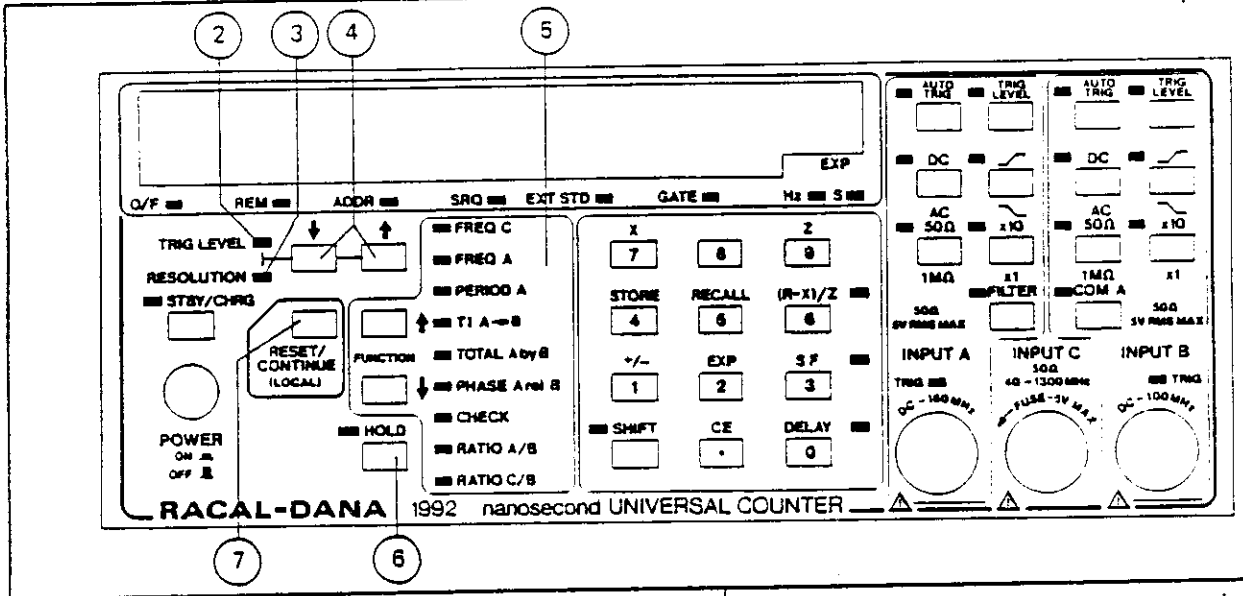


Reference	Item	Function/Description
1	Display	A 7-segment LED digital display. Used to display: - measurement results - numbers for entry into an internal store - numbers recalled from an internal store - error messages The display format uses an engineering format with 9-digit mantissa and 1-digit exponent. The exponent is normally a multiple of three

Table 3.1 - Front-Panel Controls, Indicators, and Connectors (Cont'd)

Reference	Item	Function/Description
		The exponent digit is blanked and should be assumed to be zero during the following: a. Phase measurement b. Totalize measurement with less than ten digits c. Number entries from the numeric keypad not involving an exponent
	O/F LED	Lights when the readout overflows the ninth digit of the display
	REM LED	Lights when the instrument is operating under remote control
	ADDR LED	Lights when the instrument is acting as a listener or as a talker
	SRQ LED	Lights when the instrument generates a service request
	EXT STD LED	Lights when the instrument is operating from an external frequency standard
	GATE LED	Lights while a measurement cycle is in progress
	Display Units LEDs	The Hz indicator lights for a frequency display. The s indicator lights for a time display. Neither indicator lights for a display of phase angle, ratio, total, trigger level, or a number
(2)	TRIG LEVEL Control LED	Lights when a trigger level is being displayed. The displayed trigger level can be stepped up or down using the ▲ and ▼ keys, or can be changed using the numeric keypad
(3)	RESOLUTION Control LED	Lights to show that the resolution of the display can be changed by means of the ▲ or ▼ keys

Table 3.1 - Front-Panel Controls, Indicators, and Connectors (Cont'd)



Reference	Item	Function/Description
4	Step-Up ▲ and Step-Down ▼ Keys	Used to step the display resolution or the displayed trigger-level value up or down
5	FUNCTION Keys (▲▼)	Select in succession the counter's measurement functions. The corresponding FUNCTION LED is lit. Function selection "wraps around" at both ends
6	HOLD Key	Successive operation toggles the instrument in and out of the Hold (single-shot measurement) mode. The LED lights in the Hold mode. Readings are triggered using the RESET key When the instrument is in the Manual Totalize mode (using Special Function 61), successive operation of the HOLD key will start and stop the measurement cycle
7	RESET/CONTINUE (LOCAL) Key	This key has the following three functions: RESET Clears the display and triggers a new measurement cycle when the instrument is in the measurement mode

Table 3.1 - Front-Panel Controls, Indicators, and Connectors (Cont'd)

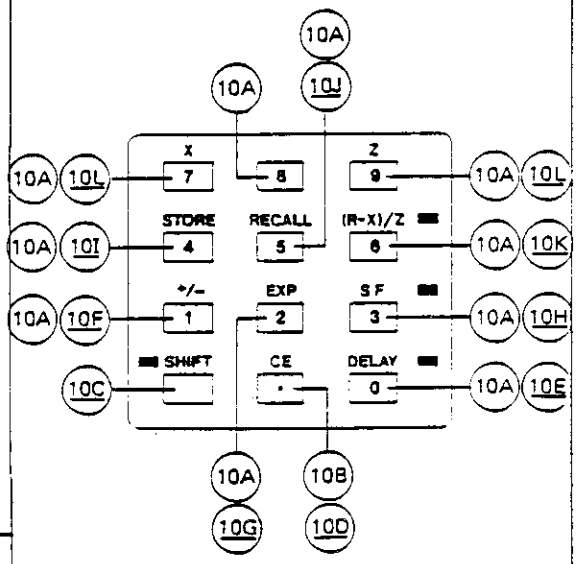
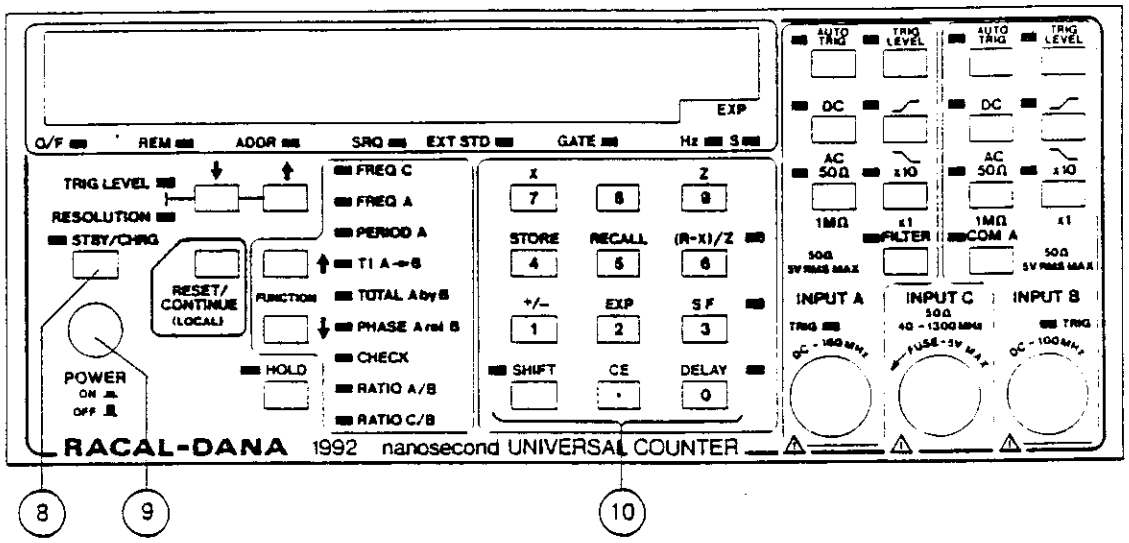
Reference	Item	Function/Description
		CONTINUE Returns the instrument to the measurement mode and triggers a measurement cycle, following the display of a number or constant recalled from store. It can also be used to clear the OP Er display LOCAL Returns the instrument to front-panel control from remote GPIB control, provided local lockout is not set
(8)	STBY/CHRG Key	Successive operation toggles the instrument in and out of the standby state. The LED lights when the instrument is in the standby state. In standby, power is supplied only to internal frequency standard and memories
(9)	POWER (ON/OFF) Button	Controls the AC power to the instrument
(10)	Data Entry Keys/LEDs	Permit data entry and user interface with the 1991/1992 other than input signal conditioning and measurement functions
	NOTE: Designators for shifted key functions are underlined	
	Unshifted Key Functions:	
(10A)	Numeric Keys (0-9)	Entry of numbers and constants for math, special functions, time-interval stop delays and trigger levels. When a numeric key is pressed, the measurement in progress is aborted and the display shows the entered number

Table 3.1 - Front-Panel Controls, Indicators, and Connectors (Cont'd)



Reference	Item	Function/Description
10B	Decimal Point (.) Key	Inserts a decimal point during numeric entry
	Shifted Key Functions:	
10C	SHIFT Key/LED	Enables any shifted key function. After pressing a shifted key function (except for STORE and RECALL), counter returns to its unshifted state with the SHIFT LED turning off
10D	CE Key	Clears current display number and entry
10E	DELAY Key/LED	Enables a TI A→B or Totalize A by B stop delay (SHIFT DELAY). Also, stores (⟨value⟩ SHIFT STORE DELAY), and recalls (SHIFT RECALL DELAY) a stored stop delay
10F	Positive/Negative (+/-) Sign Key	Toggles sign of entered number (mantissa and/or exponent) between positive (no sign displayed) and negative (sign displayed)
10G	EXP Key	Changes the data entry mode so that the next number entered is the exponent

Table 3.1 - Front-Panel Controls, Indicators, and Connectors (Cont'd)

Reference	Item	Function/Description
10H	SF Key/LED	Enables all selected special functions (SHIFT SF). Also, stores (⟨NN⟩ SHIFT STORE SF) and recalls (SHIFT RECALL SF) special functions. See Subsection 3.8 for further details
10I	STORE Key	Stores constants for math functions, time-interval delay, and special functions
10J	RECALL Key	Recalls constants for math functions, time-interval delay, and special functions
10K	(R-X)/Z Math Key/LED	Enables selection of math computation mode
10L	X/Z Keys	Store and recall math computation constants (X and Z)
11	INPUT A and B Signal Conditioning Keys/LEDs	
11A	AUTO TRIG Keys/LEDs	Toggles to select auto-trigger or manual trigger level. The LED lights when auto-trigger is selected

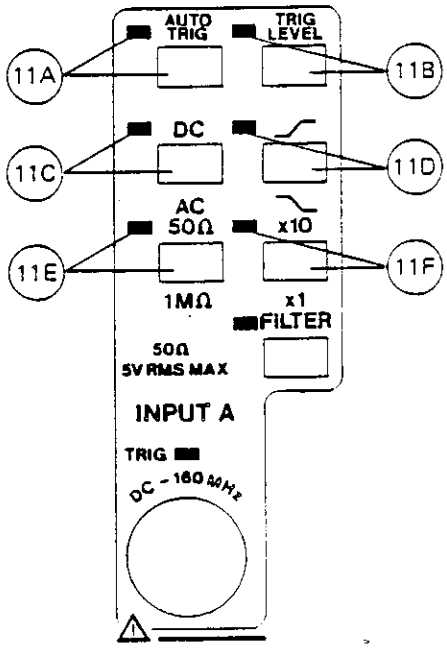
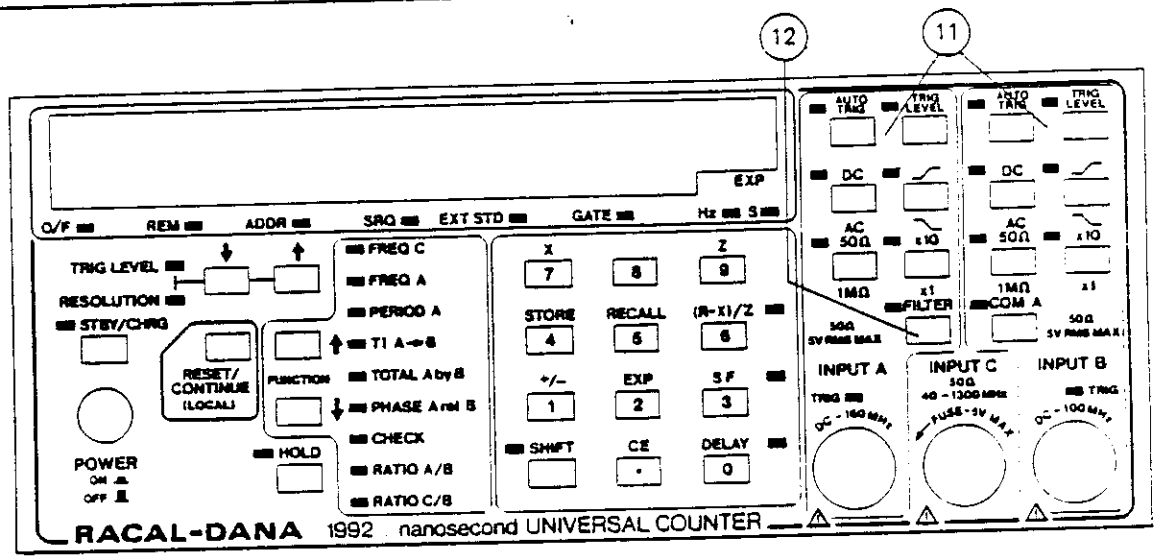


Table 3.1 - Front-Panel Controls, Indicators, and Connectors (Cont'd)

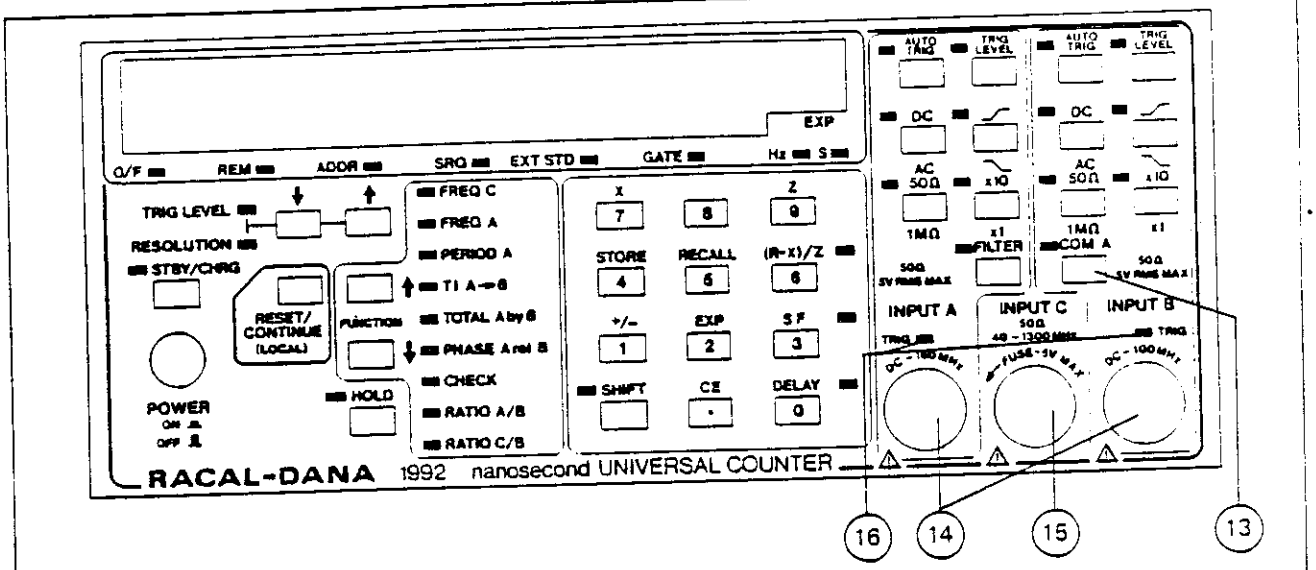


Reference	Item	Function/Description
(11B)	TRIG LEVEL Keys/LEDs	Toggles to display the trigger level in use or to enter a new trigger level. The LED flashes when the trigger level is being displayed. (The trigger-level control LED (2) will also light.)
(11C)	DC/AC Keys/LEDs	Toggles to select AC or DC coupling of the input signal. The LED lights when DC coupling is selected
(11D)	⎍/⎍ Keys/LEDs	Toggles to select the positive-going (⎍) or negative-going (⎍) edge of the input waveform for triggering The LED lights when the positive-going edge is selected
(11E)	50Ω/1MΩ Keys/LEDs	Toggles to select 50Ω or 1MΩ input impedance. The LED lights when 50Ω is selected
(11F)	x10/x1 Keys/LEDs	Toggles to select attenuation of the input signal. With x10 selected, the input is attenuated by a factor of 10. The LED lights when x10 is selected
(12)	FILTER Key/LED	Toggles to enable or disable the Channel A's input filter. LED lights when the filter is enabled

Table 3.1 - Front-Panel Controls, Indicators, and Connectors (Cont'd)

Reference	Item	Function/Description
(13)	COM A Key/LED	Toggles to connect or disconnect the signal at Channel A's input into both Channels A and B (parallel COMmon configuration) LED lights when the COM mode is selected In COM mode, Channel A's AUTO TRIG key controls both Channels A and B. Channel B's AUTO TRIG key is rendered inoperative. Channel B's AUTO TRIG LED follows the lit/unlit state of Channel A's LED Both Channels A and B adopt the same trigger level with auto-trigger level selected. Different trigger levels can be set in the two channels , however, when manual trigger level is selected Channel A's 50Ω/1MΩ, x10/x1 and DC/AC keys control both channels. Channel B's x10/x1 and DC/AC LEDs follow the lit/unlit state of Channel A's LEDs. Channel B's 50Ω/1MΩ LED continues to show the impedance of Channel B's input
(14)	INPUT(s) A and B	BNC connectors for INPUT(s) A and B. INPUT A (DC to 160 MHz) is used for all functions except Frequency C. INPUT B (DC to 100 MHz) is used with INPUT A for Time Interval, Ratio A/B, Totalize, and Phase measurement. INPUT B is used with INPUT C for Ratio C/B. Special Function 21 internally exchanges INPUTs A and B (providing, e.g., PERIOD B, etc. measurement capability)

Table 3.1 - Front-Panel Controls, Indicators, and Connectors (Cont'd)



Reference	Item	Function/Description
(15)	INPUT C (Model 1992 only)	BNC connector for high-frequency INPUT C (40 MHz - 1.3 GHz). INPUT C is used with INPUT B for Ratio C/B. Special Function 21 provides Ratio C/A capability. Protection against excessive signal levels (> 5V rms) is provided by a fuse mounted in the input socket
(16)	TRIG LEDs/Inputs A and B	Tri-state LEDs indicating the counter's trigger status: a. **LED On** - trigger level too low or input signal level held in a high state b. **LED Flashing** - channel being triggered c. **LED Off** - trigger level too high or input signal level held in a low state

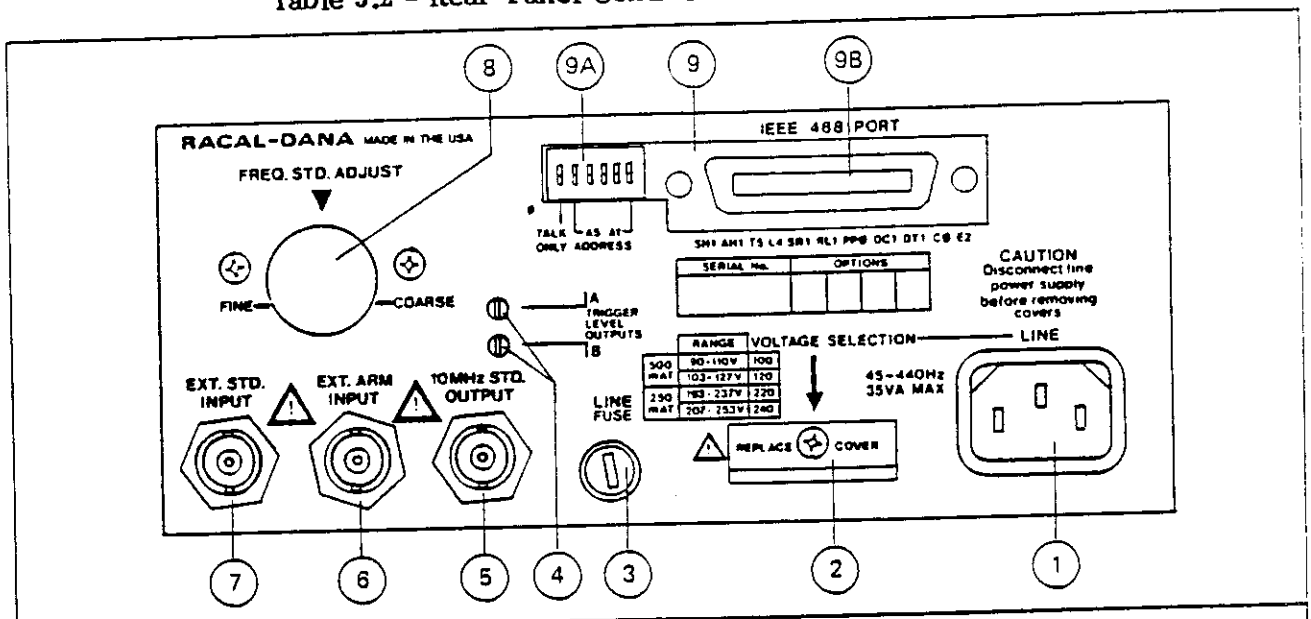
3.2.2 Rear Panel Features

3.2.2.1 Refer to Table 3.2 and figure at top. They show and briefly describe the rear-panel controls and connectors.

Table 3.2 - Rear-Panel Controls and Connectors

Reference	Item	Function/Description
(1)	AC Power Input Socket	Standard connector for the AC power supply. A RFI filter is incorporated on the instrument motherboard
(2)	VOLTAGE SELECTION Window	Line voltage selection is changed by repositioning a small printed circuit card inside the instrument. The selected voltage can be viewed through the small open window. See Subsection 2.4.2 for line voltage selection procedure
(3)	LINE FUSE	A 1/4 in x 1-1/4 in glass cartridge Slow-Blow fuse. Line fuse ratings for available line voltages are shown on the rear panel to the right of the fuse receptacle. See also Subsection 2.4.3 in this manual
(4)	TRIGGER LEVEL OUTPUTS (A, B)	Outputs for Inputs A and B trigger levels. Voltage range at both output pins is ± 5.1V, regardless of attenuation
	NOTE: Connectors (5) through (7) are BNCs	
(5)	10 MHz STD. OUTPUT Connector	Output for 10 MHz signal from the internal reference standard
(6)	EXT. ARM INPUT Connector	Input for accepting external arming/gating control signals
(7)	EXT. STD. INPUT Connector	Input for connecting an external frequency standard. The instrument will operate from the external frequency standard whenever a signal of suitable frequency and amplitude is applied. The frequency required is 10 MHz
(8)	FREQ. STD. ADJUST	Aperture providing access for adjusting the internal frequency standard

Table 3.2 - Rear-Panel Controls and Connectors (Cont'd)



Reference	Item	Function/Description
(9)	GPIB Option	
(9A)	GPIB Address Switches	Switches A1 to A5 define the listen and talk addresses for GPIB operation in the addressed mode The 2-digit GPIB address can be recalled to display using key sequence SHIFT RECALL RESET
(9B)	GPIB Connector	An IEEE-488-1978 standard connector

3.3 OPERATING PROCEDURES

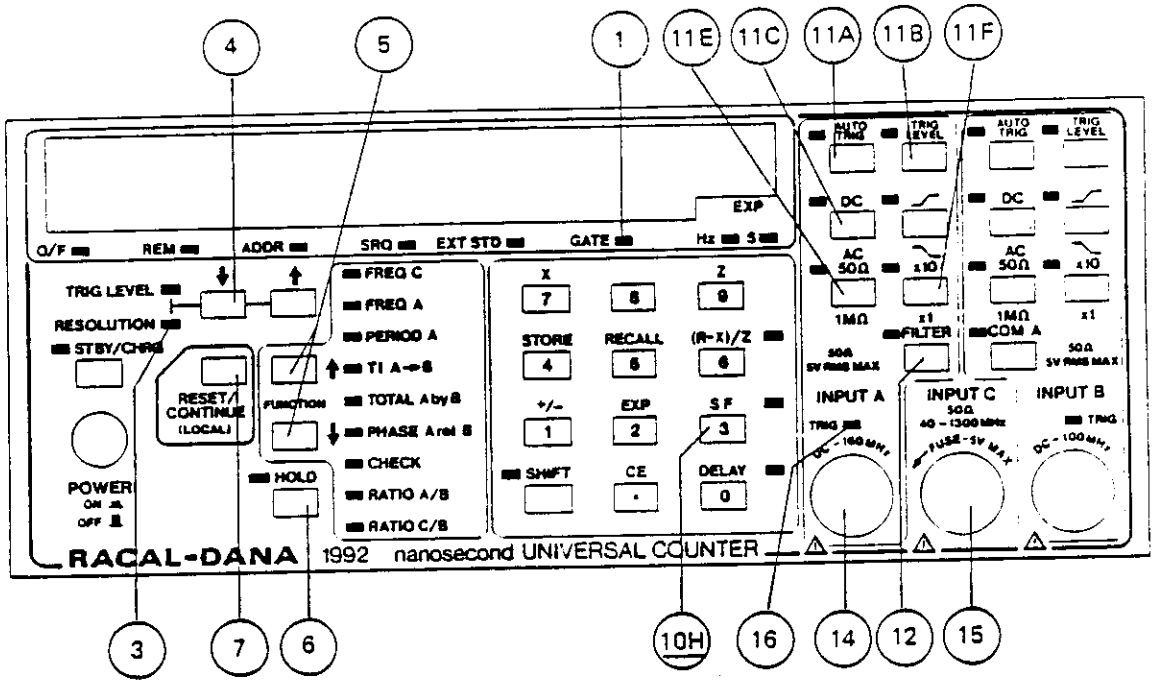
3.3.1 Measurement Functions

3.3.1.1 Tables 3.3 - 3.9 with figures describe the basic bench functions of the 1991/199

NOTE:

Review as required Table 3.1, References (14) and (15), for use of Inputs A, B, and C, including Special Function 21 permitting interchange of Inputs A and B. See also Subsection 3.8 and Table 3.12 for special functions.

Table 3.3 - Frequency Measurement



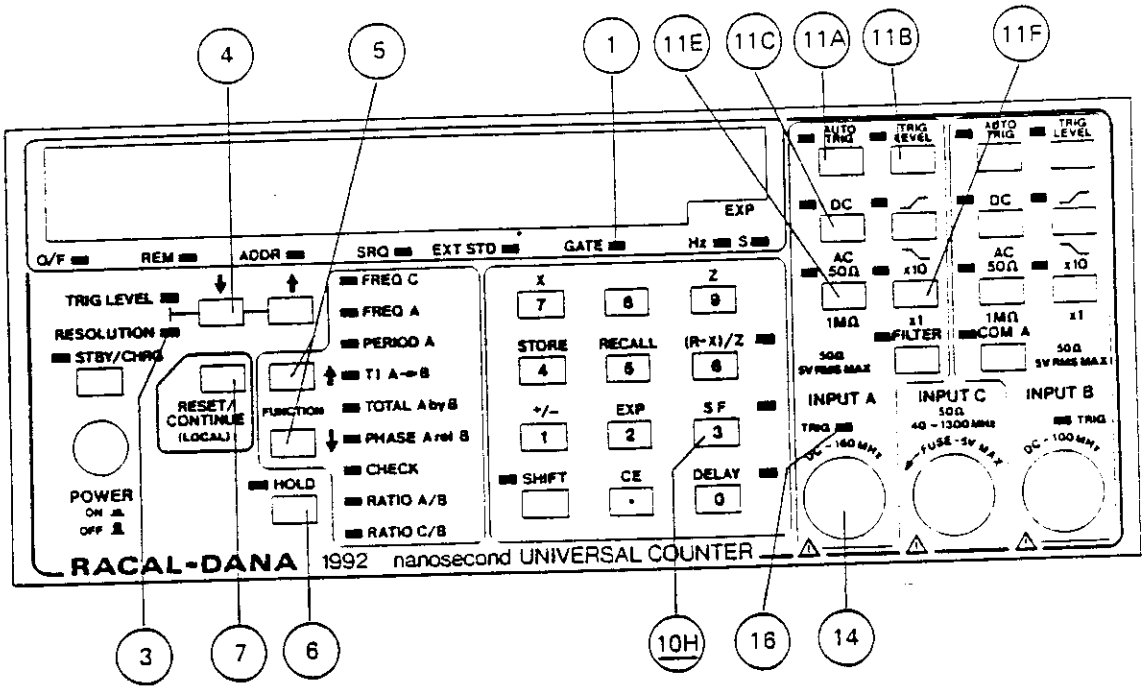
1. Turn power on.
2. Select FREQ A or FREQ C (Model 1992 only) using FUNCTION keys (5).
3. If FREQ A is selected, set the AC/DC coupling (11C), input impedance (11E), and attenuator (11F) as required.

CAUTION

Ensure that the input signal does not exceed the damage levels specified in Table 1.1 of this manual.

4. Connect the measurement signal to INPUT A (DC to 160 MHz) (14) or INPUT C (40 MHz to 1.3 GHz) (15).
5. If FREQ A is selected, select AUTO-TRIG (11A), or set the manual trigger level (11B) to the required value. Check that Input A TRIG LED (16) flashes.
6. Select the required display resolution (3) (4).
7. If a frequency below 50 kHz is to be measured in the presence of noise, select the filter (12).
8. If external arming is to be used, connect the arming signal and enter the required special function number. Enable the special functions (10H). Refer to Subsection 3.8. for special function numbers and procedures.
9. Verify that the GATE LED (1) flashes on during gating.
10. If single-shot operation is required, select HOLD (6) and press the RESET key (7) to trigger each new measurement.

Table 3.4 - Period Measurement



1. Turn power on.

2. Select PERIOD A using FUNCTION keys (5).

3. Set the AC/DC coupling (11C), input impedance (11E), and attenuator (11F) for Channel A, as required.

CAUTION

Ensure that the input signal does not exceed the damage levels specified in Table 1.1 of this manual.

4. Connect the measurement signal to INPUT A (14).

5. Select AUTO-TRIG (11A) or set the manual trigger level (11B) to the required value. Check that Input A TRIG LED (16) flashes.

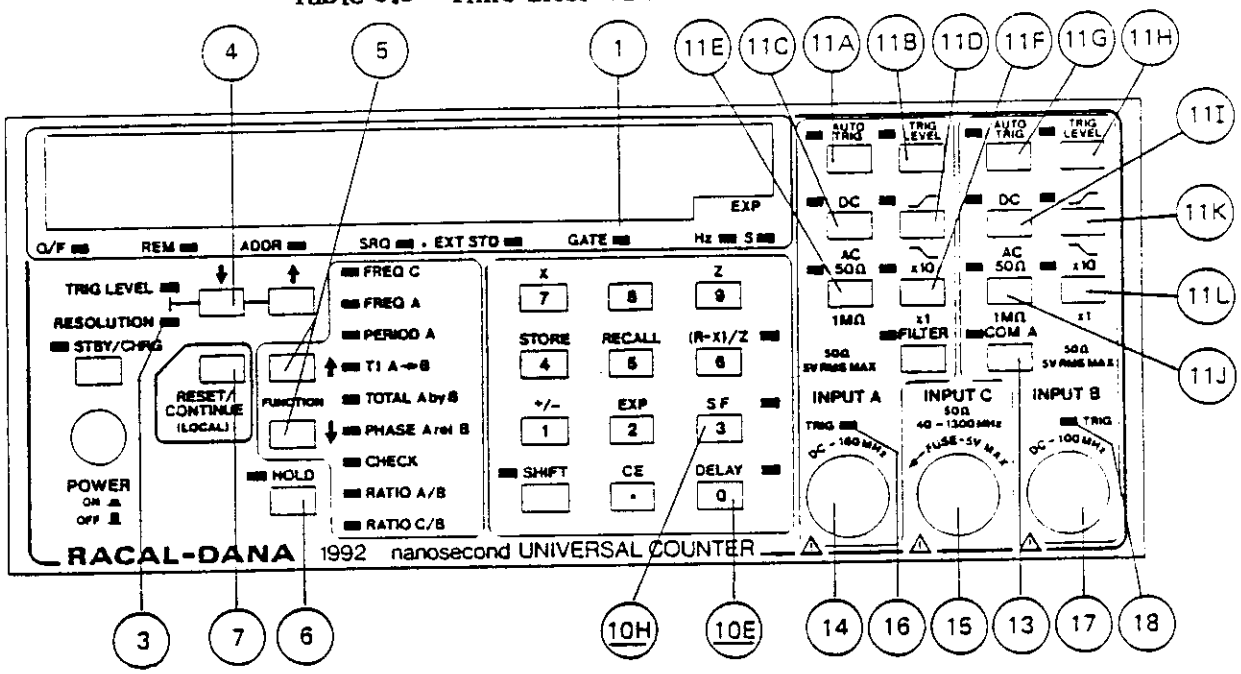
6. Select the required display resolution (3) (4).

7. If external arming is to be used, connect the arming signal and enter the required special function number. Enable the special functions (10H). Refer to Subsection 3.8 for special function numbers and procedures.

8. Verify that the GATE LED (1) flashes on during gating.

9. If single-shot operation is required, select HOLD (6) and press the RESET key (7) to trigger each new measurement.

Table 3.5 - Time Interval Measurement



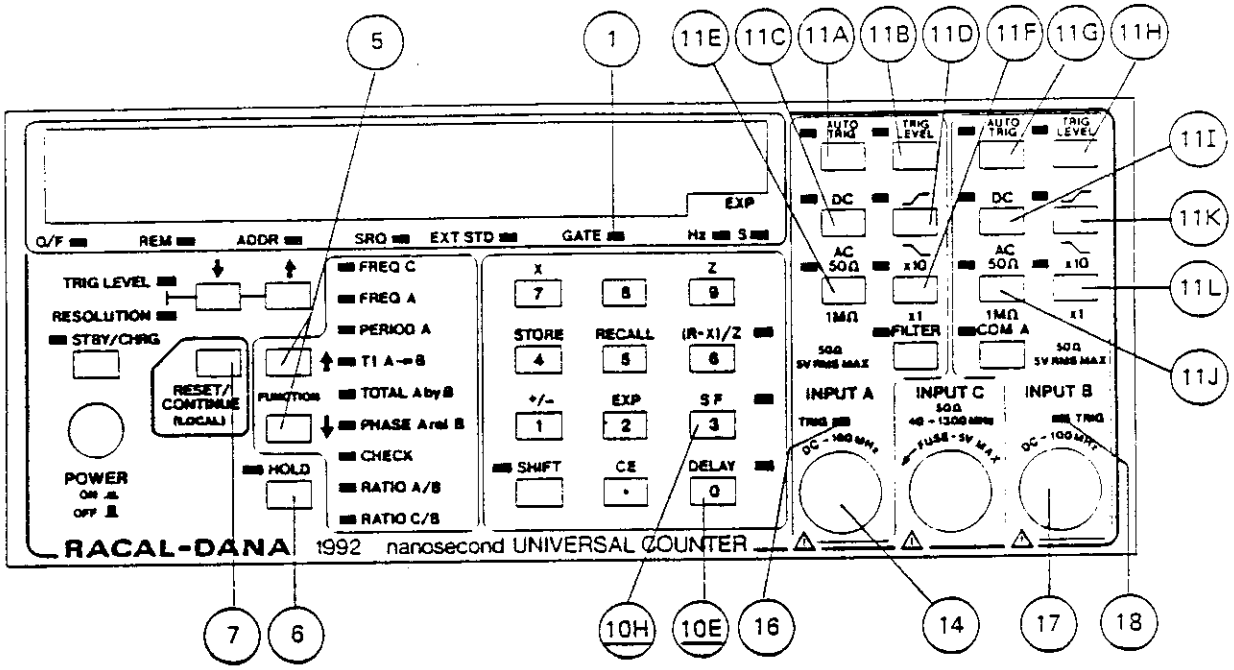
1. Turn power on.
2. Select T.I. A➔B using FUNCTION keys (5).
3. Set the AC/DC coupling (11C) / (11I), input impedance (11E) / (11J), attenuator (11F) / (11L), and slope (11D) / (11K), as required. If the start and stop signals are from the **same source**, select COM A (13).

CAUTION

Ensure that the input signals do not exceed the damage levels specified in Table 1.1 of this manual.

4. Connect the start signal to INPUT A (14). If a separate source for the stop signal is used, connect the stop signal to INPUT B (17) and set the associated input controls as needed.
5. Select AUTO-TRIG (11A) / (11G) or set the manual trigger levels (11B) / (11H) to the required values. Check that Inputs A and B TRIG LEDs (16) and (18) flash, respectively.
6. Select the required display resolution (3)(4).
7. If internal delayed arming of the stop circuit is required, enter the delay into memory and enable the delay (10E).
8. If external arming is to be used, connect the the arming signal and enter the required special function number. Enable the special functions (10H). Refer to Subsection 3.8 for special function numbers and procedures.
9. Verify that the GATE LED (1) flashes on during gating.
10. If single-shot operation is required, select HOLD (6) and press the RESET key (7) to trigger each new measurement.

Table 3.6 - Total A by B Measurement



1. Turn power on.
2. Select TOTAL A by B using FUNCTION keys (5).
3. Set the AC/DC coupling (11C) / (11I), input impedance (11E) / (11J), attenuator (11F) / (11L), and slope (11D) / (11K) as required for both Channels A and B.

NOTE:

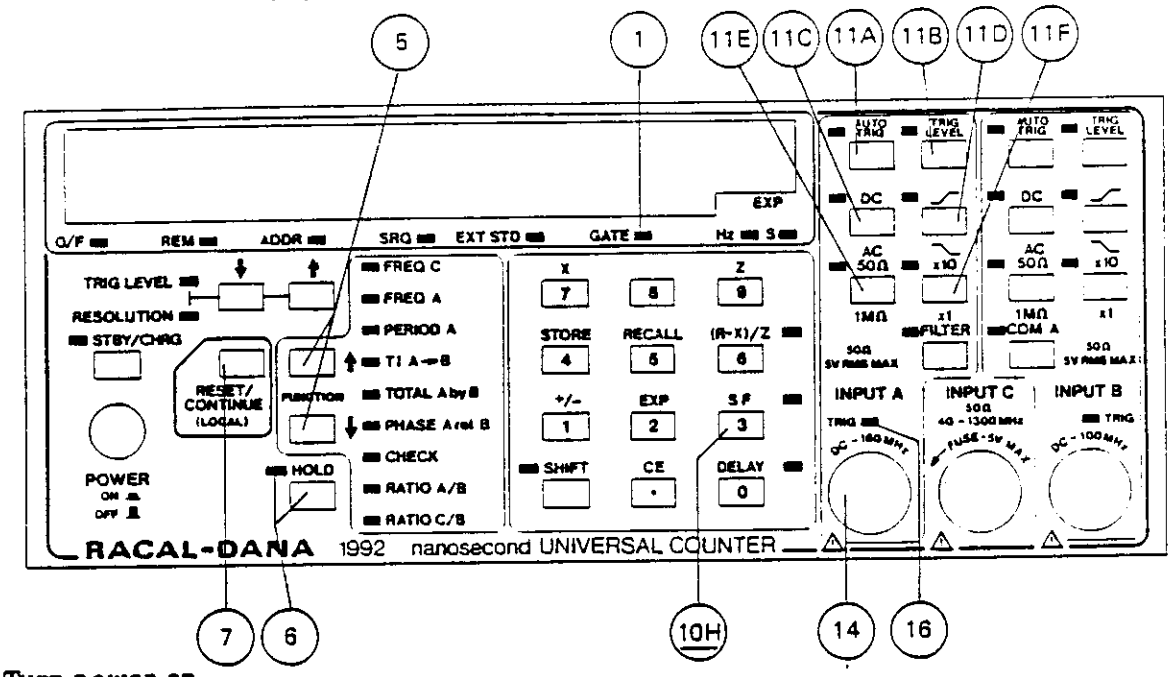
The INPUT A slope key selects the slope of the events which are counted. The gate time, however, starts on the slope of the Channel B signal selected by the INPUT B slope key and stops on the opposite slope.

CAUTION

Ensure that the signal levels do not exceed the damage levels specified in Table 1.1 of this manual.

4. Connect the signal to be totalized to INPUT A (14) and the control signal to INPUT B (17).
5. Select AUTO-TRIG (11A) / (11G) or set the manual trigger levels (11B) / (11H) to the required values. Check that Inputs A and B TRIG LEDS (16) and (18) flash, respectively.
6. If internal delayed arming of the stop circuit is to be used, enter the delay into memory and enable the delay (10E).
7. If external arming is to be used, connect the arming signal and enter the required special function number. Enable special functions (10H). Refer to Subsection 3.8 for special function numbers and procedures.
8. Verify that the GATE LED (1) flashes on when Channel B signal is either high or low.
9. If single-shot operation is required, select HOLD (6) and press the RESET key (7) to trigger each new measurement.

Table 3.7 - Manual Totalize Measurement



1. Turn power on.

2. Select TOTAL A by B using FUNCTION keys (5).

3. Set the AC/DC coupling (11C), input impedance (11E), attenuator (11F), and slope (11D) of Channel A as required.

4. Enter Special Function number 61 and enable special functions (10H). The HOLD LED (6) will light.

CAUTION

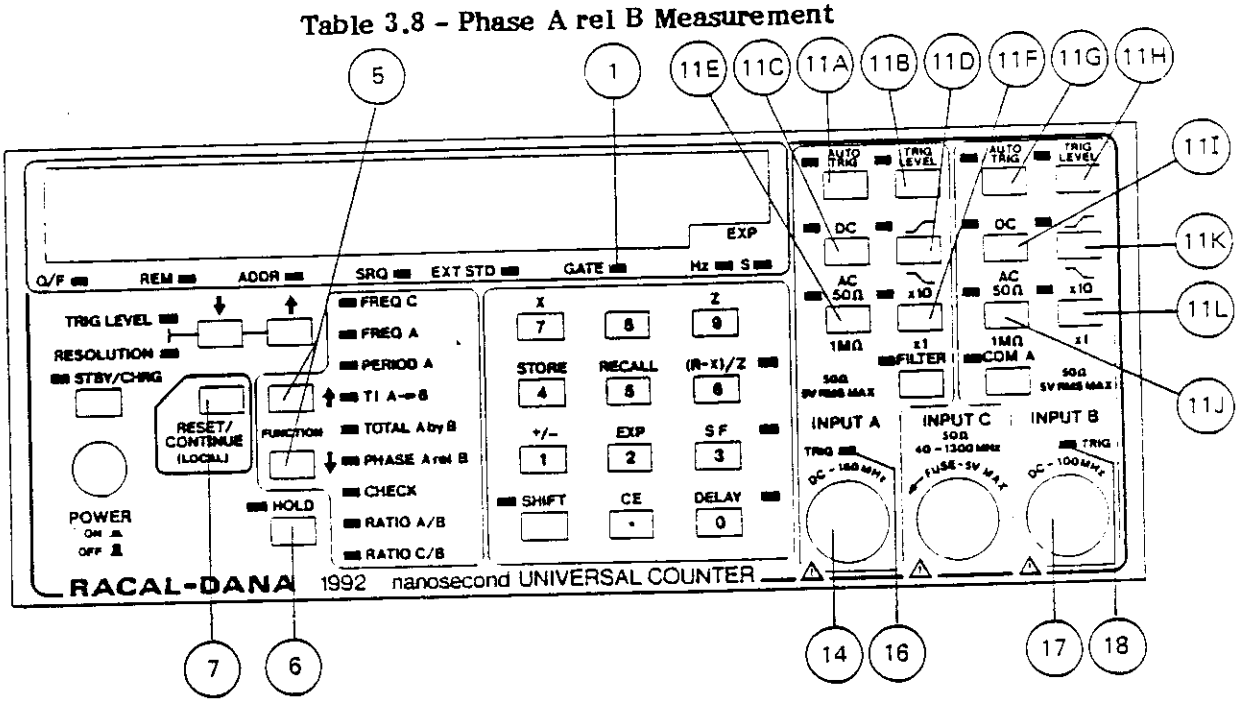
Ensure that the input signal level does not exceed the damage levels specified in Table 1.1 of this manual.

5. Connect the signal to be totalized to INPUT A (14).

6. Select AUTO-TRIG (11A) or set the manual trigger level (11B) to the required value. Check that Input A TRIG LED (16) flashes.

7. Start and stop a measurement using the HOLD key (6). The HOLD LED will turn off and the GATE LED (1) will light during gating. The displayed result is cumulative over successive measurement cycles. If required, use the RESET key (7) to clear the display after a measurement cycle.

Table 3.8 - Phase A rel B Measurement



1. Turn power on.
2. Select PHASE A rel B using FUNCTION keys (5).
3. Set the AC/DC coupling (11C) / (11I), input impedance (11E) / (11J), attenuator (11F) / (11L), and slope (11D) / (11K) as required for INPUTs A and B (14) and (17), respectively. Selected slopes for input signals for Channels A and B should be the same.

CAUTION

Ensure that the input signals do not exceed the damage levels specified in Table 1.1 of this manual.

4. Connect the signals to be compared to INPUT A and INPUT B (14) and (17).

NOTE:

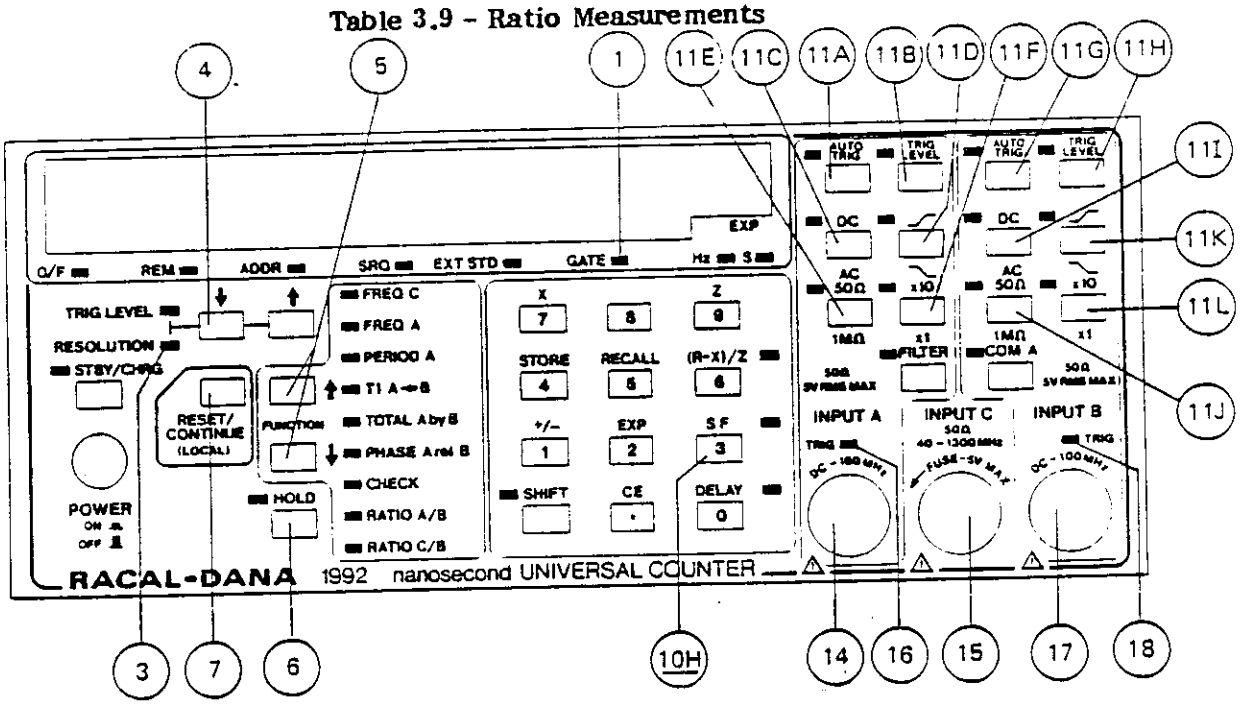
For maximum accuracy, connect the larger and cleaner signal to INPUT A.

5. Select AUTO-TRIG (11A) / (11G) or set the manual trigger levels (11B) / (11H) to the required values. Check that Inputs A and B TRIG LEDs (16) and (18) flash, respectively.
6. Verify that the GATE LED (1) flashes on during gating.
7. If single-shot operation is required, select HOLD (6) and press the RESET key (7) to trigger each new measurement.

NOTE:

A phase measurement is always positive, representing the angle by which Input A's signal leads that of Input B. The signals for phase measurement must be continuous and have the same frequency.

Table 3.9 - Ratio Measurements



1. Turn power on.

2. Select RATIO A/B or RATIO C/B (Model 1992 only) using FUNCTION keys (5).

3. Set the AC/DC coupling (11C) / (11I), input impedance (11E) / (11J), attenuator (11F) / (11L), and slope (11D) / (11K), as required, for INPUTs A (14) and B (17) and INPUT C (15).

CAUTION

Ensure that the input signals do not exceed the damage levels specified in Table 1.1 of this manual.

4. Connect one of the signals to INPUT B (17) and the other to INPUT A (14) or C (15). The lower frequency signal should be connected to INPUT B (14).

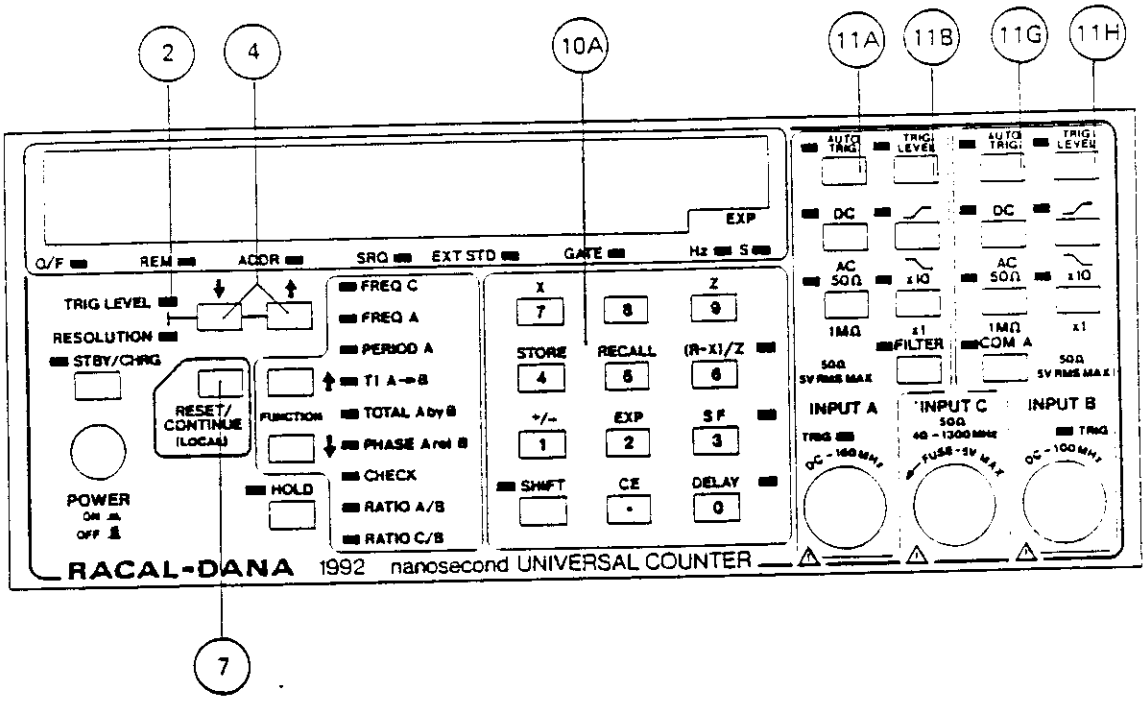
5. Select AUTO-TRIG (11A) / (11G) or set the manual trigger levels (11B) / (11H) to the required values. Check that Inputs A and B TRIG LEDs (16) and (18) flash, respectively.

6. Select the required display resolution (3)(4).

7. If external arming is to be used, connect the the arming signal and enter the required special function number. Enable the special functions (10H). Refer to Subsection 3.8 for special function numbers and procedures.

8. Verify that the GATE LED (1) flashes on during gating.

9. If single-shot operation is required, select HOLD (6) and press the RESET key (7).



3.4 TRIGGER LEVEL

3.4.1 Trigger Level Modes

3.4.1.1 The trigger level may be set by the operator (manual trigger level) or determined automatically by the instrument (auto-trigger level). The auto-trigger level is the arithmetic mean of the positive and negative-peak values of the input signal. The two modes are enabled alternately by successive operations of the AUTO TRIG key (11A) / (11G). The LED lights when the auto-trigger mode is selected.

3.4.2 Displaying and Setting the Manual Trigger Level

3.4.2.1 Perform the following procedure:

a. Select the manual trigger mode using the AUTO TRIG key (11A) / (11G)

b. Display the trigger level by pressing the TRIG LEVEL key (11B) / (11H). The associated LED will flash and the trigger level control LED (2) will light

c. To change the trigger level:

1. Enter the required value, using the numeric keypad (10A)

NOTE:

Up to this point, the instrument can be returned to the measurement mode with the trigger level unchanged by pressing the CONTINUE key (7)

or

2. Using the step up ▲ or step down ▼ control key (4). The desired trigger level can be entered in 20 mV steps

d. Return the instrument to the measurement mode by pressing the TRIG LEVEL key (11B) / (11H). The TRIG LEVEL LED and the trigger level control LED (2) will extinguish

NOTE:

There is only one trigger level store for each channel. Use of the auto-trigger mode will result in the manual trigger level being overwritten.

3.4.3 Displaying the Auto-Trigger Level

3.4.3.1 Perform the following procedure:

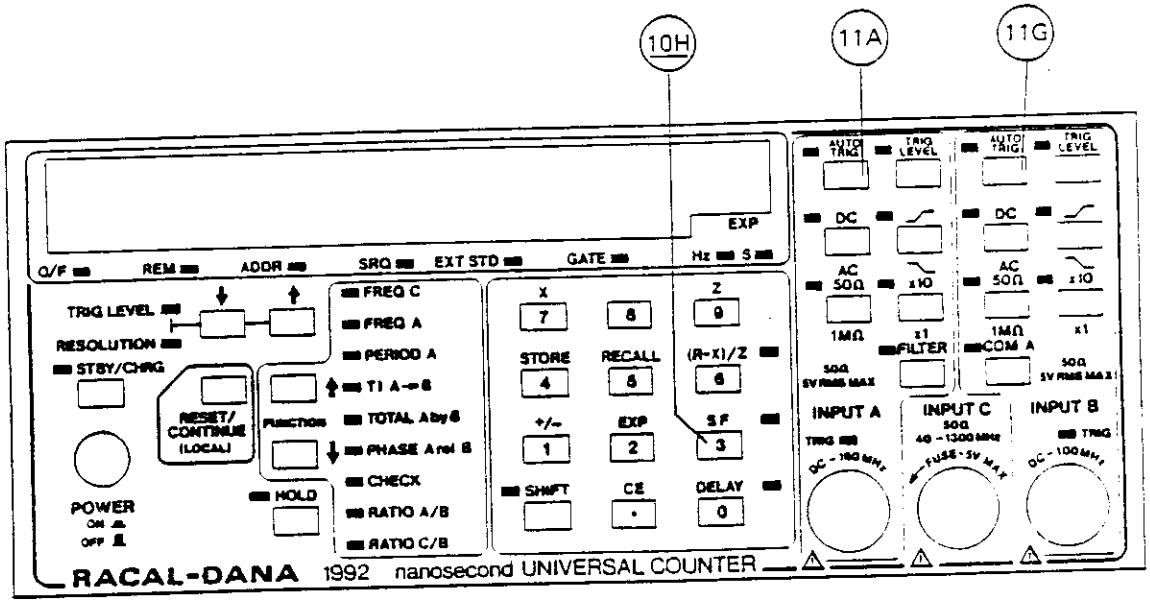
a. Select the auto-trigger mode, using the AUTO TRIG key (11A) / (11G)

b. Display the auto-trigger level by pressing the TRIG LEVEL key (11B) / (11H). The associated LED will flash and the trigger level control LED (2) will light

NOTE:

Any attempt to make a numeric entry while the auto-trigger level is being displayed will cause the OP Er (Operator Error) message to be displayed.

c. Return the instrument to the measurement mode by pressing the TRIG LEVEL key (11B) / (11H) or the CONTINUE key (7). The TRIG LEVEL LED and the trigger level control LED (2) will extinguish



3.4.4 Single-Shot Auto-Trigger Level

3.4.4.1 The auto-trigger level is normally measured continuously and varies if the peak levels of the signal change. A single-shot measurement of auto-trigger level can be made using Special Function 31. This value remains stored as a manual trigger level until:

a. Another single-shot measurement is made, or

b. A new manual trigger level is entered

3.4.4.2 Complete the following to make a single-shot measurement of auto-trigger level:

a. Enter Special Function number 31 into the special function register (10H)

b. Enable the special functions (10H)

c. Select AUTO TRIG (11A) / (11G). The associated LED lights while the level is calculated and stored, and then extinguishes

3.4.4.3 Further single-shot measurements are made by selecting AUTO TRIG (11A) / (11G) with Special Function 31 active.

3.4.5 Automatic Attenuation Setting

3.4.5.1 When operating in the auto-trigger mode, automatic switching of the x10 attenuator occurs as follows:

a. The attenuator is switched in if the peak-to-peak value of the measured signal exceeds 5.1V or if either peak is outside the ±5.1V range

b. The attenuator is switched out if the peak-to-peak value of the measured signal is less than 4.6V and both peaks are within the ±4.6V range

3.5 DISPLAY RESOLUTION

3.5.1 General Information

3.5.1.1 For all measurement functions except TOTAL A by B, the resolution refers to the number of zeros displayed when no signal is applied at the input. The resolution can be set to display 3 to 10 digits. (For a resolution of 10, the most significant digit overflows the display.) A 10% overrange of the display is permitted without a change of range. Because of this, an additional digit with a value of 1 may appear at the more significant end of the display when measurements are made.

3.5.1.2 With some measurement functions, the number of digits appearing may be less than the selected resolution to ensure they are rounded to meaningful values.

3.5.1.3 When ratio measurements are made, no more than eight digits are displayed, regardless of the resolution selected.

3.5.1.4 For the TOTAL A by B, the display shows the true total of events counted from 1 to 999 999 999. For higher totals, the exponent is used.

3.5.1.5 For the PHASE A rel B, up to four digits may be displayed for frequencies up to 1 MHz and up to three digits for higher frequencies. Leading zeros are suppressed. For frequencies above 10 MHz, the resolution of the display is 10°, and a place-holding zero is displayed as the least-significant digit.

3.5.2 Setting the Display Resolution

3.5.2.1 Whenever the resolution control LED is lit, the resolution can be changed using the step-up ▲ and step-down ▼ keys. To step up from nine to ten digits, hold the step-up key down for approximately two seconds.

3.5.3 Resolution with External Stop Circuit Arming

3.5.3.1 When external arming of the stop circuit is used, the minimum display resolution is governed by the arming period as shown in Table 3.10.

Table 3.10 - Resolution with External Arming

Arming Period	Minimum Resolution
Less than 100 µs	4
100 µs to 1 ms	5
1 ms to 10 ms	6
10 ms to 100 ms	7
100 ms to 1s	8
1s to 10s	9

3.6 GATE TIME

3.6.1 For frequency, period, and ratio measurements, the gate time is related to the selected resolution selected as shown in Table 3.11.

Table 3.11 - Resolution and Gate Time

Resolution	Gate Time
10 (9 digits + overflow)	10s
9	1s
8	100 ms (see NOTE 2)
7	10 ms
6	1 ms
5	1 ms (see NOTE 3)
4	1 ms
3	1 ms

NOTE 1:

The gate times shown in the above table are nominal. Due to the use of the reciprocatic counting technique, the gate time may be extended by:

a. Up to one period of the input signal on FREQ B and RATIO A/B

b. Up to two periods of the input signal on FREQ A and PERIOD A

c. Up to 64 periods of the input signal on FREQ C and RATIO C/B

NOTE 2:

At power-on, a display resolution of 8 is selected.

NOTE 3:

Measurements are averaged when resolutions of 3, 4, or 5 are selected.

3.6.2 For PHASE A rel B, the gate time depends upon the signal frequency. The gate time is approximately 25 ms for frequencies above 200 Hz, but is increased at lower frequencies.

3.7 STOP CIRCUIT DELAY (HOLD OFF)

3.7.1 Use of the Delay

3.7.1.1 The stop circuit can be delayed when T.I. A → B or TOTAL A by B is selected. The required delay is entered into an internal store by the operator. The delay function can then be enabled and disabled as required. At power-up, the delay is set to 204.8 us (minimum delay).

3.7.1.2 The delay can be used to prevent the stop circuit from being triggered prematurely by spurious signals such as those resulting from relay contact bounce. The principle of stop circuit delay is shown in Figure 3.1.

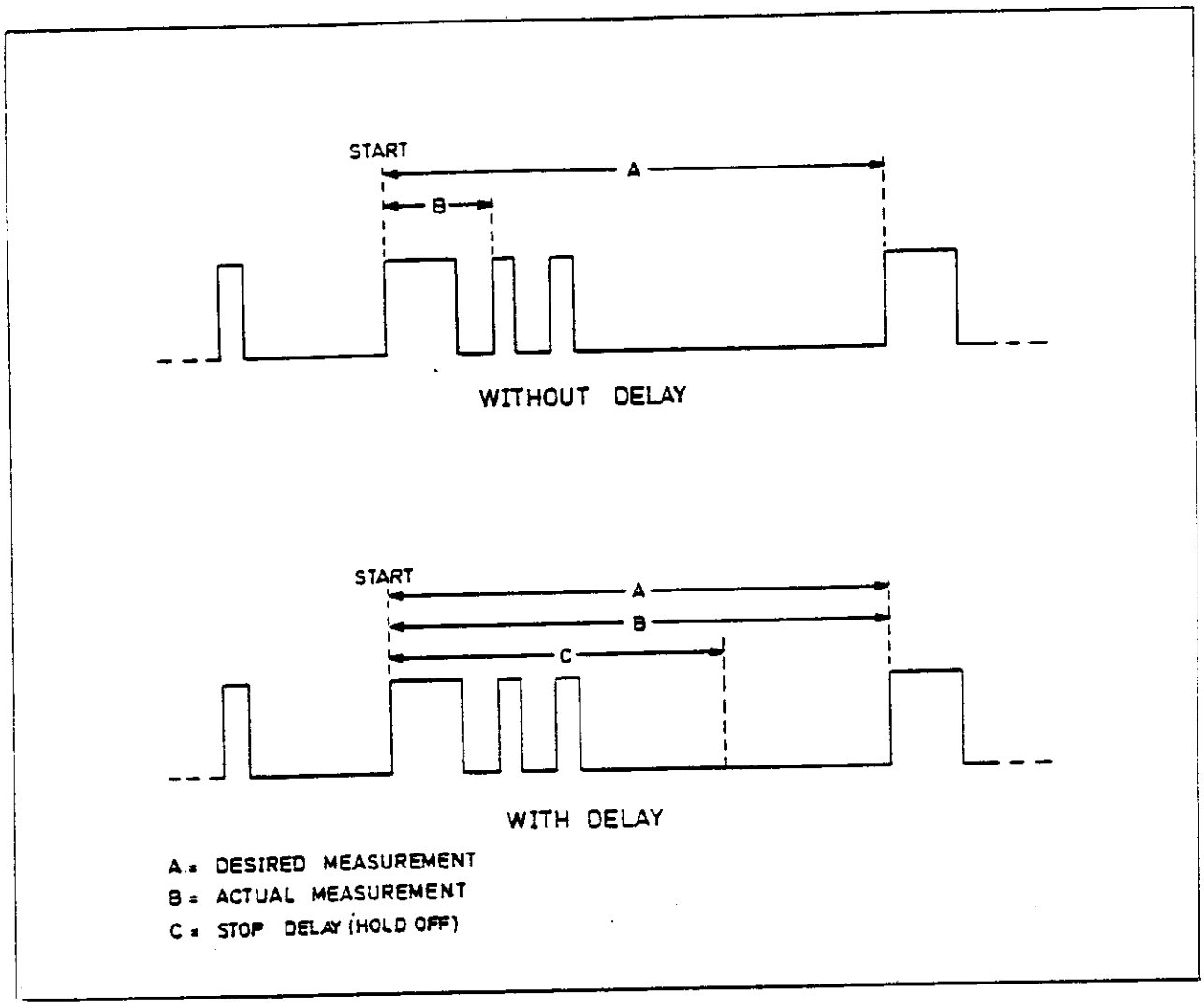


Figure 3.1 - Use of Stop Circuit Delay

3.7.2 Displaying the Delay

3.7.2.1 The value of the delay being stored can be displayed by pressing

[SHIFT] [RECALL] [DELAY]

3.7.3 Changing the Delay

3.7.3.1 A new delay value is entered into its store by using the numeric keypad. Employ either direct decimal or exponential format. For example, a delay of 305 µs may be entered using one of the following key sequences:

[.] [0] [0] [0] [3] [0] [5] [SHIFT] [STORE] [DELAY]

or [3] [0] [5] [SHIFT] [EXP] [6] [SHIFT] [+/-] [SHIFT] [STORE] [DELAY]

The instrument returns to the measurement mode automatically once the new delay value is stored.

3.7.3.2 The value of the delay entered is rounded to the nearest 25.6 μs before it is stored. The permitted range of delay is from 204.8 μs to 800 ms. Attempted entry of an out-of-range value will result in the display of OP Er. The number in the delay store is retained when the instrument is switched to standby.

3.7.4 Enabling and Disabling the Delay

3.7.4.1 The stop delay is enabled and disabled by means of the sequence

SHIFT DELAY

The DELAY LED lights when the delay is enabled.

3.8 SPECIAL FUNCTIONS

3.8.1 Special Function Numbering

3.8.1.1 The special functions provided for operator use are listed in Table 3.12. Each special function is defined by a two-digit number.

3.8.2 Special Function Register

3.8.2.1 One special function from each decade is entered into a special function register. Only the second digit is stored: the decade is indicated by the position of the digit in the register. The default state is with 0 entered in each position. The contents of the register can be displayed by pressing:

SHIFT RECALL SF

A typical display is illustrated in Figure 3.2.

Table 3.12 - Special Functions

Function Number	Function			
		Start	Stop	
10	Arming	Internal	Internal	
11		External +ve	Internal	
12		External -ve	Internal	
13		Internal	External +ve	
14		Internal	External -ve	
15		External +ve	External +ve	
16		External +ve	External -ve	
17		External -ve	External +ve	
18		External -ve	External -ve	
20	Normal Operation			
21	Channel A and B interchanged (see NOTE 1)			
30	Continuous measurement of auto-trigger level			
31	Single-shot measurement of auto-trigger level			
40	Select elapsed time between displayed measurement cycles	150 ms	between displays	See NOTE 2
41		0	between displays	
42		1s	between displays	
43		10s	between displays	
44		300s	between displays	
50	Value displayed by operation of TRIG LEVEL	Trigger level		
51		Signal positive peak		
52		Signal negative peak		
60	Measurement made with TOTAL A by B selected	Normal TOTAL A by B		
61		Manual Totalize		
70	Function with CHECK selected	10 MHz check		
71		LED check		
72-76	Reserved for diagnostic testing			
77	Channel A relay check			
78	Channel B relay check			

NOTE 1:

Special Function 21 permits FREQ B, PERIOD B, T.I. B→A, TOTAL B by A, and Phase B rel A. For these functions:

a. FREQ B is specified to 100 MHz only
b. PERIOD B is specified down to 10 ns
c. TOTAL B by A operates for one complete cycle of the Channel A signal. The stop circuit delay is available on Channel A

NOTE 2:

Special Functions 40, 42, 43, and 44 are only available when in local control. Special Function 41 is selected automatically when in remote control.

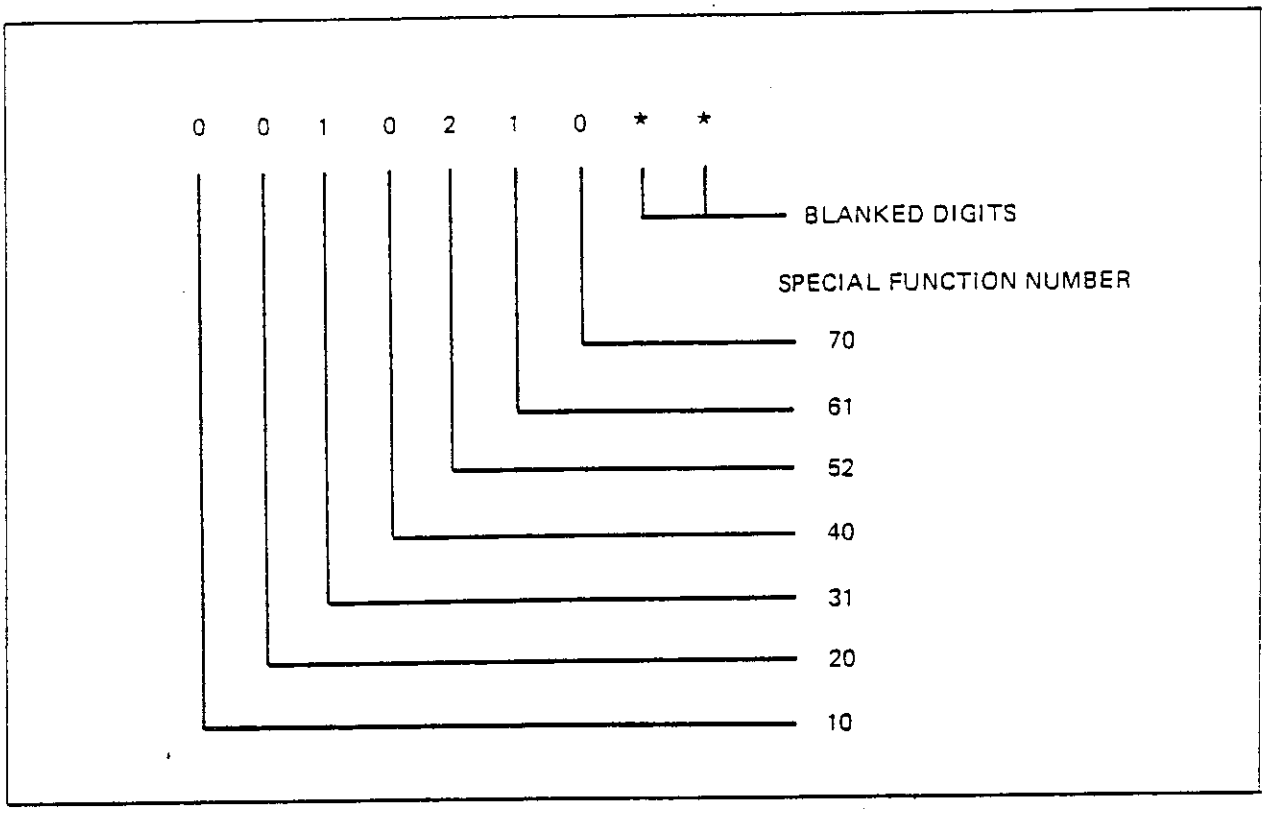


Figure 3.2 - Special Function Register Display

3.8.3 Setting the Special Function Register

3.8.3.1 Before a special function can be used, its unique number must first be entered into the special function register. Use key sequence:

[N] [N] [SHIFT] [STORE] [SF]

where NN is the special function number to be stored. The digits enter the display as the keys are pressed. The instrument returns to the measurement mode automatically once the special function number is stored.

3.8.3.2 When a special function number is stored, it overwrites the number stored in the same decade. To remove a number from the register, another special function number from the same decade must be stored.

3.8.3.3 The numbers stored in the register are retained while the instrument is in the standby mode.

3.8.4 Enabling and Disabling the Special Functions

3.8.4.1 The default state corresponds to the default state of the special function register, i.e., with Special Functions 10, 20, 30, 40, 50, 60, and 70 enabled. Special functions whose numbers are entered in the special function register are enabled and disabled using the following key sequence:

[SHIFT] [SF]

The SF LED lights when special functions are enabled.

NOTE:

A special function entered into its register while the special functions are enabled will be enabled immediately.

3.9 ERROR CODES

3.9.1 The instrument is able to detect a number of error states which are indicated on the display. Table 3.13 list the meanings of the various error codes.

Table 3.13 - Error Codes

Display	Error Description
Er 01	Phase measurement attempted on signals of different frequencies
Er 02	Measurement result too large for the display
Er 03	Overflow of internal counters
OP Er	Error in numerical entry
Er 50	Incorrect result obtained when in Check mode
Er 51	Relay or amplifier failure — Channel A — x10/x1
Er 52	Relay or amplifier failure — Channel A — 50Ω/1 MΩ
Er 53	Relay or amplifier failure — Channel A — DC/AC
Er 54	Relay or amplifier failure — Channel A — FILTER
Er 55	Relay or amplifier failure — COM A
Er 56	Relay or amplifier failure — Channel B — x10/x1
Er 57	Relay or amplifier failure — Channel B — 50Ω/1 MΩ
Er 58	Relay or amplifier failure — Channel B — DC/AC
Er 60	Microprocessor paging fault — During power-up self check
Er 61	Microprocessor RAM fault — During power-up self check

NOTE:

Error codes Er 51 to Er 55 will only be generated with Special Function 77 active. Error codes Er 56 to Er 58 will only be generated with Special Function 78 active.

3.9.2 Clearing the Error Codes

3.9.2.1 Error code Er 01 is cleared by:

a. Making a phase measurement on signals of equal frequency

b. Selecting another measurement function

3.9.2.2 Error codes Er 02 and Er 03 are cleared by:

a. Obtaining a measurement result that is within range

b. Selecting another measurement function

3.9.2.3 OP Er is cleared by pressing RESET

3.9.2.4 To clear Er 60 and 61 refer to the Fault Finding Chart in Figure 6.12

3.10 MATH FUNCTION

3.10.1 General Information

3.10.1.1 The math function may be used with all measurement functions except Phase A rel B and CHECK. Its use permits the measured value to be offset and/or scaled before being displayed.

3.10.1.2 When the math function is active, the display indicates:

$$\frac{\text{Measurement Result} - X}{Z}$$

where X and Z are values entered by the operator into instrument stores. When the instrument is first powered on, X is set to 0 and Z to 1.

NOTE:

It is possible to set the constant Z to zero. However, any attempt to use the math function with this value set will cause an error code to be generated.

3.10.1.3 Table 3.14 shows how to set constants X and Z to obtain displays of ratio, offset (null), and percentage difference.

Table 3.14 - Uses of Math Function

Function Displayed	X	Z
Ratio: Measurement/N	0	N
Offset: Measurement - N	N	1
Percentage difference: 100 (Measurement-N)/N	N	N/100

3.10.2 Displaying the Math Constants

3.10.2.1 The values held in the X and Z stores can be displayed by pressing either

[SHIFT] [RECALL] [X] or

[SHIFT] [RECALL] [Z]

3.10.3 Changing the Math Constants

3.10.3.1 New values are entered into the math-constant stores using the numeric keypad. Employ either direct decimal or exponential format. For example, a value for X of 0.0231 may be entered using one of the following key sequences:

[.] [0] [2] [3] [1] [SHIFT] [STORE] [X]

or [2] [3] [1] [SHIFT] [EXP] [4] [SHIFT] [+/-] [SHIFT] [STORE] [X]

The instrument returns to the measurement mode automatically once the new math constant is stored.

3.10.3.2 The ranges of permissible values are as follows:

a. $1 \times 10^{-9} \leq Z < 1 \times 10^{10}$

b. 0

c. $-1 \times 10^{10} < Z \leq -1 \times 10^{-9}$

For negative numbers, the ninth digit is available, but not displayed.

3.10.4 Enabling and Disabling the Math Function

3.10.4.1 The math function is enabled and disabled by means of the key sequence

SHIFT (R-X)/Z

The (R-X)/Z LED lights when the math function is enabled.

3.11 EXTERNAL ARMING

3.11.1 General Information

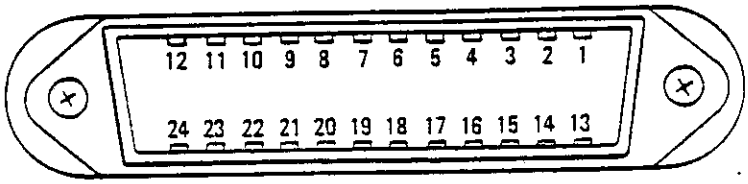
3.11.1.1 This feature allows the start and/or stop point to be synchronized to a real-time event or complex signal. The arming signal is connected to the rear-panel input and the appropriate special function selected (see Table 3.12). Measurement gate opening and closing are still determined by the input signal, but now can be conditioned (armed) by the external arming signal. Minimum start-to-stop external arming period is 50 µs (80 µs for RATIO A/B).

SECTION 4 GPIB OPERATION

4.1 GENERAL PURPOSE INTERFACE BUS (GPIB)

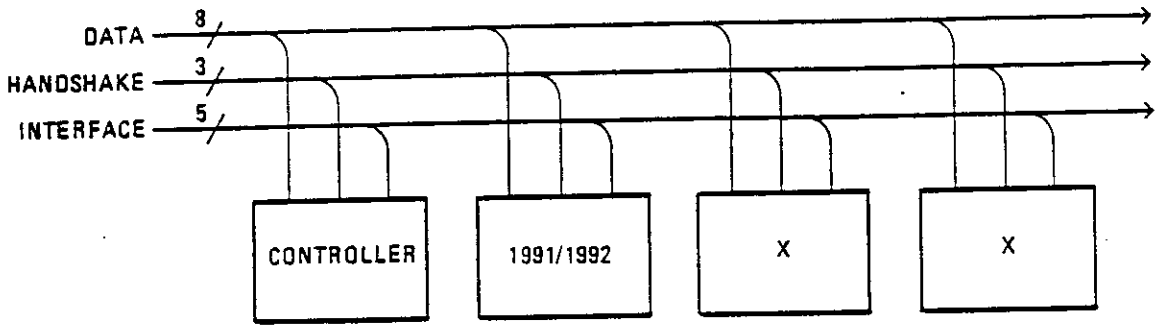
4.1.1 Introduction

4.1.1.1 This subsection provides operating information for the 1991/1992 using the GPIB interface. The IEEE-488-1978 interface permits remote control of all the counter's functions except POWER ON/OFF and STBY. Inputs and outputs are made via a standard 24-pin connector (see Figure 4.1) on the rear panel. Pin location, signal line identification, and GPIB operation comply with IEEE-STD-488-1978. An adapter, Racal-Dana P/N 23-3254, to convert the connector to the IEC 625-1 standard is available as an optional accessory. The GPIB provides interface capability with other instruments and a controller also using the interface-bus structure (see Figure 4.2). This figure also shows signal line designations and pin assignments. IEEE-STD-488-1978 subsets available are listed in Table 4.1.



Pin No.	Assignment	Pin No.	Assignment
1	DIO 1	13	DIO 5
2	DIO 2	14	DIO 6
3	DIO 3	15	DIO 7
4	DIO 4	16	DIO 8
5	EOI	17	REN
6	DAV	18	GND, (6)
7	NRFD	19	GND, (7)
8	NDAC	20	GND, (8)
9	IFC	21	GND, (9)
10	SRQ	22	GND, (10)
11	ATN	23	GND, (11)
12	SHIELD	24	GND, (5 AND 17)

Figure 4.1 - GPIB Connector (Rear Panel)



Pin	Nomenclature	Description
1	DIO-1 Data In/Out Bit 1 (LSB)	Data lines are used to transfer data from one instrument to another
2	DIO-2 Data In/Out Bit 2	
3	DIO-3 Data In/Out Bit 3	
4	DIO-4 Data In/Out Bit 4	
13	DIO-5 Data In/Out Bit 5	
14	DIO-6 Data In/Out Bit 6	
15	DIO-7 Data In/Out Bit 7	
16	DIO-8 Data In/Out Bit 8	
6	DAV (Data Valid)	Handshake lines operate in a proper time sequence for complete communication between instruments
7	NRFD (Not Ready for Data)	
8	NDAC (Not Data Accepted)	
5	EOI (End or Identify)	Interface lines are used to provide an orderly flow of information between units
9	IFC (Interface Clear)	
10	SRQ (Service Request)	
11	ATN (Attention)	
17	REN (Remote Enable)	
12	SHIELD	
18	GND (6)	
19	GND (7)	
20	GND (8)	
21	GND (9)	
22	GND (10)	
23	GND (11)	
24	GND (5 and 17)	

Figure 4.2 - Interface Signal Pin Assignments

4.2 GPIB DESCRIPTION

4.2.1 Refer to Figure 4.2. There are 24 lines available at the GPIB connector, including 16 signal and 7 ground return lines, and one shield. All of the data bus lines are either input or output lines, having the following characteristics:

Logic Levels:	1 = Low = $\leq$ .8V
	0 = High = $\geq$ 2.0V
Input Loading:	Each input = one TTL load
Output:	The output is capable of driving 15 interface bus loads. It consists of an open-collector driver and is capable of sinking 48 mA with a maximum voltage drop of 0.4 volts. See the IEEE-488 Electrical Specifications

Table 4.1 - IEEE-488-1978 Standard Interface Subset Capability

GPIB Subset	Description	Applicable Capability
SH1	Source Handshake	Complete Capability
AH1	Acceptor Handshake	Complete Capability
T5	Talker	Complete Capability: (1) Basic Talker (2) Serial Poll (3) Talk Only Mode (4) Unaddress if MLA
TE0	Extended Talker	None
L4	Listener	Complete except Listen Only (1) Basic Listener (2) Unaddress if MTA
LE0	Extended Listener	None
SR1	Service Request	Complete Capability
RL1	Remote/Local	Complete Capability: (1) REN - Remote Enable (2) LL0 - Local Lockout (3) GTL - Go to Local
PP0	Parallel Poll	No Capability
DC1	Device Clear	Complete Capability: (1) DCL - Device Clear (2) SDC - Selected Device Clear
DT1	Device Trigger	Complete Capability: GET - Group Execute Trigger
C0	Controller	No Capability
E1	Open Collector Bus Drivers	

4.2.2 The signal lines shown in Figure 4.2 consist of three functionally separate sets: Data, Handshake, and Interface.

4.2.2.1 **Data** - the data lines consist of DIO-1 to DIO-8. These lines are the signal channels over which data flows between all instruments on the bus in bit-parallel, byte-serial form.

4.2.2.2 **Handshake** - these three transfer lines consist of: DAV (Data Valid), NDAC (Not Data Accepted), and NRFD (Not Ready for Data). These lines provide communication between GPIB bus members (i.e., between the instrument that is talking and the instrument(s) that are listening) to synchronize the information flow across the eight data lines. These lines derive their nomenclature from their meaning in the low or 1 state (e.g., when NRFD is low, the device is Not Ready for Data).

a. **DAV** - when low, it signifies that valid information is available on the data lines

b. **NRFD** - when low, it signifies that the instrument is not ready to accept information

c. **NDAC** - when low, it signifies that information is not accepted by the acceptor bus device

4.2.2.3 **Interface** - these five interface lines coordinate the information flow on the bus.

a. **IFC (Interface Clear)** - places the instrument in the Idle state (i.e., Untalk, Unlisten)

b. **ATN (Attention)** - indicates the kind of information on the data lines during a handshake transfer sequence. Low indicates data lines carry interface commands; high indicates that the data lines carry data

c. **REN (Remote Enable)** - arms the instrument to select Remote operation when it's addressed as a listener

d. **SRQ (Service Request)** - signals the system controller that a peripheral device or bus member wants attention for purposes such as transmitting measurement, status, or condition information to the system controller

e. **EOI (End or Identify)** - used for (1) signifying the end of a message and (2) together with ATN, signalling bus peripherals to set the I/O bit assigned for parallel poll identification

4.2.3 GPIB Handshake

4.2.3.1 The handshake sequence is the process by which each data byte is transferred from the source to the acceptor.

4.2.3.2 Refer to Figure 4.3. It shows the sequential relationship between the DAV, NRFD, and NDAC lines used to transfer data bytes. Figure 4.4 shows the handshake flow chart.

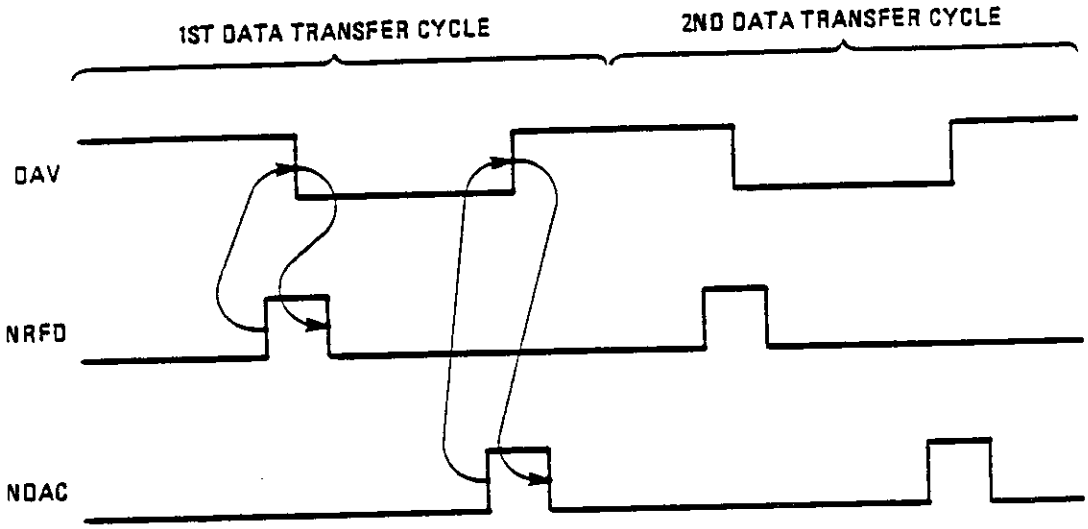


Figure 4.3 - Handshake Sequence

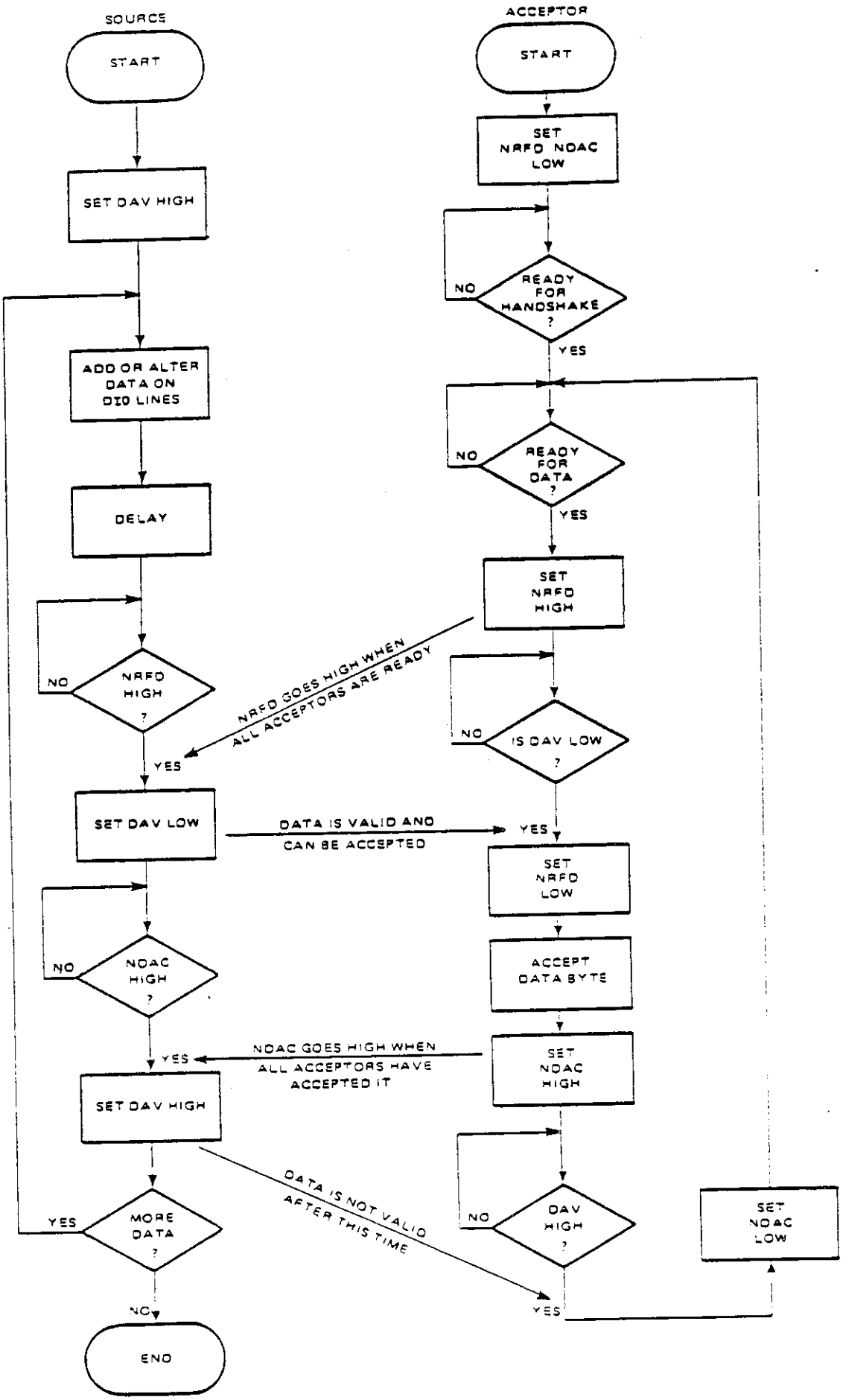


Figure 4.4 – Handshake Flow Chart

4.3 GPIB ADDRESS ASSIGNMENT

4.3.1 The 1991/1992 must be assigned an address as a bus member when operating in a GPIB system. Assigning an address to the counter permits it to be "called up" by the system controller or other resident bus device without interfering with them.

NOTE:

Only a total of 15 devices, including the 1991/1992, can reside on any single 488-bus.

4.3.2 The counter is equipped with a rear-panel switch bank, enabling the user to assign one of 31 addresses (numbers 00 to 30).

4.3.3 Table 4.2 contains all the information required for setting the counter's address and determining the talk and listen address codes used in programming the controller.

Table 4.2 - 1991/1992 GPIB Address Assignment

ASCII CHARACTERS		DATA LINES							ADDRESS SWITCH SETTING ** TALK ONLY A5 A4 A3 A2 A1	DECIMAL ADDRESS
		D_7	D_6	D_5	D_4	D_3	D_2	D_1		
TALK	LISTEN	TALK	LISTEN	ADDRESS						
				16	8	4	2	1		
	SP	0	1	0	0	0	0	0		00
@		1	0	0	0	0	0	0		
	!	0	1	0	0	0	0	1		01
A		1	0	0	0	0	0	1		
	"	0	1	0	0	0	1	0		02
B		1	0	0	0	0	1	0		
	#	0	1	0	0	0	1	1		03
C		1	0	0	0	0	1	1		
	$	0	1	0	0	1	0	0		04
D		1	0	0	0	1	0	0		
	%	0	1	0	0	1	0	1		05
E		1	0	0	0	1	0	1		
	&	0	1	0	0	1	1	0		06
F		1	0	0	0	1	1	0		
	' (APOSTROPHE)	0	1	0	0	1	1	1		07
G		1	0	0	0	1	1	1		
	(	0	1	0	1	0	0	0		08
H		1	0	0	1	0	0	0		
	)	0	1	0	1	0	0	1		09
I		1	0	0	1	0	0	1		
	*	0	1	0	1	0	1	0		10
J		1	0	0	1	0	1	0		
	+	0	1	0	1	0	1	1		11
K		1	0	0	1	0	1	1		
	,	0	1	0	1	1	0	0		12
L		1	0	0	1	1	0	0		
	–	0	1	0	1	1	0	1		13
M		1	0	0	1	1	0	1		
	.	0	1	0	1	1	1	0		14
N		1	0	0	1	1	1	0		
	/	0	1	0	1	1	1	1		15
O		1	0	0	1	1	1	1		

**The "Talk Only" switch is set to "ON" when used with a printer or other "listen only" device.

Table 4.2 – 1991/1992 GPIB Address Assignment (Cont'd)

ASCII CHARACTERS		DATA LINES							ADDRESS SWITCH SETTING	DECIMAL ADDRESS
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	** TALK ONLY (1 / 0) · A5 A4 A3 A2 A1 · switches 1–6	
TALK	LISTEN	TALK	LISTEN	ADDRESS						
				16	8	4	2	1		
	ø	0	1	1	0	0	0	0		16
P		1	0	1	0	0	0	0		
	1	0	1	1	0	0	0	1		17
Q		1	0	1	0	0	0	1		
	2	0	1	1	0	0	1	0		18
R		1	0	1	0	0	1	0		
	3	0	1	1	0	0	1	1		19
S		1	0	1	0	0	1	1		
	4	0	1	1	0	1	0	0		20
T		1	0	1	0	1	0	0		
	5	0	1	1	0	1	0	1		21
U		1	0	1	0	1	0	1		
	6	0	1	1	0	1	1	0		22
V		1	0	1	0	1	1	0		
	7	0	1	1	0	1	1	1		23
W		1	0	1	0	1	1	1		
	8	0	1	1	1	0	0	0		24
X		1	0	1	1	0	0	0		
	9	0	1	1	1	0	0	1		25
Y		1	0	1	1	0	0	1		
	:	0	1	1	1	0	1	0		26
Z		1	0	1	1	0	1	0		
	;	0	1	1	1	0	1	1		27
[		1	0	1	1	0	1	1		
	<	0	1	1	1	1	0	0		28
\		1	0	1	1	1	0	0		
	=	0	1	1	1	1	0	1		29
]		1	0	1	1	1	0	1		
	>	0	1	1	1	1	1	0		30
^		1	0	1	1	1	1	0		
NONE		ILLEGAL							NONE	31

**The "Talk Only" switch is set to "ON" when used with a printer or other "listen only" device.

4.3.4 Note in the table the column headed "ADDRESS SWITCH SETTING". It illustrates the positions of switches A1 to A5 for each number address listed in the far right column. To set the GPIB address, simply select the desired decimal address for the counter, refer to the table, and set the switches on the address selector to the corresponding pattern shown in the column.

4.3.5 Once an address has been assigned and stored, the controller may then address the 1991/1992 as a talker/listener by transmitting the appropriate ASCII character on the data lines. The "DATA LINES" column of the table shows the 7-bit binary codes for every talk/listen address assigned to the counter. The controller transmits these codes to the counter to establish its talker/listener status.

4.3.6 Note also in the table that there are two address codes for each GPIB address number. Each code represents a different ASCII character. For example, if an address of 02 is assigned to the counter, the talk address is the ASCII character B and the listen address is the ASCII character ". The only difference in the binary code in each case is the state of data lines D6 and D7.

4.3.7 The counter's GPIB address can be displayed in decimal form using key sequence SHIFT RECALL RESET. If the 1991/1992's bus address is changed, the previous key sequence must be repeated to display the new address. Press the CONTINUE key to return the 1991/1992 to the measurement mode.

4.3.8 The rear-panel GPIB switch bank provides a TALK ONLY selector switch (see Subsection 4.6.2). For addressed operation, the TALK ONLY switch must be in the logic 0 position (down).

4.3.9 The 1991/1992 is preset at GPIB address 14, 15, 16 or 17 when shipped.

4.4 GPIB FUNCTIONAL CHECK

4.4.1 Introduction

4.4.1.1 The following procedure verifies the 1991/1992's capability to accept, process, and transmit GPIB messages. Complete a satisfactory functional check of the counter under local control before starting this procedure (see Subsection 2.6).

4.4.1.2 Successful completion of this GPIB check indicates that the counter's GPIB interface is operating properly. This procedure does not check that all the device-function commands can be executed. However, if the GPIB interface works correctly and the counter operates correctly under local control, there is a high probability that it will respond to all device-function commands.

4.4.1.3 For recommended test equipment use a Hewlett-Packard Model HP-85 GPIB controller with I/O ROM in a drawer. It is assumed that the select code for the controller I/O port is 7 and the GPIB address of the counter is 15.

NOTE:

If any other controller or selected/GPIB address combination is used, the GPIB commands in the following procedure will require change.

4.4.1.4 Connect the controller to the GPIB interface of the counter using a standard GPIB cable. No connection should be made to Inputs A, B, or C.

4.4.2 Remote and Local Check

4.4.2.1 Now perform the following procedure:

a. Power-on the counter. Verify that the REM, ADDR, and SRQ LEDs flash on and off once. If the indicators do not flash or flash continuously, there is a fault on the GPIB PCB. Verify that the counter assumes the home state described in Subsection 2.6.1.2.

b. Test as shown below:

Action	HP-85 Code	Your Controller
Send the REN command true, together with the 1991/1992's listen address	REMOTE 715	

c. Verify that the REM LED lights

d. Test as shown below:

Action	HP-85 Code	Your Controller
Send the device-dependent command CK	OUTPUT 715; "CK"	

e. Verify that the ADDR LED lights and that the Check mode is selected

f. Test as shown below:

Action	HP-85 Code	Your Controller
Send the 1991/1992's listen address followed by the GTL command	LOCAL 715	

g. Verify that the REM LED is off. The ADDR LED will also turn off if the controller automatically transmits the UNL (unlisten) command true, as is the case using the HP-85

4.4.3 **Local Lockout and Clear Lockout Check**

4.4.3.1 Test as shown below:

Action	HP-85 Code	Your Controller
Send the REN command true, together with the 1991/1992's listen address	REMOTE 715	
Send the LLO command	LOCAL LOCKOUT 7	

a. Verify that the REM LED lights. Operate the LOCAL key on the front panel and check that the REM LED remains lit

b. Test as shown below:

Action	HP-85 Code	Your Controller
Send the REN command false	LOCAL 7	

c. Verify that the REM LED is off

d. Test as shown below:

Action	HP-85 Code	Your Controller
Send the REN command true, together with the 1991/1992's listen address	REMOTE 715	

e. Verify that the REM LED lights. Operate the LOCAL key and check that the REM LED turns off

4.4.4 Data Output Check

4.4.4.1 Test as shown below:

Action	HP-85 Code	Your Controller
Set the 1991/1992 in the Check mode by sending the counter's listen address, followed by the device-dependent command CK	OUTPUT 715; "CK"	
Prepare a store to receive a 21-byte data string	DIM Z$ 21	
Send the 1991/1992's talk address. Store the 21-byte data string in the prepared store	ENTER 715; Z$	
Display the contents of the store	DISP 7$	

a. Verify that the HP-85 display reads CK+0010.0000000E+06 with the cursor moved to the next line, indicating that carriage return (CR) and line feed (LF) have been accepted

4.4.5 SRQ and Status Byte Check

4.4.5.1 Test as shown below:

Action	HP-85 Code	Your Controller
Send the REN command true	REMOTE 7	
Set the 1991/1992 to transmit the SRQ command when an error is detected, and force the generation of error code 0_ by sending device-dependent command XXX	OUTPUT 715; "TPXXX"	
Store the status of the GPIB interface of the controller, in binary form, as variable T	STATUS 7,2; T	
Display the status of the SRQ line	DISP "SRQ="; BIT (T,5)	

a. Verify that the HP-85 display reads SRQ=1, the SRQ status bit is at logic 1 or the SRQ line is $\leq$0.8 V. Confirm that the SRQ LED is lit

b. Test as shown below:

Action	HP-85 Code	Your Controller
Conduct a serial poll and store the status byte as variable R	R=SPOLL (715)	
Display variable R	DISP "R="; R	

c. Verify that the SRQ LED is turned off when the serial poll is made. The value of R should be 101 (in binary form, R should be 0000000001100101). If using an HP-85 controller, verify that the ADDR LED is turned off

4.4.6 **Device Clear and Selected Device Clear Check**

4.4.6.1 Test as shown below:

Action	HP-85 Code	Your Controller
Set the 1991/1992 to the Total A by B mode by sending the instrument's listen address, followed by device-dependent command TA	OUTPUT 715; "TA"	
Send the DCL command true	CLEAR 7	

a. Verify that the function indicated on the front panel changes to FREQ A

b. Test as shown below:

Action	HP-85 Code	Your Controller
Reset the 1991/1992 to the Total A by B mode by sending the instrument's listen address, followed by device- dependent command TA	OUTPUT 715; "TA"	
Send the SDC message true	CLEAR 715	

c. Verify that the function indicated on the front panel changes to FREQ A

4.4.7 IFC Check

4.4.7.1 Test as shown below:

Action	HP-85 Code	Your Controller
Send the ATN message false	RESUME 7	
Send the IFC message true	ABORTIO 7	

a. Verify that the ADDR LED is turned off

4.4.8 TALK ONLY Selector Check

4.4.8.1 Perform the following procedure:

a. Set the TALK ONLY switch on the counter's rear panel to 1. Verify that the REM LED is turned off and the ADDR LED lights

b. Set the TALK ONLY switch to 0. Verify that the ADDR LED is turned off

4.5 INTERFACE MESSAGE REPERTOIRE and RESPONSE

4.5.1 Introduction

4.5.1.1 The 1991/1992 is equipped with a standard GPIB interface designed to meet IEEE-STD-488-1978 specifications. These specifications provide a definition of multiline interface messages, dividing them into two main groups:

a. Primary command group

b. Secondary command group

This counter includes only the primary commands in its interface repertoire.

4.5.1.2 The primary command group is further divided into four categories:

a. Listen address commands

b. Talk address commands

c. Addressed commands

d. Universal commands

4.5.2 Listen and Talk Address Commands

4.5.2.1 The counter responds to address messages defined by the programmed GPIB address set from the rear panel. Refer back to Table 4.2 as required for a listing of the 31 talk and 31 listen addresses. The 1991/1992 will respond to talk and listen address messages regardless of its addressed state.

4.5.2.2 Listen Addresses

4.5.2.2.1 Receipt by the counter of a listen address makes it a listener. If previously addressed to talk, the counter ceases to be a talker. In in Local mode, the counter reverts to its Remote state, provided the REN message is true.

4.5.2.3 Talk Addresses

4.5.2.3.1 Receipt by the counter of a talk address makes it a talker. If previously addressed to listen, the counter ceases to be a listener. If in Local mode, the counter will remain under local control.

4.5.2.4 Talk Addresses - Other Devices

4.5.2.4.1 If the counter was previously addressed to talk, then receives the talk address of another bus device, the 1991/1992 ceases to be a talker.

4.5.3 Addressed and Universal Commands

4.5.3.1 Table 4.3 lists the Addressed and Universal commands to which the 1991/1992 responds. These multiline interface commands are recognized because they are sent with the ATN message as true. The following paragraphs describe the counter's response to each of these commands.

Table 4.3 - Addressed and Universal Commands

Message	Meaning	Hex Code	Decimal Equivalent	Data Line Code						
				7	6	5	4	3	2	1
GTL	Go To Local	01	1	0	0	0	0	0	0	1
SDC	Selected Device Clear	04	4	0	0	0	0	1	0	0
GET	Group Execute Trigger	08	8	0	0	0	1	0	0	0
LLO	Local Lock Out	11	17	0	0	1	0	0	0	1
DCL	Device Clear	14	10	0	0	1	0	1	0	0
SPE	Serial Poll Enable	18	24	0	0	1	1	0	0	0
SPD	Serial Poll Disable	19	25	0	0	1	1	0	0	1
UNL	Unlisten	3F	63	0	1	1	1	1	1	1
UNT	Untalk	5F	9	1	0	1	1	1	1	1

4.5.3.2 Go To Local (GTL)

4.5.3.2.1 Provided the counter is in remote and a listener, it reverts to local operation. The counter remains addressed to listen. It now operates by front-panel controls, until returned to remote control by receipt of the first byte of a device-dependent message. The decimal and hex equivalents are both 01.

4.5.3.3 Selected Device Clear (SDC)

4.5.3.3.1 Provided the counter is in remote and a listener, it reverts to home state. The condition of the GPIB interface remains unchanged. The decimal and hex equivalents are both 04.

4.5.3.4 Group Execute Trigger (GET)

4.5.3.4.1 Provided the counter is a listener and no measurement is in progress, it triggers a previously programmed measurement. The GET command permits several bus devices to simultaneously perform a number of different operations. (All bus members have been previously programmed to perform a function on receiving the GET command or trigger command.) The decimal and hex equivalents are both 08.

4.5.3.5 Local Lockout (LLO)

4.5.3.5.1 The counter responds to the LLO command regardless of its addressed state. The LLO command disables the LOCAL key on the front panel. Local lockout is cleared by sending the REN message as false, returning all bus devices to the local control state. A GTL command returns the counter to local control. The decimal and hex equivalents are 17 and 11, respectively.

4.5.3.6 Device Clear (DCL)

4.5.3.6.1 Same as the SDC command, except that all bus devices in remote are cleared. The counter responds to this command regardless of its addressed state. The decimal and hex equivalents are 10 and 14, respectively.

4.5.3.7 Serial Poll Enable (SPE)

4.5.3.7.1 This command permits all bus members, including the counter, to set their SRQ line to binary 1, informing the controller that attention is required. The 1991/1992 responds to this command regardless of its addressed state. Each bus member, having been made a talker, is then serially interrogated by the controller to determine which bus member(s) requested service and the purpose of each request. Bus members respond by transmitting their respective status bytes to the controller. All members respond to the SPE regardless of their addressed state. The hex and decimal equivalents are 18 and 24, respectively.

4.5.3.8 Serial Poll Disable (SPD)

4.5.3.8.1 This command returns all bus members to normal operation after completion of a serial poll. All bus members respond to the SPD command regardless of their addressed state. If addressed to talk, a bus device will put its data output string on the GPIB, provided such data is available in its output buffer. The decimal and hex equivalents are 25 and 19, respectively.

4.5.3.9 Untalk (UNT)

4.5.3.9.1 This universal command instructs all talkers, including the counter, to return to their untalk or talker-idle state. All bus members are also removed from their talker state whenever a talk address other than their own is received. In the Untalk state, the front-panel ADDR LED is turned off. The decimal and hex equivalents are 9 and 5F, respectively.

4.5.3.10 Unlisten (UNL)

4.5.3.10.1 This universal command instructs all listeners, including the counter, to return to their unlisten or listen-idle state. In the Unlisten state, the front-panel ADDR LED is turned off. The decimal and hex equivalents are 63 and 3F, respectively.

4.6 GPIB OPERATING MODES

4.6.1 Introduction

4.6.1.1 Before operating the counter on the GPIB, ensure that the instrument has been assigned its correct bus address (see Subsection 4.3) and that the correct AC line voltage has been selected (see Subsection 2.4.2). The last instruction is especially important if the 1991/1992 is being used for the first time or at a new location.

4.6.1.2 The 1991/1992 can be operated on the GPIB in either its Talk-Only or Addressed mode.

4.6.2 Talk-Only Mode

4.6.2.1 To set the counter in this mode, place the TALK ONLY switch of the GPIB switch bank in its logic "1" position. The GPIB interface is now in the Talk-Only mode and the settings of switches A1 to A5 are irrelevant.

4.6.2.2 The Talk-Only mode may be used in systems not having a controller. Such a system permits remote reading of counter measurement data, however, the instrument is controlled from the front panel (see Section 3).

4.6.2.3 The counter determines the rate at which measurements are made. The output buffer is updated at the end of each measurement cycle, overwriting the previous measurement data if not transferred to the listener.

4.6.2.4 The listener triggers the transfer of data from the counter. The counter's output buffer is cleared when data transfer is completed.

4.6.2.5 Differences between the measurement rate and data-transfer trigger-rate are resolved as follows:

a. If data transfer is in progress at the end of a measurement cycle, updating of the output buffer is delayed. Data transferred will correspond to the previous measurement cycle

b. If data transfer is requested during a measurement cycle and the output buffer is empty, data transfer is delayed until the buffer is updated. Data transferred will then correspond to the latest measurement cycle

c. If a measurement cycle is completed before the results of the previous cycle have commenced transfer to the listener, the buffer will be updated. The data from the previous cycle will be overwritten and lost.

4.6.2.6 Measurement rate in the 1991/1992 can be controlled in the following ways:

a. The gate time can be controlled by selecting an appropriate display resolution

b. A time interval delay can be set between measurement cycles by using Special Functions 40 to 44

c. The counter can be operated in the Hold mode (single-shot measurements). Readings are displayed indefinitely in Hold until the RESET key is pressed, initiating a new measurement cycle

4.6.3 Addressed Mode

4.6.3.1 In the Addressed mode, all of the counter's functions (except POWER ON/OFF and STBY) can be controlled by device-dependent commands (see Subsection 4.10). These commands are sent over the GPIB after the counter has been addressed to listen. Completed measurement readings and counter status information are then read back over the bus after the counter is addressed to talk. If the counter is addressed to talk when its output buffer is empty, no data transfer will occur and bus activity will cease. Data transfer will start again after the output buffer is updated at the completion of the next measurement cycle.

4.7 OUTPUT MESSAGE FORMAT (TALKER)

4.7.1 Introduction

4.7.1.1 Refer to Table 4.4. The 1991/1992 uses the same output message format for both transmitting measurement values as well as numbers recalled from the counter's internal stores.

4.7.1.2 The output message consists of a string of 21 ASCII characters for each transmitted value. Output messages should be interpreted using Tables 4.4 and 4.5. Measurement units should be assumed as hertz, seconds, volts, degrees, or a ratio, depending on commands previously sent to the counter.

NOTE:

An SRQ message is not enabled by data recall from the counter's stores.

Table 4.4 - Output Message Format

Byte No.	Interpretation	Permitted ASCII Characters	Notes
1	Function letter or space	See Table 4.5	Spaces are transmitted only if programmed with Special Function 81 active
2	Function letter or space	See Table 4.5	
3	Measurement sign	+ or -	
4	Most significant digit	0 to 9	Bytes 4 to 15 will always include 11 digits and decimal point. Zeros are added when necessary in the more significant positions
5	Digit	0 to 9 or.	
6	↓	↓	
7			
8			
9			
10			
11			
12			
13			
14			
15	Least significant digit		
16	Exponent indicator	E	Upper case only
17	Exponent sign	+ or -	
18	More significant digit	0 to 9	Exponent is a multiple of 3
19	Less significant digit	0 to 9	
20	Carriage return	CR	
21	Line feed	LF	

Table 4.5 - Function Letters

Function	Function Letters
Frequency A	FA
Frequency C (Model 1992 only)	FC
Ratio A/B	RA
Ratio C/B (Model 1992 only)	RC
Time Interval A→B	TI
Totalize A by B	TA
Phase A rel B	PH
Period A	PA
Check	CK
Recalled Data	**Function Letters**
Unit Type	UT
Resolution	RS
Trigger Level A	LA
Trigger Level B	LB
Math Constant X	MX
Math Constant Z	MZ
Delay Time	DT
Special Function	SF
Master Software Issue Number	MS
GPIB Software Issue Number	GS

4.8 SERVICE REQUEST (SRQ)

4.8.1 The counter can be set, by means of device-dependent commands, to enable an SRQ message whenever:

a. A measurement cycle is completed

b. A change of frequency standard occurs

c. An error state is detected

d. Any combination of a, b, and c

4.8.2 The front-panel SRQ LED lights when an SRQ message is asserted.

4.8.3 SRQ enablement may also be inhibited. Refer to Table 4.17 which provides the necessary SRQ commands. When in home state, condition "c" indicated above is active.

NOTE:

An SRQ message is not enabled by data recall from the counter's stores.

4.9 STATUS BYTE

4.9.1 To inform the controller of its status, the counter assembles and transmits a status message referred to as a status byte. The controller generates a serial poll enable cycle to determine which bus member has requested service and the purpose of the request. When the 1991/1992 receives the SPE command, and has been made a talker, it outputs the status byte to the controller. Table 4.6 shows the format of the counter's status byte.

Table 4.6 - Status Byte Format

DIO Line	Function
1	Error - Least significant bit - See NOTE 1
2	Codes
3	in Binary - Most significant bit
4	1 = Frequency standard changed
5	1 = Reading ready - See NOTE 2
6	1 = Error detected
7	1 = Service requested
8	1 = Gate open

Table 4.6 – Status Byte Format (Cont'd)

DIO Line	Function
	NOTE 1: The error codes and numbers are as follows: 1 = Phase measurement attempted on waveforms of differing frequency (Ratio ≠ 1) 2 = Result out-of-range of display 3 = Overflow of internal counters 4 = Numerical entry error 5 = GPIB syntax (programming) error See NOTE 3 No measurement output string is available if error codes 1, 2, or 3 is produced. **NOTE 2:** Regardless of the current SRQ mode, the SRQ message that a reading is ready is not generated after a data-recall operation. **NOTE 3:** The five error codes are cleared as follows: Error 1 – correct the difference in input frequencies or change the measurement mode Error 2 – complete an in-range measurement Error 3 – complete an in-range measurement Error 4 – complete a valid numerical entry Error 5 – the erroneous command string will be correctly executed up to the error; the rest will be handshaken, but not executed. Receipt of the next valid command clears the error

4.10 INPUT COMMANDS (LISTENER)

4.10.1 Introduction

4.10.1.1 The 1991/1992 responds to device-dependent commands in a "deferred" mode. This means that the GPIB interface continues to accept commands until a terminating character or message is received, then the entire string will be executed. There is no "immediate" mode in which commands are obeyed as they are received.

4.10.2 Device-Dependent Commands

4.10.2.1 When the counter is addressed to listen, it can be controlled by device-dependent commands. These commands are listed below, and tabulated in Tables 4.8 to 4.18.

a. Table 4.8 - Instrument Preset Code
b. Table 4.9 - Numerical Input Format
c. Table 4.10 - Measurement Function Codes
d. Table 4.11 - Numerical Input Ranges
e. Table 4.12 - Resolution Selection
f. Table 4.13 - Input Control Codes
g. Table 4.14 - Measurement Control Codes
h. Table 4.15 - Store and Recall Codes
i. Table 4.16 - Special Function Codes
j. Table 4.17 - Service Request Codes
k. Table 4.18 - Alphabetic List of Command Codes

4.10.2.2 Device-dependent commands are executed sequentially beginning with the first one sent and ending with the last.

4.10.2.3 If more than one command is to be sent, no delimiters are required. If necessary, commas, spaces, and semicolons may be included in the command strings for clarification without affecting counter operation.

4.10.2.4 Each command string must be followed by an end-of-string terminating group. Table 4.7 shows the valid terminator groups.

Table 4.7 - Permitted Terminators

1	2	3	4	5	6
LF	LF EOI	CR EOI	CR LF	CR LF EOI	Last Character EOI

Where LF=Line feed, CR=carriage return; EOI is considered true

NOTE:

Data output terminators are CR LF without EOI asserted.

4.10.2.5 Table 4.8 provides the instrument preset code for the 1991/1992. Refer to Subsection 1.6.15 for a listing of the counter's initialization conditions.

Table 4.8 - Instrument Preset Code

Function	Code
Sets counter functions and settings to home state	IP

4.10.2.6 Some of the device-dependent commands in the following tables require additional numerical input data. Such numerical input succeeds its command and is indicated by an asterisk (*) in the tabulations. Also, home-states are underlined. Refer to Table 4.9 as required for numerical input format.

Table 4.9 - Numerical Input Format

Byte No.	Interpretation	Permitted ASCII Characters
1	Sign of mantissa	+ or -
2	Most significant digit	0 to 9 or .
3	Digit	↓
4	↓	
5		
6		
7		
8		
9		
10	↓	
11	Least significant digit	↓
12	Exponent indicator	E or e
13	Exponent sign/space	+ or - or space
14	More significant digit	0 to 9
15	Less significant digit	0 to 9

NOTE 1:

Spaces, nulls, or zeros occurring before byte 1 are ignored by the counter.

NOTE 2:

Byte 1 may be omitted and a positive mantissa assumed.

NOTE 3:

Bytes 2 to 11 may have up to 9 digits and a decimal point. The decimal point, however, is not essential. After entry of 9 digits (without a decimal point), additional digits are ignored and a GPIB programming error is generated. Excess digits that are truncated will still increase the power-of-ten stored. Also, if fewer than 9 digits are needed, unused bytes may be omitted.

NOTE 4:

Spaces or nulls entered between bytes 11 and 12 are ignored by the counter.

Table 4.9 - Numerical Input Format (Cont'd)

NOTE 5:

Bytes 12 to 15 (exponent group) may be omitted. Also, byte 13 may be omitted or transmitted as a space (a positive exponent should be assumed in either instance).

NOTE 6:

Byte 15 may be omitted for a single-digit exponent.

NOTE 7:

Numbers may be terminated by one of the same terminators used for output messages, or by another device-dependent message.

NOTE 8:

Units are implied; volts for trigger levels, seconds for delay times.

4.10.2.7 Table 4.10 presents the measurement function codes for the 1991/1992.

Table 4.10 - Measurement Function Codes

Function	Code
Frequency A	FA
Frequency C (Model 1992 only)	FC
Period A	PA
Time Interval A→B	TI
Totalize A by B	TA
Ratio A/B	RA
Ratio C/B (Model 1992 only)	RC
Phase A rel B	PH
Check	CK

NOTE:

Only the 1992 accepts FC and RC as valid commands.

4.10.2.8 Table 4.11 provides the various numerical input ranges for the 1991/1992.

Table 4.11 - Numerical Input Ranges

Function	Command Code	Numerical Limits	
		Low	High
Resolution	SRS	3	10
Trigger Level (x1)	SLA, SLB	-5.1	+5.1
Trigger Level (x10)	SLA, SLB	-51	+51
Math Constant	SMX, SMZ	$\geq 1 \times 10^{-9}$	$< 1 \times 10^{10}$
		0	
		$> -1 \times 10^{10}$	$\leq -1 \times 10^{-9}$
Delay Time	SDT	200×10^{-6}	0.8

NOTE 1:

Entered numbers will be rounded up before storage as follows:

a. Trigger level x1 to next multiple of 20 mV

b. Trigger level x10 to next multiple of 200 mV

c. Delay to next multiple of 25.6 μs

NOTE 2:

Resolution entries are rounded down to the next integer. Refer to Table 4.12 for related gate times and GPIB resolution numbers.

NOTE 3:

Math constant Z can be set to zero. However, an error message will result if the Math function is enabled with this value set.

4.10.2.9 Table 4.12 provides the 1991/1992 GPIB resolution selection.

Table 4.12 - Resolution Selection

GPIB Resolution Number	Number of Selected Digits in Frequency, Period, Ratio, and Check	Gate Time
10	9 + Overflow	10 s
9	9	1 s
8	8	100 ms
7	7	10 ms
6	6	1 ms
5	5	1 ms
4	4	1 ms
3	3	1 ms

NOTE:

Refer to Table 3.11 as required. It shows the relationship of gate time and display resolution in the 1991/1992.

4.10.2.10 The following tables complete the necessary GPIB commands for the 1991/1992:

Table 4.13 - Input Control Codes

Function	Code
FILTER Disable/Enable	AFD/AFE
COM A Disable/Enable	BCS/BCC
DC/AC Coupling A	ADC/AAC
DC/AC Coupling B	BDC/BAC
1 MΩ/50Ω impedance A	AHI/ALI
1 MΩ/50Ω impedance B	BHI/BLI
Slope A +ve/-ve	APS/ANS
Slope B +ve/-ve	BPS/BNS
x10 attenuator A Disable/Enable	AAD/AAE
x10 attenuator B Disable/Enable	BAD/BAE
Manual/AUTO-TRIG A	AMN/AAU
Manual/AUTO-TRIG B	BMN/BAU

Table 4.14 - Measurement Control Codes

Function	Code
Continuous measurement mode selection	T0 (See NOTE 1)
Single (One-Shot) measurement mode selection	T1 (See NOTE 2)
Start Totalize or trigger a measurement (T1 mode)	T2 (See NOTE 3)
Stop Totalize	T3 (See NOTE 3)
Read current value while measurement is in progress (i.e., next reading on the fly)	RF (See NOTE 4)
Math function Disable/Enable	MD/ME
Delay Disable/Enable	DD/DE
Reset measurement	RE

NOTE 1:

In continuous measurement mode, the output buffer is updated at the end of each gate period. If the buffer is being read out via the bus when the gate period ends, updating is delayed until reading is complete.

NOTE 2:

In single-measurement mode, the output buffer is cleared every time a T1 command is received. The measurement completed must be read, therefore, before the next measurement cycle is triggered.

NOTE 3:

In making totalize measurements, T2 and T3 commands are used with the TA command and Special Function 61. In this mode, the readings executed in successive totalize periods are cumulative; the RE command is used to reset the count to zero when required.

NOTE 4:

The RF command must be sent each time a reading is required. The reading is obtained when the counter is made a talker.

Table 4.15 - Store and Recall Codes

Function	Code
Recall unit type	RUT
Store display resolution number	SRS
Recall display resolution number	RRS
Store A channel manual trigger level	SLA (See NOTE 1)
Recall A channel manual trigger level or peak level	RLA (See NOTES 1 and 2)
Store B channel manual trigger level	SLB (See NOTE 1)
Recall B channel manual trigger level or peak level	RLB (See NOTES 1 and 2)
Store math constant X	SMX
Recall math constant X	RMX
Store math constant Z	SMZ
Recall math constant Z	RMZ
Store arming delay value	SDT
Recall arming delay value	RDT
Recall special function register	RSF
Recall master software issue number	RMS
Recall GPIB software issue number	RGS

NOTE 1:

The manual trigger level is automatically scaled by a factor of 10 when the x10 attenuator is switched in or out of circuit. Ensure that the correct input attenuation is selected before storing or recalling the trigger level.

NOTE 2:

The levels recalled by commands RLA and RLB depend upon the enablement of Special Functions 50, 51, and 52.

NOTE 3:

Numbers to be stored should follow the store command. The format to be used for numerical entry is provided in Table 4.9. The limiting values for numerical entries are given in Table 4.11.

NOTE 4:

The counter returns to the measurement mode automatically at the completion of a store or recall operation.

NOTE 5:

No SRQ message is generated for recalled data.

Table 4.16 - Special Function Codes

Function	Code
Special functions Disabled/Enabled	SFD/SFE
Store special function nn	Snn

NOTE 1:

The list of special functions (SFs) is provided in Table 3.12.

NOTE 2:

Storing a special function when special functions are enabled immediately enables that special function.

Table 4.17 - Service Request Codes

Function	Code
SRQ generation inhibited	Q0
upon error detection	Q1
for measurement ready	Q2
for measurement ready or error detection	Q3
for frequency standard change	Q4
for frequency standard change or error detection	Q5
for measurement ready or frequency standard change	Q6
for measurement ready, frequency standard change, or error detection	Q7

NOTE:

An SRQ message is not generated by data recalled from stores.

Table 4.18 - Alphabetic List of Command Codes

Code	Command	Code	Command
AAC	A Channel, AC coupling	PA	Period A
AAD	A Channel, x10 attenuator disabled	PH	Phase A relative to B
AAE	A Channel, x10 attenuator enabled	Qn	SRQ mode
AAU	A Channel auto-trigger	RA	Ratio A/B
ADC	A Channel, DC coupling	RC	Ratio C/B (Model 1992 only)
AFD	A Channel filter disabled	RDT	Recall arming delay time
AFE	A Channel filter enabled	RE	Reset measurement
AHI	A Channel, 1 Mohm	RF	Read total so far
ALI	A Channel, 50 ohms	RGS	Recall GPIB software issue number
AMN	A Channel manual trigger	RLA	Recall trigger level A or peak level
ANS	A Channel, -ve slope	RLB	Recall trigger level B or peak level
APS	A Channel, +ve slope	RMS	Recall master software issue number
BAC	B Channel, AC coupling	RMX	Recall math constant X
BAD	B Channel, x10 attenuator disabled	RMZ	Recall math constant Z
BAE	B Channel, x10 attenuator enabled	RRS	Recall display resolution
BAU	B Channel auto-trigger	RSF	Recall special function
BCC	A and B Channels common	RUT	Recall unit type
BCS	A and B Channels separate	Snn	Special function number
BDC	B Channel, DC coupling	SDT	Store arming delay time
BHI	B Channel, 1 Mohm	SFD	Special function disabled
BLI	B Channel, 50 ohms	SFE	Special function enabled
BMN	B Channel manual trigger	SLA	Store trigger level A
BNS	B Channel, -ve slope	SLB	Store trigger level B
BPS	B Channel, +ve slope	SMX	Store math constant X
CK	Check	SMZ	Store math constant Z
DD	Delay disabled	SRS	Store display resolution
DE	Delay enabled	Tn	Measurement mode or start/stop reading
FA	Frequency A	TA	Total A by B
FC	Frequency C (Model 1992 only)	TI	Time Interval
IP	Instrument Preset		
MD	Math function disabled		
ME	Math function enabled		

SECTION 5 GENERAL THEORY OF OPERATION

5.1 INTRODUCTION

5.1.1 This section describes the general theory of operation for the 1991/1992.

5.1.2 The theory of operation provided is based on the simplified overall block diagram shown in Figure 5.1. Key circuit blocks of the 1991/1992 are described and supported in this section using simplified block and schematic diagrams. These diagrams supplement the complete schematics found in Section 7 of this manual. As much as possible, the simplified schematic and block diagrams provided here use the same reference designators found in the complete schematics. This should facilitate cross-referencing between this section of the manual and the schematics.

5.1.3 Integrated circuits (ICs) in the following circuit descriptions are designated by circuit references provided on the supporting simplified block and schematic diagrams. The IC designations employed in the following key circuit descriptions follow those found in supplied schematics.

When an IC package contains more than one circuit, suffix letters are used to distinguish them (e.g., IC1a). Finally, when it is necessary to identify a specific pin in an IC, the reference designator, with a suffix letter if necessary, is followed by a hyphen and then the required pin number (e.g., IC1a-1).

5.2 FUNCTIONAL BLOCKS

5.2.1 The 1991/1992 contains the following ten main functional blocks:

a. Channel A/B block (see Subsection 5.3.1)

b. Channel C (Model 1992 only) block (see Subsection 5.3.2)

c. Measurement block (see Subsection 5.3.3)

d. Display block (see Subsection 5.3.4)

e. Keyboard block (see Subsection 5.3.5)

f. Microprocessor block (see Subsection 5.3.6)

g. Standby and IRQ block (see Subsection 5.3.7)

h. Power Supply block (see Subsection 5.3.8)

i. Internal Frequency Standard block (see Subsection 5.3.9)

j. GPIB Interface (see Subsection 5.3.10)

5.2.2 The functional relationship between the blocks of the 1991/1992 is illustrated in Figure 5.1. The measurement block is internally configured by the microprocessor according to the instructions entered via the keyboard or over the GPIB. The signal to be measured and the signal from the frequency standard are fed to the measurement block. The measured result is passed to the microprocessor. If mathematical manipulation of the result is required, this is performed by the

microprocessor before the final output is passed to the display or system.

5.2.3 The standby and IRQ block handles instructions to switch to standby. These instructions are received from the keyboard block and interrupt requests made by other systems.

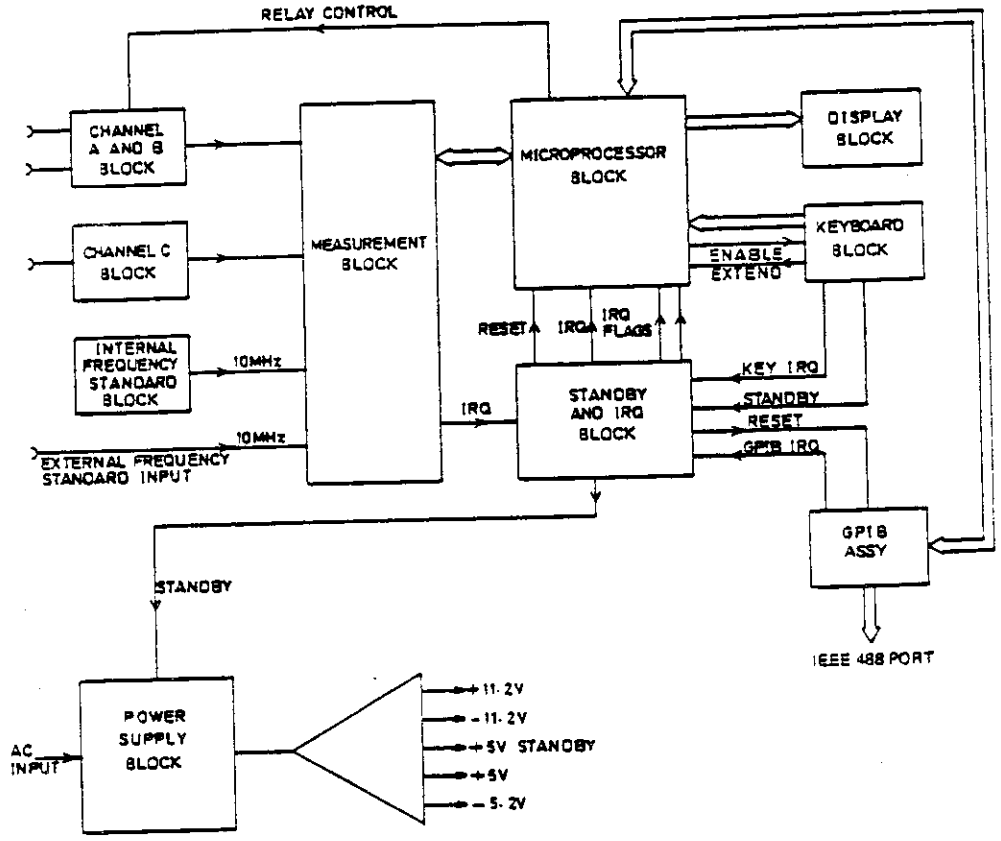


Figure 5.1 - Simplified Overall Block Diagram

5.3 THEORY OF OPERATION BY BLOCK

5.3.1 Channel A/B Block

5.3.1.1 Functional Description

5.3.1.1.1 Channel A/B block processes the signals applied at the respective A/B inputs to produce differential pairs of signals which are fed to the measurement block. A block diagram is shown in Figure 5.2.

5.3.1.1.2 Each channel includes relay-controlled circuits which allow selection of 50 Ω/1 MΩ input impedance, AC/DC coupling, and x1/x10 attenuation. The COM(mon) A configuration (Channel B signal disconnected and Channel A signal connected to both amplifiers in parallel) can be selected.

5.3.1.1.3 The channel amplifiers feature separate high frequency and low frequency paths. The crossover frequency is nominally 5 kHz. Signal filtering can be introduced, in Channel A only, by disconnecting the high-frequency amplifier path and increasing the bandwidth of the low frequency path to 50 kHz nominal. The signals from the high and low frequency paths are combined and drive a Schmitt trigger output stage.

5.3.1.1.4 The trigger levels for the two channels are derived independently in the digital-to-analog converter (DAC) using data supplied from the microprocessor.

5.3.1.1.5 Control signals for the system relays are supplied from the microprocessor.

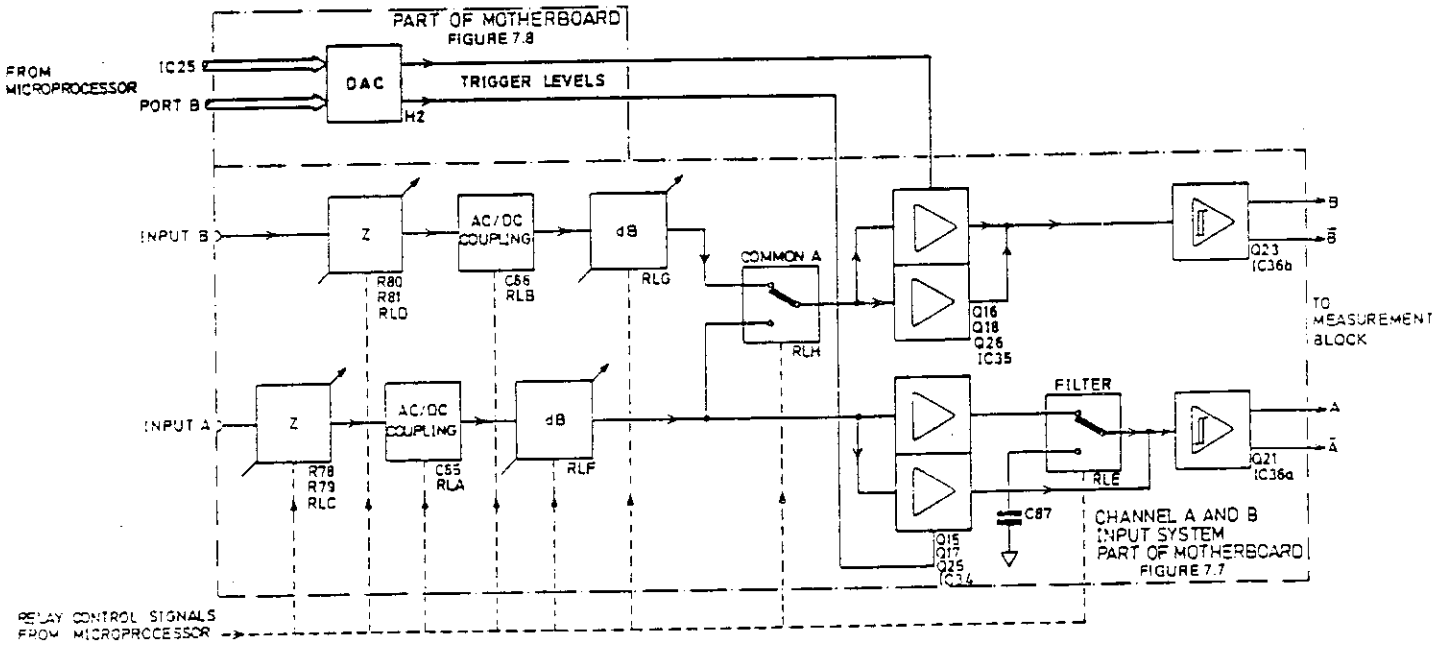


Figure 5.2 - Channel A/B Block Diagram

5.3.1.2 Circuit Description

5.3.1.2.1 Refer to the schematic shown in Figure 7.7. When relay RLC is energized, the input impedance seen at SK5 (INPUT A) is 50Ω , given by resistors R78 and R79 in parallel.

5.3.1.2.2 When energized, RLA gives DC coupling of the input signal. With RLA deenergized, the signal is AC coupled via C65. R165 limits the current surge which occurs if DC coupling is selected while C65 is in the charged state.

5.3.1.2.3 The x1/x10 attenuator is formed by R82, R83, R87 and RLF. With RLF deenergized, the attenuator has a series element, R82, and a shunt element formed by R83 and R87 in parallel. The attenuation is 20 dB (nominal). With RLF energized R82 is short-circuited, giving 0 dB attenuation.

5.3.1.2.4 The attenuator output is fed to the high-frequency channel buffer, Q15 and Q17, via R160 and C73. The gate of Q15 is protected against excessive negative voltage swings by D5. The gain from the attenuator output to the emitter of Q17 is approximately 0.94.

5.3.1.2.5 The buffer of the low frequency channel, IC34 and Q25, receives its input from the potential divider R87. The gain from R87 pin 1 to the emitter of Q25 is approximately 0.94. Any offset in the system can be nulled by adjusting R192.

5.3.1.2.6 When RLE is deenergized (Channel A filter not selected), the signals from the two buffers are combined at the base of Q21 by the network C79 and R107. These components act as a low-pass filter to the output of the low frequency buffer, and as a high-pass filter to the output of the high frequency buffer. The crossover frequency is 5 kHz.

5.3.1.2.7 The signal at Q21 emitter is fed to the Schmitt trigger IC36a via the diode bridge formed by D18, D19, D20, and D21. This protects the input of IC36a by limiting the signal swing to approximately ±1V.

5.3.1.2.8 The differential output of IC36 forms the input to the measuring block. The hysteresis of IC36, and therefore the channel sensitivity, can be set by adjusting R149.

5.3.1.2.9 The trigger level is set by the DAC, H2, shown in Figure 7.8 and is fed to IC34-2 via R202 and one section of R89. Feedback, taken from the emitter of Q21 to IC34-2 via R89 pins 5 and 3, makes R89 pin 3 a virtual ground point, and the gain from the R136/R202 junction to the emitter of Q21 is -0.94. A 1 VDC level at the Channel A input and a 1V trigger level, therefore, combine to give 0V at Q21's emitter. Thus, the selected trigger point on the input signal is always brought to 0V at Q21's emitter.

5.3.1.2.10 When Channel A's low-pass filter is selected, RLE is energized. This opens the high-frequency channel circuitry and connects C87 across the low frequency channel. The low-frequency channel bandwidth is then nominally 50 kHz.

5.3.1.2.11 The circuit of Channel B is similar to that of Channel A, but is not provided with a low-pass filter. Energizing RLH connects the signal applied at the Channel A input to both channel amplifiers.

5.3.1.2.12 The relays are controlled by the microprocessor. The voltage levels on the control lines are latched in IC24 as shown in Figure 7.8.

5.3.2 Channel C Block (Model 1992 Only)

5.3.2.1 Functional Description

5.3.2.1.1 Refer to the block diagram given in Figure 5.3. Channel C processes the signal applied at the Channel C input and feeds it to the measurement block.

5.3.2.1.2 Channel C's input is protected by a fuse, mounted in the input connector, and by a signal-limiting circuit. Next is an automatic level control circuit which reduces the range of the signal level applied to the amplifier.

5.3.2.1.3 After amplification, the signal is prescaled by 64 before being passed via a buffer and a signal gate to the measurement block.

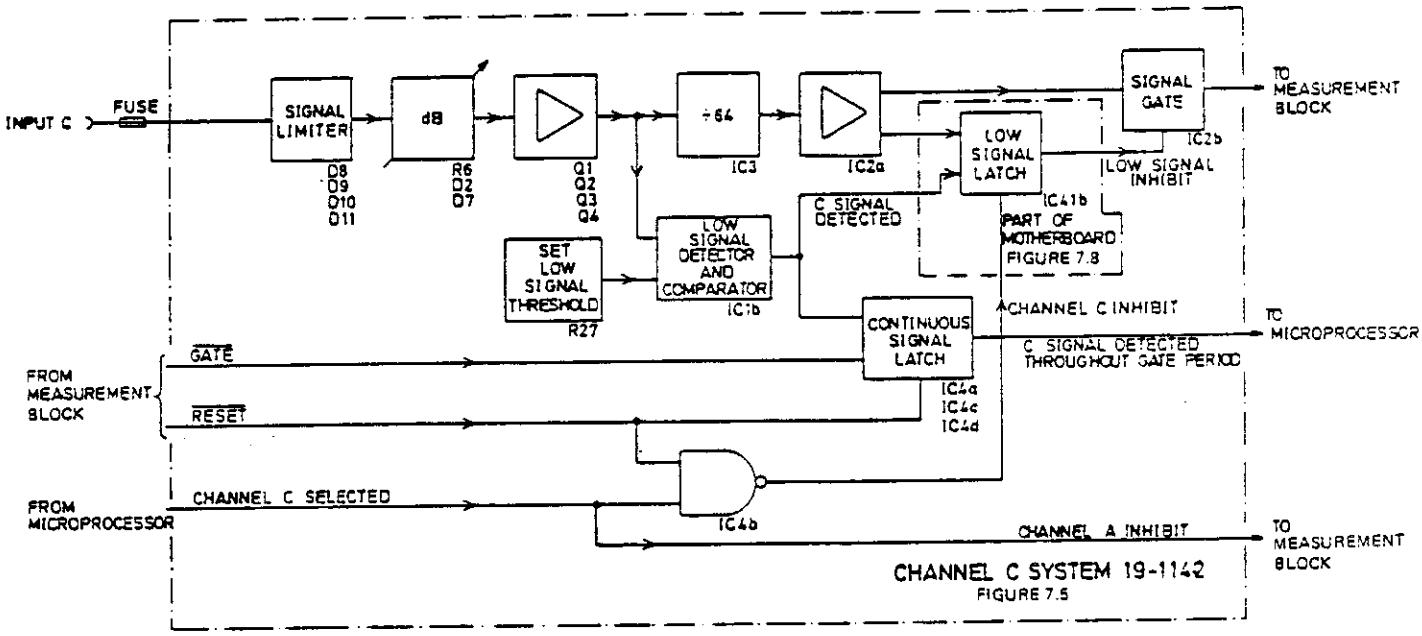


Figure 5.3 - Channel C Block Diagram

5.3.2.1.4 The amplitude of the signal at the amplifier output is monitored by a detector and comparator. The comparator output controls the low-signal latch. If the detector output is below the threshold, the latch is set and the channel output is inhibited by the signal gate. When the detector output goes above the threshold, the low-signal latch is armed and opens the signal gate on the next signal edge from the prescaler. This enables the instrument to make measurements on signal bursts.

5.3.2.1.5 The detector output is also applied to the continuous signal latch. This latch is reset at the beginning of each gate period and is set if the detector output falls below the threshold level. The microprocessor samples the latch output throughout the gate period. If the measured signal falls below the threshold level during this period, the measured result is set to zero.

5.3.2.1.6 If Channel C is not selected, the low-signal latch is held in reset by a control signal from the microprocessor and the output to the measurement block is inhibited. The same control signal is used to enable Channel A so that the two channels cannot be enabled at the same time.

5.3.2.2 Circuit Description

5.3.2.2.1 Refer to the schematic shown in Figure 7.5. The signal to be measured is connected via SK13 (INPUT C). The circuit is protected by a fuse which is mounted within SK13. The signal amplitude is limited by the diode clamp comprised of D8, D9, D10, and D11.

5.3.2.2.2 A degree of automatic gain control is achieved by means of an attenuator, formed by R6 and the impedance of the PIN diodes D2 and D7. The peak-to-peak detector D1, D3, R7, and C48 produces a negative voltage proportional to the signal amplitude. A direct current proportional to this voltage flows through the PIN diodes via L1. The impedance of the diodes decreases if the current increases so that changes in signal amplitude are offset by changes in attenuation.

5.3.2.2.3 The signal passes through four amplifier stages incorporating Q1, Q2, Q3, and Q4. The amplified signal is fed to the counter IC3 via the shaping circuit formed by R37, C46, and R36.

5.3.2.2.4 The signal frequency is prescaled by 64 in IC3 and buffered in IC2a. Provided that Channel C is selected and the amplitude of the signal is adequate, the output at IC2a-2 passes to the measurement block via the gate IC2b and SK7 pin 5.

5.3.2.2.5 The signal at the output of Q4 is fed to the low-signal detector D5 and C23. The comparator IC1b compares the detector output with a threshold voltage set by R27. The comparator output is at logic 1 if the detector output is below the threshold (Channel C's signal amplitude too low for accurate counting).

5.3.2.2.6 The logic level at the comparator output is inverted in IC1-A and is fed via SK7 pin 14 to the D input (pin 10) of the low-signal latch IC41b shown in Figure 7.8. IC41b is clocked by the output of IC2-A via SK7 pin 8. If the signal from Q4 is below the threshold, IC41b-14 goes to logic 1. This level is fed back via SK7 pin 7 to disable the gate IC2-B and inhibit the output to the measurement block.

5.3.2.2.7 The $\overline{\text{GATE}}$ signal enters the system at SK7 pin 17 and is inverted in IC1-C. The resulting signal and the output of the comparator IC1-B are fed to IC4-A. If both inputs are at a logic 1, indicating that the Channel C signal level is too low while the gate is open, the continuous signal latch IC4-C and IC4-D is set. The latch output is fed to the microprocessor via SK7 pin 11 and prevents the result of any measurement made during that gate period from being displayed.

5.3.2.2.8 The U signal at SK7 pin 16 is at a logic 1 when Channel C is selected. A buffered version of this signal is fed to SK7 pin 1 via IC2-C and disables Channel A at IC41a shown in Figure 7.8. When Channel C is not selected, SK7 pin 16 is at logic 0. This level is inverted and buffered in IC4-B and IC1-D, and is then fed to IC41b via SK7 pin 13. IC41b is held in reset, inhibiting the Channel C signal at IC2-B via SK7 pin 7.

5.3.3 Measurement Block

5.3.3.1 Functional Description

5.3.3.1.1 The measurement circuits of the instrument are provided by three custom-built integrated circuits. These are the two Multiple Counter and Control (MCC) circuits, MCC1 and MCC2, and the Timing Error Correction (TEC) circuit. A block diagram is shown in Figure 5.4.

5.3.3.1.2 The circuits within MCC1 and MCC2 are configured by the microprocessor according to the measurement function selected. The reciprocatic counting technique is used. With this technique the measured signal, not the counter clock pulses, controls the start and stop of the measurement period (gate time) as shown in Figure 5.5. The gate time, therefore, extends over an integral number of cycles of the measured waveform. The gate time is measured by counting the clock pulses which occur while the gate is open. This leads to timing errors at both ends of the gate time, as shown. The TEC circuit enhances the measurement accuracy by compensating for these errors.

5.3.3.1.3 For all measurement functions except FREQ A and PERIOD A, the signals to be measured are fed directly to MCC2. For FREQ A and PERIOD A, the Channel A signal is scaled by two and fed to the $\overline{C}$ input of MCC2. When FREQ C is selected, the prescaler is disabled by the CHANNEL A INHIBIT signal from the Channel C block.

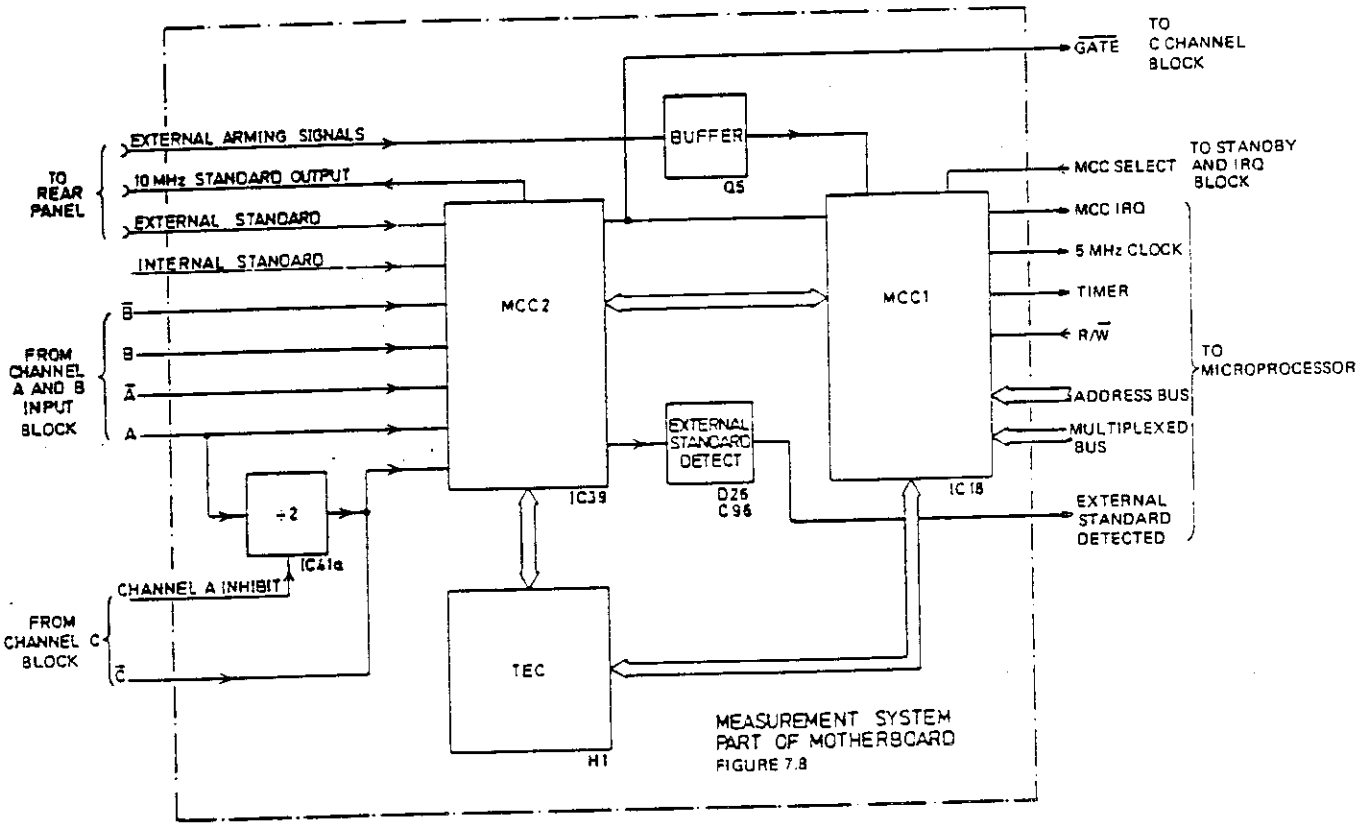


Figure 5.4 - Measurement - Block Diagram

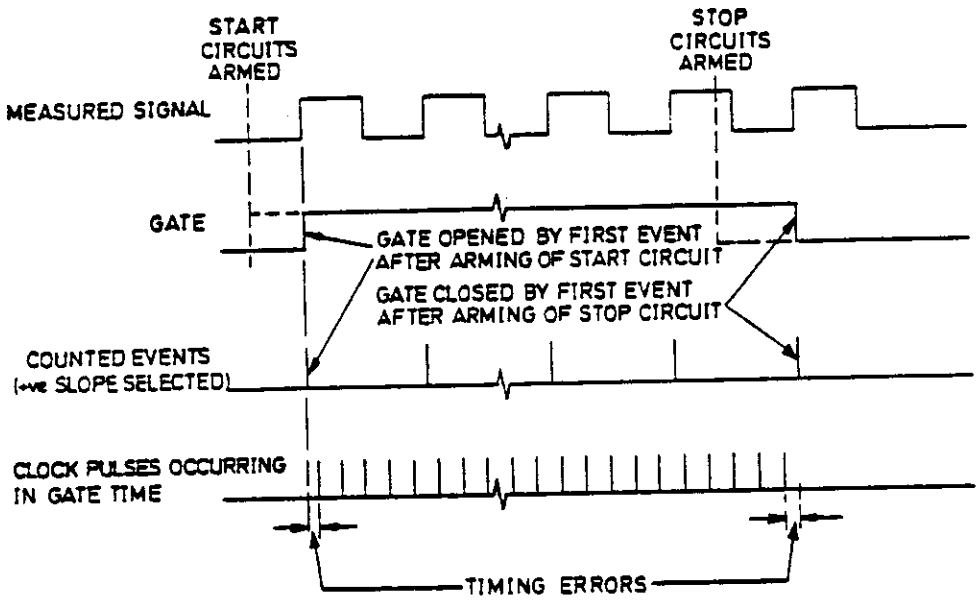


Figure 5.5 - Basic Reciprocmatic Counting Technique

5.3.3.1.4 At the end of each measurement period, MCC1 generates an interrupt request for the microprocessor. The registers within MCC1 are addressed using the address bus and the MCC SELECT line. The measured value is transferred to the microprocessor via the multiplexed bus.

5.3.3.1.5 The internal and external frequency standard inputs are both fed to MCC2. The system will operate from the external standard provided that the input is of sufficient amplitude. A 10 MHz output, derived from the frequency standard in use, is made available at a socket on the rear panel.

5.3.3.2 Circuit Description

5.3.3.2.1 Refer the the schematic shown in Figure 7.8.

5.3.3.2.2 Measured Signal Input

5.3.3.2.2.1 For all measurement functions other than FREQ A and PERIOD A, the differential outputs from Channel A and Channel B are applied to the measuring circuit at IC39-15, 16, 17 and 18. For the FREQ A and PERIOD A functions, the A signal frequency is divided by two in IC41a and fed to IC39-19.

5.3.3.2.2.2 For the FREQ C and RATIO C/B functions, the $\overline{C}$ signal is fed to IC39-19. For these functions IC41a-5 is held at logic 1 by the PST1 control line (CHANNEL A INHIBIT) from the Channel C block. As a result, IC41a is held in set and the A signal is inhibited from reaching IC39-19.

5.3.3.2.3 Reference Frequency

5.3.3.2.3.1 The internal reference signal is applied to IC39-2 and the external reference signal, if present, to IC39-3. A buffered version of the external reference is present at IC39-24 and is applied to the detector D26, C96, and R129. The detector output is fed to IC23-6 and is read periodically by the microprocessor. If the level is above the TTL logic 1 threshold, the microprocessor sets IC39-38 to logic 0 and the measurement block switches to use the external reference.

5.3.3.2.3.2 A 10 MHz signal, derived from the frequency standard, is present at IC39-37 and is fed to the 10 MHz STD OUTPUT socket on the rear panel via PL19 pin 2.

5.3.3.2.3.3 A 10 MHz reference signal, derived from the frequency standard, is present at IC39-36. This signal is applied to the TEC, H1, at pin 6, and, after inversion in IC29e, to IC18-24.

5.3.3.2.4 Microprocessor Clock and Timer

5.3.3.2.4.1 A 5 MHz clock signal for the microprocessor (and the GPIB microprocessor if installed) is taken from IC18-2. A 39.0625 kHz clock signal for the microprocessor timer is taken from IC18-4.

5.3.3.2.5 Channel C Gate and Reset

5.3.3.2.5.1 A $\overline{\text{GATE}}$ signal (logic 0 during the measurement period) and a $\overline{\text{RESET}}$ signal (negative-going pulse at the end of each measurement period) are taken from IC39-27 and IC18-40 and fed to the Channel C block via PL7 pins 17 and 15.

5.3.3.2.6 External Arming Input

5.3.3.2.6.1 Signals connected to the EXT ARM INPUT socket on the rear panel are fed to IC18-27 via PL19 pin 1 and the amplifier stage Q5.

5.3.3.2.7 Control Signals

5.3.3.2.7.1 The logic levels on lines Q0 to Q4, between IC18 and IC39 are shown in Table 5.1. These levels are stable if the following conditions exist:

a. No signals are applied to any of the channel inputs

b. Auto-trigger is disabled on Channels A and B

Table 5.1 - Control Logic Levels by Function

Measurement	Control Line				
Function:	Q0	Q1	Q2	Q3	Q4
FREQ A	1	1	0	1	0
PERIOD A	1	1	0	1	0
FREQ B	1	0	0	1	0
PERIOD B	1	0	0	1	0
FREQ C	1	1	0	1	0
T.I. A→B	0	0	1	1	0
T.I. B→A	0	0	0	1	0
TOTAL A by B	1	0	0	1	1
TOTAL B by A	1	0	1	1	1
RATIO C/B	1	1	0	1	1
RATIO A/B	1	0	1	1	1
Special Function 72	1	1	1	0	1
Special Function 73	1	1	1	0	0
Special Function 74	1	1	1	0	1
Special Function 75	1	1	1	0	0

NOTES:

a. The FREQ B, PERIOD B, TOTAL B by A, and T.I. B→A functions are obtained using Special Function 21.

b. Special Functions 72 to 75 can only be used when CHECK is selected.

5.3.4 Display Block

5.3.4.1 Functional Description

5.3.4.1.1 A simplified diagram of the display block is given in Figure 5.6. The GPIB LEDs, GATE LED, Channels A and B TRIGGER LEDs, and the STANDBY LED are held on or off by control signals from other systems. The remainder of the display is multiplexed under the control of the display drivers.

5.3.4.1.2 To update the display, the microprocessor selects the appropriate display driver using the MODE 1 and MODE 2 control lines. A string of nine 8-bit words (a control word and eight data words) is then put onto the bus. Each word is entered into a memory within the display driver under the control of the STROBE signal.

5.3.4.1.3 The display driver then sequentially puts the data words onto its output bus. For each data word, the appropriate numeric indicator or group of LEDs is enabled by a signal on its control line.

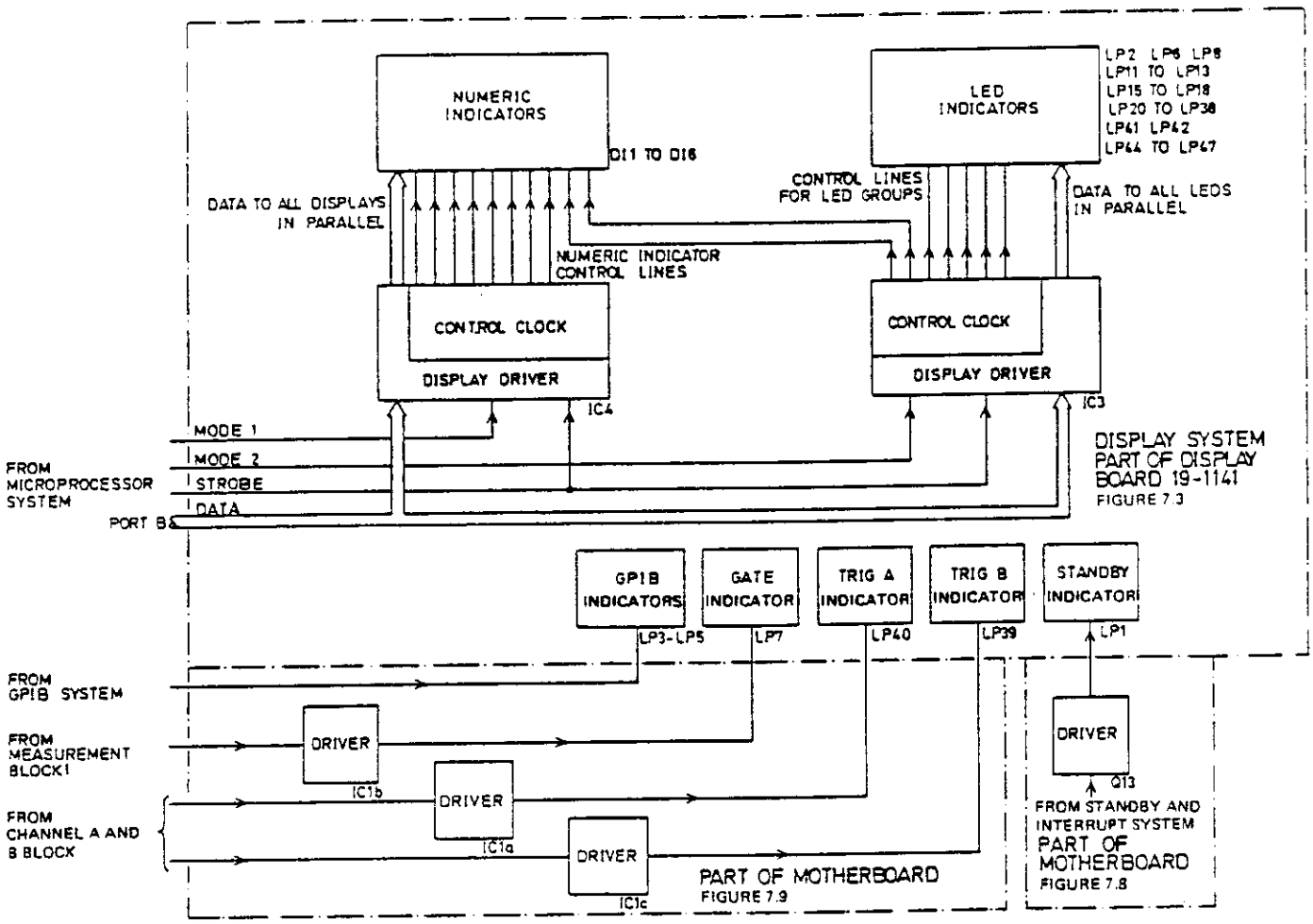


Figure 5.6 - Display-Block Diagram

5.3.4.2 Circuit Description

5.3.4.2.1 The schematic is shown in Figure 7.3. The GPIB LEDs LP3, LP4, and LP5 are driven via SK1 from the GPIB system. The GATE LED LP7 is driven from the measurement block via a driver stage, shown in Figure 7.9, and SK2 pin 11. The TRIG LEDs LP39 and LP40 are driven from the Channel A/B block via driver stages, shown in Figure 7.9, and SK2 pins 7 and 3. The STANDBY LED LP1 is driven via SK1 pin 8 from the standby and interrupt block. The remaining LED indicators and the numeric indicators DI5 and DI6 are controlled by the display driver IC3. Numeric indicators DI1 to DI4 are controlled by IC4.

5.3.4.2.2 Display data is stored in memory within IC3 and IC4. To change the data, the microprocessor puts a control word on the port B bus. The microprocessor writes this word into the display driver by means of a negative pulse applied to the DISPLAY STROBE line at SK1 pin 4. The control word determines the operating mode of the display drivers.

5.3.4.2.3 The microprocessor then selects the display driver required by setting a logic 0 on the appropriate MODE line at SK1 pin 3 or 6. Eight words containing display data are written into the selected display driver via the port B bus, controlled by eight negative-going pulses on the DISPLAY STROBE line.

5.3.4.2.4 The output of each display driver is multiplexed under the control of an internal clock. Eight-bit display data (for seven segments + decimal point or eight LED indicators) are put onto the device output bus (pins 1 to 4 and 24 to 27). A positive pulse is then applied to the enablement line of the device or group of indicators which is to display the data. The enablement line waveforms consist of 500 μs positive-going pulses at approximately 250 pps.

5.3.5 Keyboard Block

5.3.5.1 Functional Description

5.3.5.1.1 A simplified diagram of the keyboard block is given in Figure 5.7. The encoding of the keyboard data is performed within the system without microprocessor action. An interrupt request (IRQ) is made to the microprocessor when encoding is complete. Data transfer is initiated by the KEYBOARD ENABLE signal from the microprocessor.

5.3.5.1.2 The 32 keys are divided into two 16-key matrices. When a key is pressed, its position is encoded into a 5-bit word. One bit, carried on the $\overline{\text{KEYBOARD EXTEND}}$ line, indicates the matrix in which the key is located. The remaining bits indicate the position of the key within the matrix.

5.3.5.1.3 When a key is pressed, the encoder examines both matrices simultaneously and generates a 4-bit code representing the key position. The same four bits are generated regardless of the matrix in which the key is located.

5.3.5.1.4 If the key pressed is in the extended key matrix, one of the inputs to the NAND gate is pulled low. The $\overline{\text{KEYBOARD EXTEND}}$ line is then set to logic 0. If the key is in the non-extended matrix, the inputs to the NAND gate are isolated from the key line by one of the diodes and the $\overline{\text{KEYBOARD EXTEND}}$ line remains at logic 1.

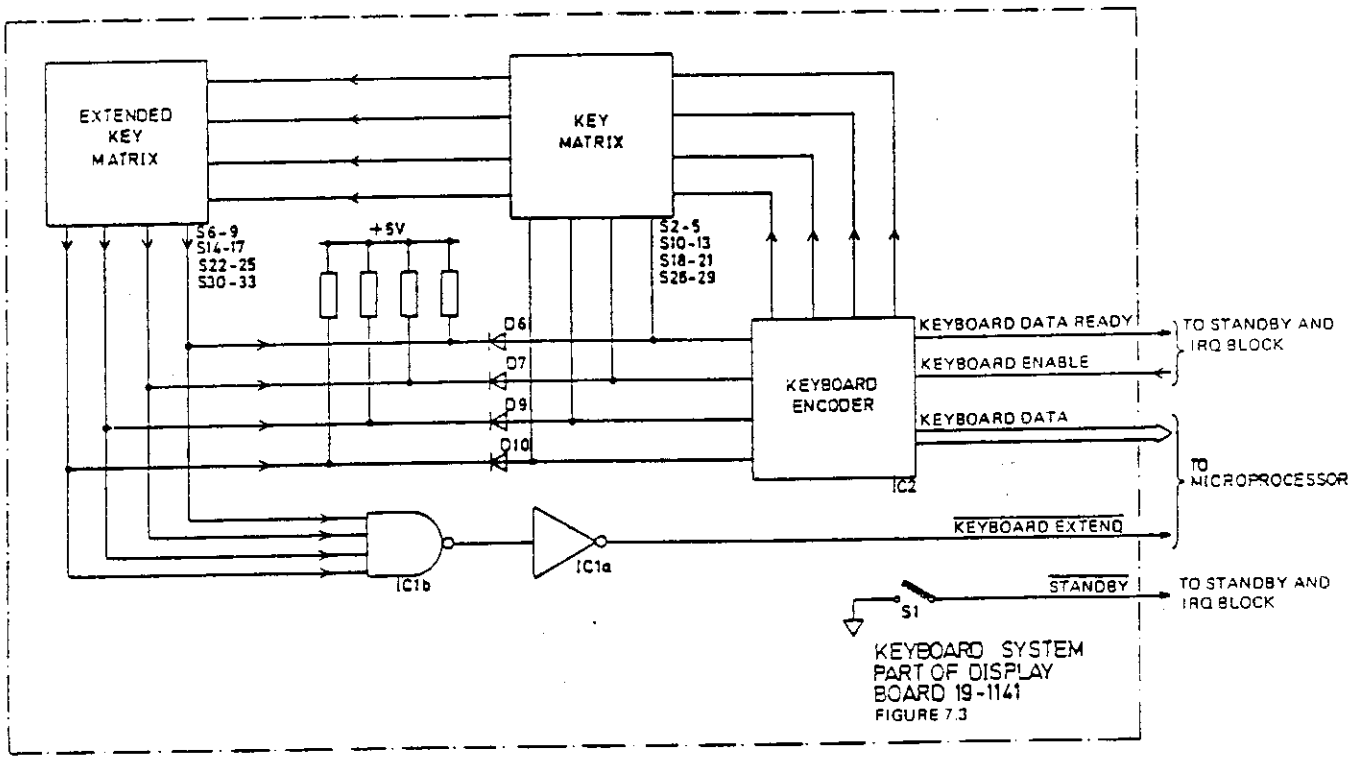


Figure 5.7 - Keyboard-Block Diagram

5.3.5.2 Circuit Description

5.3.5.2.1 The schematic is given in Figure 7.3. The keys are divided into two 16-key matrices having common row lines connected to the encoder at IC2-7, 8, 10, and 11. The matrices have separate column lines connected in pairs to IC2-1, 2, 3, and 4.

5.3.5.2.2 The encoder normally holds the row lines at logic 0. When a key is pressed. the corresponding column line is pulled to logic 0. The encoder then scans the keyboard and stores a 4-bit code, corresponding to the row and column of the key, in an internal register. Because the column lines are connected to the encoder in pairs, it cannot find which matrix contains the key.

5.3.5.2.3 The $\overline{\text{KEYBOARD EXTEND}}$ line indicates which matrix contains the key that is pressed. The inputs to IC1b are normally held at logic 1 so that SK2 pin 9 is at logic 1. If a key in the extended matrix (column lines connected directly to the inputs of IC1b) is pressed, one input of IC1b is pulled to logic 0 and SK2 pin 9 will go to logic 0. The column lines of the other matrix are isolated from the inputs of IC1b by D6, D7, D9, and D10, so that the logic level at SK2 pin 9 is not changed when a key in this matrix is pressed.

5.3.5.2.4 When the key-position code has been stored, the encoder sets the KEYBOARD DATA READY line, at SK2 pin 4, to logic 1 giving a microprocessor interrupt. The microprocessor sets IC2-13 to logic 0 using the KEYBOARD ENABLE line, and the encoder puts the 4-bit code onto the bus. The microprocessor reads the code and the state of the KEYBOARD EXTEND line to determine which key has been pressed.

5.3.6 Microprocessor Block

5.3.6.1 Functional Description

5.3.6.1.1 A simplified diagram of the microprocessor block is given in Figure 5.8. The microprocessor used has a 5-bit bus for the high-order address bits and an 8-bit multiplexed bus which is used for the low-order address bits and for data. The low-order address bits are strobed into the address latch, which holds them on an 8-bit address bus, to free the multiplexed bus for data.

5.3.6.1.2 Two latches, fed from port B of the microprocessor, are used to maintain voltage levels on the instrument control lines. A third latch is used to read the status of the instrument flags via port B. The latches and registers for the connection of the multiplexed bus to the measurement system are in the measurement block, and are controlled by the MCC SELECT signal. The display data latches are in the display block, and are controlled by strobe and chip select signals obtained from port A.

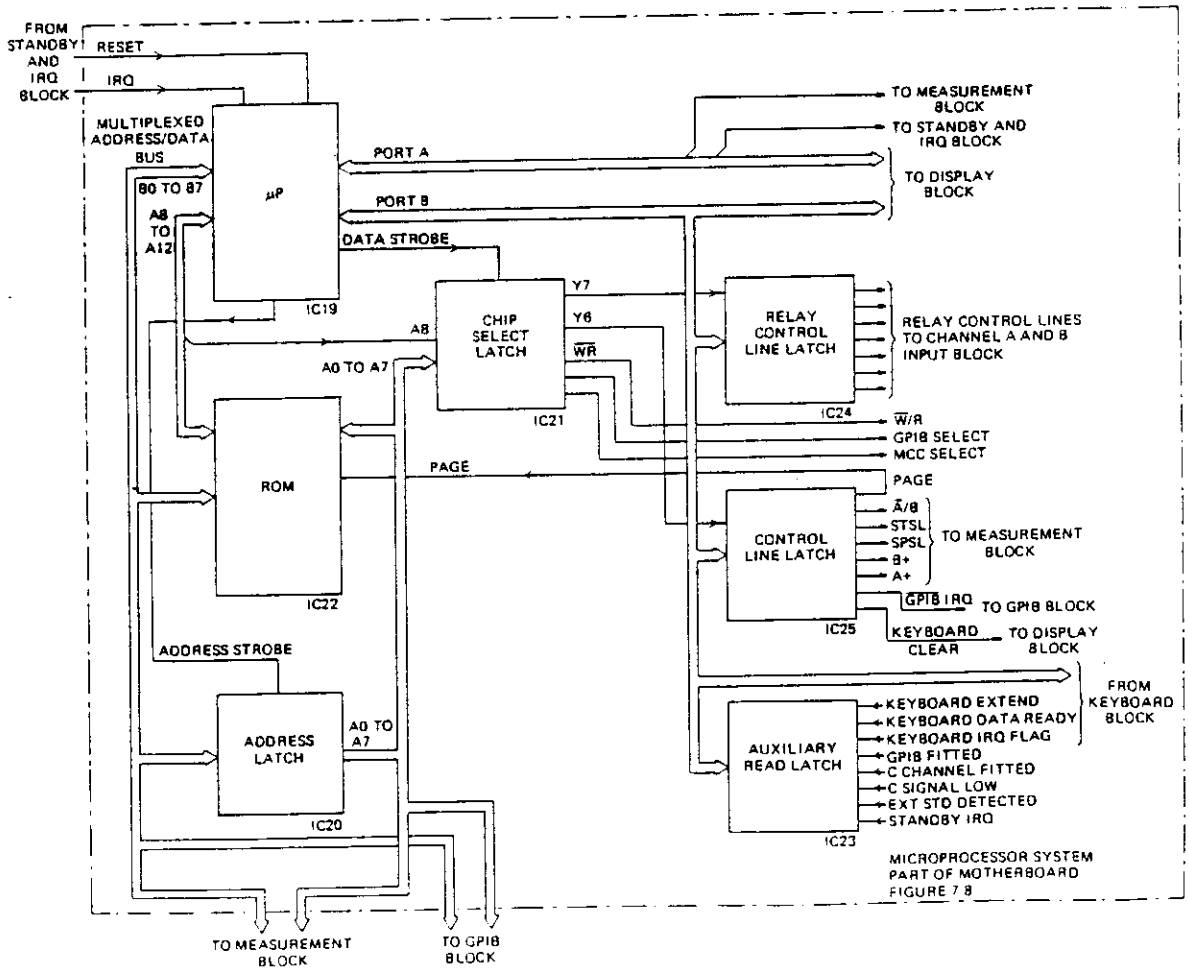


Figure 5.8 - Microprocessor-Block Diagram

5.3.6.2 Circuit Description

5.3.6.2.1 The schematic is given in Figure 7.8. The microprocessor clock and timer signals are generated in the measurement block and are fed to IC19-39 and IC19-37. A $\overline{\text{RESET}}$ signal is generated in the standby and IRQ block when the instrument is switched on or off and is fed to IC19-1.

5.3.6.2.2 The microprocessor bus for the high-order address bits is designated A8 to A12. The multiplexed bus, used for the low-order address bits and for data is designated B0 to B7. The microprocessor also has two input/output ports PA0 to PA7 and PB0 to PB7.

5.3.6.2.3 Multiplexed Bus Operation

5.3.6.2.3.1 The microprocessor puts IC19-6 (ADDRESS STROBE) at logic 1 and (DATA STROBE) at logic 0. This enables the address latch IC20 (IC20-11 at logic 1), disables ROM IC22 (IC22-20 at logic 1), and disables the address decoder IC21 (IC21-6) at logic 0).

5.3.6.2.3.2 This address is put onto lines B0 to B7 and A8 to A12. When the lines have settled, the ADDRESS STROBE line is taken to logic 0. The low-order bits of the address are latched into IC20 and are held on address lines A0 to A7. Lines B0 to B7 are now free for use as a data bus.

5.3.6.2.4 Address Decoding

5.3.6.2.4.1 The levels on address lines A6 to A12 are decoded in IC21 to provide the following outputs:

a. $\overline{\text{MCC SEL}}$, the chip-select signal for IC18

b. $\overline{\text{GPIB SEL}}$, the chip-select for the GPIB address decoder

c. $\overline{\text{WR}}$, the write control signal for H2

d. Y6, the chip select signal for output latch IC25

e. Y7, the chip select signal for output latch IC24

5.3.6.2.4.2 These outputs are only available when IC21 is enabled by a logic 1 at IC21-6 and a logic 0 at IC21-4,5. The level at IC21-6 is set by the DATA STROBE output at IC19-4, which is at logic 1 when the multiplexed bus is available for data transfer. All outputs from IC21 are decoded from addresses with lines A9 to A12 at logic 0 when IC21-4, 5 are held at logic 0 by the output from IC27a, b, and d.

5.3.6.2.5 Input and Output Latches

5.3.6.2.5.1 The logic levels required on the instrument control lines and on the PAGE line (most significant bit of RAM address) are set into the output latches IC24 and IC25 from data port B of the microprocessor. The latch strobe signals are decoded in IC21. Data may be read by the microprocessor from the input latch IC23. The latch strobe signal is provided via data port A of the microprocessor.

5.3.7 Standby and IRQ Block

5.3.7.1 Functional Description

5.3.7.1.1 This block generates reset signals for the microprocessor and GPIB interface, and the standby switching signal for the power supply system. It also combines the IRQ signals from the GPIB interface, the measurement block, and the keyboard block for connection to the microprocessor. A block diagram is given in Figure 5.9.

5.3.7.1.2 Reset signals for the microprocessor and the GPIB interface are generated whenever power is applied to or removed from the instrument's power supply system.

5.3.7.1.3 On switching to standby, the standby signal from the keyboard block sets the standby IRQ latch. The latch outputs provide the standby IRQ and a standby flag for the microprocessor. The standby IRQ output also clocks the standby ON/OFF latch to the set state. This provides signals to switch the power supply to standby, light the STANDBY LED, and disable IC30b, thereby inhibiting the other IRQs. At the end of the microprocessor interrupt routine, the standby IRQ latch is reset, removing the standby IRQ. The state of the standby ON/OFF latch is not changed.

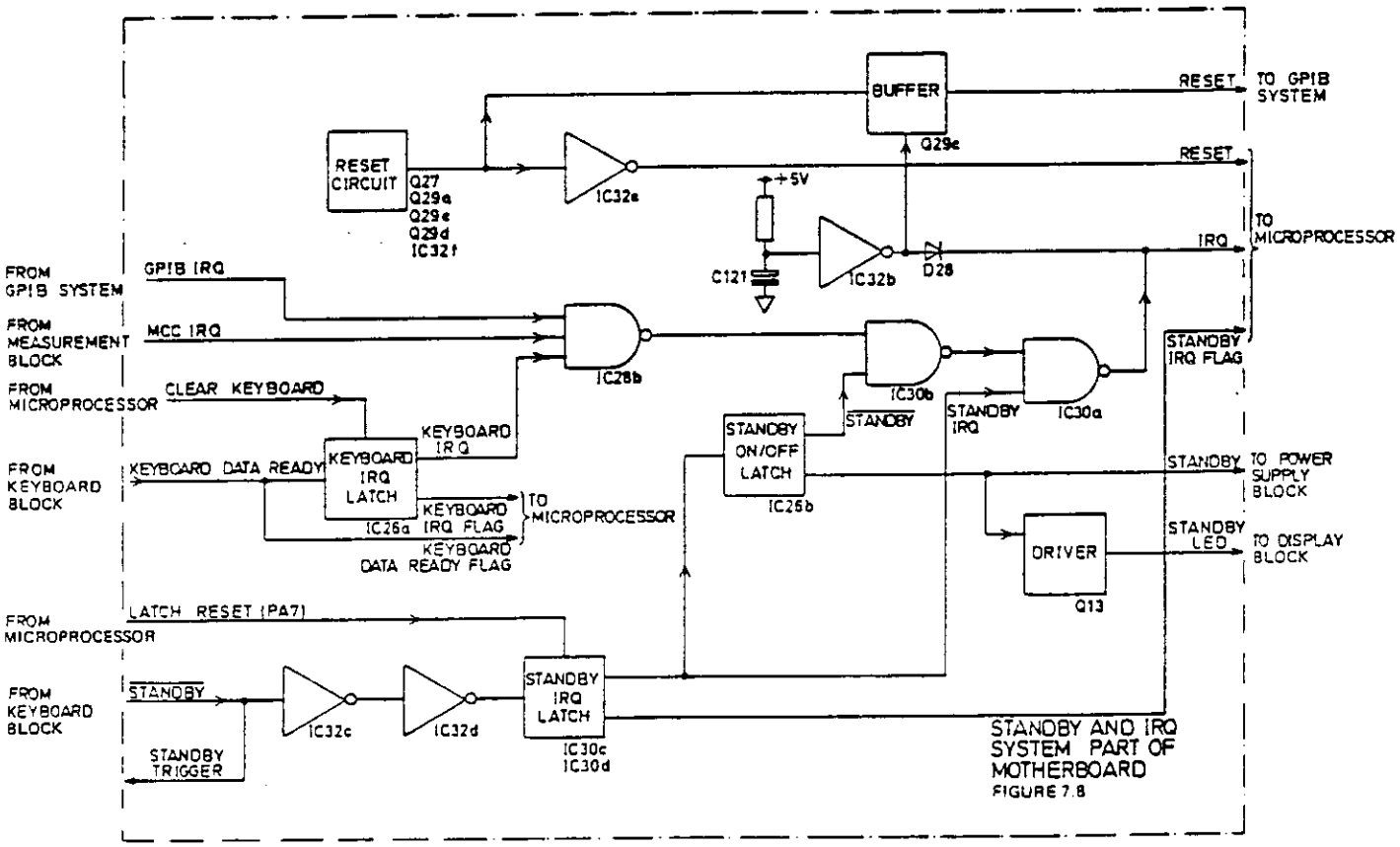


Figure 5.9 - Standby and IRQ Block Diagram

5.3.7.1.4 While the instrument is in standby, the input to IC32b is held low and the IRQ input to the microprocessor is held high via D28. This inhibits all IRQs. The output from IC32b also holds the GPIB interface in reset via Q29c.

5.3.7.1.5 On return from standby, the standby IRQ latch is again set by the standby signal from the keyboard block. The standby ON/OFF latch is clocked to the reset state, the power supply is returned to normal operation, and IC30b is enabled. The input to IC32b rises as C121 charges, removing the reset signal from the GPIB interface and enabling the microprocessor IRQ input. The microprocessor is now able to accept the IRQ from IC30a. At the end of the restart sequence, the standby IRQ latch is reset.

5.3.7.1.6 When the encoder in the keyboard system has data ready to be read by the microprocessor, the keyboard IRQ latch is clocked via the KEYBOARD DATA READY line. The latch outputs provide the keyboard IRQ and a keyboard IRQ flag. Once the keyboard has been identified as the source of the interrupt, the latch is reset by the microprocessor.

5.3.7.2 Circuit Description

5.3.7.2.1 The schematic is shown in Figure 7.8.

5.3.7.2.2 Reset Circuit

5.3.7.2.2.1 The $\overline{\text{RESET}}$ signal is generated in the circuit containing Q27, Q29a, d, and e, and C125. When the instrument is switched on, the input to IC32f is held low until C125 charges through R215, Q29a, and R216. The output at IC32f-12 goes to logic 1 when power is applied, but drops to logic 0 after approximately 500 ms. This output is inverted by IC32e to provide the microprocessor reset and by Q29c to provide the GPIB reset.

5.3.7.2.2.2 If there is a reduction in the +5V STANDBY supply, due to the instrument being switched off or to power failure, the potential across R217 falls. The potential at Q27 emitter is maintained by the charge in C125, so Q27 conducts. The current in R218 makes the base of Q29d positive, so the transistor conducts and holds the base of Q27 low until C125 is completely discharged. This ensures that a good reset action is obtained, even if the power is quickly restored.

5.3.7.2.3 Standby Operation

5.3.7.2.3.1 On switching to standby, PL1 pin 14 is taken to 0V by the STANDBY key. Debouncing is provided by R158 and C126. The leading edge of the signal is sharpened in IC32c, C118, R151, and IC32d, and sets the standby IRQ latch IC30c, d.

5.3.7.2.3.2 The negative-going output from IC30c-10 is passed via IC30a, IC32a, and R152 to IC19-2 to provide a microprocessor interrupt. The positive-going output from IC30d-11 forms the standby IRQ flag (read by the microprocessor via IC23 during the interrupt routine) and clocks the standby latch IC26b to the set state.

5.3.7.2.3.3 The logic 0 level at IC26b-8 switches on Q13 and provides power for the STANDBY LED via PL1 pin 8. The same output is applied to IC30b-5 and disables the other interrupts which are connected to IC30b-6.

5.3.7.2.3.4 The logic 1 level at IC26b-9 shuts down the power supplies except the +5V STANDBY supply.

5.3.7.2.3.5 At the end of the interrupt routine, the microprocessor resets the standby IRQ latch by applying logic 1 to IC30c-8 from IC19-7.

5.3.7.2.3.6 On return from standby, the standby IRQ latch is again set. This provides a microprocessor interrupt and sets the standby IRQ flag as before. The positive-going output from IC30d-11 clocks the standby latch back to the reset state, so that the STANDBY LED is turned off and the power supplies are restored. The microprocessor resets the standby IRQ latch at the end of the interrupt routine.

5.3.7.2.4 The IRQ Circuits

5.3.7.2.4.1 The KEYBOARD DATA READY line at PL2 pin 4 goes to logic 1 when the keyboard encoder has data available. This clocks IC26a to the set state to provide a keyboard IRQ flag at IC23-11 and an interrupt signal at IC28b-9. Interrupts from the measurement system ($\overline{\text{MCC IRQ}}$) and the GPIB interface ($\overline{\text{GPIBIRQ}}$) are connected to IC28b-12 and IC28b-10, 13.

5.3.7.2.4.2 If any of these interrupts occur, IC28b-8 and IC30b-6 will go to logic 1. Provided the standby latch IC26b is not set, IC30b-5 will be at logic 1 and the interrupt signal passes via IC30a and IC32a to IC19-2.

5.3.7.2.4.3 When the instrument is switched into or out of the standby state, the standby IRQ latch IC30c, d is set. The standby IRQ from IC30c-10 is fed to IC19-2 via IC30a and IC32a.

5.3.7.2.4.4 The circuit comprising R220, C121, IC32b, and D28 disables the microprocessor interrupt input and holds the GPIB microprocessor reset line low (via Q29c), while the +5V power supply to R220 is switched off. On return from standby, C121 charges and IC32b-4 goes to logic 0. The microprocessor interrupt input is enabled and the GPIB microprocessor is reset. The delay in enabling the interrupts prevents the standby IRQ, which occurs on return from standby, from being acted upon before the power supplies are fully restored.

5.3.8 Power Supply Block

5.3.8.1 Functional Description

5.3.8.1.1 A simplified diagram of the power supply block is given in Figure 5.10. The AC supply enters at a plug mounted on the rear panel and passes via a fuse and RFI filter, mounted on the motherboard, to the line switch.

5.3.8.1.2 The switched supply is connected to the primary winding of the power transformer via the operating-voltage range selector. The voltage range selector is a small plug-in printed circuit board which is positioned according to the desired line voltage.

5.3.8.1.3 The transformer has a tapped secondary winding which supplies two bridge rectifiers. The smoothed but unregulated outputs from the rectifiers feed regulators providing +11.2V, -11.2V, +5V, +5V and -5.2V. The -5.2V regulator and one of the +5V regulators, which supply most of the instrument's circuits, are shut down by a signal from the microprocessor when the instrument is switched to standby.

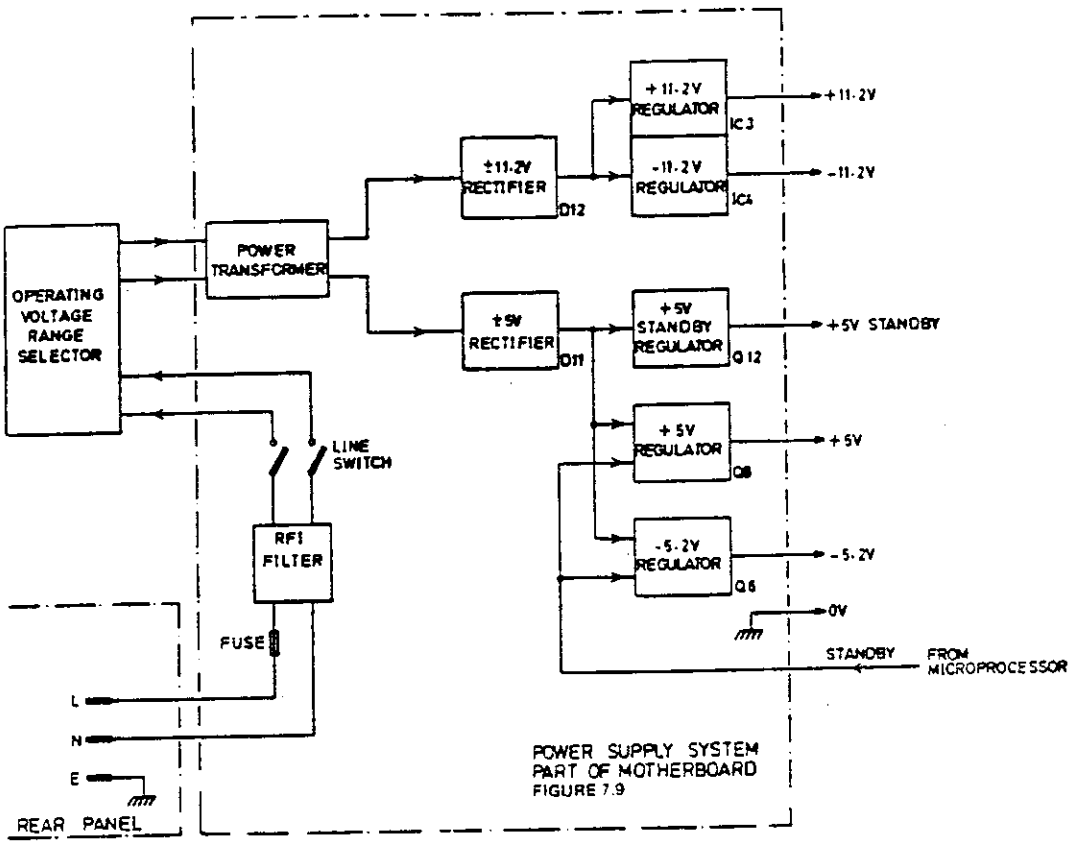


Figure 5.10 - Power-Supply-Block Diagram

5.3.8.2 Circuit Description

5.3.8.2.1 The schematic is shown in Figure 7.9. AC power connected at the power input plug passes via fuse FS1 and the RF filter, formed by L1, L2, C46, C47, and C48, to the POWER switch S1b. The switched supply is connected to the primary windings of transformer T1 via the tracks of a printed circuit board which is inserted in SK8.

5.3.8.2.2 The secondary windings of transformer T1 supply the ±5V rectifier D11, C49 and C50, and the ±11V rectifier D12, C52, and C59.

5.3.8.2.3 Regulated supplies at ±11.2V are provided by the regulators IC3 and IC4. The common terminals of these regulators are held at approximately -0.7V and +0.7V by diodes D13 and D14.

5.3.8.2.4 Regulated supplies at +5V are provided by two discrete component regulators having series elements Q8 and Q12. The non-inverting inputs to the comparators IC31a and IC31c are connected to a +2.5V reference voltage, derived in the hybrid circuit H2 shown in Figure 7.8. Potential dividers formed by elements of R49 hold each inverting input at half the output voltage of the associated regulator.

5.3.8.2.5 A regulated supply at -5.2V is provided by a discrete component regulator having Q6 as its series element. The comparator inputs are held at approximately 0V. The potential divider controlling the inverting input is connected across the +5V and -5.2V supplies.

5.3.8.2.6 Standby Mode

5.3.8.2.6.1 When the instrument is switched to standby, the standby latch IC26b (see Figure 7.8) is clocked to the set state. The base of Q11 is pulled high and IC31a-3 is pulled low. The base of Q9 is pulled low by IC31a, the base current of Q8 is cut off, and the regulator is shut down. When the voltage of the +5V supply falls, IC31b-6 goes more negative. The base of Q7 is taken towards 0V by IC31b so that the base current of Q6 is cut off and the -5.2V regulator is shut down.

5.3.9 Internal Frequency Standard Block

5.3.9.1 Functional Description

5.3.9.1.1 The internal frequency standard consists of a 5 MHz oscillator and a frequency doubler. A block diagram of the internal frequency standard is shown in Figure 5.11.

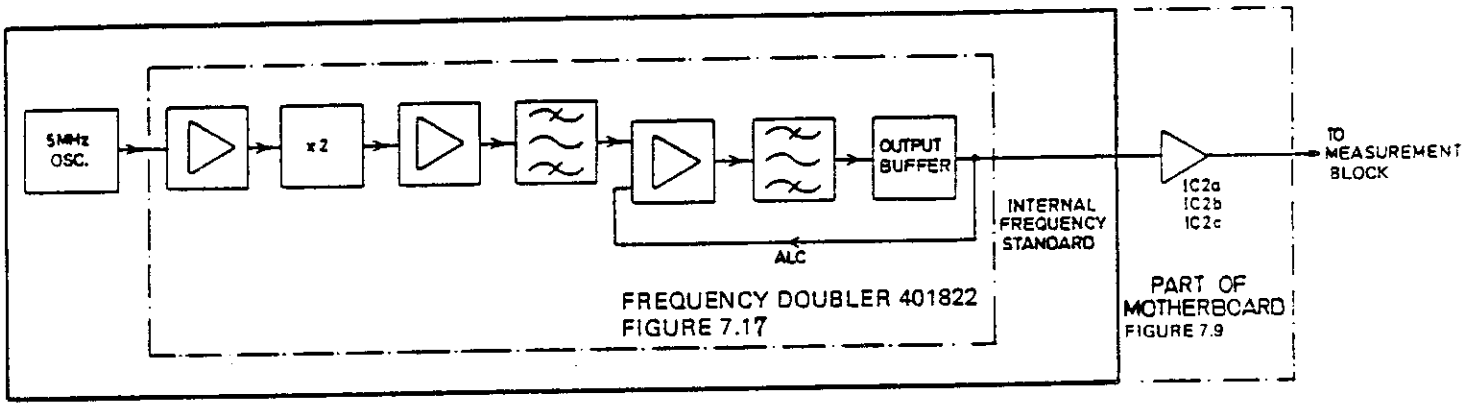


Figure 5.11 - Internal Frequency Standard Block Diagram

5.3.9.1.2 The 10 MHz signal is passed to the measurement block via a buffer (IC2) on the motherboard.

5.3.9.1.3 Signals from an external frequency standard are applied to a signal conditioning circuit on the motherboard. If a 10 MHz external frequency standard is used, the output of this circuit is connected directly to the measurement circuitry.

5.3.9.2 Circuit Description

5.3.9.2.1 Frequency Doubler

5.3.9.2.1.1 The schematic of the frequency doubler, used with the internal frequency standard is given in Figure 7.18. The 5 MHz input is applied to the balanced amplifier containing Q1 and Q2. The base of Q3 is driven by the differential outputs from the amplifier via D1 and D2 so that the frequency here is 10 MHz.

5.3.9.2.1.2 The 10 MHz signal is amplified and filtered in the two stages containing Q3 and Q5, and fed to pin 3 via buffer Q6.

5.3.9.2.1.3 The output signal is fed back via C6 to switch Q4 on during the positive peaks of the signal. The gain of Q5 is controlled by the potential across C3 which charges via R12 and discharges via Q4. If the output signal increases, the time for which Q4 conducts increases so that the mean potential across C3 decreases. The resulting decrease in gain of Q5 provides automatic level control.

5.3.9.2.2 Internal Frequency Standard Buffer

5.3.9.2.2.1 The buffer circuit is shown in Figure 7.9. The 10 MHz input at PL14 pin 4 is shaped and buffered in IC2a, IC2b, and IC2c before being fed to the measurement block at IC39-2. The inverting inputs of IC2 are connected to the bias voltage at IC2-11.

5.3.9.2.3 External Frequency Standard Buffer

5.3.9.2.3.1 The buffer circuit is shown in Figure 7.9. The signal connected to the EXT. STD. INPUT socket on the rear panel is fed to PL20 pin 4. Protection against excessive signal amplitude is provided by D6, D7, and R32.

5.3.9.2.3.2 The buffer comprises IC14a, IC14b, and IC14c. The inverting inputs are connected to the bias voltage at IC14-11. The final stage has feedback connected via R11 to give a Schmitt trigger action.

5.3.9.2.3.3 Link LK1 is fitted between pins 8 and 9 of the PL16 to connect the differential output of the final stage to the measurement block at IC39-3.

5.3.10 GPIB Interface

5.3.10.1 Introduction

5.3.10.1.1 The GPIB interface is a self-contained, microprocessor-controlled system. It handles the transfer of data between its internal memory and the GPIB without involving the main instrument's microprocessor. Data transfer is made one byte at a time, each transfer being controlled by the IEEE-488 handshake protocol. Refer to the schematic in Figure 7.12.

5.3.10.1.2 The microprocessor $\overline{\text{RESET}}$ signal is derived from the standby and IRQ block. The clock signal is derived from MCC1, IC18, shown in Figure 7.8.

5.3.10.1.3 The microprocessor uses a multiplexed bus, the eight low-order bits being used for both address and data. The low-order address bits are put onto the bus first and are latched into IC11 by the address strobe. The bus is then free for data use.

5.3.10.1.4 Data transfer between the microprocessors is initiated by an interrupt and is controlled by a 3-wire handshake protocol. The transfer is in the form of a data string, the number of bytes in the string being indicated by the first byte.

5.3.10.2 Address Setting and Recognition

5.3.10.2.1 The microprocessor reads the settings of the address switches in switchbank S1, via its port B inputs, approximately every 1 ms and writes the settings into an address register within the general purpose interface adapter (GPIA) IC12.

5.3.10.2.2 When the interface address is set on the bus by the controller, it is recognized by the GPIA by comparison with the contents of the internal address register.

5.3.10.3 Reading from the Bus

5.3.10.3.1 When the interface is addressed to listen, the GPIA conducts the handshake procedure up to the point where the ready for data (RFD) indication is given. At this point IC12-27 is at logic 0, giving a logic 1 level at IC18-11. This puts three of the bilateral switches of IC13 into the conducting state, thus completing the RFD line. The logic 0 at IC12-27 also puts the buffers in IC14 and IC15 into the receive condition. Data from the bus enters the GPIA data-in register and IC12-40 goes to logic 0 providing an interrupt request to the microprocessor IC9.

5.3.10.3.2 The microprocessor interrupt routine establishes the reason for the interrupt. The address decoder IC8 is enabled via IC27-15, IC26-8, and A7. The decoder is addressed using lines GA4, 5, and 6, and gives the GPIA enable signal at IC8-15. The data-in register of the GPIA is addressed using the R/$\overline{W}$ line and lines A0, 1, and 2. The microprocessor then reads the contents of the data-in register and transfers the data to memory.

5.3.10.3.3 When the data-in register has been read, the GPIA cancels the interrupt request and allows the data accepted (DAC) line to go high. The handshake routine then continues, and a further byte, if available is loaded into the data-in register. The interrupt and data transfer sequence is then repeated.

5.3.10.4 Writing to the Bus

5.3.10.4.1 When the GPIA is addressed to talk, its internal data-out register will normally be empty. Under these conditions IC12-40 goes to logic 0 and provides an interrupt request to the microprocessor.

5.3.10.4.2 IC17B is in the reset state, giving a logic 1 at IC18-12. Since IC12-27 is at logic 1 when the GPIA is addressed to talk, IC18-13 is also at logic 1. The resulting logic 0 at IC18-11 opens three circuits of bilateral switches in IC13 to break the RFD line. The fourth bilateral switch conducts, due to the logic 1 at IC19-10, and holds IC12-18 at 0V. Even if the listening device asserts that it is ready for data, IC12 will not attempt to load the contents of the data-out register onto the bus.

5.3.10.4.3 The microprocessor interrupt routine establishes the reason for the interrupt. The microprocessor then enables the address decoder, IC8, via IC27-15, IC26-8, and A7. The decoder is addressed using lines GA4, 5, and 6, and gives the GPIA enable signal at IC8-15. The data-out register of the GPIA is addressed using the R/$\overline{W}$ line and lines GA0, 1 and 2, and a data byte is written into the register. The GPIA then cancels the interrupt request.

5.3.10.4.4 Following the data transfer, the microprocessor sets IC17B, using line PB7, to give a logic 0 at IC18-12. This gives a logic 1 at IC18-11, which enables three bilateral switches in IC13 and connects the RFD line. The fourth switch in IC13 is disabled, thereby releasing IC12-18 from 0V. When the listening device asserts that it is ready for data, the GPIA loads the contents of the data-out register onto the bus and continues with the handshake routine.

5.3.10.4.5 When the data-out register has been read, the GPIA generates a further interrupt request. The microprocessor resets IC17B, using line PB6, giving a logic 1 at IC18-12 so that the RFD line is again broken at IC13. The data transfer and data transmission sequence is then repeated.

5.3.10.5 Serial Poll

5.3.10.5.1 The status byte register of the GPIA is normally updated approximately every 1 ms by the microprocessor. When the interface is addressed to talk following the receipt of the serial poll enable (SPE) message, the GPIA puts the status byte onto the bus without further action by the microprocessor.

5.3.10.5.2 When the serial poll is completed, the controller sends the serial poll disable (SPD) message, which is detected by IC26, IC7, IC18, and IC19. The resulting logic 1 at IC17B-3 clocks IC17B to the reset condition, and gives a logic 1 at IC18-12.

5.3.10.6 Data Transfer Between Microprocessors

5.3.10.6.1 Data transfer between microprocessors is made using the multiplexed data bus on both devices. Connections between the buses is made by means of a D-type latch, IC1 or IC2, depending on the direction of data transfer. All data transfers are initiated by the sending device. The first byte indicates the number of bytes to be transferred.

5.3.10.6.2 For data transfer to the GPIB microprocessor, the instrument's microprocessor sets SK1 pin 22 (GPIBIRQ) low. This provides an interrupt request (IRQ) to the GPIB microprocessor via IC4. As part of the interrupt routine, IC8 is enabled and addressed to give an enabling signal for IC5A. The microprocessor reads the IRQ flag via IC5A and data bus line 7 to establish that the IRQ is from the instrument and not the GPIA.

5.3.10.6.3 The GPIB microprocessor prepares to receive data, and then enables and addresses IC8 to give a signal which clocks IC16B via IC20-6. The level set on line 0 of the data bus is transferred to IC16B-5, and forms the ready for data (RFD) signal to the instrument's microprocessor.

5.3.10.6.4 The instrument's microprocessor enables and addresses IC3 to give an enabling signal to IC5B, reads the RFD signal, puts the first data byte on the bus, and readdresses IC3 to give a clock signal which latches the data into IC1. It then addresses IC3 to give a clock signal for IC16A, so that the logic level set at IC16A-12 is transferred to IC16A-19 to form the data valid (DAV) signal to the GPIB microprocessor.

5.3.10.6.5 The GPIB microprocessor addresses IC8 to give a signal to enable IC5A, and reads the DAV signal via data bus line 6. It then cancels its RFD signal, addresses IC8 to give an output enable signal for IC1 (via IC20-8) and reads the data. A data accepted (DAC) signal is sent via IC2 and the RFD signal is reset. The instrument's microprocessor responds by cancelling its DAV signal and entering the next data byte into IC1. Data transfer continues in this manner until the required number of bytes have been received.

5.3.10.6.6 Data transfer from the GPIB microprocessor to the instrument's microprocessor follows a similar pattern. The IRQ signal is passed from port A line 0 via IC18 and IC4. The IRQ flag is read by the instrument's microprocessor during its interrupt routine, via IC5B (enabled by an output from IC3). The IRQ signal is cancelled by the instrument's microprocessor setting data bus line 0 to logic 0 and then addressing IC3 to clock IC17A. The resulting logic 0 at IC17B-9 disables IC18-4.

5.3.10.6.7 During data transfer from the GPIB interface to the instrument, the RFD signal is passed via IC16A and IC5A, the DAV signal via IC16B and IC5B, the DAC signal via IC1, and the data via IC2.

SECTION 6 MAINTENANCE

6.1 INTRODUCTION

6.1.1 This section is written in eight parts including the following:

a. PVP/Calibration Inspection Intervals

b. Required Test Equipment

c. Dismantling and Reassembly

d. Special Functions for Diagnostic Purposes

e. Troubleshooting

f. Post-Repair Setup (or after the instrument fails the overall performance verification procedure)

g. Internal Frequency Standard - routine calibration

h. Overall Performance Verification Procedure

6.1.2 The Performance Verification Procedures (PVPs) provided in this section are used for (1) receiving inspection/acceptance, (2) periodic determination of the need for recalibration, (3) upon failure of a routine specification check, and (4) after repair of unit. Verify the basic operation of the counter before starting these procedures by completing the rapid functional check found in Subsection 2.6.

6.1.3 Satisfactory completion of these performance tests will confirm the counter's operation by measurement function. Complete the performance tests in the order given.

6.1.4 The following conditions must be maintained during these tests:

a. The counter must be operated from an AC supply

b. The line voltage must be within ±10% of the indicated value of the line voltage selector

c. The ambient temperature must be 23° C ±2° C except at receiving inspection/acceptance when a requirement of 23° C ±5° C is acceptable

d. The power supply to the internal frequency standard must remain uninterrupted. (This does not apply if the counter is locked to an external frequency standard.)

6.1.5 Warm up the counter for one hour (switched to standby if necessary) before beginning these procedures.

6.2 PVP/CALIBRATION INSPECTION INTERVALS

6.2.1 PVP Interval

6.2.1.1 First, refer to Subsection 6.1.2 and review those situations when PVPs should be performed. Periodic PVPs should be carried out, however, at least once a year to verify the basic operation of the 1991/1992 and the possible need for recalibration.

6.2.2 Calibration Interval

6.2.2.1 The need for calibration is determined by the results of carrying out the set of PVPs, except in the case of the internal frequency standard. The calibration interval for the internal frequency standard will depend on the accuracy required and the aging rate of the 04E frequency standard installed. Simply divide the desired accuracy by the aging rate per day to determine the required calibration interval for the internal standard.

NOTE:

All other calibration points for the 1991/1992 except the internal frequency standard should be on a minimum annual basis.

6.3 REQUIRED TEST EQUIPMENT

6.3.1 A complete list of the test equipment required to carry out the procedures described in this section is given in Table 6.1. The items required for each operation are listed at the start of the corresponding instructions.

6.3.2 A particular model of test equipment is recommended in some cases, but other equipment having the required parameters given in Table 6.1 may be used. Although the procedures to be followed are given in general terms, they are based on the use of the recommended test equipment. Some modification to the procedure may be necessary if other test equipment is used.

6.4 DISMANTLING AND REASSEMBLY

6.4.1 Introduction

6.4.1.1 Instructions for dismantling and reassembling the instrument are limited to those areas where special care is needed or difficulty may be experienced.

WARNING

LETHAL VOLTAGE: Dangerous AC voltages are exposed when the instrument is connected to the AC supply with the covers removed. Switch the instrument off and disconnect the supply socket from the rear panel before carrying out any dismantling or reassembly operation.

Table 6.1 - Required Test Equipment

Item	Description/Recommended Model	Required Parameters
1	Signal Generator Racal-Dana 9087	Low phase noise. Jitter < 0.5 ns Frequency range 10 kHz to 1.3 GHz Output level 1 mV to 1V 10 MHz INT STD OUTPUT
2	Oscilloscope with 1:1 Probe	Bandwidth 50 MHz
3	Digital Multimeter Racal-Dana 5001	Frequency range: DC to 5 kHz Level: 20 mV to 20V
4	Frequency Standard Racal-Dana 9475	10 MHz Accuracy better than ± 3 parts in 10^{10}
5	Audio Oscillator Racal-Dana 9085	Frequency range: 10 Hz to 5 kHz Level: 30 mV into 50Ω
6	Pulse Generator Racal-Dana 1515	To provide a single positive-going pulse with a low level of +0.4V and a high level of +2.4V (TTL output limit levels)
7	Connecting Lead	50Ω coaxial cable with BNC connectors. Length between 60 cm and 1m
8	T-piece	BNC, 50Ω
9	Coaxial Load	BNC, 50Ω
10	GPIB Controller HP-85	—
11	GPIB Analyzer Racal-Dana 488	—

6.4.2 Instrument Covers

6.4.2.1 Complete the following procedure to remove the instrument covers:

a. Disconnect the power cord from the rear panel

b. Remove the two screws and washers securing the rear-panel bezel shown in Figure 6.1. Then remove the bezel

c. Remove the top cover by sliding it to the rear of the instrument

d. Remove the bottom cover by sliding it to the rear of the instrument

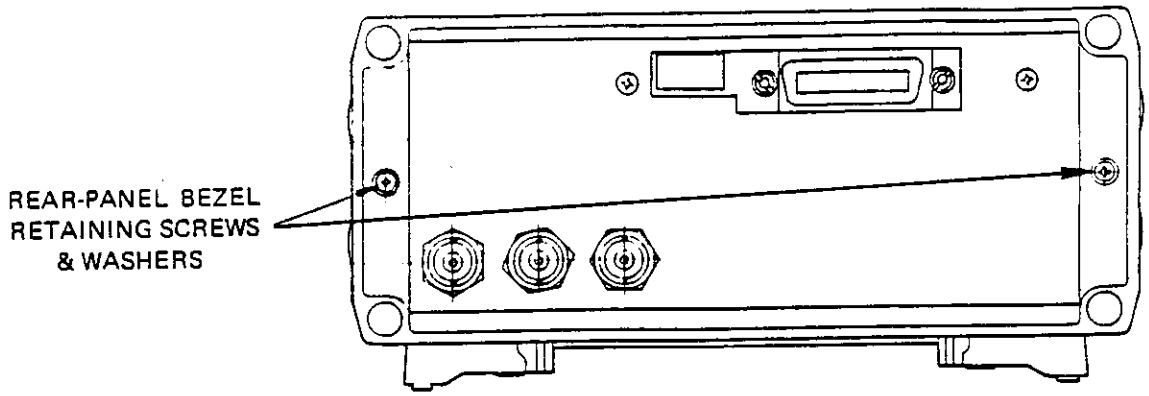


Figure 6.1 - Rear-Panel Bezel Removal

6.4.2.2 To replace the covers, reverse the above procedure. When replacing the bottom cover, ensure that the tilt bail is facing toward the front of the instrument and that the tongue of the cover fits into the slot on the front panel as shown in Figure 6.2. When replacing the top cover, ensure that the access holes are towards the front of the instrument (see Figure 6.3) and that the tongue of the cover fits under the edge of the front panel at all points. Refer to Figure 6.4 for orientation of the bezel to the rear panel.

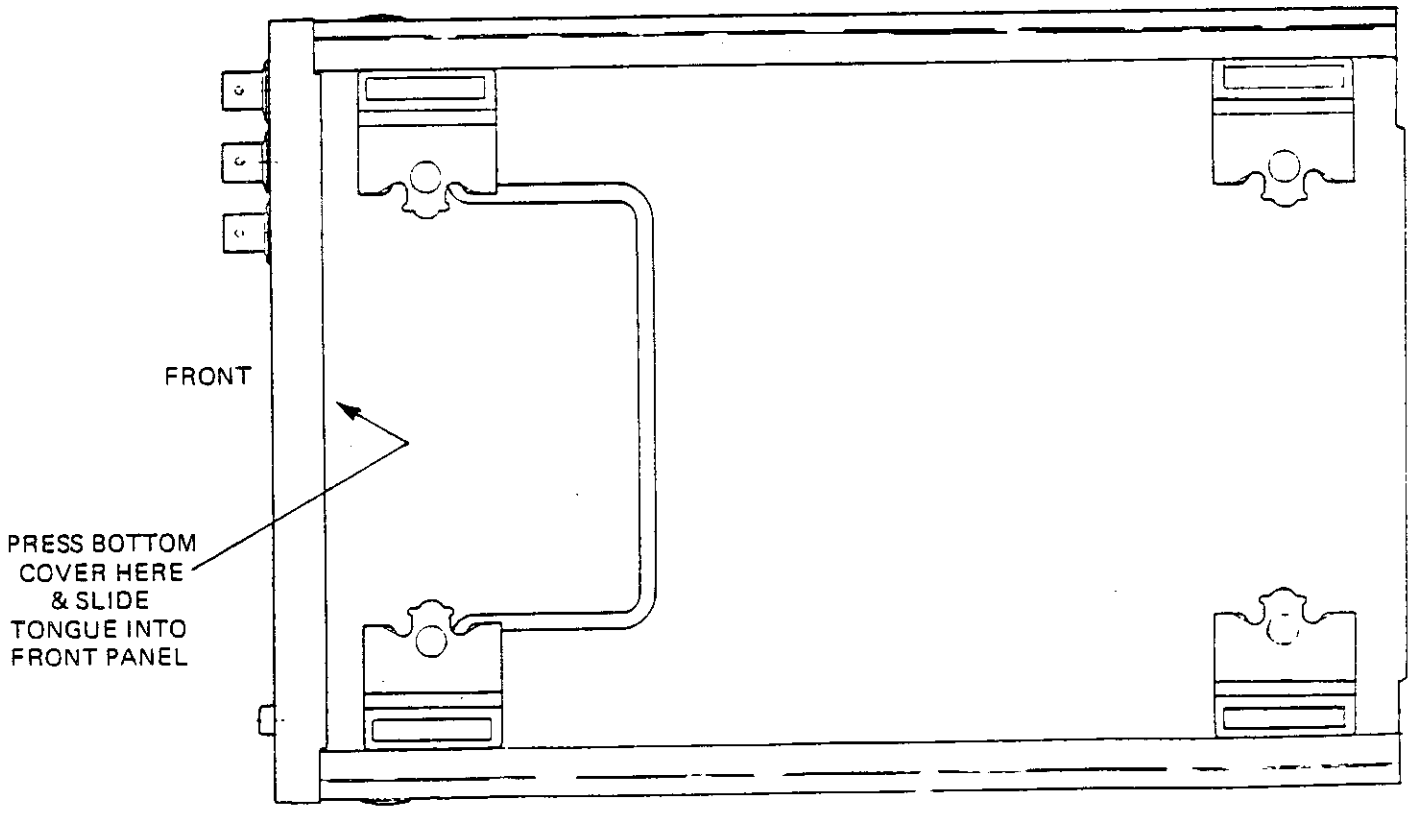


Figure 6.2 - Bottom Cover Replacement

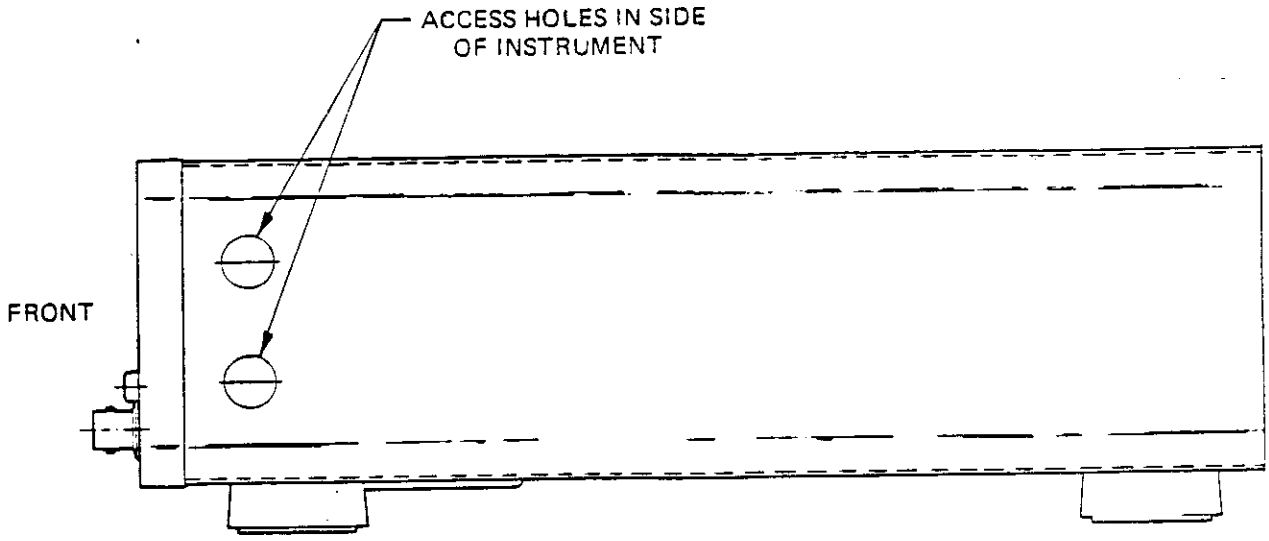


Figure 6.3 - Proper Access Hole Orientation

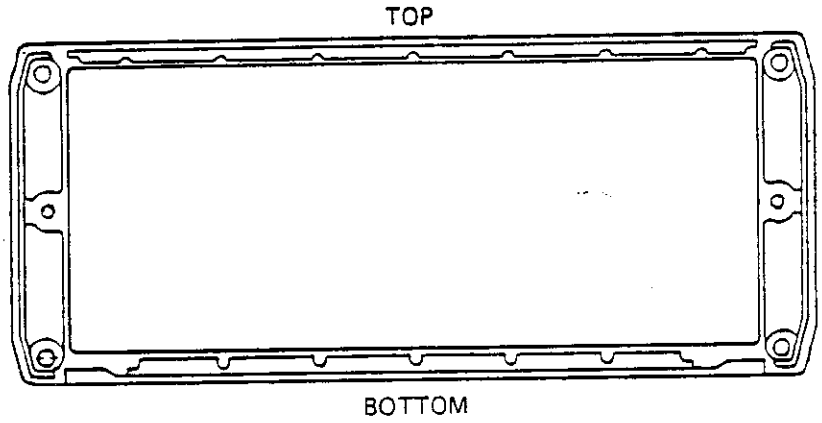


Figure 6.4 - Rear Panel Bezel Orientation

6.4.3 Front Panel

6.4.3.1 Complete the following procedure to remove the instrument front panel:

a. Remove the top and bottom covers of the instrument

b. Remove the clamping collars from the channel A and B inputs. Use the special spanner available from Racal-Dana (P/N R-14-1586) and turn counterclockwise. Refer to Figures 6.5A and 6.5B for this step

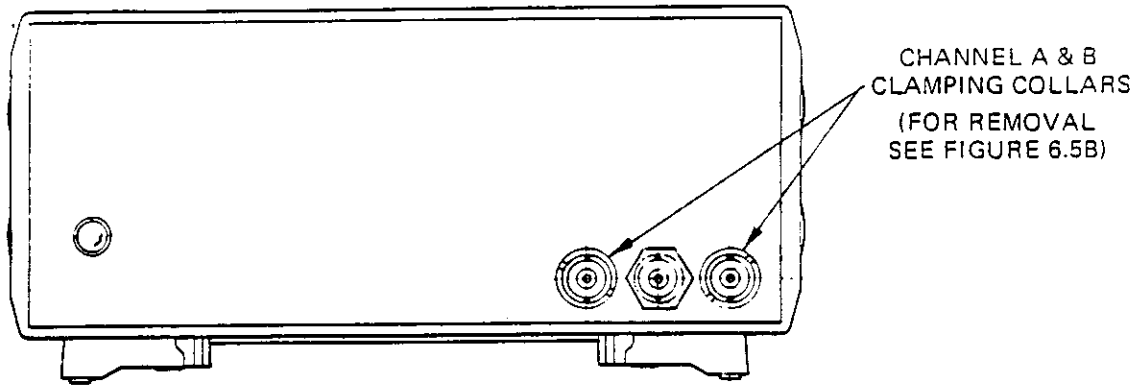


Figure 6.5A - Channel A and B Clamping Collars

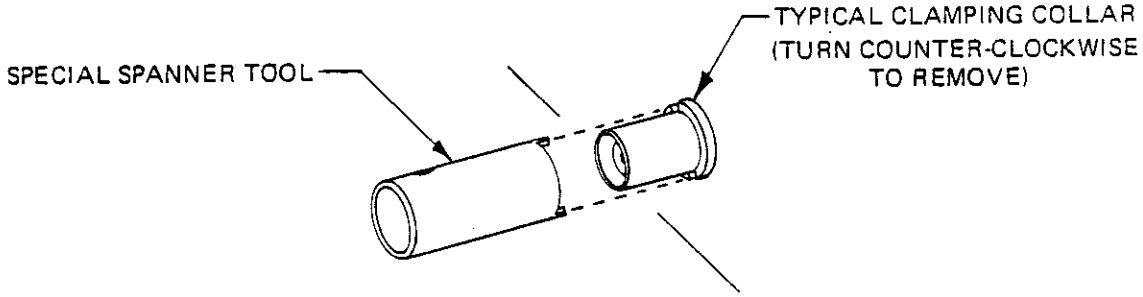


Figure 6.5B - Clamping Collar Removal

c. Remove the two screws and washers securing the front panel to each side frame of the instrument. See Figure 6.6

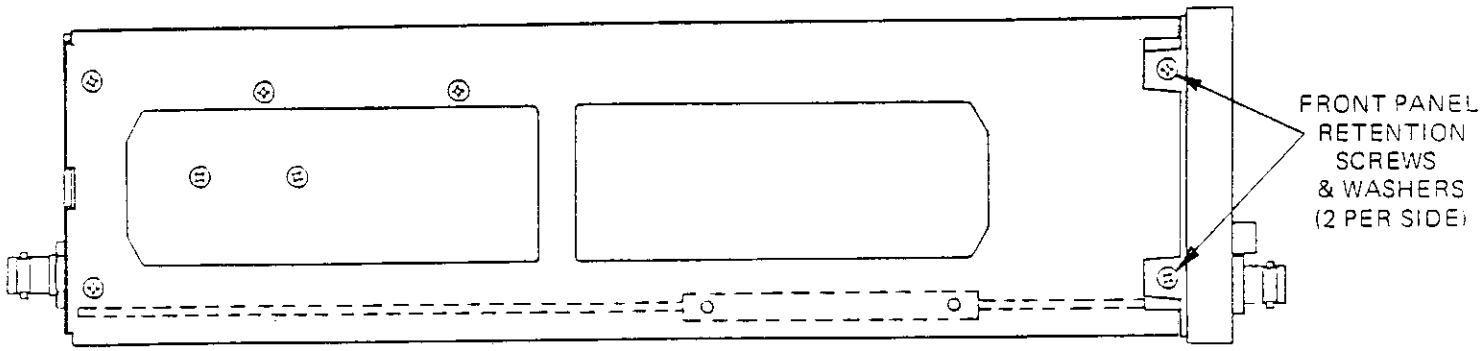


Figure 6.6 - Front-Panel Retention Screw Removal

d. Ease the front panel forward until the display board disconnects from the motherboard at PL1 and PL2. See Figure 6.7

e. Disconnect the coaxial lead from the back of the Channel C input. See Figure 6.7

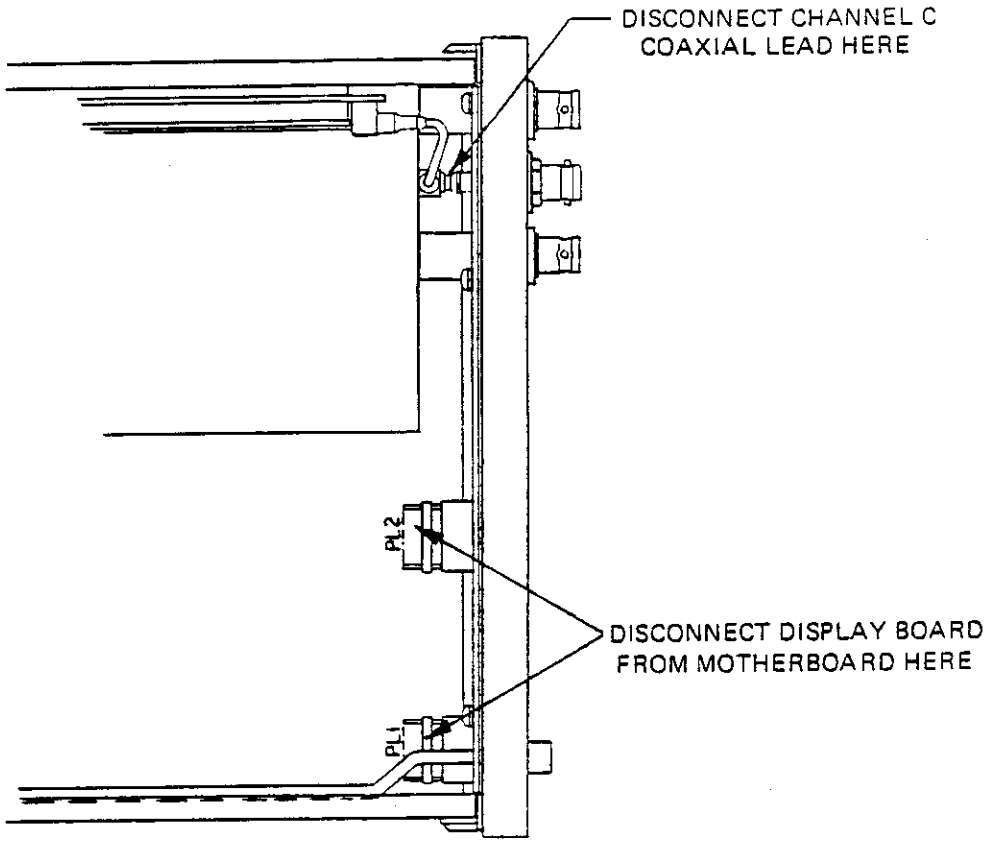


Figure 6.7 - Display Board and Channel C Disconnection

6.4.3.2 To replace the front panel, reverse the above procedure. Pass the POWER switch button through its opening in the front panel and reconnect Channel C's coaxial lead to the PCB to Channel C's input connector before securing the panel.

6.4.4 Rear Panel

6.4.4.1 Complete the following procedure to remove the instrument rear panel:

a. Remove the instrument covers

b. Refer to Figure 6.8. Remove the GPIB board from the unit by completing the following steps:

1. Remove the two screws and lock washers on the rear panel as shown

2. Remove the two screws on the GPIB board itself as shown

3. Lift up the GPIB board where shown and unplug the GPIB/motherboard cable from the motherboard at SK4

4. Now the GPIB board is free to remove

c. Remove the two screws and washers (2 each/side) securing the rear panel to each side frame of the instrument. See Figure 6.9

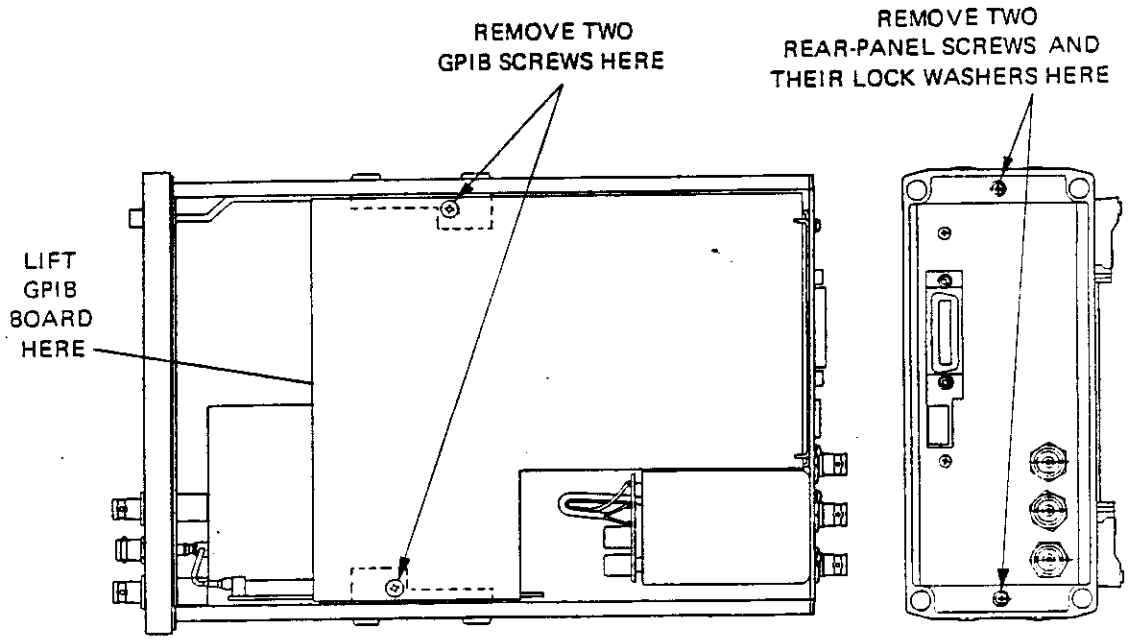


Figure 6.8 - GPIB Board Removal

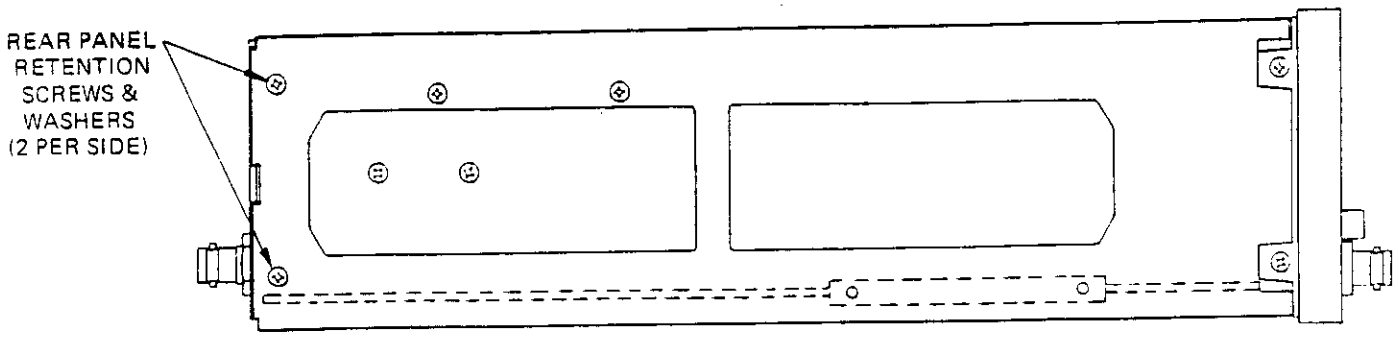


Figure 6.9 - Rear-Panel Retention Screw Removal

d. Ease the rear panel away from the instrument and disconnect from the motherboard at PL19 and PL20. See Figure 6.10

e. Disconnect the frequency standard's flying lead from PL14 on the motherboard. See Figure 6.10

f. Remove the nut and crinkle washer securing the rectifier bridge D11 to the rear panel. See Figure 6.10

g. Disconnect the green/yellow lead connecting the rear-panel stud to the power input plug. See Figure 6.10

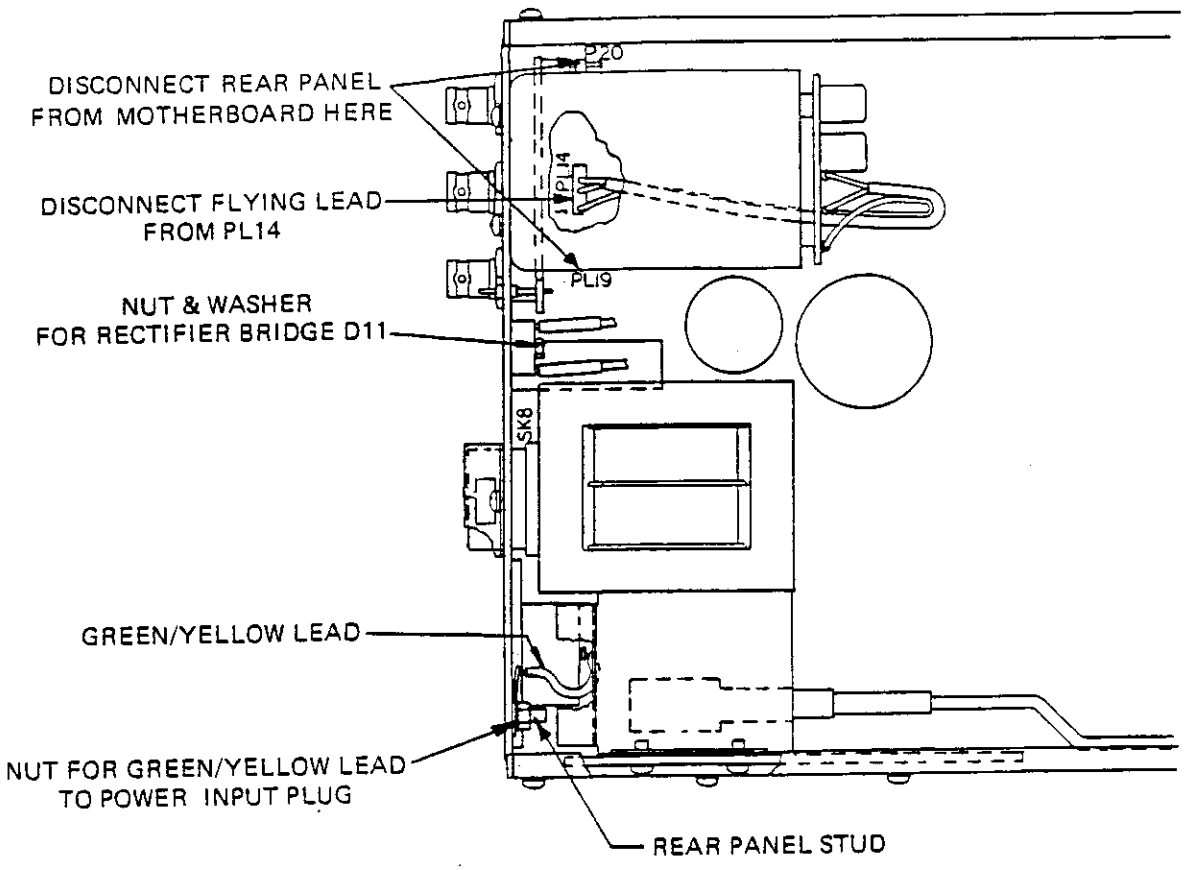


Figure 6.10 - Rear-Panel Removal Detail

6.4.4.2 To replace the rear panel, reverse the above procedure.

WARNING

LETHAL VOLTAGE - the grounding of external metalwork of the instrument depends upon the connection between the rear-panel stud and the power input plug. Ensure that the green/yellow lead to the power input plug is correctly connected during reassembly.

6.4.5 Channel C Board (Model 1992 only)

6.4.5.1 Complete the following procedure to simply access Channel C's PCB:

a. Remove the top cover

b. Remove GPIB board. Refer to Subsection 6.4.4.1.b for instructions

c. Remove the two screws and washers securing Channel C's amplifier PCB to the right-hand side frame. See Figure 6.11

6.4.5.2 Complete the following steps to remove the amplifier board completely:

a. Remove the front panel (see Subsection 6.4.3)

b. Disconnect the coaxial lead from the back of Channel C's input

6.4.5.3 To replace the amplifier board, reverse the above procedure.

6.4.6 Display Board

6.4.6.1 Complete the following procedure to remove the display board:

a. Remove the instrument covers (see Subsection 6.4.2)

b. Remove the front panel (see Subsection 6.4.3)

c. Remove the three screws and washers securing the display board to the front panel (see Figure 6.11) and remove the board

6.4.6.2 To replace the display board, reverse the above procedure.

6.5 SPECIAL FUNCTIONS FOR DIAGNOSTIC PURPOSES

6.5.1 The special functions listed in Table 6.2 are for use during maintenance. The functions are used in conjunction with the CHECK mode. They are entered in the special function register by pressing:

[N] [N] [SHIFT] [STORE] [SF]

and are enabled and disabled by pressing:

[SHIFT] [SF]

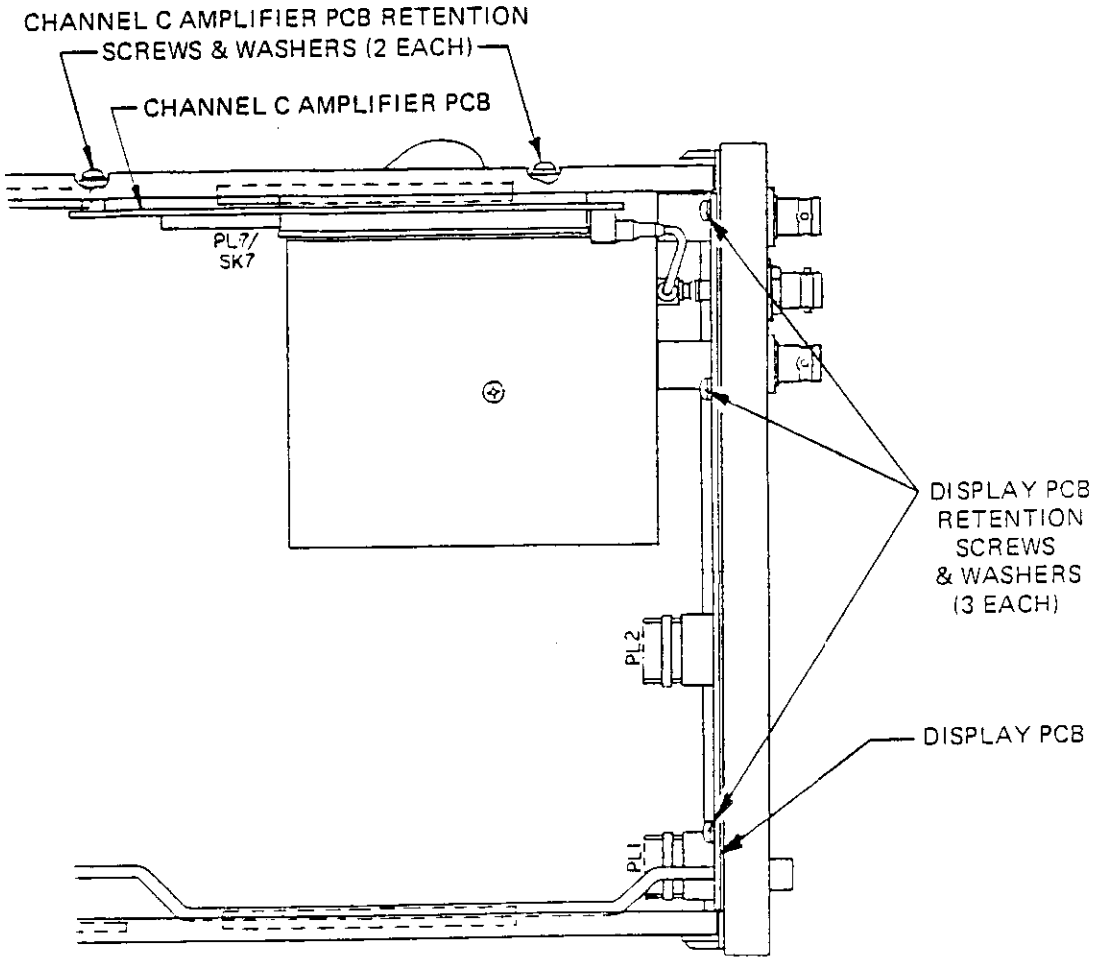


Figure 6.11 - Channel C Amplifier Board and Display Board Removal

Table 6.2 - Diagnostic Special Functions

Special Function Number	Function With CHECK Mode Selected
70	10 MHz check
71	LED check
72	Measurement of short start TEC count
73	Measurement of long start TEC count
74	Measurement of short stop TEC count
75	Measurement of long stop TEC count
76	D-to-A converter check
77	Channel A relay check
78	Channel B relay check

6.5.2 Special Function 70

6.5.2.1 Special Function 70 is the default state of its decade. It provides measurement of the 10 MHz internal frequency standard and verifies operation of the microprocessor system, MCC1, MCC2, and the TEC.

6.5.3 Special Function 71

6.5.3.1 Special Function 71 exercises all the LEDs, except STANDBY, GATE, TRIG A, TRIG B, REM, ADDR and SRQ, at approximately 0.5 Hz. If the GPIB interface is installed, the REM, ADDR and SRQ LEDs light.

6.5.4 Special Functions 72, 73, 74, and 75

6.5.4.1 Special Functions 72, 73, 74, and 75 should only be used for diagnostic purposes at an ambient temperature of $23^{\circ}C \pm 2^{\circ}C$.

6.5.4.2 The long counts must be 800 ± 220. The short counts (0.5 x long count) must be in the range +20 to -40. Counts outside these ranges indicate that the TEC has failed.

6.5.5 Special Function 76

6.5.5.1 With Special Function 76 active, the microprocessor continuously exercises the D-to-A converters in both Channel A and Channel B through the range -5.1V to +5.1V. The waveform (51 levels spaced by 0.2V) can be monitored at the trigger output pins on the rear panel.

6.5.6 Special Function 77

6.5.6.1 With the 10 MHz STD OUTPUT socket on the rear panel connected to the Channel A input, activating Special Function 77 causes the microprocessor to exercise the Channel A relays for x10/x1, 50Ω/1 MΩ and DC/AC, FILTER, and COM A. See NOTE below.

6.5.7 Special Function 78

6.5.7.1 With the 10 MHz STD OUTPUT socket on the rear panel connected to the Channel B input, activating Special Function 78 causes the microprocessor to exercise the Channel B relays for x10/x1, 50Ω/1MΩ and DC/AC. See NOTE below.

NOTE:

Cable length is important during use of either Special Function 77 or 78 for diagnostic purposes. The cable should be between 0.6 to 1 meter in length. See Item 7 in Table 6.1.

6.6 TROUBLESHOOTING

6.6.1 A guide to fault location is given in the flowcharts of Figures 6.12 to 6.20. The charts provide a logical procedure for localizing the fault to an area of circuit. When using the charts it is essential to begin at the start point in Figure 6.12 or 6.17 and act in sequence according to the results of each decision box. Starting part way through any chart is unlikely to lead to satisfactory fault isolation.

6.6.2 Required Test Equipment

Item	Table 6.1, Item No.
Oscilloscope	2
Digital Multimeter	3
Coaxial Connecting Lead	7
GPIB Controller	10
GPIB Analyzer	11

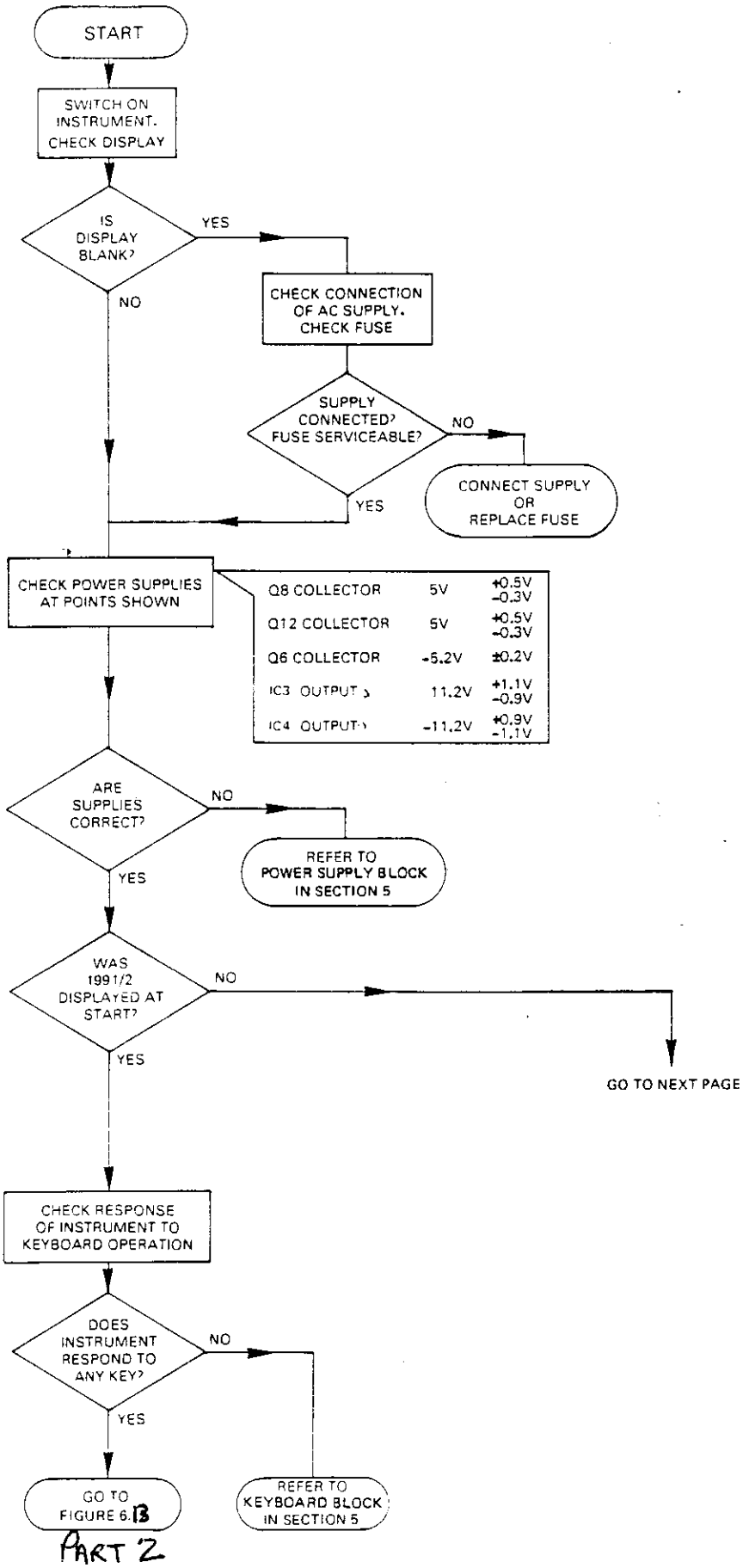


Figure 6.12 - Fault Finding Flowchart - Part 1

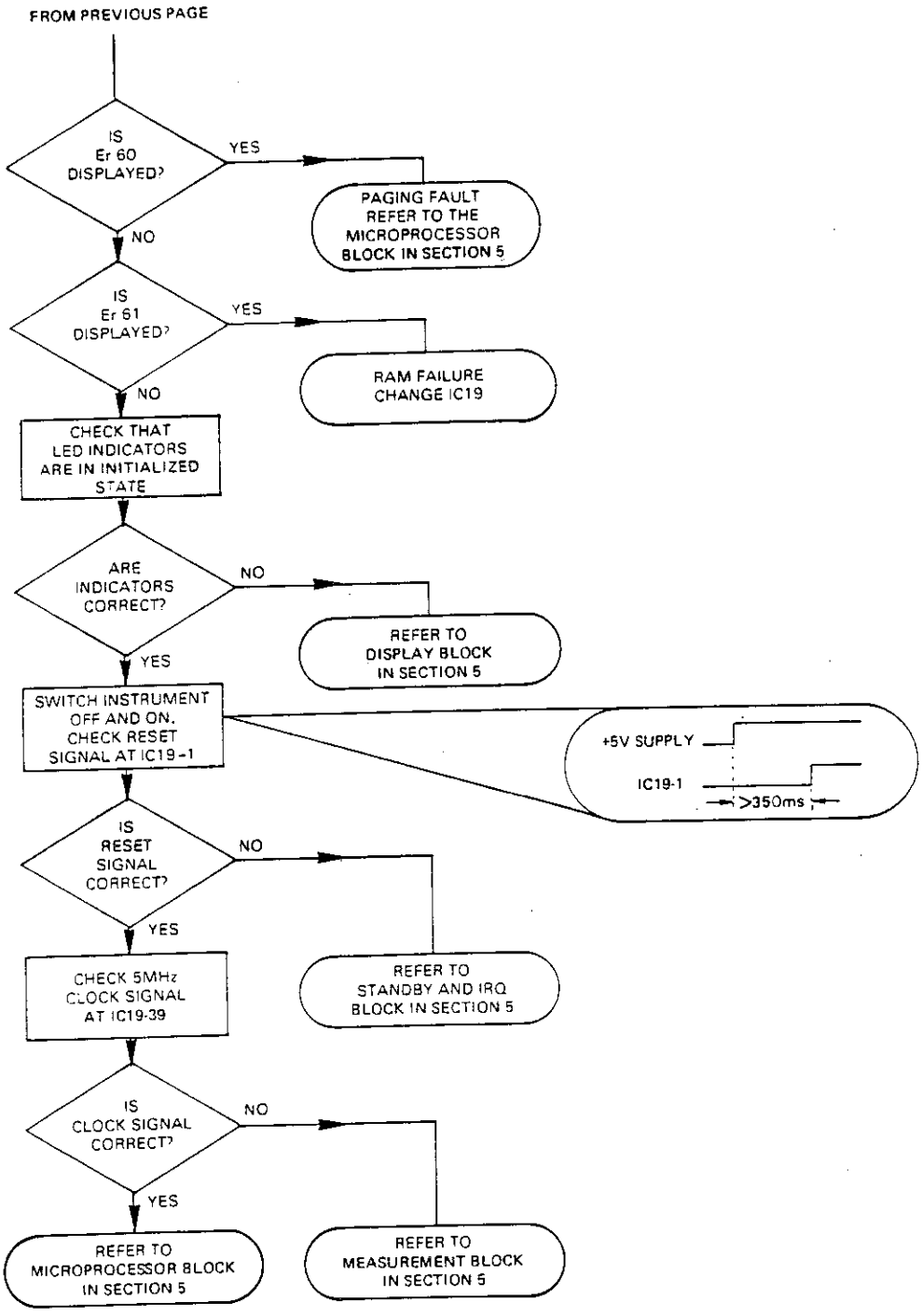


Figure 6.12 - Fault Finding Flowchart - Part 1 (Cont'd)

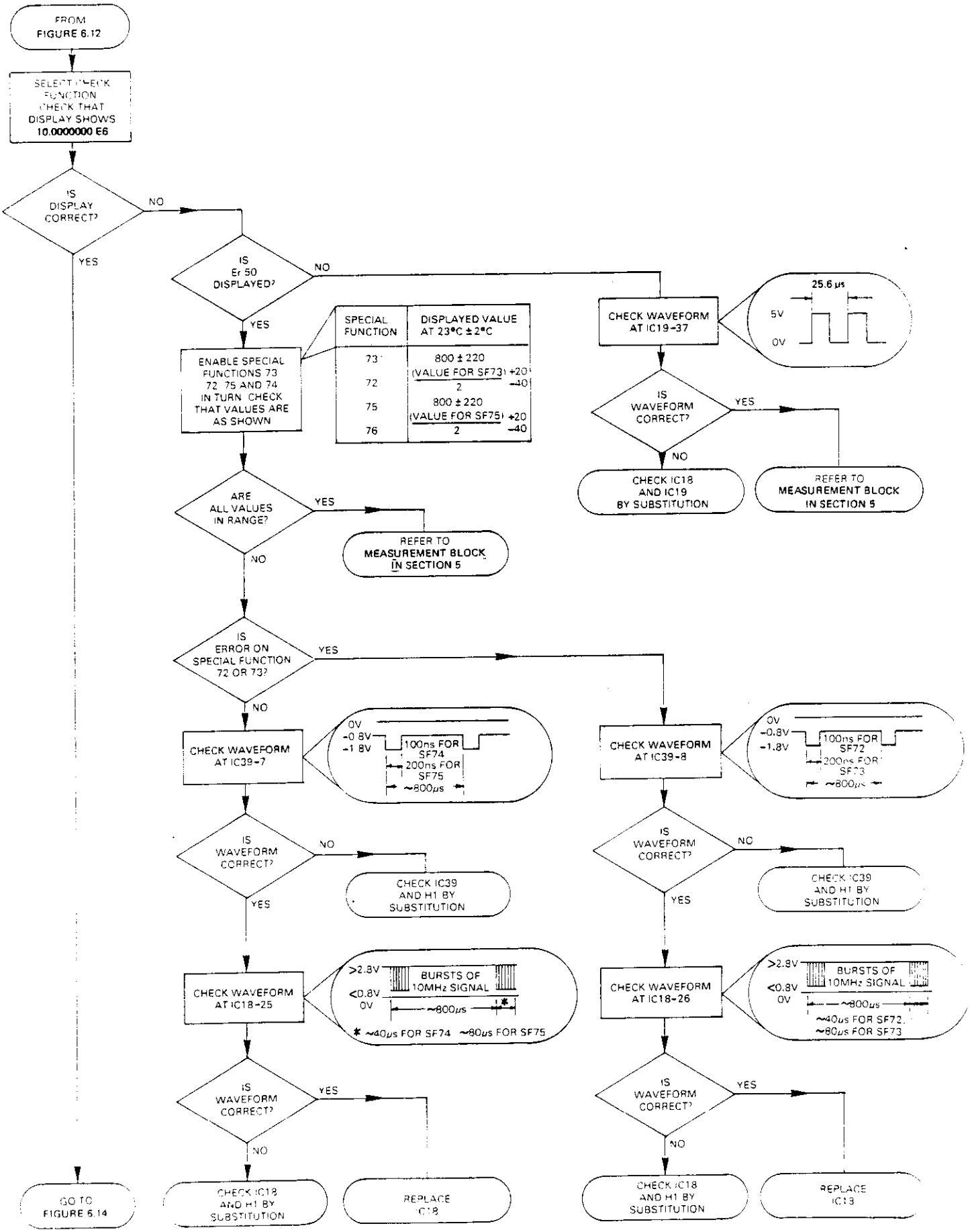


Figure 6.13 - Fault Finding Flowchart - Part 2

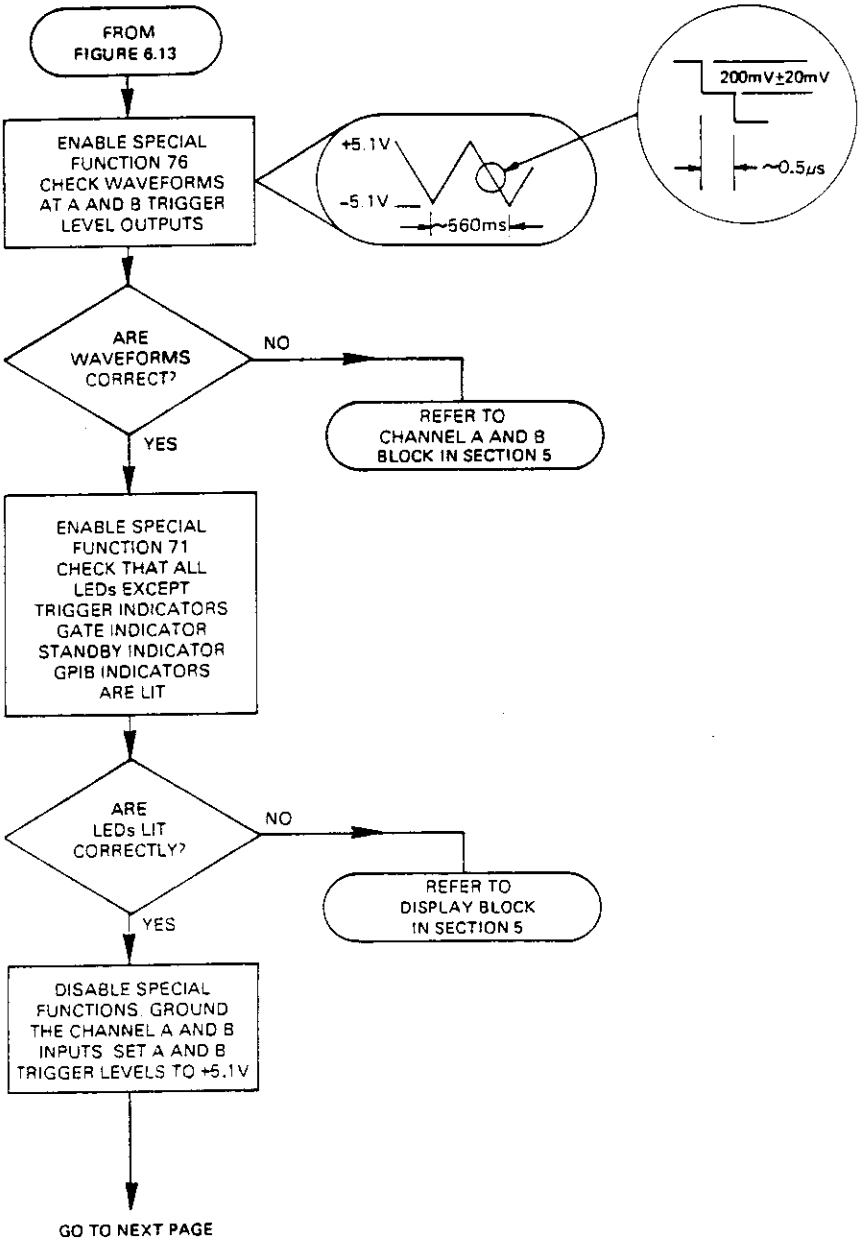


Figure 6.14 - Fault Finding Flowchart - Part 3

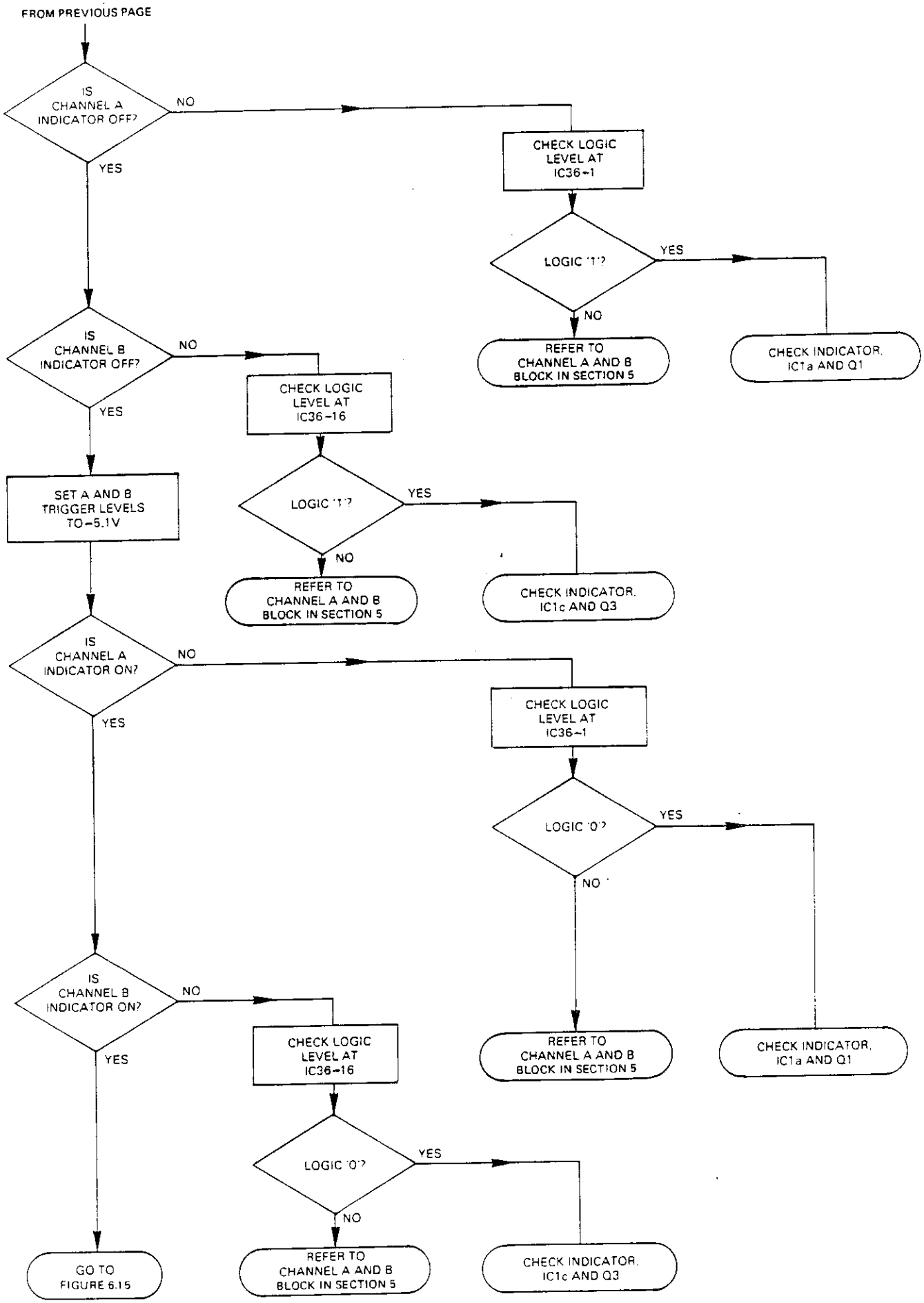


Figure 6.14 - Fault Finding Flowchart - Part 3 (Cont'd)

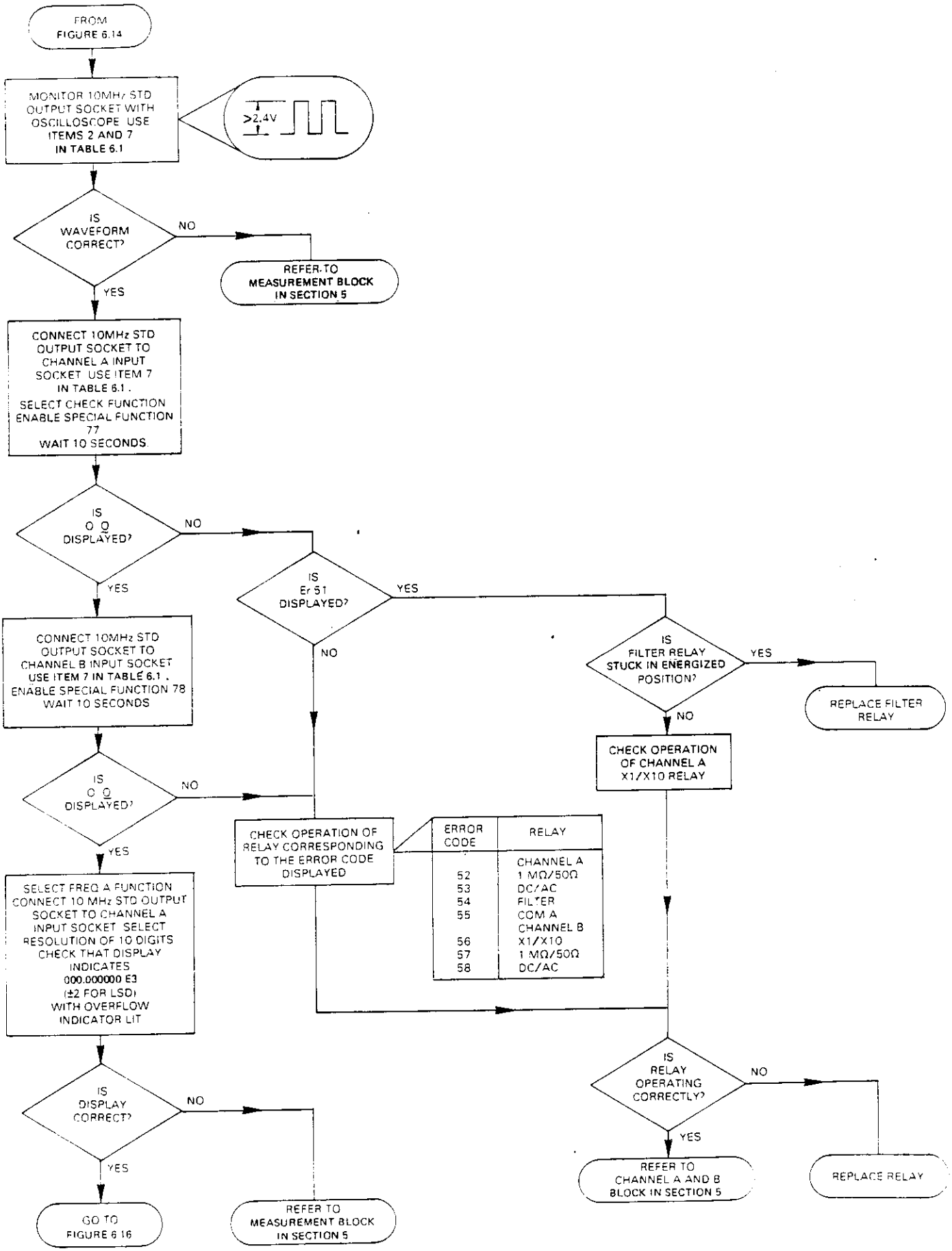


Figure 6.15 - Fault Finding Flowchart - Part 4

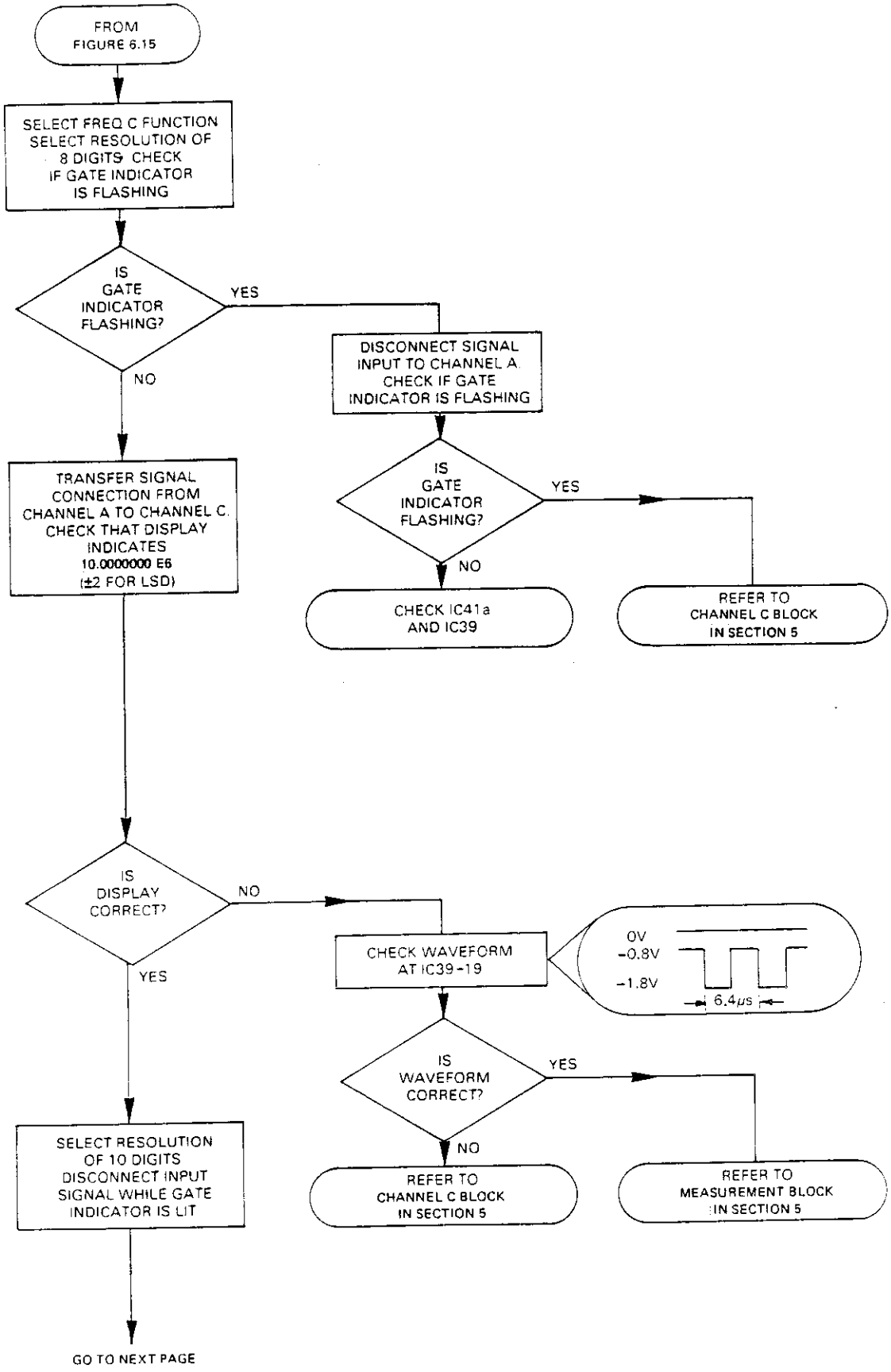


Figure 6.16 - Fault Finding Flowchart - Part 5

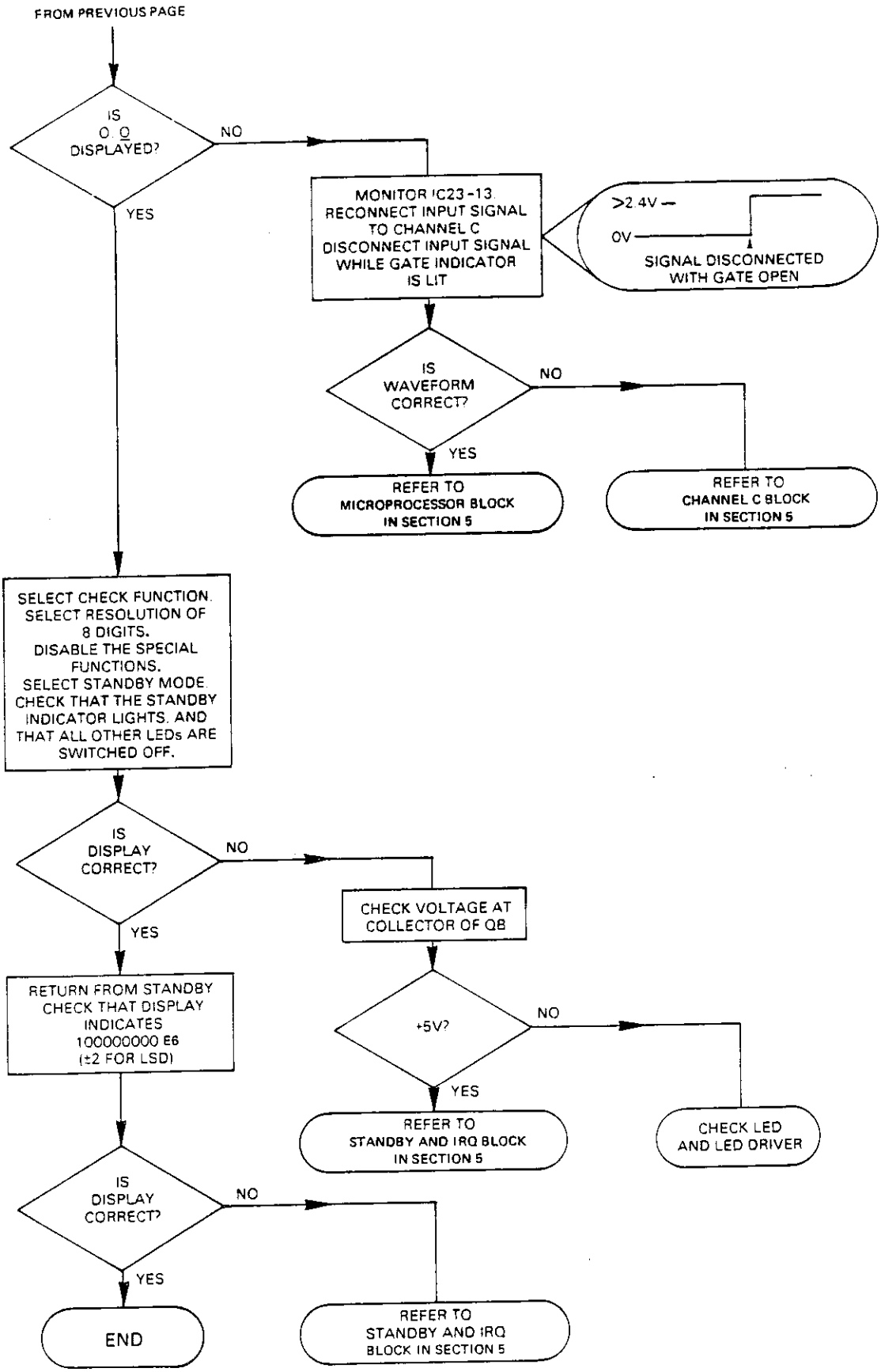


Figure 6.16 - Fault Finding Flowchart - Part 5 (Cont'd)

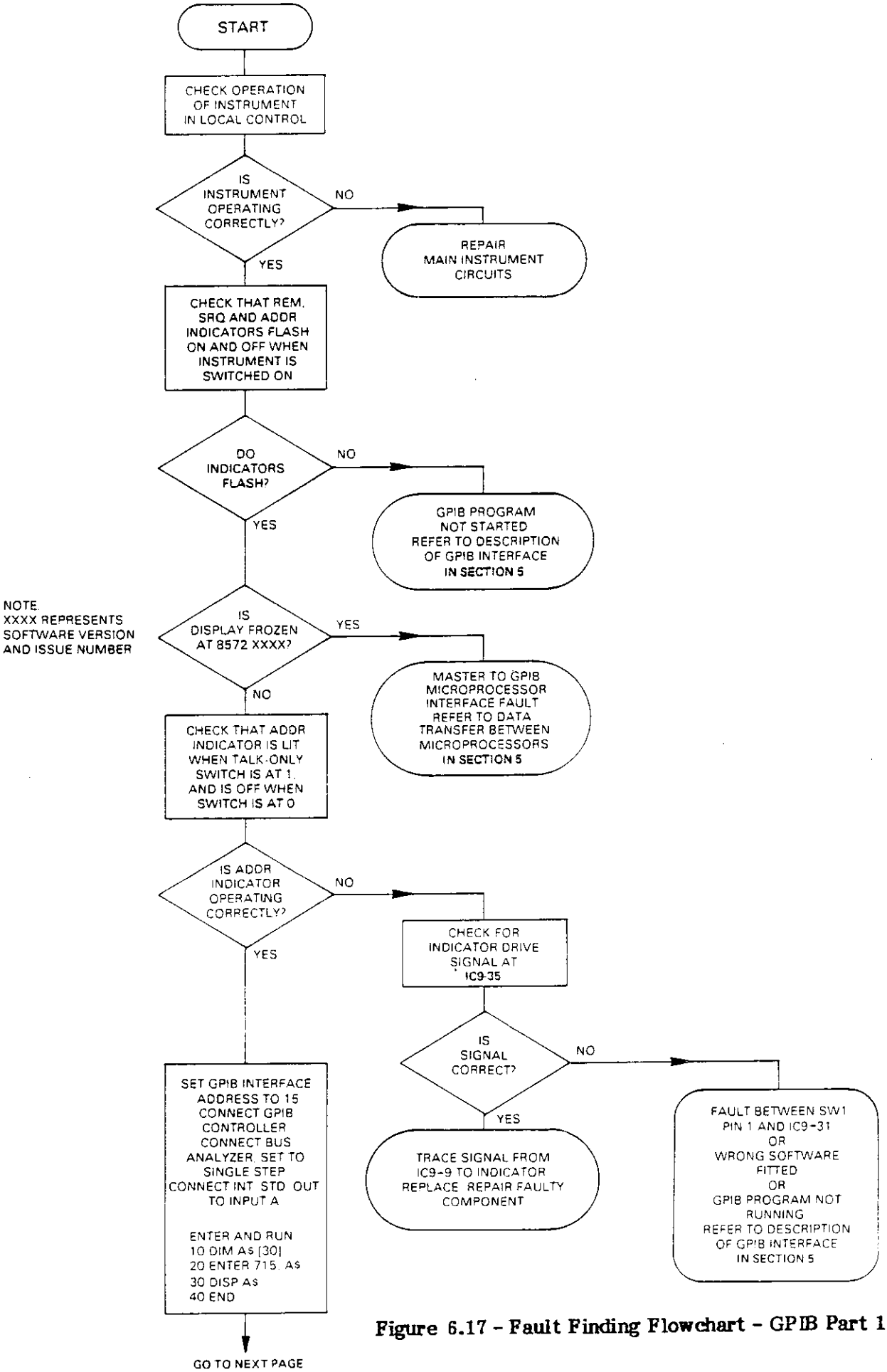


Figure 6.17 - Fault Finding Flowchart - GPIB Part 1

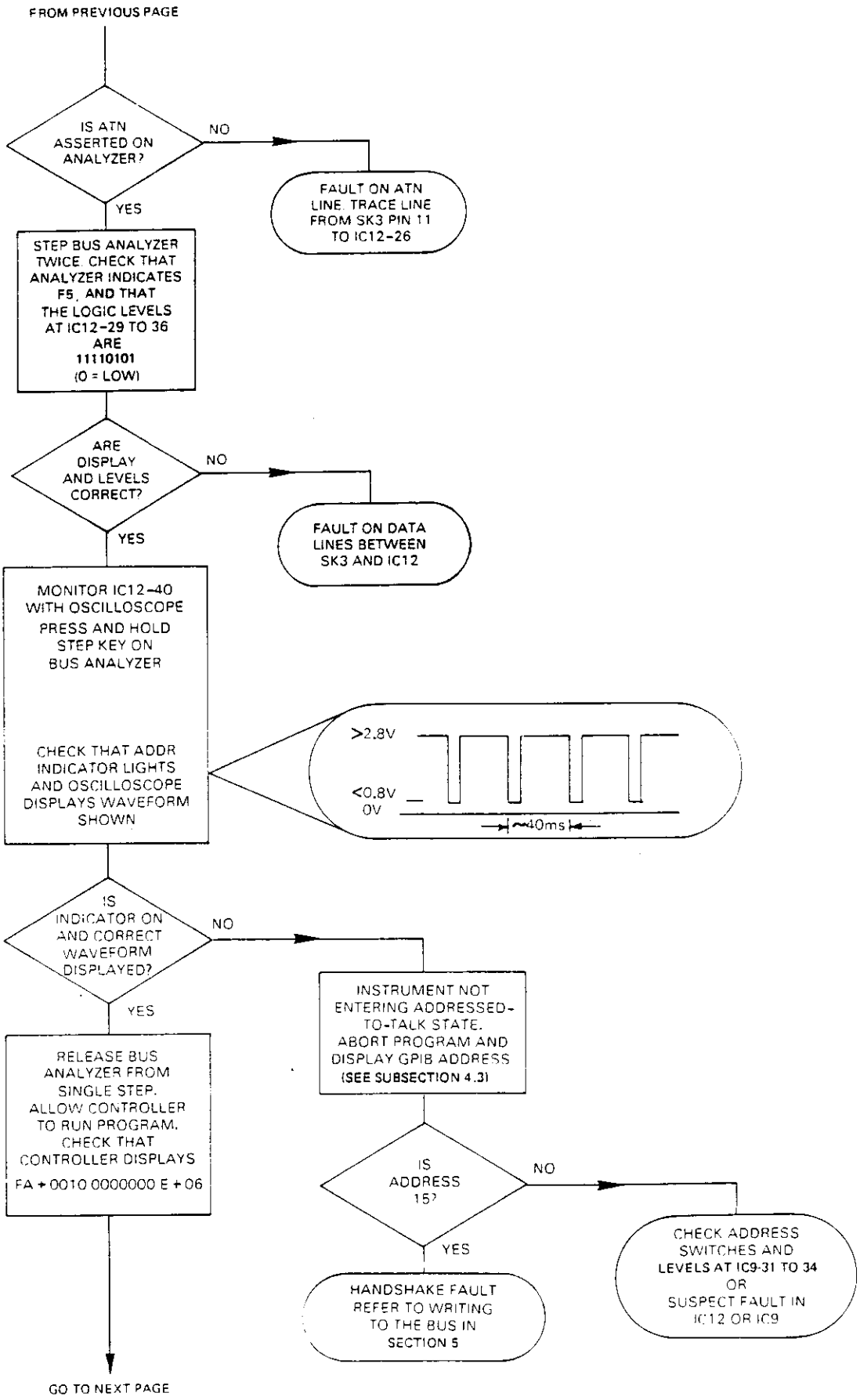


Figure 6.18 - Fault Finding Flowchart - GPIB Part 2

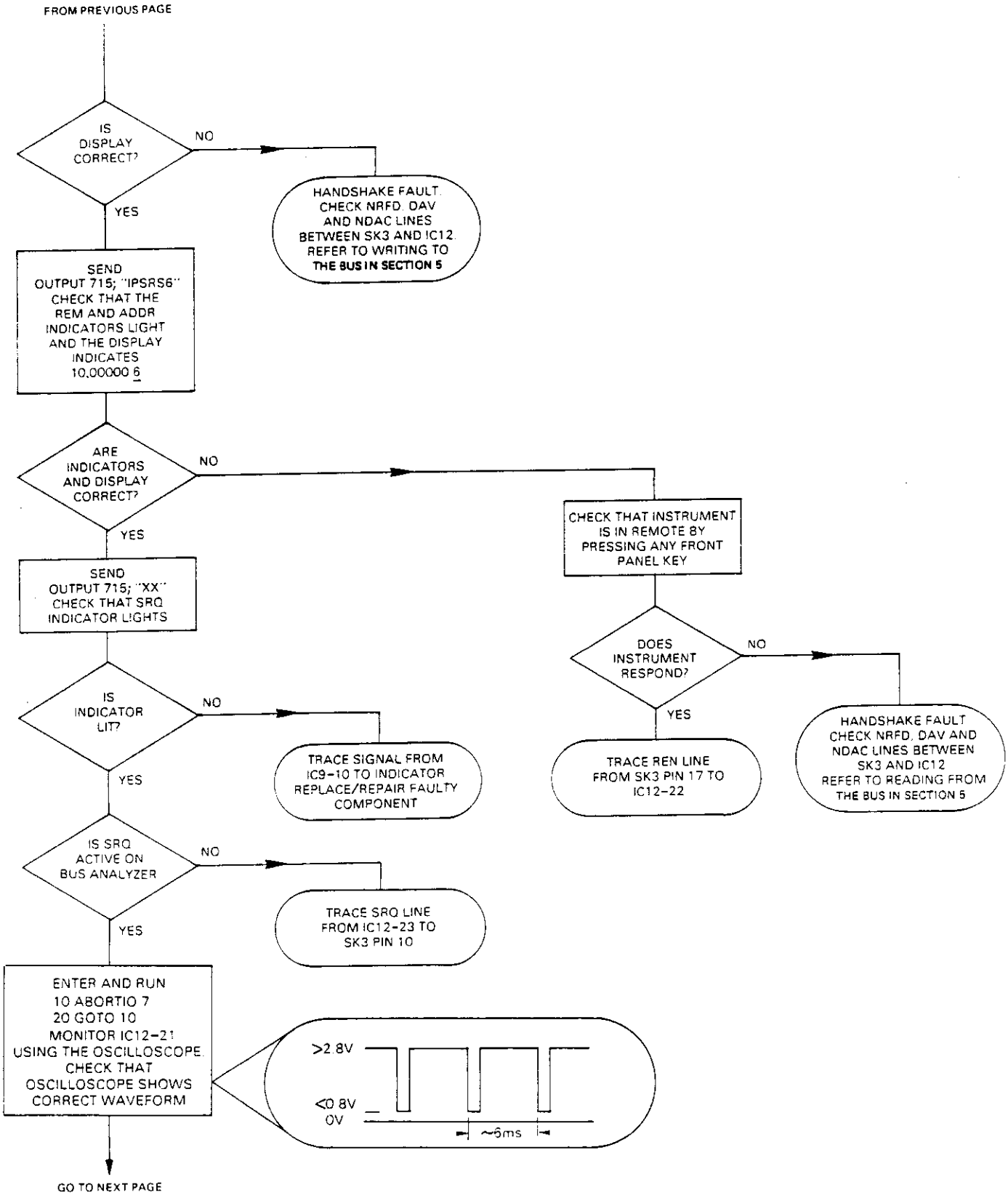


Figure 6.19 - Fault Finding Flowchart - GPIB Part 3

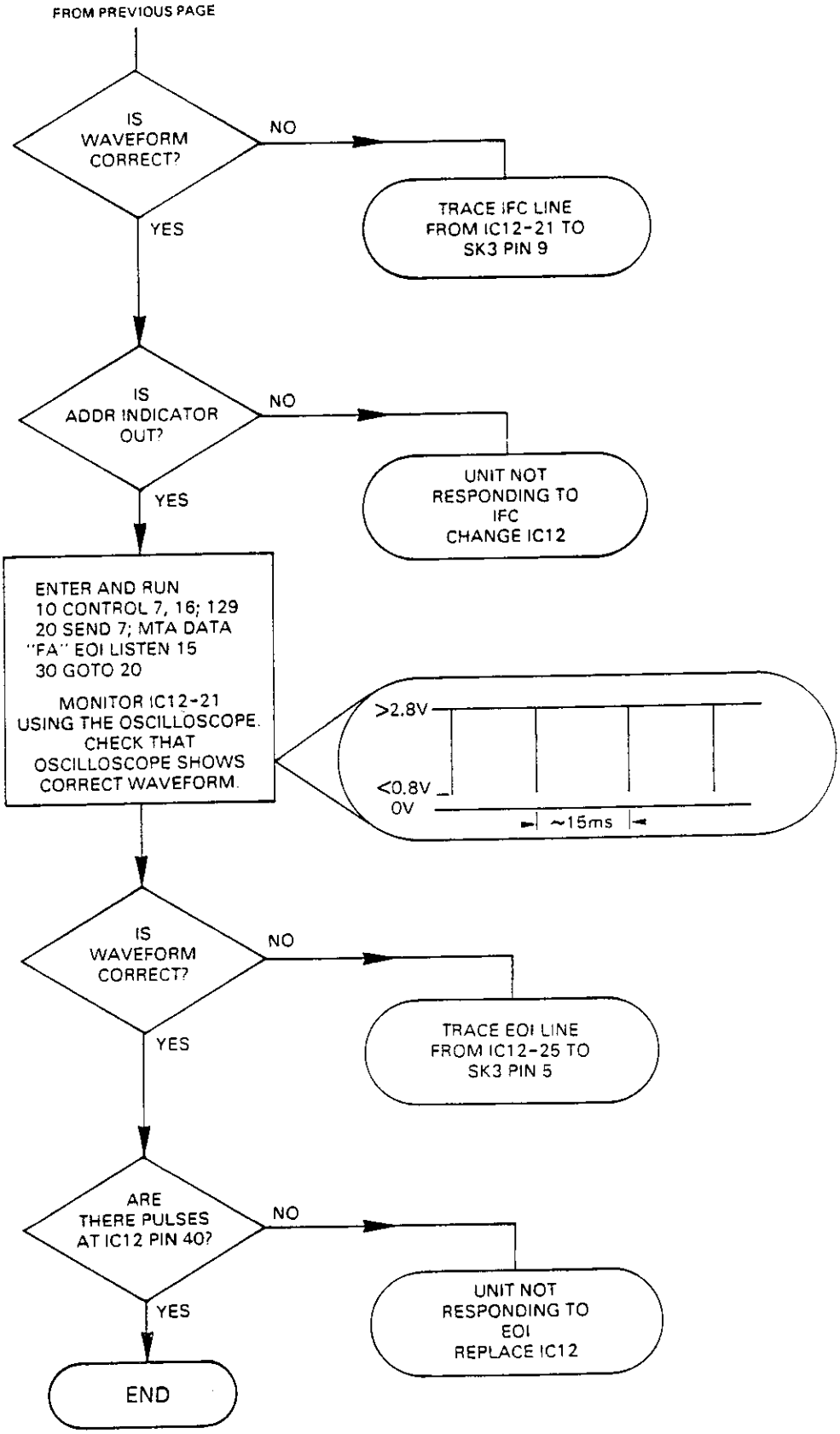


Figure 6.20 – Fault Finding Flowchart – GPIB Part 4

6.7 POST-REPAIR SETUP

6.7.1 Introduction

6.7.1.1 After repair, implement the appropriate setup procedure from the following subsections before performing the overall performance verification. These procedures should also be used if the instrument fails the overall performance verification check.

6.7.1.2 The ambient temperature must be maintained at 23° C ± 2° C throughout these procedures. The instrument should be powered from an AC supply.

WARNING

LETHAL VOLTAGE: These procedures require the instrument to be operated with the covers removed. Lethal voltage levels are exposed under these conditions.

6.7.2 Channel A Input System

6.7.2.1 Required Test Equipment

Item	Table 6.1, Item No.
Signal Generator	1
Coaxial Connecting Lead (Qty. 2)	7

6.7.2.2 Counter Setup Procedure

6.7.2.2.1 Set R149 fully counterclockwise and R192 to its mid-position. R192 is located inside the screened module as shown in Figure 6.21.

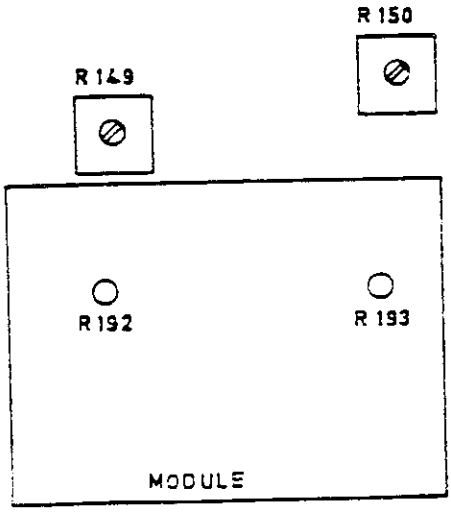


Figure 6.21 - Location of R149 and R192

6.7.2.2.2 Complete the following procedure:

a. Switch the 1991/1992 on. Select FREQ A

b. Select 50Ω impedance for Channel A

c. Press the RESOLUTION ▼ key five times until 000 is displayed

d. Connect the test equipment as shown in Figure 6.22

e. Set the signal generator output to 100 MHz at a level of 3.0 mV RMS

f. Verify that the EXT STD LED is lit and that the Channel A TRIG LED is flashing

g. Adjust R192 to obtain the most stable display indication of 100.0 E6 ± 0.1 E6, with the GATE LED flashing

NOTE:

Care is needed when adjusting R192. The display indication is random with R192 set to either side of the correct position.

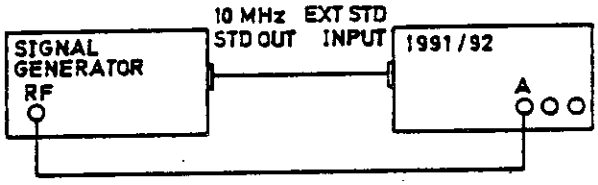


Figure 6.22 – Connections for Channel A Input System Adjustment

6.7.2.3 **Counter Test Procedure**

a. Switch off the RF output of the signal generator

b. Press the RESOLUTION ▲ key five times until 00000000 is displayed

c. Switch on the RF output of the signal generator

d. Increase the signal generator output to 13 mV RMS

e. Adjust R149 slowly clockwise until the display just becomes unstable. Turn back until the display is just stable and indicates 100.000000 E6 0.000001 E6

f. Reduce the signal generator output to 7 mV RMS. Verify that the GATE LED stops flashing. If it does not, repeat steps d to f

g. Switch off the counter. Disconnect the test equipment

6.7.3 Channel B Input System

6.7.3.1 Required Test Equipment

Item	Table 6.1, Item No.
Signal Generator	1
Coaxial Connecting Lead (Qty. 2)	7

6.7.3.2 Counter Setup Procedure

6.7.3.2.1 Set R150 fully counterclockwise and R193 to its mid-position. R193 is located inside the screened module as shown in Figure 6.23.

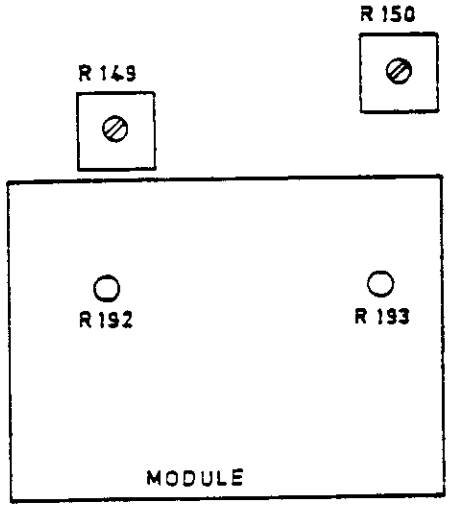


Figure 6.23 - Location of R150 and R193

6.7.3.2.2 Complete the following procedure:

a. Switch the 1991/1992 on. Select FREQ A

b. Select 50Ω impedance for Channel B and press

[2] [1] [SHIFT] [STORE] [SF] [SHIFT] [SF]

c. Press the RESOLUTION ▼ key five times, until 000 is displayed

d. Connect the test equipment as shown in Figure 6.24

e. Set the signal generator output to 100 MHz at a level of 3.0 mV RMS

f. Verify that the EXT STD LED is lit and that the Channel B TRIG LED is flashing

g. Adjust R193 to obtain the most stable display indication of 100.0 E6 ± 0.1 E6, with the GATE LED flashing

NOTE:

Care is needed when adjusting R193. The display indication is random with R193 set to either side of the correct position.

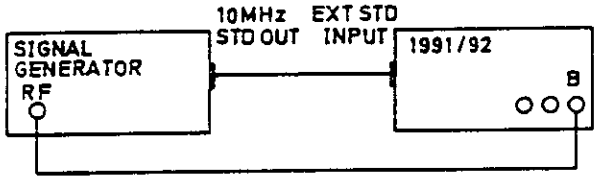


Figure 6.24 - Connections for Channel B Input System Adjustment

6.7.3.3 Counter Test Procedure

a. Switch off the RF output of the signal generator

b. Press the RESOLUTION ▲ key five times until 00000000 is displayed

c. Switch on the RF output of the signal generator

d. Increase the signal generator output to 13 mV RMS

e. Adjust R150 slowly clockwise until the display just becomes unstable. Turn back until the display is just stable and indicates 100.000000 E6 ± 0.000001 E6

f. Reduce the signal generator output to 7 mV RMS. Verify that the GATE LED stops flashing. If it does not, repeat steps d to f

g. Switch off the counter. Disconnect the test equipment

6.7.4 Channel C Assembly (Model 1992 only)

6.7.4.1 Required Test Equipment

Item	Table 6.1, Item No.
Signal Generator	1
Coaxial Connecting Lead (Qty. 2)	7

6.7.4.1.1 Connect the test equipment as shown in Figure 6.25.

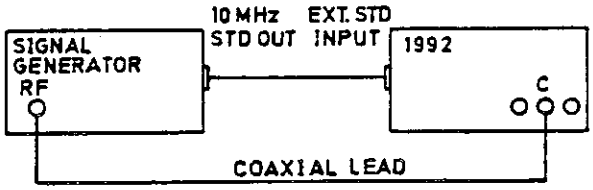


Figure 6.25 - Connections for Channel C Input System Adjustment

6.7.4.2 Counter Test Procedure

a. Set R27 on Channel C assembly fully clockwise

b. Switch the 1991/1992 on. Select FREQ C. Verify that the EXT STD LED is lit

c. Set the signal generator output to 1 GHz at a level of 8.0 mV RMS

d. Adjust R27 until the gate LED just starts flashing and the counter display indicates 1000.00000 E6 ± 0.00001 E6

e. Switch the output of the signal generator off. Reduce the output level to 7.5 mV RMS

f. Switch the output of the signal generator on. Verify that the counter is not counting. If it is, repeat steps c to f

g. Switch off the counter. Disconnect the test equipment

6.8 INTERNAL FREQUENCY STANDARD - ROUTINE CALIBRATION

6.8.1 Required Test Equipment

Item	Table 6.1, Item No.
Signal Generator	1
Coaxial Connecting Lead	7

6.8.2 Calibration Procedure

a. Switch on the 1991/1992. Select FREQ A and verify that 00000000 is displayed and allow at least 72 hours of uninterrupted operation

b. Connect the test equipment as shown in Figure 6.26

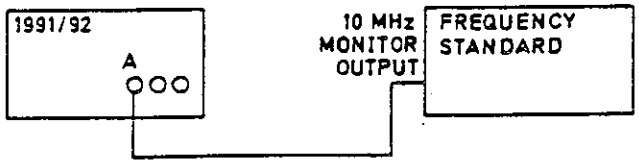


Figure 6.26 - Connections for Internal Frequency Standard Adjustment

c. Press [1] [0] [SHIFT] [EXP] [6] [SHIFT] [STORE] [X]

d. Press [SHIFT] [RECALL] [X]

Verify that 10.000000 E6 is displayed

e. Press [CONTINUE] and [SHIFT] [R-X/Z]

f. Adjust the internal frequency standard, via the aperture in the rear panel, to be as near to 10 MHz as possible. The display limits are shown in Table 6.3

g. Switch off the counter. Switch off and disconnect the test equipment

Table 6.3 - Internal Frequency Standard Accuracy

Frequency Standard	Display	Accuracy
Standard Oscillator	± 16 E0	1.6 parts in 10^6
Option 04A	± 3 E0	3 parts in 10^7
Option 04T	± 30 E-3	3 parts in 10^9
Option 04E	± 10 E-3	1 part in 10^9

6.9 OVERALL PERFORMANCE VERIFICATION PROCEDURE

6.9.1 Introduction

6.9.1.1 By correctly completing the following Performance Verification Procedures (PVPs), functional operation of the 1991/1992 is verified. The primary purpose of these tests is to provide a relatively fast and easy method for determining the operability of the counter. These PVPs should be performed in the order given.

6.9.1.2 These PVPs should be performed whenever it is necessary to determine whether the 1991/1992 is operating correctly. These tests may also be used as an incoming inspection procedure, or to verify a suspected failure. In addition, after diagnosing and repairing a 1991/1992 failure, these PVPs can be used to confirm a satisfactory repair.

6.9.1.3 Before beginning the performance check, ensure that the counter satisfactorily passes the preliminary functional check given in Subsection 2.6 of this manual.

6.9.1.4 The following conditions must be maintained throughout the performance check:

a. The instrument must be operated from an AC supply

b. The line voltage must be within 10% of the value indicated by the line voltage selector

c. The instrument covers must be installed

d. The ambient temperature must be 23°C ± 2°C

e. The power supply to the frequency standard must be uninterrupted

6.9.1.5 The instrument should be allowed to warm up for one hour (switched to standby, if required) before beginning the performance check.

6.9.2 Channel A Sensitivity PVP

6.9.2.1 Required Test Equipment

Item	Table 6.1, Item No.
Signal Generator	1
Digital Multimeter	3
Audio Oscillator	5
T-piece	8
Coaxial Connecting Lead (Qty. 2)	7

6.9.2.2 Channel A PVP (I)

a. Switch on the 1991/1992. Select 50Ω on Channel A

b. Connect the test equipment as shown in Figure 6.27. Check that the EXT STD LED lights

c. Set the signal generator output to the frequencies shown in Table 6.4 in turn. Set the counter's resolution to the corresponding value

d. At each frequency, determine the minimum input level to the counter which gives stable counting. Verify that this is not more than the level shown in Table 6.4

e. Disconnect the test equipment

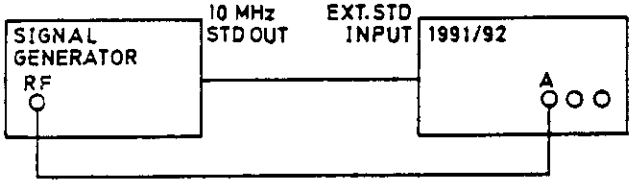


Figure 6.27 - Connections for Channel A Sensitivity PVP (I)

Table 6.4 - Channel A Sensitivity (I)

Frequency	1991/1992 Resolution	Signal Level
160 MHz	8 digits	50 mV
100 MHz	8 digits	25 mV
10 MHz	7 digits	25 mV
100 kHz	5 digits	25 mV

6.9.2.3 Channel A PVP (II)

a. Connect the test equipment as shown in Figure 6.28

b. Set the Audio Oscillator output to the frequencies shown in Table 6.5 in turn. Set the counter's resolution to the corresponding value

c. At each frequency, determine the minimum input level to the counter which gives stable counting. Verify that this is not more than the level shown in Table 6.5

d. Disconnect the test equipment

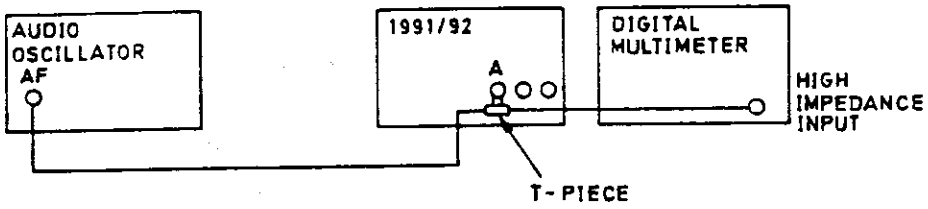


Figure 6.28 - Connections for Channel A Sensitivity PVP (II)

Table 6.5 - Channel A Sensitivity (II)

Frequency	1991/1992 Resolution	Signal Level
5 kHz	3	25 mV
10 Hz	3	25 mV

6.9.3 Channel B Sensitivity PVP

6.9.3.1 Required Test Equipment

Item	Table 6.1, Item No.
Signal Generator	1
Digital Multimeter	3
Audio Oscillator	5
T-piece	8
Coaxial Connecting Lead (Qty. 2)	7

6.9.3.2 Channel B PVP (I)

a. Select 50Ω on Channel B

b. Connect the test equipment as shown in Figure 6.29. Check that the EXT STD LED lights

c. Press [2] [1] [SHIFT] [STORE] [SF] [SHIFT] [SF]

d. Set the signal generator output to the frequencies shown in Table 6.6 in turn. Set the counter's resolution to the corresponding value

e. At each frequency, determine the minimum input level to the counter which gives stable counting. Verify that this is not more than the level shown in Table 6.6

f. Disconnect the test equipment

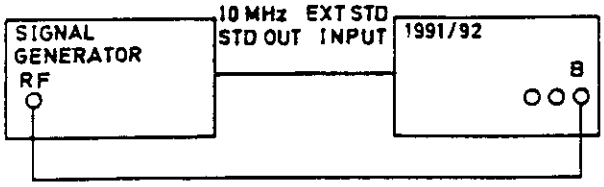


Figure 6.29 - Connections for Channel B Sensitivity PVP (I)

Table 6.6 - Channel B Sensitivity (I)

Frequency	1991/1992 Resolution	Signal Level
100 MHz	8 digits	25 mV
10 MHz	7 digits	25 mV
100 kHz	5 digits	25 mV

6.9.3.3 Channel B PVP (II)

a. Connect the test equipment as shown in Figure 6.30

b. Set the Audio Oscillator output to the frequencies shown in Table 6.7 in turn. Set the counter's resolution to the corresponding value

c. At each frequency, determine the minimum input level to the counter which gives stable counting. Verify that this is not more than the level shown in Table 6.7

d. Press [2] [0] [SHIFT] [STORE] [SF] [SHIFT] [SF]

e. Disconnect the test equipment

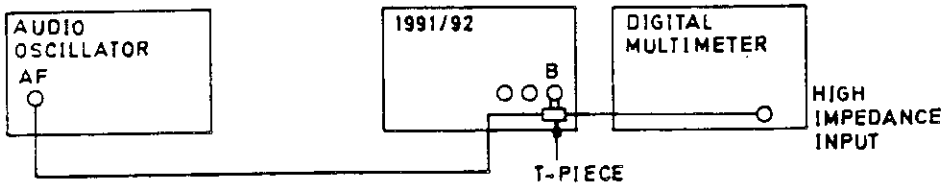


Figure 6.30 - Connections for Channel B Sensitivity PVP (II)

Table 6.7 - Channel B Sensitivity (II)

Frequency	1991/1992 Resolution	Signal Level
5 kHz	3	25 mV
10 Hz	3	25 mV

6.9.4 Channel C Sensitivity PVP (Model 1992 only)

6.9.4.1 Required Test Equipment

Item	Table 6.1, Item No.
Signal Generator	1
Coaxial Connecting Lead (Qty. 2)	7

6.9.4.2 Channel C PVP (Model 1992 only)

a. Connect the test equipment as shown in Figure 6.31

b. Select FREQ C

c. Set the signal generator output to the frequencies shown in Table 6.8 in turn. Set the counter's resolution to the corresponding value

d. At each frequency, determine the minimum input level to the counter which gives stable counting. Verify that this is not more than the level shown in Table 6.8

e. Disconnect the test equipment

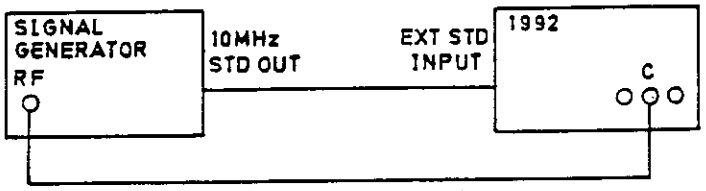


Figure 6.31 - Connections for Channel C Sensitivity PVP

Table 6.8 - Channel C Sensitivity

Frequency	1992 Resolution	Signal Level
40 MHz	8 digits	15 mV
100 MHz	8 digits	15 mV
500 MHz	8 digits	15 mV
1000 MHz	9 digits	15 mV
1300 MHz	9 digits	75 mV

6.9.5 External Standard Input Sensitivity PVP

6.9.5.1 Required Test Equipment

Item	Table 6.1, Item No.
Signal Generator	1

6.9.5.2 External Standard Input PVP

a. Connect the signal generator output to the EXT STD INPUT socket on the rear panel of the 1991/1992

b. Set the signal generator output to 10 MHz at a level of 10 mV RMS

c. Slowly increase the signal level until the counter's EXT STD LED lights steadily

d. Verify that the signal level is not more than 100 mV RMS

e. Disconnect the test equipment

6.9.6 10 MHz Standard Output Level PVP

6.9.6.1 Required Test Equipment

Item	Table 6.1, Item No.
Oscillator	2
T-piece	8
Load	9
Coaxial Connecting Lead	7

6.9.6.2 10 MHz Standard Output PVP

a. Connect the test equipment as shown in Figure 6.32

b. Verify that the peak-to-peak amplitude of the displayed waveform is greater than 600 mV into 50 ohms. Verify that the mark/space ratio is between 30:70 and 70:30

c. Disconnect the test equipment

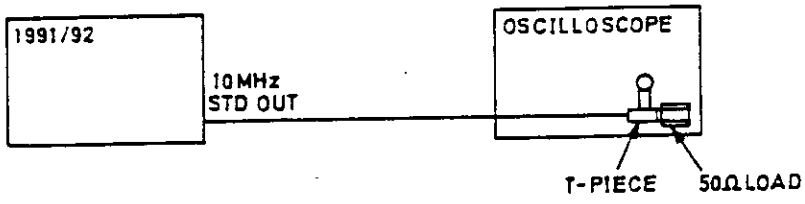


Figure 6.32 - Connections for 10 MHz Standard Output Level PVP

6.9.7 **Minimum Time Interval PVP**

6.9.7.1 **Required Test Equipment**

Item	Table 6.1, Item No.
Signal Generator	1

6.9.7.2 a. Connect the test equipment as shown in Figure 6.33

b. Select 50Ω on Channel A, T.L. A→B, and COM A

c. Set the signal generator output to 100 MHz at a level of 1V

d. Verify that a display of 0 ± 2ns is obtained

e. Disconnect the test equipment

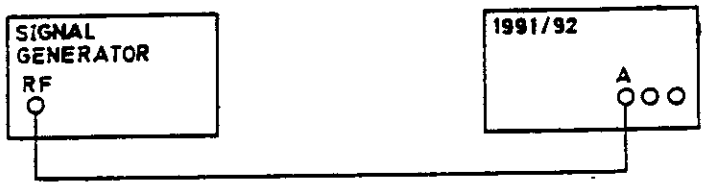


Figure 6.33 - Connections for Minimum Time Interval PVP

6.9.8 **External Arming PVP**

6.9.8.1 **Required Test Equipment**

Item	Table 6.1, Item No.
Signal Generator	1
Pulse Generator	6
Coaxial Connecting Lead (Qty. 3)	7

6.9.8.2 a. Select 50Ω on Channel A and FREQ A. Press the RESOLUTION ↓ key three times until 00000 is displayed

b. Connect the test equipment as shown in Figure 6.34

c. Set the signal generator output to 10 MHz at a level of 200 mVRMS

d. Prepare the pulse generator to give a single, 300 µs, positive-going pulse with a low level of +0.4V and a high level of +2.4V (TTL limit levels)

e. Press [1] [6] [SHIFT] [STORE] [SF] [SHIFT] [SF]

f. Verify that the instrument is not counting

g. Trigger the pulse generator to obtain a single pulse output

h. Verify that the display indicates 10.0000 E6 Hz ±1 count and that the instrument is not continuously gating

i. Press [1] [0] [SHIFT] [STORE] [SF] [SHIFT] [SF]

j. Disconnect the test equipment

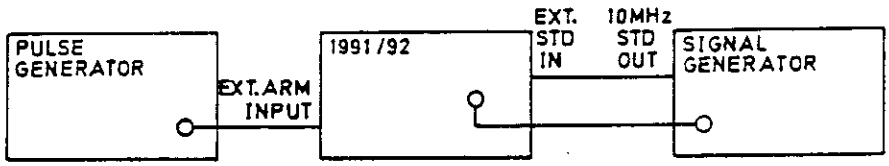


Figure 6.34 - Connections for External Arming PVP

6.9.9 Trigger Level PVP

6.9.9.1 Required Test Equipment

Item	Table 6.1, Item No.
Oscilloscope with Probe	2
Digital Multimeter	3

6.9.9.2 Trigger Level PVP (I)

a. Connect the test equipment as shown in Figure 6.35

b. Select DC coupling of the oscilloscope input

c. Set the oscilloscope to monitor a waveform of approximately 10V peak-to-peak with a frequency of approximately 2 Hz

d. Select CHECK

e. Press [7] [6] [SHIFT] [STORE] [SF] [SHIFT] [SF]

f. Verify that the Channel A and B TRIG LEDs are flashing and that the displayed waveform is as shown in Figure 6.36

g. Transfer the oscilloscope probe to the Channel B TRIG LEVEL OUTPUT pin and verify that the same waveform is displayed

h. Press [7] [0] [SHIFT] [STORE] [SF] [SHIFT] [SF]

i. Disconnect the test equipment

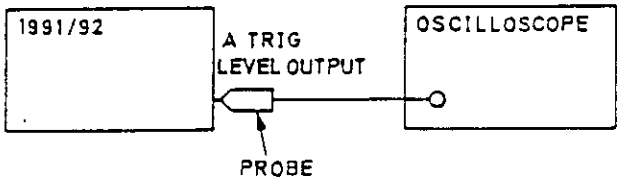


Figure 6.35 - Connections for Trigger Level PVP (I)

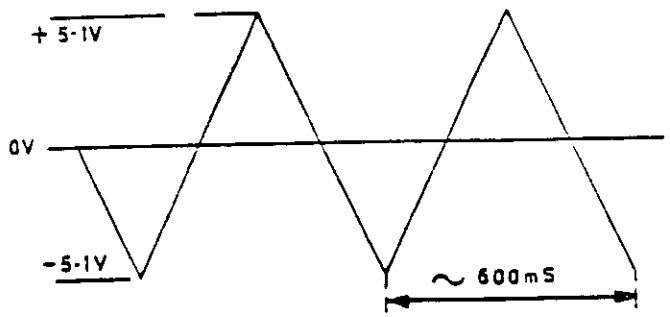


Figure 6.36 - Trigger Level Waveform

6.9.9.3 Trigger Level PVP (II)

a. Connect the test equipment as shown in Figure 6.37

b. Set the multimeter to measure DC volts

c. Press [TRIG LEVEL] [5] [TRIG LEVEL] on Channels A and B

d. Verify that the multimeter indicates +5V ± 60 mV

e. Transfer the probe to the Channel B TRIG LEVEL OUTPUT pin and verify that the multimeter indicates +5V ± 60 mV

f. Press [TRIG LEVEL] [0] [TRIG LEVEL] on Channels A and B

g. Verify that the multimeter indicates 0V ± 10 mV

h. Transfer the probe to the Channel A TRIG LEVEL OUTPUT pin and verify that the multimeter indicates 0V ± 10 mV

i. Press [TRIG LEVEL] [5] [SHIFT] [±] [TRIG LEVEL]

j. Verify that the multimeter indicates -5V ± 60 mV

k. Transfer the probe to the Channel B TRIG LEVEL OUTPUT pin and verify that the multimeter indicates -5V ± 60 mV

l. Disconnect the test equipment

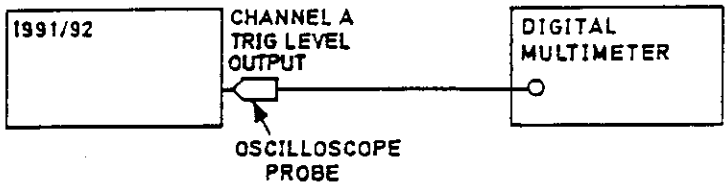


Figure 6.37 - Connections for Trigger Level PVP (II)

6.9.10 Internal Frequency Standard PVP

6.9.10.1 Required Test Equipment

Item	Table 6.1, Item No.
Frequency Standard	4
Coaxial Connecting Lead	7

6.9.10.2 a. Switch on the 1991/1992. Select FREQ A and verify that 00000000 is displayed. Allow 72 hours of uninterrupted operation

b. Connect the test equipment as shown in Figure 6.38

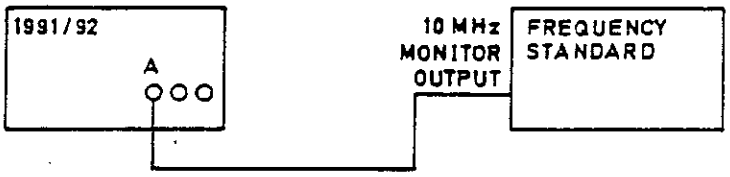


Figure 6.38 - Connections for Internal Frequency Standard PVP

c. Press [1] [0] [SHIFT] [EXP] [6] [SHIFT] [STORE] [X]

d. Press [SHIFT] [RECALL] [X]
Verify that 10.000000 E6 is displayed

e. Press [CONTINUE] and [SHIFT] [R-X/Z]

f. Verify that the value displayed is within the limits shown in Table 6.9

g. Switch off the 1991/1992. Switch off and disconnect the test equipment

Table 6.9 - Internal Frequency Standard Accuracy

Frequency Standard	Display	Accuracy
Standard Oscillator	± 16 E0	1.6 parts in 10^6
Option 04A	± 3 E0	3 parts in 10^7
Option 04T	±300 E-3	3 parts in 10^8
Option 04E	±300 E-3	3 parts in 10^8

SECTION 7 DRAWINGS

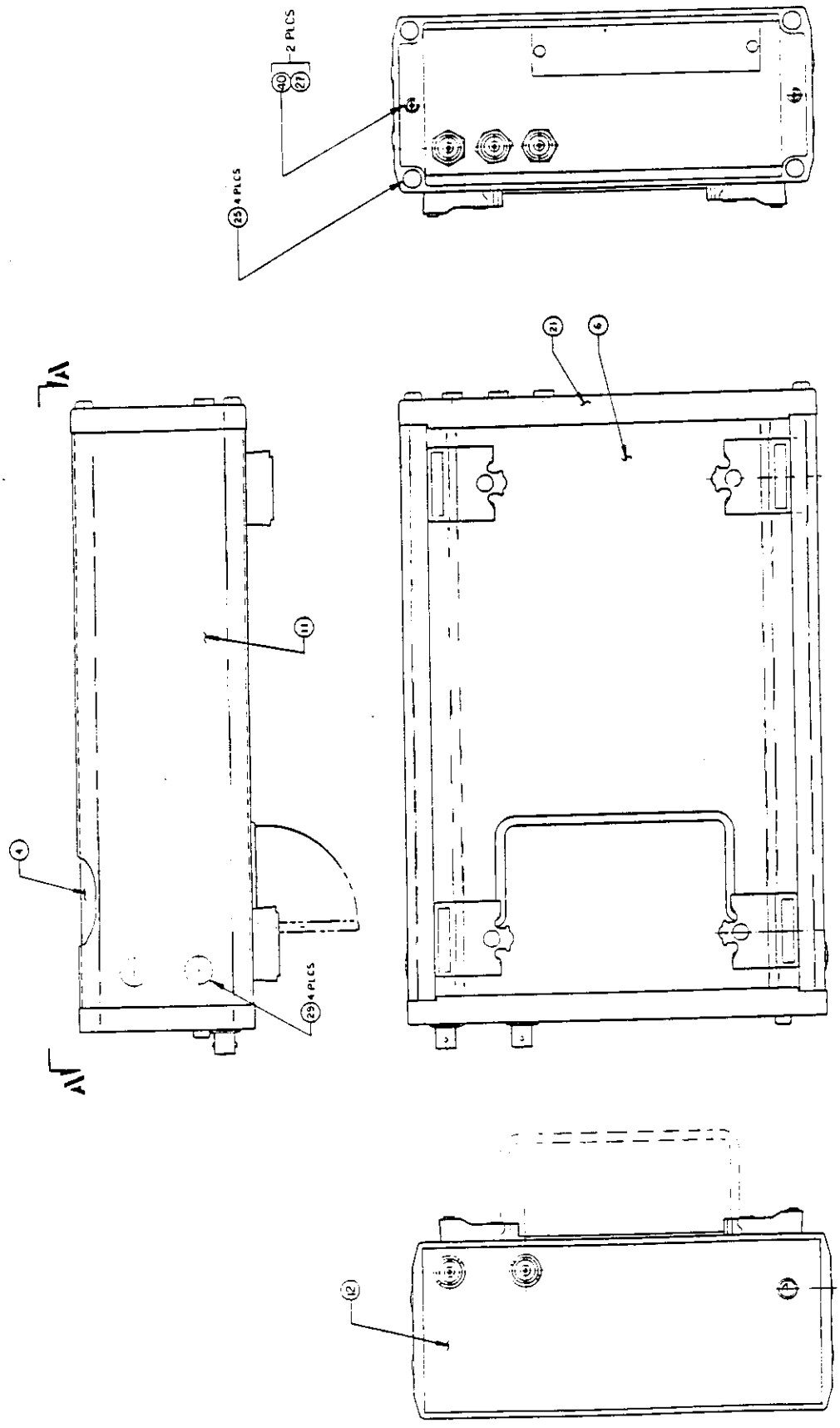


Figure 7.1A - Final Assembly, 1991 (404577)

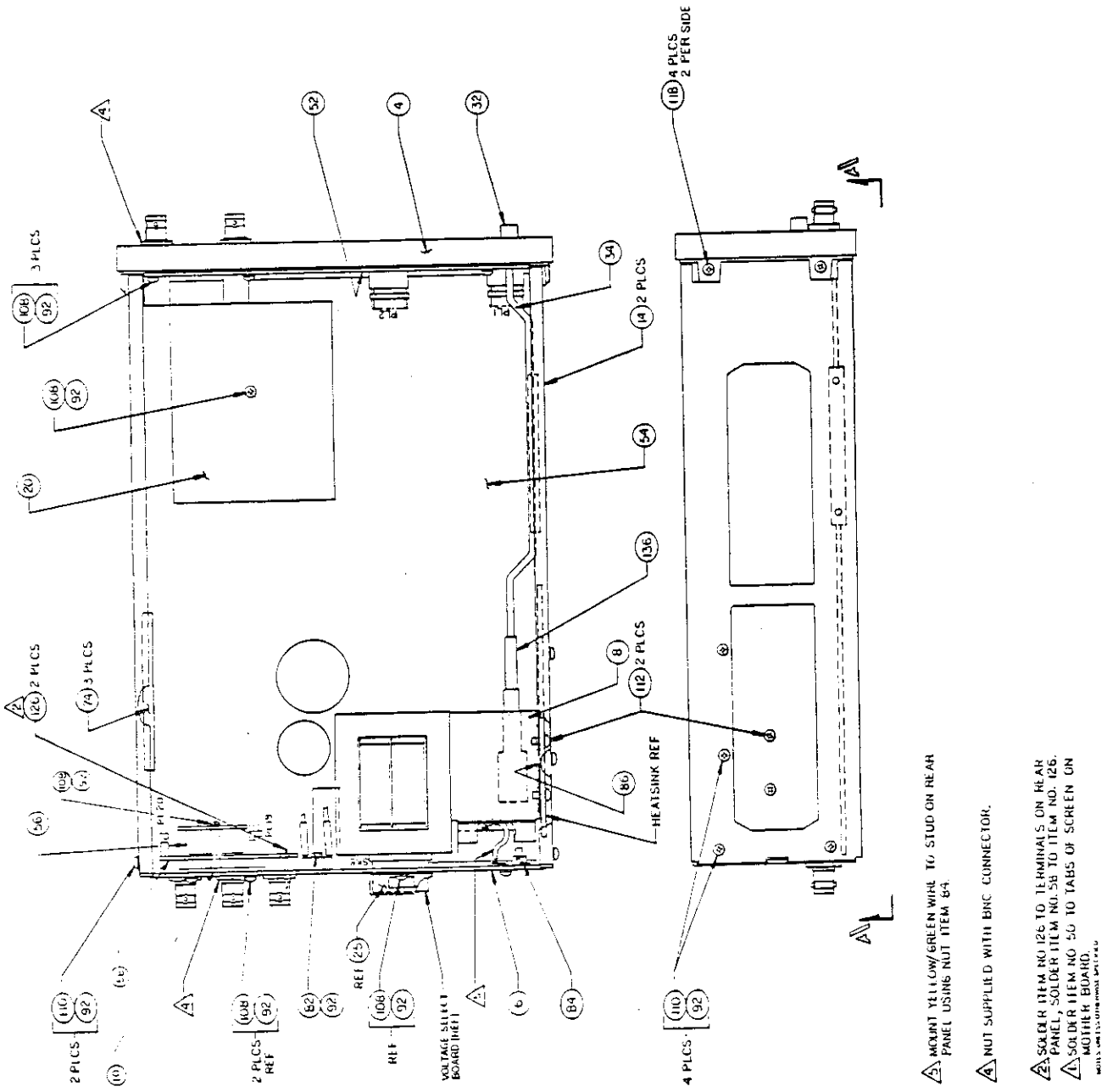


Figure 7.1B - Chassis Assembly, 1991 (404576)

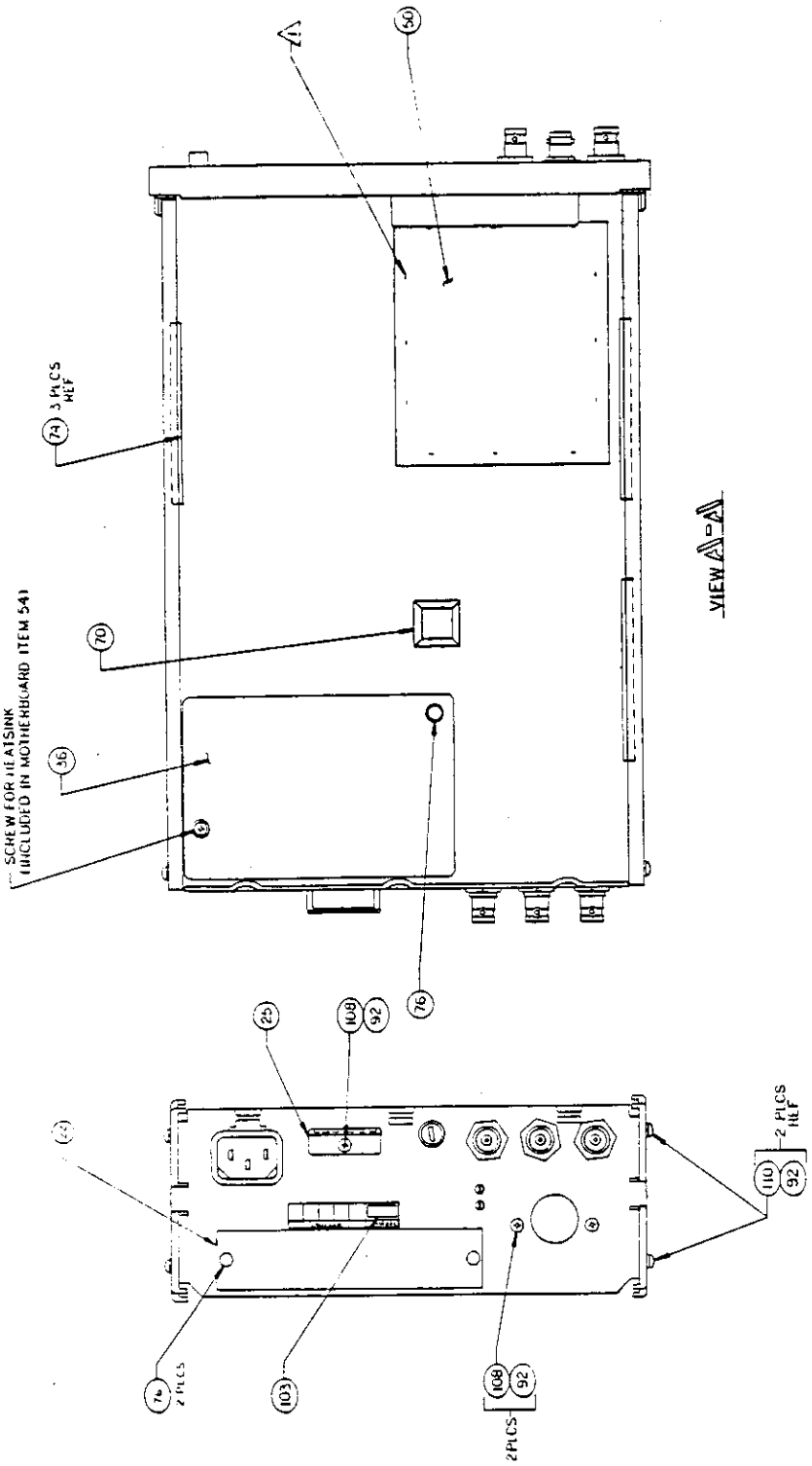


Figure 7.1B - Chassis Assembly, 1991 (404576) (Cont'd)

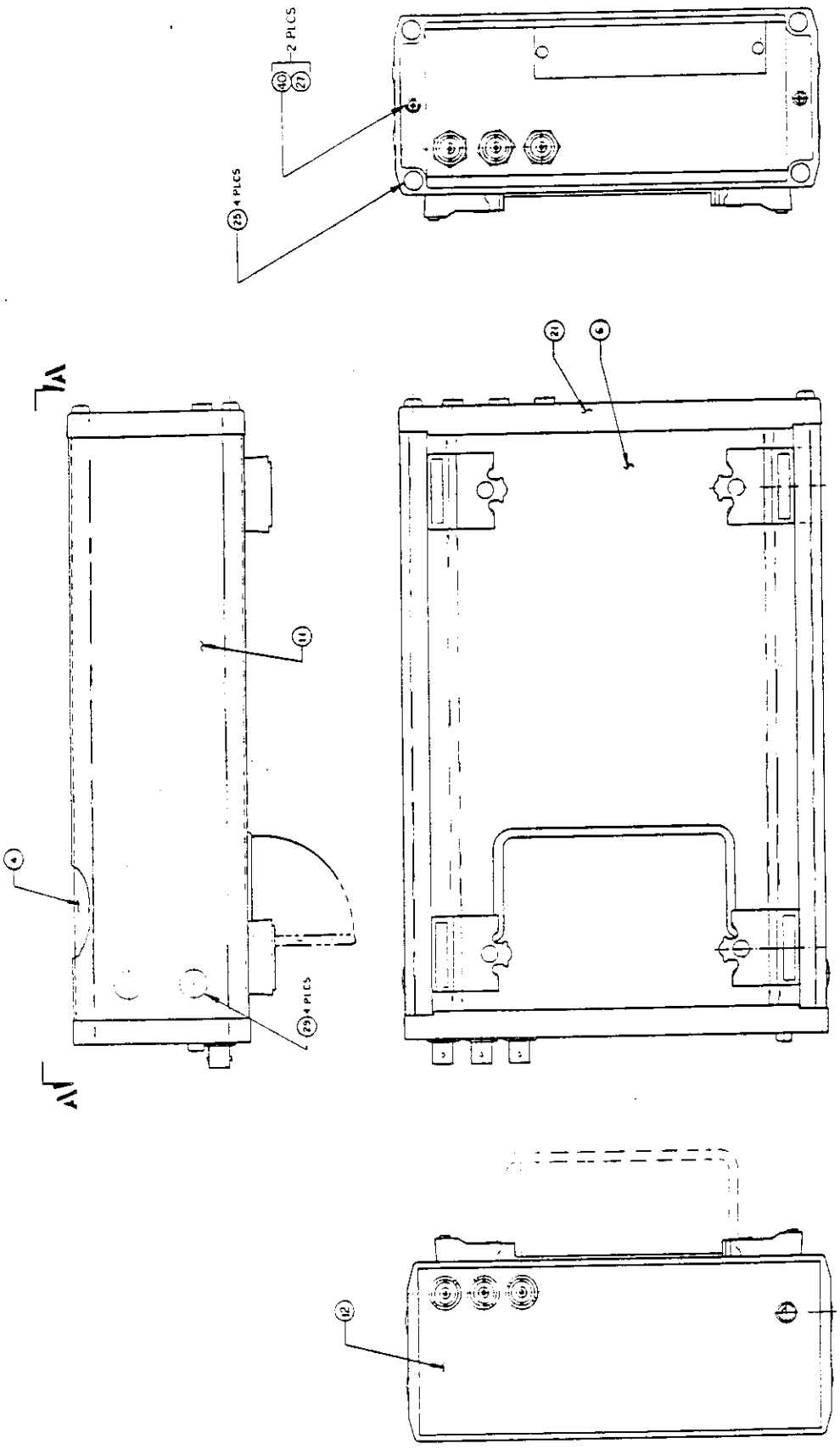
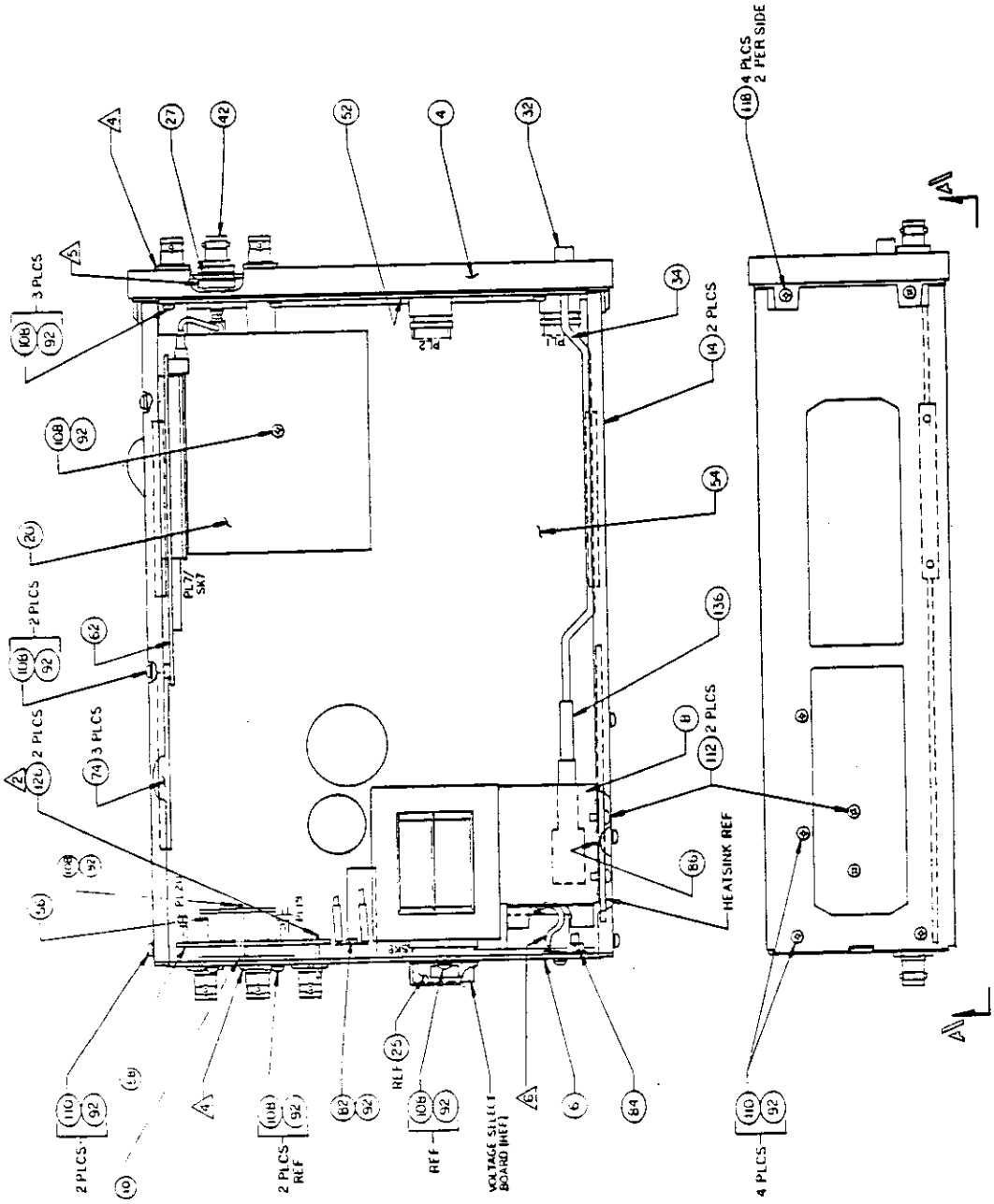


Figure 7.1C - Final Assembly, 1992 (404571)



6 MOUNT YELLOW/GREEN WIRE TO STUD ON REAR PANEL USING NUT ITEM 84

5 NUT AND WASHER SUPPLIED WITH ITEM 42.

4 NUT SUPPLIED WITH BNC CONNECTOR.

3 SOLDER ITEM NO 126 TO TERMINALS ON REAR PANEL, SOLDER ITEM NO 58 TO ITEM NO. 126.

2 SOLDER ITEM NO 50 TO TABS OF SCREEN ON MOTHER BOARD.

Figure 7.1D - Chassis Assembly, 1992 (404572)

REV. A

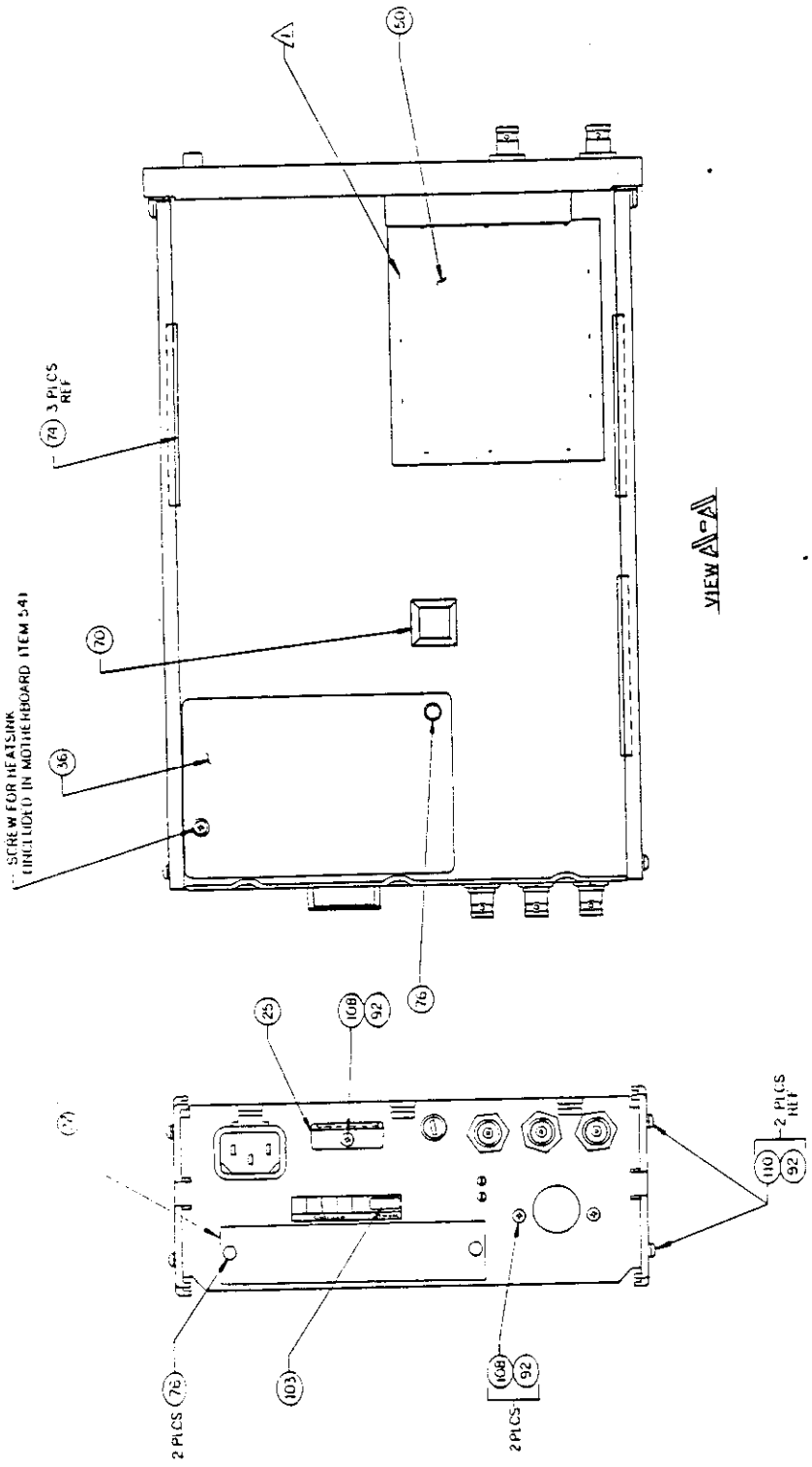
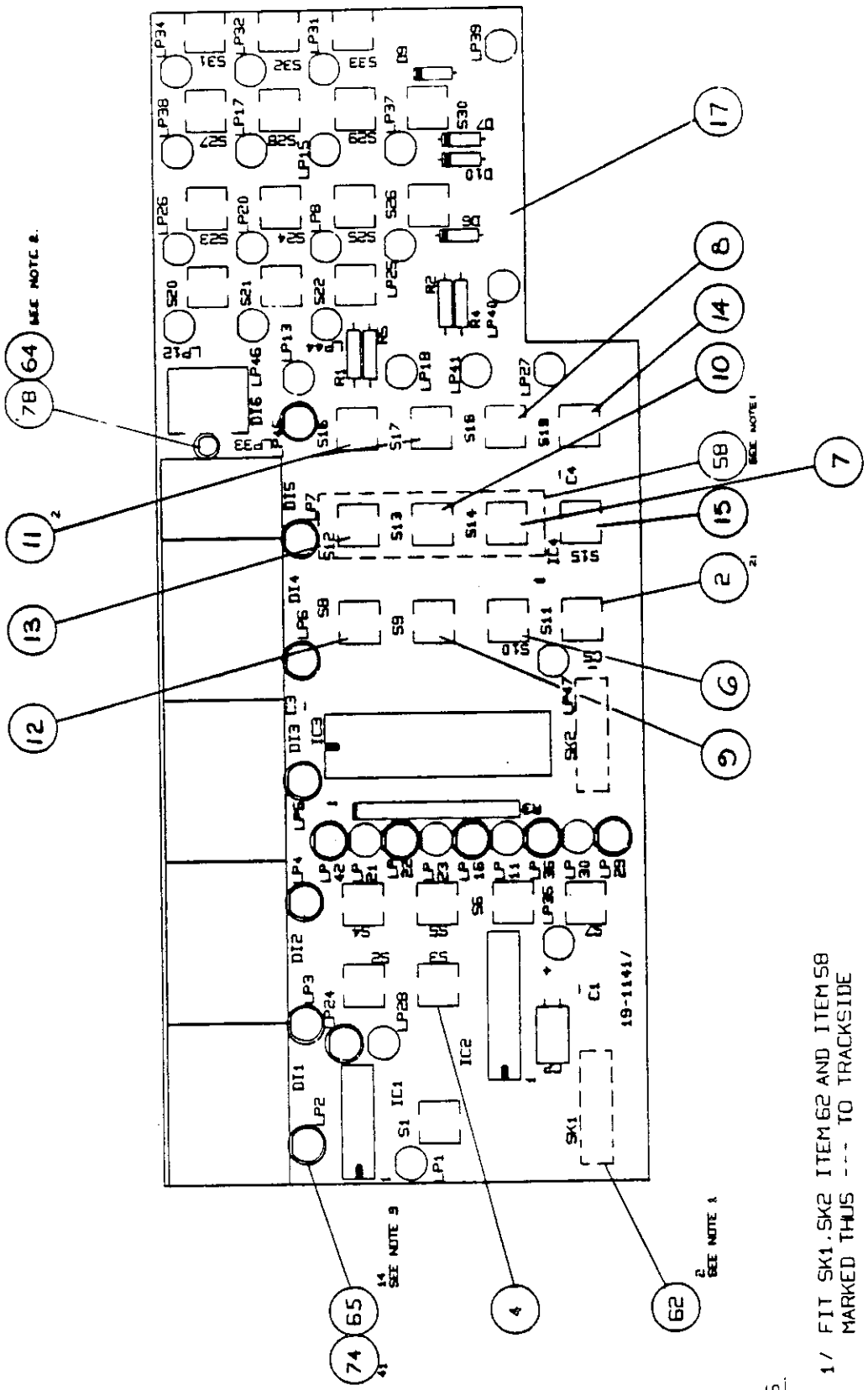


Figure 7.1D - Chassis Assembly, 1992 (404572) (Cont'd)



NOTES

1/ FIT SK1, SK2 ITEM 62 AND ITEM 58 MARKED THUS --- TO TRACKSIDE

2/ FIT SLEEVING ITEM 64 TO LED ITEM 78 IN 1 POSITION.

3/ FIT SLEEVING ITEM 65 TO LED ITEM 74 IN 13 POSNS LP 2-7 ,16,22,24,29,36, 42,45

Figure 7.2 - Component Layout, Display (19-1141)

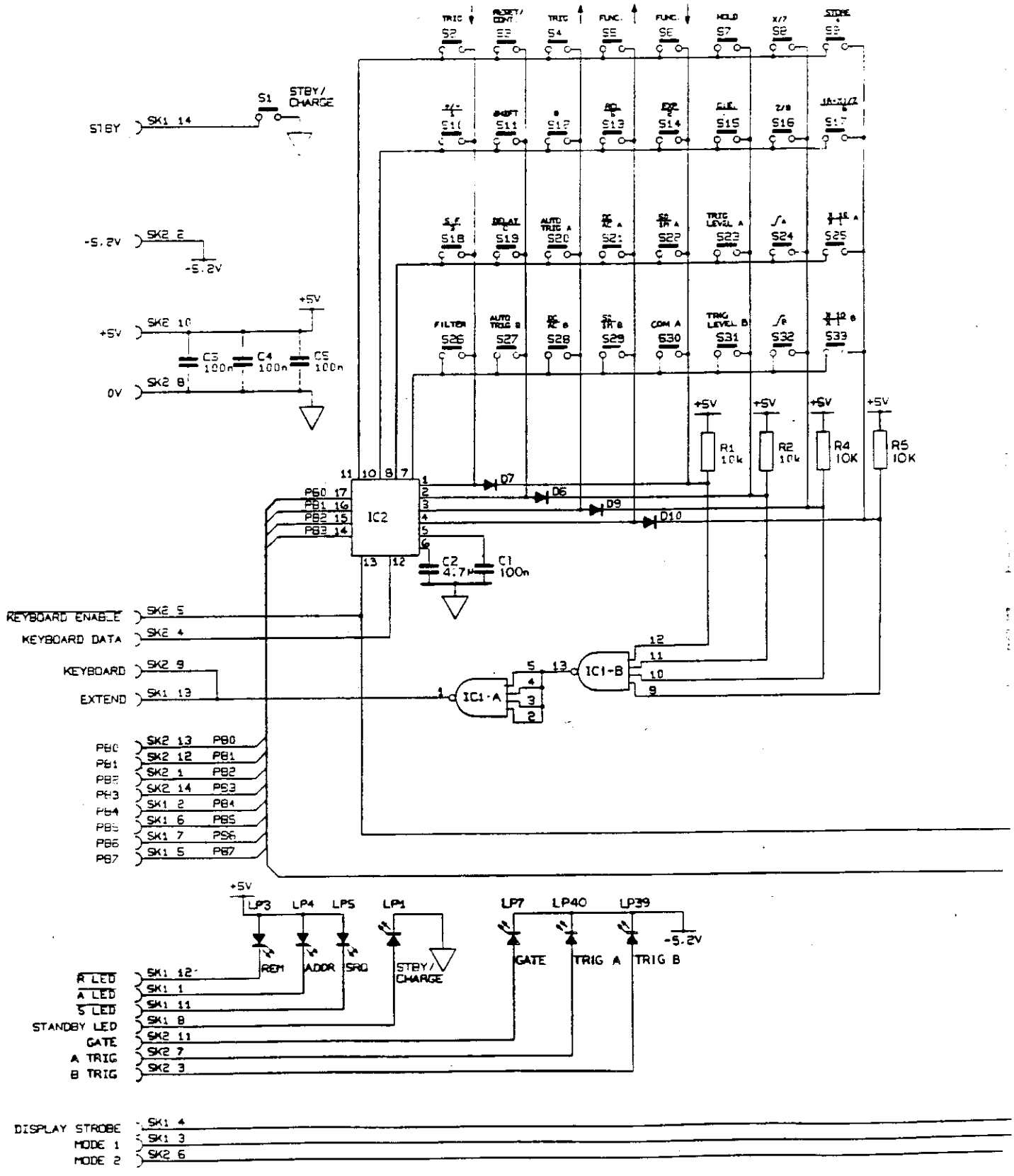
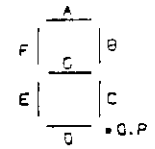


Figure 7.3 - Circuit Diagram, Display (19-1141)

REV. A

REFERENCE	TYPE NO.	PART NO.	+5V	0V
D6,7,9,10	IN4149	A-22-1029		
IC1	4012	A-22-4754	14	7
IC3,4	7513AIOI	2504S7	18	29
IC2	74C922	A-22-4779	16	9
DI6	HD1105	A-26-1511		
DI1-4	MAN6910	A-26-1512		
DI5	MAN6960	A-26-1513		
LP33	LED RED	A-26-5018		
LP1-8,11-13	LED RED	A-26-5026		
15-18,20-32				
34-42,44-47				

COMPONENT REFERENCE	
R1-5	LP1-8,11-13
C1-5	15-18,20-42
D6,7,9,10	44-47
IC1-4	
DI1-6	
S1-33	
SK1,2	



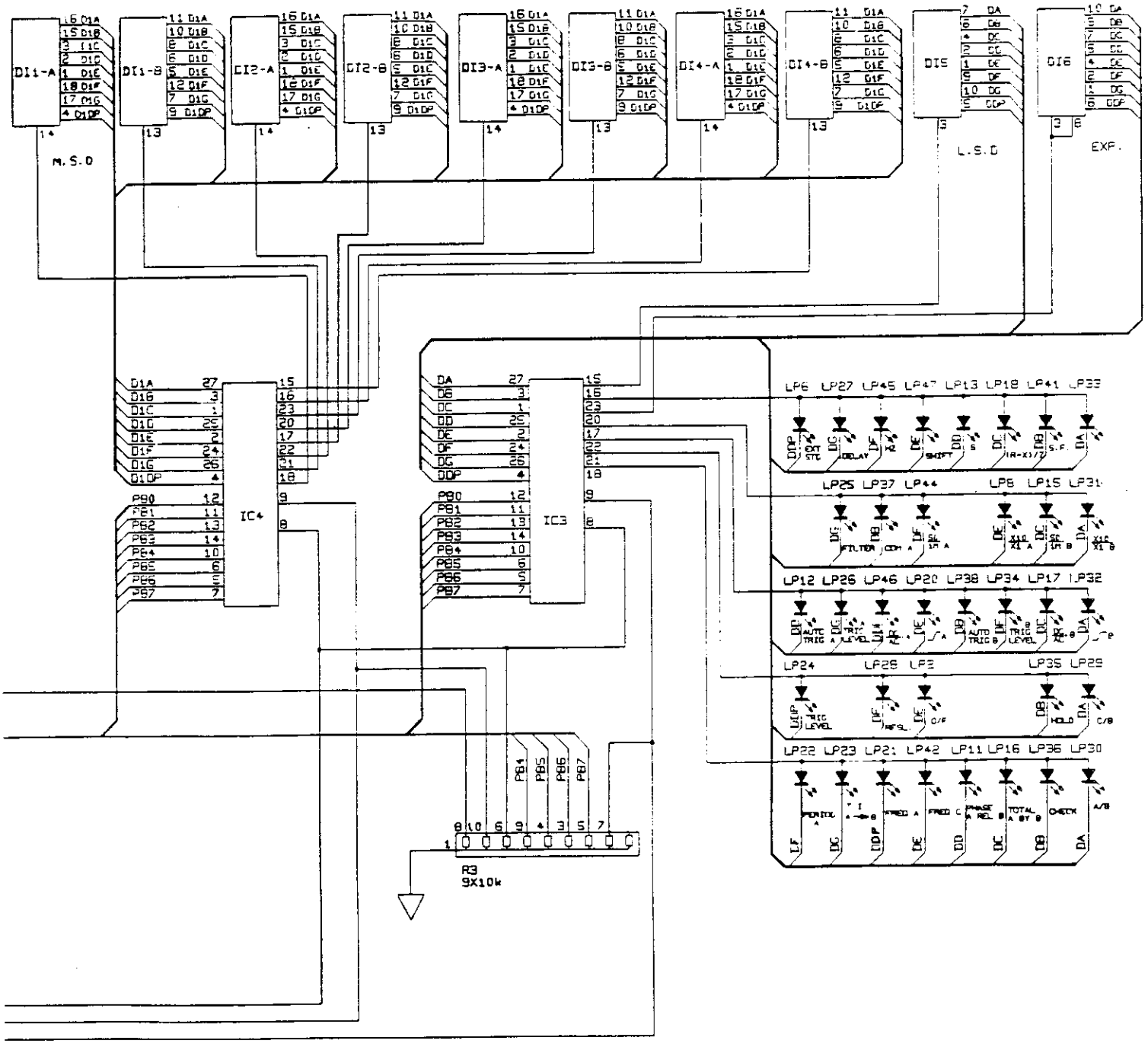


Figure 7.3 – Circuit Diagram, Display (19-1141) (Cont'd)

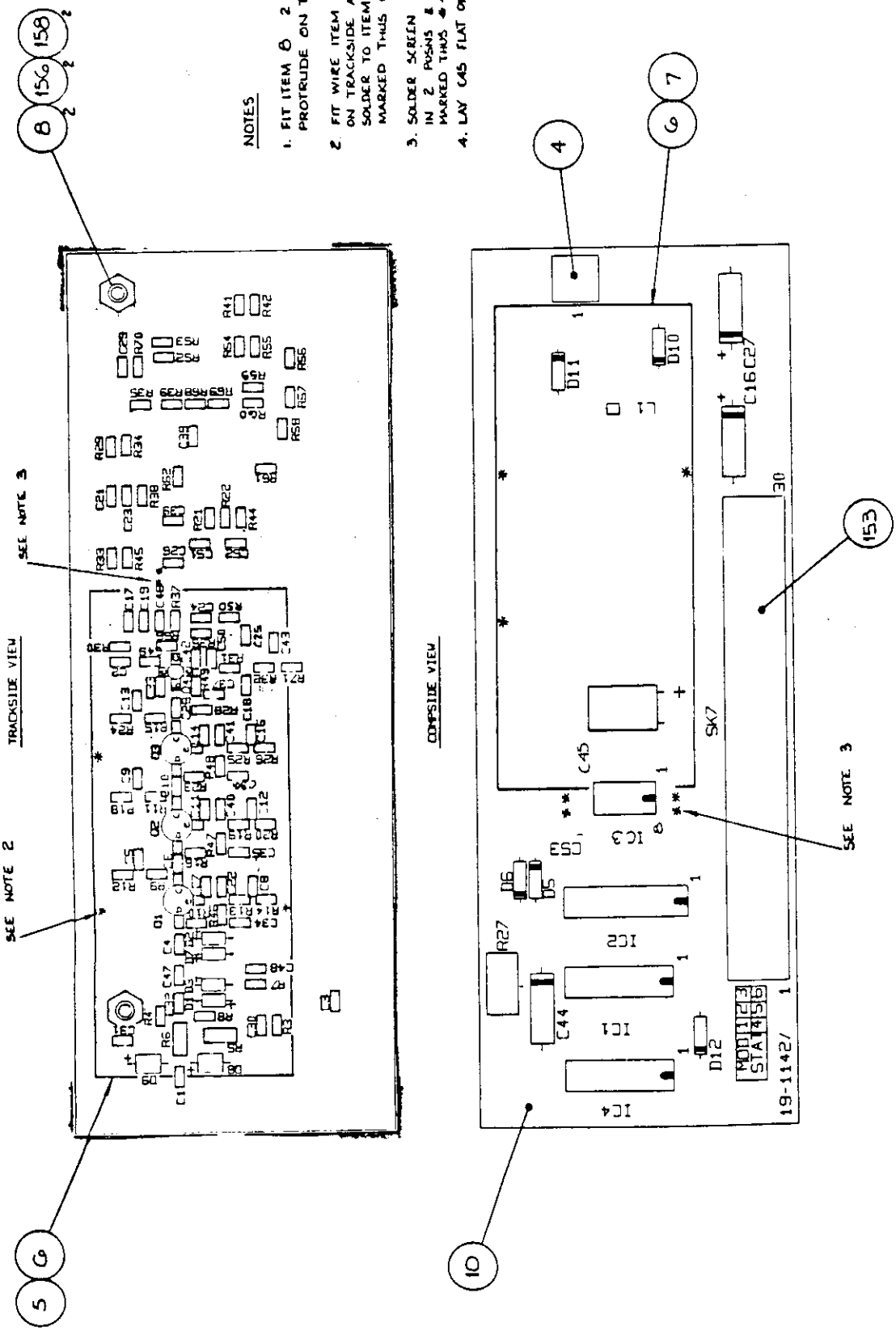


Figure 7.4 - Component Layout, Channel C (19-1142)

REV.

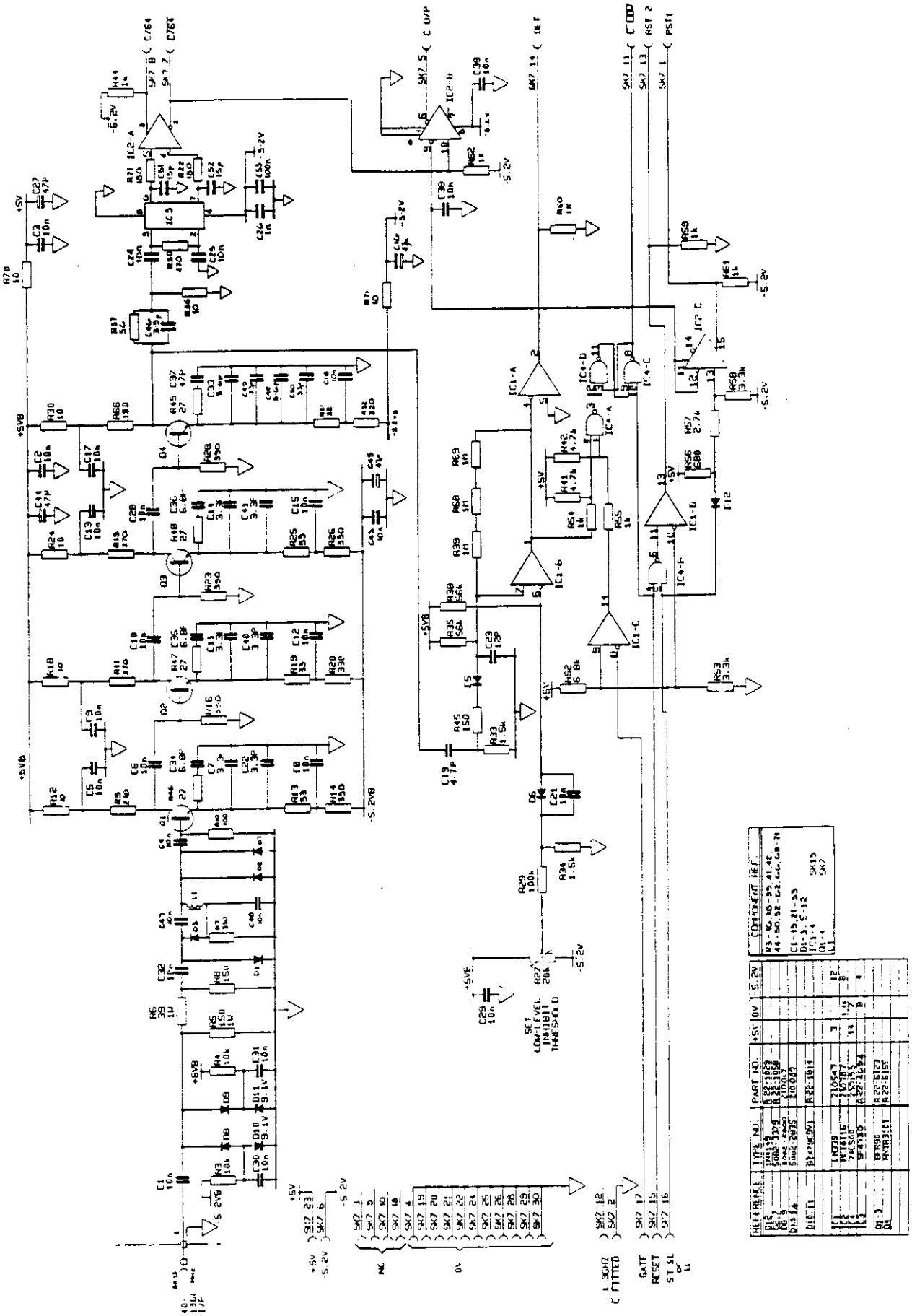


Figure 7.5 - Circuit Diagram, Channel C (19-1142)

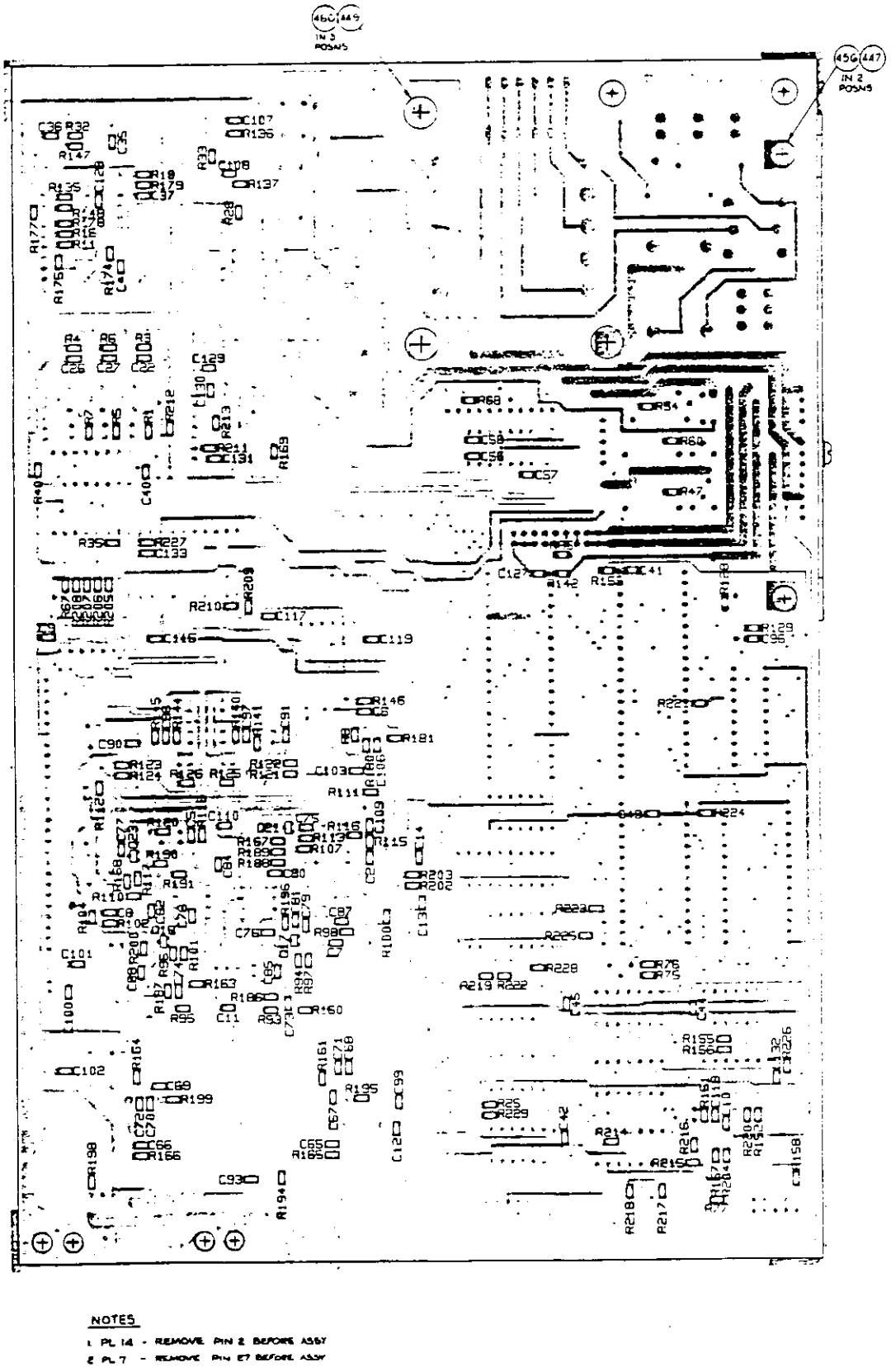


Figure 7.6 - Component Layout, Motherboard (19-1145)

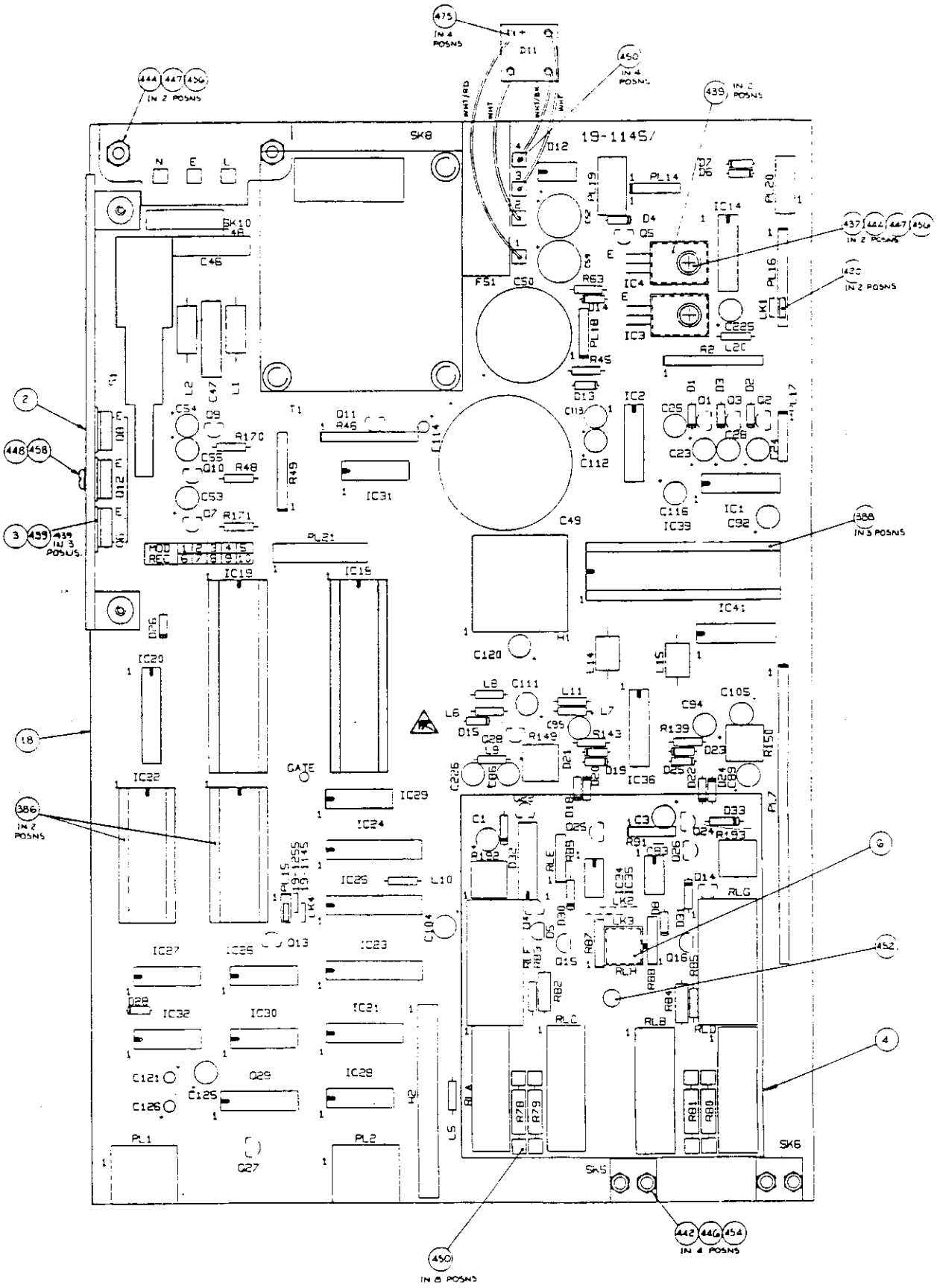
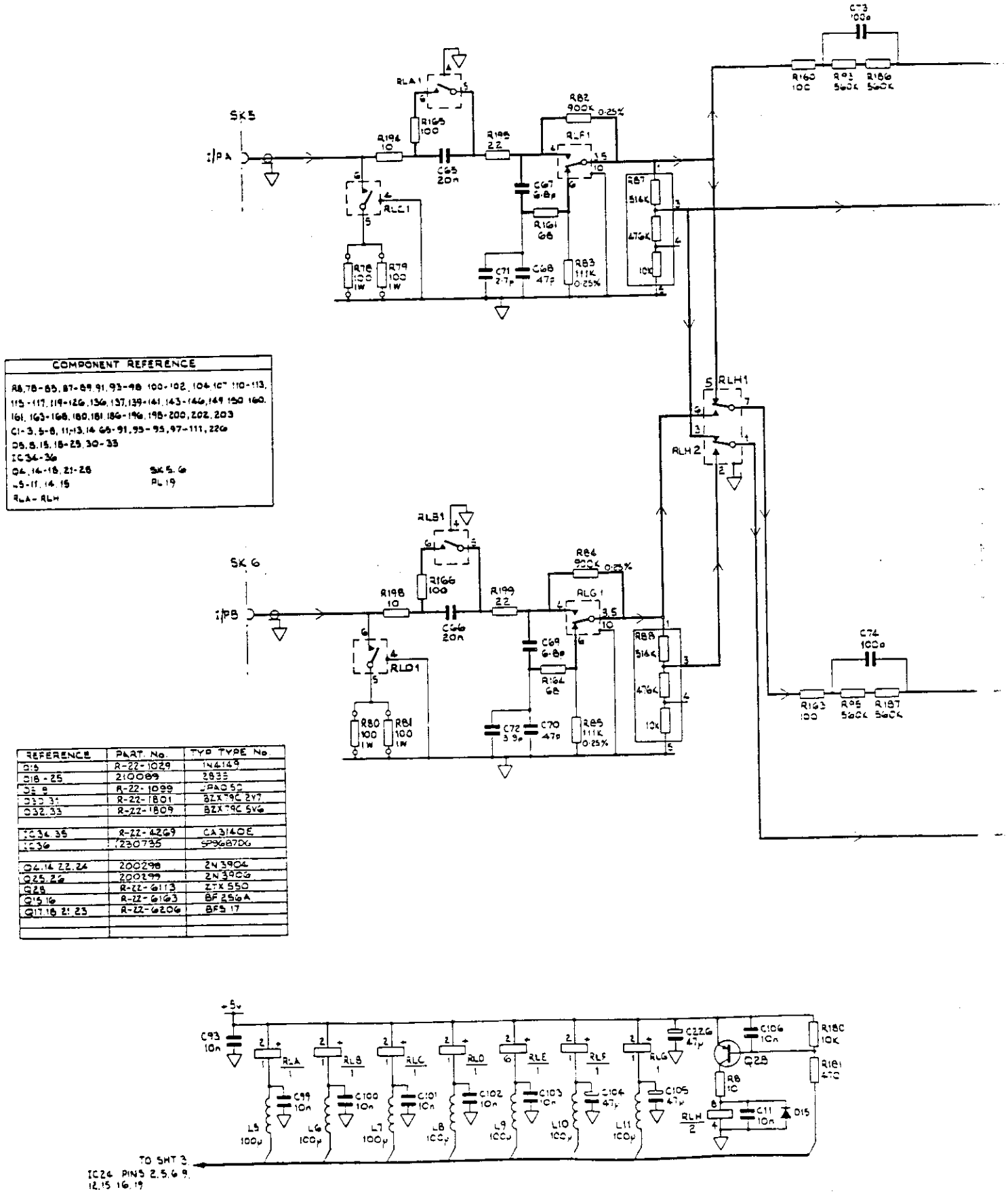


Figure 7.6 - Component Layout, Motherboard (19-1145) (Cont'd)



REFERENCE	PART No.	TYP TYPE No.
D5	R-22-1029	IN4148
D18-25	210089	2835
D8	R-22-1099	UPAD52
D30,31	R-22-1801	BZX79C 2V7
D32,33	R-22-1809	BZX79C 5V6
IC34,35	R-22-4269	CA3140E
IC36	7230735	SP96B7DG
Q4,14,22,24	200298	2N3904
Q25,26	200299	2N3906
Q28	R-22-6113	ZTX550
Q15,16	R-22-6163	BF256A
Q17,18,21,23	R-22-6206	BF517

 Figure 7.7 - Circuit Diagram, Motherboard (19-1145)

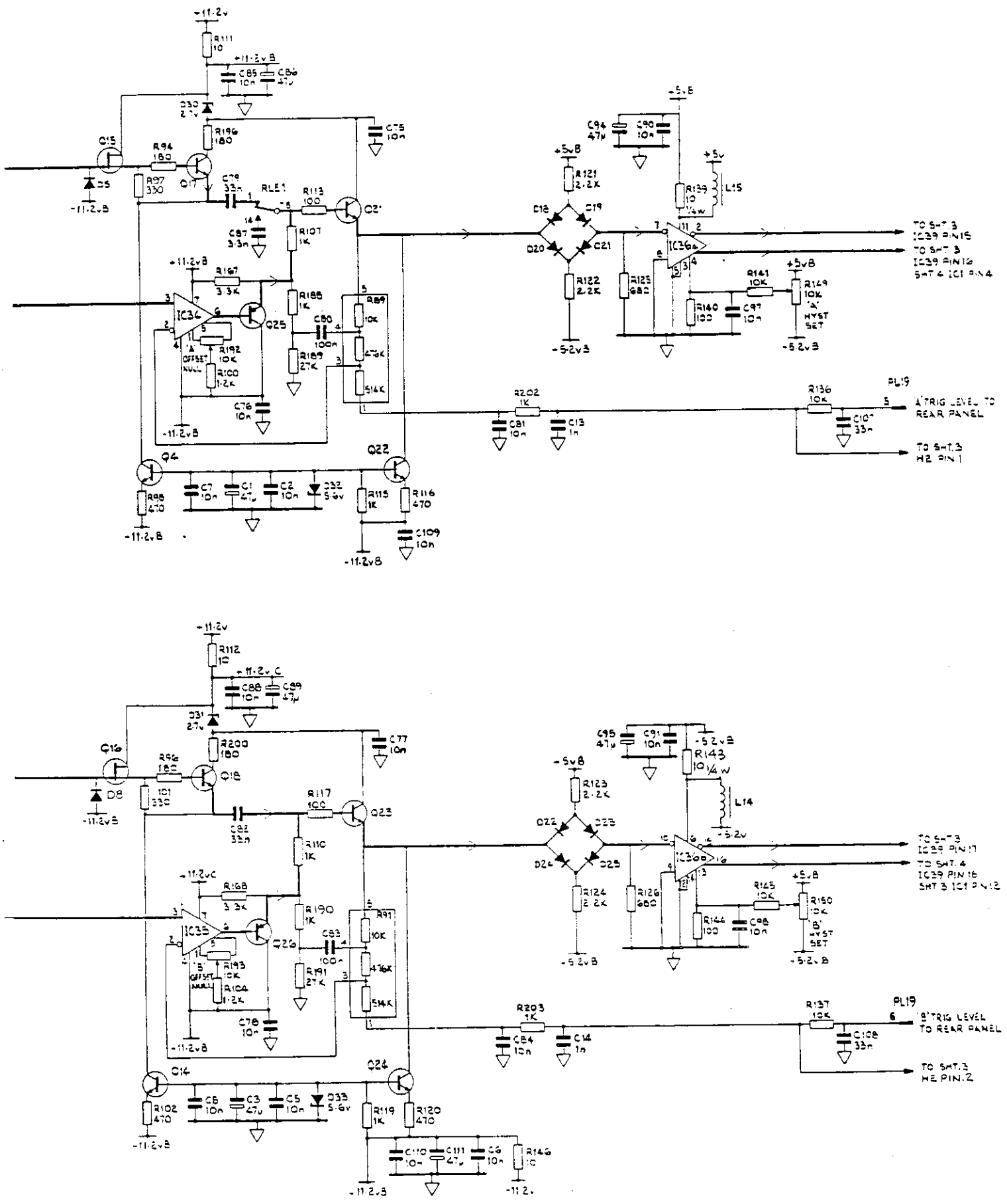
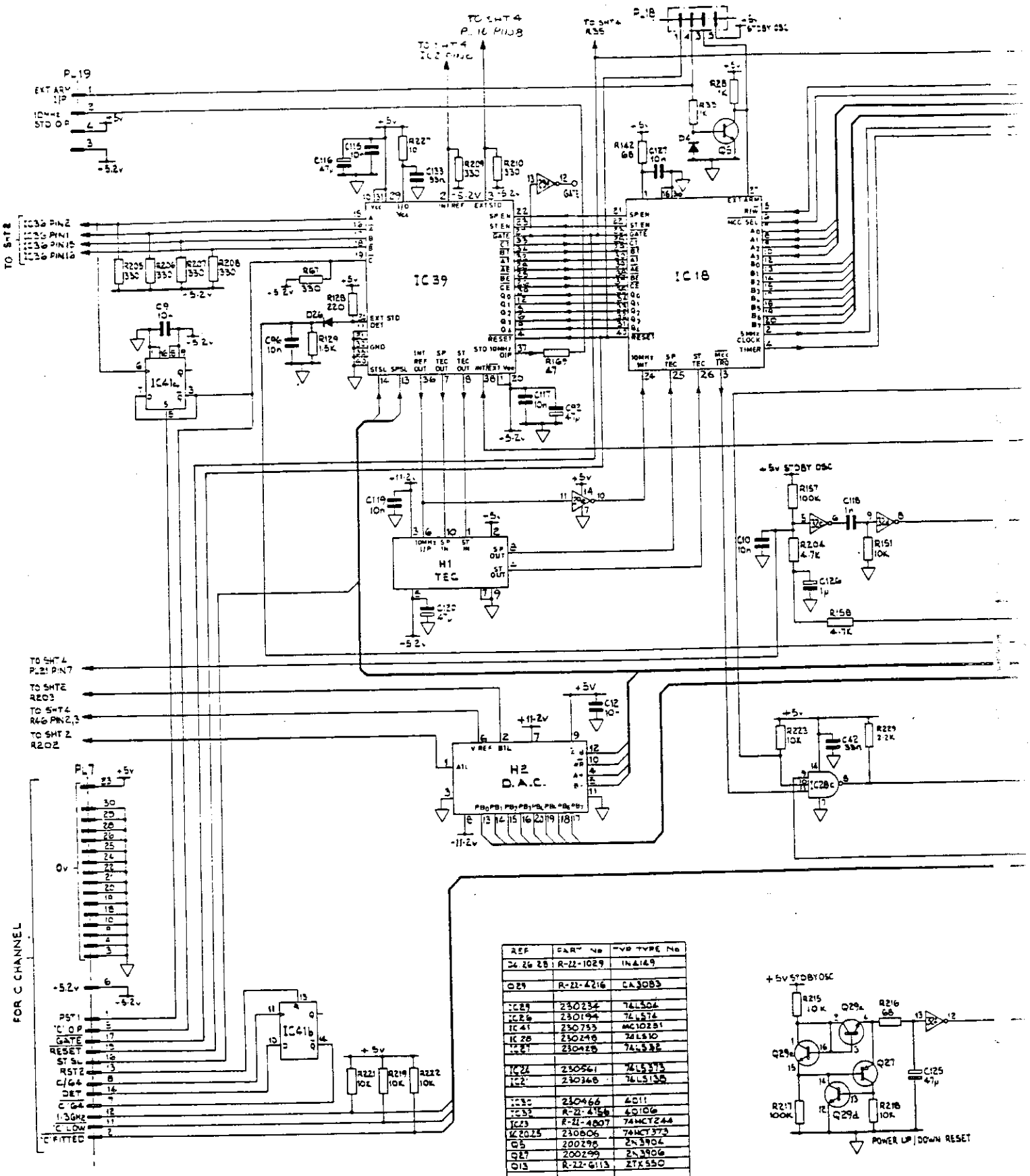


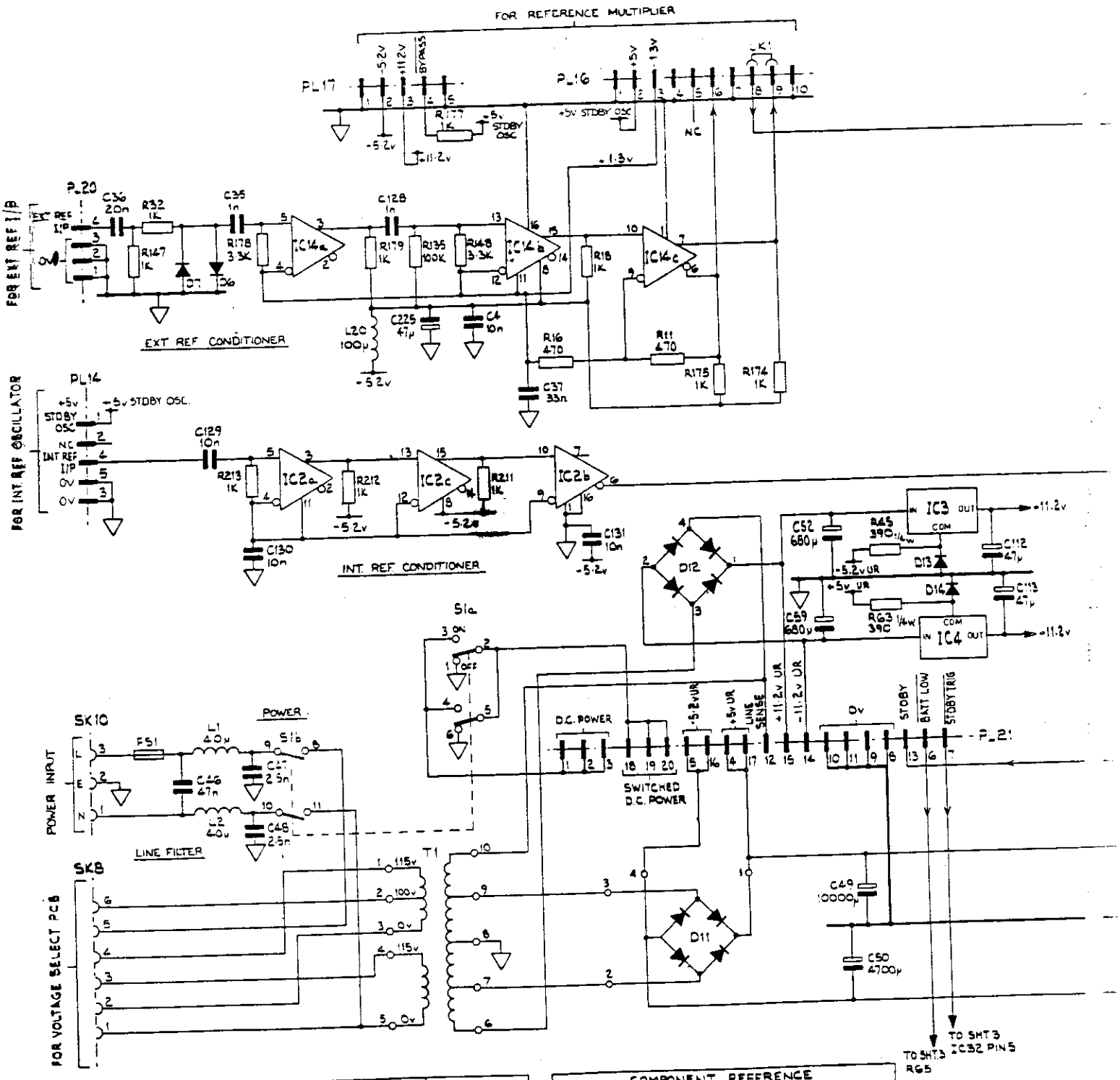
Figure 7.7 – Circuit Diagram, Motherboard (19-1145) (Cont'd)



REF	PART No	PVD TYPE No
24 26 28	R-22-1029	IN4149
Q29	R-22-4216	CA3083
IC29	230234	74LS04
IC26	230194	74LS74
IC41	230753	MC10231
IC28	230249	74LS10
IC27	230428	74LS32
IC24	230561	74LS373
IC21	230368	74LS138
IC30	230466	4011
IC33	R-22-4156	40106
IC23	R-22-4807	74HCT244
IC2025	230806	74HCT373
Q5	200298	2N3904
Q27	200299	2N3906
Q13	R-22-6113	ZTX550
IC19	R-22-8307	146805E2
IC18	230790	MCC1
IC39	230789	MCC2
IC22	230867	27128

Figure 7.8 -
Circuit Diagram, Motherboard (19-1145) (Cont'd)

REV. D



REF	PART No	TYP TYPE No
D1-3,6,7,13,14	R-22-1029	1N4149
D11	R-22-1662	VH248
D12	R-22-1664	B40C800
IC3	230200	7812CT
IC31	R-22-9262	MC3403
IC4	230201	7912CT
IC12,14	230787	10116
IC2	230750	10216

REF	PART No	TYP TYPE No
Q11	200298	2N3904
Q1-3	R-22-6018	MPS3640
Q9,10	R-22-6112	ZTX450
Q7	R-22-6113	ZTX550
Q6	200302	BDT91
Q8,12	200301	BDT92

COMPONENT REFERENCE	
R1-7,11,16,18,32,35,40,45-49,54,60 63,68,135,147,148, 159,170,171,174,175,177-179,211-213 226 C4,22-28,35-37,40,41,46-50 52-59 112-114 128-132, 225	FS1
D1-3,6,7,11-14,	B1 LK1
IC1-4,14,31	T1
Q1-3 6-12	SKB,10
L1,2,20	PL2,14,16,17,20,21

REV

Figure 7.9 - Circuit Diagram, Motherboard (19-1145) (Cont'd)

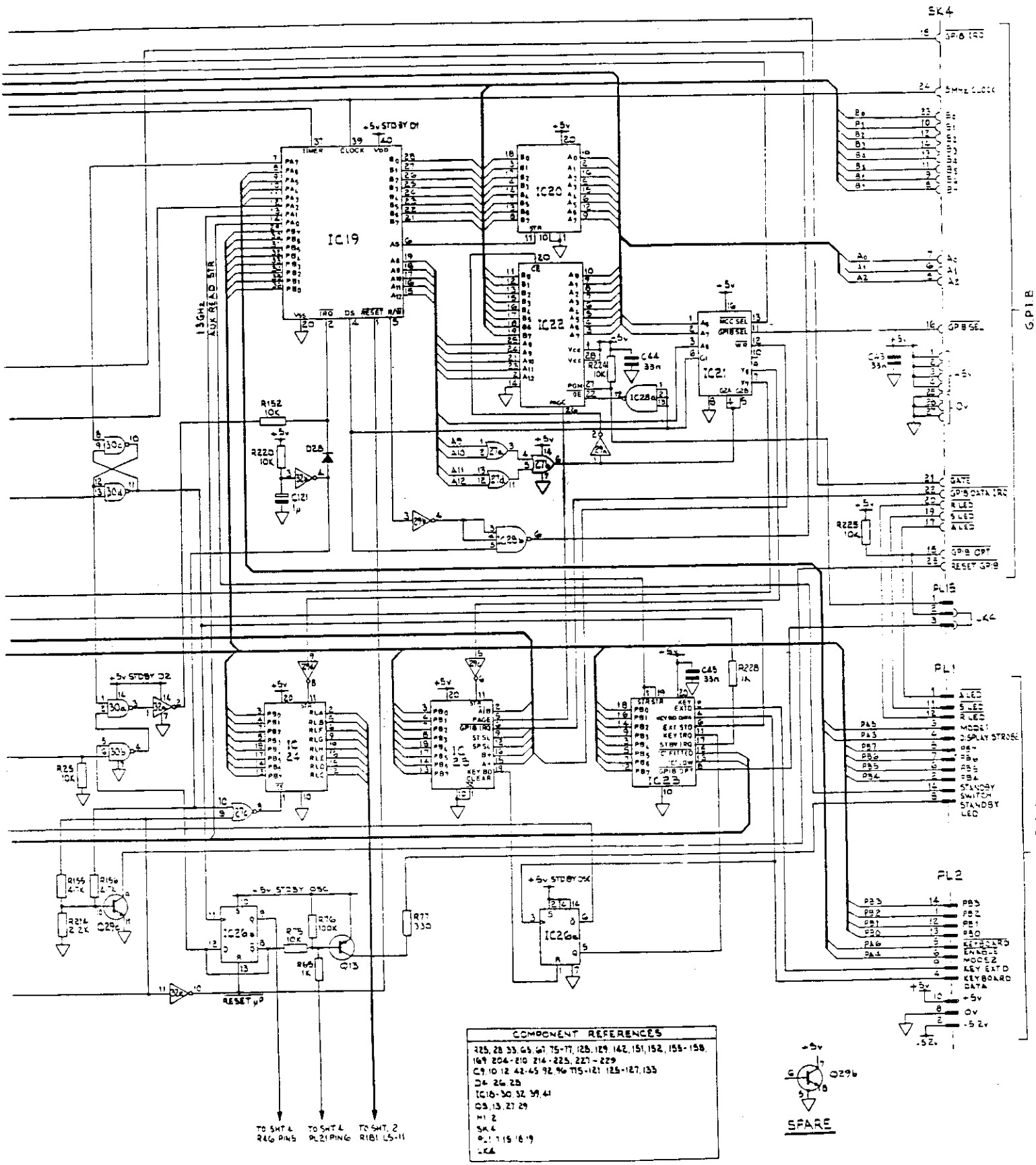
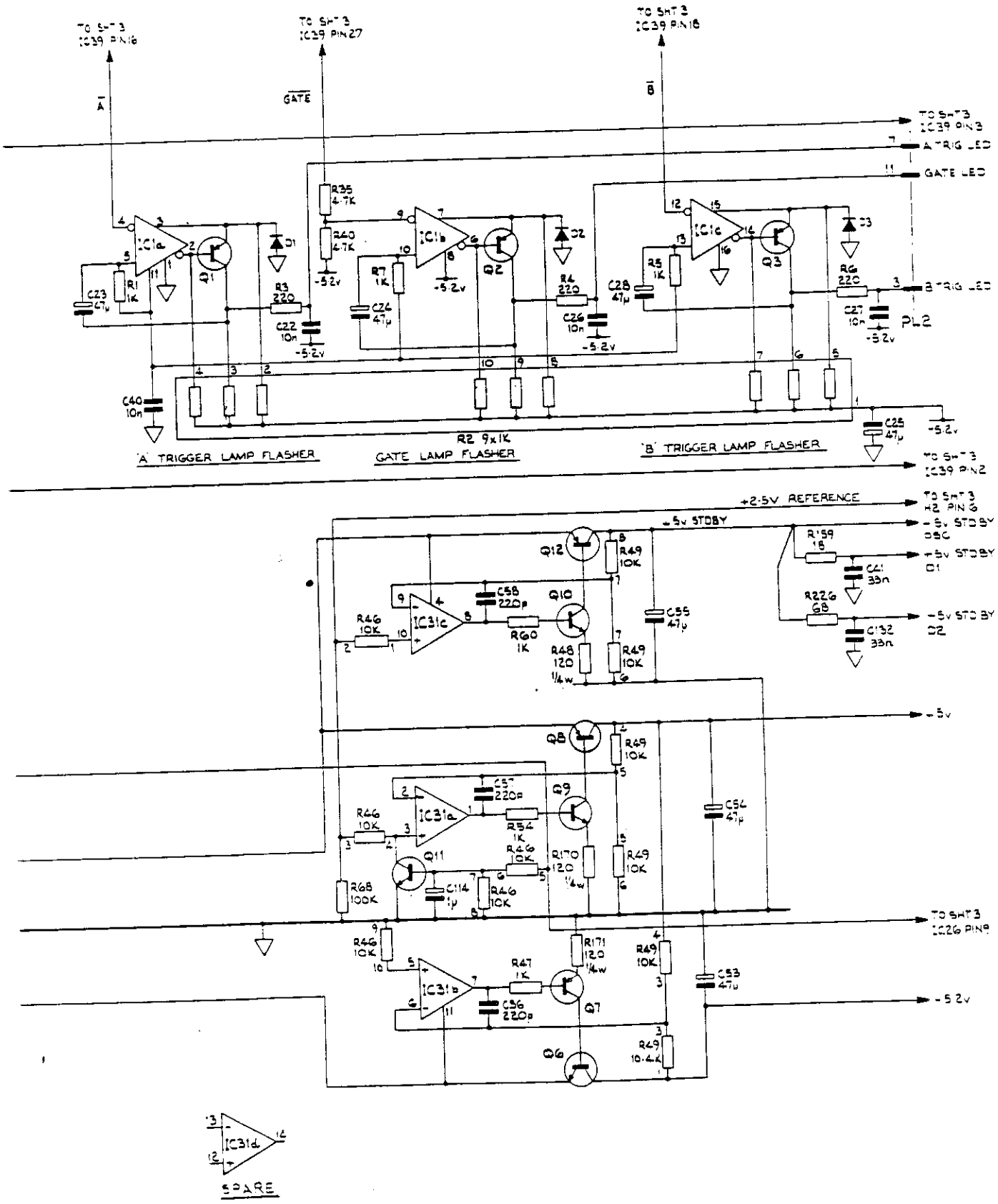
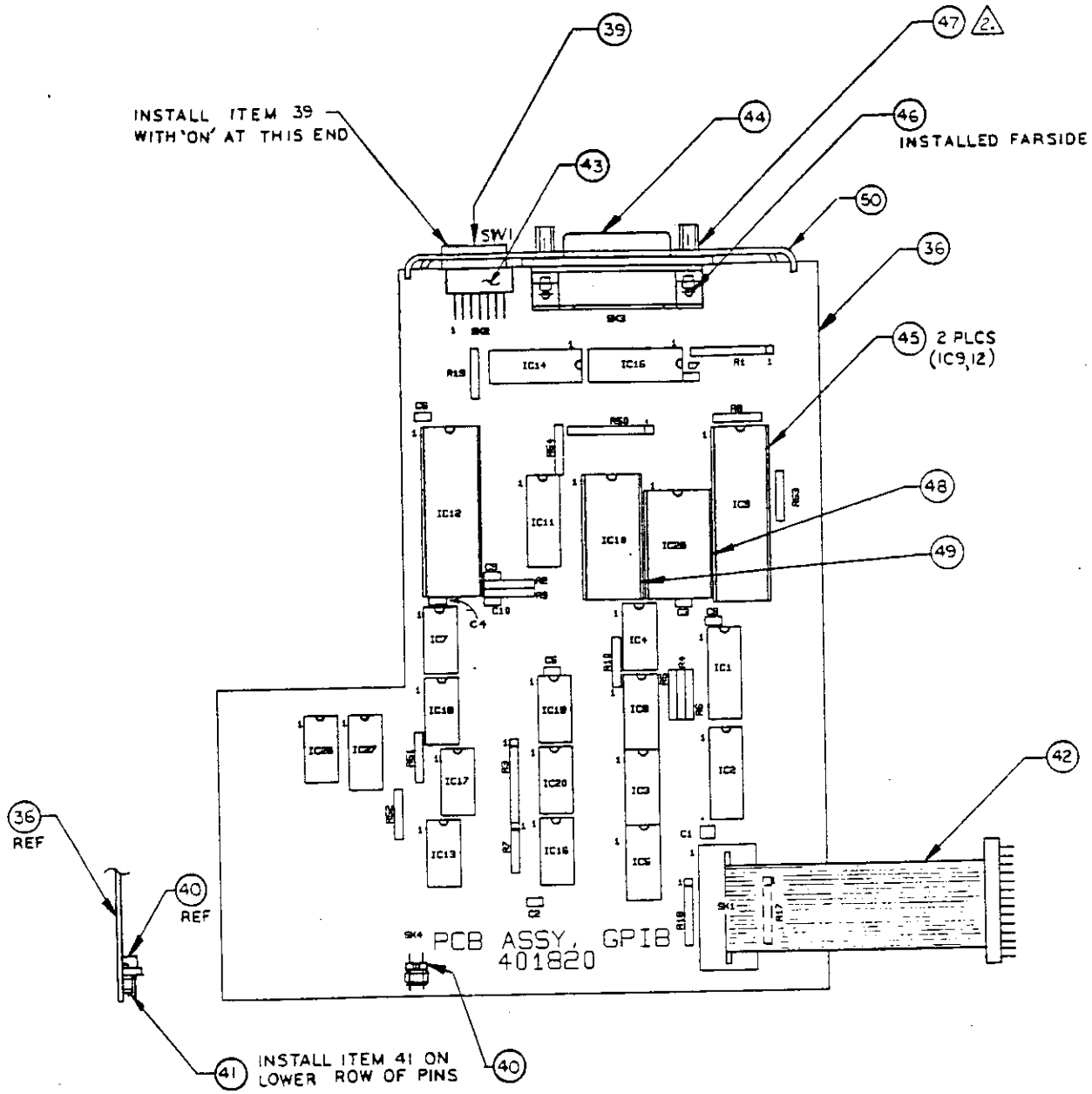


Figure 7.8 - Circuit Diagram, Motherboard (19-1145) (Cont'd)



REV. D

Figure 7.9 - Circuit Diagram, Motherboard (19-1145) (Cont'd)



2. DISCARD NUTS & LOCKWASHERS SUPPLIED WITH ITEM 47.

1. REF. SCHEM. 411820.

NOTES UNLESS OTHERWISE SPECIFIED

Figure 7.10 - Component Layout, GPIB (401820)

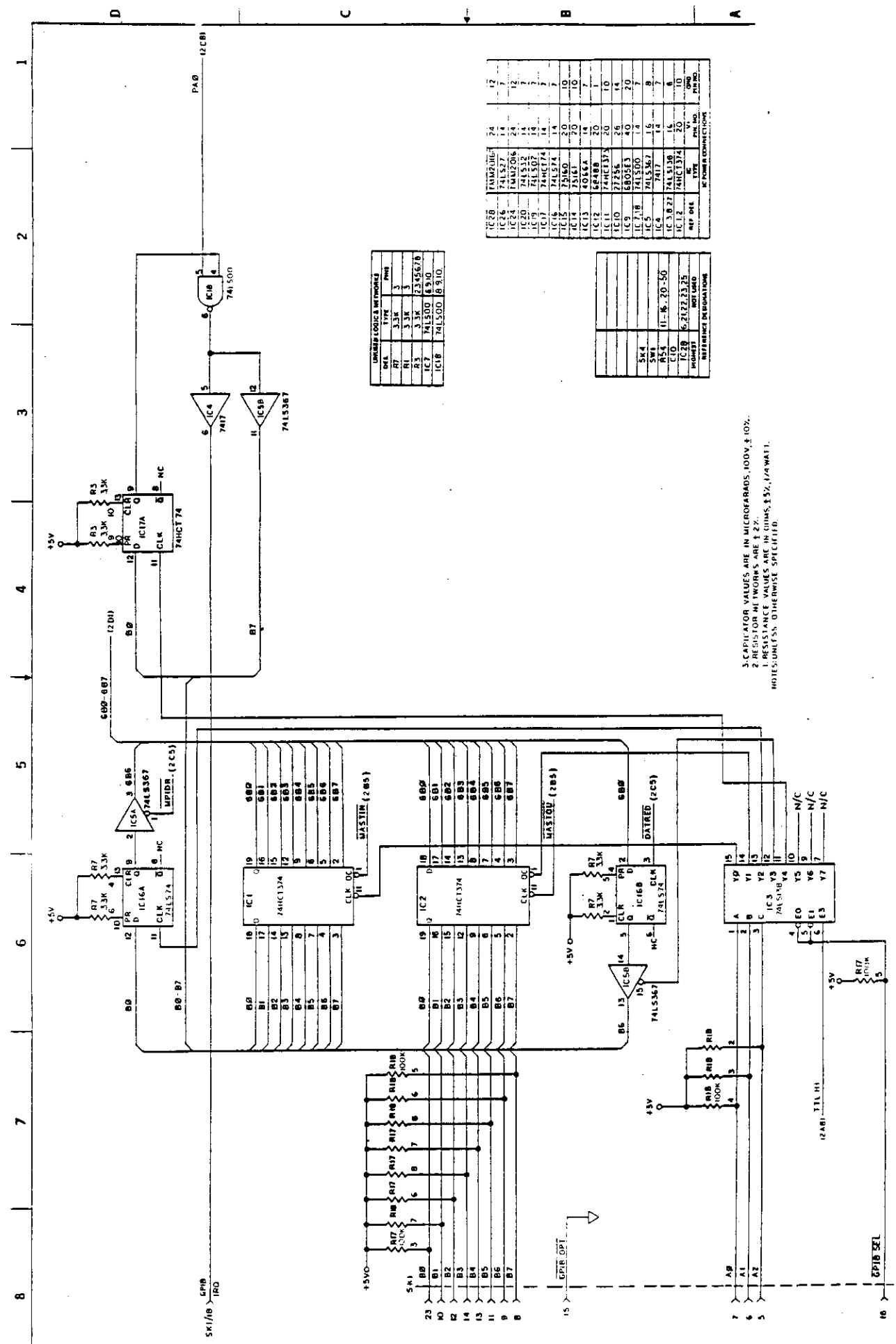


Figure 7.11 - Circuit Diagram, GPIB (431820)

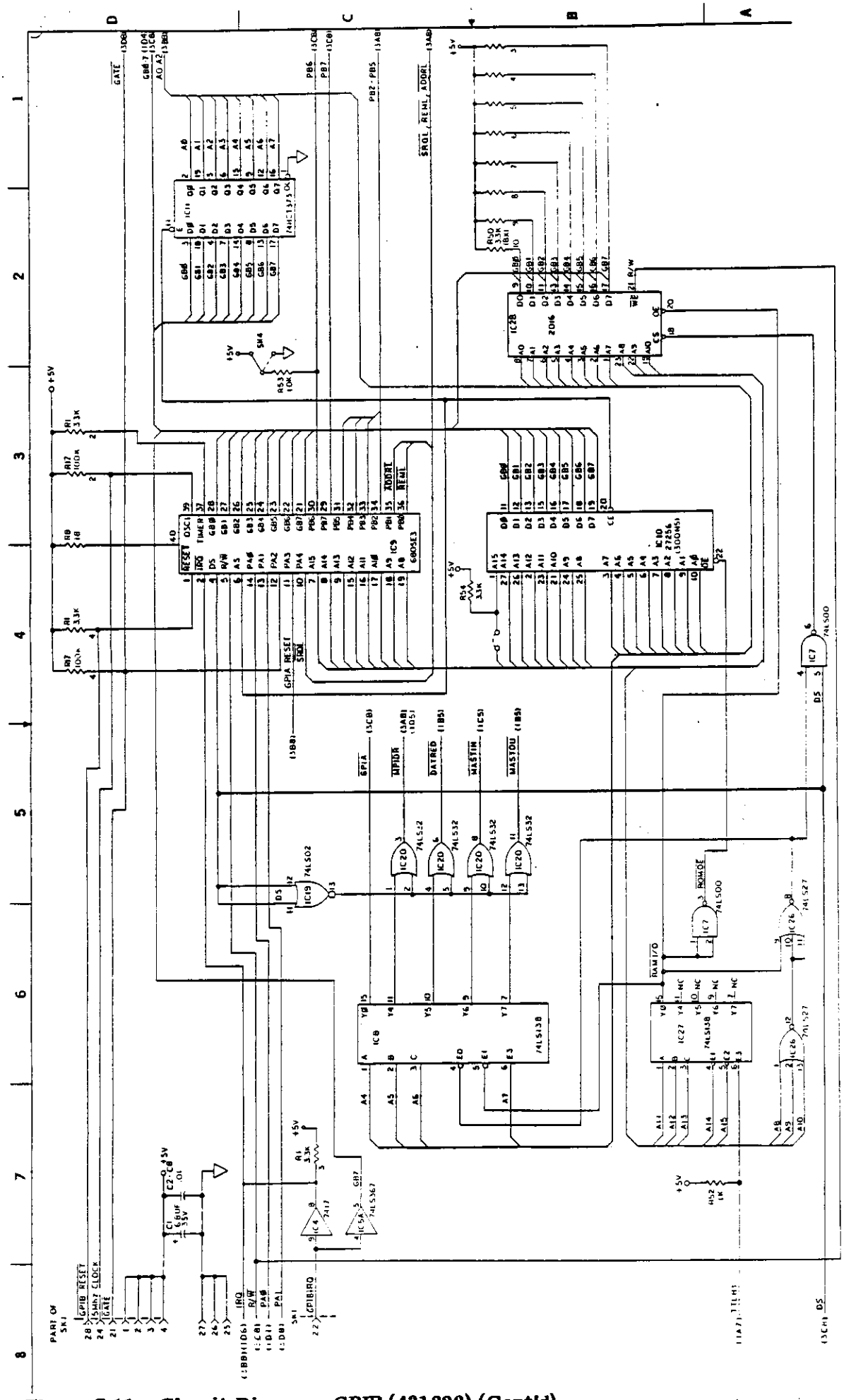


Figure 7.11 – Circuit Diagram, GPIB (431820) (Cont'd)

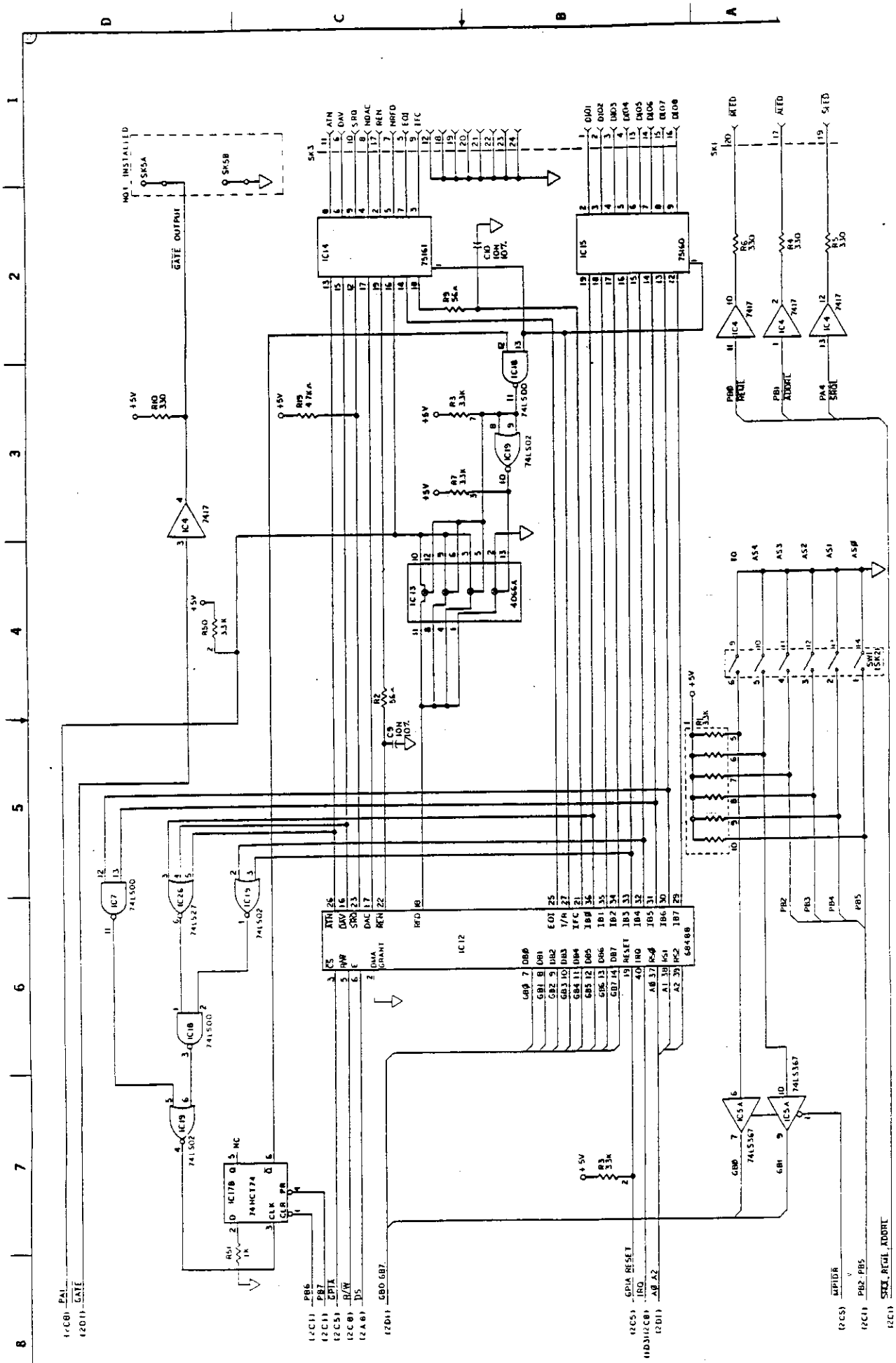


Figure 7.11 - Circuit Diagram, GPIB (431820) (Cont'd)

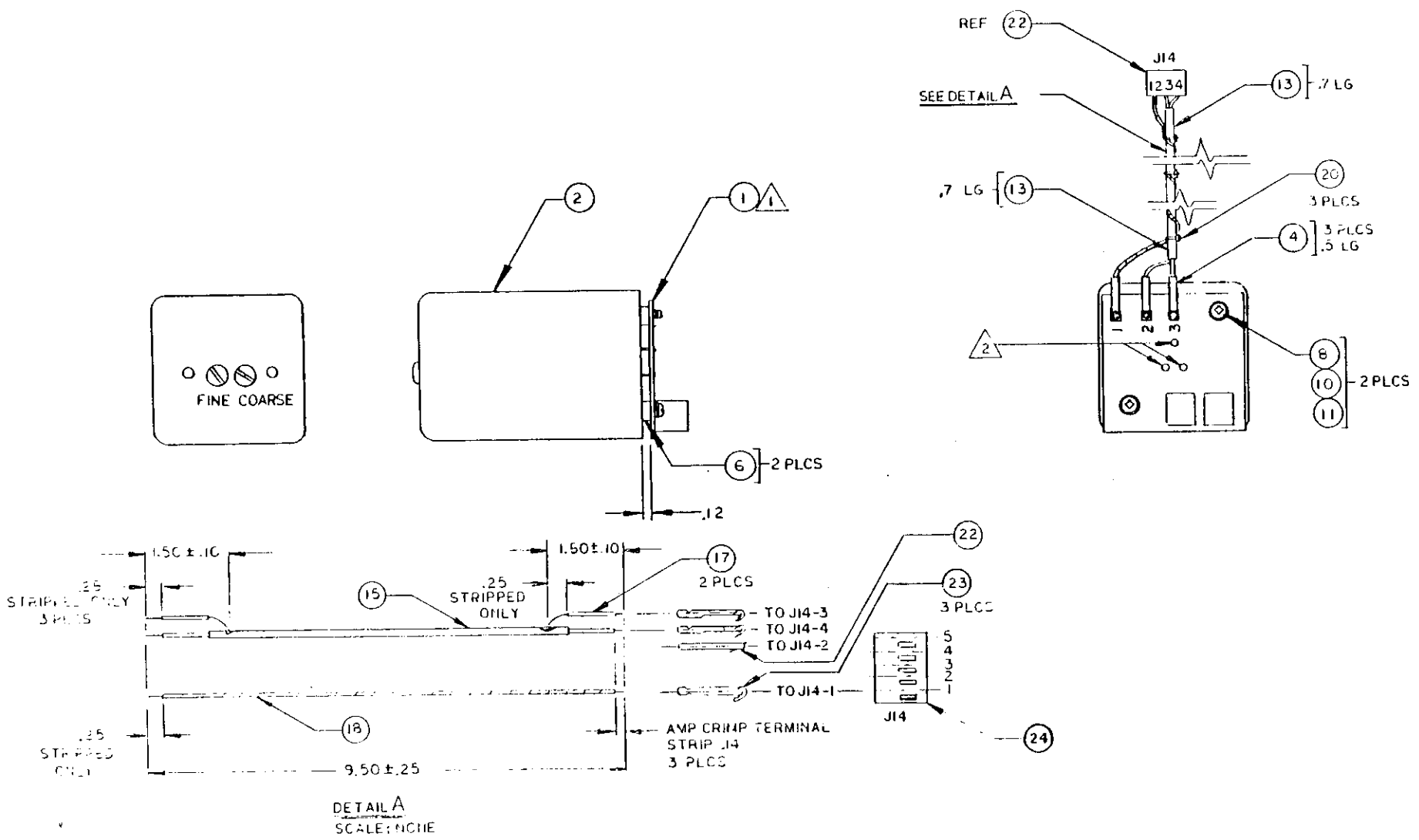


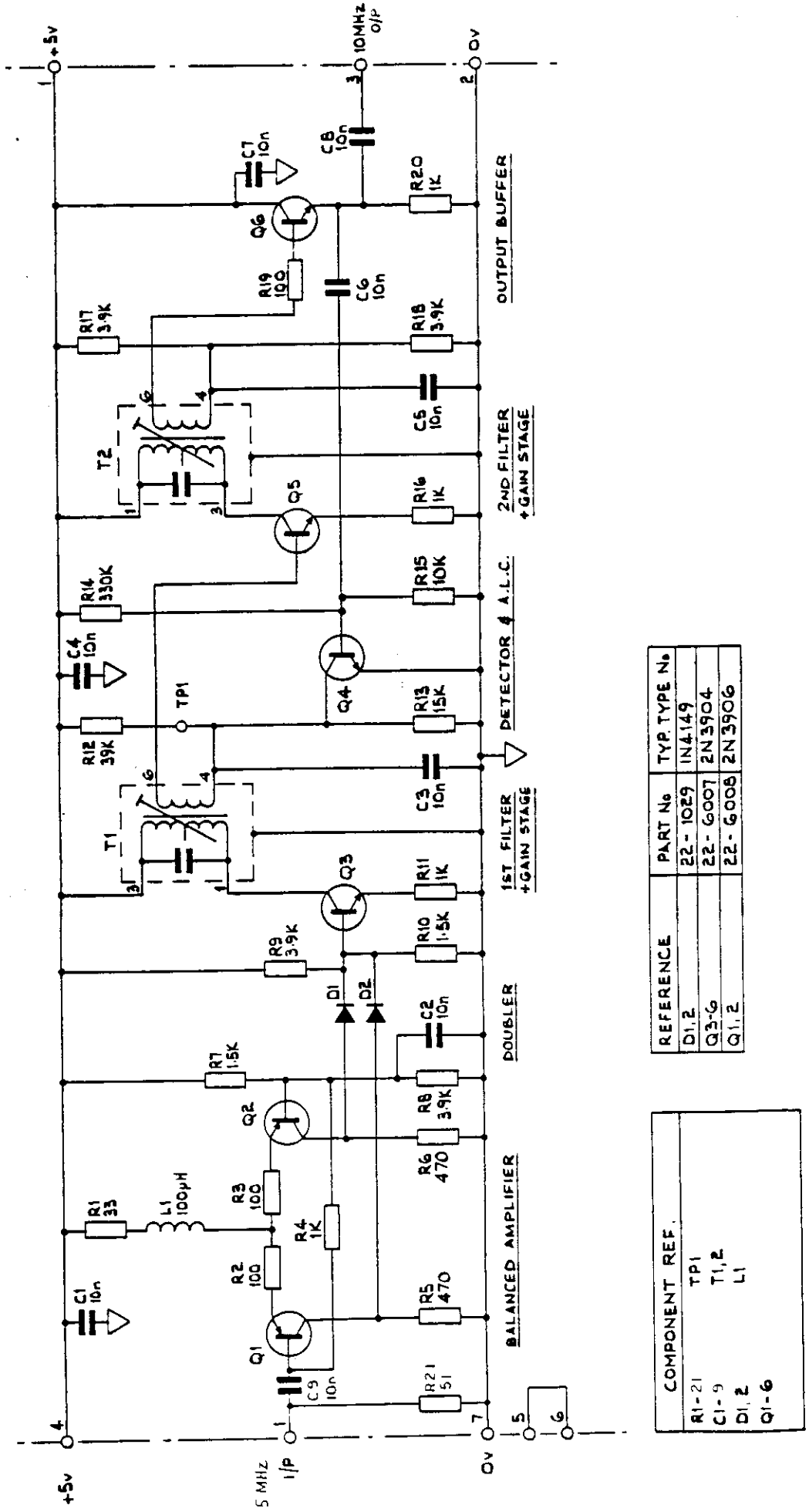
Figure 7.12 – Oscillator Assembly, Option 04E (404386)

2. SOLDER AT ASSY.

1. REMOVE AND DISCARD CABLE SUPPLIED WITH ITEM 1 AND REPLACE WITH ITEMS 13,15,17,18,20,22,23,24.

NOTES UNLESS OTHERWISE SPECIFIED

Figure 7.13 - Component Layout, Doubler (401822)



7-28 **Figure 7.14 - Circuit Diagram, Doubler (431822)**

REV. A

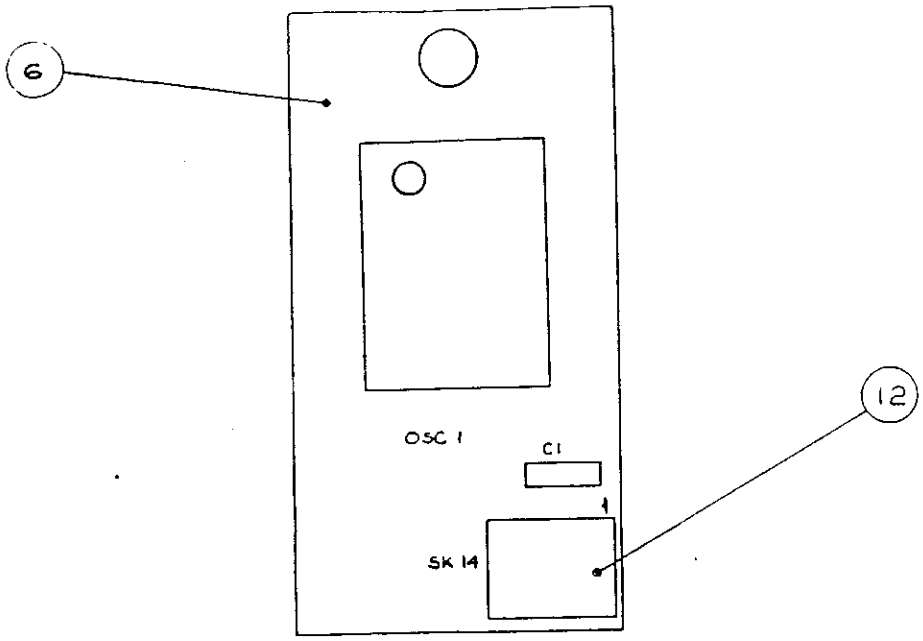


Figure 7.15 - Oscillator Assembly, Standard (19-1147)

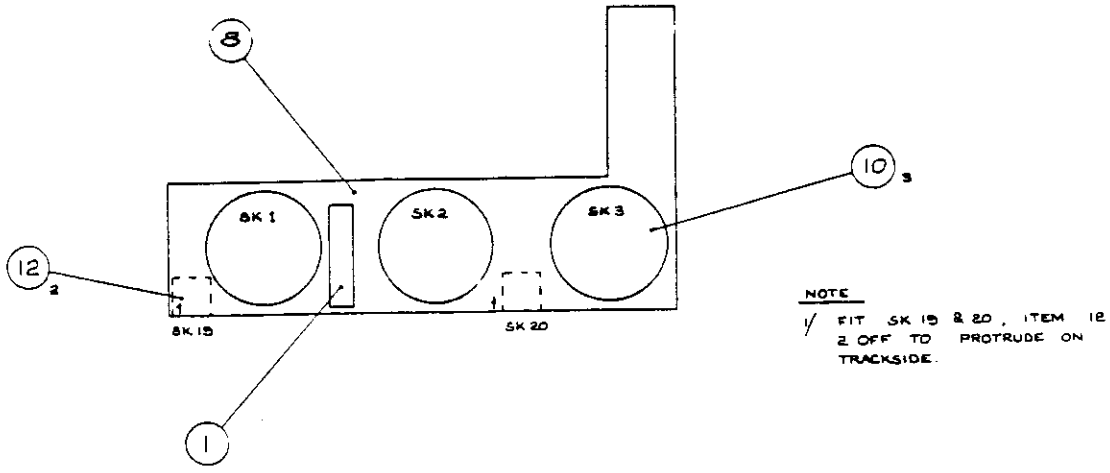


Figure 7.16 - Component Layout, BNC Mounting Board (19-1206)

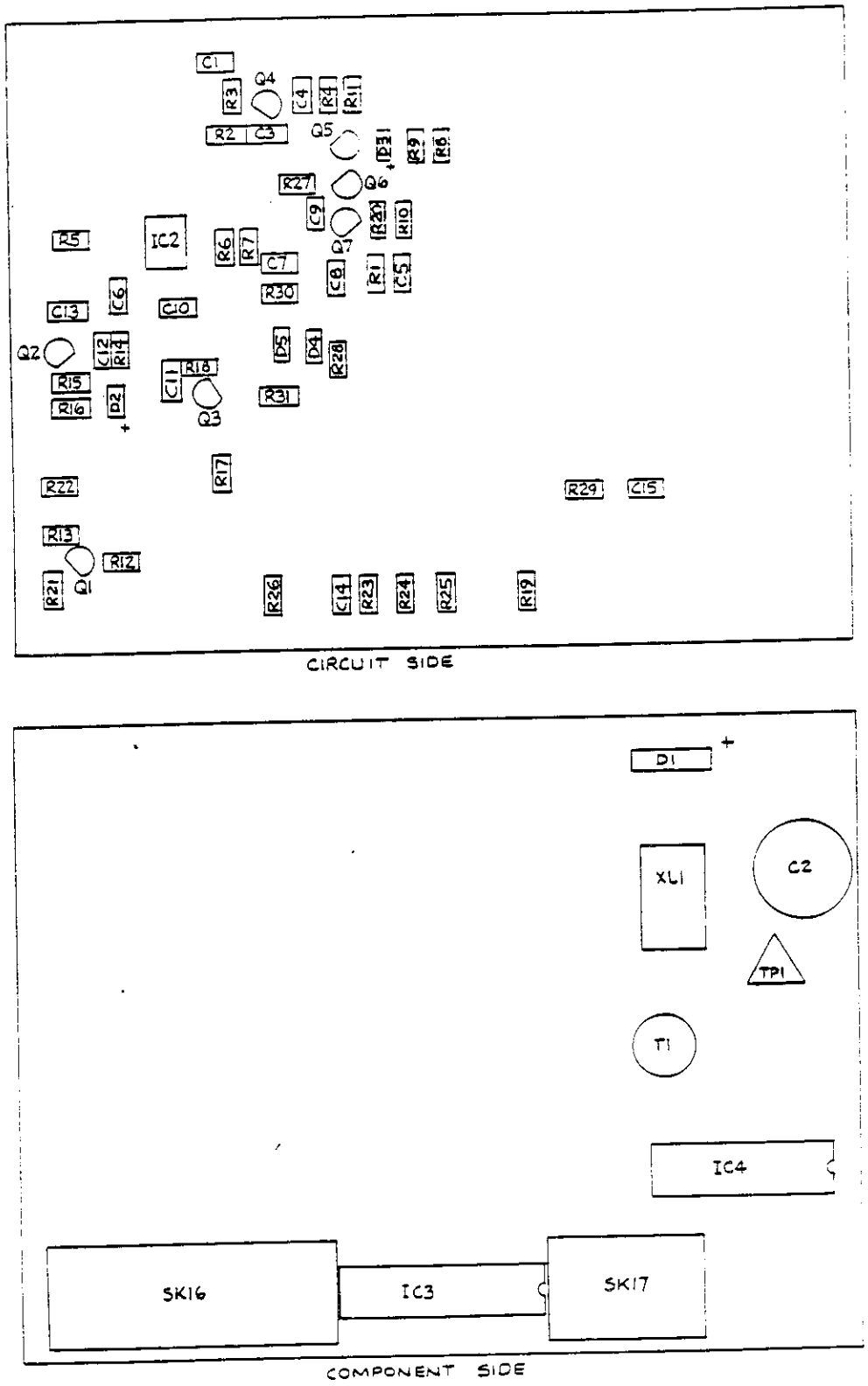


Figure 7.17 - Component Layout, Reference Frequency Multiplier (19-1164)

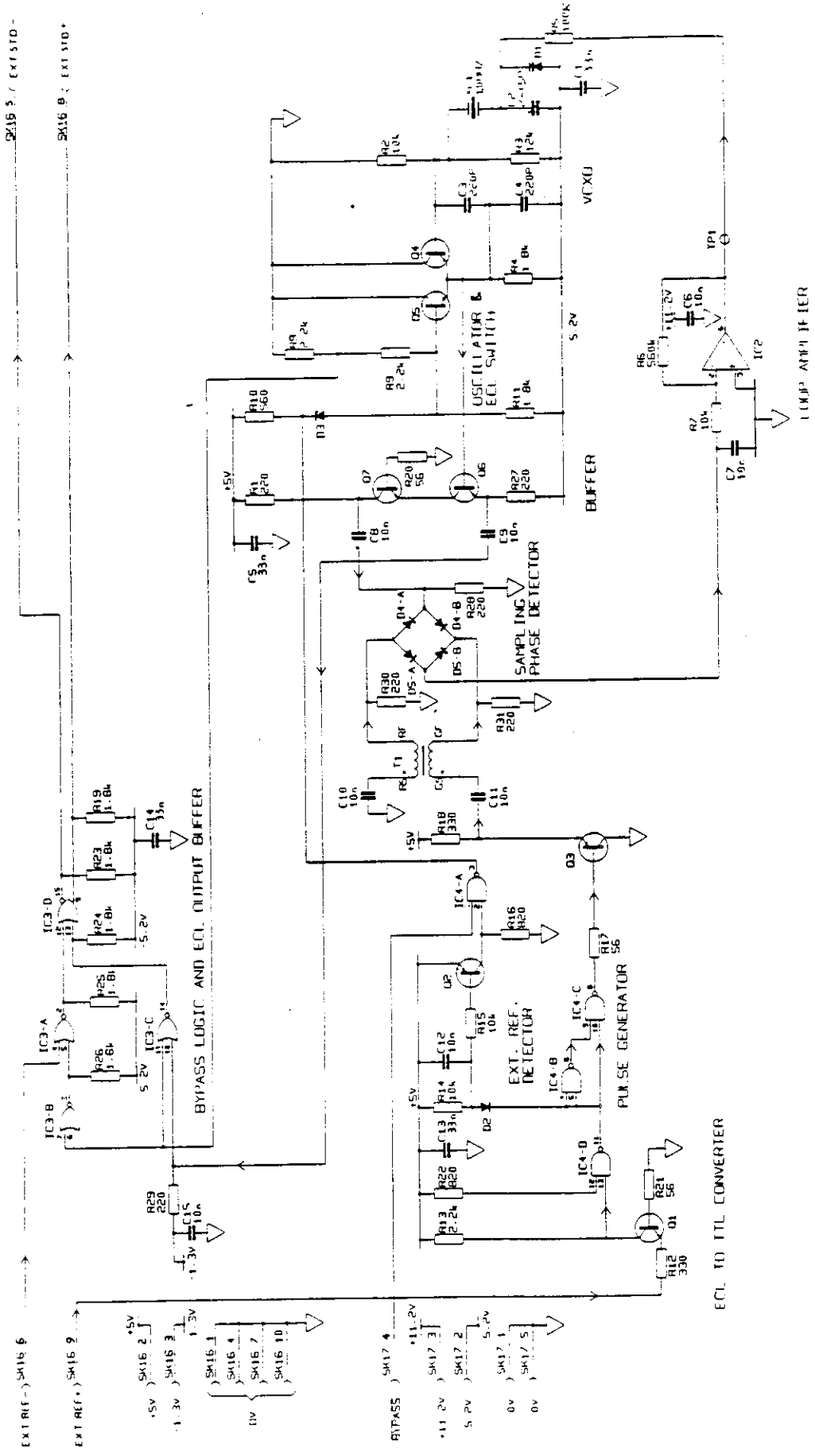


Figure 7.18 - Circuit Diagram, Reference Frequency Multiplier (19-1164)

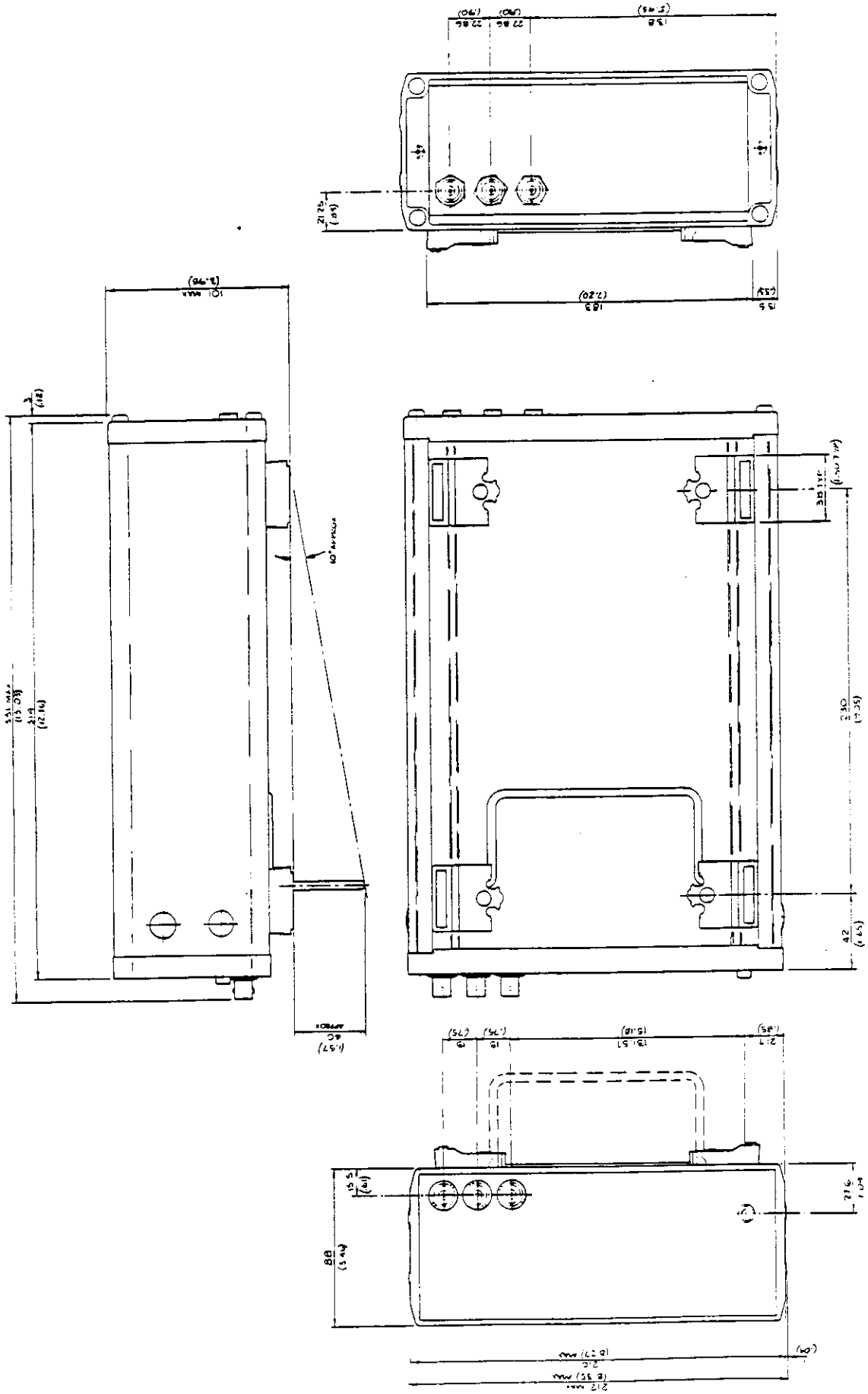


Figure 7.19 - Outline Drawing (455124)

SECTION 8 PARTS LIST

8.1 This section contains lists of replaceable parts arranged in the order of the following subassemblies:

8.2 Manufacturers are identified by FSC numbers listed in Table 8.1, "List of Suppliers." The code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbook H4-1, H4-2, and their supplements.

Table 8.1 - List of Suppliers

FSC	NAME
00779	AMP, INC. HARRISBURG, PA
01121	ALLEN BRADLEY CO. MILWAUKEE, WISCONSIN
01295	TEXAS INSTRUMENTS, INC. DALLAS, TEXAS
02114	FERROXCUBE CORP. SAUGERTIES, N.Y
02660	AMPHENOL CORP. BROADVIEW, ILLINOIS
04713	MOTOROLA, INC. (SEMI-CONDUCTOR PRODUCTS DIV.) PHOENIX, ARIZONA
05397	UNION CARBIDE CORP. (MATERIALS SYSTEMS DIV.) CLEVELAND, OHIO
05915	RICHCO PLASTIC CO. CHICAGO, ILLINOIS
07263	FAIRCHILD (SEMICONDUCTOR DIV.) MOUNTAIN VIEW, CA
11237	CTS KEENE, INC. PASO ROBLES, CA
13764	MICRO PLASTICS INC. FLIPPIN, AR
14433	ITT SEMICONDUCTORS WEST PALM BEACH, FLORIDA
14936	GENERAL INSTRUMENTS CORP. (SEMICONDUCTOR PRODUCTS GROUP) HICKSVILLE, L.I., N.Y.
15955	DENNISON MFG. CO. FRAMINGTON, MA
17856	SILICONIX, INC. SANTA CLARA, CA
18324	SIGNETICS CORP. SUNNYVALE, CA
18565	CHOMERICS, INC. WOBURN, MA
18714	RCA (COMMERCIAL REC. TUBE & SEMI. DIV.) FINDLAY, OH
19738	AVDEL-CHOBERT TELESBORO, NJ
1CJ86	BOSSARD BROOKFIELD, CT
21793	RACAL-DANA INSTRUMENTS INC. IRVINE, CA
22119	FERRANTI ELECTRIC PLAINVIEW, NY
22958	TELEDYNE ELECTRO MECHANISMS NASHUA, NH
24335	COOPER LABORATORIES, INC. WAYNE, NJ
24931	SPECIALTY CONNECTOR CO., INC. FRANKLIN, IN
24972	AEG-TELEFUNKEN CORP. SUMMERVILLE, NJ
25088	SIEMENS CORP. (COMP. GROUP) ISELIN, NJ
25403	AMPEREX ELECTRONIC CORP. (SEMICONDUCTOR & REC. TUBE DIV.) SLATERSVILLE, RHODE ISLAND
27014	NATIONAL SEMI-CONDUCTOR CORP. SANTA CLARA, CA
27264	MOLEX PRODUCTS CO. DOWNERS GROVE, ILLINOIS
27777	VARO ELECTRAN DEVICES, INC. GARLAND, TX
28848	MULLARD, INC. FARMINGDALE, L.I., N.Y.
29005	STORM PRODUCTS CO. LOS ANGELES, CA
2V900	BULGIN A.F. AND CO., LTD. BARKING ESSEX, ENGLAND
32293	INTERSIL, INC. CUPERTINO, CA

Table 8.1 - List of Suppliers (Cont'd)

FSC	NAME
32897	MURATA ERIE NORTH AMERICA INC. CARLISLE, PA
46384	PENN ENG. & MFG. CORP. DOYLESTOWN, PA
50434	HEWLETT-PACKARD CO. (HPA DIV.) PALO ALTO, CA
52072	CIRCUIT ASSY. CORP. COSTA MESA, CA
52210	KASON CORP. NEWARK, NJ
52648	PLESSEY MEMORIES SANTA ANA, CA
53387	THREE (3)M CO. (ELECTRONIC PRODUCTS DIV.) ST. PAUL, MN
56235	STATE OF THE ART INC. STATE COLLEGE, PA
61058	MATSUSHITA ELECTRIC CORP. OF AMERICA PANASONIC INDUSTRIAL CO. DIV. SECAUCUS, NJ
61802	TOSHIBA INTERNATIONAL HOUSTON, TX
61935	SCHURTER, INC. PETALUMA, CA
63878	AP PRODUCTS, INC. MENTOR, OH
65238	NOVACAP BURBANK, CA
65940	ROHM CORP. IRVINE, CA
70903	BELDEN CORP. CHICAGO, IL
71400	BUSSMAN MFG. (DIV. MCGRAW & EDISON CO.) ST. LOUIS, MO
71450	CTS CORP. ELKHART, IN
72982	ERIE TECHNOLOGICAL PRODUCTS, INC. ERIE, PA
75915	LITTELFUSE, INC. DES PLAINES, IL
78189	ILLINOIS TOOL WORKS, INC. (SHAKEPROOF DIV.) ELGIN, IL
78553	EATON CORP. (TINNERMAN PRODUCTS, INC.) CLEVELAND, OH
80031	MEPCO-ELECTRA MORRISTOWN, NJ
81349	MILITARY SPECIFICATION
82219	PHILIPS ECG INC. DIV. OF NORTH AMERICAN PHILIPS CORP. EMPORIUM, PA
83125	NYTRONICS, INC. DARLINGTON, SC
83330	HERMAN H. SMITH, INC. BROOKLYN, NY
88044	AERONAUTICAL STANDARDS GROUP DEPT. OF NAVY AND AIR FORCE
8C945	ELECTRONIZED CHEMICAL CO. BALTIMORE, MD
91506	AUGAT, INC. ATTLEBORO, MA
91637	DALE ELECTRONICS, INC. COLUMBUS, NE
91718	GENTECH AN INDIAN HEAD CO. LINDEN, NJ
95275	VITRAMON, INC. BRIDGEPORT, CN
96906	MILITARY SPECIFICATION
K0536	HARWIN ENGINEERS HANTS, ENGLAND
K1160	WELWNY MICROELECTRONICS NORTHUMBERLAND, ENGLAND
K1935	JERMYN MANUFACTURING KENT, ENGLAND
K2324	WEBB FASTENERS BERKSHIRE, ENGLAND
U3065	TOKO BERKSHIRE, ENGLAND
U3441	QUADRANT METER CO., LTD. HERTS, ENGLAND

404577 - FINAL ASSY., 1991

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
{4}1	404576	CHASSIS ASSY	21793	404576
{5}1	404582	SHIPPING KIT	21793	404582
{6}1	R-11-1623	COVER KIT ASSY	21793	R-11-1623
{11}1	R-13-1972	COVER,FORMED	21793	R-13-1972
{12}1	R-13-1991	FRONT PANEL OVERLAY	21793	R-13-1991
{21}1	R-15-0672	REAR BEZEL	21793	R-15-0672
{25}4	R-24-0250	PUSH-IN FASTENER,BLACK,NYLON	21793	R-24-0250
{27}2	R-24-2801	WASHER, CRINKLE, M3	21793	R-24-2801
{29}4	R-24-7042	BLIND GROMMET,GREY	21793	R-24-7042
{40}2	616315	SCREW, PPH, M3X6	1CJ86	7985-A-M3X6MM

404576 - CHASSIS ASSY., 1991

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
{4}1	R-11-1592	FRONT PANEL SUB ASSY	21793	R-11-1592
{6}1	R-11-1593	REAR PANEL SUB. ASSY	21793	R-11-1593
{8}1	455112	SHIELD, POWER	21793	455112
{10}1	R-11-1610	OSCILLATOR PLATE ASSY	21793	R-11-1610
{14}2	R-11-1643	SIDE PANEL ASSY	21793	R-11-1643
{20}1	R-13-2024	LID	21793	R-13-2024
{22}1	R-13-2026	BLANKING PLATE	21793	R-13-2026
{25}1	R-13-2102	KEEPER PLATE	21793	R-13-2102
{32}1	R-15-0674	PUSH BUTTON MAINS	21793	R-15-0674
{34}1	R-15-0693	SWITCH CONTROL ROD	21793	R-15-0693
{36}1	455110	MAINS COVER	21793	455110
{50}1	R-18-1239	SCREEN	21793	R-18-1239
{52}1	R-19-1141	DISPLAY BOARD ASSY	21793	R-19-1141
{54}1	R-19-1145	MOTHERBOARD ASSY	21793	R-19-1145
{56}1	R-19-1147	OSCILLATOR SSY.,10 MHZ	21793	R-19-1147
{58}1	R-19-1206	B.N.C. BOARD ASSY	21793	R-19-1206
{70}1	R-24-0187	BUTTON, RUBBER	53387	SJ5023
{74}3	921065	CARD GUIDE, 3" LG	21793	921065
{76}3	R-24-0244	RIVET, PLASTIC, BLACK	06915	SR3045
{82}1	617042	NUT, HEX, M3	1CJ86	DIN934-M3
{84}1	617044	NUT, HEX, M4	1CJ86	DIN934-M4
{86}1	611153	NUT, TINNERMAN, TWIN TYPE, 4Z	78553	C6069-4Z-4
{92}15	R-24-2801	WASHER, CRINKLE, M3	21793	R-24-2801
{103}1	R-24-6127	LABEL, ALUMINUM	21793	R-24-6127
{108}8	616315	SCREW, PPH, M3X6	1CJ86	7985-A-M3X6MM
{110}6	616316	SCREW, PPH, M3X8	1CJ86	7985-A-M2.5X14MM
{112}2	611154	SCREW, PPH, 4B SELF TAP	-	-
{118}4	R-24-7822	SCREW, TAPTITE, M3 X 8	21793	R-24-7822
{126}20MM	500023	WIRE, BARE COPPER/TIN, 24 GA	21793	500023
{136}35MM	R-25-5202	HEATSHRINK SLEEVING, .188 ID, BLK	21793	R-25-5202

404571 - FINAL ASSY., 1992

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
{4}1	404572	CHASSIS ASSY	21793	404572
{5}1	404582	SHIPPING KIT	21793	404582
{6}1	R-11-1623	COVER KIT ASSY	21793	R-11-1623
{11}1	R-13-1972	COVER,FORMED	21793	R-13-1972
{12}1	R-13-1976	FRONT PANEL OVERLAY	21793	R-13-1976
{21}1	R-15-0672	REAR BEZEL	21793	R-15-0672
{25}4	R-24-0250	PUSH-IN FASTENER,BLACK,NYLON	21793	R-24-0250
{27}2	R-24-2801	WASHER, CRINKLE, M3	21793	R-24-2801
{29}4	R-24-7042	BLIND GROMMET,GREY	21793	R-24-7042

404572 - CHASSIS ASSY., 1992

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
{4}1	R-11-1592	FRONT PANEL SUB ASSY	21793	R-11-1592
{5}1	404582	SHIPPING KIT	21793	404582
{6}1	R-11-1593	REAR PANEL SUB. ASSY	21793	R-11-1593
{8}1	455112	SHIELD, POWER	21793	455112
{10}1	R-11-1610	OSCILLATOR PLATE ASSY	21793	R-11-1610
{14}2	R-11-1643	SIDE PANEL ASSY	21793	R-11-1643
{20}1	R-13-2024	LID	21793	R-13-2024
{22}1	R-13-2026	BLANKING PLATE	21793	R-13-2026
{25}1	R-13-2102	KEEPER PLATE	21793	R-13-2102
{27}1	611072	SPACER, BNC	21793	R-14-1577
{32}1	R-15-0674	PUSH BUTTON MAINS	21793	R-15-0674
{34}1	R-15-0693	SWITCH CONTROL ROD	21793	R-15-0693
{36}1	455110	MAINS COVER	21793	455110
{42}1	R-17-1038	BNC-SMA FUSED SKT	U3441	TG-5001
{50}1	R-18-1239	SCREEN	21793	R-18-1239
{52}1	R-19-1141	DISPLAY BOARD ASSY	21793	R-19-1141
{54}1	R-19-1145	MOTHERBOARD ASSY	21793	R-19-1145
{56}1	R-19-1147	OSCILLATOR SSY.,10 MHZ	21793	R-19-1147
{58}1	R-19-1206	B.N.C. BOARD ASSY	21793	R-19-1206
{62}1	R-19-1142	1.3 GHZ PRESCALER BD	21793	R-19-1142
{70}1	R-24-0187	BUTTON, RUBBER	53387	SJ5023
{74}3	921065	CARD GUIDE, 3" LG	21793	921065
{76}1	R-24-0244	RIVET, PLASTIC, BLACK	06915	SR3045
{82}1	617042	NUT, HEX, M3	1CJ86	DIN934-M3
{84}1	617044	NUT, HEX, M4	1CJ86	DIN934-M4
{86}1	611153	NUT, TINNERMAN, TWIN TYPE, 4Z	78553	C6069-4Z-4
{92}17	R-24-2801	WASHER, CRINKLE, M3	21793	R-24-2801
{103}1	R-24-6127	LABEL, ALUMINUM	21793	R-24-6127
{108}10	615315	SCREW, PPH, M3X6	1CJ86	7985-A-M3X6MM
{110}6	616315	SCREW, PPH, M3X6	1CJ86	7985-A-M3X6MM
{112}2	611154	SCREW, PPH, 4B SELF TAP	-	-
{118}4	R-24-7822	SCREW, TAPTITE, M3 X 8	21793	R-24-7822
{126}20MM	500023	WIRE, BARE COPPER/TIN, 24 GA	21793	500023
{136}35MM	R-25-5202	HEATSHRINK SLEEVING, .188 ID, BLK	21793	R-25-5202

R-19-1141, PCB ASSY., DISPLAY

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
C1	100062	CAP, CER, .01 UF 100V, 10 PERCENT	05397	C320C103K1R5CA
C2	R-21-0785	CAP, ALUM. ELEC., 4.7 UF	61058	ECEA1HK4R7E
C3-5	100062	CAP, CER, .01 UF 100V, 10 PERCENT	05397	C320C103K1R5CA
D6-7	R-22-1029	DIODE, SILICON	14433	1N4149
D8-10	R-22-1029	DIODE, SILICON	14433	1N4149
DI1-4	R-26-1512	DISPLAY, DOUBLE DIGIT	14936	MAN6910
DI5	R-26-1513	DISPLAY, SINGLE DIGIT	14936	MAN6960
DI6	R-26-1511	DISPLAY, SINGLE DIGIT	25088	HD1105
IC1	R-22-4754	IC, DUAL 4-INPUT NAND GATES	18324	HEF40128P
IC2	R-22-4779	IC, CMOS 16-KEY ENCODER	27014	MM74C922N/A
IC3-4	230457	IC, LED DRIVER	32293	ICM7218AIJI
LP1-8	R-26-5026	LED, RED	14936	MV6754-21
LP11-13	R-26-5026	LED, RED	14936	MV6754-21
LP15-18	R-26-5026	LED, RED	14936	MV6754-21
LP20-32	R-26-5026	LED, RED	14936	MV6754-21
LP33	R-26-5027	LED, ORANGE	24972	TLSO-3501
LP34-42	R-26-5026	LED, RED	14936	MV6754-21
LP44-47	R-26-5026	LED, RED	14936	MV6754-21
R1-2	000103	RES, CARB COMP, 10K, 5 PERCENT 1/4W	21793	RC07GF103J
R3	090015	RES NETWORK, 9R, 10K, 5 PERCENT	71450	750-101-R10K
R4-5	000103	RES, CARB COMP, 10K, 5 PERCENT 1/4W	21793	RC07GF103J
S1-33	501211	SWITCH, PUSHBUTTON	U3065	R-7005
SK1-2	R-23-5160	SOCKET, 14-WAY	63878	929975-07
(2)21	R-15-0703	PUSH BUTTON, GREY	21793	R-15-0703
(4)4	R-15-0705	PUSH BUTTON, BLUE	21793	R-15-0705
(5)1	R-16-0651	BUTTON, PRINTED (NO. 1)	21793	R-16-0651
(7)1	R-16-0652	BUTTON, PRINTED (NO. 2)	21793	R-16-0652
(8)1	R-16-0653	BUTTON, PRINTED (NO. 3)	21793	R-16-0653
(9)1	R-16-0654	BUTTON, PRINTED (NO. 4)	21793	R-16-0654
(10)1	R-16-0655	BUTTON, PRINTED (NO. 5)	21793	R-16-0655
(11)2	R-16-0656	BUTTON, PRINTED (NO. 6 & 9)	21793	R-16-0656
(12)1	R-16-0657	BUTTON, PRINTED (NO. 7)	21793	R-16-0657
(13)1	R-16-0658	BUTTON, PRINTED (NO. 8)	21793	R-16-0658
(14)1	R-16-0659	BUTTON, PRINTED (NO. 0)	21793	R-16-0659
(15)1	R-16-0660	BUTTON, PRINTED (DECIMAL POINT)	21793	R-16-0660
(17)1	R-19-1141	P.C. BOARD (UNLOADED)	21793	R-19-1141
(53)1	920396	SOCKET, 28-PIN	52072	CA-28S-TSO-BC
(54)14	500002	TUBING, SHRINK, .187 ID	80945	M23053/5-105-0

R-19-1142, PCB ASSY., CHANNEL C

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
C1-6	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C7	R-21-1781	CAP, CHIP, 3.3 PF	95275	VJ1206A3R3CF
C8-10	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C11	R-21-1781	CAP, CHIP, 3.3 PF	95275	VJ1206A3R3CF
C12-13	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C14	R-21-1781	CAP, CHIP, 3.3 PF	95275	VJ1206A3R3CF
C15	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C16	R-21-0795	CAP, ALUM. ELEC., 47 UF	28848	2222-036-35479
C17-18	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C19	R-21-1783	CAP, CHIP, 4.7 PF	95275	VJ1206N4R7CF
C21	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C22	R-21-1781	CAP, CHIP, 3.3 PF	95275	VJ1206A3R3CF
C23	R-21-1788	CAP, CHIP, 12 PF	95275	VJ1206A120JF
C24-25	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C26	R-21-1800	CAP, CHIP, 1 NF	95275	VJ1206Y102KF
C27	R-21-0795	CAP, ALUM. ELEC., 47 UF	28848	2222-036-35479
C28-32	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C33	R-21-1784	CAP, CHIP, 5.6 PF	95275	VJ1206A5R6CF
C34-36	R-21-1785	CAP, CHIP, 6.8 PF	95275	VJ1206A6R8CF
C37	R-21-1795	CAP, CHIP, 47 PG	95275	VJ1026A470JF
C38-39	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C40-41	R-21-1781	CAP, CHIP, 3.3 PF	95275	VJ1206A3R3CF
C42	R-21-1784	CAP, CHIP, 5.6 PF	95275	VJ1206A5R6CF
C43	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C44	R-21-0795	CAP, ALUM. ELEC., 47 UF	28848	2222-036-35479
C45	R-21-0704	CAP, ALUM. ELEC., 47 UF	28848	122-53479
C46	R-21-1782	CAP, CHIP, 3.9 PF	95275	VJ1206A3R9CF
C47-48	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C49-50	R-21-1781	CAP, CHIP, 3.3 PF	95275	VJ1206A3R3CF
C51-52	R-21-1799	CAP, CHIP, 15 PF	95275	VJ1026A150JF
C53	100133	CAP, CER, .1 UF, LOW PROFILE, 20 PERCENT	32897	8131LP-100-25U-104M
D1	210089	DIODE, LOW OFFSET SCHOTTKY	50434	HP5082-2835
D2	R-22-1058	DIODE, SILICON	50434	5082-3379
D3	210089	DIODE, LOW OFFSET SCHOTTKY	50434	HP5082-2835
D5-6	210089	DIODE, LOW OFFSET SCHOTTKY	50434	HP5082-2835
D7	R-22-1058	DIODE, SILICON	50434	5082-3379
D8-9	210017	DIODE, MATCHED PAIR	21793	210017
D10-11	R-22-1814	DIODE, ZENER	25403	BZX79C5V1
D12	R-22-1029	DIODE, SILICON	14433	1N4148
IC1	230547	IC, QUAD COMPARATOR	27014	LM339N/A-1
IC2	230787	IC, DIGITAL, TRIPLE LINE RECEIVER	04713	MC10116P05
IC3	R-22-4594	IC, 1.3 GHZ PRESCALER	52648	SP4731
IC4	230193	IC, NAND GATE	01295	SN74LS00N3
L1	R-17-3240	COIL ASSY.	21793	R-17-3240
Q1-3	R-22-5123	TRANSISTOR, NPN	82219	BFR90
Q4	R-22-6155	TRANSISTOR, RF	50434	HXTR-3101
R3-4	R-20-5763	RES, CHIP, 10K, 1/8W, 5 PERCENT	65940	MCR18-10K OHM-5 PCT
R5	R-20-5641	RES, CHIP, 150 OHM, 1W	56235	2021CPX151J
R6	R-20-5837	RES, CHIP, 39 OHM, 1W	56235	2021CPX390J
R7	R-20-5737	RES, CHIP, 330 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-330 OHM-5 PCT
R8	R-20-5783	RES, CHIP, 150 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-150 OHM-5 PCT
R9	R-20-5786	RES, CHIP, 270 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-270 OHM-5 PCT
R10	R-20-5754	RES, CHIP, 100 OHM, 1/8W, 5 PERCENT	65940	MCR18-100 OHM-5 PCT

R-19-1142, PCB ASSY., CHANNEL C (CONT'D)

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
R11	R-20-5786	RES, CHIP, 270 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-270 OHM-5 PCT
R12	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-10 OHM-5 PCT
R13	R-20-5776	RES, CHIP, 33 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-33 OHM-5 PCT
R14	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-330 OHM-5 PCT
R15	R-20-5786	RES, CHIP, 270 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-270 OHM-5 PCT
R16	R-20-5788	RES, CHIP, 390 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-390 OHM-5 PCT
R18	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-10 OHM-5 PCT
R19	R-20-5776	RES, CHIP, 33 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-33 OHM-5 PCT
R20	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-330 OHM-5 PCT
R21-22	R-20-5784	RES, CHIP, 180 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-180 OHM-5 PCT
R23	R-20-5788	RES, CHIP, 390 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-390 OHM-5 PCT
R24	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-10 OHM-5 PCT

R-19-1145, PCB ASSY., MOTHERBOARD

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
C1	R-21-0789	CAP, ALUM. ELEC., 47 UF, 25V	61058	ECEA1EV470S
			95275	VJ1206Y103MF
C2	R-21-1801	CAP, CHIP, 10 NF	61058	ECEA1EV470S
C3	R-21-0789	CAP, ALUM. ELEC., 47 UF, 25V	95275	VJ1206Y103MF
C4-12	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y102KF
C13-14	R-21-1800	CAP, CHIP, 1 NF	95275	VJ1206Y103MF
C22	R-21-1801	CAP, CHIP, 10 NF	61058	ECEA1EV470S
C23-25	R-21-0789	CAP, ALUM. ELEC., 47 UF, 25V	95275	VJ1206Y103MF
C25-27	R-21-1801	CAP, CHIP, 10 NF	61058	ECEA1EV470S
C28	R-21-0789	CAP, ALUM. ELEC., 47 UF, 25V	95275	VJ1206Y102KF
C35	R-21-1800	CAP, CHIP, 1 NF	65238	1206B203K401N
C36	R-21-1847	CAP, CHIP, 20 NF, 400V	95275	VJ1206Y333KF
C37	R-21-1808	CAP, CHIP, 33 NF	95275	VJ1206Y103MF
C40	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y333KF
C41-45	R-21-1808	CAP, CHIP, 33 NF	25088	081121-C-123
C46	R-21-7003	CAP, POLYPROP., 47 NF, 250V	25088	881121-C-8141
C47-48	R-21-7002	CAP, POLYPROP., 2.5 NF	28848	2222-050-55103
C49	R-21-0583	CAP, ALUM. ELEC., 10000 UF, 16V	28848	2222-050-55472
C50	R-21-0667	CAP, ALUM. ELEC., 4700 UF, 16V	28848	2222-035-55681
C52	R-21-0797	CAP, ALUM. ELEC., 680 UF, 25V	61058	ECEA1EV470S
C53-55	R-21-0789	CAP, ALUM. ELEC., 47 UF, 25V	95275	VJ1206A221JF
C56-58	R-21-1838	CAP, CHIP, 220 PF	28848	2222-035-55681
C59	R-21-0797	CAP, ALUM. ELEC., 680 UF, 25V	65238	1206B203K401N
C65-66	R-21-1847	CAP, CHIP, 20 NF, 400V	95275	VJ1206A6RBCX7400
C67	R-21-1859	CAP, CHIP, 6.8 PF, 400V	95275	NJ1206A470GXA
C68	R-21-1862	CAP, CHIP, 47 PF, 2 PCT	95275	VJ1206A6RBCX7400
C69	R-21-1859	CAP, CHIP, 6.8 PF, 400V	95275	NJ1206A470GXA
C70	R-21-1862	CAP, CHIP, 47 PF, 2 PCT	95275	VJ1206A2R7CF
C71	R-21-1780	CAP, CHIP, 2.7 PF	95275	VJ1206A3R9CF
C72	R-21-1782	CAP, CHIP, 3.9 PF	65238	1206N101K401N
C73-74	R-21-1857	CAP, CHIP, 100 PF, 400V	95275	VJ1206Y103MF
C75-78	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y333KF
C79	R-21-1808	CAP, CHIP, 33 NF	95275	VJ1206Y104MF
C80	R-21-1802	CAP, CHIP, 100 NF	95275	VJ1206Y103MF
C81	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y333KF
C82	R-21-1808	CAP, CHIP, 33 NF	32997	8131LP-100-25C-104M
C83	100133	CAP, CER, .1 UF, LOW PROFILE, 20 PERCENT	95275	VJ1206Y103MF
C84-85	R-21-1801	CAP, CHIP, 10 NF	61058	ECEA1EV470S
C86	R-21-0789	CAP, ALUM. ELEC., 47 UF, 25V	95275	VJ1025Y332KF
C87	R-21-1858	CAP, CHIP, 3.3 NF, 50V	95275	VJ1206Y103MF
C88	R-21-1801	CAP, CHIP, 10 NF	61058	ECEA1EV470S
C89	R-21-0789	CAP, ALUM. ELEC., 47 UF, 25V	95275	VJ1206Y103MF
C90-91	R-21-1801	CAP, CHIP, 10 NF	61058	ECEA1EV470S
C92	R-21-0789	CAP, ALUM. ELEC., 47 UF, 25V	95275	VJ1206Y103MF
C93	R-21-1801	CAP, CHIP, 10 NF	61058	ECEA1EV470S
C94-95	R-21-0789	CAP, ALUM. ELEC., 47 UF, 25V	95275	VJ1206Y103MF
C96-100	R-21-1801	CAP, CHIP, 10 NF	61058	ECEA1EV470S
C104-105	R-21-0789	CAP, ALUM. ELEC., 47 UF, 25V	95275	VJ1206Y103MF
C106	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y333KF
C107-108	R-21-1808	CAP, CHIP, 33 NF	95275	VJ1206Y103MF
C109-110	R-21-1801	CAP, CHIP, 10 NF	61058	ECEA1EV470S
C111-113	R-21-0789	CAP, ALUM. ELEC., 47 UF, 25V	61058	ECEA1HKP1PE
C114	R-21-0779	CAP, ELECT, 1 UF, 50V	95275	VJ1206Y103MF
C115	R-21-1801	CAP, CHIP, 10 NF		

R-16-1145, PCB ASSY., MOTHERBOARD (CONT'D)

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
C116	R-21-0789	CAP, ALUM. ELEC., 47 UF, 25V	61058	ECEA1EV470S
C117	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C118	R-21-1800	CAP, CHIP, 1 NF	95275	VJ1206Y102KF
C119	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C120	R-21-0789	CAP, ALUM. ELEC., 47 UF, 25V	61058	ECEA1EV470S
C121	R-21-0779	CAP, ELECT, 1 UF, 50V	61058	ECEA1HKP1RE
C125	R-21-0789	CAP, ALUM. ELEC., 47 UF, 25V	61058	ECEA1EV470S
C126	R-21-0779	CAP, ELECT, 1 UF, 50V	61058	ECEA1HKP1RE
C127	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C128	R-21-1800	CAP, CHIP, 1 NF	95275	VJ1206Y102KF
C129	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C130-131	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C132	R-21-1808	CAP, CHIP, 33 NF	95275	VJ1206Y333KF
C133	R-21-1808	CAP, CHIP, 33 NF	95275	VJ1206Y333KF
C225-226	R-21-0789	CAP, ALUM. ELEC., 47 UF, 25V	61058	ECEA1EV470S
D1-4	R-22-1029	DIODE, SILICON	14433	1N4149
D5	R-22-1099	DIODE, SILICON	17856	JPAD50
D6-7	R-22-1029	DIODE, SILICON	14433	1N4149
D8	R-22-1099	DIODE, SILICON	17856	JPAD50
D11	R-22-1662	DIODE, BRIDGE RECTIFIER	27777	VH240
D12	R-22-1664	DIODE, BRIDGE, 800 DF	27777	VM18
D13-15	R-22-1029	DIODE, SILICON	14433	1N4149
D16-25	210089	DIODE, LOW OFFSET SCHOTTKY	50434	HP5082-2835
D26	R-22-1029	DIODE, SILICON	14433	1N4149
D28	R-22-1029	DIODE, SILICON	14433	1N4149
D30-31	R-22-1801	DIODE, VOLTAGE REGULATOR, 2.7V, 400 MW	14433	ZPD2.7
D32-33	R-22-1809	DIODE, VOLTAGE REGULATOR, 5.6V, 400 MW	14433	ZF.5.6A
F31	R-23-0062	FUSE HOLDER	61935	FAU-031-3573
H1	R-17-1034	HYBRID TEC (NON-REPARABLE ITEM)	21793	R-17-1034
H2	R-17-1035	HYBRID DAC (NON-REPARABLE ITEM)	21793	R-17-1035
IC1	230750	IC, DIGITAL, ECL	04713	MC10215PDS
IC2	230797	IC, DIGITAL, TRIPLE LINE RECEIVER	04713	MC10116PDS
IC3	230200	IC, 12 VDC REGULATOR	04713	MC7812CT
IC4	230201	IC, REGULATOR	07263	UA7912UCQR
IC14	230797	IC, DIGITAL, TRIPLE LINE RECEIVER	04713	MC10116PDS
IC18	230790	IC, DIGITAL, CUSTOM CHIP	21793	230790
IC19	R-22-3807	IC, 8-BIT CMOS MICROPROCESSOR	04713	MC146805E2P
IC20	230805	IC, OCTAL TRANSPARENT LATCH, 3-STATE OUTPUT	18714	CD74HCT373EX
IC21	230368	IC, DEMULTIPLEXER	27014	SN74LS138N3
IC22	230367	IC, MEMORY	21793	230367
IC23	R-22-4807	IC, OCTAL BUFFER/LINE DRIVER, 3-STATE	18714	CD74HCT244E
IC24	230581	IC, OCTAL LATCH	18324	N74LS373N-8
IC25	230805	IC, OCTAL TRANSPARENT LATCH, 3-STATE OUTPUT	18714	CD74HCT373EX
IC26	230194	IC, DUAL D FLIP-FLOP	01295	SN74LS74AN3
IC27	230428	IC, QUAD 2 INPUT OR GATE	01295	SN74LS32N3
IC28	230248	IC, POSITIVE NAND GATE	01295	SN74LS10N3
IC29	230234	IC, HEX INVERTER	01295	SN74LS04N
IC30	R-22-4700	IC, QUAD 2-INPUT NAND GATE	21793	R-22-4700
IC31	R-22-4262	IC, QUAD OP-AMP	07263	UA3403PC
IC32	R-22-4756	IC, HEX SCHMITT TRIGGER	18324	HEF40106BP
IC34-35	R-22-4259	IC, MOS/FET INPUT, BI POLAR OUTPUT OP-AMP	18714	CA3140E
IC36	230735	IC, COMPARATOR, DUAL ULTRA FAST	51870	AD9687BD
IC38	230789	IC, DIGITAL, CUSTOM CHIP	21793	230789

R-19-1145, PCB ASSY., MOTHERBOARD (CONT'D)

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
IC41	230733	IC, DIGITAL, ECL FLIP-FLOP	04713	MC10231PDS
L1-2	R-23-7217	CHOKE, MAINS, 40 UH	25088	8822111-A-C7
L5-11	310151	CHOKE, 10 PERCENT, 100 UH	83125	DD100UH
L14-15	310152	CHOKE, WIDEBAND	02114	VK200-10/3B
L20	310151	CHOKE, 10 PERCENT, 100 UH	83125	DD100UH
LK1	601195	PLUG, JUMPER, 0.1 CTR, LOW PROFILE	00779	530153-2
LK2-3	600245	JUMPER, INSULATED	52210	L-2007-1
LK4	601195	PLUG, JUMPER, 0.1 CTR, LOW PROFILE	00779	530153-2
PL1-2	601250	CONN, 14-PIN RT. ANGLE, DUAL ROW	52072	CA-D14R-238-19
PL7	601208-013	CONN., PCB, PLUG, 30-PIN	52072	CA-S30-238-43
PL14	601208-012	CONN, PCB, PLUG, 5-PIN	52072	CA-S05-238-43
PL15	601208-016	CONN, PCB, PLUG, 3-PIN	52072	CA-S03-238-43
PL16	601208-015	CONN., PCB, PLUG, 10-PIN	52072	CA-S10-238-43
PL17	601208-012	CONN, PCB, PLUG, 5-PIN	52072	CA-S05-238-43
PL19	R-23-5175	PLUG, 2 X 3-WAY	27264	10-90-1061
PL20	R-23-5161	PLUG, RT. ANGLE, 2 ROW, 2 PIN	63878	929839-01-02
PL21	R-23-5168	PLUG, 2 X 10, 10-WAY	K0536	M20-998-10-05
Q1-3	R-22-6018	TRANSISTOR, PNP	04713	MPS3640
Q4	200298	TRANS, NPN	04713	2N3904
Q5	200299	TRANS, NPN	04713	2N3904
Q6	200302	TRANSISTOR, NPN	04713	MJE3055T
Q7	R-22-6113	TRANSISTOR, PNP	22119	ZTX550
Q8	200301	TRANSISTOR, PNP	04713	MJE2955T
Q9	R-22-6112	TRANSISTOR, NPN	22119	ZTX450
Q10	R-22-6112	TRANSISTOR, NPN	22119	ZTX450
Q11	200298	TRANS, NPN	04713	2N3904
Q12	200301	TRANSISTOR, PNP	04713	MJE2955T
Q13	R-22-6113	TRANSISTOR, PNP	22119	ZTX550
Q14	200298	TRANS, NPN	04713	2N3904
Q15-16	R-22-6153	TRANSISTOR, N-CH SILICON JFET	28848	BF256A
Q17-19	R-22-6205	TRANSISTOR, RF, NPN	22119	BFS17
Q21	R-22-6205	TRANSISTOR, RF, NPN	22119	BFS17
Q22	200298	TRANS, NPN	04713	2N3904
Q23	R-22-6205	TRANSISTOR, RF, NPN	22119	BFS17
Q24	200298	TRANS, NPN	04713	2N3904
Q25-27	200299	TRANS, PNP	04713	2N3906
Q28	R-22-6113	TRANSISTOR, PNP	22119	ZTX550
Q29	R-22-4216	IC, LINEAR HIGH CURRENT	18714	CA3083E
R1	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R2	R-20-5541	RES ARRAY, 9 X 1K OHM, 10 PIN SIL	81349	710A102
R3-4	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-330 OHM-5 PCT
R5	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R6	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-330 OHM-5 PCT
R7	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R8	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-10 OHM-5 PCT
R11	R-20-5765	RES, CHIP, 470 OHM, 1/8W, 5 PERCENT	65940	MCR18-470 OHM-5 PCT
R16	R-20-5765	RES, CHIP, 470 OHM, 1/8W, 5 PERCENT	65940	MCR18-470 OHM-5 PCT
R18	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R25	R-20-5768	RES, CHIP, 10K, 1/8W, 5 PERCENT	65940	MCR18-10K OHM-5 PCT
R29	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R32	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R33	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R35	R-20-5799	RES, CHIP, 4.7K, 1/8W, 5 PERCENT, 200V	65940	MCR18-4.7K-5 PCT

R-19-1145, PCB ASSY., MOTHERBOARD (CONT'D)

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
R40	R-20-5799	RES, CHIP, 4.7K, 1/8W, 5 PERCENT, 200V	65940	MCR18-4.7K-5 PCT
R45	000391	RES, CARBON, 390 OHM 1/4W, 5 PERCENT	81349	RC07GF390J
R46	R-20-5562	RES ARRAY, 10K, 10 PIN	61058	EXBF10V103G
R47	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R48	000121	RES, CARBON, 120 OHM, 1/4W, 5 PERCENT	81349	RC07GF120J
R49	R-20-5556	CUSTOM RES ARRAY, SIL	K1160	747026
R54	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R50	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R53	000391	RES, CARBON, 390 OHM 1/4W, 5 PERCENT	81349	RC07GF390J
R55	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R57	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-330 OHM-5 PCT
R58	R-20-5813	RES, CHIP, 100K, 1/8W, 5 PERCENT, 200V	65940	MCR18-100K-5 PCT
R75	R-20-5768	RES, CHIP, 10K, 1/8W, 5 PERCENT	65940	MCR18-10K OHM-5 PCT
R76	R-20-5813	RES, CHIP, 100K, 1/8W, 5 PERCENT, 200V	65940	MCR18-100K-5 PCT
R77	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-330 OHM-5 PCT
R78-81	001675	RES, CARBON, 100 OHM, 1/2W, 5 PERCENT	01121	RC20GF101J
R82	010990	RES, CARBON FILM, 900K, 1/2W, 0.25 PERCENT	80031	RN65C9003B
R83	010989	RES, METAL FILM, 111K, 1/8W, 0.25 PERCENT	80031	RN55C1113B
R84	010990	RES, CARBON FILM, 900K, 1/2W, 0.25 PERCENT	80031	RN65C9003B
R85	010989	RES, METAL FILM, 111K, 1/8W, 0.25 PERCENT	80031	RN55C1113B
R87-89	R-20-5554	CUSTOM RES ARRAY, SIL	21793	R-20-5554
R91	R-20-5554	CUSTOM RES ARRAY, SIL	21793	R-20-5554
R93	R-20-5817	RES, CHIP, 560K, 1/8W, 5 PERCENT, 200V	65940	MCR18-560K-5 PCT
R94	R-20-5784	RES, CHIP, 180 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-180 OHM-5 PCT
R95	R-20-5817	RES, CHIP, 560K, 1/8W, 5 PERCENT, 200V	65940	MCR18-560K-5 PCT
R96	R-20-5784	RES, CHIP, 180 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-180 OHM-5 PCT
R97	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-330 OHM-5 PCT
R98	R-20-5765	RES, CHIP, 470 OHM, 1/8W, 5 PERCENT	65940	MCR18-470 OHM-5 PCT
R100	R-20-5793	RES, CHIP, 1.2K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1.2K-5 PCT
R101	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-330 OHM-5 PCT
R102	R-20-5765	RES, CHIP, 470 OHM, 1/8W, 5 PERCENT	65940	MCR18-470 OHM-5 PCT
R104	R-20-5793	RES, CHIP, 1.2K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1.2K-5 PCT
R107	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R110	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R111-112	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-10 OHM-5 PCT
R113	R-20-5764	RES, CHIP, 100 OHM, 1/8W, 5 PERCENT	65940	MCR18-100 OHM-5 PCT
R115	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R116	R-20-5765	RES, CHIP, 470 OHM, 1/8W, 5 PERCENT	65940	MCR18-470 OHM-5 PCT
R117	R-20-5764	RES, CHIP, 100 OHM, 1/8W, 5 PERCENT	65940	MCR18-100 OHM-5 PCT
R119	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R120	R-20-5765	RES, CHIP, 470 OHM, 1/8W, 5 PERCENT	65940	MCR18-470 OHM-5 PCT
R121-124	R-20-5795	RES, CHIP, 2.2K, 1/8W, 5 PERCENT, 200V	65940	MCR18-2.2K-5 PCT
R125-126	R-20-5790	RES, CHIP, 680 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-680 OHM-5 PCT
R128	R-20-5785	RES, CHIP, 220 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-220 OHM-5 PCT
R129	R-20-5794	RES, CHIP, 1.5K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1.5K-5 PCT
R135	R-20-5813	RES, CHIP, 100K, 1/8W, 5 PERCENT, 200V	65940	MCR18-100K-5 PCT
R136	R-20-5768	RES, CHIP, 10K, 1/8W, 5 PERCENT	65940	MCR18-10K OHM-5 PCT
R137	R-20-5768	RES, CHIP, 10K, 1/8W, 5 PERCENT	65940	MCR18-10K OHM-5 PCT
R139	000100	RES, CARBON, 10 OHM, 1/4W, 5 PERCENT	81349	RC07GF100J
R140	R-20-5764	RES, CHIP, 100 OHM, 1/8W, 5 PERCENT	65940	MCR18-100 OHM-5 PCT
R141	R-20-5768	RES, CHIP, 10K, 1/8W, 5 PERCENT	65940	MCR18-10K OHM-5 PCT
R142	R-20-5780	RES, CHIP, 68 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-68 OHM-5 PCT
R143	000100	RES, CARBON, 10 OHM, 1/4W, 5 PERCENT	81349	RC07GF100J
R144	R-20-5764	RES, CHIP, 100 OHM, 1/8W, 5 PERCENT	65940	MCR18-100 OHM-5 PCT

R-19-1145, PCB ASSY., MOTHERBOARD (CONT'D)

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
R145	R-20-5768	RES, CHIP, 10K, 1/8W, 5 PERCENT	65940	MCR18-10K OHM-5 PCT
R146	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-10 OHM-5 PCT
R147	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R148	R-20-5797	RES, CHIP, 3.3K, 1/8W, 5 PERCENT, 200V	65940	MCR18-3.3K-5 PCT
R149-150	R-20-7071	POT, 10K, TOP ADJ	21793	R-20-7071
R151-152	R-20-5768	RES, CHIP, 10K, 1/8W, 5 PERCENT	65940	MCR18-10K OHM-5 PCT
R153-154	R-20-5799	RES, CHIP, 4.7K, 1/8W, 5 PERCENT, 200V	65940	MCR18-4.7K-5 PCT
R155	R-20-5813	RES, CHIP, 100K, 1/8W, 5 PERCENT, 200V	65940	MCR18-100K-5 PCT
R156	R-20-5799	RES, CHIP, 4.7K, 1/8W, 5 PERCENT, 200V	65940	MCR18-4.7K-5 PCT
R157	R-20-5763	RES, CHIP, 18 OHM, 1/8W, 5 PERCENT	65940	MCR18-18 OHM-5 PCT
R158	R-20-5764	RES, CHIP, 100 OHM, 1/8W, 5 PERCENT	65940	MCR18-100 OHM-5 PCT
R159	R-20-5780	RES, CHIP, 68 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-68 OHM-5 PCT
R160	R-20-5764	RES, CHIP, 100 OHM, 1/8W, 5 PERCENT	65940	MCR18-100 OHM-5 PCT
R161	R-20-5780	RES, CHIP, 68 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-68 OHM-5 PCT
R162-166	R-20-5764	RES, CHIP, 100 OHM, 1/8W, 5 PERCENT	65940	MCR18-100 OHM-5 PCT
R167-168	R-20-5797	RES, CHIP, 3.3K, 1/8W, 5 PERCENT, 200V	65940	MCR18-3.3K-5 PCT
R169	R-20-5778	RES, CHIP, 47 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-47 OHM-5 PCT
R170-171	000121	RES, CARBON, 120 OHM, 1/4W, 5 PERCENT	81349	RC07GF120J
R174	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R175	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R177	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R178	R-20-5797	RES, CHIP, 3.3K, 1/8W, 5 PERCENT, 200V	65940	MCR18-3.3K-5 PCT
R179	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R180	R-20-5768	RES, CHIP, 10K, 1/8W, 5 PERCENT	65940	MCR18-10K OHM-5 PCT
R181	R-20-5765	RES, CHIP, 470 OHM, 1/8W, 5 PERCENT	65940	MCR18-470 OHM-5 PCT
R185-187	R-20-5817	RES, CHIP, 560K, 1/8W, 5 PERCENT, 200V	65940	MCR18-560K-5 PCT
R188	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R189	R-20-5806	RES, CHIP, 27K, 1/8W, 5 PERCENT, 200V	65940	MCR18-27K-5 PCT
R190	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R191	R-20-5806	RES, CHIP, 27K, 1/8W, 5 PERCENT, 200V	65940	MCR18-27K-5 PCT
R192-193	R-20-7071	POT, 10K, TOP ADJ	21793	R-20-7071
R194	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-10 OHM-5 PCT
R195	R-20-5774	RES, CHIP, 22 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-22 OHM-5 PCT
R196	R-20-5784	RES, CHIP, 180 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-180 OHM-5 PCT
R198	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-10 OHM-5 PCT
R199	R-20-5774	RES, CHIP, 22 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-22 OHM-5 PCT
R200	R-20-5784	RES, CHIP, 180 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-180 OHM-5 PCT
R202-203	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R204	R-20-5799	RES, CHIP, 4.7K, 1/8W, 5 PERCENT, 200V	65940	MCR18-4.7K-5 PCT
R205-210	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-330 OHM-5 PCT
R211-213	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R214	R-20-5796	RES, CHIP, 2.2K, 1/8W, 5 PERCENT, 200V	65940	MCR18-2.2K-5 PCT
R215	R-20-5768	RES, CHIP, 10K, 1/8W, 5 PERCENT	65940	MCR18-10K OHM-5 PCT
R216	R-20-5780	RES, CHIP, 68 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-68 OHM-5 PCT
R217	R-20-5813	RES, CHIP, 100K, 1/8W, 5 PERCENT, 200V	65940	MCR18-100K-5 PCT
R218-225	R-20-5768	RES, CHIP, 10K, 1/8W, 5 PERCENT	65940	MCR18-10K OHM-5 PCT
R226	R-20-5780	RES, CHIP, 68 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-68 OHM-5 PCT
R227	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-10 OHM-5 PCT
R228	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R229	R-20-5796	RES, CHIP, 2.2K, 1/8W, 5 PERCENT, 200V	65940	MCR18-2.2K-5 PCT
RLA-RLD	R-23-7529	RELAY, REED, 1A	91718	G570X424
RLE	R-23-7530	RELAY, DIL, 1 FORM C	91718	GT231C-236
RLF-RLG	R-23-7528	RELAY, REED, 1A1B	21793	R-23-7528
RLH	R-23-7527	RELAY, DPDT	22958	172-5

R-18-1145, PCB ASSY., MOTHERBOARD (CONT'D)

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
S1	R-23-4124	MAINS SWITCH	21793	R-23-4124
SK5-6	501234	CONNECTOR, BNC, PCB MOUNT	U3441	TG-5000
SK8	R-23-5177	MAINS SELECTOR SOCKET	27264	09-03-1061
SK10	R-23-3429	MAINS SOCKET	2V900	P580/PC
T1	R-17-4102	TRANSFORMER, MAINS	21793	R-17-4102
(2)1	455117	HEATSINK ASSY.	21793	455117
(3)1	R-11-1706	CLAMP ASSY.	21793	R-11-1706
(4)1	R-13-1988	SCREEN	21793	R-13-1988
(5)1	R-13-2038	INSULATOR	21793	R-13-2038
(18)1	R-18-1145	P.C. BOARD, MOTHERBOARD (UNLOADED)	21793	R-18-1145
(381)3	511059	CONN, DIP, LOW PROFILE, 40-PIN	91506	240-AG39D
(386)2	920991	SOCKET, 28-PIN	52072	CA-28S-TSD-BC
(437)2	R-23-9148	INSULATING BUSH, M3	K1935	J22-5006
(439)5	510351	INSULATOR, TO-220	18565	60-11-5791-1674
(442)4	617041	NUT, HEX, M2.5	1CJ86	DIN934-M2.5
(444)4	617042	NUT, HEX, M3	1CJ86	DIN934-M3
(446)4	R-24-2800	WASHER, M2.5	21793	R-24-2800
(447)6	R-24-2801	WASHER, CRINKLE, M3	21793	R-24-2801
(448)1	R-24-2802	WASHER, M4	21793	R-24-2802
(449)3	R-24-2805	WASHER, M3.5	21793	R-24-2805
(450)12	R-24-3519	AV LUGS	19738	AVLUG1107/020B
(452)1	R-24-4146	STAND-OFF, M3 X 14	46384	KTF-M3-14-ET
(454)4	616306	SCREW, PAN. HD., M2.5 X 14	21793	616306
(455)6	616316	SCREW, PAN. HD., M3 X 8	1CJ86	7985-A-M2.5X14MM
(459)1	616344	SCREW, PAN HD., M4 X 12	1CJ86	7985-A-M4X12MM
(460)3	616328	SCREW, PAN HD., M3.5 X 6	1CJ86	7985-A-M3.5X6MM
(468)70MM	520999	WIRE, TEFLON STRANDED, 20 GA, WHITE	21793	520999
(470)70MM	520909	WIRE, TEFLON STRANDED, 20 GA, WHT/BK	92194	5856/7 WHT/BLK
(472)70MM	520929	WIRE, TEFLON STRANDED, 20 GA, WHT/RED	21793	520929
(475)40MM	500009	TUBING, SHRINK, .125 ID, BLK	29005	RNF-100-1-1/8

401820, PCB ASSY., GPIB

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
C1	110110	CAP, TANTA, 6.8 UF, 20V, 10 PERCENT	05397	T350115K020AS
C2-10	100062	CAP, CER, .01 UF 100V, 10 PERCENT	05397	C320C103K1R5CA
IC1-2	230802	IC, OCTAL D-TYPE F-F, 3-STATE	18714	CD74HCT374EX
IC3	230368	IC, DEMULTIPLEXER	27014	SN74LS138N3
IC4	230105	IC, HEX BUFFER/DRIVER	01295	SN7417N3
IC5	230330	IC, TRI-STATE BUFFER	01295	SN74LS367AN3
IC7	230193	IC, NAND GATE	01295	SN74LS00N3
IC8	230368	IC, DEMULTIPLEXER	27014	SN74LS138N3
IC9	230821	IC, CPU, CMOS, 64K EXT MEMORY	18714	CD6805E33X
IC10	230917	IC, MEMORY	21793	230917
IC11	230805	IC, OCTAL TRANSPARENT LATCH, 3-STATE OUTPUT	18714	CD74HCT373EX
IC12	230430	IC, GENERAL PURPOSE INTERFACE ADAPTER	04713	MC68488P
IC13	230247	IC, MOS BILATERAL SWITCH	18714	CD4066AEX
IC14	230472	IC, OCTAL GPIB TRANS	01295	SN75161AN3
IC15	230459	IC, OCTAL GPIB TRANS	01295	SN75160AN3
IC16	230194	IC, DUAL D FLIP-FLOP	01295	SN74LS74AN3
IC17	230799	IC, QUAD D W/SET & RESET	18714	CD74HCT74EX
IC18	230193	IC, NAND GATE	01295	SN74LS00N3
IC19	230305	IC, QUAD, 2 INPUT NOR GATES	01295	SN74LS02N3
IC20	230428	IC, QUAD 2 INPUT OR GATE	01295	SN74LS32N3
IC25	230716	IC, DIGITAL, 3 INPUT NOR	01295	SN74LS27N3
IC27	230368	IC, DEMULTIPLEXER	27014	SN74LS138N3
IC28	230648	IC, MEMORY, 2K X 8 RAM	61802	TMM2016P
R1	080082	RES NETWORK, 10P, 9RES, 3.3K, 2 PERCENT	11237	750-101-R3.3K
R2	000560	RES, CARB COMP, 56 OHM, 5 PERCENT 1/4W	81349	RC07GF560J
R3	080082	RES NETWORK, 10P, 9RES, 3.3K, 2 PERCENT	11237	750-101-R3.3K
R4-6	000331	RES, CARB COMP, 330 OHM, 5 PERCENT 1/4W	81349	RC07GF331J
R7	080024	RES NETWORK, 6P, 5RES, 3.3K, 2 PERCENT	11237	750-61-R3.3K
R8	000180	RES, CARB COMP, 18 OHM, 5 PERCENT 1/4W	81349	RC07GF180J
R9	000560	RES, CARB COMP, 56 OHM, 5 PERCENT 1/4W	81349	RC07GF560J
R10	000331	RES, CARB COMP, 330 OHM, 5 PERCENT 1/4W	81349	RC07GF331J
R17-18	080057	RES NETWORK, 9P, 7RES, 100K, 2 PERCENT	11237	750-81-R100K
R19	000472	RES, CARB COMP, 4.7K, 5 PERCENT, 1/4W	81349	RC07GF472J
R20	080082	RES NETWORK, 10P, 9RES, 3.3K, 2 PERCENT	11237	750-101-R3.3K
R51-52	000102	RES, CARB COMP 1.0K 5 PERCENT 1/4W	81349	RC07GF102J
R53	000103	RES, CARB COMP, 10K, 5 PERCENT 1/4W	21793	RC07GF103J
R54	000332	RES, CARBON, 3.3K, 1/4W, 5 PERCENT	81349	RC07GF332J
SK2	601249	CONN, DIP, RIGHT ANGLE, 14-PIN	52072	CA-14SE-10RA03-01
SK3	601582	CONN, RECEPTACLE, 24 PIN	00779	553811-4
SK4	R-23-5151	PLUG, RT. ANGLE, 2 ROW, 2 PIN	63573	929838-01-02
SW1	800814	SWITCH-SLIDE-6SPST	02660	31-010
(A6)1	411820	PCB, GPIB (UNLOADED)	21793	411820
(A7)1	601196	PLUG, JUMPER, 0.1 CTR, LOW PROFILE	00779	530153-2
(A2)1	601247	CABLE ASSY, 28 PIN	52072	CA-D28P02-28-1-TT-430
(A5)2	611059	CONN, DIP, LOW PROFILE, 40-PIN	91506	240-AG39D
(A5)2	616252	SCREW, PPH,SEMS ASSY,4-40X.312	78189	83-040545-25
(A7)1	930010	HARDWARE KIT, STANDOFF, STUD MOUNT	00779	552533-3
(A8)1	920624	SOCKET, IC, 24-PIN	52072	CA-24STSD-BC
(A9)1	920891	SOCKET, 28-PIN	52072	CA-28S-TSD-BC
(A5)1	R-11-1603	G.P.I.B. PLATE ASSY.	21793	R-11-1603

404386, OSCILLATOR ASSY. (04E)

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
J14	611056	CONNECTOR, CABLE, 5-PIN	21793	611056
(1)1	401822	PCB, DOUBLER (UNLOADED)	21793	411822
(2)1	454879	OSCILLATOR, 5 MHz FREQ. STD (NON-REPARABLE ITEM)	21793	454879
(4)A/R	500064	TUBING, SHRINK, .093 ID, BLK	29005	RNF-100-1-3/32
(6)2	610304	SPACER, .250D X .125 LG	21793	610304
(8)2	611074	SCREW, METRIC PAN HD., M3 X 10	21793	611074
(10)2	617102	WASHER, FLAT, #4, LIGHT SERIES	96906	MS15795-803
(11)2	617127	WASHER, LOCK, #4	88044	AN935C4
(13)A/R	500063	TUBING, SHRINK, .125 ID, BLK	29005	RNF-100-1-1/8
(15)A/R	500174	WIRE, TEFLON COAX	21793	500174
(17)A/R	524555	WIRE, TEFLON, STRANDED, 24 GA, GRN	21793	524555
(18)A/R	524929	WIRE, TEFLON, STRANDED, 24 GA, WHT/RED	21793	524929
(20)3	610777	CABLE TIE	16956	08-432
(22)*	611052	KEY, POLARIZING, PLUG	00779	87077-1
(23)3	611053	TERMINAL, CRIMP	00779	530553-2

401822, PCB ASSY., DOUBLER

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
C1-6	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
D1-2	R-22-1029	DIODE, SILICON	14433	1N4149
L1	310151	CHOKE, 10 PERCENT, 100 UH	83125	DD100UH
Q1-2	200299	TRANS, PNP	04713	2N3906
Q3-6	200298	TRANS, NPN	04713	2N3904
R1	R-20-5776	RES, CHIP, 33 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-33 OHM-5 PCT
R2-3	R-20-5764	RES, CHIP, 100 OHM, 1/8W, 5 PERCENT	65940	MCR18-100 OHM-5 PCT
R4	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R5-6	R-20-5785	RES, CHIP, 470 OHM, 1/8W, 5 PERCENT	65940	MCR18-470 OHM-5 PCT
R7	R-20-5794	RES, CHIP, 1.5K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1.5K-5 PCT
R8-9	R-20-5798	RES, CHIP, 3.9K, 1/8W, 5 PERCENT, 200V	65940	MCR18-3.9K-5 PCT
R10	R-20-5794	RES, CHIP, 1.5K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1.5K-5 PCT
R11	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R12	R-20-5803	RES, CHIP, 39K, 1/8W, 5 PERCENT, 200V	65940	MCR18-39K-5 PCT
R13	R-20-5803	RES, CHIP, 15K, 1/8W, 5 PERCENT, 200V	65940	MCR18-15K-5 PCT
R14	R-20-5816	RES, CHIP, 330K, 1/8W, 5 PERCENT, 200V	65940	MCR18-330K-5 PCT
R15	R-20-5768	RES, CHIP, 10K, 1/8W, 5 PERCENT	65940	MCR18-10K OHM-5 PCT
R16	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R17-18	R-20-5798	RES, CHIP, 3.9K, 1/8W, 5 PERCENT, 200V	65940	MCR18-3.9K-5 PCT
R19	R-20-5764	RES, CHIP, 100 OHM, 1/8W, 5 PERCENT	65940	MCR18-100 OHM-5 PCT
R20	R-20-5792	RES, CHIP, 1K, 1/8W, 5 PERCENT, 200V	65940	MCR18-1K-5 PCT
R21	R-20-5814	RES, CHIP, 51 OHM, 1/8W, 5 PERCENT, 200V	65940	MCR18-51 OHM-5 PCT
T1-2	R-23-7149	TRANSFORMER	21793	R-23-7149
TP1	R-24-3537	TERMINAL ASSY.	21793	R-24-3537
(10)1	411822	PCB, DOUBLER (UNLOADED)	21793	411822
(58)3	R-24-3519	AV LUGS	19738	AVLUG1107/0208

R-19-1147 – OSCILLATOR ASSY (STANDARD)

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
C1	100133	CAP, CERAM, .1 UF, LOW PROFILE, 20 PERCENT	32897	8131LP-100-25U-104M
OSC1	921013	OSCILLATOR, 10 MHZ	21793	921013
SK14	R-23-5166	CONNECTOR, 5-WAY	21793	R-23-5166
(6)1	R-18-1147	PCB, OSCILLATOR(UNLOADED)	21793	R-18-1147

R-18-1205, B.N.C. MOUNTING BOARD ASSY.

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
SK19-20	R-23-5159	CONNECTOR, FEMALE, DUAL-ROW, 2 X 2 WAY	63878	929975-02
(1)1	R-15-0138	LABEL	21793	R-15-0138
(8)1	R-18-1206	P.B. BOARD, BNC MOUNTING (UNLOADED)	21793	R-18-1206
(10)3	R-23-3421	BNC SOCKET	24931	28JR175-7

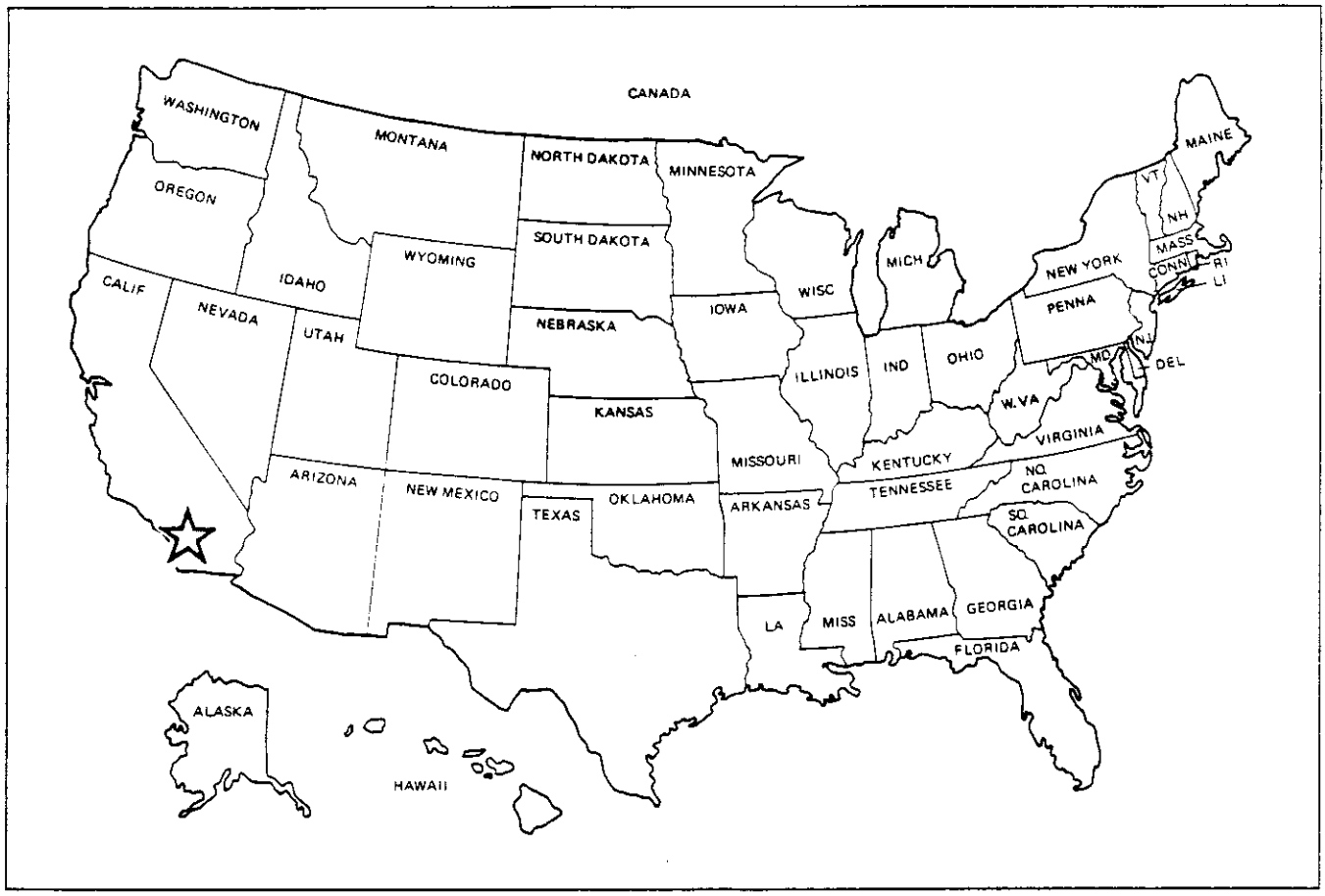
R-19-1164 – REFERENCE FREQUENCY MULTIPLIER ASSY.

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
C1	R-21-1808	CAP, CHIP, 33 NF	95275	VJ1206Y333KF
C2	R-21-6043	CAP, TRIMMER, 2-15P	18324	R-21-6043
C3	R-21-1838	CAP, CHIP, 220 PF	95275	VJ1206A221JF
C4	R-21-1838	CAP, CHIP, 220 PF	95275	VJ1206A221JF
C5	R-21-1808	CAP, CHIP, 33 NF	95275	VJ1206Y333KF
C6	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C7	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C8	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C9	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C10	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C11	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C12	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
C13	R-21-1808	CAP, CHIP, 33 NF	95275	VJ1206Y333KF
C14	R-21-1808	CAP, CHIP, 33 NF	95275	VJ1206Y333KF
C15	R-21-1801	CAP, CHIP, 10 NF	95275	VJ1206Y103MF
D1	R-22-1097	DIODE, VARACTOR	04713	R-22-1097
D2	R-22-1093	DIODE, SILICO	22119	R-22-1093
D3	R-22-1882	DIODE, VOLTAGE REGULATOR	22119	R-22-1882
D4	R-22-1096	DIODE, SILICO	22119	R-22-1096
D5	R-22-1096	DIODE, SILICO	22119	R-22-1096
IC2	R-22-4292	IC,HA-741CD	01295	R-22-4292
IC3	R-22-4514	IC	04713	R-22-4514
IC4	R-22-4582	IC	04713	R-22-4582
Q1	R-22-6197	TRANSISTOR	22119	R-22-6197
Q2	R-22-6199	TRANSISTOR	22119	R-22-6199
Q3	R-22-6199	TRANSISTOR	22119	R-22-6199
Q4	R-22-6197	TRANSISTOR	22119	R-22-6197
Q5	R-22-6197	TRANSISTOR	22119	R-22-6197
Q6	R-22-6197	TRANSISTOR	22119	R-22-6197
Q7	R-22-6197	TRANSISTOR	22119	R-22-6197
R1	R-20-5785	RES, CHIP, 220 OHM,1/8W,5 PCT,200V	65940	MCR18-220 OHM-5 PCT
R2	R-20-5768	RES, CHIP, 10K, 1/8W, 5 PCT	65940	MCR18-10K OHM-5 PCT
R3	R-20-5802	RES,CHIP,12K,1/8W,5 PCT	65940	MCR18-12K-5 PCT
R4	R-20-5795	RES, CAP, 1.8K,1/8W, 5 PCT/5	18324	R-20-5795
R5	R-20-5813	RES, CHIP, 100K, 1/8W, 5 PCT, 200V	65940	MCR18-100K-5 PCT
R6	R-20-5817	RES, CHIP, 560K, 1/8W, 5 PCT, 200V	65940	MCR18-560K-5 PCT
R7	R-20-5768	RES, CHIP, 10K, 1/8W, 5 PCT	65940	MCR18-10K OHM-5 PCT
R8	R-20-5796	RES, CHIP, 2.2K, 1/8W, 5 PCT, 200V	65940	MCR18-2.2K-5 PCT
R9	R-20-5796	RES, CHIP, 2.2K, 1/8W, 5 PCT, 200V	65940	MCR18-2.2K-5 PCT
R10	R-20-5789	RES, CHIP, 560 OHM,1/8W,5 PCT	18324	R-20-5789
R11	R-20-5795	RES, CAP, 1.8K,1/8W, 5 PCT/5	18324	R-20-5795
R12	R-20-5787	RES, CHIP, 330 OHM,1/8W,5 PCT,200V	65940	MCR18-330 OHM-5 PCT
R13	R-20-5796	RES, CHIP, 2.2K, 1/8W, 5 PCT, 200V	65940	MCR18-2.2K-5 PCT
R14	R-20-5768	RES, CHIP, 10K, 1/8W, 5 PCT	65940	MCR18-10K OHM-5 PCT
R15	R-20-5768	RES, CHIP, 10K, 1/8W, 5 PCT	65940	MCR18-10K OHM-5 PCT
R16	R-20-5791	RES, CHIP, 820 OHM,1/8W,5 PCT	18324	R-20-5791
R17	R-20-5779	RES, CHIP, 56 OHM, 1/8W, 5 PCT,200V	65940	MCR18-56 OHM-5 PCT
R18	R-20-5787	RES, CHIP, 330 OHM,1/8W,5 PCT,200V	65940	MCR18-330 OHM-5 PCT
R19	R-20-5795	RES, CAP, 1.8K,1/8W, 5 PCT/5	18324	R-20-5795
R20	R-20-5779	RES, CHIP, 56 OHM, 1/8W, 5 PCT,200V	65940	MCR18-56 OHM-5 PCT
R21	R-20-5779	RES, CHIP, 56 OHM, 1/8W, 5 PCT,200V	65940	MCR18-56 OHM-5 PCT
R22	R-20-5791	RES, CHIP, 820 OHM,1/8W,5 PCT	18324	R-20-5791
R23	R-20-5795	RES, CAP, 1.8K,1/8W, 5 PCT/5	18324	R-20-5795
R24	R-20-5795	RES, CAP, 1.8K,1/8W, 5 PCT/5	18324	R-20-5795
R25	R-20-5795	RES, CAP, 1.8K,1/8W, 5 PCT/5	18324	R-20-5795
R26	R-20-5795	RES, CAP, 1.8K,1/8W, 5 PCT/5	18324	R-20-5795
R27	R-20-5785	RES, CHIP, 220 OHM,1/8W,5 PCT,200V	65940	MCR18-220 OHM-5 PCT
R28	R-20-5785	RES, CHIP, 220 OHM,1/8W,5 PCT,200V	65940	MCR18-220 OHM-5 PCT

R-19-1164 – REFERENCE FREQUENCY MULTIPLIER ASSY. (CONT'D)

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
R29	R-20-5785	RES, CHIP, 220 OHM,1/8W,5 PCT,200V	65940	MCR18-220 OHM-5 PCT
R30	R-20-5785	RES, CHIP, 220 OHM,1/8W,5 PCT,200V	65940	MCR18-220 OHM-5 PCT
R31	R-20-5785	RES, CHIP, 220 OHM,1/8W,5 PCT,200V	65940	MCR18-220 OHM-5 PCT
SK16	R-23-5166	CONNECTOR, 5-WAY	21793	R-23-5166
SK17	R-23-5167	CONNECTOR, 10-WAY	21793	R-23-5167
T1	R-17-3226	TRANSFORMER	21793	R-17-3226

RACAL-DANA Instruments Inc.



SALES, APPLICATIONS AND SERVICE SUPPORT

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REPAIR REQUEST FORM

To allow us to better understand your repair requests, we suggest you use the following outline and include a copy with your instrument to be sent to your local Racal-Dana repair facility.

Model Number _____ Options _____ Date _____

Serial Number _____ P. O.# _____

Company Name _____

Address _____

City _____ State _____ Zip Code _____

Contact _____ Phone Number _____

1. Describe, in detail, the problem and symptoms you are having.

_____

_____

2. If you are using your unit on the bus, please list the program strings used and the controller type, if possible.

_____

_____

3. List all input levels, and frequencies this failure occurs.

_____

_____

4. Indicate any repair work previously performed.

_____

_____

5. Please give any additional information you feel would be beneficial in facilitating a faster repair time. (I. E., modifications, etc.)

_____

_____