4.14.2 When the instrument is first switched on the percent store will be loaded with 1 volt. The value in the store can be displayed and, if necessary, changed using the same procedures as those described for the ratio store. The keyboard address of the percent store is

/%/.

4.15 NULL MEASUREMENTS

4.15.1 With the null function selected the instrument computes

measured voltage - voltage value in null store.

To select the null function, press

/NULL/.

The NULL indicator will light. The current displayed value will be entered into the NULL store, and the display will indicate zero. When the input level is changed the display will indicate a difference of voltages or powers according to whether the voltage or power measuring function is selected. The conversion to power units uses the current resistance value in the Ω store.

4.15.2 When the null function is selected the contents of the NULL store can be displayed and, if required, changed using the same procedures as those described for the ratio store. This allows the difference between the measured value and an operator set value to be displayed. The keyboard address of the NULL store is

/NULL/

Note that, if the instrument leaves and re-enters the null measurement function, the value in the NULL store will be over-written with the measured value current when the mode is re-entered.

4.16 dB MEASUREMENTS

4.16.1 With the dB function selected the instrument computes

$$20 \log \frac{\text{measured volts}}{\text{voltage value in dB store}}$$

The calculation does not involve the resistance value held in the Ω store. However, if the voltage value in the dB store and the resistance value in the Ω store represent a power of 1 mW, the display units annunciator will indicate dBm. To select the dB function, press

/dB/.

The dB indicator will light.

4.16.2 When the instrument is first switched on the dB store will be loaded with 223.6 mV. The value in the store can be displayed and, if necessary, changed using the same procedures as those described for the ratio store. The keyboard address of the dB store is

/dB/.

4.17 ANALOGUE DISPLAY

4.17.1 The analogue display will be found to be particularly useful for obtaining peak or trough indications but may be used with all the measurement functions. The display is switched on and off by successive operations of

/METER/.

The coarse part of the display is automatically switched on when the manual ranging mode is selected. To obtain the full display press

/METER//METER/.

4.18 STORAGE OF FRONT PANEL SETTINGS

4.18.1 Up to 12 complete sets of front panel settings may be stored for later recall. The settings stored are:

(a) Primary measurement function

(b) Computed measurement function

(c) Measurement range

(d) Ranging mode

(e) Contents of Ω, RATIO, %, NULL and dB stores

(f) User ECAL factors

(g) User ECAL factor enablement

(h) Calibration factors

(j) Calibration factor enablement

(k) Averaging period

(l) Measuring head selected

Each set of front panel settings should be allocated a numeric address in the range 01 to 12. To store the front panel settings, press

/STORE//DIGIT*//DIGIT*/.

* of the allocated address

Note that the leading zero must be entered for addresses 01 to 09. The STORE indicator will light when the key is pressed. It will be extinguished, and the instrument will return to the measurement mode with panel settings unchanged, when storage is completed.

4.18.2 The front panel settings can be recalled by pressing

/RECALL//DIGIT*//DIGIT*/.

* of the allocated address

The RECALL indicator will light when the key is pressed. It will be extinguished, and the instrument will be reset to the measurement mode with the recalled front panel settings, when the recall is complete. The pressing of

/RECALL//0//0/

will recall the switch-on state (initialisation) settings. The stored front panel settings are not lost on recall, so that stored patterns may be recalled as often as required. Individual settings in the stored pattern cannot be amended, so changes must be made by over-writing the stored pattern with a complete, revised pattern.

4.18.3 When the power to the instrument is switched off the front panel settings are automatically stored. They can be recalled immediately after switching on again by pressing

/RECALL//9//9/.

The first change of front panel settings after switching on overwrites the data stored in location 99. The facility of recalling the settings in use when the instrument was switched off is then lost.

4.19 SPECIAL FUNCTIONS

4.19.1 A number of special functions are available to the operator. These are listed in Table 4.1, and are called by pressing

/MSD*//DIGIT//.//LSD*//SHIFT//SF/.

* of the special function number

4.20 ERROR CODES

4.20.1 The instrument is able to detect a numer of error states, some of which are indicated on the display. The meanings of the error codes are given in Table 4.2.

TABLE 4.1

Special Functions

Special Function Number	Function
0	Cancels all special functions.
20.0	Allows timed, automatic internal calibrations (ACAL).
20.1	Initiates an immediate ACAL.
20.2	Inhibits automatic ACAL.
30.0	Switches off external calibrator.
30.1	Turns on external calibrator.
40.0	Displays ACAL factor.
40.1	Displays USER ECAL factor.
40.2	Displays USER ECAL noise cancellation factor.
40.3	Displays FACTORY ECAL factor.
40.4	Displays FACTORY ECAL noise cancellation factor.

Note: (1) To return to the measurement mode press /CONTINUE/.

(2) The ECAL and noise cancellation factors displayed relate to the measuring head selected.

50.0	Selects the fixed average mode.
50.1	Selects the continuous average mode.
70.1	Initiates FACTORY ECAL cycle.
80.0	Allows over range (Or) and under range (Ur) indication.
80.1	Inhibits Or and Ur indication.
81.0	Displays software issue number

Note: (1) To return to the measurement mode press /CONTINUE/.

(2) The software issue number is displayed in the format XY.Z

The number XY is the last two digits of the Racal-Dana part number of one of the ROMs fitted, and identifies the hardware compatible set in use. The number Z is the issue number. (Early model instruments display the number Z only).

TABLE 4.2

Error Codes

Error	Error Code
Non-Volatile memory contents corrupted	01
Over range signal	02
Under range signal	03
Computed result to be displayed exceeds display capacity	11
Number entered to be stored has incorrect format	12
Zero entered as a number to be stored	13
Measuring head USER ECAL factor outside allowed range	14
Noise measured during USER ECAL outside allowed range	15
Both noise and USER ECAL factor outside allowed range	16
Stored noise value more than 20 µV greater than input	17
GPIB syntax error	18
RAM failure	20
ROM failure, IC16 on 19-1014	23
ROM failure, IC17 on 19-1014	24
ROM failure, IC18 on 19-1014	25
ROM failure, IC19 on 19-1014	26

Note: (1) Errors 02 and 03 are displayed as Or and Ur. Error 18 is not displayed. The other errors displayed appear as Er followed by two digits.

(2) When Error 01 is detected, nominal values are entered in the FACTORY ECAL, USER ECAL and CALIBRATION FACTOR memory locations. The display will flash Error 01, and the EXT CAL indicator will flash to indicate that the FACTORY ECAL factor stored is not valid. To return the instrument to an operational state, carry out the FACTORY ECAL procedure given in paragraph 4.4.1 in respect of <u>both</u> INPUT sockets.

(3) When Error 01 is detected the switch-on state front panel settings are entered into memory locations 01 to 12.

4.21 CONTROL VIA THE GPIB

4.21.1 The 9303 can be operated via the GPIB in either the addressed mode or the talk only mode. In the former the instrument makes measurements in response to commands, prefaced by the instrument's listen address, sent via the bus by the controller. The last measured value is loaded onto the bus when the instrument is addressed to talk.

4.21.2 In the talk only mode the 9303 will take measurements continually, at a rate determined by the averaging time in use, in accordance with instructions entered using the front panel controls. At the end of each measurement cycle the measured value is entered into a buffer store, from where it is loaded onto the bus in response to a signal on the NRFD line (commencement of the handshake sequence). If a measurement cycle is completed while data transfer is in progress, the updating of the buffer store is delayed until the data transfer is completed.

4.22 REMOTE/LOCAL CHANGEOVER

4.22.1 LOCAL TO REMOTE CONTROL CHANGEOVER

4.22.1.1 The 9303 is switched from local to remote control by the following sequence of control and data line messages:

(a)	Remote enable (REN) true (low)	This primes the remote control enable, but the 9303 remains in local control. REN must remain true if any instrument on the bus is to remain in remote control.
(b)	Attention (ATN) true (low)	
(c)	Listen address	The 9303 enters the listener addressed state (LADS) on recognition of its listen address.
(d)	ATN false (high)	The 9303 enters the listener active state (LACS) after a delay, and enters the remote state (REMS) on receipt of the first data byte.

4.22.1.2 No change to any of the 9303 control settings occurs on changeover from local to remote control.

4.22.2 REMOTE TO LOCAL CONTROL CHANGEOVER

4.22.2.1 The 9303 will be switched from remote to local control on:

(a) Operation of the front panel LOCAL key. This is effective only if local lockout is not set.

(b) Receiving the go to local (GTL) command when in the LADS.

(c) Receiving the REN message false (high). This is independent of the addressed state of the 9303.

4.22.2.2 No change to any of the 9303 control settings occurs on changeover from remote the local control.

4.22.3 LOCAL LOCKOUT (LLO)

4.22.3.1 Operation of the front panel LOCAL key during the transfer of data to the 9303 could result in the instrument being switched from remote to local control with the control settings in an unknown state. To prevent this the LOCAL key can be disabled by setting local lockout.

4.22.3.2 Local lockout may be set at any time when the REN message is true (low). The recognition of the LLO message is not dependent on the addressed state of the instrument. Apart from the disablement of the LOCAL key it causes no changes to the operation of the 9303. The only method of cancelling LLO is to sent the REN message false (high). This affects all instruments on the bus, putting them to the local control state (LOCS).

4.23 COMMAND CODES FOR ADDRESSED MODE OPERATION

4.23.1 Once the 9303 has been addressed the instrument functions can be set by means of device dependent commands, consisting of pairs of alpha and numeric characters, as listed in Tables 4.4 to 4.17. If more than one command is to be sent no delimiter is required. The end of message may be signalled by sending any of the terminating groups shown in Table 4.3. The changes in 9303 operation are implemented at the end of the message.

TABLE 4.3

Permitted Terminating Groups

1	2	3	4	5
CR EOI true	LF	CR,LF	CR,LF EOI true	LF EOI true

TABLE 4.4

Primary Measurement Function Commands

Function	Code
Volts	FØ
Watts	F1

TABLE 4.5

Ω Store Commands

Function	Code
Store contents of numerical input buffer in Ω store	Q1
Load contents of the Ω store into the output buffer	Q2

Note: After loading the contents of a store into the output buffer the 9303 must be put to the talker active state for the data to be put onto the bus. The instrument will return to the measurement mode once the output buffer is loaded, but failure to read the buffer contents will prevent measurement data being entered.

TABLE 4.6

Compute Function Commands

Function	Code
Select RATIO	G1
Store the contents of the numerical input buffer in the RATIO store. If the numerical input buffer is empty, store the last measured value.	G2
Load the RATIO store contents into the output buffer	G3
Select dB	L1
Store the contents of the numerical input buffer in the dB store. If the numerical input buffer is empty, store the last measured value	L2
Load the dB store contents into the output buffer	L3
Select NULL	N1
Store the contents of the numerical input buffer in the NULL store. If the numerical input buffer is empty store the last measured value	N2
Load the NULL store contents into the output buffer	N3
Select %	P1
Store the contents of the numerical input buffer in the % store. If the numerical input buffer is empty, store the last measured value	P2
Load the % store contents into the output buffer	P3

Note: (1) Selection of one compute function will automatically cancel any other compute function. Cancellation code CØ allows cancellation of all computed functions.

(2) The numerical input buffer is cleared, if required, by means of cancellation code C1.

(3) After loading the contents of a store into the output buffer the 9303 must be put to the talker active state for the data to be put onto the bus. The instrument will return to the measurement mode once the output buffer is loaded, but failure to read the buffer contents will prevent measurement data being entered.

TABLE 4.7

Range Commands

Range	Code
Autorange	RØ
300 µV	R1
1 mV	R2
3 mV	R3
10 mV	R4
30 mV	R5
100 mV	R6
300 mV	R7
1 V	R8
3 V	R9
Manual Range	RM
Load the output buffer with the full scale value of the range in use	RZ

Note: (1) The use of code RM will take the instrument from the autorange mode to the manual range mode without changing the range in use.

(2) After loading the contents of a store into the output buffer the 9303 must be put to the talker active state for the data to be put onto the bus. The instrument will return to the measurement mode once the output buffer is loaded, but failure to read the buffer contents will prevent measurement data being entered.

TABLE 4.8

Head Selection Commands

Measuring Head	Code
Front	VØ
Rear	V1

TABLE 4.9

Calibrator Control Commands

Function	Code
External calibration turned off	WØ
External calibration turned on	W1

TABLE 4.10

Control Setting Storage Commands

Function	Code
Store current control settings and stored values in memory locations numbered Ø1 to 12	AØ1 to A12

Note: Memory location ØØ always contains the values set when the instrument is first switched on, and cannot be overwritten.

TABLE 4.11

Control Setting Recall Commands

Function	Code
Recall and set initial control settings	BØØ
Recall and set control settings from stores numbered Ø1 to 12	BØ1 to B12
Recall control settings in use when instrument was last switched off	B99

Note: (1) The data stored in location 99 is overwritten as each change of instrument settings is made. The facility for recalling the settings in use when the instrument was switched off is only available immediately after switching on.

(2) Either the Device Clear (DCL) or the Selective Device Clear (SDC) command may be used instead of BØØ.

TABLE 4.12

Calibrate Commands

Function	Code
Disable USER ECAL factor	KØ
Enable USER ECAL factor	K1
Measure and store USER ECAL factor	K2
Load contents of USER ECAL store into the output buffer	K3
Load contents of noise cancellation store into the output buffer	K4
Timed ACAL sequences enabled	K5
Trigger an immediate ACAL	K6
ACAL inhibited	K7

Note: Codes KØ to K4 relate to the measuring head selected when the command is executed.

TABLE 4.13

Calibration Factor Commands

Function	Code
Disable calibration factor	UØ
Enable calibration factor	U1
Store contents of numerical input buffer in calibration factor store	U2
Load contents of calibration factor store into the output buffer	U3

Note: (1) Codes UØ to U3 relate to the measuring head selected when the command is executed.

(2) After loading the contents of a store into the output buffer the 9303 must be put to the talker active state for the data to be put onto the bus. The instrument will return to the measurement mode once the output buffer is loaded, but failure to read the buffer contents will prevent measurement data being entered.

TABLE 4.14

Interrupt Commands

Function	Code
No service requests generated	IØ
Service request generated when measured value is available	I1
Service request generated when error is detected	I2
Service request generated when measured value is available or when error is detected.	I3
Load error code number into output buffer	I4

Note: (1) After loading the contents of a store into the output buffer the 9303 must be put to the talker active state for the data to be put onto the bus. The instrument will return to the measurement mode once the output buffer is loaded, but failure to read the buffer contents will prevent measurement data being entered.

(2) The loading of the error code into the output buffer does not cancel the error code. Error codes other than Ø1 are cancelled using the cancellation code C2.

TABLE 4.15

Measurement Averaging Mode and Timing Selection Commands

Function	Code
Select fixed averaging mode	SØ
Select continuous averaging mode	S1
Store contents of numerical input buffer in the AVERAGE store	S2
Load contents of the AVERAGE store into the output buffer	S3
Store contents of numerical input buffer in the TRIGGER DELAY store	S4
Load contents of the TRIGGER DELAY store into the output buffer	S5

Note: After loading the contents of a store into the output buffer the 9303 must be put to the talker active state for the data to be put onto the bus. The instrument will return to the measurement mode once the output buffer is loaded, but failure to read the buffer contents will prevent measurement data being entered.

TABLE 4.16

Trigger Commands

Function	Code
Perform continuous measurement cycles, updating the output buffer at the end of each cycle	TØ
Leave the continuous measurement mode and enter the triggered measurement mode	T1
If in the triggered measurement mode, perform one averaged measurement and update the output buffer.	T2
If in the triggered measurement mode, perform one averaged measurement after a delay, equal to the value in the trigger delay store, and update the output buffer.	T3

Note: (1) After a change of range a three second delay, additional to that held in the trigger delay store, is automatically inserted after the trigger command.

(2) The Group Execute Trigger (GET) command may be used instead of code T2 using the following procedure:

a) Send command T1.

b) Send command T2. The 9303 will perform one measurement cycle.

c) Send the GET command each time a further measurement cycle is required. Note that, when using the GET command, the 9303 must be put to the talker active state after each measurement cycle.

(3) The use of the GET command after code TØ has been used will terminate the current measurement cycle. A new cycle will begin immediately.

(4) The instrument will revert to continuous measurement if the continuous averaging mode is selected (see Table 4.15). If the continuous averaging mode is cancelled the instrument will return to the last trigger mode enabled.

TABLE 4.17

Cancellation Commands

Function	Code
Cancel compute functions	CØ
Clear numerical input buffer	C1
Clear error code	C2

Note: Code C2 will not cancel error code Ø1.

4.24 ENTRY OF NUMERICAL VALUES

4.24.1 The format for numbers to be entered in the numerical input buffer for subsequent loading into the internal stores is given in Table 4.18.

TABLE 4.18

Numerical Input Format

Byte	Interpretation	Permitted ASCII Characters
1	Sign of mantissa	Space or +
2 3 4 5 6	Most significant digit Digit/decimal point Digit/decimal point Digit/decimal point Least significant digit	Up to four digits, with a decimal point if required, may be entered. Unused bytes need not be filled. Excess spaces are ignored.
7	Exponent indicator	E or e
8	Sign of exponent	Space, + or -
9	Digit	0 to 9

Note: (1) An unsigned mantissa or exponent is assumed positive. Bytes 1 and/or 8 may be omitted when the sign is positive.

(2) The string may be terminated with CR, LF or by the first byte of the succeeding command.

(3) If the exponent group is not required bytes 7 to 9 may be omitted.

(4) The exponent group replaces the units keys used when entering values in local control. The units assumed by the numbers held in store are given in Table 4.19.

TABLE 4.19

Stored Value Units

Store	Units	
	VOLTS Mode	WATTS Mode
Ohms	Ω	Ω
Ratio	Volts	Watts
%	Volts	Watts
Null	Volts	Watts
dB	Volts	Watts
Average	Seconds	Seconds
Time Out	Seconds	Seconds
Calibration factor	Number	Number

4.25 OUTPUT MESSAGE FORMAT

4.25.1 The same output message format is used for the transmission of measured values, error code numbers or the values held in the instrument's internal stores. The message consists of a string of 12 ASCII characters for each value transmitted. These are to be interpreted as shown in Table 4.20. No parity check is included. Each byte is accompanied by the full handshake procedure on the NRFD, DAV and NDAC control lines.

TABLE 4.20

Interface Output Message Format

Byte No	Interpretation	Permitted ASCII Characters
1	Sign of mantissa	+ or -
2	Most significant digit	0 to 9
3	Decimal point	.
4	Digit	0 to 9
5	Digit	0 to 9
6	Least significant digit	0 to 9
7	Exponent indicator	E
8	Sign of exponent	+ or -
9	More significant digit	0 to 9
10	Less significant digit	0 to 9
11	Carriage return	CR
12	Line Feed	LF

4.26 STATUS BYTE FORMAT

4.26.1 The data line usage for the status byte, generated in response to a serial poll, is given in Table 4.21.

TABLE 4.21

Status Byte

DIO Line	Function
1	Not used
2	Not used
3	Not used
4	Not used
5	'1' indicates that the instrument is busy
6	'1' indicates that an error has been detected
7	'1' indicates that service was requested
8	Not used

NOTE: The status byte does not provide information about the nature of any error which has been detected. The addressed command I4 can be used to have the error number loaded into the output buffer. This will then be transmitted via the bus when the instrument is addressed to talk.

4.27 SERVICE REQUEST (SRQ) OUTPUT

4.27.1 The instrument can be instructed via the bus to generate an SRQ output as follows:

(a) SRQ generation inhibited

(b) SRQ sent true when data are available

(c) SRQ sent true when an error is detected

(d) SRQ sent true when data are available or when an error is detected

The codes used are given in Table 4.14. Option (d) is adopted automatically on switching on.

4.27.2 When the 9303 is being used in the triggered mode a delay, equal to the value set in the AVERAGE store, will occur between the generation of the SRQ output and the appearance of the SRQ annunciator on the front panel.

4.28 LOGIC LEVELS

4.28.1 The control, handshake and data lines operate at standard +5 V TTL levels. Negative logic is used, i.e. logic '1' is represented by a level $\leqslant 0.8$ V and logic '0' by a level >2 V.

5.1 INTRODUCTION

5.1.1 This section is written in two parts. Paragraph 5.2 covers the operating principles of the 9303 in general terms, with reference to the block diagram, Fig. 5.1. Paragraph 5.3 describes the operation of the circuits in greater detail, with reference to the circuit diagrams given in Section 7. It is essential that the principles of operation are understood before the detailed circuit description is read.

5.1.2 In the circuit descriptions the integrated circuits are referred to by the circuit reference given on the appropriate circuit diagram. Note that a separate series of numbers, starting at IC1, is allocated to each assembly. Where an integrated circuit package contains more than one circuit, suffix letters are used to distinguish between them. Where it is necessary to identify a particular pin of an integrated circuit, the circuit reference, with suffix letter if appropriate, is followed by an oblique stroke and the required pin number.

5.2 PRINCIPLES OF OPERATION

5.2.1 FUNCTIONAL SYSTEMS

5.2.1.1 The instrument contains six functional systems. These are:

(a) A pseudo-random signal sampling system
(b) An analogue signal processing system
(c) A microprocessor system, which operates both as a digital signal processor and a control system
(d) A keyboard/display system
(e) A calibrator system
(f) An interface to the IEEE 488 GPIB

5.2.2 THE SAMPLING SYSTEM

5.2.2.1 The sampling system uses a diode sampling bridge to measure the voltage across the 50Ω μ-stripline conductor in the measuring head. The sampling period is approximately 300 ps, but the waveform of the sample taken is shaped to give a pulse which reaches its maximum value after approximately 1.5 μs. This pulse may be positive or negative going, according to the polarity of the measured signal at the instant of sampling.

5.2.2.2 To prevent the sampling frequency ever being an exact sub-multiple of the measured signal frequency, the sampling process is made pseudo-random by varying the sampling frequency over the range from 35 kHz to 70 kHz at a rate of 10 Hz. A 100 Hz signal, from a clock on assembly 19-1014, is divided by 10 and applied to an integrator in the timer and sweep generator on assembly 19-1015. This provides a 10 Hz triangular waveform, which is applied to the voltage-controlled oscillator (VCO) on assembly 19-1016. The variable frequency pulse waveform from this oscillator drives the sampling pulse generators, which are mounted within the measuring heads.

5.2.2.3 If zero signal is to be obtained from the sampling head when no measured signal is applied, the sampling bridge must be balanced symmetrically about 0 V. Once the bias voltages have been set to achieve this, balance is maintained automatically by the bias level control circuit on assembly 19-1016.

5.2.3 THE ANALOGUE PROCESSING SYSTEM

5.2.3.1 The analogue processing system measures the true r.m.s. value of the train of bipolar pulses fed to it from the sampling system. The measuring head to be used is selected by means of a multiplexer on assembly 19-1016. The pulses from the measuring head are applied to the high frequency sample and hold circuit during a gate period of approximately 1.5 ms. The gating signal is derived from the sampling pulse drive VCO, and its start is coincident with the sampling pulse. During the gate period the pulse from the measuring head reaches a peak value, and this value is held until the next gate period occurs.

5.2.3.2 The sample and hold circuit output therefore has a bipolar pulsed waveform. The amplitude of each pulse is proportional to the amplitude of the related sample taken from the measured signal, while the pulse frequency is the same as the sampling frequency. The output is clamped during the gate period to ensure that each voltage transition starts from the same level. The r.m.s. value of the output waveform is proportional to the r.m.s. value of the measured signal.

5.2.3.3 To permit measurements to be made over a wide range of input levels, while maintaining a restricted range of output levels from the sample and hold circuit, a switched gain amplifier is included in the analogue signal path on assembly 19-1016. The gain variation is obtained by means of electronically switched attenuators of 10dB, 20dB, 30dB and 30dB, which provide attenuations from 0dB to 90dB in 10dB steps. The insertion of the attenuators is controlled by the microprocessor system.

5.2.3.4 The alternating signal from the sample and hold circuit is fed to a true r.m.s. measuring circuit on assembly 19-1015. The measuring circuit is in the form of a feedback loop containing a differential multiplier, an integrator and an amplifier, and features an auto-zeroing system which cancels out the effects of noise and the multiplier input offsets.

5.2.3.5 The output of the analogue processing system is fed to the analogue-to-digital converter on assembly 19-1014 via a sample and hold circuit, which maintains a steady input to the converter during the auto-zeroing period of the r.m.s. detector.

5.2.4 THE MICROPROCESSOR SYSTEM

5.2.4.1 The microprocessor system is contained on assembly 19-1014. The system performs two separate functions:

(a) It converts the output of the voltage measuring circuits to digital form. The result is operated upon arithmetically to provide the measured value to be displayed.

(b) It provides signals to control the operation of the instrument in accordance with instructions entered by the operator.

5.2.4.2 The microprocessor is interrupt controlled, IRQs being generated every 100ms by the measured signal peripheral interface adaptor (PIA), at every operation of a key in the input/output system and for every data byte received by the GPIB interface.

5.2.4.3 Digital Signal Processing

5.2.4.3.1 The output of the r.m.s. detector is converted to digital form in the analogue-to-digital converter. In response to an IRQ from the measured signal PIA the output of the converter is scaled, according to the values held in the ACAL and FACTORY ECAL stores (and the USER ECAL and CAL FACTOR stores if these are enabled) and stored. A number of successive values, determined by the value held in the AVERAGE store, are then averaged. After noise cancellation the averaged value is processed, in accordance with the primary and computed measurement functions in use, to provide the value which is to be displayed. This value is used to set up a 96-bit serial data string, which is fed to the display on assembly 19-1013. The system also converts the value to be displayed into the nine data bytes of the GPIB output word. The exponent indicator byte and the CR and LF terminating bytes are incorporated to complete the output word, which is fed to assembly 19-1017 after the display has been updated.

5.2.4.4 Instrument Control

5.2.4.4.1 The majority of the instructions governing the operation of the instrument are internal to the microprocessor system, and govern such matters as the manner in which measurement data are processed, the selection of data to be displayed, the storage of data displayed or entered via the keyboard, range setting, error detection, etc. External control lines are limited to:

(a) Selection of the input to the switched gain amplifier
(b) Gain of the switched gain amplifier (attenuator switching)
(c) Calibrator system switching

In addition, the microprocessor system provides a 100 Hz output which provides the drive for the timer and sweep generator on assembly 19-1015.

5.2.5 THE KEYBOARD/DISPLAY SYSTEM

5.2.5.1 The keyboard/display system incorporates a custom built liquid crystal display (LCD). At display update the fresh data to be displayed, which may be the output of the digital signal processor, the contents of a store or an error code, is fed to assembly 19-1013 in the form of a 96-bit serial data string. This is fed into three 32-bit shift registers to convert it from serial to parallel form, the shift register outputs being latched until the next display update occurs. Each element of the LCD is controlled from a separate shift register output. The time taken to update the display is extremely short, and display blanking during updating is unnecessary. The 30Hz alternating supply for the LCD is obtained from an oscillator on assembly 19-1014.

5.2.5.2 The input section of the system is formed by a 7 x 4-line keyboard. This may be used to give instructions to the control system or to enter values into the stores used during the digital signal processing. Each key operation generates an IRQ, and is serviced individually by the microprocessor. The first of a series of numeric key operations puts the display to the numbers mode. In this mode the instrument continues to make measurements, but the display continues to show the numbers entered until the instrument is returned to the measurement mode.

5.2.6 THE CALIBRATOR SYSTEM

5.2.6.1 The calibrator system generates two independent outputs. One of these, driven by the sampling pulse drive VCO, provides pulses shaped to simulate the output of a measuring head. These are used to calibrate the measuring circuits in the analogue processing system during the automatic internal calibration (ACAL) sequence. The second output is a fixed frequency square wave having a true r.m.s. value of 223.6 mV in 50Ω. This output is available at the front and rear panel CALIBRATOR sockets, and may be used for the external calibration of the measuring heads (FACTORY ECAL) and for the measurement of the USER ECAL factors for use with measuring head attachments.

5.2.6.2 Both calibrator outputs are controlled automatically by the microprocessor during calibration sequences. In addition the use of the special functions permits operator control of the external calibrator output.

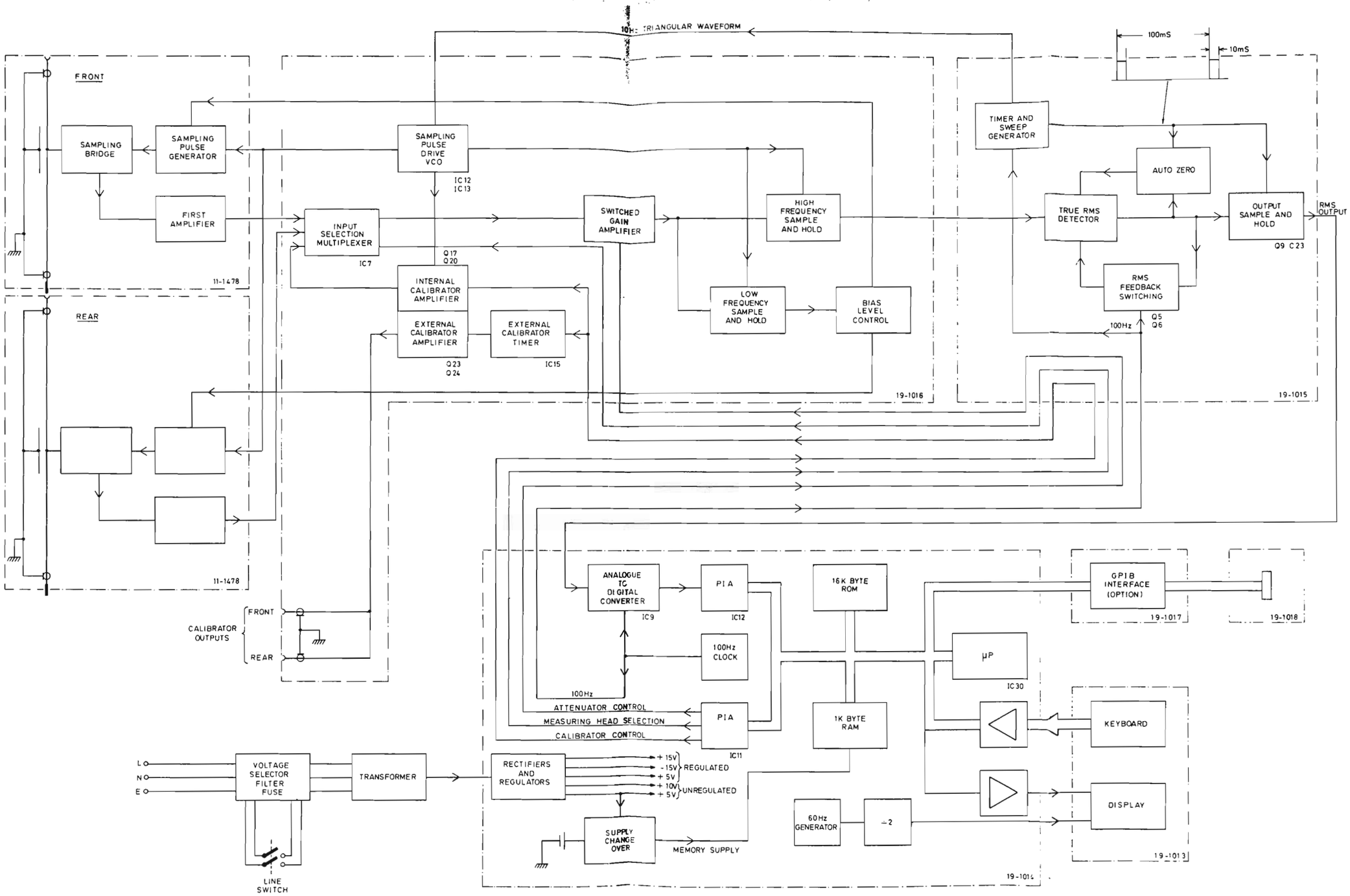
5.2.7 THE GPIB INTERFACE

5.2.7.1 The following functions are carried out by the GPIB interface without involvement of the microprocessor system.

(a) Distinguishing between universal and addressed commands occurring on the bus.
(b) Talk and listen address recognition.
(c) Generation of the signals required by the handshake protocol.

5.2.7.2 The interface passes device dependent data and certain universal bus commands between the bus and the microprocessor. An interrupt is generated for each of the following situations:

(a) A device dependent data byte is held in the data-in register for the microprocessor to read.
(b) The last device dependent data byte loaded into the data-out register has been read by the bus.
(c) DCL or SDC received.
(d) GET received.
(e) SPE or SPD received.
(f) Instruction to change remote/local status (RLC) received. This may be the REN message received false or the GTL command received when in the remote control mode, or REN and the listen address received when in the local control mode.



RACAL
TH3174

Fig. 5.1 Block Diagram

5.3 TECHNICAL DESCRIPTION

5.3.1 THE SAMPLING SYSTEM

5.3.1.1 The sampling system involves circuits mounted on five printed circuit boards. Three of these, assemblies 19-1014, 191-1015 and 19-1016 are mounted in the instrument. The other two, assemblies 19-1011 and 19-1012, are mounted in the measuring head. The circuit diagrams for these assemblies are given in Fig. 3, Fig. 7, Fig. 9 and Fig. 11 in Section 7 of this manual.

5.3.1.2 10 Hz Triangular Waveform Generation

5.3.1.2.1 The timing of the 10 Hz triangular waveform is controlled by the 100 Hz clock, IC3, on assembly 19-1014. The voltage at IC3c/9 is switched between a high and a low level by feedback via R5. The voltage at IC3c/8 ramps towards that at IC3c/9 as C15 charges or discharges via R8. Switching of the voltage level at IC3c/14 occurs each time the voltage at IC3c/8 passes through the level at IC3c/9.

5.3.1.2.2 The clock output passes off assembly 19-1014 at PL15 pin 19 and enters assembly 19-1015 at PL12 pin 19. Here the waveform passes via the driver, IC1d, and clocks the divide-by-ten circuit, IC2. The 10 Hz, unity mark/space ratio waveform occurring at IC2/12 is applied to the integrator, IC1a. The integrator output, which can be monitored at TP3, has a triangular waveform and a frequency of 10 Hz. The waveform leaves assembly 19-1015 at PL11 pin 16.

5.3.1.3 Voltage Controlled Oscillator

5.3.1.3.1 The triangular waveform generated on assembly 19-1015 enters assembly 19-1016 at PL4 pin 16, and is applied to the voltage controlled oscillator formed by IC12 and Q25. As the collector current of Q25 charges C46 the voltage at IC12/2 goes more positive, IC12 being triggered when this voltage equals the internally set trigger level. When this occurs C46 is discharged through IC12/7 and an internal current sink, so that the voltage at IC12/2 and 6 falls. When IC12/6 falls below an internally set threshold level IC12 is reset, disabling the current sink. C46 commences to charge, and the cycle is repeated.

5.3.1.3.2 The frequency of the oscillator depends upon the time taken for the voltage at IC12/2 to change from the threshold level to the trigger level, and therefore upon the collector current of Q25. This is controlled by the 10 Hz triangular waveform, so that the output of IC12 is frequency modulated at 10 Hz. The limits of the frequency sweep are approximately 35 kHz and 70 kHz.

5.3.1.3.3 The variable frequency output from IC12/3 clocks a monostable circuit, IC13b, which provides pulses of controlled length at IC13b/12 and 5. The nominal pulse duration is 1.5 µs, and is set by adjustment of R99.

5.3.1.4 Sampling Pulse Generation

5.3.1.4.1 The positive going pulses from IC13b/5 pass to the front or rear INPUT socket, via the gate formed by IC14 a, b, c and d, and so to the measuring head in use. The gate directs the pulses according to the logic levels present at IC14c/5 and IC14a/1. These levels are set on the measuring head selection lines by the microprocessor system. A logic '0' on the control line disables the related drive pulse output.

5.3.1.4.2 The measuring head contains assemblies 19-1011 and 19-1012. In the quiescent state Q3, Q2 and Q1 on assembly 19-1012 do not conduct. Current flows from the +15 V rail through L1, R2 and R1 on assembly 19-1012 and then through the step-recovery diode D5 and L1 on assembly 19-1011. Charge storage occurs in the diode.

5.3.1.4.3 When a positive going pulse occurs at pin 1 of board 19-1012, Q3, Q2 and Q1 all conduct. The voltage at Q1 drain falls, so that the step-recovery diode is reverse biased, and a high reverse current flows in D5, L1 and R1 until the charge stored in D5 is reduced to zero. At this point the diode cuts off rapidly, and the energy stored in L1 gives a pulse in the circuit consisting of L1, C3, T2, T1, the sampling bridge, T1, T2 and C2. The amplitude of this pulse is determined in part by the value of the reverse current which occurs when D5 is reverse biased, since this determines the energy stored in L1. The value of this reverse current depends on the value of R1.

5.3.1.4.4 Transformers T1 and T2 ensure that the current pulse gives symmetrical, antiphase voltage pulses, positive at the D2/D4 junction, across the sampling bridge. The voltage across the bridge is sufficient to overcome the reverse bias applied via pins 3 and 4 of assembly 19-1011, so that the bridge is forward biased for the duration of the sampling pulse.

5.3.1.5 Sampling Bridge Operation

5.3.1.5.1 The µ-stripline carrying the signal to be measured is connected to the sampling bridge by C1 and R1. High frequency boost is provided by C10. While the bridge is reverse biased the D1/D2 junction is isolated from the D3/D4 junction, but, when the bridge is forward biased by the sampling pulse, any voltage applied at the D1/D2 junction unbalances the bridge. A voltage approximately equal to the measured signal value appears at the D3/D4 junction, charging C11.

5.3.1.6 Pulse Amplification

5.3.1.6.1 During the 300 ps sampling period C11 charges rapidly through the low impedance of the input circuit and the bridge. At the end of the sampling period it discharges through R6 and R5, with a time constant of approximately 1.5 µs. The input to the amplifier containing Q1 and Q2 is therefore a pulse, which may be of either polarity, having a sharp leading edge followed by an exponential return to 0 V lasting some 7.5 µs. This is buffered by the unity gain stage containing Q1 and Q2, and fed via pin 5 of assembly 19-1011 to R18 on assembly 19-1012.

5.3.1.6.2 Adjustment of R18 controls the final amplitude of the measuring head output pulse, permitting it to be set to a value for which the FACTORY ECAL factor will be within the permitted range. The output pulse is fed via the measuring head cable to the analogue signal processing system.

5.3.1.7 Bias Control Circuit

5.3.1.7.1 The sampling bridge is biased such that the diodes are non-conducting, except during the presence of the sampling pulse. The bias level must maintain the bridge balanced symmetrically, about 0 V. If this is not so, excessive sampling pulse breakthrough may occur. This can overload the analogue processing system, particularly in the lower ranges.

5.3.1.7.2 The bias voltages are taken from the resistor chain R13, R11, R12 and R14 on assembly 19-1012. The voltage across this chain is maintained at 20.4 V by diodes D2, D3, D4 and D5. The total bias across the bridge may be set by adjustment of R11, while the bias balanced is set by the voltage applied, through the measuring head cable, to pin 5. This voltage is derived in the second sampler circuit of the analogue signal processing system, on assembly 19-1016.

5.3.2 ANALOGUE SIGNAL PROCESSING SYSTEM

5.3.2.1 The analogue signal processing system circuits are carried on two printed circuit boards, assemblies 19-1016 and 19-1015. The circuit diagrams are given in Fig. 9 and Fig. 11 in Section 7 of this manual.

5.3.2.2 Input Multiplexer

5.3.2.2.1 The signal which is to be processed is selected by the input multiplexer, IC7, on assembly 19-1016. The operation of the multiplexer is controlled by the logic levels on the front and rear measuring head selection control lines, which are set by the microprocessor system. The pulse waveforms from the measuring heads enter the board at the coaxial sockets SK9 and SK10. A waveform, simulating the output of a measuring head, and having an amplitude of 1 V peak-to-peak, is fed to IC7/5 from the calibrator system. Only one of these signals will be present at any one time, since sampling pulse drive signals are only fed to the measuring head selected for use, and both measuring heads are disabled while the internal calibrator is enabled during an ACAL sequence.

5.3.2.3 Switched Gain Amplifier

5.3.2.3.1 The selected signal at IC7/14 is passed, via the buffer stage containing Q1 and Q2, to the 30 dB attenuator comprising R4, R5, R6 and R7. The multiplexer IC6 selects either the full output of the buffer stage, from the junction of C43 and R4, or the attenuated signal, from the junction of R5 and R6, as the input to the amplifier containing Q3, Q4 and Q5. The mulitplexer is controlled by the logic level on a 30 dB attenuator control line, which is set by the microprocessor system. The attenuator is in circuit when the line is at logic '0'. Adjustment of R4 permits accurate setting of the attenuator.

5.3.2.3.2 Three further attenuator/amplifier stages, incorporating attenuators of 30 dB, 20 dB and 10 dB, follow the one described. Although the four stages operate in a similar manner they differ in the following respects:

(a) The amplifier Q3/Q4/Q5 incorporates filtering circuits C2/R12 and C3/R15. These shape the amplifier reponse such that, while it is still able to respond efficiently to the sharp leading edge of the input pulse, the output pulse takes approximately 1.5 µs to reach its peak value and has an almost flat top.

(b) The amplifiers Q9/Q10/Q11 and Q12/Q13/14 incorporate catching diodes D8 and D9 to prevent saturation. These are necessary because, should the amplifier saturate, the output signal would be nearly constant. Since AC coupling is used the signal into the next stage would be small, and the auto-ranging system could down range. This would drive the amplifier further into saturation.

(c) Two 10 dB attenuators are provided before the final amplifier stage. One of these, formed by R118, R119, R120 and R117, is inserted in the signal path only when the lowest, 316 µV, measurement range is in use.

5.3.2.3.3 The gain of each amplifier stage is nominally 20 dB. When the 1 V measurement range is in use, the gain between TP7 and TP3 is approximately unity.

5.3.2.4 Second Sampler

5.3.2.4.1 The second sampler comprises two sample and hold circuits, fed from the output of the switched gain amplifier. One converts the bipolar pulsed output of the amplifier to an AC signal suitable for driving the r.m.s. measuring circuit, while the other provides the control voltage for the measuring head bias balance.

5.3.2.4.2 The signal for the r.m.s. measuring circuits is provided by the sample and hold circuit fed via C28. The transmission gate in IC2a is held in the conducting state by a 1.5 µs pulse fed, via Q15, from IC13b/12. During this period C19 charges. When IC2a returns to the non-conducting state the voltage on C19 is held, due to the high input impedance of IC1a.

5.3.2.4.3 The pulse used to drive IC2a is taken from the VCO which generates the measuring head sampling pulse drive, so that its leading edge is coincident with the sampling pulse. The output of the switched gain amplifier reaches its peak 1.5 µs after the sampling of the measured waveform, so that it is this peak value which is held on C19. This value is proportional to the instantaneous value of the measured signal at the instant it is sampled by the measuring head.

5.3.2.4.4 The outpt of the circuit is taken via the voltage follower, IC1a, a high pass filter, C64, R123, and a second voltage follower IC1b. While C19 is being charged the junction of R46 and R47 is held at 0 V by the transmission gate in IC2b. This ensures that the voltage steps fed out to the r.m.s. measuring circuit at the beginning of each hold period all start from the same level.

5.3.2.4.5 Idealised waveforms for the sampling and signal processing systems are given in Fig. 5.2

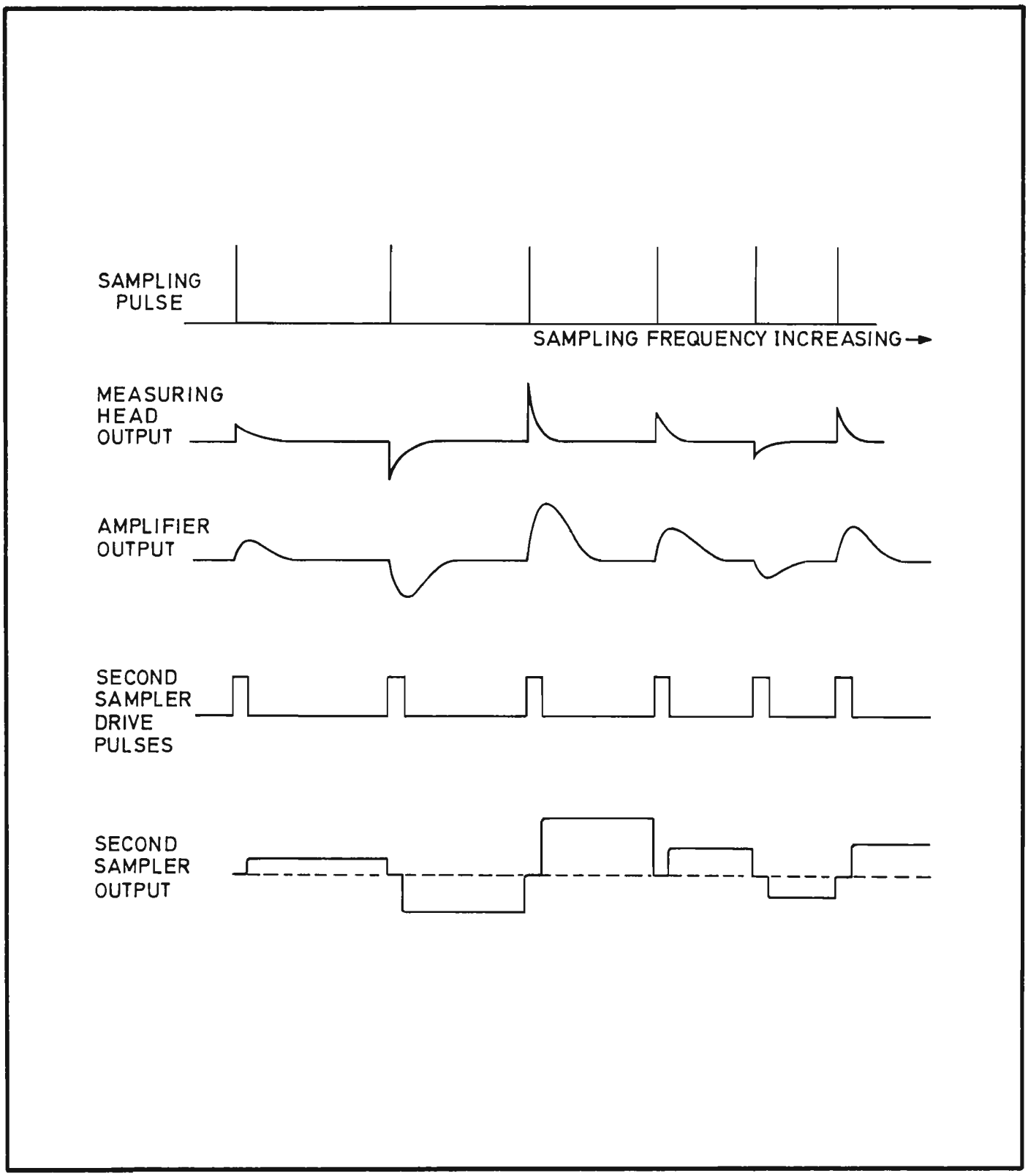


Fig. 5.2 Idealised Waveforms:
Sampling and Signal Processing

5.3.2.4.6 If the measuring head bias is not balanced about 0 V, an offset will be added to each sample of the measured signal fed from the measuring head. This will give an offset to the mean level of the input to the second sampler.

5.3.2.4.7 A second sample and hold circuit is fed from the amplifier output via C18. This operates in a similar manner to the circuit previously described. However, it is fed via a circuit of comparatively long time constant, and it does not contain a high pass filter between IC1c and R49 similar to that between IC1a and R46. The output consists of pulses, at the sampling rate, whose mean value is proportional to the mean level of the amplifier output.

5.3.2.4.8 The output from IC1d/8 is fed to the differential input integrator, IC8a. The integrator output is fed, via the voltage follower, IC8b, to the measuring head, where it is used to control the balance of the sampling bridge bias. If a voltage difference exists between IC8a/5 and IC8a/6 a voltage ramp occurs at IC8a/7. The sampling head bias balance will be changed, and this will result in a variation in the mean level of the signal applied to the second sampler. This, in turn, will give a voltage change at IC1d, reducing the voltage difference at the inputs to IC8a. When this difference is reduced to zero the voltage ramp at IC8a ceases. The operating point of the loop can be adjusted by means of R68.

5.3.2.5 True RMS Detector

5.3.2.5.1 The output from IC1b/14, in the sample and hold circuit, forms the input to the true r.m.s. detector on assembly 19-1015. The detector is in the form of a feedback loop containing a multiplier and an integrator. The principle of operation, ignoring the effects of noise and the multiplier input offsets, is given in Fig. 5.3.

5.3.2.5.2 The signal enters the assembly at PL11 pin 4, passing via the gate, Q1, and the voltage follower, IC3, to the inputs to the multiplier IC6/6 and 9. The gate Q1 conducts, except during a period of 10 ms in every 100 ms when the loop auto-zeroing system is operating.

5.3.2.5.3 The multiplier is of the linearised transconductance type, a schematic circuit diagram being given in Fig. 5.4. The operation of the multiplier is covered in Appendix 2 to this section.

The inputs to the multiplier are $(V_S + V_R)$ and $(V_S - V_R)$

The multiplier output is therefore $(V_S + V_R)(V_S - V_R)$

$$= (V_S^2 - V_R^2)$$

The integrator output is the mean value of the multiplier output

$$= \overline{(V_S^2 - V_R^2)}$$

The amplifier output is therefore $A\overline{(V_S^2 - V_R^2)}$

But the amplifier output is V_R, so $\frac{V_R}{A} = \overline{(V_S^2 - V_R^2)}$

If the amplifier gain is large $\frac{V_R}{A}$ approximates to zero, so that

$$\overline{V_S^2} = \overline{V_R^2}$$

Since V_R is a direct voltage $\overline{V_R^2} = V_R^2$, and

$V_R = \sqrt{\overline{V_S^2}}$, the r.m.s. value of V_S.

A more complete analysis of the loop operation, taking account of noise and multiplier input offsets is given in Appendix 1 to this section.

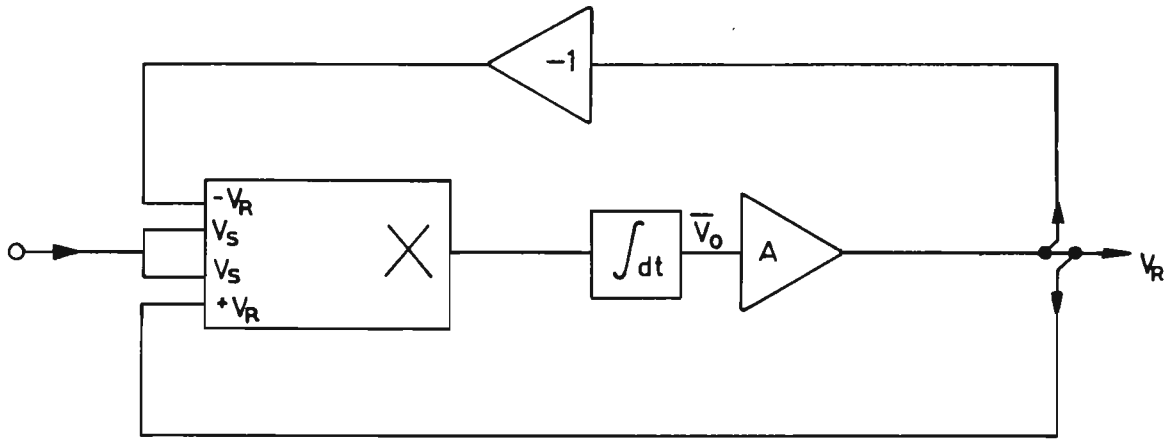


Fig. 5.3 Feedback Loop Operation

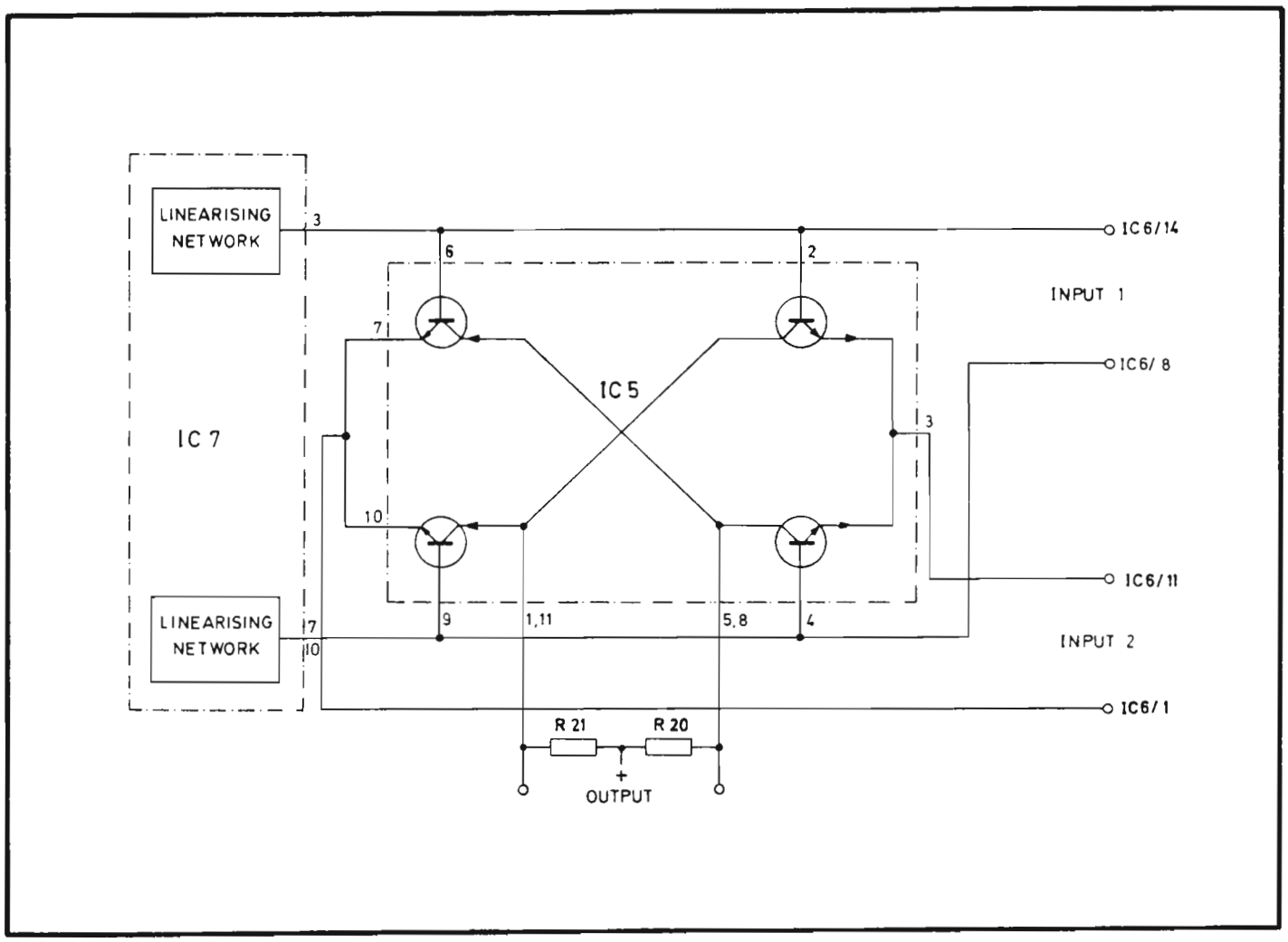


Fig. 5.4 Multiplier

5.3.2.5.4 The transistors of the multiplier are contained in IC5. The use of the transistor array, rather than discrete components, affords close matching of the transistor characteristics. IC5 is specially selected to obtain the degree of matching required. The multiplier linearising networks are formed by the transistors in IC7. This array is also specially selected to obtain the required degree of matching. The base/emitter diodes of these transistors form the loads for the input currents from IC6 pins 8 and 14. They provide an exponential relationship between the input currents and the voltages applied at IC5 pins 4, 9, 2 and 6, which offsets similar non-linearities in the transistors of IC5.

5.3.2.5.5 The multiplier inputs are driven by the transistors in IC6, which are connected, with two of the transistors from IC5 and IC7, to form two long-tailed-pair differential amplifiers. Good matching of these transistors is essential, and IC6 is specially selected to achieve this. When measuring signals of high crest factor the differential signal at the amplifier inputs becomes large, and the transistors may be driven close to cut off at the signal peaks. This results in non-linearity. The effect is overcome by means of D4 and D5, which conduct when the differential signal is large, reducing the emitter coupling resistor value and increasing the amplifier gain.

5.3.2.5.6 The differential output from the multiplier is fed to IC4d. Except during the auto-zeroing period Q3 and Q4 are held in the conducting state, while Q10 and Q8 are in the high impedance state. Feedback is therefore applied to IC4d via C20, and the circuit acts as an integrating amplifier. The voltage at TP6 is proportional to the mean level of the multiplier output, and to the true r.m.s. value of the measured signal.

5.3.2.5.7 The output of IC4d is fed back to the input of the multiplier at IC6/2 and IC6/12. The feedback circuit is shown in Fig. 5.5.

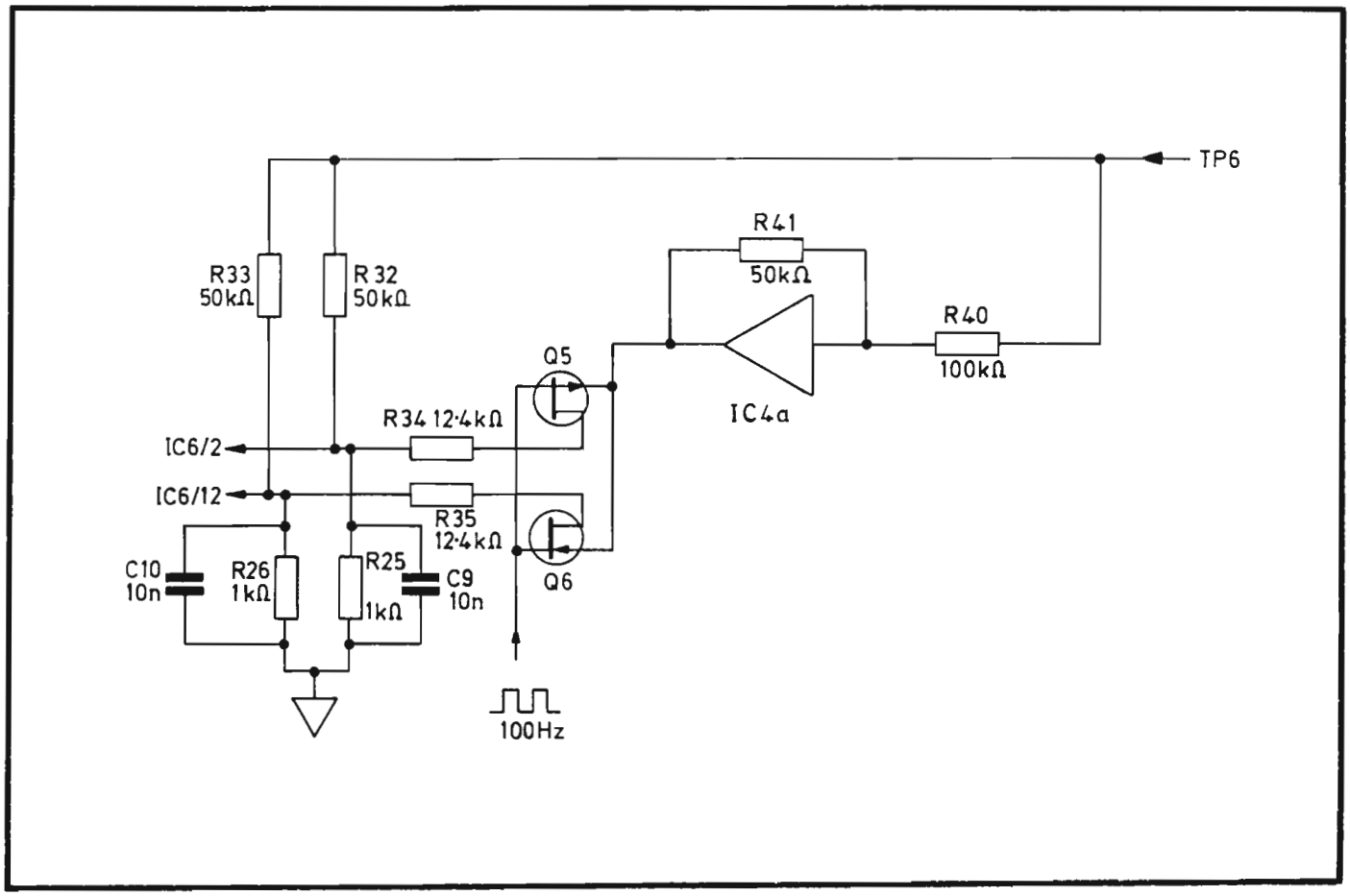


Fig. 5.5 Feedback Switching

5.3.2.5.8 The feedback from TP6 to IC6/2 and IC6/12 is in two parts:

(a) A positive voltage, fed to both IC6/2 and IC6/12 via R32 and R33.

(b) A negative voltage fed via IC4a, Q5/Q6 and R34/R35. This is fed to IC6/2 or IC6/12, according to whether Q5 or Q6 is conducting, and is switched between these inputs at 100 Hz.

5.3.2.5.9 The gain of IC4a is set by R40 and R41 to 0.5, and the resistance ratios R35/R33 and R34/R32 are 0.25. The negative signal is therefore twice the positive signal, and IC6/2 and IC6/12 receive signals of equal amplitude but opposite sign. The switching transistors are driven from the 100 Hz clock in the microprocessor system via IC1d.

5.3.2.6 Output Sample and Hold

5.3.2.6.1 The voltage at TP6 is proportional to the true r.m.s. value of the measured signal. Except during the auto-zeroing period Q9 is in the low impedance state, and C23 charges to this value. The voltage is fed to the digital signal processing system via the voltage follower, IC4b. During the auto-zeroing period Q9 is put to the high impedance state and the output voltage is maintained at the level held on C23.

5.3.2.7 Auto-Zeroing

5.3.2.7.1 Every 100 ms an auto-zeroing cycle, lasting 10 ms, is performed. During this period the measured signal input is reduced to zero, and the residual signal at the output of IC4d is used to generate a correction voltage, which is stored. During the 90 ms measurement period which follows, this voltage is injected into the feedback loop of the r.m.s. detector, cancelling the zero error.

5.3.2.7.2 The timing of the auto-zeroing system is controlled by the waveform from IC2/3 in the timing and sweep generator circuit. This waveform, derived from the 100 Hz clock on assembly 19-1014, consists of 10 ms positive-going pulses occurring at 10 Hz, and is applied to the comparators, IC1b and IC1c.

5.3.2.7.3 The edges of the pulses are slowed down by the low-pass filter, R37/C17. A resistor chain, formed by elements of R36 and R37, holds IC1b/6 more positive than IC1c/10, so the comparators are not triggered simultaneously. Idealised waveforms are shown in Fig. 5.6.

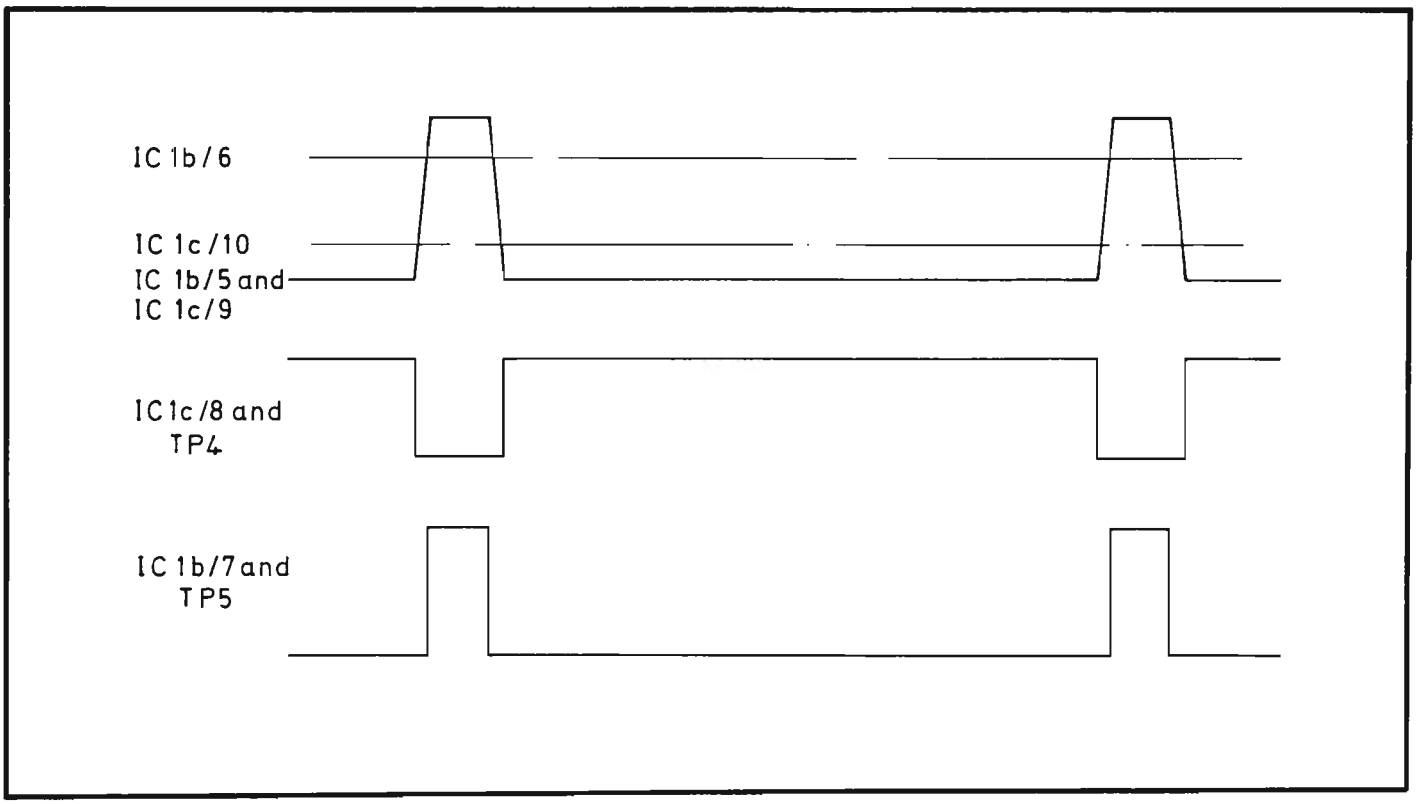


Fig. 5.6 Comparator Waveforms

5.3.2.7.4 At the commencement of the auto-zeroing period the following actions are performed by the pulses from IC1b and IC1b:

(a) The negative-going pulse from IC1c puts Q1 to the high impedance state, isolating the r.m.s. detector loop input.

(b) Q9 is put to the high impedance state, isolating the loop output.

(c) Q3 and Q4 are put to the high impedance state, preventing feedback around IC4d via C20.

(d) Q10 is put to the low impedance state, allowing feedback around IC4d via C25.

(e) Q8 is put to the low impedance state. This connects the residual loop output, which exists at IC4d/14 when the loop input is open circuited, to the integrator, IC4c. The output of IC4c is applied to IC4d/12, providing an input which drives the output of IC4d to 0 V.

5.3.2.7.5 At the end of the auto-zeroing period the circuit is reset to the measurement mode. The input of IC4c is disconnected from the signal path, as Q8 reverts to the high impedance state, but the zero error correction voltage at TP15, stored in C18, remains connected to the input of IC4d. This provides zero correction during the following measurement period.

5.3.2.8 Prevention of Lock Up

5.3.2.8.1 When the instrument is operated with no input signal, there may be a tendency for the output of the loop to drift negative. If such an output is fed back to the multiplier the effect is cumulative, and the loop locks up with the output driven negative. This is prevented by D10, which becomes reverse biased if the voltage at TP6 is negative, so open circuiting the feedback path.

5.3.3 THE MICROPROCESSOR SYSTEM

5.3.3.1 The microprocessor system is carried on assembly 19-1014. The circuit diagram is given in Fig. 7 in Section 7 of this manual.

5.3.3.2 The system acts as a digital signal processing system and as the instrument control system. The digital signal processing function includes the following:

(a) Conversion of the true r.m.s. detector output to digital form, and reading the digitised measurement.

(b) Scaling the measurement according to the values held in the ACAL and FACTORY ECAL stores (and the USER ECAL and CAL FACTOR stores if these are enabled).

(c) Averaging a number of measurements according to the value in the AVERAGE store.

(d) Noise cancellation, according to the noise level measured during the FACTORY ECAL and USER ECAL sequences.

(e) Arithmetic processing in accordance with the primary and computed measurement functions set by the control system.

(f) Conversion of the processed data into a serial data string for the display.

(g) Conversion of the processed data into the 12-byte data word to be fed to the GPIB interface.

(h) Transmission of the serial data string to the display, accompanied by the clock pulses for the output system shift registers.

(j) Transmission of the 12-byte data word to the GPIB interface.

5.3.3.3 The instrument control function includes the following:

(a) Acceptance of control instructions from the keyboard or the GPIB interface.

(b) Acceptance and storage of numerical data from the keyboard or the GPIB interface.

(c) Setting the attenuator control line logic levels.

(d) Setting the measuring head control line logic levels.

(e) Enabling and disabling the calibrator system, and directing the measurements made during calibration cycles to the appropriate stores.

5.3.3.4 Analogue to Digital Conversion

5.3.3.4.1 The analogue signal from the true r.m.s. detector enters assembly 19-1014 at PL15 pin 16. It passes via a bilateral switch in IC8 to the input of the analogue-to-digital converter, IC9. The output of the converter is in the form of $3\frac{1}{2}$ digits in BCD on 13 lines, and is fed to the Peripheral Interface Adaptor (PIA), IC12, at pins 2 to 14. Additional signals are fed to IC12/16, 17 and 18 to indicate that the conversion cycle has been completed, and to IC12/15 to indicate that the output data from IC9 is valid.

5.3.3.4.2 A 100 Hz clock signal for IC9 is taken from an astable circuit at IC3/14, and used to drive a monostable circuit, IC14b. The output pulses at IC14/5 have a duration controlled by R9 and C7.

5.3.3.4.3 The positive and negative supply voltages for IC9 are derived from the +15 V and -15 V supply rails across D15 and D14. The current reference to IC9/13 can be adjusted, by means of R15, to set the full scale gain of the converter.

5.3.3.5 Digital Data Input

5.3.3.5.1 The digital data output from IC9 is fed to the data-in registers of the PIA, IC12. At the end of each analogue-to-digital conversion cycle of IC9, IC12/18 is put to logic '0'. This results in the generation of an $\overline{IRQ}$ signal at IC12/37. The microprocessor enters its interrupt routine, during which it establishes that IC12 was the source of the interrupt, and then reads the data from the PIA.

5.3.3.6 Digital Data Processing

5.3.3.6.1 The digital data processing operations given in sub-paragraphs 5.3.3.2(b) to (j) are carried out by the microprocessor in accordance with the instructions in the system software, where necessary using numeric values held in memory. A description of the software is considered unnecessary for the purposes for which this manual is intended.

5.3.3.7 Serial Data Output to the Display

5.3.3.7.1 Once the value to be displayed has been determined it is used, together with data regarding the non-numeric items to be displayed, to set up the 96-bit data string used to update the display. This data string is fed to the keyboard/display system on the microprocessor data line D0, via IC36a to d and IC33c.

5.3.3.7.2 A series of 96 clock pulses is sent in synchronism with the data string, 32 pulses being directed to each of the display clock lines in turn. The clock pulses are directed to the required lines by IC32, according to the levels set on IC32/1, 2 and 3 by the address lines A0, A1 and A2. The enablement of IC32 is controlled by the chip select circuit, which sets the logic level at IC32/4.

5.3.3.8 Parallel Data Output to the GPIB Interface

5.3.3.8.1 After the display has been updated, the measured value is converted to the format required for the GPIB interface output message. The first byte is passed to the data-out register of the General Purpose Interface Adaptor (GPIA) chip on assembly 19-1017.

5.3.3.8.2 When the first data byte has been read from the data-out register to the bus the GPIA chip generates an interrupt request. The microprocessor then transfers a further byte. This process is repeated until the final byte has been transferred.

5.3.3.9 Data Input from the GPIB Interface

5.3.3.9.1 The data input from the GPIB interface also takes place byte by byte under interrupt control. When a byte has been written into the data-in register of the GPIA chip from the bus, an interrupt request will be generated. The microprocessor interrupt routine will establish the reason for the interrupt, and the data will be transferred to the microprocessor.

5.3.3.9.2 When the first byte has been read by the microprocessor, the GPIA chip is able to accept a further byte from the bus. When this has been written into the data-in register a further interrupt request is generated. The process is repeated until no further data are available.

5.3.3.10 Data Input from the Keyboard

5.3.3.10.1 Each operation of a key generates an interrupt request. The microprocessor interrupt routine will establish the keyboard as being the source of the interrupt, and the keyboard servicing routine which follows will detect which key has been operated. A data byte, determined by the key operated, is stored, and the $\overline{IRQ}$ control line is reset.

5.3.3.10.2 The LED indicators associated with the control keys are operated immediately the data input occurs, and the digits associated with a numerical data input are displayed as the bytes are stored. In other respects the processing of a multi-byte input does not commence until a valid terminating byte is recognised.

5.3.3.10.3 The generation of the $\overline{IRQ}$ signal is performed by IC27 and IC31a. The key row lines are normally held at logic '0' by IC37 a, b, c and d, while the column lines are pulled to logic '1' by the resistors in R30. The operation of a key pulls one of the column lines to logic '0' and puts IC27/8 to logic '1', clocking IC31a/6 to logic '0'. This output, buffered by IC33d, forms the $\overline{IRQ}$ signal.

5.3.3.10.4 The keyboard servicing routine commences with IC28/1 and 19 being put to logic '0', and IC37/2, 5, 9 and 12 being put to logic '1', by the chip select circuit. Both devices are then in the enabled state. The microprocessor address lines A0, A1, A2 and A3 are first put to logic '1', and then used to set each keyboard row line to logic '0' in turn via IC37 a, b, c and d. When the row line associated with the key which has been operated is put to logic '0', the column line for that switch will also be put to logic '0'. The corresponding output of IC28 will go to logic '1', providing a data byte on the bus which, considered in conjunction with the logic levels on address lines A0, A1, A2 and A3 is unique to the operated key. This byte is transferred into the microprocessor.

5.3.3.10.5 When the byte from the keyboard has been loaded, IC31a is cleared by a logic '0' level applied to IC31a/1 from the chip select circuit. This clears the interrupt request.

5.3.3.11 Attenuator, Measuring Head and Calibrator Control

5.3.3.11.1 The logic levels on the control lines for the attenuators of the variable gain amplifier, measuring head selection and the calibrator are set by transferring data into the data-out register of the control PIA, IC11.

5.3.3.11.2 The control lines are driven from the peripheral data bus ports of IC11. The levels remain set when IC11 is deselected at the completion of the data transfer. The outputs from IC11 are buffered in IC4, IC5 and IC6.

5.3.3.12 The Chip Select Circuit

5.3.3.12.1 The logic levels for chip selection within the system are generated in a circuit containing IC25, IC26 and IC34. The valid memory address (VMA) line from IC30/5 is used to enable IC25 whenever chip selection is required.

5.3.3.12.2 The ROM enabling signals (logic '0' level) are obtained directly from IC25/7, 9, 10 or 11, according to the logic levels applied to IC25/1, 2 and 3 by the microprocessor via address lines A12, A13 and A14. For all other chip enabling signals these address lines are set to give a logic '0' at IC25/15, which is used to enable IC26.

5.3.3.12.3 When enabled, IC26 generates one of the following outputs, according to the logic levels set on address lines A10, A9 and A8 by the microprocessor.

(a) The RAM selection signal (M)

(b) The keyboard servicing enablement for IC28 and IC37.

(c) The display clock enablement ($\overline{OPE}$) for IC32

(d) The enablement for IC22 or IC29

(e) The enablement for IC34.

5.3.3.12.4 When enabled IC34 generates the enabling signal for the PIAs IC11 and IC12, or for the GPIA chip in the GPIB interface, ($\overline{GCS}$), according to the logic levels set on address lines A6, A5 and A4 by the microprocessor.

5.3.3.13 Reset and Memory Supply Changeover Circuit

5.3.3.13.1 When the power supply to the instrument is off IC43, IC44, IC45, IC42 and IC15 are powered from the battery, B1. The voltage level detectors IC44 and IC45 detect the low voltage on the +5 V supply rail, and both IC45/6 and IC44/5 are at logic '0'. As a result IC42a/3 and IC42d/13 are at logic '1'. The bistable circuit formed by IC15b and IC15c will have been reset when the instrument supply was switched off, leaving IC15c/8 at logic '1'. Both inputs to IC42d are therefore at logic '1', and IC42d/11 ($\overline{RESET}$) is held at logic '0'. The logic '1' at IC15c/8 also holds the R/$\overline{W}$ line in the read condition and the RAM select line at logic '1', via IC43b and IC43c, so preventing access to the memory.

5.3.3.13.2 When power is applied the potential on the +5 V rail increases until IC45/6 and IC44/5 go to logic '1', and IC42a/3 goes to logic '0'. As a result IC42d/11 goes to logic '1', releasing the microprocessor from reset, while IC42c/10 goes to logic '1'. As part of its start-up procedure the microprocessor sets a logic '1' at IC11/19, and, therefore, at IC42c/9. The bistable circuit, IC15b and IC15c, is put to the set state, with IC15c/8 at logic '0', releasing the R/$\overline{W}$ and $\overline{CS}$ lines.

5.3.3.13.3 When power to the instrument is switched off or fails the reduction in the voltage on the +5 V supply rail is sensed by IC44, and IC44/6 goes to logic '1'. Since IC15d/12 is already held at logic '1' by IC15b, IC15d/11 goes to logic '0', providing a non-maskable interrupt ($\overline{NMI}$) at IC30/6. At the completion of the current instruction the microprocessor enters its non-maskable interrupt routine. As part of this routine a logic '0' is set at IC11/39, and applied to IC15c/9. This puts the bistable circuit formed by IC15b and IC15c to the reset state, with IC15c/8 at logic '1'. The R/$\overline{W}$ line is held in the read state and the RAM select line is held at logic '1' via IC43b and IC43c, so preventing corruption of the memory contents with spurious data which may be generated during the power fade period.

5.3.3.14 Test Switchbank S30

5.3.3.14.1 The switchbank S30 is used to set a pattern onto the data bus for test purposes, and to indicate to the microprocessor that the GPIB interface is fitted. In normal operation switches 1 to 7 must be set to the open position (where the slider is furthest from the switch section number). Switch 8 must be closed.

5.3.4 THE KEYBOARD/DISPLAY SYSTEM

5.3.4.1 The system comprises a 7 x 4 - line keyboard, a liquid crystal display (LCD) and a number of light emitting diode (LED) indicators. Although the LED indicators are related to particular keys, all connection between the keyboard and the display is via the microprocessor system.

5.3.4.2 A 30 Hz switching waveform for the LCD is generated by IC3d and IC31b on assembly 19-1014. The remainder of the system is mounted on assembly 19-1013. The circuit diagrams are given in Fig. 5 and Fig. 7 in Section 7 of this manual.

5.3.4.3 The Keyboard

5.3.4.3.1 The keyboard switches are of the mechanical, push-operated type. When the microprocessor is not servicing the keyboard all four row lines, entering assembly 19-1013 at pins 7, 8, 11 and 12, are held at logic '0', while the seven column lines, entering the assembly at pins 13 to 19, are held at logic '1'.

5.3.4.3.2 Closure of any switch will result in the corresponding column line being pulled to logic '0'. This action generates a IRQ for the microprocessor, which will then service the keyboard. The generation of the IRQ and the keyboard servicing procedure are described in the description of the microprocessor system.

5.3.4.4 The Liquid Crystal Display

5.3.4.4.1 The LCD is a custom built device having 79 segments. The information to be displayed is fed from the microprocessor in the form of a 96-bit data string. This enters assembly 19-1013 at pin 22, and is applied to the data input pins of the shift registers, IC1, IC2 and IC3, in parallel. The clock lines for the shift registers enter the assembly at pins 20, 21 and 10. The waveforms on these lines are controlled by the microprocessor system such that 32 bits of the data string are clocked into each register.

5.3.4.4.2 All the shift register outputs are switched between logic '0' and logic '1' at 30 Hz by the TRUE/COMPLETMENT signal applied to each register at pin 1. Shift register outputs loaded with logic '0' from the 96-bit data string change level in phase with the signal at pin 1, while those loaded with logic '1' are in antiphase.

5.3.4.4.3 The back plane of the LCD is driven from IC2/36 via R1, while the display segments are driven from the remaining shift register outputs. Those segments driven in antiphase to IC2/36 will darken.

5.3.4.5 The LED Indicators

5.3.4.5.1 With the exception of the LINE indicator LP1, which lights whenever the +5 V supply is available, the LED indicators are controlled by the shift registers, IC4, IC5 and IC6. An indicator will light when the associated shift register output is held at logic '0'.

5.3.4.5.2 When a change in the indicator pattern is required suitable data strings are generated in the microprocessor system. These enter the assembly at pin 4, and are applied to the data inputs of the three registers in parallel. The clock lines of the shift registers enter the assembly at pins 3, 5, and 6, and carry waveforms, generated in the microprocesor system, which clock the data into the appropriate register.

5.3.5 THE CALIBRATOR SYSTEM

5.3.5.1 The system is carried on assembly 19-1016. It contains two independent calibration sources. These are:

(a) The internal calibration source, which is used during the automatic internal calibration sequence (ACAL).

(b) The external calibration source, which provides the signal at the front and rear panel CALIBRATOR sockets used during the measurement of FACTORY ECAL and USER ECAL factors.

The circuit diagram is given in Fig. 11 in Section 7 of this manual.

5.3.5.2 The Internal Calibrator

5.3.5.2.1 The signal provided by the internal calibrator simulates the output of a measuring head. The output waveform consists of bipolar pulses, shaped to match the output of a measuring head, and having an amplitude of 1 V peak-to-peak. The pulse frequency is derived from the sampling system VCO, and so varies between 35 kHz and 70 kHz at a 10 Hz rate. Each output pulse is coincident with the leading edge of one of the 1.5 µs drive pulses to the second sampler.

5.3.5.2.2 The trigger pulses for the calibrator are taken from the VCO at IC13b/5, and clock a divide-by-two counter in IC16. The counter output, at IC16/5, is therefore at half the VCO frequency, and has a unity mark/space ratio. When the calibrator is not in use this output is disabled by a logic '0' at IC16/4, which holds IC16a in the set state. This logic level is set by the microprocessor system via the INT CAL SELECT control line.

5.3.5.2.3 The transistors Q17, Q18, Q19 and Q20, with IC17a, form a controlled gain DC amplifier. When the output at IC16/5 is disabled (logic '1') Q17 is switched off, and current flows in Q18, Q20 and R77. When the output from IC16/5 is enabled, Q17 is switched between the on and off states. This in turn, switches Q20 on and off, giving current pulses in R77.

5.3.5.2.4 The current in R77 is stabilised by feedback via R80 to the integrator, IC17a. The output at IC17a/1 varies according to the mean level of the feedback pulses, and controls the current in Q19 and Q18. The mean level at which the current stabilises is set by means of a voltage added to the feedback at IC17a/2. This voltage is adjusted by means of R83.

5.3.5.2.5 The voltage square wave across R77 is shaped (differentiated) by C33/R76, to provide a bipolar waveform similar to that produced by a measuring head. Since the square wave is at half the VCO frequency, and an output pulse is generated by both the leading and trailing pulse edges, the calibrator output is at the VCO frequency.

5.3.5.3 External Calibrator

5.3.5.3.1 The external calibrator provides a square wave output at 500 kHz having a true r.m.s. voltage of 223.6 mV when loaded with 50 Ω. The output of a 1 MHz oscillator in IC15 is divided by two in IC16 to provide a 500 kHz signal of accurate unity mark/space ratio at IC16/8. When the calibrator is not in use this output is inhibited by a logic '0' at IC16/10, which holds IC16b in the set state. This logic level is set by the microprocessor system via the EXT CAL SELECT control line.

5.3.5.3.2 When the output at IC16/8 is enabled it drives the amplifier formed by Q21, Q22, Q23, Q24 and IC17b. This amplifier operates in a similar manner to the one used in the internal calibrator, except that current flows in Q24, and not in Q23, when the calibrator is inhibited. The calibrator output is taken across R91, which provides a 50 Ω source impedance, and is fed to both CALIBRATOR sockets in parallel. The correct output level is only obtained when the system is loaded with 50 Ω, so that only one socket may be used at a time.

5.3.6 THE GPIB INTERFACE

5.3.6.1 The GPIB interface is carried on assembly 19-1017. The circuit diagram is given in Fig. 13 in Section 7 of this manual.

5.3.6.2 Address Setting and Recognition

5.3.6.2.1 When the interface address is set on the bus by the controller it is recognised by the General Purpose Interface Adaptor (GPIA), IC2, by comparison with the interface address held in an internal address register. The address set on the rear panel switches is read by the microprocessor and written into the GPIA address register every 10 ms.

5.3.6.2.2 The microprocessor sees the address switches as an addressable register within the GPIA. When the GPIA receives the appropriate address it responds by generating an enable signal ($\overline{ASE}$) at IC2/4. This enables IC12, putting the logic levels set by the address switches onto the data bus. The microprocessor reads the switch settings from the bus, and then writes the pattern into the GPIA address register.

5.3.6.3 Operation as a Listener

5.3.6.3.1 When the interface is addressed to listen the GPIA conducts the handshake procedure up to the point where the ready for data (RFD) indication is given. At this point IC2/27 is at logic '0', setting the data line buffers in IC3 and IC13 to the receive condition. Data from the bus enters the GPIA data-in register, and an interrupt request is generated by IC2/40 going to logic '0'. This puts IC18/8 to logic '1' and so enables IC9c, which pulls the microprocessor $\overline{IRQ}$ line to 0 V.

5.3.6.3.2 The microprocessor interrupt routine will establish the reason for the interrupt. The GPIA and IC19 are enabled by the $\overline{GCS}$ signal, and the direction of data transfer through IC19 is set by the R/$\overline{W}$ signal. The GPIA data-in register is addressed, and the data are transferred to the microprocessor.

5.3.6.3.3 When the data transfer is complete the GPIA cancels the interrupt request and allows the data accepted (DAC) line to go high. The handshake routine then continues, and a further data byte, if available, is loaded into the data-in register. The interrupt and data transfer sequence is then repeated.

5.3.6.4 Operation as a Talker

5.3.6.4.1 When the GPIA is addressed to talk the data-out register will normally be empty. Under these conditions an interrupt request is generated by putting IC2/40 to logic '0'. This output is used to generate an interrupt request for the microprocessor, via IC18, IC14d and IC9c, and to set IC10a.

5.3.6.4.2 When IC10a is set a logic '1' is applied to IC11/10. Since IC10b is normally reset, and IC2/27 is at logic '1' when the GPIA is addressed to talk, IC11/9 and 11 are also at logic '1', giving logic '0' at IC11/8. This open circuits the bilateral switches between TP1 and TP2, breaking the RFD line to IC2/18. Even if the listening device asserts that it is ready for data, the GPIA will not attempt to load the contents of the data-out register onto the bus, as IC2/18 is held at logic '0' by the bilateral switch in IC6 which is driven from IC4b.

5.3.6.4.3 The microprocessor interrupt routine will establish the reason for the interrupt. The GPIA and IC19 are enabled by the $\overline{GCS}$ signal, and the direction of data transfer through IC19 is set by the logic level on the R/$\overline{W}$ line. The GPIA data-out register is addressed and a data byte is written into the register.

5.3.6.4.4 Following the data transfer the microprocessor sets data bus line BD0 to '0' and addresses IC15, using address lines A0, A1 and A2, so that the microprocessor enable (E) pulse is directed to IC10a/11. This clocks IC10a to the reset condition, giving a logic '0' at IC11/10. The bilateral switches in IC6 reconnect the RFD line to the GPIA, and release IC2/18 from 0 V. When the RFD line puts IC2/18 to logic '1' the GPIA loads the contents of the data-out register onto the bus and continues with the handshake sequence.

5.3.6.4.5 If, for any reason, the GPIA is taken out of the talk state part way through a message, the data-out register will be left containing an untransmitted data byte. This situation can arise, for example, if the controller stops the message in order to conduct a serial poll.

5.3.6.4.6 When the GPIA is readdressed to talk, either of two requirements may apply. The GPIA may be required to continue with the interrupted message, or may be required to transmit a byte (e.g. the status byte) other than that held in the data-out register. The two situations are distinguished by whether there has, or has not, been a data transfer between the GPIA and the microprocessor since the GPIA left the talk state.

5.3.6.4.7 In the latter case IC10a will be in the reset condition, giving a logic '0' at IC10a/9 and a logic '1' at IC11/8. The bilateral switches of IC6 between TP1 and TP2 will be in the conducting condition, so the RFD line to IC2/18 is unbroken. When the GPIA is addressed to talk the byte in the data-out register will be transmitted, followed by the remainder of the interrupted message.

5.3.6.4.8 If a data transfer from the GPIA to the microprocessor has occurred since the GPIA left the talk state, IC10a will have been set by the last interrupt request from IC2/40. This will be the situation if, for example, a serial poll is to be conducted, as the serial poll enable (SPE) message byte will have been received and transferred. When the GPIA is addressed to talk, IC2/27 goes to logic '1', and, because IC11/9 and 10 are at logic '1', the RFD line is broken by IC6. When the listener sets the RFD line high IC18/1 is put to logic '1'. Since IC18/2 and 13 are at logic '1' an interrupt request to the microprocessor is generated via IC14d and IC9c. The microprocessor will see this as a demand for fresh data from the GPIA, and will over-write the byte held in the data-out register.

5.3.6.4.9 During a serial poll, after transferring the status byte to IC2, the microprocessor addresses IC15 to direct the enable (E) signal to IC10b, clocking it to the set state. If the byte transferred is not the status byte, IC15 is addressed to direct the enable signal to IC10a, clocking it to the reset state. In either case IC11/8 will go to logic '1', the RFD input will be connected by IC6 to IC2/18, and the byte will be transmitted.

5.3.6.5 Detection of the Serial Poll Disable Message

5.3.6.5.1 When a serial poll sequence has been completed the controller sends the serial poll disable (SPD) message. This is detected by IC8b, c and d and IC1, giving a logic '0' at IC1/8. This returns IC10b to the reset condition, giving a logic '1' at IC11/9 and disconnecting the RFD line from IC2/18 at IC6.

APPENDIX 1

ANALYSIS OF RMS MEASURING CIRCUIT

5.A.1.1 The block diagram of the measuring circuit is shown in Fig. 5.7. The voltages Vs and Vn represent the signal and noise inputs from the preceding circuit, while Vox and Voy are the input offset voltages occurring at the multiplier inputs. The input Vc is a voltage generated during the auto-zero period and injected into the circuit during the following measurement period.

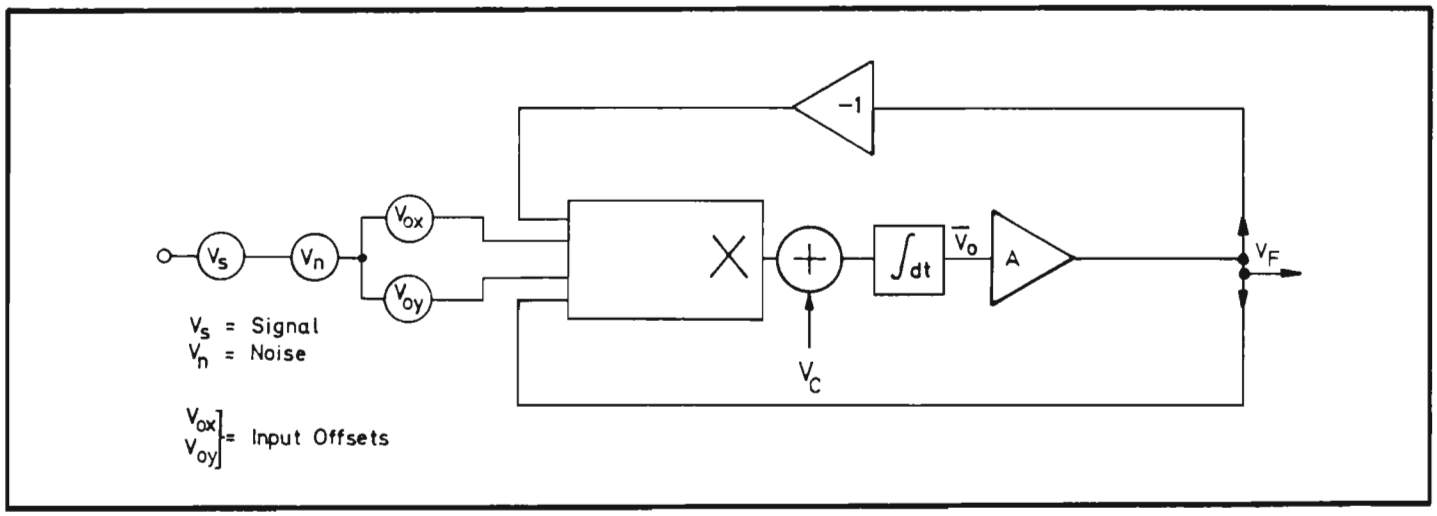


Fig. 5.7 Feedback Loop

5.A.1.2 At the multiplier output:

$$V_o = (V_s + V_n + V_{ox} + V_F)\ (V_s + V_n + V_{oy} - V_F)$$

$$= (V_s + V_n + V_{ox})\ (V_s + V_n + V_{oy}) - V_F\ (V_s + V_n + V_ox) + V_F\ (V_s + V_n + V_{oy}) - V_F^2$$

$$= (V_s + V_n)^2 + (V_{ox} + V_{oy})\ (V_s + V_n) + V_{ox}V_{oy} - V_F\ (Vox - Voy) - V_F^2$$

$$= V_s^2 + V_n^2 + 2V_sV_n + V_s\ (V_{ox} + V_{oy}) + V_n\ (V_{ox} + V_{oy}) + (V_{ox}V_{oy}) - V_F\ (V_{ox} - V_{oy}) - V_F^2$$

Since V_s and V_n are AC quantities, and so have mean values of zero, at the amplifier input

$$\overline{V_o + V_c} = \overline{V_s^2 + V_n^2 + V_{ox}\,V_{oy} - V_F\ (V_{ox} - V_{oy}) - V_F^2 + V_c}$$

But $V_F = A(\overline{V_o + V_c})$, and if A is large $\overline{V_o + V_c} = \frac{V_F}{A} = 0$

$$0 = \overline{V_F^2 + V_F\ (V_{ox} - V_{oy}) - (V_s^2 + V_n^2 + V_{ox}V_{oy} + V_c)}$$

5.A.1.3 If the sense of the feedback voltages to the x and y inputs is reversed the last expression becomes

$$0 = V_F^2 - V_F (V_{ox} - V_{oy}) - \overline{(V_s^2 + V_n^2 + V_{ox} V_{oy} + V_c)}$$

The difference between the two expressions is the sign of the second term. Thus, if the feedback sense is switched at a rate such that the integrator provides adequate averaging, the mean value of this term is zero, and it can be ignored. Such feedback switching thus reduces the effect of the offsets at the multiplier input.

Solving $0 = V_F^2 - \overline{(V_s^2 + V_n^2 + V_{ox} V_{oy} + V_c)}$ for V_F gives

$$V_F = \sqrt{\overline{V_s^2 + V_n^2 + V_{ox}V_{oy} + V_c}}$$

The required output from the circuit is

$$V_F = \sqrt{\overline{V_s^2}}$$

so the actual output shows an error of $\sqrt{\overline{V_n^2 + V_{ox}V_{oy} + V_c}}$

5.A.1.4 The voltage V_C is generated in the auto-zero circuit. During auto-zeroing V_S is made zero, and the residual value of V_F is integrated. This integral is injected as V_C, such that the residual value of V_F is driven to zero. At this point

$$\overline{V_c} = - \overline{(V_n^2 + V_{ox}V_{oy})}$$

V_C is maintained during the measurement period, so that the unwanted input to the amplifier due to noise and the multiplier input offsets is cancelled.

APPENDIX 2

OPERATION OF LINEARISED TRANSCONDUCTANCE MULTIPLIER

5.A.2.1 A schematic circuit of the multiplier is given in Fig. 5.8. The inputs are the differential current inputs at 1 and 2. It is a property of this circuit that the ratios I_P/I_Q and I_S/I_R are equal, and are equal to the ratio of the currents in the linearising networks. (Proof of this property is unnecessary for the purposes of this manual).

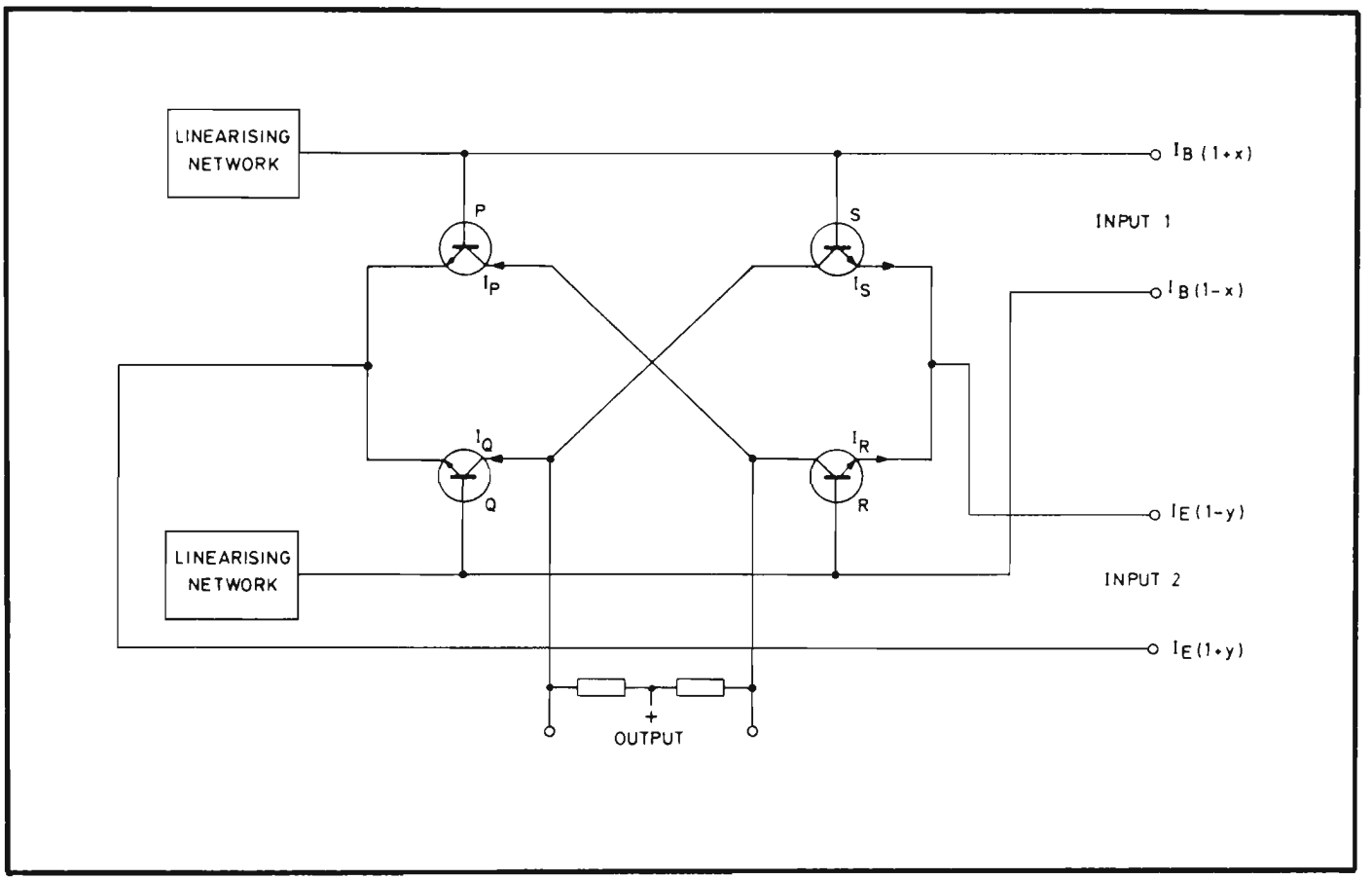


Fig. 5.8 Multiplier Operation

5.A.2.2 If the currents at input 1 with zero input signal are both I_B, then the currents with an applied signal of $2I_Bx$ will be $I_B(1+x)$ and $I_B(1-x)$. The currents at input 1 form the currents in the linearising networks, and so set the ratios of the collector currents I_P/I_Q and I_S/I_R to $(1+x)(1-x)$.

5.A.2.3 The currents at input 2 with a signal of $2I_Ey$ will be $I_E(1+y)$ and $I_E(1-y)$. The collector currents of the multiplier transistors will then be:

$I_P = \frac{1}{2}I_E\ (1+y)(1+x)$
$I_Q = \frac{1}{2}I_E\ (1+y)(1-x)$

Two currents having a total of $I_E(1+y)$ and a ratio $1+x/1-x$ (equal to the ratio of the linearising networks.

$I_S = \frac{1}{2}I_E\ (1-y)(1+x)$
$I_R = \frac{1}{2}I_E\ (1-y)(1-x)$

Two currents having a total of $IE(1-y)$ and a ratio of $1+x/1-x$.