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1255/60
Frequency Response & Impedance/Gain-Phase Analyzers

MAINTENANCE MANUAL
Volumes 1 & 2

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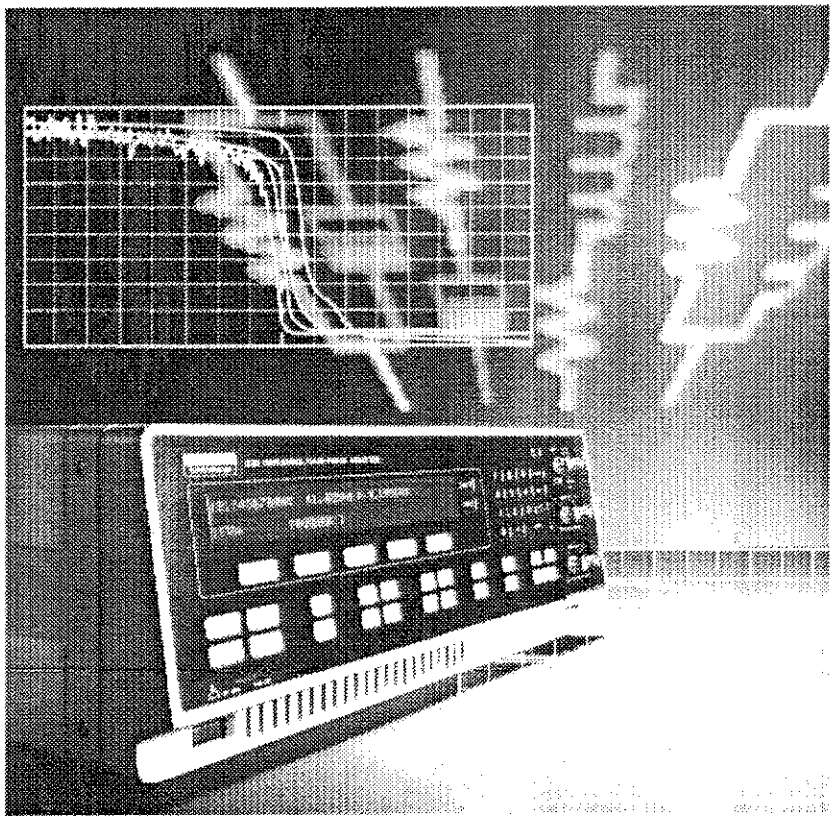
1255 & 1260
Frequency Response Analyzer & Impedance/Gain-Phase Analyzer



MAINTENANCE MANUAL

Volume 1

GENERAL SAFETY PRECAUTIONS

The equipment described in this manual has been designed in accordance with IEC publication 348 (Class 1) Safety Requirements for Electronic Measuring Apparatus, and has been supplied in a safe condition. To avoid injury to an operator or service technician the safety precautions given below, and throughout the manual, must be strictly adhered to, whenever the equipment is operated, serviced or repaired. For specific safety details, please refer to the relevant sections within the manual.

The equipment is designed solely for electronic measurement and should be used for no other purpose. Solartron Instruments accept no responsibility for accidents or damage resulting from any failure to comply with these precautions.

GROUNDING
To minimize the hazard of electrical shock it is essential that the equipment is connected to a protective ground whenever the power supply, measurement or control circuits are connected, even if the equipment is switched off. The protective ground for ac and dc supplies is connected separately.

AC GROUND is connected via the ac supply cord. The cord must be plugged into an ac line outlet with a protective ground contact. When an extension lead is used, this must also contain a ground conductor. Always connect the ac supply cord to the supply outlet before connecting the control and signal cables; and, conversely, always disconnect control and signal cables before disconnecting the ac supply cord. The ac ground connection must have a continuous current rating of 6A.

DC GROUND is connected via a ground stud on the equipment power supply unit (PSU). The dc ground connection must have a continuous current rating of 35A.

Where both protective grounds are used it must be ensured that these grounds are, and will remain, at the same potential.

AC SUPPLY VOLTAGE
Never operate the equipment from a line voltage or frequency in excess of that specified. Otherwise, the insulation of internal components may break down and cause excessive leakage currents.

FUSES
Before switching on the equipment check that the fuses accessible from the exterior of the equipment are of the correct rating. The rating of the ac line fuse must be in accordance with the voltage of the ac supply.

Should any fuse continually blow, do not insert a fuse of a higher rating. Switch the equipment off, clearly label it "unserviceable" and inform a service technician.

EXPLOSIVE ATMOSPHERES
NEVER OPERATE the equipment, or any sensors connected to the equipment, in a potentially explosive atmosphere. It is NOT intrinsically safe and could possibly cause an explosion.

Continued overleaf.

SAFETY PRECAUTIONS (continued from previous page)

SAFETY SYMBOLS

For the guidance and protection of the user, the following safety symbols appear on the equipment:

SYMBOL	MEANING
	Refer to operating manual for detailed instructions of use.
	Hazardous voltages.
	Protective conductor terminal. This must be connected to ground before operating the equipment.

NOTES, CAUTIONS AND WARNINGS

For the guidance and protection of the user, Notes, Cautions and Warnings appear throughout the manual. The significance of these is as follows:

NOTES	highlight important information for the reader's special attention.
CAUTIONS	guide the reader in avoiding damage to the equipment.
WARNINGS	guide the reader in avoiding a hazard that could cause injury or death.

AVOID UNSAFE EQUIPMENT

The equipment may be unsafe if any of the following statements apply:

- Equipment shows visible damage.
- Equipment has failed to perform an intended operation.
- Equipment has been subjected to prolonged storage under unfavorable conditions.
- Equipment has been subjected to severe physical stress.

If in any doubt as to the serviceability of the equipment, don't use it. Get it properly checked out by a qualified service technician.

LIVE CONDUCTORS

When the equipment is connected to its measurement inputs or supply, the opening of covers or removal of parts could expose live conductors. The equipment must be disconnected from all power and signal sources before it is opened for any adjustment, replacement, maintenance or repair. Adjustments, maintenance or repair, must be done only by qualified personnel, who should refer to the Maintenance Manual.

EQUIPMENT MODIFICATION

To avoid introducing safety hazards, never install non-standard parts in the equipment, or make any unauthorized modification. To maintain safety, always return the equipment to Solartron Instruments for service and repair.

1255/60 Maintenance Manual Contents

VOLUME 1

5 BOARD DESCRIPTIONS

6 CALIBRATION OF 1255 & 1260

VOLUME 2

Chapter *Page*

7 MECHANICAL DETAILS

8 PARTS LISTS & COMPONENT LOCATION DIAGRAMS

9 1255 & 1260 CIRCUIT DIAGRAMS

10 FAULT DIAGNOSIS

Chapter 1
Introduction to the 1255-60 Maintenance Manual

1 GENERAL

This Maintenance Manual is in two volumes. Volume 1 contains Chapters 1 to 6 and Volume 2 contains Chapters 7 to 10.

The information in the manual is provided to facilitate fault diagnosis, fault rectification and calibration of the 1255 and 1260 instruments, both on-site and at a service centre.

Before commencing any work on the 1255 or 1260 instruments, refer to the safety notes given below.

On-site servicing is normally restricted to pcb replacement. To assist in the location of a faulty pcb, both 1255 and 1260 have built-in diagnostic programs The use of these programs and the interpretation of their results is described in in Chapter 4 'Self Test Facilities'.

Calibration routines for both instruments are given in Chapter 6. This chapter is sub-divided into two parts, Part A for the 1255 and Part B for the 1260 It is recommended that the Calibration Test Unit (Schlumberger Instruments Part No. 12606801) be used where stated; however a locally manufactured alternative, of suitable standard, may be used where necessary.

The mechanical design of the 1255 and 1260 instruments is such that disassembly and reassembly is straightforward. The removal of instrument top and bottom covers, pcbs and some other major components is fully described in Chapter 7 of the manual. This chapter also contains diagrams showing the locations of the various pcbs, plus other main components, within the instrument frame assemblies.

The circuit descriptions in Chapter 5 are written on the assumption that the service technician has a sound understanding of basic circuit techniques and is familiar with digital integrated circuit theory. For each pcb, a circuit description is included and where neccessary, a simplified schematic diagram. Due to the volume of information contained in this chapter, all diagrams are given a three number code, eg, 5.2.1, indicating the chapter (5), section (2) and figure number (1).

The System Description in Chapter 2, describes the data flow between the various instrument pcbs. Chapter 3, 'The 1255-60 Bus', describes the 1255-60 bus connections, program interrupts and the bus 'read - write' cycles.

The descriptive chapters mentioned above are complemented by parts lists and component location (annotation) diagrams in Chapter 8, circuit diagrams in Chapter 9 and fault finding procedures in Chapter 10.

2 SAFETY

Extreme care should be taken when working on the internal areas of these instruments while they are, or have recently been, switched ON. Hazardous voltages exist in the area of the ac supply circuitry. To ensure a safe working environment, it is recommended that the following points be strictly observed:

- Ensure that feet are always insulated from the floor, either by wearing footwear with insulating rubber soles, or by standing on a rubber mat.
- Always use insulated-handle tools of the correct voltage rating.

- Always use the 'single hand' technique, viz, work with only one hand in the hazardous area. Keep the other hand away from grounded surfaces, such as the instrument mainframe.

If an instrument has been switched off for only a short space of time, it is advisable to discharge any capacitors in hazardous voltage areas with a resistor of suitable value. Alternatively, allow the capacitor time to discharge through the internal circuitry.

Chapter 2
System Description

1 GENERAL

This chapter gives an overall description of the 1255/60 and describes briefly the board functions, the interaction between these functions and the supervisory control of 1255/60 by the main processor, pcb 22.

2 SYSTEM CONFIGURATION

Fig. 2.2, at the rear of this chapter, is a schematic block diagram of the 1255/60 system.

3 SYSTEM CONTROL

The internal operation of the 1255/60 is supervised by the main processor. The processor responds to any valid local (front panel) or remote command to set up the functions of other boards in the system. It also performs the software routines that process the measurement data.

The main processor memory consists of the following:

- EEPROM. Used to hold calibration constants and for program storage. Also contains database set-ups.
- RAM (CMOS). Used mainly as a scratchpad memory but also some program storage. Has a battery back-up.
- EPROM. Holds the command translation and analysis instructions.

Memory maps defining these areas are shown in Table 2.1a to g, at the end of this chapter.

4 POWER-UP STATE

The 1255/60 is protected by a power-fail detect facility which determines the control state of the instrument on power-up. On power-down, the main processor calculates a checksum of the measurement and control data contained in its battery sustained RAM and stores the checksum. When power returns, the processor re-calculates the checksum and compares it with the original. If the checksums are identical and no option boards have been inserted (1260 only), or removed from the instrument since power down, then the instrument powers-up in the same state as it was before power-down but with measurement stopped and the generator output turned off.

5 COMMAND STRUCTURE

The main processor can receive commands from three sources:

the front panel keyboard controls

an RS232/RS423 serial link

the general purpose interface Bus (GPIB)

Each of these sources is serviced by an appropriate interface in the main processor. The commands received by the processor consist of a simple string of ASCII alpha-

numeric characters, whose significance parallels the hardkey-softkey arrangement on the instrument front panel. The action of the front panel keys is translated into ASCII form by the front panel processor. Arbitration over the command source priorities , for the local 1, local 2 and remote control modes, is maintained by the main processor.

Once the main processor receives a command from one of the above sources, it implements it by setting up the control states of the appropriate instrument pcbs. It does this by writing the required states into the control registers on these pcbs. Any pcb requiring attention can alert the main processor by means of an interrupt request. When the processor receives such a request, it interrogates the pcbs through their status registers.

6 STIMULUS SIGNAL GENERATION

A stimulus signal for a passive system under test is produced by the high frequency (HF) generator board (pcb 14). Synchronism between this signal and the analysis is achieved through the low frequency (LF) synthesizer board (pcb 18). The LF synthesizer board contains a crystal-controlled oscillator and frequency dividers that provide a digital drive signal for the HF generator and synchronisation signals for the remainder of the system.

The frequency of the HF generator output is written, by the main processor, into the LF synthesizer control registers. Frequency division in line with these parameters takes place on three boards, the LF synthesizer board, the HF generator board, and the analyser control board, pcb17. The distribution of the frequency dividers used is shown in Fig. 2.2 whilst the division of ratios is listed in Table 5.9.1 in Chap. 5 of this manual. The remainder of the generator output parameters, eg, amplitude, bias, and sine/square waveform, are written into the generator control registers.

7 SIGNAL ANALYSIS

Signal analysis for each channel, takes place on two pcbs for the 1255; the analyzer board, pcb 10 and the main processor board, pcb 22. For the 1260 an additional board, pcb 31, is combined with a pcb 10 to form a current analyzer.

The analysis uses a technique derived from the Fourier transform. With this, the incomming signal is first converted into a digital form and then summed, cycle-by-cycle, across 104 sample points (see Fig. 2.1). The signal is thus 'integrated' into a single cycle which is stored in the analyser RAM. This process gives noise rejection. The main processor then takes the result and uses the reference functions sine and cos θ, to compute respectively, the in-phase and quadrature components.

The number of cycles to be included in the measurement is set into the control register of the analyzer control board (pcb 17) as are the measurement commands. During the signal integration process, the analyzer control board, addresses the analyzer RAM for each successive measurement sample. The main processor, alerted on the completion of each data block, is then (on completion of a measurement) allowed to retrieve the stored result.

The control settings for amplitude range, ac/dc coupling, etc., are written by the main processor into the control registers of the individual analyzer boards.

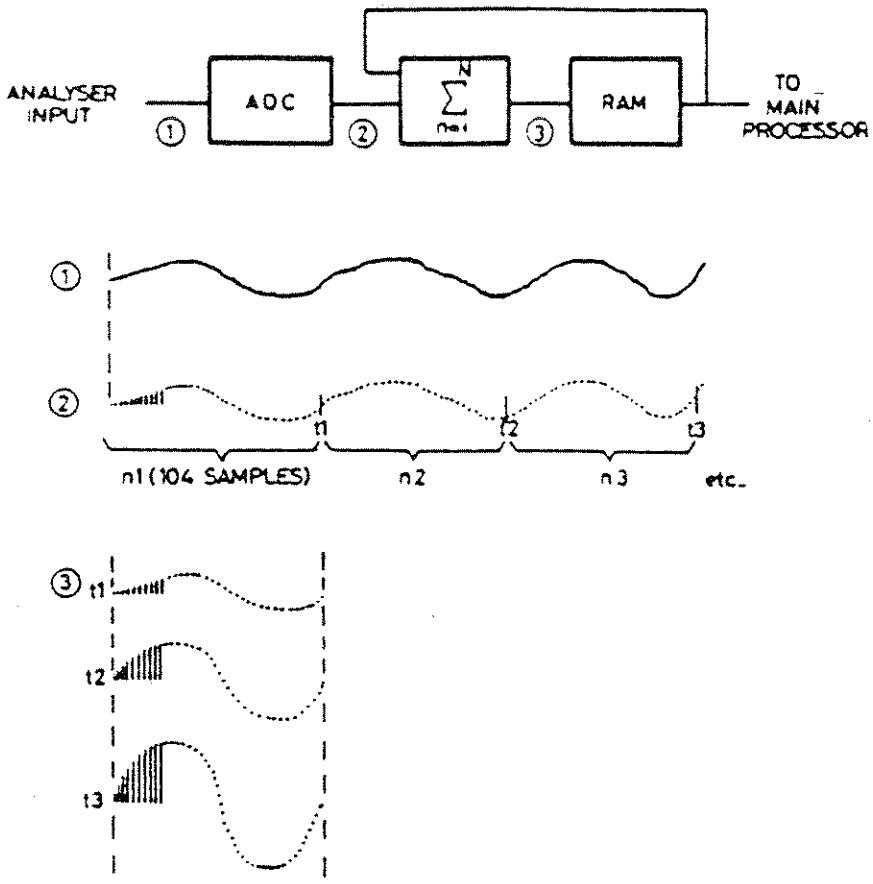


Fig. 2.1 *Analyzer Integration Process*

8 POST ANALYSIS DATA PROCESSING & OUTPUT CONTROL

In addition to its analysis action, the main processor scales the analysis result, subjects the result to any pre-selected limit checks, stores successive results in the 'history file' and outputs the results as requested by the user.

Data for display on the front panel are translated into a suitable format by the front panel processor.

9 PCB LOCATIONS

The recommended locations for pcbs within the mainframe are included in Chapter 7. Figs. 7.1 and 7.2 refer.

Table 2.1a to g. *1255-65 Bit maps*

a. Primary Map

Address Range	Function
0000-38FF	Paged RAM
3900-39FF	Board Presence
3A00-3AFF	Interface Devices
3B00-3BFF	Device Enables
3C00-3FFF	Paged Analyzer RAMS
4000-7FFF	Paged ROM
8000-FFFF	ROM

b. Memory IC Locations Map

Address Range	IC No./ Page No. P1 P2 P3 P4
0000-1FFF	14 16 18 20
2000-38FF	15 17 19 21
4000-7FFF	25* 28* 25† 28†
8000-BFFF	26
C000-FFFF	27

* Lower half of IC
† Upper half of IC

c. Board Presence Map (msb Reads 0 if board present and 1 otherwise)

Address	Pcb
390F	Analyzer Control
391F	Analyzer 1
392F	Analyzer 2
393F	Generator
394F	HF Generator
395F	Synthesizer
396F	HF Synthesizer
397F	Spare
398F	Spare
399F	Spare
39AF	Kbd./Display
39BF	Analyzer 3 (Current)
39CF	Spare
39DF	Binsort
39EF	Spare
39FF	Spare

d. Interface Device Map

Address Range	Interface
3A00-3A0F	GPIB
3A10-3A1F	ACIA (Spare)
3A20-3A2F	ACIA (Kbd/Disp)
3A30-3A3F	ACIA (RS423)
3A40-3A4F	ACIA (Spare)
3A50-3A5F	Timer
3A60-3A6F	F.P.Processor (Not used)
3A70-3A7F	Switches/LEDs *
3A80-3AFF	Spare

* Refer to Table 'e' below

e. LED / Switch Map

Address	Function
3A70	Processor Board LEDs
3A71	Analyzer RAM Page
3A72	RAM/ROM Page Select
3A73	Processor Board Switches.
3A74	RS 423 Sw itches.
3A75	GPIB Switches
3A76	Spare
3A77	Spare

f. Device Enable Map

Address	Board
3B00-3B0F	Analyzer Control
3B10-3B1F	Analyzer 1
3B20-3B2F	Analyzer 2
3B30-3B3F	Generator
3B40-3B4F	HF Generator
3B50-3B5F	Synthesizer
3B60-3B6F	HF Synthesizer
3B70-3B7F	Spare
3B80-3B8F	Spare
3B90-3B9F	Spare
3BA0-3BAF	Kbd./Display
3BB0-3BBF	Analyzer 3 (Current)
3BC0-3BCF	Spare
3BD0-3BDF	Binsort
3BE0-3BEF	Spare
3BF0-3BFF	Spare

g. Device Control Map

Pcb	Read/ Write	Function	Bit Function (msb) d7	d6	d5	d4	d3	d2	d1	(lsb) d0	Approved Address
17	R	STATUS	FIRQ	MEAS. ENABLE						CARRY*	3B00
	W	CONTROL	RESET CARRY	MEAS.	MEAS. N	PRESET N	RANGE CHANGE	HF/LF	ASYNC.	PRESET ASYNC. COUNT	3B00
	W	CYCLES	256 - N0 0F CYCLES								3B01
10, CH1	R	STATUS	FIRQ								3B10
	W	CONTROL	R2 0 0 0	R1 1 0 0	R0 1=3V 1=300mV 0=30mV	DC/AC	GRND. OUTER	SINGLE / DIFF.	HET COUP.	INT. ENAB.	3B10
10, CH2			(AS FOR CHANNEL 1)								3B20
15	R	STATUS	FIRQ							GEN KILL	3B30
	W	BIAS MS		SPARE WFM	SINE SQ	B-/B+	b11	b10	b9	b8	3B30
	W	BIAS LS	b7	b6	b5	b4	b3	b2	b1	b0	3B31
	W	AMP. MS				POL-ARITY ENAB.	SPARE 2	SPARE 1	a9	a8	3B32
	W	AMP. LS	a7	a6	a5	a4	a3	a2	a1	a0	3B33
14	R	STATUS	FIRQ					O/P O/LOAD	COM. MODE O/LOAD		3B40
	W	CONTROL			AGC 0 + 1 + 0 + 1 +	AGC 0=-40dB 0=-40dB 1=-20dB 1=0dB	O/P ENAB.	V/I	HF	LF	3B40

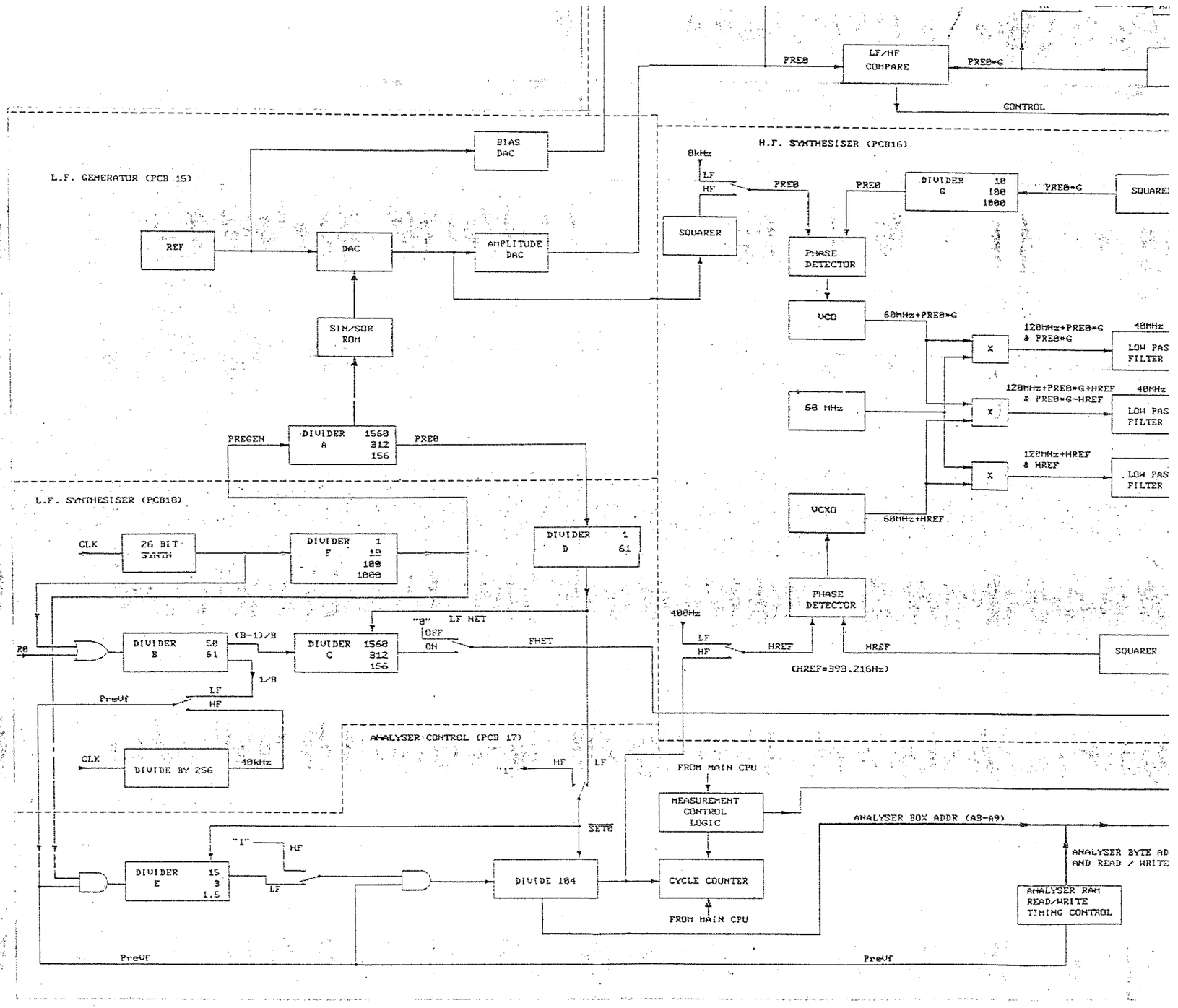
*Causes FIRQ

g. Device Control Map *(Contd)*

Pcb	Read/ Write	Function	Bit Function (*Causes FIRQ) (msb) d7	d6	d5	d4	d3	d2	d1	(lsb) d0	Approved Address
18	W			R3	R2	R1	HF/LF		F26	F25	3B50
	W		F24	F23	F22	F21	F20	F19	F18	F17	3B51
	W		F16	F15	F14	F13	F12	F11	F10	F9	3B52
	W		F8	F7	F6	F5	F4	F3	F2	F1	3B53
	W	CONTROL	---------- FORCE WAVEFORM DIVIDER ----------								3B54
	W	CONTROL	---------- PRE Vf END ----------								3B55
	W	CONTROL	---------- PRE Vf START ----------								3B56
	W	CONTROL	---------- SET 0 DIVIDER ----------								3B57
16	R	STATUS									3B60
	W	CONTROL	RESET				HF/LF	×1000	×100	×10	3B60
SPARE											3B70
SPARE											3B80
SPARE											3B90
KBD / DISPLAY											3BA0
10 CH3 (I I/P)			(AS FOR CHANNEL 1)								3BBO
SPARE											3BC0
B'sort	R	STATUS	FIRQ					START OF SEQ.	ERR	INTER-LOCK	3BD0
	W	CONTROL				HI/LO	.....	BIN SELECT.		.....	3BD0
	W	CONTROL	..... POSITIVE OR NEGATIVE LOGIC				.....	18/5V	EOM	ENAB. INTER.	3BD1
	W	CONTROL	.....	.....	COUNTER			.....		.....	3BD2
SPARE											3BE0
SPARE											3BF0

Range	Max. Freq.	Range Dividers A	B	C	D	E	F	G	H	LF/HF	LF Het.
10	32MHz (20MHz)*	156	-	-	-	-	1	1000	-	HF	OFF
9	6.5535999MHz	156	-	-	-	-	1	100	-	HF	OFF
8	655.35999kH	156	-	-	-	-	1	10	-	HF	OFF
7	65.535999kH	156	251 (199)*	156	251 (199)*	1.5	1	-	1	LF	ON
6B	32.767999kHz	312	199	312	199	3	1	-	1	LF	ON
6A	19.999999kHz	312	199 (61)*	312	199 (61)*	3	1	-	1	LF	ON
5	6.5535999kHz	1560	61	1560	61	15	1	-	1	LF	ON
5A (4A)*	6.5535999Hz	1560	31 (50)*	1560 (-)*	31 (1)*	15 (3)*	10	-	10 (1)	LF	ON (OFF)*
4	299.99999Hz	1560	50	-	1	3	10	-	1	LF	OFF
3	65.535999Hz	1560	50	-	1	15	100	-	1	LF	OFF
2	6.5535999Hz	1560	50	-	1	15	1000	-	1	LF	OFF
1	not used	-	-	-	-	-	-	-	-	-	-
0	655.35999mHz	1560	50	-	1	15	1000	-	1	LF	OFF

* 1255 only. Other values apply to 1260.



H.F. GENERATOR (PCB14)

GENERATOR OUTPUT

BIAS

LF

HF

CURRENT / VOLTAGE AMPLIFIER

PRE8

LF/HF COMPARE

PRE8*G

AGC

CONTROL

L.F. GENERATOR (PCB 15)

BIAS DAC

REF

DAC

AMPLITUDE DAC

SIN/SQR ROM

PREGEN

DIVIDER A 1560 312 156

PRE8

H.F. SYNTHESISER (PCB16)

8kHz

LF

HF

PRE8

PRE8

DIVIDER G 10 100 1000

PRE8*G

SQUARER

SQUARER

PHASE DETECTOR

VCO

60MHz+PRE8*G

X

120MHz+PRE8*G & PRE8*G

40MHz

LOW PASS FILTER

PRE8*G

60 MHz

X

120MHz+PRE8*G+HREF & PRE8*G-HREF

40MHz

LOW PASS FILTER

PRE8*G HREF

HF

LF

X

120MHz+HREF & HREF

LOW PASS FILTER

HREF

VCXO

60MHz+HREF

PHASE DETECTOR

400Hz

LF

HF

HREF

HREF

(HREF=393.216Hz)

SQUARER

L.F. SYNTHESISER (PCB10)

CLK

26 BIT SYNTH

DIVIDER F 1 10 100 1000

DIVIDER D 1 61

"0" LF HET

OFF

ON

FHET

R8

DIVIDER B 80 61

(B-1)/B

DIVIDER C 1560 312 156

1/B

PreUf

LF

HF

CLK

DIVIDE BY 256

40kHz

ANALYSER CONTROL (PCB 17)

"1"

HF

LF

SET8

"1"

HF

DIVIDER E 15 3 1.5

LF

DIVIDE 184

CYCLE COUNTER

FROM MAIN CPU

FROM MAIN CPU

MEASUREMENT CONTROL LOGIC

ANALYSER BOX ADDR (A3-A9)

ANALYSER ADDRESS (A0-A9) AND R/W*

ANALYSER BYTE ADDRESS (A0-A2) AND READ / WRITE CONTROL (R/W*)

ANALYSER RAM READ/WRITE TIMING CONTROL

PreUf

PreUf

INPUT V1 (PCB18)

LO

HI

INPUT AMPLIFIER

X

LP FILTER

RANGING

ADC

GATE ARRAY

BUFFER

RAM

INPUT V2 (PCB18)

LO

HI

INPUT AMPLIFIER

X

LP FILTER

RANGING

ADC

GATE ARRAY

BUFFER

RAM

CURRENT INPUT

I-U CONVERTR (PCB21)

CURRENT TO VOLTAGE CONVERTER

Sohm/Skohm

LO

HI

VOLTAGE ANALYSER (PCB18)

INPUT AMPLIFIER

X

LP FILTER

RANGING

ADC

GATE ARRAY

BUFFER

RAM

ANALYSER RAM ADDRESS AND CONTROL (R/W*)

MUX

BUFFER

ADDRESS BUS AND R/W*

PROCESSOR BOARD (PCB22)

DATA BUS

BUFFER

MAIN PROCESSOR 6809

Chapter 3
1255-60 Bus

1 GENERAL

This chapter contains information on the interconnections between the instrument printed circuit boards and on the signals conveyed by them.

2 BUS CONFIGURATION

Signals within the instrument are conveyed on bus lines. The bus lines can be divided into three main groups:

1. The device address and data bus, which conveys control and measurement data between the main processor and the other boards.

2. The asynchronous Rx/Tx (UART) links, which convey data between the main processor and the processors in the front panel.

3. Lines conveying signals that are not under the direct control of the main processor.

The routes taken by the three groups of signal lines are shown in Fig 3.3 at the end of this chapter. The signals within each group are listed in Chart 3.1 and Tables 3.1 and 3.2.

Since the device address and data bus is common to all boards, the function and timing of the signals it conveys are described in some detail in Section 3 below. Details of signals not under direct control of the main processor are included in the respective board descriptions. Brief details of the asynchronous Rx/Tx links are included in the description of the main processor.

3 DEVICE ADDRESS AND DATA BUS

The device addess and data bus is used by the main processor to communicate with the instrument functions under its control. Data are transferred via an 8-bit data highway. This is connected to the control and status registers on the printed boards and to the Analyzer random access memories (RAMs).

The main processor uses the data highway to:

* write to the device control registers,

* read from the device status registers,

* retrieve measurement data from the Analyzer RAMs.

* clear the Analyzer RAMs (by writing zeroes) at the beginning of a measurement.

To define the period during which data on the bus are valid the main processor uses the STR/CLK line. This is taken Lo to enable the selected register or RAM location, after the states of the address lines have settled.

Addresses, both for the control and status registers and for Analyzer RAM locations, are applied to the boards via a ten bit address highway.

3.1 DEVICE ADDRESSING

The instrument 'devices' are sections of circuitry through which the main processor controls signal generation and analysis, as distinct from the analyzer RAMs from which it retrieves the measurement data. To access a particular control or status register the main processor asserts the appropriate DEVice ENable line (DEVEN 0-F *[Bar]*) and, where a board contains several registers, the register address. The device enable lines are usually allocated one to a board.

A control register and a status register for the same device have, in many cases, the same address. To differentiate between the two, the main processor uses the Read/Write (R/W*[Bar]*) line. The 'read' state (Hi) indicates a status address and the 'write' state (Lo) a control address.

3.2 ANALYZER RAM ADDRESSING

To access an analyzer RAM the main processor asserts the appropriate RAM enable line (RAMEN 0-3 *[Bar]*) and the location address.

4 PROCESSOR INTERRUPT

Devices that need to alert the main processor, eg, when an operation is finished or when an alarm state occurs, do so via the Fast Interrupt Request (FIRQ *[Bar]*) Line. On receiving such a request the main processor addresses each status register in turn and examines the FIRQ *[Bar]* bit. If this is in the '1' state the processor reads the status of the associated device; if not the device is ignored.

5 BOARD PRESENCE

To check the presence, or absence, of a board in the 1250 the main processor uses the PRESEN*T[Bar]* line. This line should go to a '0' state when a board is fitted and the associated DEVE*N[Bar]* line is asserted. If a board is not fitted the PRESENT*[Bar]* line remains in the '1' (Hi) state.

6 DEVICE REQUEST

Any status bits unable to be reset through the control registers, ie, those relating to alarm states, can be cleared by the RESE*T[Bar]* line.

7 BUS TIMING

The timing of the device address and data bus, for write and read cycles, is shown in Figs 3.2 and 3.3 respectively.

8 DC SUPPLY LINES

The routes taken by the various dc supplies within the instrument are shown in Fig 3.3.

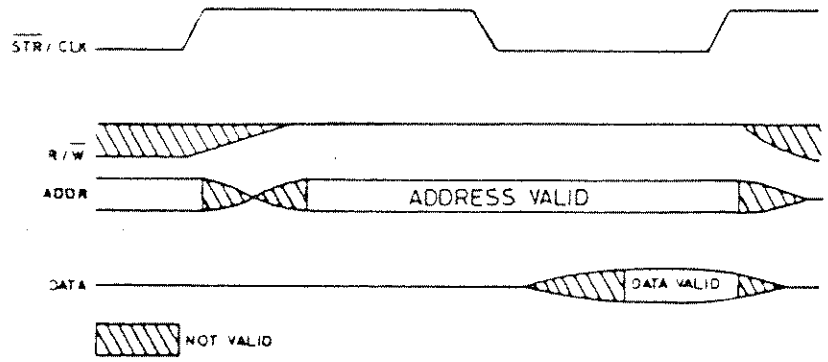


Fig 3.1 *Read Data from Memory or Status Registers.*

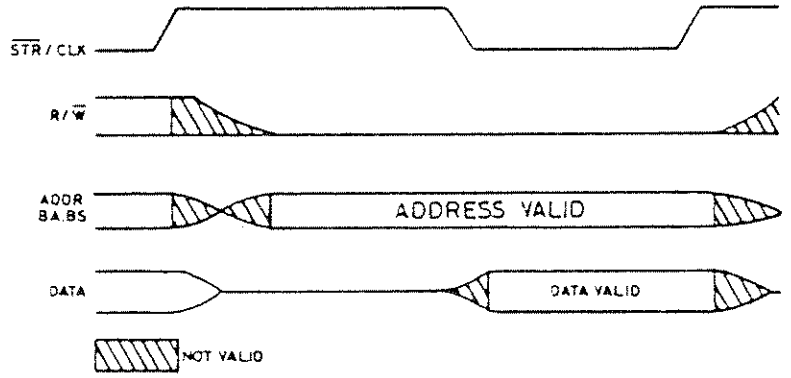


Fig 3.2 *Write Data to Memory or Control Registers.*

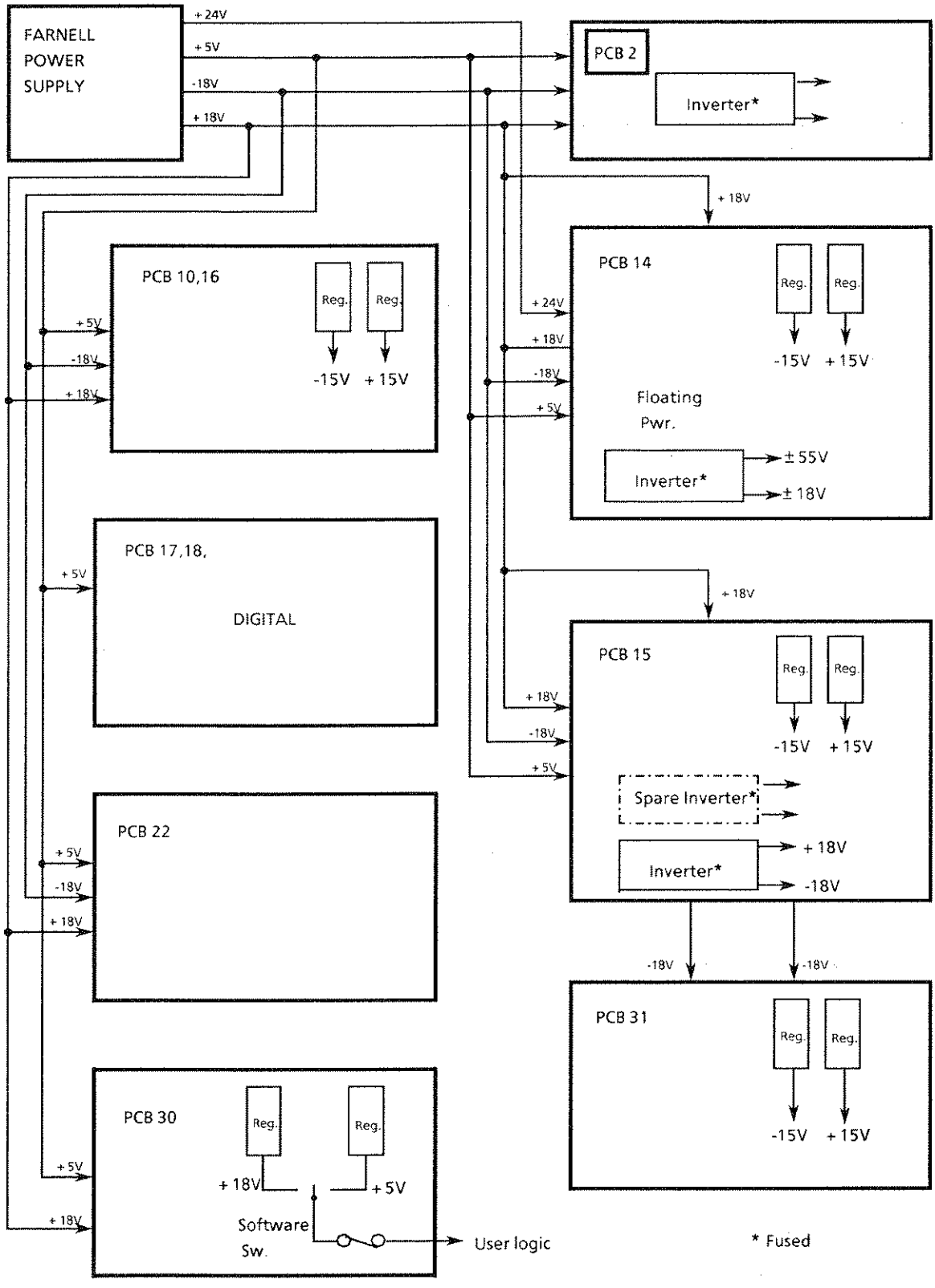


Fig 3.3 *DC supply routes*

Table 3.1 *PLAa and PLAc*

Pin No.	PLA a	PLA c
1	+5V	+5V
2	+5V	+5V
3	0V	0V
4	F/Panel ACIA CLOCK	RESET *[Bar]*
5	RXA Spare ACIA IC107	RXC Spare ACIA IC108
6	TXA Spare ACIA IC107	TXC Spare ACIA 1C108
7	0V	0V
8	-	ACIA CLOCK
9	-	CTS Spare ACIA IC107
10	A0	MODE SEL*[Bar]*
11	A1	RAMEN 0 *[Bar]*
12	A2	RAMEN 1 *[Bar]*
13	A3	RAMEN 2 *[Bar]*
14	-	RAMEN 3 *[Bar]*
15	DEVEN 0 *[Bar]*	D0
16	DEVEN 1 *[Bar]*	D1
17	DEVEN 2 *[Bar]*	D2
18	DEVEN 3 *[Bar]*	D3
19	DEVEN 4 *[Bar]*	D4
20	DEVEN 5 *[Bar]*	D5
21	DEVEN 6 *[Bar]*	D6
22	DEVEN 7 *[Bar]*	D7
23	DEVEN 8 *[Bar]*	A4
24	DEVEN 9 *[Bar]*	A5
25	DEVEN A *[Bar]*	A6
26	DEVEN B *[Bar]*	A7
27	DEVEN C *[Bar]*	A8
28	DEVEN D *[Bar]*	A9
29	PRESENT *[Bar]*	R/W*[Bar]*
30	-	PWR FAIL *[Bar]*
31	FIRQ *[Bar]*	STR*[Bar]*/CLK
32	0V	0V

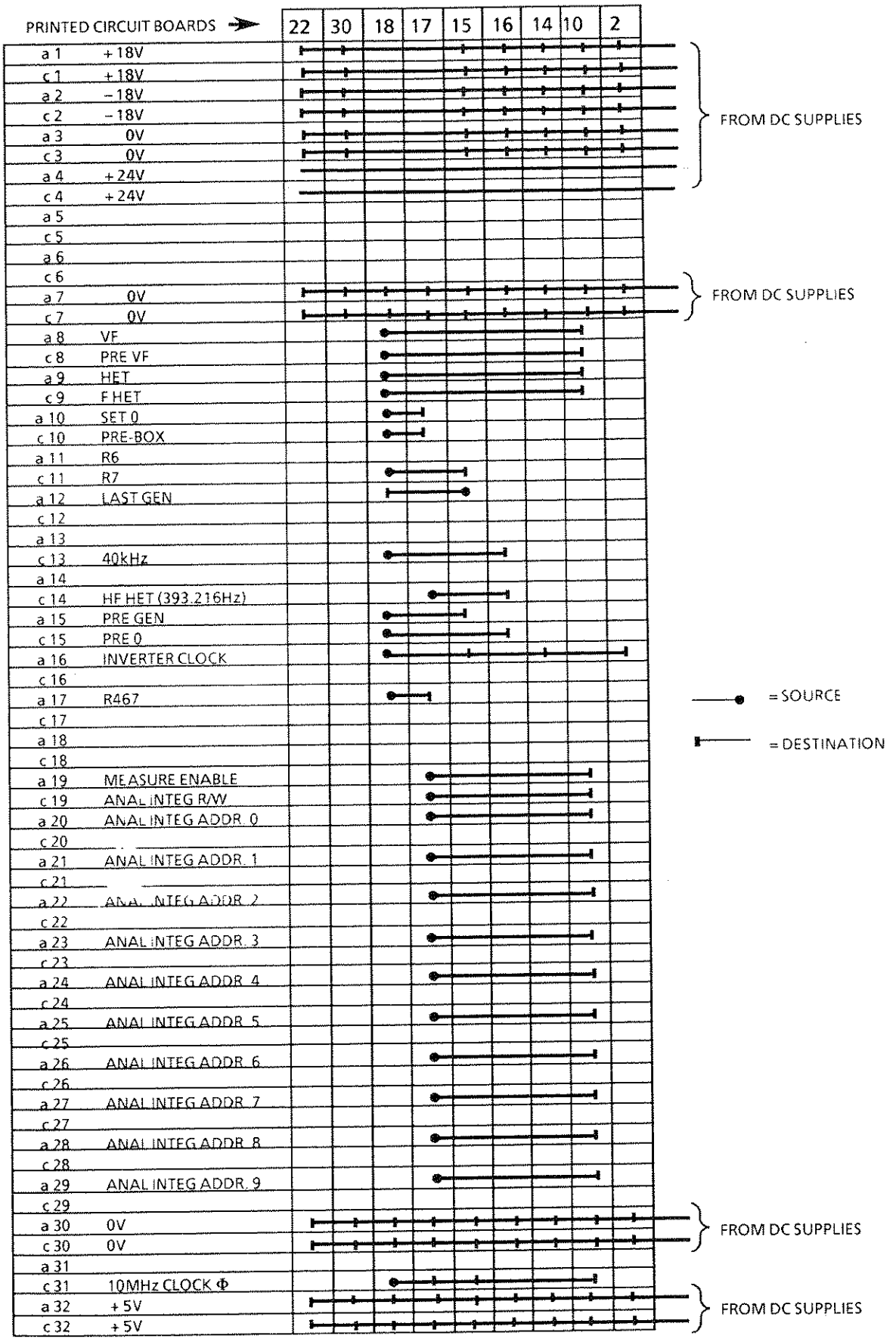
Table 3.2 *PLBa and PLBc*

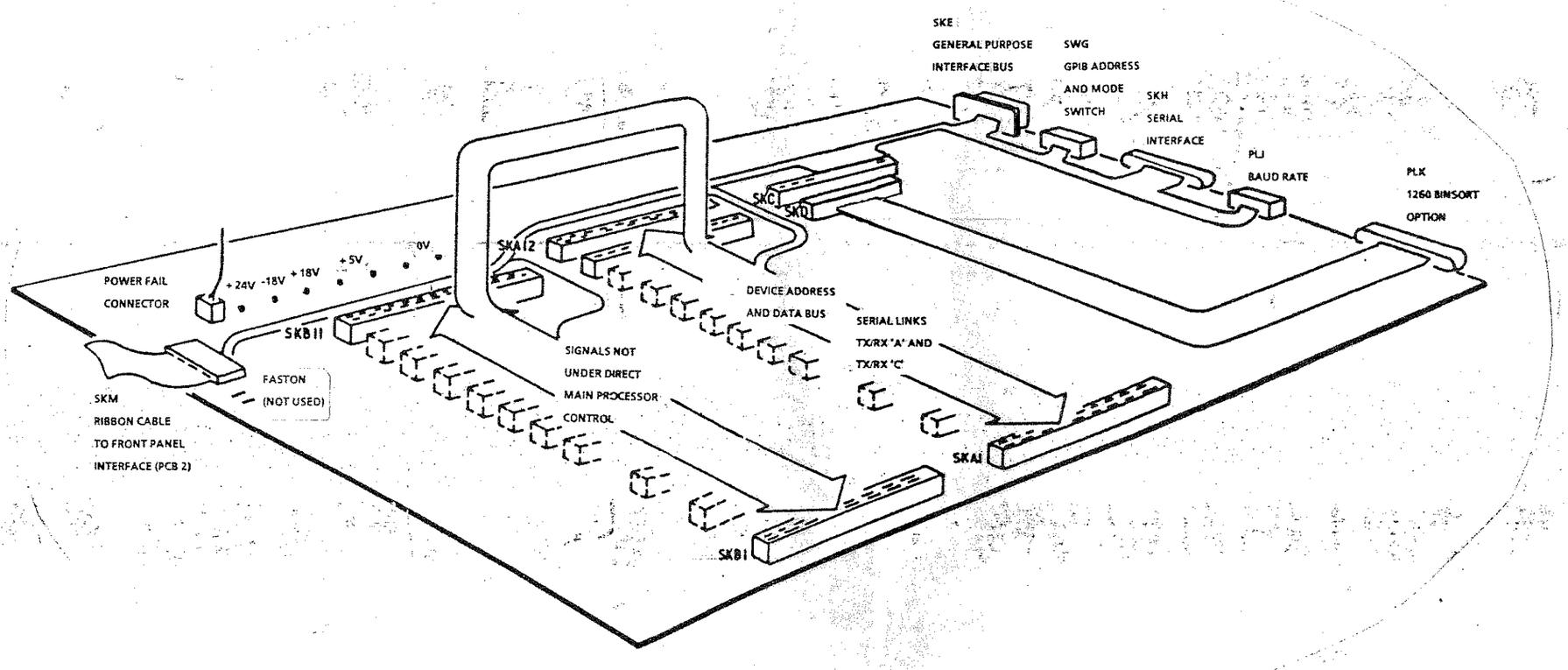
Pin No.	PLB a	PLB c
1	+18V	+18V
2	-18V	-18V
3	0V	0V
4	+24V	+24V
5	-	-
6	-	-
7	0V	0V
8	V_F	PRE V_F1
9	HET	FHET
10	SETϕ*[Bar]*	PREBOX
11	R6*[Bar]*	R7*[Bar]*
12	LASTGEN*[Bar]*	-
13	-	40kHz
14	-	HF HET (393.216Hz)
15	PREGEN	PRE0 *[Bar]*
16	INVERTER CLOCK	-
17	R467	-
18	-	-
19	MEASURE ENABLE *[Bar]*	ANAL.INTEG. R/W
20	ANAL.INTEG. ADDR0	-
21	ANAL.INTEG. ADDR1	-
22	ANAL.INTEG. ADDR2	-
23	ANAL.INTEG. ADDR3	-
24	ANAL.INTEG. ADDR4	-
25	ANAL.INTEG. ADDR5	-
26	ANAL.INTEG.ADDR6	-
27	ANAL.INTEG. ADDR7	-
28	ANAL.INTEG.ADDR8	-
29	ANAL.INTEG.ADDR9	-
30	0V	0V
31	-	10.468983MHz CLOCK (ϕ)
32	+5V	+5V

Table 3.3 *PLCa and PLCc*

Pin No.	PLC a	PLC c
1	+18V	+18V
2	-18V	-18V
3	0V	0V
4	-	-
5	-	-
6	-	-
7	0V	0V
8	GPIB TON	GPIB FUNCTION 2
9	GPIB FUNCTION 1	GPIB ADD SEL 4
10	GPIB ADD SEL 3	GPIB ADD SEL 2
11	GPIB ADD SEL 1	GPIB ADD SEL 0
12	-	-
13	GPIB 0V	GPIB SHIELD (0V)
14	GPIB ATTEN 0V	GPIB ATTEN
15	GPIB SRQ 0V	GPIB SRQ
16	GPIB IFC 0V	GPIB IFC
17	GPIB NDAC 0V	GPIB NDAC
18	GPIB NRFD 0V	GPIB NRFD
19	GPIB DAV 0V	GPIB DAV
20	GPIB REN	GPIB EOI
21	GPIB DIO 8	GPIB DIO 4
22	GPIB DIO 7	GPIB DIO 3
23	GPIB DIO 6	GPIB DIO 2
24	GPIB DIO 5	GPIB DIO 1
25	RS423 POWER 0V	RS423 TX
26	RS423 RX	RS423 RTS
27	RS423 CTS	RS423 DSR
28	RS423 SIGNAL 0V	RS423 DTR
29	RS423 DCD	FRONT PANEL CTS
30	FRONT PANEL TX	FRONT PANEL RX
31	0V	0V
32	+5V	+5V

Table 3.4 *Socket B Connections*




SKE
GENERAL PURPOSE
INTERFACE BUS
SWG
GPIB ADDRESS
AND MODE
SWITCH
SKH
SERIAL
INTERFACE
PL1
BAUD RATE
PL4
1260 BINSORT
OPTION
SKC
SKD
SKA2
POWER FAIL
CONNECTOR
+24V
-18V
+18V
+5V
0V
SKB11
DEVICE ADDRESS
AND DATA BUS
SERIAL LINKS
TX/RX 'A' AND
TX/RX 'C'
SIGNALS NOT
UNDER DIRECT
MAIN PROCESSOR
CONTROL
FASTON
(NOT USED)
SKM
RIBBON CABLE
TO FRONT PANEL
INTERFACE (PCB 2)
SKA1
SKB1

Chapter 4
Self-test Facilities

1 INTRODUCTION

The instrument can perform self tests and supply the user with information on its state of serviceability. Part of the test is performed automatically whenever the instrument is switched on. User action is then required to progress through the remainder of the tests. The self-tests are described in Chapter 5 of the 1255 and 1260 Operating Manuals. If either the message 'INITIALIZED' or 'RESET' is displayed, it is for the reasons given in Section 3 below.

The self-test may also be commanded remotely using the commands given in Chapter 8 of the 1255 and 1260 Operating Manuals.

2 THE MEMORY MAP

The memory map in Chapter 2 (System Description) shows the allocation of instrument memory for specified tasks.

Any operation which causes the instrument to re-start, with the exception of BREAK, automatically directs the main microprocessor to address 8000_H. From this initial address, a variety of software sub-routines can be implemented, according to which operation has been commanded. In all cases, any activity in which the instrument is engaged, such as measuring, sweep, plotting etc., is stopped.

Operations which cause re-start are:

1. Power-up
2. Initialize
3. Break
4. Reset
5. Test

3 POWER UP

When the instrument is switched on, an automatic self-test sequence should be initiated. However, as all self-testing is controlled from the processor (pcb 22), this board must be present for the self-test facilities to function. If pcb 22 is missing, the display will remain blank. With the pcb present, but not running, then a 'copyright' message will be displayed alongside a front panel issue number, eg:

Copyright Schlumberger Elec. (UK) 1987

[Issue 'nn']

If the instrument powers-up correctly, the running time and either, POWER RESTORED, INITIALIZED or RESET will be displayed.

The power-up sequence is as follows:

a. A check is made to ensure that all the **essential** pcbs are present, viz:

Analyser channel 1 (pcb 10),
Generator (pcb 15),
HF generator (pcb 14),
Analyser control (pcb 17,)
Synthesiser (pcb 18).
HF synthesiser (pcb 16).

b. The main processor RAMs are checksum tested, to verify the data base, eg, frequency setting etc, plus any learnt programs and the file.

c. A check is made on the printed circuit board complement, to see if any boards have been added or removed since the instrument was switched off.

Note that the instrument must be switched off before fitting or removing a pcb. If the number or type of boards is changed, and the instrument switched on again, the unit will reset, which leaves programs unchanged but sets the instrument set up to the default condition.

Board presence is checked by a software sub-routine. A DEVEN (DEVice ENable) signal is sent to each board in turn via Connector A on the motherboard. Board presence, with +5V supplied, is indicated by a PRESENT *[Bar]* signal, which is then sent to the wired-OR configuration at pin A29. All pcb connections are listed in Chapter 3.

d. The link list is checked. Learnt programs and file data are stored in several separate locations throughout memory, and are linked together by address pointers. These pointers form the link list.

If a failure is detected in step c., the instrument is automatically reset; if any other failure occurs, the instrument is initialized.

Note. If the INITIALIZED or RESET messages appear for no obvious reason, or the instrument is behaving irrationally, run the self-test program.

4 BREAK

The BREAK key does not initiate any self-test procedures. Its function is primarily to interrupt various activities of the instrument, as described in Table 3.1 in the Operating Manual.

5 THE "SELF TEST" FACILITY

The power-up and initialise routines already described do not give the user any detailed diagnostic information on faults found. A much more rigorous test can be made with the self test facility. For this, TEST is commanded, either from the front panel or remotely.

The pcbs tested (with appropriate Section references) are listed below.

a. The processor, pcb 22 (6.1 through 6.8)

b. The synthesizer, pcb 18 (6.9)

c. The h f synthesizer, pcb 16 (6.10)

d. The generator, pcb 15 (6.11)

e. The h f generator, pcb 14 (6.12)

f. The analyzers, pcb 10 (6.13 through 6.15)

g. The analyzer controller, pcb 17 (6.16)

h. The front panel (6.17)

As the self-test and initialisation software is stored mainly in the ROMs on processor pcb 22, a fault on this pcb may prevent the self-test routines working correctly.

5.1 SELF TEST FROM THE FRONT PANEL

To initiate the self-test sequences from the front panel (which must, of course, be fully working) press the SELF TEST hard key, then the TEST soft key.

Once started, TEST continues automatically until either:

a. the sequence terminates with no fault found, in which case the display shows TEST PASS, or

b. a fault message is displayed, as explained in Section 5.2.

The TEST sequence requires some user intervention:

a. A horizontal line of dots is displayed, This line rolls downwards automatically until all display pixels are lit. This allows you to check for short- and open-circuits in the display unit and associated circuitry. The pattern repeats indefinitely to allow a thorough visual inspection. When satisfied that the display is correct, press ENTER.

b. A vertical line is displayed and moves across the display from left to right, allowing you to check for short and open circuits in that plane. When satisfied that the display is correct, press ENTER.

c. Two lines of characters are displayed:

ABCDEFGHIJKLMNOPQRSTUVWXYZ ; Ω∫@ % ω # Π Δ Θ ↑ ↓ = [ ]

+ - */0123456789abcdefghijklmnopqrstuvwxyz

When satisfied that the display is correct, press ENTER.

d. A message is displayed:

"Press all keys, ending with the ENTER key"

number of keys pressed =

As each key is pressed, a number following the "=" sign is incremented by one, and an abbreviated note of the key name is displayed. Press ENTER to end the sequence. The message displayed is then either of the form :

TEST PASS ISS: nn CAL: ww/yy @ GB - F

where nn represents a number which indicates the issue state of the instrument's software; ww = week; yy = year and the final four characters; the location.
or:
a fault message, as explained in section 5.2.

failure is registered, it may be because other components have prevented the specific

The operation of the front panel interface, which drives the display, is described in Chapter 5, Section 1.

5.2 FRONT PANEL FAULT MESSAGES

The software for the self-test sequence is divided into a series of sub-routines, each of which tests a particular section of the instrument. Each sub-routine has an associated fault message, which appears on the display if that particular fault is found.

The fault messages are listed in Section 6, where each appears as a sub-heading accompanied by a test description. The sub- headings are given in in test sequence order.

The '?TS' and 'Fail Code' numbers refer to the remote control operations, and are explained in sections 5.4 and 5.5.

5.3 SELF TEST FROM REMOTE CONTROL

To start the test sequence via the remote control ports:

1. Send the code ' TT0' for TEST.

2. Allow 2 seconds delay for the instrument to complete the test.

(Code TT0 also starts the display test sequence, but this is not relevant in remote control operations. The horizontal line of dots is left rotating until the next command is received, whereupon the display automatically reverts to normal).

3. Send the query code ' ?TS0', to get the test result:

'0' = no fault; '1' = fault found.

5.4 REMOTE CONTROL FAULT MESSAGES

The self-test software for remote control is the same as that for front panel operations. Fault messages are still displayed, whilst the results of individual tests are stored in memory. When the reply to ?TS0 is '1', i.e. a fault has been found, further details can be obtained by sending further query codes, e.g. ?TS1, ?TS2, etc, as listed in Section 6.

Sections 6 and 7 below describe the tests in the order in which they are applied. Each test appears under the heading of its respective fault message, as presented on the display. Each heading also includes the test query code, in brackets.

The instrument actions one query code at a time and retains the reply to the last query only. Therefore the reply to each query must be read before the next is sent. If the approximate area of the fault is known, only those query commands relevant to that area need be sent.

5.5 FAIL CODES

When the self-test sequence finds no fault, '0' is stored in memory, and is sent in reply to the test query. A fault, however, is indicated by a number from 1 to x, according to the degree of detail that the test can yield. These numbers (fail codes) are shown against the relevant query code headings in Sections 6 and 7.

It must be emphasised that where the fail code description refers to a specific component or group of components, these are the items that the software is attempting to test. If a failure is registered, it may be because other components have prevented the specific

ones working correctly, e.g. a defective ACIA may cause the ROM under test to be incorrectly addressed and hence appear faulty. Where situations like this may occur, the text accompanying each fail code not only defines the specific components being tested, but also gives a list of other components which, if defective, may cause the same fault to be indicated. In order to keep the lists of possibly defective components within reasonable limits, it is assumed that the fault has been traced to a particular pcb, and therefore, as a general rule, only components on that pcb are listed.

Note that if TT0 has been commanded remotely, any query codes from ?TS10 onwards will automatically receive the reply 0, regardless of the fault state of the instrument.

6 SELF-TEST DETAILS

This section describes the individual tests in the self-test sequence and gives the meaning of the test result codes. These tests are intended to test mainly the digital circuitry in the instrument. Diagnostics on the analogue circuitry are best done by taking actual measurements and by swapping pads.

6.1 EPROM FAIL (?TS2 = 1 to 6)

A fault has been detected during checksum tests on the four read- only memories, ICs 25 to 28 inclusive, on the processor (pcb 22).

Fail Codes:
Bd 22

1 indicates probable failure of IC25
2 " " " " IC26
3 " " " " IC27
4 " " " " IC28
5 " " " " IC25
6 " " " " IC28

Other possible cause: IC7 or IC29

6.2 RAM FAIL (?TS1 = 1 to 5)

A fault has been detected during the following sequence:

1 " " " " IC14
2 " " " " IC15
3 " " " " IC16
4 " " " " IC17
5 " " " " IC18

A non-destructive test on the 5 Random Access Memories, IC14 to 18 inclusive, on the processor (pcb 22). The RAMs are scanned one address at a time and any data already in the current address is transferred temporarily to a register in microprocessor IC1.

The number AA_H (10101010_2) is then written to and read from the current address, followed by the inverse number 55_H (01010101_2). The original data is then transferred back from the microprocessor register, and the next RAM address called up.

A checksum test is performed on the learnt programs.

A link list, as explained in Section 3d is checked.

Other than the RAMs themselves, IC8 may be faulty.

6.3 TIMER FAIL (?TS3 = 1)
Indicates a probable fault in IC111 on pcb 22 during the following test:

A number is written into the three timer registers, which then commence counting. After a fixed delay the Timer registers are checked to ensure that the count is complete.

Other ICs which may be faulty are IC109, IC125 or IC105.

6.4 PROG. MEMORY FAIL (?TS1 = 1)
Checksum test on the programs held in RAM. Linked list test on these programs.

Try initialising memory first of all, if the problem persists then it indicates a fault on one of the following :-

Fault : Battery or ICs 14,15 or ICs 7,8 and 9

6.5 NV PROG. MEMORY FAIL (?TS1 = 2)
Checksum test on the programs held in EEROM. Linked list test on these programs.

Problem may be caused by turning power off with unit in "Supervisor" mode. Fault can be cleared by pressing "Initialise" with the unit in "Supervisor" mode. If fault persists after this, then this indicates a hardware fault on the following components:-

Fault: IC21 or IC 7,8,9.

6.6 GPIB FAIL (?TS4 = 1)
Indicates a probable fault in IC113 on pcb 22.

This results from a partial test in which the numbers AA_H, then 55_H are written to and read from the register section.

Other possible causes: IC105 and IC124.

6.7 SET-UP FAIL (?TS1 = 1)
Checksum test on the set-ups held in RAM.

Try initialising memory first of all, if the problem persists then it indicates a fault on one of the following :-

Fault: IC 18 or ICs 7,8 or 9.

6.8 NVSETUP FAIL (?TS1 = 2)
Checksum test on the set-ups held in EEROM

Problem may be caused by turning power off with unit in "Supervisor" mode. Fault can be cleared by pressing "Initialise" with the unit in "Supervisor" mode. If fault persists after this, then this indicates a hardware fault on the following components:-

Fault: IC19 or ICs 7,8 or 9.

6.9 SYNTH. FAIL (?TS7 = 1)
Indicates a fault on the synthesiser (pcb 18).

Fault: Pcb 18 not present, or IC1 is defective.

6.10 HF SYNTH FAIL (?TS8 = 1)
Pcb not present, or IC301 failed.

6.11 GEN. FAIL (?TS5 = 1)
Indicates a fault on the generator pcb 15.

Fail Codes:

1 Pcb 15 not present, or IC1 or IC6 failed.

6.12 HF GEN. FAIL (?TS6 = 1)
Pcb not present or IC102 or IC103 failed.

6.13 CH.1 FAIL (?TS9 = 1)
A write/read test has failed on RAM IC114 on analyser 1 (pcb 10). The test is similar to that applied to the processor RAM (see Section 6.2). Other than the RAMs themselves, the fault may be due to IC101, 106, 204, 113.

6.14 CH.2 FAIL(?TS10 = 1)
As for 'CH.1 FAIL' in section 6.13 but on Analyser 2 (pcb 10).

6.15 CH.3 FAIL (?TS15 = 1)
Current analyser on 1260 only.

6.16 CTRL FAIL (?TS11 = 1 to 6)

There is a fault on the analyser control pcb (pcb 17).

Fail Codes:

1 Pcb 17 is missing, or there is a fault on IC100 or IC101.

2 The analyser control circuitry has not been set to IDLE. The idle state is indicated by address 3B00 containing 00, and should appear after the following sequence:

1. FF_H written to address 3B01.
2. FC_H written to address 3B00.
3. $6C_H$ written to address 3B00.

The fault may be due to IC2, 101, 103, 104, 113, 118, 122, 123, plus any fault which causes the cycle counter to run.

3 The analyser control circuitry has failed to start a measurement, after the following test sequence:

1. 28_H written to address 3B00.
2. 68_H written to address 3B00.

After a delay produced by a repeated loop instruction in the microprocessor, address 3B00 should contain C1.

The fault may be due to IC2, 101, 102, 103, 104, 112, 113, 118, 121, 122, 123, plus any fault that prevents the cycle counter running.

4 The carry bit has not been removed, or the measurement is no longer enabled, after the following test sequence:

1. E8 written to address 3B00.
2. 68 written to address 3B00.
3. Address 3B00 checked for 40.

The fault may be due to IC101, 103, 104, 113, 118, 122, 123.

5 The measurement has not been stopped, or the microprocessor has not been notified by FIRQ.

The microprocessor checks for these conditions by waiting 3 milliseconds after completion of the previous test, then examines address 3B00 for 81.

The fault may be due to IC2, 104, 112, 113, 117, 118.

6 The measurement has not been disabled, or the carry has not been removed, after the following test sequence:

1. E8 written to address 3B00.
2. 68 written to address 3B00.
3. Address 3B00 is checked for 00.

The fault may be due to IC101, 103, 104, 113, 118, 122, 123.

6.17 FRONT PANEL FAIL

This message indicates a fault in the front panel interface circuitry. The faults which may occur are listed below, each under its respective query code and fault number.

?TS12 = 1 After waiting for a predetermined time, the main microprocessor, on pcb 22, has received no reply to a self-test instruction sent to the front panel microprocessor, IC101. Alternatively, the reply has been corrupted and is not in the expected format.

Other than IC101 itself, the fault may be due to ROM IC111 or RAM IC113, or to a defect in any of the components connected to the front panel address and data buses,or in the connections to the front panel.

?TS13 = 1 to 2 A fault has been found during write/read tests made by the front panel microprocessor on its RAMs. The tests are similar to those described for the pcb 22 RAMs in Section 7.2.

Fail Codes:

1 Microprocessor internal RAM is faulty.

2 External RAM IC 113 is faulty. The fault may also be due to IC 107, 108, 102, 103, 104, 105

?TS14 = 1 A fault has been found during the checksum test made by the front panel microprocessor on its ROMs (IC111, 112, and 113). As well as the microprocessor itself, and the ROMs, the fail codes given below may also be due to defects in IC 107(d), 108 (e,f) 114(a,d), 102, 103, 104, 105(a).

7 THE PROCESSOR PCB LEDS.

Four LEDs are mounted along the top edge of the Processor pcb 22. One of the functions of these LEDs is to light up in sequence as the tests comprising the TEST routine are made. The sequence is shown in the table below.

If the instrument is unable to complete one of the tests for any reason, ie, it cannot achieve a valid pass or fail result, the routine cannot terminate correctly and a lock-out condition may occur. In this event, the state of the LEDs indicates the last completed test.

D104 MSB	D103	D102	D101 LSB	COMMENTS
0	0	0	0	EPROM test starte
0	0	0	1	EPROM completed
0	0	1	0	RAM test completed
0	0	1	1	Timer test completed
0	1	0	0	Program memory/GPIB tests completed
0	1	0	1	SET UP memory test completed
0	1	1	0	Synthesizer test completed
0	1	1	1	HF Synthesizer test complete
1	0	0	0	Generator completed
1	0	0	1	HF Gen completed
1	0	1	0	Analyser tests complete
1	0	1	1	Analyzer control tests complete

Chapter 5
Board Descriptions

1 FOREWORD

Chapter 5 contains information on individual printed circuit boards. Where appropriate, a simplified block schematic diagram is included.

Throughout the text, a *'[Bar]'* convention is used, where applicable, to indicate an active Lo state of a signal line ,eg:

FIRQ*[Bar]*

(the active Lo Fast Interrupt Request)

This is identical to:

$\overline{\text{FIRQ}}$

(The latter will be found more usually on the schematic diagrams that accompany the circuit descriptions).

In addition, some of the 1255-60 cicuits include signals whose active states are implicit in their titles, eg:

R/WBAR

2 FRONT PANEL INTERFACE (PCB 2)

2.1 INTRODUCTION

Refer to Circuit Diagram 12607502, Sheets 1 to 3.

The front panel interface permits local operation of the instrument via its front panel keyboard and display.

The interface scans the keyboard for commands, encodes these into ASCII format, and sends them to the main processor via a serial link. Analysis data, operator messages, and softkey menu data, received back from the main processor via the serial link, are decoded from ASCII into display format to produce the appropriate characters on a vacuum fluorescent display.

Fig. 5.2.1 is a block schematic diagram of Pcb 2.

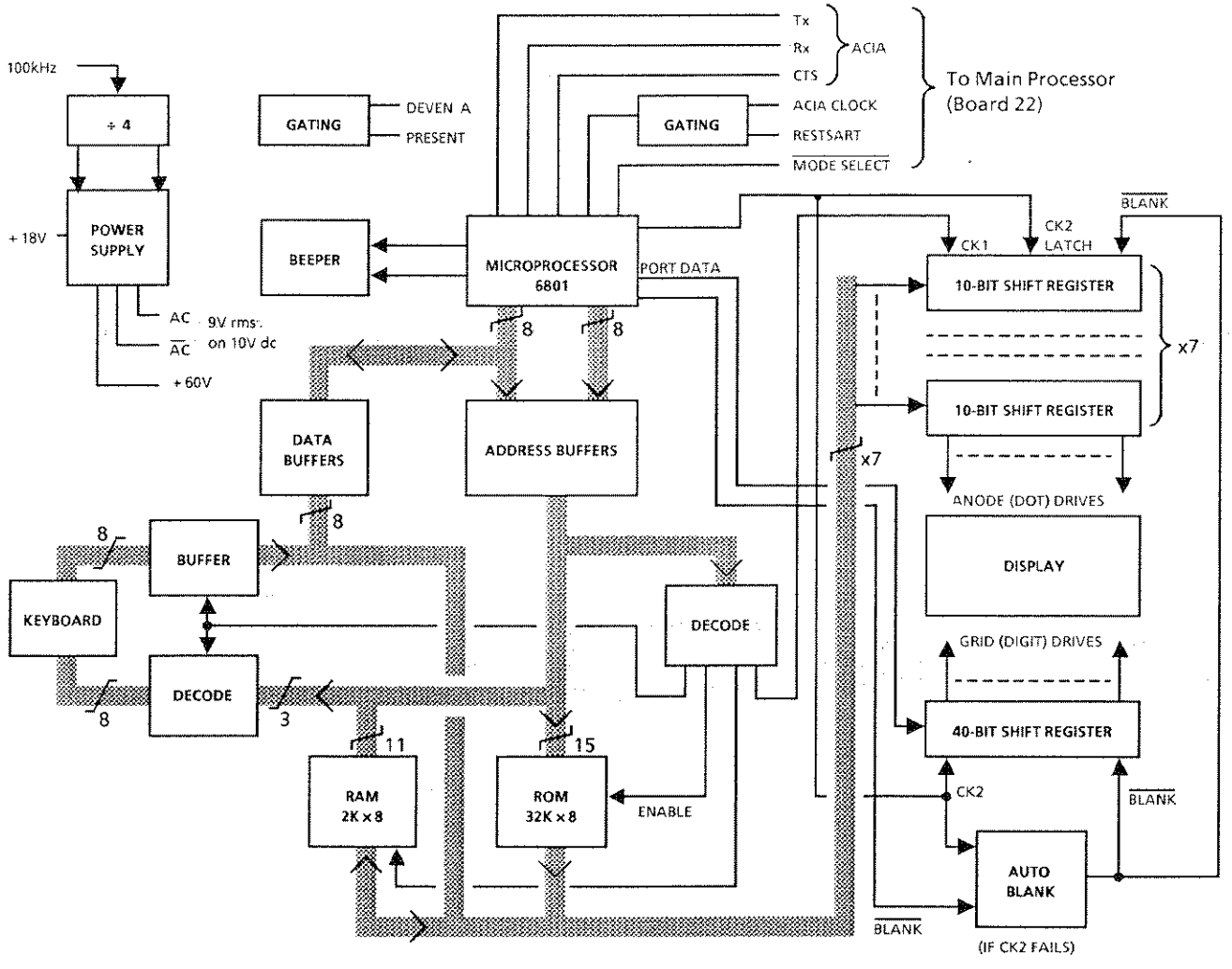


Fig 5.2.1 *Front Panel Interface*

2.2 MICROPROCESSOR CONTROL

All data transfers through the front panel interface are processed by the type 6801 front panel microprocessor. The microprocessor program is contained in a 32k × 8-bit ROM. An integral 128 × 8-bit RAM serves as a scratchpad memory and where

necessary, this is augmented by a separate 2k × 8-bit RAM. The primary function of the 2k× 8 RAM is for data buffering.

The keyboard and display logic is treated by the microprocessor as simply another memory area and the associated location addresses are are to be found on the device control map (see Table 5.2.5e on Page 5.9). Timing for the display refresh logic is controlled by a 16-bit programmable timer within the microprocessor. Display refresh gating signals and PORT DATA are output through the I/O port. The timer and the I/O Port are each accessed through the microprocessor 'on-chip' registers.

Communication between the front panel interface microprocessor and the main processor takes place via a serial link. This link is serviced at the front panel end by an asynchronous serial interface within the front panel microprocessor. A CTS (Clear To Send) is routed to the main processor via bit 7 of the I/O Port. The serial interface, also, is accessed through an 'on-chip' register.

2.3 MEMORY ADDRESSING

Table 5.2.5 includes memory maps defining the various areas of memory used by the front panel microprocessor. Each area is enabled by a unique block decode that is performed on address bits A3, A6, A7, A14 and A15 by Address Decode. Address bits A0 to A13 are commonly used by all memory areas to select individual memory locations.

2.4 KEYBOARD INTERROGATION

The keyboard contains a matrix of pressure-activated keys, as listed in Table 5.2.1. Each row of keys is enabled in sequence by the keyboard enable signals W0 through W7, which are selected through the *[Bar]* KEYEN locations in the Device Control Area. When a key is activated it causes the related keyboard output, A to H, to go Lo (0V). The outputs of unactivated keys are maintained Hi (+5V).

Keyboard Inputs	A	B	C	D	E	F	G	H
W0	F1	F2	F3	F4	F5	Select Up	Select Down	-
W1	Generator Menu	Analyzer Menu	Sweep Menu	Display Menu	Plotter Menu	Data Output	Scale Limits	Status
W2	Recycle	Single	Sweep Hold	Plot	Plotter Axes Menu	View File	Vernier	Store Recall
W3	Exp.	Clear	6	9	5	8	4	7
W4	Enter	±	-	3	. (Dec. Pt.)	2	0	1
W5	Self-test	Pause Cont.	Execute	Learn	Break	Local	-	-
W6	-	-	-	-	-	-	-	-
W7	-	-	-	-	-	-	-	-

Table 5.2.1 *Keyboard-matrix Switch Relations*

2.5 DISPLAY OPERATION

The vacuum fluorescent display of the front panel interface contains 40 pairs of characters, as shown in Fig 5.2.2. Each character is in the form of a dot matrix comprising 5 x 7 individually controllable elements. The elements are excited by the display logic to produce the required character.

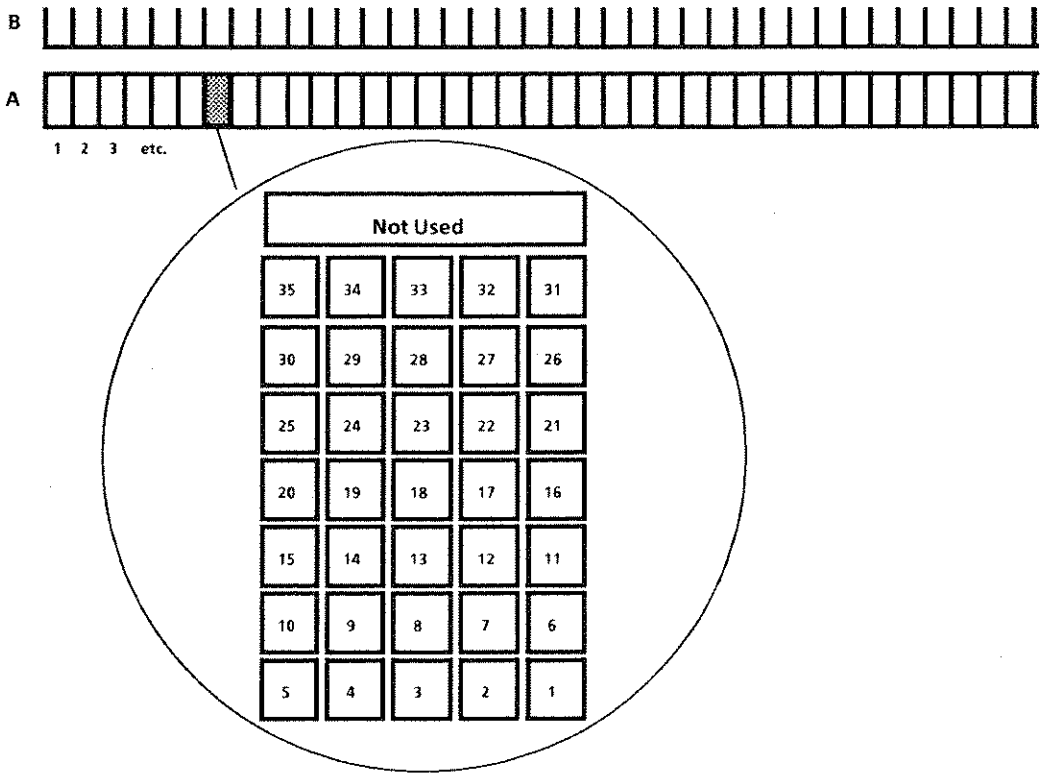


Fig 5.2.2 *Display Configuration.*

The general construction of the display is shown in Fig 5.2.3, which views the top left hand corner of the display from the front. Each dot matrix comprises 36 phosphor coated anode plates, formed on an insulating anode base. In front of each matrix pair is a wide mesh grid and in front of the grids are the cathodes, comprising 6 low temperature filaments at approximately 700 °C.

Characters are enabled by making the associated grid positive (+50V) with respect to the cathode, or disabled by making the grid negative (-10V). Individual dots are made to fluoresce by making the anode potential positive (+50V) with respect to the cathode. Dots required not to fluoresce have the anode potential made negative (-10V) with respect to the cathode.

Display characters are selected by the PORT DATA held in a 40 bit shift register. The port data contains 39 logic '0's, and a single logic '1' that is shifted at a frequency of approximately 80Hz to enable each pair of display grids in succession. The selection frequency of 80Hz is sufficiently high for the viewer's persistence of vision to make it appear that all characters are displayed simultaneously. ANODE (dot) data, for the character pair to be excited, are held in seven 10 Bit Shift Registers. The outputs of these registers are common to all character pairs. Each of the anode data registers holds the data relating to a specific pair of dot matrix rows, as shown in Fig 5.2.4.

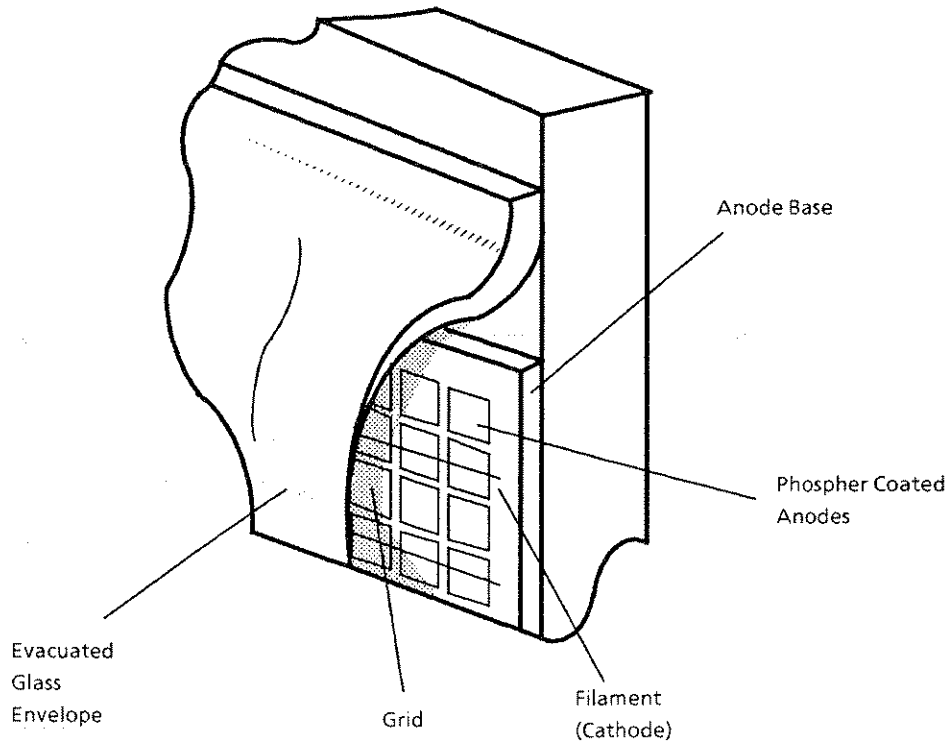


Fig 5.2.3 *Display Construction*

2.6 DISPLAY REFRESH TIMING

The timing of the display refresh sequence is shown in Fig 5.2.5. For each character pair, 10 CK1 pulses are required to enter the dot column data into the seven 10-bit Shift Registers. This data is intended for the next character pair in the selection sequence.and does not yet appear at the register outputs. After the tenth pulse, the blank signal is asserted to disable the currently selected GRID output. A CK2 pulse then occurs to latch the new anode data at the register outputs and to increment the contents of the PORT DATA register (0 Bit Shift) so that the next character pair is enabled. The *[Bar]* BLANK data signal is then negated to excite the anodes in accordance with the anode data.

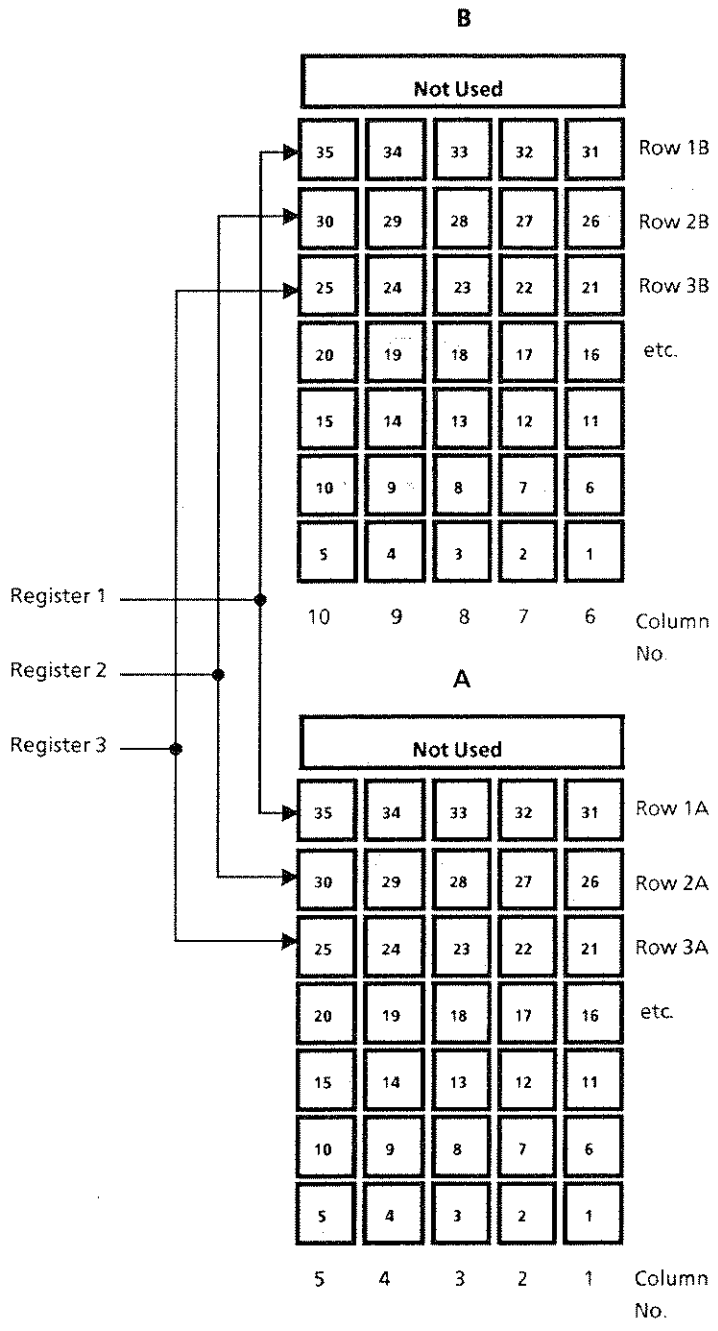


Fig 5.2.4 *Anode Data Storage.*

a. Primary Map

Address Range	Function
0000-001F	Special On-chip.Reg.
0020-003F	Not Used
0040-007F	Device Control
0080-00FF	On-chip RAM
0100-3FFF	Not Used
4000-7FFF	External RAM (IC113) 2kx8
8000-FFFF	External ROM (IC111) 32kx8 or 16kx8 selected by split pads A&B

b. I/O Port 1 Address 0002

Title	Pin	Read/ Write	Function
BEEPER *[Bar]*	0	W	Beeper Output
DIAG	1	W	Diagnostics Indicator
CK2	2	W	Display Ground Shift
SELF TEST	3	R	Initiate Self Test
PORT DATA	4	W	Display Grid Data Output
BLANK *[Bar]*	5	W	Display Blanking
CLICK	6	W	Click Output
CTS	7	W	Clear to Send

c. Device Control Map

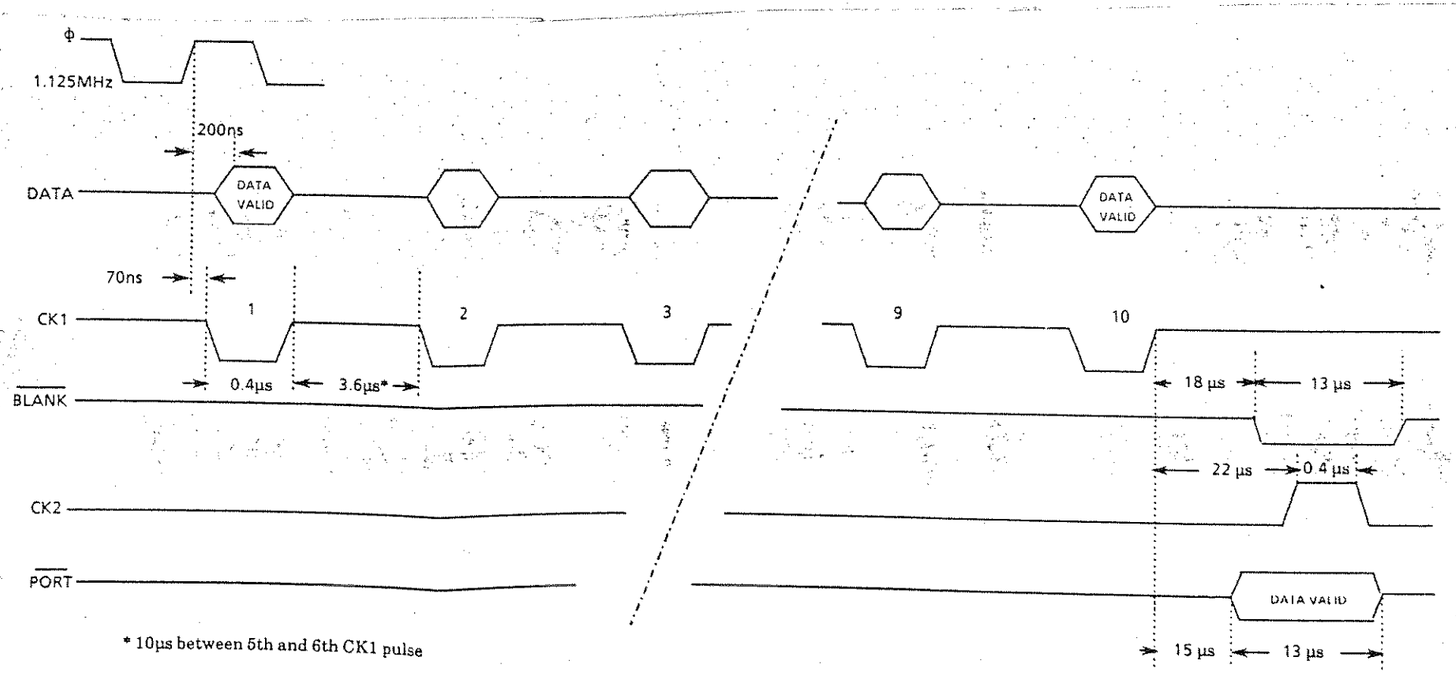
Name	Address	Read/ Write	Function	Address Range	Approved Address Range
CK1	0XXX XXXX 01XX 0XXX	W	Display Anode Data	0040 or 0041 or 0042 etc	0040
KEYEN [Bar]	0XXX XXXX 01XX 0XXX	R	Keyboard Scan and Data Enabled		0048-004F

d. I/O Port 1 Address 00002

Title	Pin	Read/ Write	Function
BEEPER *[Bar]*	0	W	Beeper Output
DIAG	1	W	Diagnostics Indicator
CK2	2	W	Display Ground Shift
SELF TEST	3	R	Initiate Self Test
PORT DATA	4	W	Display Grid Data Output
BLANK *[Bar]*	5	W	Display Blanking
CLICK	6	W	Click Output
CTS	7	W	Clear to Send

e. Device Control Map

Name	Address	Read/ Write	Function	Address Range	Approved Address Range
CK1	0XXX XXXX 01XX 0XXX	W	Display Anode Data	0040 or 0041 or 0042 etc	0040
KEYEN [Bar]	0XXX XXXX 01XX 0XXX	R	Keyboard Scan and Data Enabled		0048-004F



* 10µs between 5th and 6th CK1 pulse

Tables 5.2.5 a. to e. *Memory Maps*

3 POWER FAIL DETECT (PCB 5)

3.1 INTRODUCTION

Refer to Circuit Diagram 12607505,

The power fail detect board, Pcb 5, monitors the ac input supply of the instrument.

Within 10ms of the supply failing or being switched off, the POWER FAIL output of Pcb 5 is taken Lo, viz, 0V, to alert the main processor. The main processor then has 5ms to perform its power fail routine. When the ac supply returns, or the instrument is switched on again, a delay of >200ms occurs before the POWER FAIL output is taken Hi. This allows the dc supplies of the instrument and the synthesiser crystal oscillator to settle before the main processor begins the power up routine.

3.2 CIRCUIT DESCRIPTION

Operational amplifier IC1a compares the outputs of a pair of full wave rectifiers, D1/D2 and D3/D4, each of which is driven by the centre-tapped transformer T1. The output of D1/D2 charges capacitor C4 and therefore provides a reference voltage (via zener diode D5) for the inverter input of amplifier IC1a. The same rectifier output also provides the dc supply for Pcb 5. A period of >10ms without an ac supply is reflected at the output of rectifier D3, D4 and allows the non-inverting input of amplifier IC1a to approach 0V. This causes the output of amplifier IC1a, and hence the output of amplifier IC1b, to also approach 0V, switching FET TR1 on. This action causes the POWER FAIL output to go Lo.

On power up, the R-C network R6, R7 and C2, at the non-inverting input of amplifier IC1b, allows a delay of >200ms to elapse before the POWER FAIL output is taken Hi.

Note On some 1255-60 models, the power fail detect circuit is located on the power supply unit pcb.

4 HIGH FREQUENCY ANALYZER: VOLTAGE INPUTS (PCB 10)

4.1 INTRODUCTION

Refer to Circuit Diagram 12607510, Sheets 1 to 7.

The high frequency analyzer converts the voltage signal to be analyzed into digital form and under the control of the analyzer controller (Pcb 17), stores the resultant data in an onboard RAM. The digital data are subsequently retrieved for analysis by the main processor. High frequency demodulation signals for frequencies > 655.35Hz are received from the HF synthesiser (Pcb16). A block diagram of the analyzer is shown in Fig 5.4.1

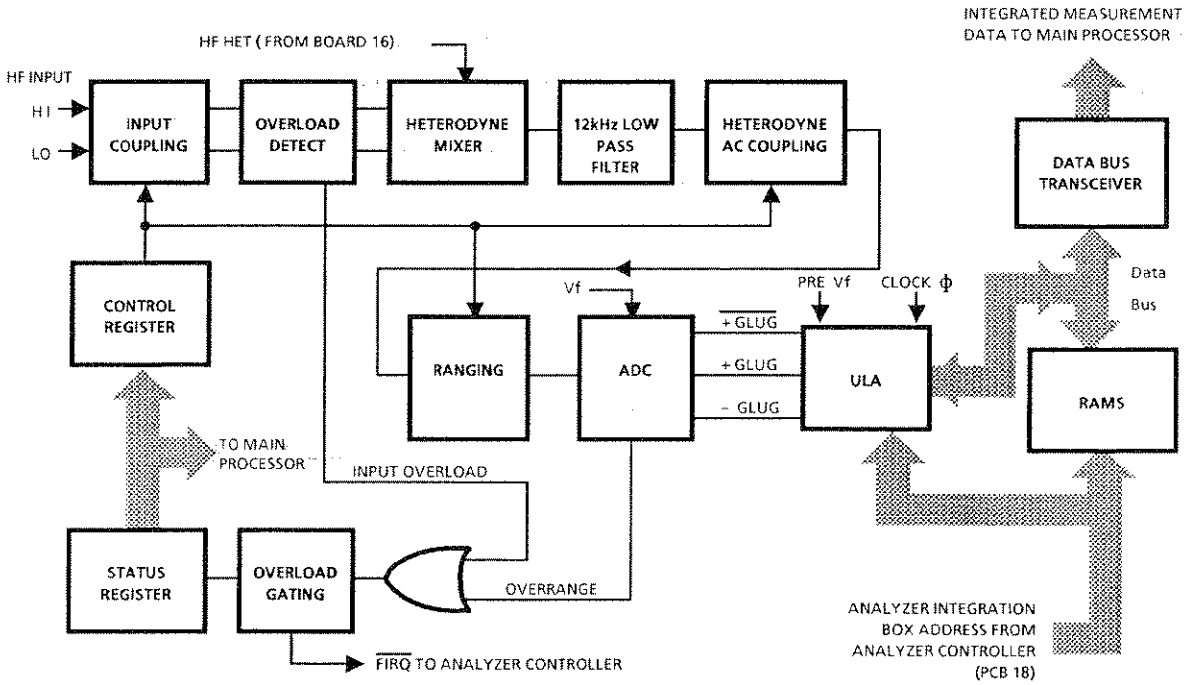


Fig. 5.4.1 *High Frequency Analyzer*

4.2 AC/DC COUPLING (Sheet 4)

Input coupling is selected via relays RL401 and RL402, with the relays energized for dc coupling. The relays are controlled from the D4 input to the Analyzer Control Register (ACR) resulting in DC/AC BAR 1 and DC/AC BAR 2. outputs from relay driver IC209 (Sheet 2).

For frequencies > 65.536kHz, ac is automatically selected.

4.3 SINGLE / DIFFERENTIAL INPUT (Sheet 4)

The signal input configuration, either single or differential, is selected via relay RL403. This relay is controlled by the D2 input to the ACR. When D2 is present, SINGLE is output to the relay via driver, IC 209.

4.4 FLOATING / GROUNDED SHIELDS (Sheet 4)

The input shield configuration, either floating or grounded, is switched via relay RL404. This relay is controlled by the D3 input to the ACR. A D3 input results in a SHIELD output to the relay via driver IC209 (Sheet 2).

4.5 OVERLOAD DETECTION (Sheet 5)

An overload is registered either by a logic '1' on the HETOL1 output of IC 504a or by a logic '0' HTL2BAR output from IC503a . Both signals are routed to the overload detection circuit (Sheet 7), where they produce an OVERLOAD signal. This signal is routed to IC207 (Sheet 2) to cause a fast interrupt request (FIRQ *[Bar])* which is routed, via the motherboard, to the microprocessor on Pcb 22.

4.6 OVERLOAD PROTECTION (Sheet 4)

Overload protection against high inputs is provided by TR401, D401 and D402 and for low inputs, by TR403, D405 and D406. These components limit the input swing to approximately ± 5V with respect to ground.

4. 7 HETERODYNE OPERATION (Sheet 4)

The Hi and Lo input signals are buffered and applied across R435 in such a way as to produce a current difference in the drains of dual FET TR405 equal to:

$$(V_{Hi} - V_{Lo})/1500 \text{ amps}$$

The diodes of IC406 are driven by a squarewave signal, derived from Pcb 16, which contains a component at the frequency $F_o - F_m$

F_m = analyzer measurement frequency.

(Above 65535kHz F_m is always fixed at 393.216Hz.)

The driven diodes switch the anti-phase currents in the drains of TR405 to the input of filter IC407 and produce at the filter output (TP402) a signal which has a component at the analyzer measurement frequency F_m. Most of the other products of this mixing process are attenuated by the filter, before being rejected by the correlation process of the analyzer.

The gain of the mixer stage at the frequency F_m, depends partly on the feedback of filter IC407 and partly on the heterodyning used to convert the frequency F_o to F_m. Table 5.4.1, shows the relationship between F_o and F_m, and the mixer gain, for each generator output frequency range. Note however that the peak voltage of the mixed signals at test point TP402, is always twice the peak input voltage.

4.8 HETERODYNE COUPLING (Sheet 6)

Above 1.1MHz, ac coupling is used to remove any dc offset caused by the HF Mixer (heterodyne). Selection of either ac or dc coupling is via relay RL 601, which is controlled by the ACR D1 input. The input to relay RL601, HETC, is via driver IC209. (Sheet 2).

Table 5.4.1 *Mixer Characteristics*

F_0 Range	Frequency Ratio	Mixer Gain
$F_0 < 300Hz$	F_0	2
$300 \leq F_0 < 655.36Hz$	$F_0 \div 31$	$4 \div \pi$
$655.36 \leq F_0 < 6553.6Hz$	$F_0 \div 61$	$4 \div \pi$
$6553.6 \leq F_0 < 32768Hz$	$F_0 \div 199$	$4 \div \pi$
$32768 \leq F_0 < 65536Hz$	$F_0 \div 251$	$4 \div \pi$
$65.536 \leq F_0 < 32MHz$	393.216Hz	$4 \div \pi$

4.9 RANGING

To keep within the input range of the analyzer's analog-to-digital converter (ADC) viz, 600mV (2 x 300mV), the signal for analysis is passed through an amplifier/attenuator chain (Sheet 6). The gain settings of this combination are selected by the main processor, via data lines D5, D6 and D7, which sets range bits R0, R1 and R2 of the ACR, IC201 (Sheet 2). Details are given in Table 5.4.2.

Table 5.4.2 *Range Settings & Bit Codes*

				Range Codes		
Range	Atten (R2)	Gain (R1)	Gain (R0)	R2	R1	R0
30mV	×1	×10	×1	0	0	1
300mV	×1	×1	×1	0	1	1
3V	×0.1	×1	×1	1	1	1

If the input voltage is too high for the range selected, the analyzer sets the 'overrange' bit (bit 0) in the analyzer status register to logic '1' and sends the FIRQ*/Bar/* signal.

During autorange selection, the main processor selects the most sensitive range that will not result in an overrange reaction. The overrange indicator bit is cleared by the main processor on 'read'. Further interrupts are inhibited until the overload is gated and bit 1 on the control register is set Lo.

Table 5.4.3 below summarises the settings of the analyser control register, IC201 (Sheet 2). The use of this register is described in Sections 4.1 through 4.8.

Table 5.4.3 *Analyser Control Bit Settings*

Bit	'1'	'0'	Function
D0	Enable O/L on FIRQ	Clear O/L in status register	Overload signal enable and clear
D1	Disable [HETC]	Enable [HETC]	AC coupling select; above 65.535kHz
D2	Single	Differential	Single or diff. input select
D3	Grounded	Floating	Grounded or floating sig. shields select
D4	DC	AC	AC/DC coupling select. (Always ac above 65.535kHz)
D5	×1	×3	R0 input amp gain
D6	×1	×10	R1 input amp. gain
D7	×0.1	×1	R2 input amp. atten.

4.10 ANALOG-TO-DIGITAL CONVERSION

The analyzer's analog-to-digital converter (ADC) uses a 'voltage-to-time' conversion technique.

A forcing waveform V_F, applied to one input of an integrator, gives the sawtooth waveform shown in Fig 5.4.3. This waveform is compared with two reference levels (+50mV and -50mV) to produce positive and negative 'glug' pulse trains from the comparator outputs. The difference between the widths of positive and negative glugs is directly proportional to the input voltage. To obtain a time count representative of the input voltage the glug pulses are used to gate the clock input (ϕ) to a counter. The clock count, accrued over a defined period, is a measure of the voltage applied to the ADC input

To ensure that the integrator output is dynamically balanced about zero, the glug pulses are also fed back to a current switching network at the integrator input. This network produces a switched reference current at the integrator summing junction, which exactly balances the input signal current.

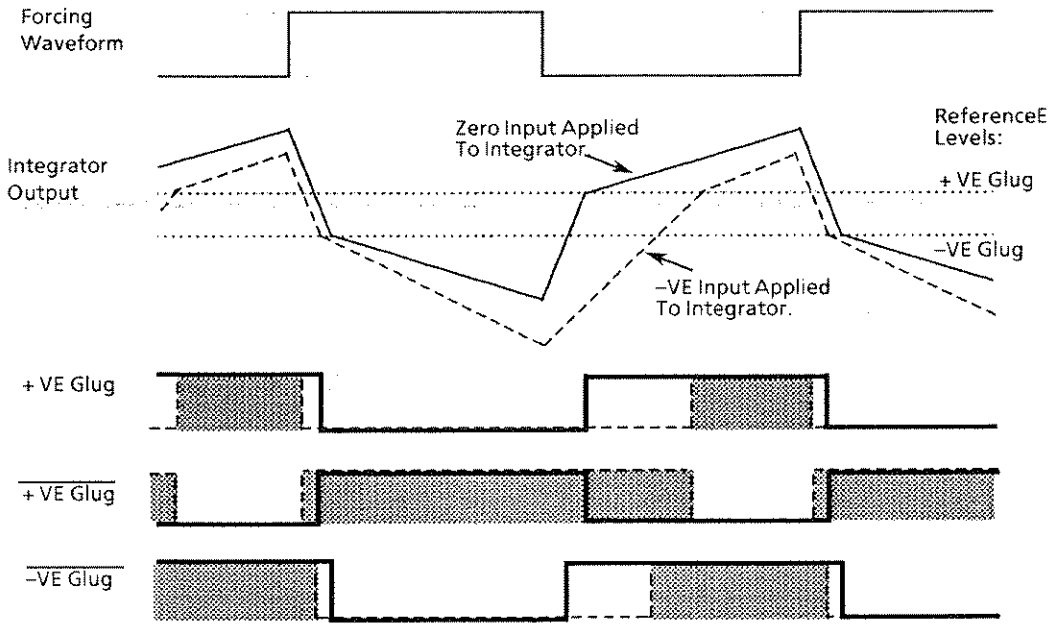


Fig 5.4.2 ADC Waveforms.

With zero volts applied to the ADC input, the sawtooth swings between approximately +300mV and -300mV and is symmetrical about the zero line. Hence the positive and negative glug pulses have the same width (shown by bold lines in Fig 5.4.2). A positive or a negative voltage applied to the ADC input displaces the sawtooth and produces a corresponding variation in the glug pulse widths. The shaded area in Fig 5.4.3 represents the glug states with a negative input to the integrator. The difference between the negative and positive states is detected by gating the glug pulses together and using the resultant waveform as an enabling envelope for a 12-bit clock counter (ULA).

There are three discrete states for the glug outputs. These are shown in Table 5.4.4 overleaf.

Table 5.4.4 *Glug Output States*

Integrator Output	-Glug [Bar]	+ Glug [Bar]	+ Glug
< + ve ref. level	Hi	Hi	Lo
zero level	Hi	Lo	Hi
< -ve ref. level	Lo	Lo	Hi

4.11 UNCOMMITED LOGIC ARRAY (ULA)

The ULA consists of a glug gate controlling the clock input to a 12-bit counter. Clock pulses are counted until a PRE V_f signal arrives to latch and preset the counters. The PRE V_f signal triggers the external control circuit to accumulate the 12-bit result in RAM using an 8-bit adder.

A block diagram of the ULA is shown in Fig 5.4.3 below:

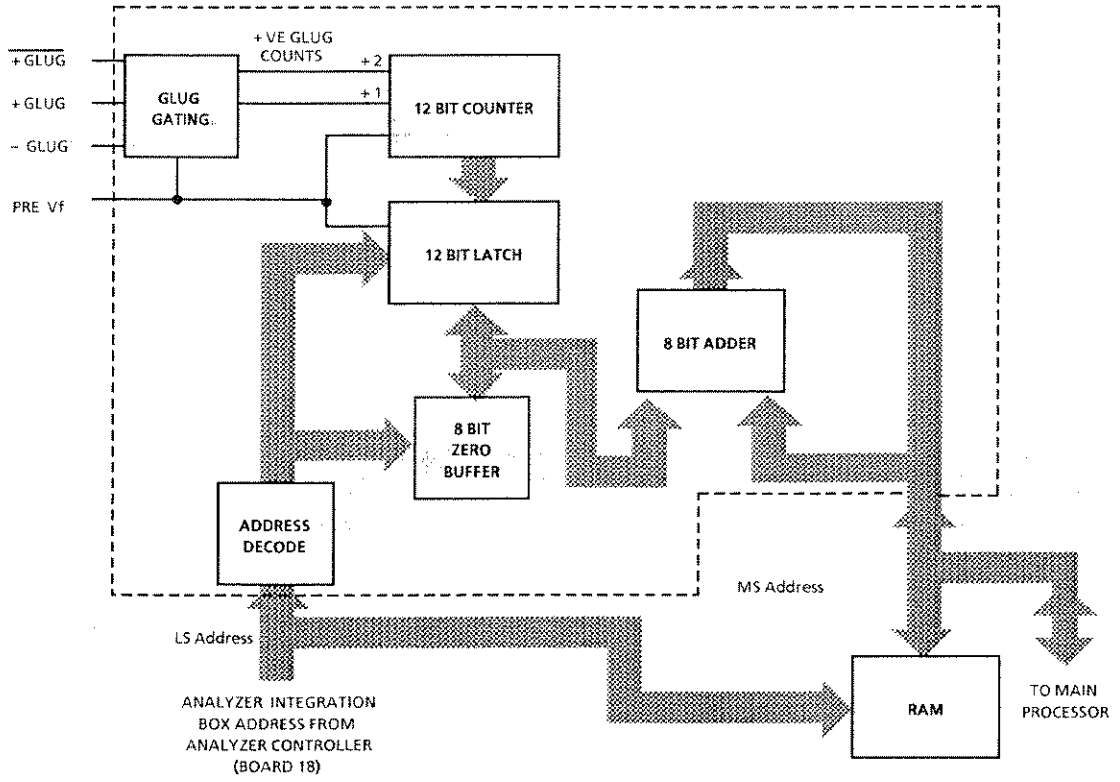


Fig 5.4.3 *ULA Operation*

4.12 MEASUREMENT INTEGRATION

The composition of a measurement result is shown in Fig 5.4.4. The result consists of 104 blocks of glug counts: each block is accrued over a one hundred and fourth of the period of analysis and is stored in a uniquely addressable 'box' in the analyzer RAM. These are the discrete time-based data from which the main processor computes the analysis result.

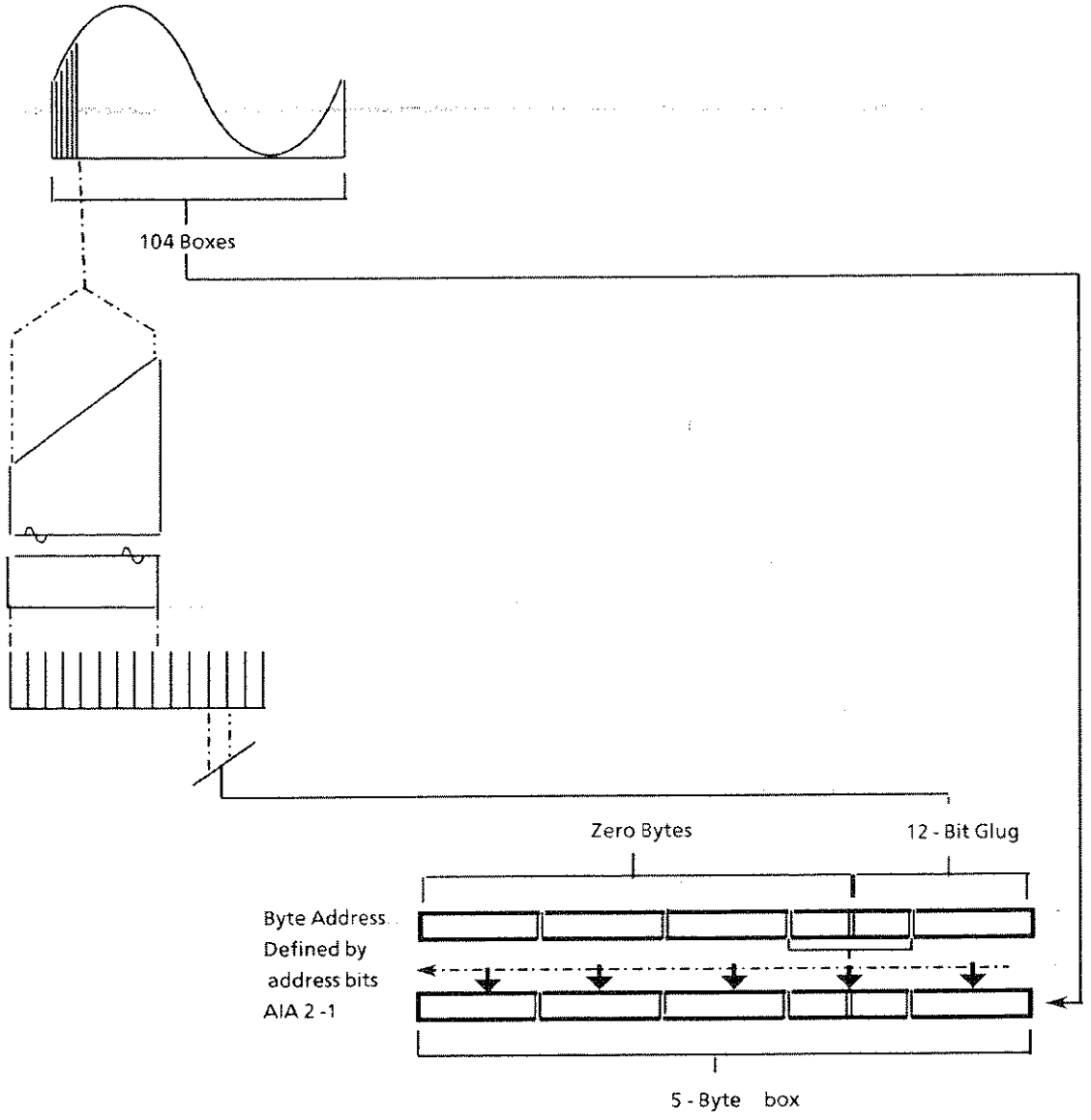


Fig 5.4.4 *Measurement Integration*

For each cycle of analysis, each analyzer RAM box contains a number of PRE V_f defined glug counts. The number of counts varies according to the frequency of analysis. At a frequency of 300Hz for example, there are 3 counts, whilst at a frequency of 3Hz, there are 300 counts.

Prior to a measurement, each RAM box is set to zero by the main processor. The measurement begins when the analyzer receives a measurement enable signal,

MEASEN *[Bar]*, from the analyzer controller, together with the first box (and byte) address.

The capacity of each RAM box is five 8-bit bytes. Byte addressing is used in transferring the glug counts from a 12 bit latch, via an 8 bit adder, to the selected box. The sequence is shown in Fig 5.4.6.

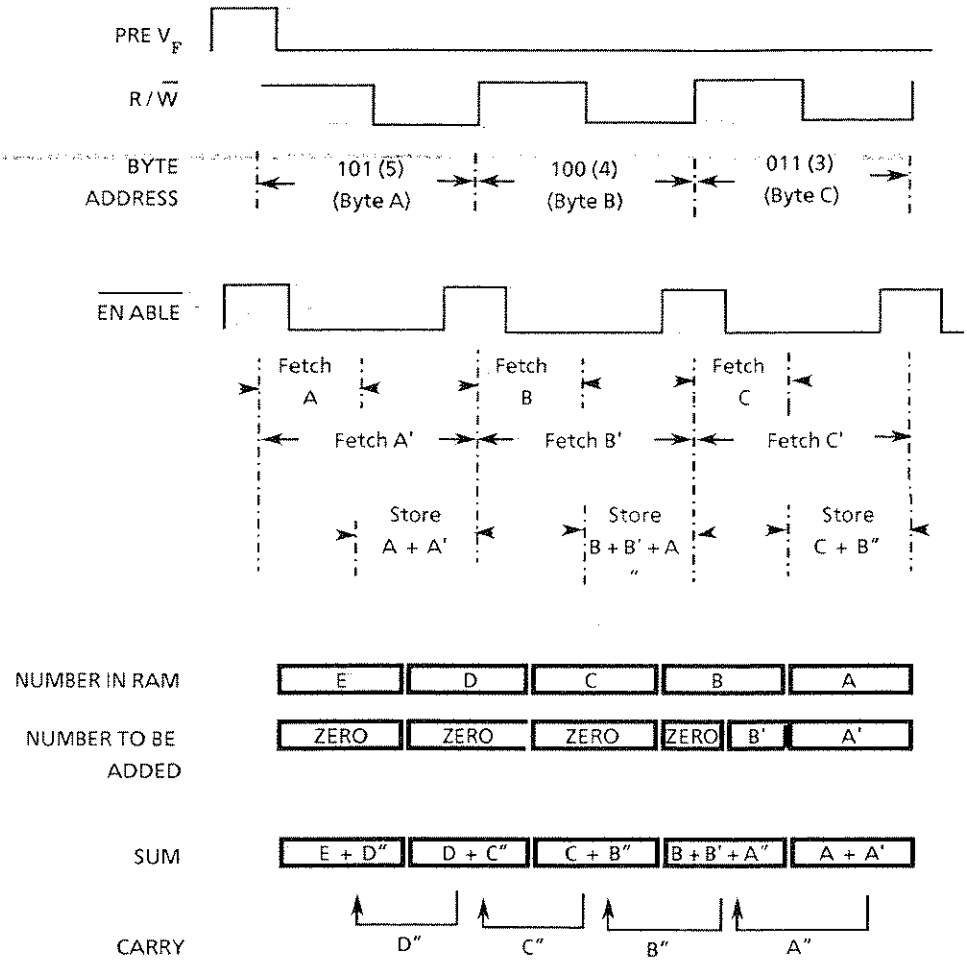


Fig 5.4.5 *RAM Read/Write Sequence*

Following a SET 0 pulse, together with a PRE V_f pulse, the analyzer controller outputs the address of the least significant byte in the first box (Box 0) and holds the R/*W[Bar]* line Hi (= read analyzer RAM). After an address settling delay, the controller takes the MEASEN *[Bar]* line Lo to enable the RAM, this allows the value held in the least significant eight bits of Box 0 and the value held in the glug clock counter to be added and stored by the adder. Whilst maintaining the same box/byte address, the controller then takes the R/W*[Bar]* line Lo. This allows the value stored in the adder to be written into the RAM and completes the transfer of the first byte of glug data.

The RAM read/write sequence continues, as shown in Fig 5.4.5, by adding the value contained in the four most significant bits of the glug count latch to the second byte of Box 0, together with any carry from the first addition. Since the most significant byte of the glug count contains only four bits, the remaining four bits are made up by the 8 bit zero buffer, which is addressed at the same time as the analyzer RAM.

The remaining three bytes of Box 0 have zero added to them from the zero buffer, together with any carry from the previous add operation.

For each subsequent PRE V_f pulse the byte addressing cycle is repeated and carries are passed from byte to byte by the adder.

At the end of each box period the analyzer controller increments the box address to start filling the next box.

Measurement integration continues for the number of cycles that the main processor writes into the 'cycles' count register of the analyzer controller. If only one cycle is specified, the measurement will stop when the 104th box is filled. If 'n' cycles are specified, then the box address is returned to zero at the end of each successive analysis cycle, thus allowing glug counts to be accrued as shown in Fig 5.4.5.

The main processor accesses the data stored in the analyzer RAM by taking the appropriate RAME*N[Bar]* (RAM enable) line Lo, addressing the RAM via the analyzer controller, and strobing the RAM with the ST*R[Bar]*/CLK line.

5 HIGH FREQUENCY GENERATOR (PCB 14)

5.1 INTRODUCTION

Refer to Circuit Diagram 12607514, Sheets 1 to 7.

The high frequency generator (Pcb 14) is simply a wide-band amplifier at the generator output that provides power amplification for signals from the low frequency Generator (Pcb15) and the high frequency synthesiser (Pcb 16). The amplifier has a floating output; differential currents are produced to give an output voltage or current which may be referenced to any voltage within the compliance range of the output stage. In the context of Pcb 14, the terms 'high frequency' and 'low frequency' refer to frequencies above and below 65kHz respectively.

5.2 DIGITAL CONTROL AND STATUS SECTION

Refer to Sheet 1.

Control signals for the relays on Pcb 14 are stored in register IC101. Two other ICs, IC107 and IC109, shift the levels of the control signals while IC108 drives the relay coils.

The remainder of the digital section gives overload warning to the system. If either a common mode overload (COM MOD OL*[Bar]*) or a generator overload (GOPOL *[Bar]*) occurs (or is cleared) then IC105A or IC105B is clocked to the state Q = Lo. This results in a Lo FIRQ *[Bar]* signal, which indicates to the system that an event has occurred on one of the boards. The system then polls each board in turn to find the one which has registered the event.

The FIRQ*[Bar]* signal stays Lo until the system responds by taking READ/WRITE BAR high and DEVEN4 Lo. This prompts the board to take two actions. First, the S *[Bar]* inputs to IC105A and IC105B are taken Lo, forcing their outputs Hi to release FIRQ*[Bar]*. Second, the output buffers of IC102 are enabled, giving a '1' or '0' as appropriate. IC104A applies a '1' to the 7D input of IC102 to show that a FIRQ has been made. A '1' at the 2D input of IC102 indicates a common mode overload, whilst a '1' at the 3D input indicates a generator overload.

5.3 VOLTAGE-TO-CURRENT CONVERSION

Refer to Sheets 2 and 3.

The circuits on Sheets 2 and 3 convert single-ended voltage signals to differential current signals for low and high frequencies respectively.

Low frequency signals are referenced to a dc bias voltage, BIAS 5 VFS, through IC204 and TR201. RL201 feeds low frequency signals to IC202. When the circuit is working with high frequencies the low frequency input (i.e. the input to IC202) is clamped to ground.

The voltage difference between the positive inputs of IC202 and IC201 is level shifted to give the same voltage difference between the positive inputs of IC205 and IC206. This results in a redistribution of the currents flowing through TR210 and TR211, such that the current from the left current source decreases by 2mA/V (where V is the voltage difference between the input to IC202 and the BIAS 5VFS input) and the current from the right current source increases by the same amount.

For the high frequencies, the signal input to the base of TR302 causes an increase in the collector current of between 0.3mA/V and 3.0mA/V, depending on frequency. The

collector current of TR305 decreases by the same amount. These signal currents are capacitively coupled to two fixed current sinks, comprising essentially IC302 / TR307B and IC303 / TR307A . The current sinks are cascaded by TR306A and TR306B respectively.

The voltages of the signal current source are monitored by a pair of limit detectors. Detector D302-D307, TR308 responds to voltages higher than +3V, whilst detector D308-D313, TR309 responds to voltages lower than -3V. If either condition arises the COM MOD OL *[Bar]* signal goes Lo and flags an error warning to the system.

5.4 HF AGC LOOP

Refer to Sheet 7.

Board 16 provides the loop with a high frequency input signal of approximately constant amplitude (560mV rms). This signal is applied to R701 and TR701, which form an input attenuator. The attenuator, which has increased linearity due to the network TR702, R704, R707 and C702, is controlled by a dc voltage from the amplitude comparator.

IC703 and IC704 form an amplifier with a gain of -100, whose output follows two paths. On one path the signal amplitude is compared with the amplitude of the low frequency (reference) input. The dc voltage which results from IC702 is dependent on the difference between the two amplitudes. This voltage controls the collector current through TR703, which in turn provides the control voltage for the h.f. input attenuator. The other amplifier output path is through a switched attenuator, which consists of RL701, RL702 and the R720 resistor network. An attenuation in keeping with the amplitude range of the output signal is selected by the signals AGC1 and AGC2. The three values selectable, 0dB, -20dB or -40dB, together with the 20dB variation of the low frequency input amplitude, give an overall range of 60dB.

The AGC loop continues to operate even if the output from the system is in the low frequency range, but under these conditions its output is disconnected at RL301.

5.5 OUTPUT AMLIFIER

The cicuits shown on Sheets 2 and 3 of the circuit diagram, produce the differential current signals that are needed to give a floating output; a simplified circuit is shown in Fig 5.5.1.

When I1 = I2 and I3 = I4 there should be no output voltage because I5 = I6 = 0. However, any difference between I1-I2 and I3-I4 results in a net current I5(= I6) which gives rise to an output voltage (if the generator is in voltage mode) of V(Hi)-V(Lo) = 10000*I5.

The FLOAT OFFSET potentiometer (RV302) varies the voltage of the floating ground with respect to the fixed ground. The OUTPUT OFFSET potentiometer (RV301) is used to set V(Hi)-V(Lo) = 0.

A resistor is connected between the floating ground and the fixed ground to return any difference in current between I5 and I6.

A simple schematic of the compound amplifier is shown in Fig 5.5.2; for circuit details refer to Sheets 4 and 5 of the circuit diagram.

The bias power amplifier (Sheet 5) has a dc gain of approximately ×100 (set by R503, R506 and C507) which decreases to unity for frequencies above 2Hz. The output of this amplifier provides the power rails for the signal power amplifier and so affects the

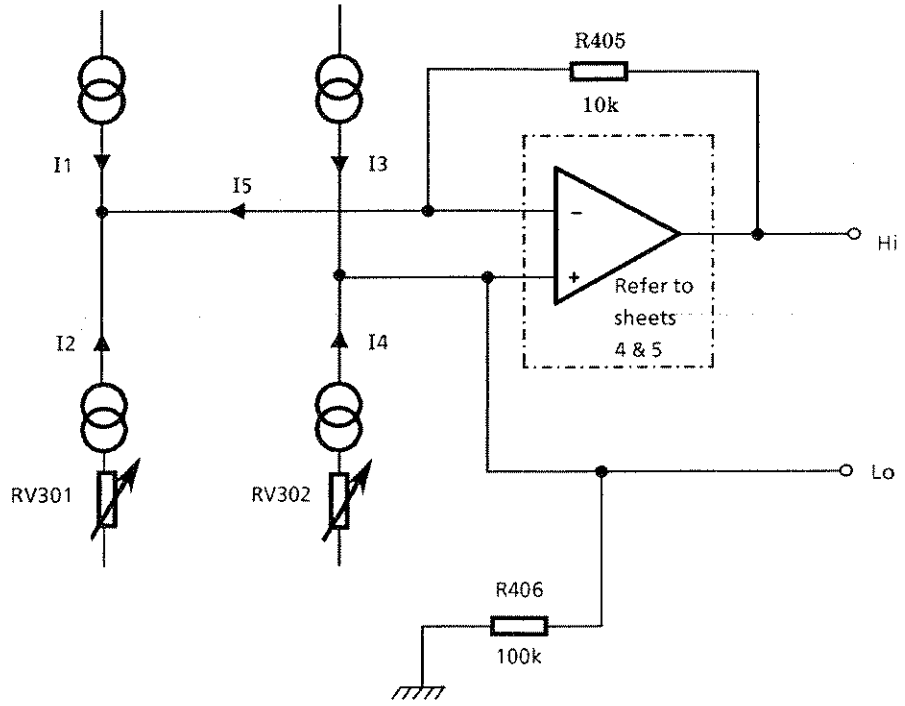


Fig. 5.5.1 *Amplifier Floating Output*

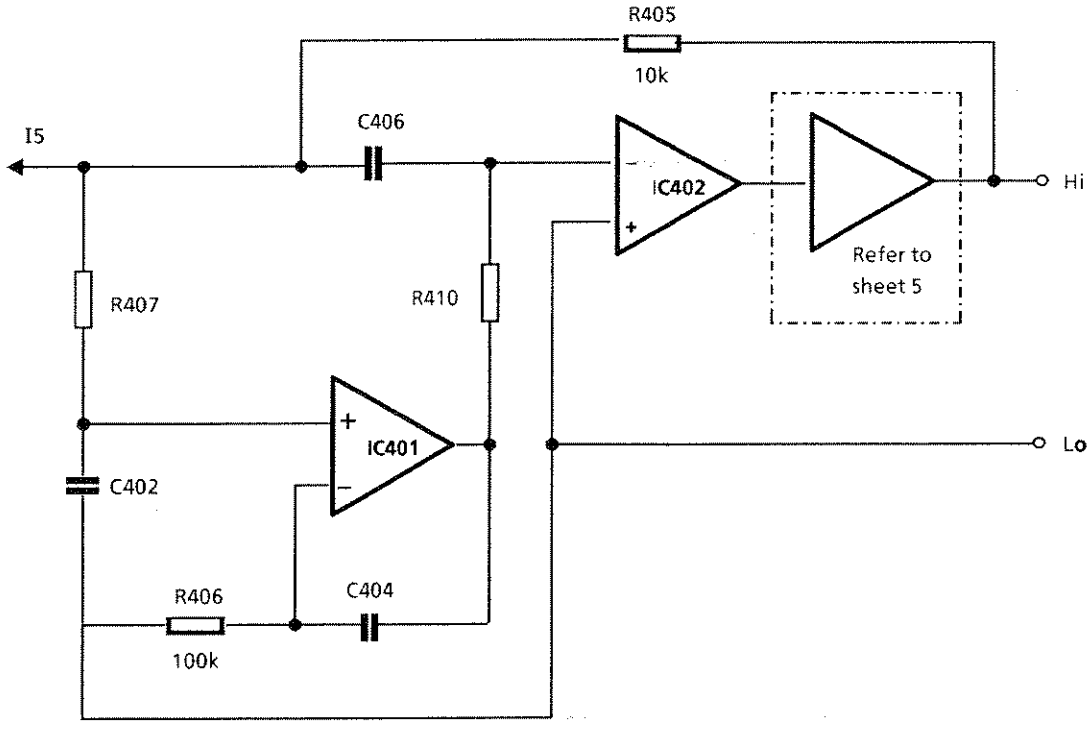


Fig. 5.5.2 *Compound Amplifier Schematic*

output of that amplifier. This allows the signal amplifier to be powered on lower supply voltages than the bias signal at the output.

In constant voltage mode, the output is defined by the 10k feedback resistor R405 whereas in constant current mode, it is defined by R404, R540 and R405.

5.6 BIAS AMPLIFIER

The section of circuit consisting of TR501, D501, D502, C505 and TR503 can be considered as an operational amplifier with a level-shifted output. Bias inputs are applied to the amplifier through R501 and are amplified by a factor of 100 at dc. The amplifier output drives two emitter follower stages, whose output levels are displaced by approximately 15 volts, the the zener voltage of D503 minus $2 \times V_{BE}$. These stages power the supply rails for the signal amplifier. This arrangement allows the range of output bias to be large whilst reducing the power dissipated in HF transistors TR 509 and 510.

5.7 SIGNAL AMPLIFIER

The signal current amplifier consists of a two-stage zero-offset complementary follower. Input signals are capacitively coupled and are applied through R514 and R518 to the bases of TR506 and TR507. These transistors in turn drive the complementary output pair TR509 and TR510. The centre point between the emitter resistors, R531 and R532 provides the zero offset output.

5.8 CURRENT OVERLOAD

Rail current is sensed on resistors R529 and R534. In the event that the current exceeds approximately 140mA, transistor TR512 or TR513 (depending on the polarity of the overload) will conduct. This will limit the base drive current to TR508 and TR511 and at the same time, shut off the current in the opto-diode part of IC 501 or 502. When this occurs, GOPOL *[Bar]* will go to a logic 0 state, an interrupt will occur and an appropriate message will be displayed.

6 LOW FREQUENCY GENERATOR (PCB 15)

6.1 INTRODUCTION

The low frequency (LF) generator produces a stimulus signal for a system under test.

To produce this signal, the LF generator receives a digital drive signal (PRE GEN), frequency range information and synchronisation signals from the synthesizer (Pcb18). The signal is power-amplified by the HF generator (Pcb14) before being applied to the system under test..

Control data from the main processor define the following generator output signal parameters:

a. stimulus signal amplitude,
b. stimulus signal waveform,
c. bias amplitude,
d. bias polarity,

A simplified block diagram of the LF generator is shown in Fig 5.6.1.

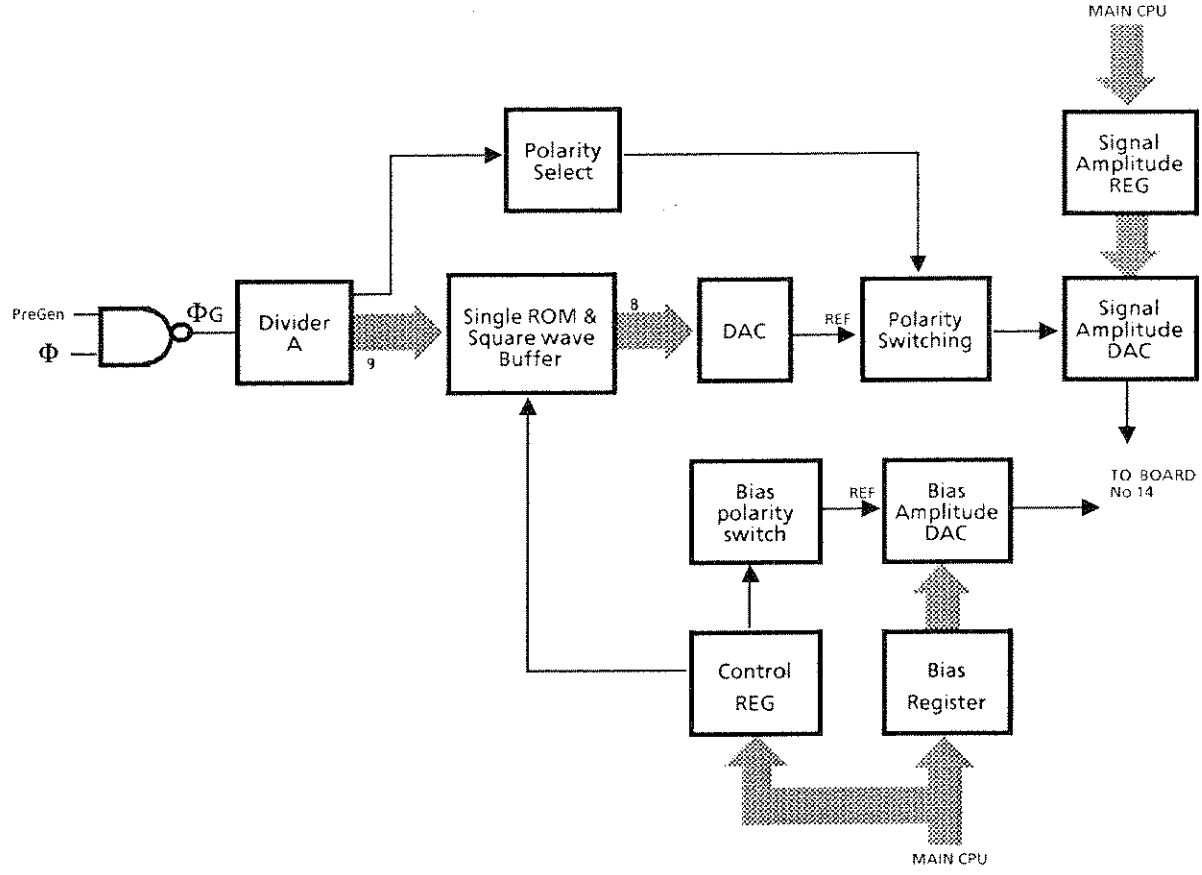


Fig 5.6.1 *Generator*

6.2 SIGNAL PROCESSING

The PRE GEN signal is gated with the clock (ϕ) signal. The resultant stream of gated clock pulses, ϕ_G is used to drive divider 'A'.

The division ratio of Divider 'A' is set in accordance with the frequency range selected in the synthesizer. (Refer to Table 5.9.1 in Sect 9). Outputs from Divider 'A' are the polarity switching signals and a sequence of 9-bit addresses for the sine ROM.

Digital sine values from the sine ROM are converted into analog form by the reference digital-to-analog converter (DAC). Since the sine ROM contains positive sine values only, the waveform of the resultant signal is uni-directional (see Figs 5.6.2a).

To obtain a signal of the correct form, with negative and positive half-cycles, the output of the DAC is processed by a polarity switching amplifier. This produces the signals shown in Figs 5.6.2b. The output of the polarity switching amplifier is applied to the reference input of the signal amplitude DAC, where it is combined with the amplitude data written into the generator amplitude register by the main processor.

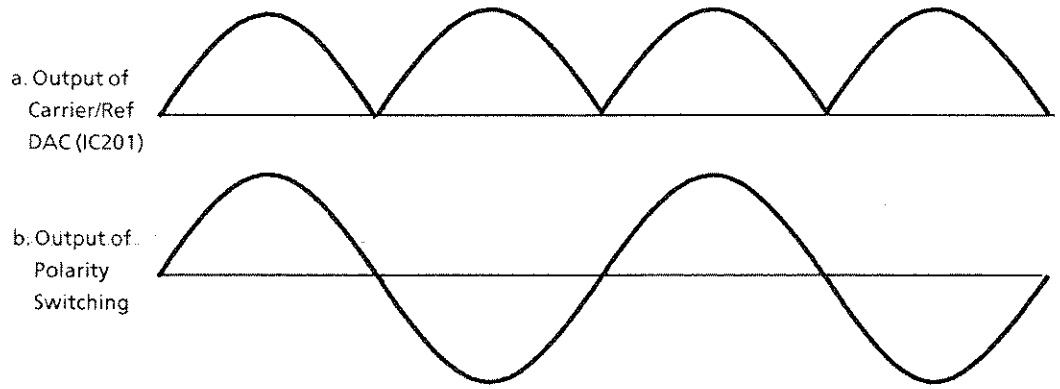


Fig. 5.6.2 *Sine Generation*

Bias and bias polarity are defined by data written into the bias register by the main processor. This data is converted into analog form by the bias DAC and the resultant 'bias' signal is output to Pcb 14.

6.3 DIVIDER 'A' OPERATION

A block diagram of divider 'A' is shown in Fig 5.6.4. The function of the divider is:

a. to address the sine ROM at a rate that will produce a stream of sine values at the required analysis frequency.

b. to provide quadrature information for polarity switching.

The sine ROM contains a single quadrant of sine data, comprising 390 positive values. These values are accessed sequentially by addressing the sine ROM from the output of an up /down counter. This produces a sequence of positive sine half-cycles, of which the alternate half-cycles are inverted in accordance with the quadrature count (see Fig 5.6.2a and b. up /down counting, also, is controlled by the quadrature count.

For each ϕ_G pulse (ϕ & PRE GEN) the value stored in the up/down counter is incremented/decremented by the addition of a preselected value from the addend ROM. The addend value is selected by the R6*[Bar]* and R7*[Bar]* lines. On frequency ranges 0 through 5, the addend value is 1. On range 6, the value is 5 whilst for range 7 and above, the addend value is 10. This gives a division ratio of 1560 for ranges 0 through 5, and 312 and 156 respectively for ranges 6 and 7. For all other ranges , the division ratio is 156. The addend and reset vaues contained in the addend ROM are listed in Table 5.6.2.

On frequency ranges 0 through 5, every sine value is accessed ; on range 6, every fifth, and on ranges $\geq$ 7, every tenth value. In each case, however, there is ample information to define the required sinewave.

Quadrant data is stored in the quadrant counter. This counter is incremented by the '=' output of a comparator that compares the contents of the up /down counter with a preselected quadrant, defining value stored in the 'end of count' ROM. The quadrant defining and reset values are listed in Table 5.6.3.

Table 5.6.2 *Addend Memory Map (IC108)*

Address	Data	Address	Data
00		19	AX
to	XX	1A	5X
08		1B	EX
09		1C	XX
to	FX	1D	5X
0B		1E	AX
0C	XX	1F	1X
0D			
to	00		
0F			
10	XX		
11	XD		
12	X9		
13	XB		
14	XX		
15	XD		
16	X9		
17	XB		

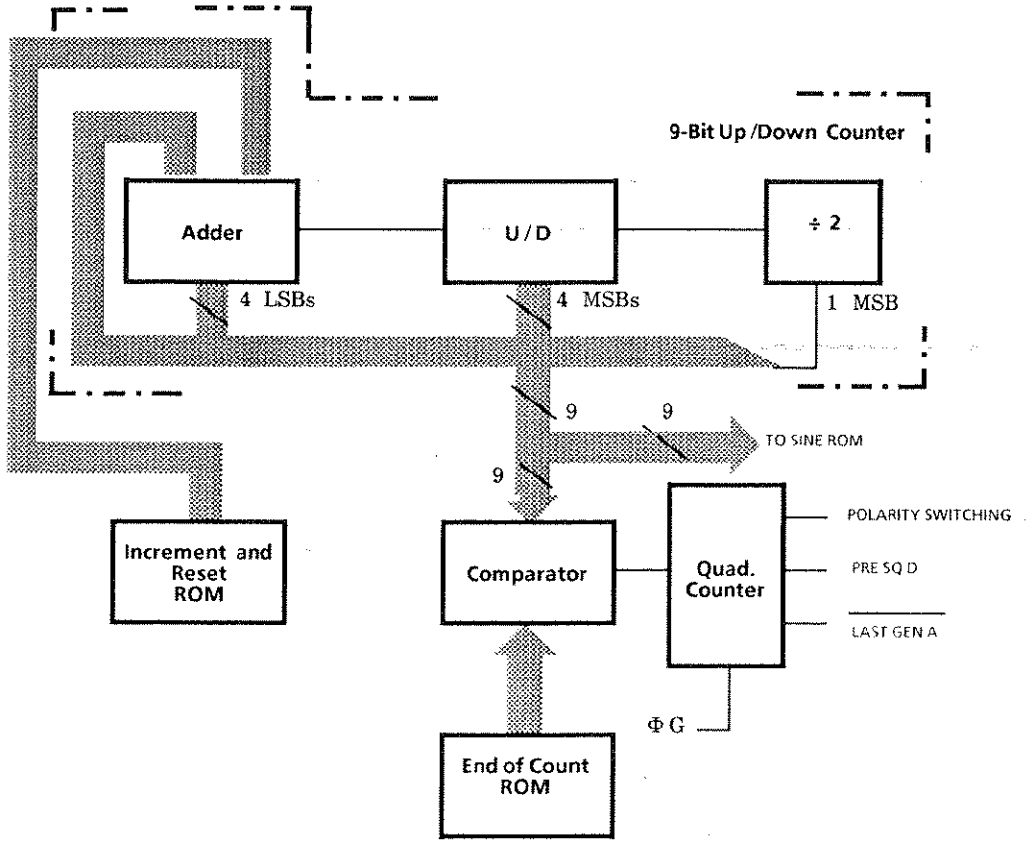


Fig 5.6.3 *Divider 'A' Detail*

Table 5.6.3 'End of Count' Memory Map (IC109)

Address	Data
00	XX
01	0D
02	19
03	03
04	XX
05	7A
06	6D
07	84
08 to 1F	XX

'X' is the 'don't care' state and is set to zero.

6.4 HF OPERATION

A reference signal is required by the HF synthesizer (Pcb 16) when operating in high frequency mode (≥65.536kHz). This sinusoidal reference signal is taken from the output of the polarity switching circuit. The signal is used as the reference input for the high frequency phase-lock loop on Pcb 16.

6.5 RELAY SWITCHING CIRCUIT

A control signal is provided for the 1260 current-to-voltage converter (Pcb 31). This signal is used to switch the 50Ω / 5kΩ range resister.

6.6 POWER SUPPLY CIRCUITS

Two floating power supply circuits are provided. One is not used, the other provides power to the 1260 current-to-voltage converter (Pcb 31).

7 HIGH FREQUENCY SYNTHESIZER (PCB 16)

7.1 INTRODUCTION

Refer to circuit diagram 12607516, sheets 1 to 4.

The high frequency (HF) synthesizer provides drive signals for the HF generator (Pcb14) and for the voltage and current analyzers (Pcbs 10 and 10 + 31 respectively).

A simplified schematic of the HF synthesizer is shown in Fig. 5.7.1.

Basically, the synthesizer consists of two phase-locked loops, a generator loop and a heterodyne loop. The first provides the drive for the HF generator and the second for the analyzers.

The range of frequencies required by the HF generator is 65kHz to 32MHz. This is obtained from the HF synthesizer by mixing the output of a 60-90MHz voltage controlled oscillator (VCO) with a crystal-controlled reference frequency.

In order to measure at these higher frequencies, the signal analyzers use a heterodyne method which mixes the signal down to a lower frequency (393.216Hz.)

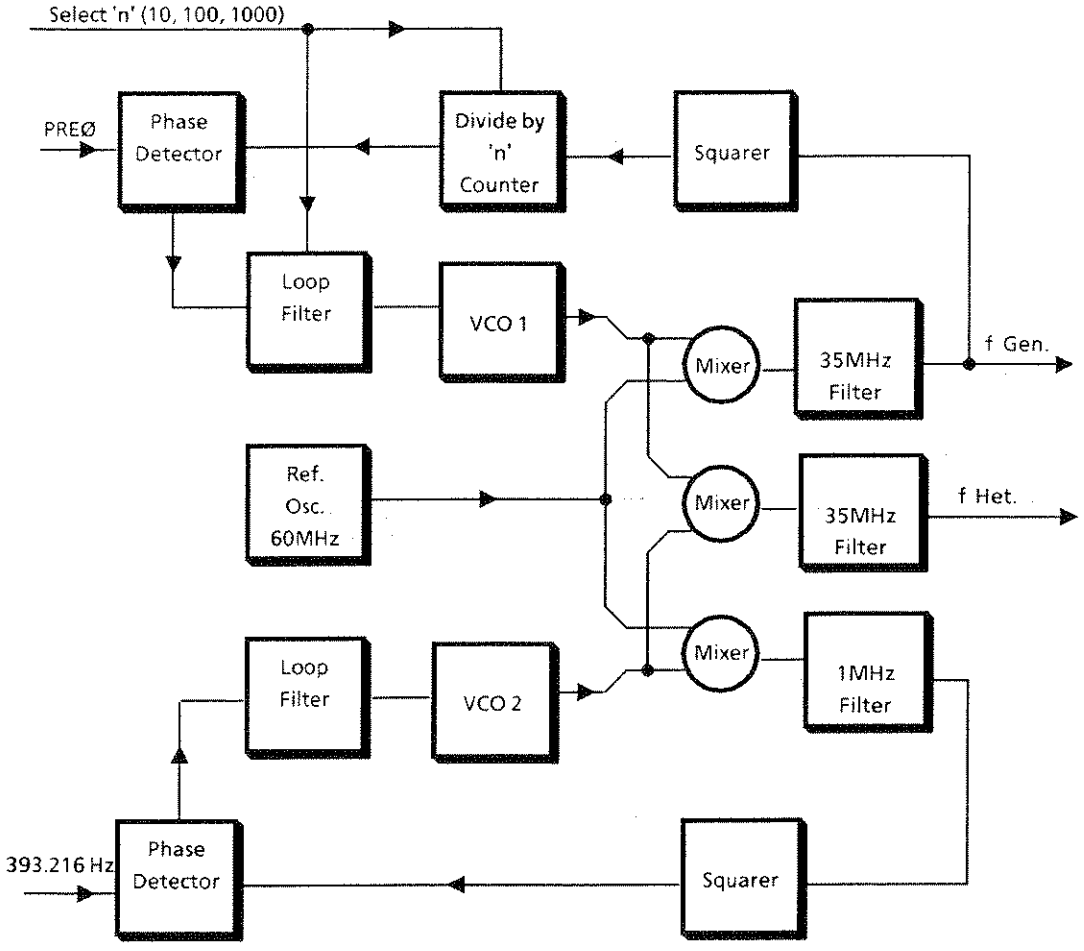


Fig 5.7.1 *H F Synthesizer Schematic.*

7.3 GENERATOR LOOP (Sheet 1)

The 60MHz reference outputs, F REF1 and F REF2, are taken to the signal input of mixer IC103 via a filter to remove harmonics; these would otherwise give rise to unwanted products in the mixer output.

VCO1 is an LC oscillator tuned by a hyper-abrupt diode, D101. The oscillator output is an ECL-type square-wave. After attenuation to appoximately 200mV p-to-p, this is fed to the local oscillator input of mixer IC103. The mixer output is filtered to remove products above 35MHz, then amplified to approximately 1.8V p-to-p by IC104. This signal is connected to the generator board via PLG. The output signal is then further amplified (× 11) by IC108 and finally squared-up to TTL levels by IC113.

In this form the signal drives decade dividers IC106 and IC 107 to give outputs 1/10, 1/100 and 1/1000. The appropriate division ratio is gated by IC109 to the input of phase detector IC105. An extended version of PRE0 is taken from IC306 and used as the reference input.

The phase detector generates positive or negative error pulses, of fixed amplitude and variable width, on pins 2 and 13 of PLG. When the frequency is locked, the width of these pulses is proportional to phase error, otherwise the output is correctly phased to enable pull-in. The pulses are combined with PRE0 to give a small offset ; this avoids the phase detector dead-band around zero. The resulting pulse is taken to the loop filter IC111b via switched input resistors which optimise the loop response for each range.

Normally the VCO frequency exceeds the reference frequency and increasing the VCO frequency increases the output frequency. However, if the VCO frequency falls below reference frequency then the reverse is true and the loop will have positive, instead of negative, feedback. The output of IC111b latches at its negative limit with the VCO frequency at minimum. Comparator IC111a detects this situation. If the output voltage falls below -10V it forces the phase detector input low, simulating a low frequency, until the filter output has regained a safe value (about -8V). In normal operation IC111/1 remains negative.

After a small amount of additional filtering by R122 and C116 the filter output becomes the control voltage for the VC0. The control voltage may be measured on TP102. A swing of -9V to + 10V gives a frequency range of approximately 60-90MHz.

7.4 HETERODYNE LOOP (Sheet 2)

The heterodyne phase-locked loop used here is simpler than that of the generator since there is no divider and the low mixer output frequency makes filtering and squaring easier. The frequency range required for VCO2 is so small that a VCXO can be used. Latch-up is prevented by TR201 driven by comparator IC206a.

7.5 RANGE CONTROL (Sheet 3)

The HF synthesizer receives control signals from the data bus in a way similar to that of other boards in the instrument. Most control signals are at TTL level but to drive the filter input range switches, comparators IC304c and IC304d are used to provide level-shifting. Similarly, IC304b enables the ECL buffers for the HF heterodyne output. When high frequency is not selected, the LF heterodyne drive from pcb17 is gated through to PLD, E and F. SP302 and SP301 select either PRE0 or a squared-up sine input from pcb15. Normally SP301 is linked. IC310 generates signals at 8kHz and 400kHz to keep the HF system running during LF operation. IC309 selects these as required.

7.6 OUTPUT MIXER AND REFERENCE OSCILLATOR (Sheet 4)

The output of VCO2 is taken to the signal input of mixer IC401. The attenuated output of VCO1 is taken to the local input of this mixer and the difference frequency, f_{het}, is taken from the output via a filter which removes frequencies above 35MHz. The triangular waveform so obtained is squared-up by ECL amplifiers which are part of IC402. For frequencies above 65.535kHz, this output is routed, via IC 403, to PLE and F and hence by cable to the Pcb10 voltage analyzers and (where applicable) current analyzer (Pcb10+31).

For frequencies below 65.535kHz, the HF drive is inhibited and IC403 is driven by the LF heterodyne signal. Note that below 655Hz, the latter is a dc level, ie, no heterodyning takes place.

The 60MHz oscillator is based on a 60MHz 3rd overtone crystal with an ECL gate. This device is used as an amplifier. The circuit is very similar to the VCXO (refer to sheet 2 of the circuit diagram) but a trimmer capacitor, CV401, is substituted in place of the varactor diode. The trimmer is adjusted to allow for tolerances of the two 60MHz crystals.

8 ANALYZER CONTROLLER (PCB 17)

8.1 INTRODUCTION

The analyzer controller receives measurement command signals from the main processor, and measurement synchronisation signals from the Synthesizer. In response to these signals, the analyzer controller provides common control signals for the analyzers .

When a measurement sequence has been completed the analyzer controller issues a fast interrupt request (FIRQ). The main processor is then able to read the measurement data from the various analyzers by accessing the appropriate analyzer RAM.

The basic operation of the analyzer controller can be followed with the aid of the block diagram below. During a measurement the analyzer controller outputs an enabling signal to the analyzers and a sequence of storage addresses for the analyzer RAMs. On measurement completion, when the main processor asserts a particular RAMEN line to access an analysis RAM, the RAM address output of the analyzer controller is inhibited and the RAM address output of the main processor is used instead.

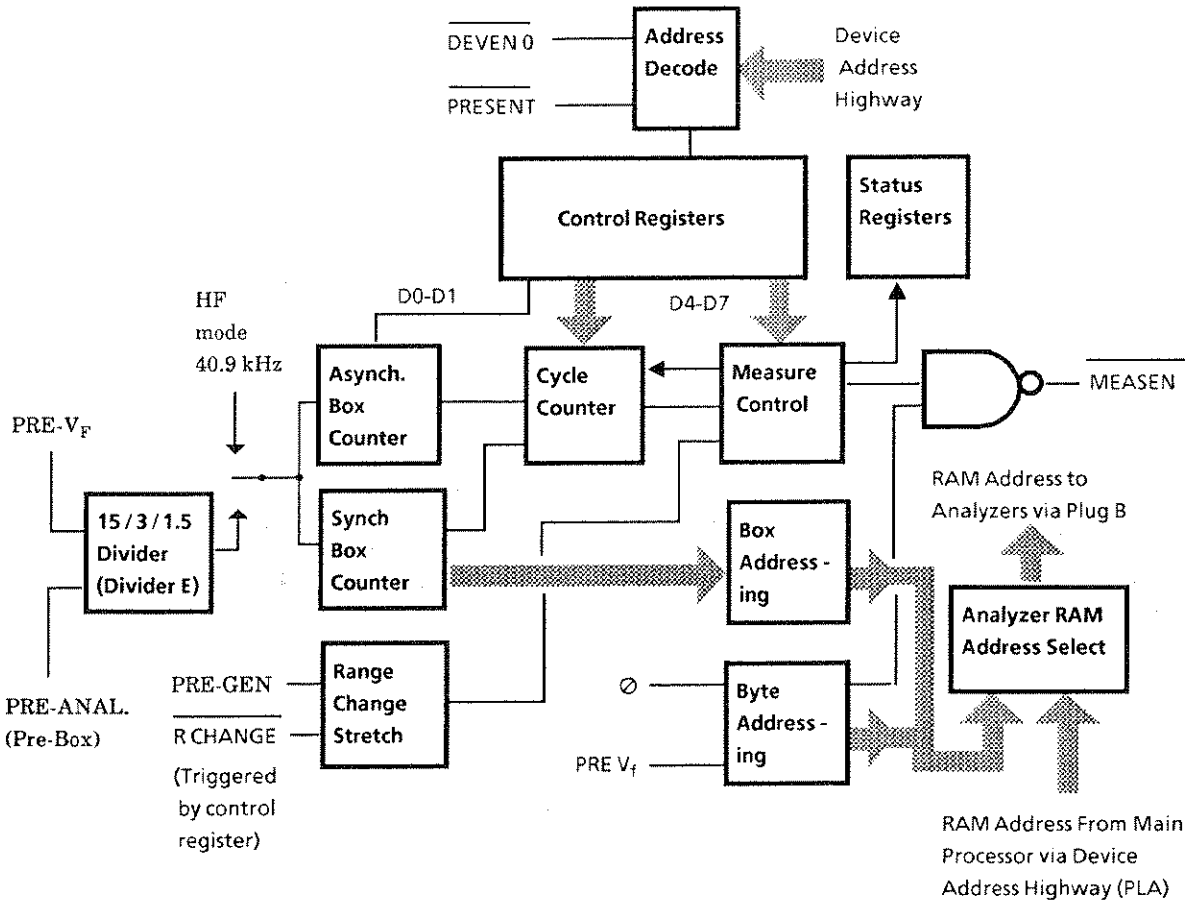


Fig 5.8.1 *Analyzer Controller.*

8.2 MEASUREMENT CONTROL

Measurements can be commanded singly or repetitively, in blocks of 'N' cycles. The number N *[Bar]* (=256-N) is written by the main processor into the analyzer controller cycle register and is transferred to the cycle counter at the beginning of each measurement.

A 'single' or a 'repetitive' measurement is defined by bits D6 and D5, respectively, in the analyzer controller control register. These bits act through the command queuing circuit shown below.

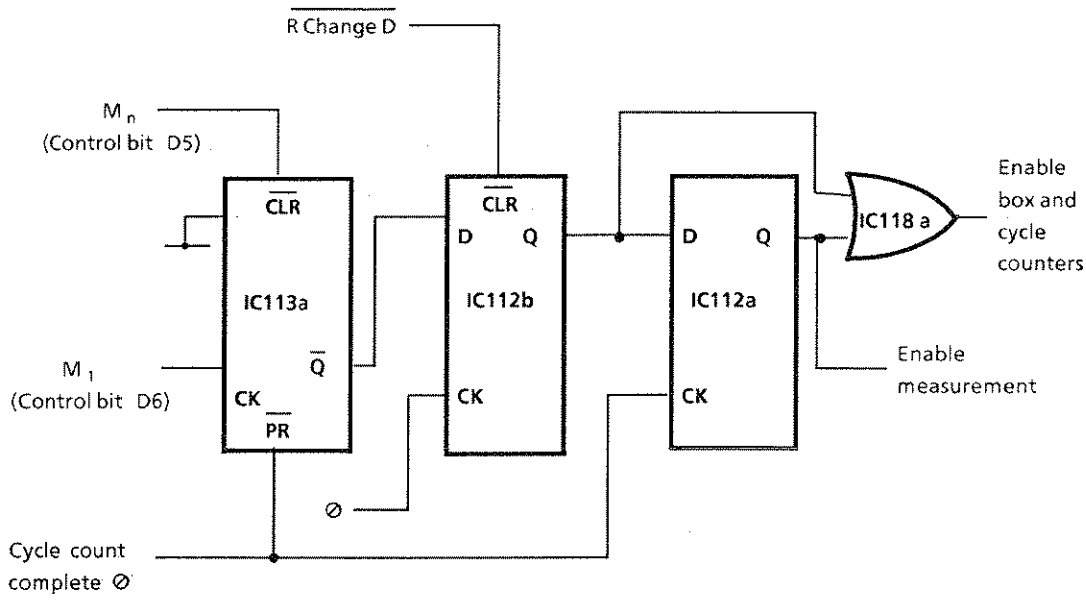


Fig 5.8.2 *Command Queuing Circuit.*

Bits D6 and D5 act at the clock and preset inputs, respectively, of bistable IC113a. A 'single' command clocks IC113a to the measurement priming state, *[Bar]* Q = Hi, which can be cleared on 'cycle count complete'; a 'repetitive' command however, holds IC113a in the measurement priming state until bit D5 is cleared by the main processor.

Bistable IC112b in the queuing circuit is dependent on the R CH D*[Bar]* output of range change stretch. A change in the synthesizer frequency range causes the R CH D *[Bar]* signal to go Lo for eight Pre-gen pulse periods. Hence a measurement can be started only after the synthesizer has settled down. The range change delay is triggered by the microprocessor writing to bit 3 of the control register.

The first Pre-gen pulse that occurs without a Lo R CH D *[Bar]* signal present clocks a Hi measurement priming signal to the Q output of IC112b. A Hi enabling signal is thus sent to the box and cycle counters via IC118a and the cycle counter, previously set to FF, is allowed to produce a carry on the next carry from either the synchronous or asynchronous box counter. The resultant carry from the cycle counter has four effects:

1. the cycle counter is loaded with the two's complement value of the required cycle count,

2. for a single measurement, IC113a is preset to the 'stop measurement' priming state, Q*[Bar]* = Lo,

3. the Hi Q output of IC112b is clocked to the Q output of IC112a to enable the measurement,

4. a fast interrupt request (FIRQ) is sent to the main processor to signify that the measurement has started.

For a single measurement, IC113a is simultaneously set to the Q *[Bar]* = Lo state, in preparation for stopping the measurement.

On completion of N cycles a carry from the cycle counter causes another interrupt request to be issued to the main processor and, in the case of a single measurement, clocks IC112a to the 'stop measurement' state, Q = Lo.

For repetitive measurements IC112a continues to be clocked to the Q = Hi state, because M_n holds IC113c Q *[Bar]* in a Hi state, and an interrupt request is issued to the main processor at the end of each N cycle count.

8.3 ANALYZER RAM ADDRESSING

Each analyzer RAM address consists of two parts; a box address and a byte address.

Box addresses are output from the synchronous box counter, which is enabled by:

1. the output of the 15/3/1.5 divider, to determine the rate at which the box addresses are incremented and;

2. the PRE V_F signal, to establish synchronism with the measurement integration process in the analyzer.

Synchronism of the box address count with the zero degrees reference point is achieved with the SET 0 signal. This sets a base count of 152 (98_H) into the box counter, which is incremented to 255 (FF_H) to cover the 104 (68_H) box addresses.

A full box address count, ie, 104, covers one complete measurement cycle, therefore the carry output of the synchronous box counter can be used to increment the cycle counter. This is normally the case at analysis frequencies greater than 4Hz. At frequencies lower than this, however, the cycle counter is incremented instead by the output of the asynchronous box counter.

The asynchronous box counter is incremented in synchronism with the synchronous box counter, but can be set, via control bit D0, to start its count from any box address. Hence, a measurement can start anywhere in the analysis cycle, ending at the same point in the next cycle. The result, however, is still referred to zero degrees. This is demonstrated in Fig 5.8.3. Asynchronous measurements are selected with control bit D1.

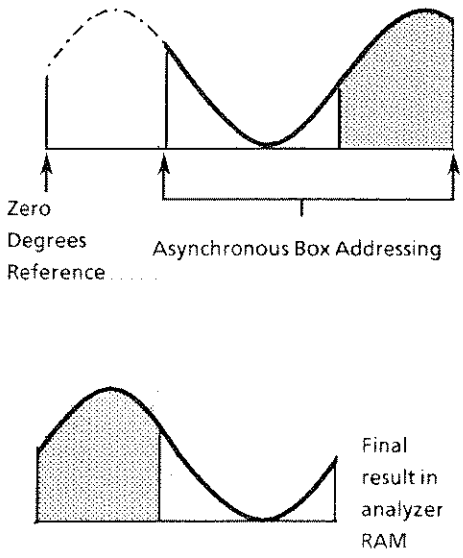


Fig 5.8.3 *Asynchronous Box Addressing.*

Byte addresses are output to the byte address counter. This consists of a counter, IC9, which which divides the ϕ clock frequency by 4 to define the duration of each byte address period and a down counter, IC3 (driven by IC9) which controls the byte address and RAM read/write (R/ W*[Bar]*) lines.

The timing of the byte address counter is shown in Fig 5.8.4. The byte addressing sequence shown covers a read/write operation for each of the five bytes of a measurement data box and occurs once for each PRE V_F pulse.

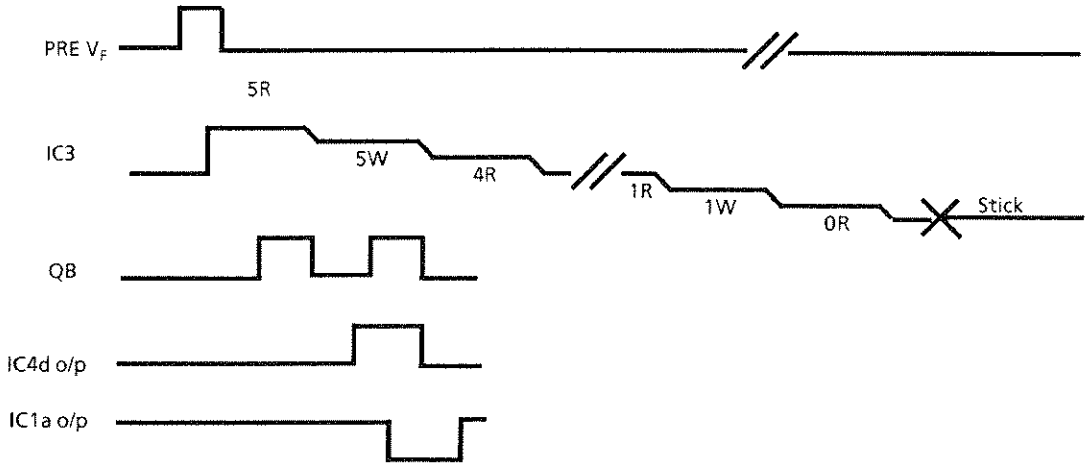


Fig 5.8.4 *Byte Address Timing.*

Prior to each PRE VF pulse the byte address counter is locked in a non-operational state, with the CARRY*[Bar]* output of IC3 Hi and the CARRY output of IC9 Hi. A byte addressing sequence begins when a PRE V_F pulse sets IC9 to a count of 12 (C_H). IC9 then counts up on the ϕ clock to produce a carry and to preset itself to 12 (C_H) on every fourth pulse. IC3 divides down on the carry output of IC9 to step through the byte addresses and associated read/write states. During the byte address changeover periods the analyzer RAM is disabled by the Hi output of IC1a.

8.4 HIGH FREQUENCY OPERATION (≥65.536kHz)

Control bit 2 from the control register selects between high and low frequency operation. At high frequency, measurements are taken at a fixed frequency of 393.216Hz. The HF /LF control signal is used to switch the multiplexer (IC127) so that the SET 0 *[Bar]* signal is disabled and counters IC106 and IC108 are always enabled to count. These counters therefore increment whenever the PRE VF signal from Pcb18 is present. (This is arranged to be a constant 40.9kHz signal when in HF mode)

The cycle is complete when 104 clocks have been received from pcb18, thus giving the 393.216Hz measurement frequency. The SET 0 *[Bar]* signal is related to the generator reference frequency (which varies between 6.5kHz and 65kHz in HF mode). This is asynchronous to the 393Hz measurement frequency and therefore must be disabled to prevent the SET 0 *[Bar]* signal from resetting the analyzer box address at random points in the waveform.

9 LOW FREQUENCY SYNTHESIZER (Board 18)

9.1 INTRODUCTION

The low frequency (LF) synthesizer provides a digital drive signal for the LF generator (pcb 15) and drive signals for the analyzer and analyzer control boards (pcbs 10 and 17 respectively). These signals are derived from a 10MHz (10.468983MHz) crystal oscillator by a series of frequency dividers. The basic interconnections between the LF synthesizer and pcbs 10, 15, and 17 are shown in Fig. 5.9.1 below.

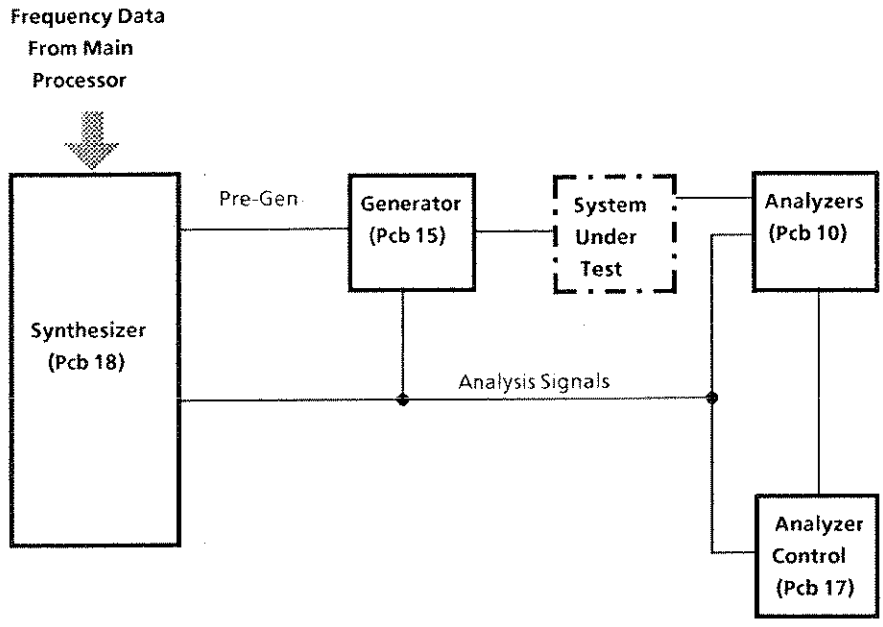


Fig 5.9.1 *Synthesizer - System Interfacing*

9.2 FREQUENCY CONTROL

Control data for the frequency divider chain are taken from the frequency and range control registers of the LF synthesizer, which are loaded by the main processor.

Table 5.10.1 shows how the frequency and range data act on the frequency divider chain to produce the required output frequencies. The frequency value produces, at the output of the frequency divider, an enabling 'envelope' for the range divider. This envelope encompasses a number of clock (ϕ) pulses proportional to the frequency value. The range value sets up the division ratios in the remainder of the divider chain.

Table 5.9.1 *Division Ratios of. Signal Generation and Analysis Dividers*

Range	Max. Freq.	Range Dividers								LF/HF	LF Het.
		A	B	C	D	E	F	G	H		
10	32MHz (20MHz)*	156	-	-	-	-	1	1000	-	HF	OFF
9	6.5535999MHz	156	-	-	-	-	1	100	-	HF	OFF
8	655.35999kH	156	-	-	-	-	1	10	-	HF	OFF
7	65.535999kH	156	251 (199)*	156	251 (199)*	1.5	1	-	1	LF	ON
6B	32.767999kHz	312	199	312	199	3	1	-	1	LF	ON
6A	19.999999kHz	312	199 (61)*	312	199 (61)*	3	1	-	1	LF	ON
5	6.5535999kHz	1560	61	1560	61	15	1	-	1	LF	ON
5A (4A)*	6.5535999Hz	1560	31 (50)*	1560 (-)*	31 (1)*	15 (3)*	10	-	10 (1)	LF	ON (OFF)*
4	299.99999Hz	1560	50	-	1	3	10	-	1	LF	OFF
3	65.535999Hz	1560	50	-	1	15	100	-	1	LF	OFF
2	6.5535999Hz	1560	50	-	1	15	1000	-	1	LF	OFF
1	not used	-	-	-	-	-	-	-	-	-	-
0	655.35999mHz	1560	50	-	1	15	1000	-	1	LF	OFF

* 1255 only. Other values apply to 1260.

9.3 LOW FREQUENCY HETERODYNING (RANGES 5,6 AND 7)

In order to keep within the specification of the analyser ADCs, the frequency of the signal for analysis on frequency ranges 5 to 7 is divided by a heterodyning process (refer to the table above).

The heterodyne configuration of the frequency divider chain is shown in Fig 5.9.2. For every 'n' ϕ pulses entering the clock input of divider B, a single pulse one ϕ period wide is produced. An example of the resulting signal (SIGNAL B) is shown in Fig 5.9.3. An inversion of signal B, SIGNAL B *[Bar]*, is ANDed with signal A and the resulting signal, SIGNAL C, is used to control the response of divider C. Without the SIGNAL B *[Bar]* input, divider C would count the same number of ϕ pulses as divider A; with it, however, one ϕ pulse in 'n' is 'nibbled' out. On each of the frequency ranges 5 to 7, divider C has the same division ratio as divider A, the ratio therefore, between frequencies D and E, is n-1:n. For the frequency difference output of the mixer, this gives a ratio between signals F and E of 1:n, which is the required division ratio of the signal for analysis.

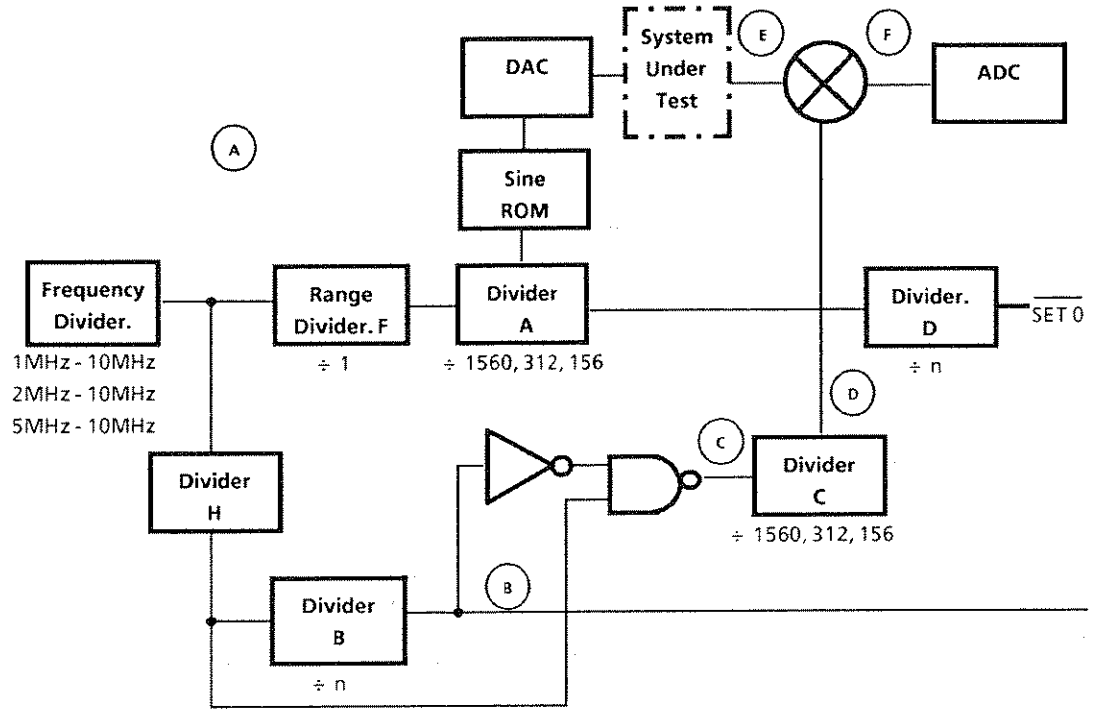


Fig 5.9.2 *Low Frequency Heterodyning Configuration*

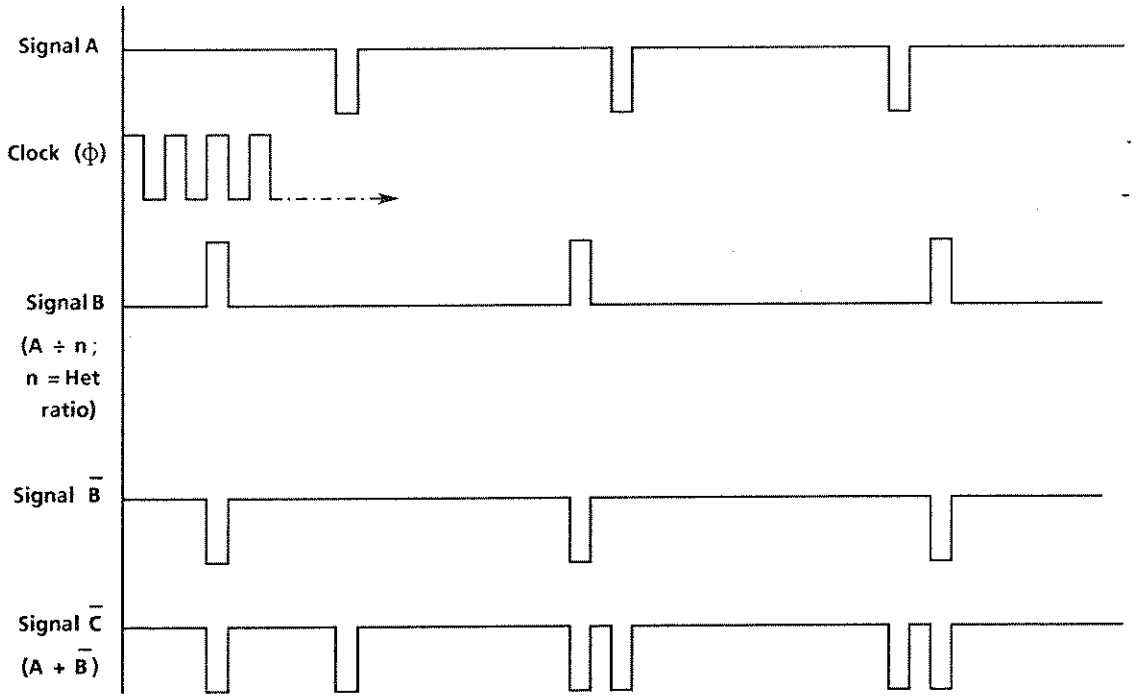


Fig 5.9.3 *n-1/n Frequency Division Process*

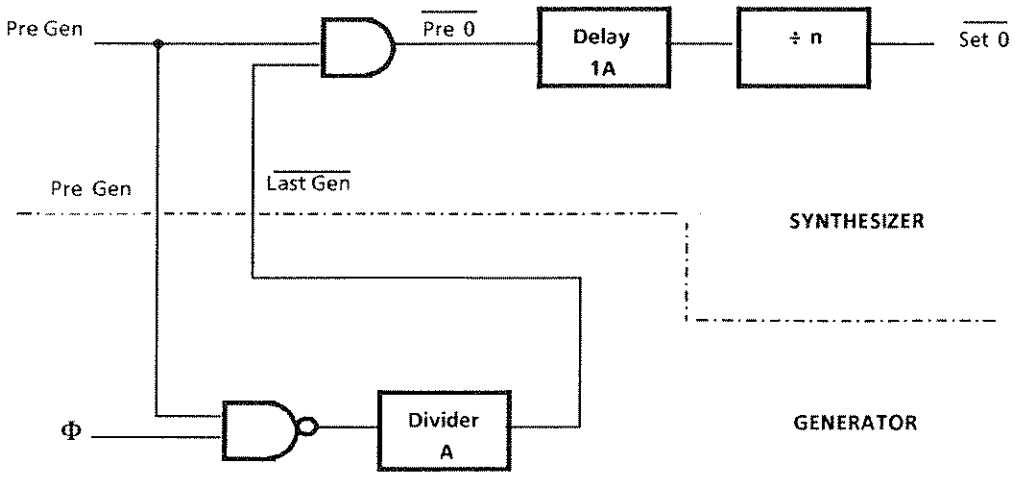


Fig 5.9.4 *Circuit Configuration For $\overline{Pre\ 0}$ Signal*

9.4 PHASE REFERENCE

A zero degrees reference point for the analysis is provided by the SET 0 *[Bar]* signal. This is a delayed, and in the case of the heterodyned frequency ranges, a divided down version of the PRE 0 *[Bar]* signal.

PRE 0 *[Bar]* is derived, on the LF synthesiser board, from the LAST GEN *[Bar]* output of the LF generator (pcb 15). (LAST GEN *[Bar]* occurs on the carry from divider A, when this is clocked to the address of the negative-to-positive cross-over point of the data contained in the sine ROM.)

The circuit configuration used to obtain the PRE 0 *[Bar]* signal is shown in Fig 5.9.4.

9.5 PHASE COMPENSATION

Time delays introduced by the generator output amplifier, the analyser input amplifier, and the analyser ADC, would, if not compensated for, produce a phase error in the analysis results. Delay compensation takes the form of delay 1 (A and B) and delay 2. These have the effect of delaying the phase (SET 0 *[Bar]*) and other analysis synchronisation signals by the same amount as the above mentioned inherent delays and therefore they neutralize the effect of the inherent delays on the analysis. The software calibration removes any residual phase errors.

9.7 HIGH FREQUENCY OPERATION (RANGES 8 to 10)

When operating in high frequency mode, analysis takes place at a constant frequency (393.216Hz). The generator frequency is synthesized in the usual way, the PRE GEN signal being used to enable the generator waveform to step. Pcb 17 requires a clock signal, which is at 40.9kHz. (393.216Hz $\times$ 104) to step the analyzer box counters. This signal is derived from the 10.468983 MHz crystal by a divide by 256 circuit (IC130 and IC128). A multiplexer is then used to select this signal instead of the normal PRE V_f signal and this is output to pcb 17 via the PRE V_f bus line. The PRE V_f signal is used to clock the analyzer box address on pcb17. The same signal is used to trigger the analyzers to accumulate new data, from the ADC, into the analyzer box RAM.

10 MAIN PROCESSOR (PCB 22)

10.1 INTRODUCTION

The main processor responds to any valid local or remote commands to set up and supervise the operation of all other boards in the instrument. It also performs the software routines which permit measurement data to be analysed.

Fig. 5.10.1 is a block diagram of the main processor. The memory available to the main processor is shown on the memory maps in Table 2.1 (a to g) in Chapter 2 of this manual

10.2 MEMORY ADDRESSING

The various areas of memory, mapped in Table 2.1 are enabled by the block decodes performed on high significance address lines by the address decode. Individual locations within each area are selected by the less significant address lines.

10.3 COMMUNICATION INTERFACES

The main processor communicates with several devices by means of asynchronous communication interface adapters (ACIAs). These devices include the front panel interface (pcb 2) and any external device connected to the serial port.

Communication with devices on the general purpose interface bus (GPIB) [IEEE 488] is achieved via the GPIB interface.

10.4 STATUS LEDs

The status of the program being executed by the main processor is indicated by means of four on-board LEDs. (The significance of these, for test purposes, is explained in Chapter 4, 'Self Test').

10.5 POWER FAIL PROTECT

Control and 'File' data are stored in the battery sustained RAM, and are therefore retained, for a minimum of 100 hours, during power- down. The validity of the stored data is checked by means of a 'checksum' that the main processor calculates on power-down and re-calculates on power-up. A battery back-up control ensures that the RAM is disabled immediately the checksum is stored, and is enabled smoothly, on power-up, prior to the operation of the main processor being reset.

10.6 EEPROM ; IC19 and 21

Programs, machine set-ups and functions, can be stored in electrically-erasible PROMS (EEPROMS). This memory is write-protected by a keyswitch on the rear panel and cannot be modified unless the keyswitch is set to 'supervisor' mode.

The data in EEPROM is retained permanently, even with the unit switched off for long periods.

10.7 EEPROM; IC20

One of the EEPROMS, IC20, is used for the storage of calibration data and is write protected by a separate switch (S2) which is located on pcb 22. Except when calibration is being carried out, the switch is set to 'normal' to protect the calibration constants.

10.8 PCB 22 SWITCHES

The bank of switches on pcb 22 are for diagnostic / calibration purposes and should normally be in the 'up' position.

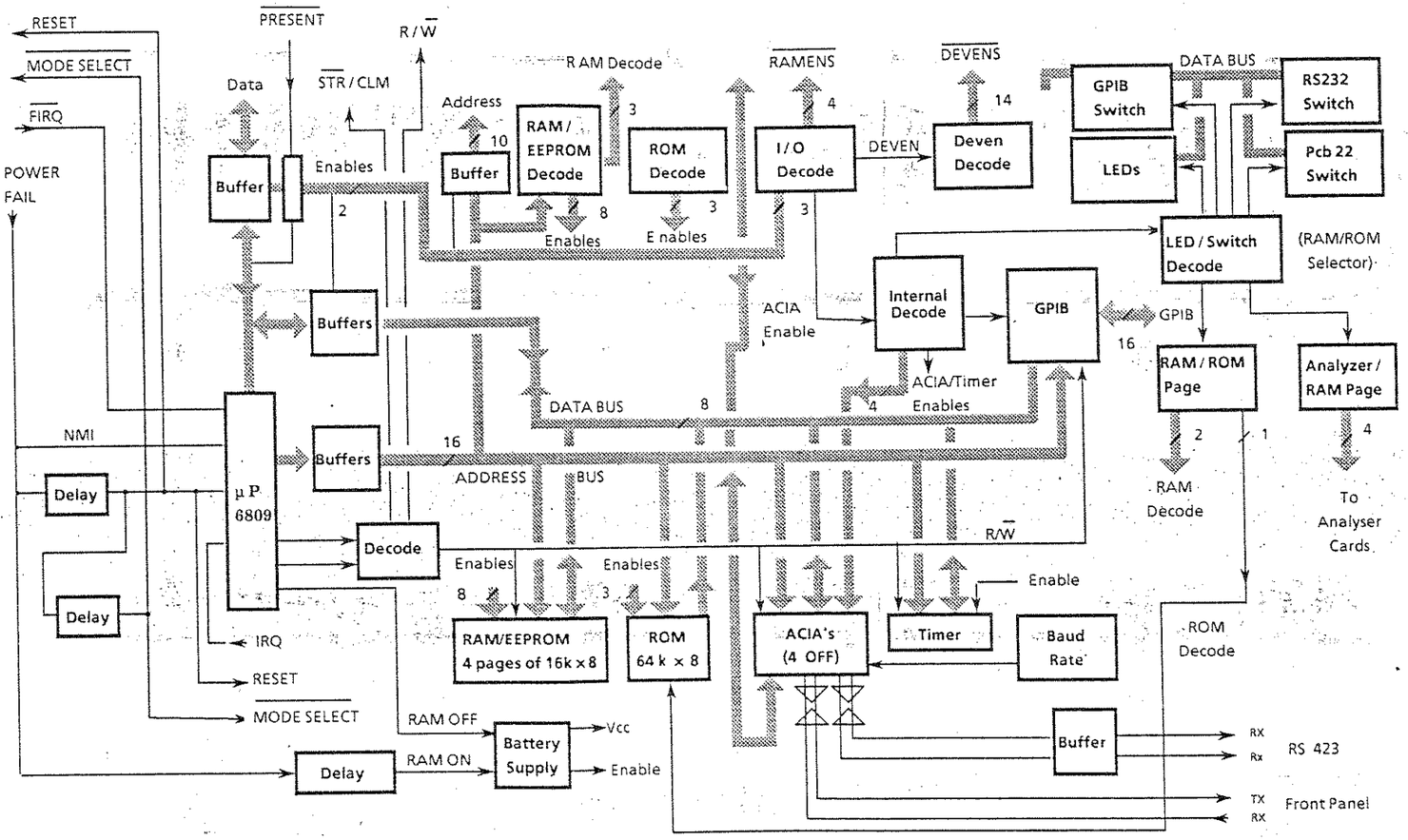


Fig.5.10.1 *Main Processor Board*

11 BINSORT INTERFACE (PCB 30)

11.1 INTRODUCTION

The binsort interface, pcb 30 interfaces between the 1260 impedance analyser and component test and binsort handlers. Under control of 1260's binsort facility, the interface outputs control signals to a handler and decodes signals coming from the handler. These signals step the components in synchronism with measurements taken by the 1260. The interface can detect a handler that is in open loop mode and can react to an interlock signal from the handler.

The main processor generates a 5-bit code, whose value depends upon the result of a measurement. This output is decoded by the binsort interface as a 'bin selection'. The interface controls 16 parallel lines and a 2-state selection extender line, permitting the selection of up to 2 × 16 (32) bins. The interface can operate using either +5V or +15V lines and either positive or negative logic. The combination used is determined by the program from the main control register.

The binsort interface can be programmed to step 'n' components before interrupting the main processor for a measurement. Components stepped in this way will be sorted into bin number 1.

Fig. 5.11.1 is a simplified block schematic diagram of pcb 30.

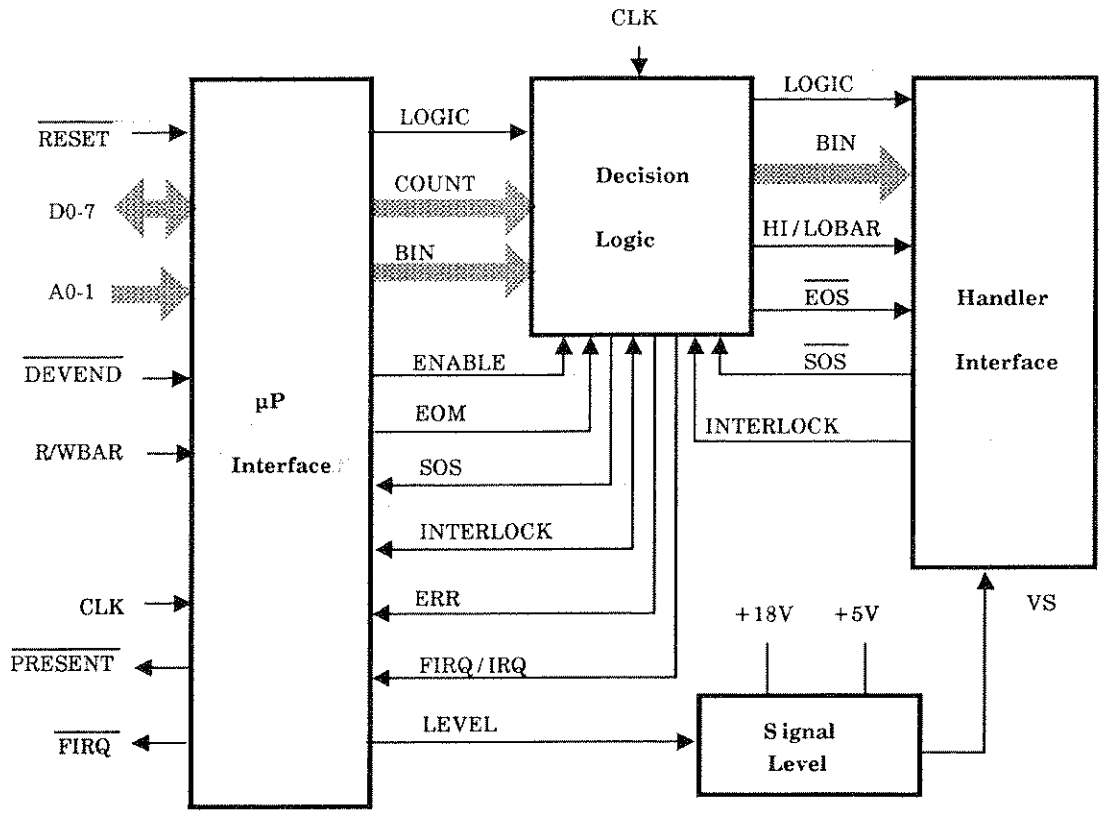


Fig 5.11.1 Binsort Interface *Schematic.*

11.2 MICROPROCESSOR (μP) INTERFACE

This part of the pcb contains the control and status registers, ICs 1 to 5. The registers have the following functions:

IC1 **Address Decode.** This IC decodes the address lines A0 and A1, the R/WBAR line and the DEVEND*[Bar]* line. The DEVEND*[Bar]* line gives the registers an address offset of $3BD0_H$.

IC2 **Component Step Count Register.** This 'write only' register is located at address 2 + offset. It controls the number of components stepped between measured components.

IC3 **Bin Selection Register.** This 'write only' register is located at address 0 + offset. It defines a bin line to be asserted for the component just measured.

IC4 **Main Control Register.** This 'write only' register is located at address 1 + offset. The bin functions of this register are as follows:

Bit	Function	Comment
0	Board Enable	If set to 1, the board is enabled and can interrupt the main processor on the FIRQ *[Bar]* line.
1	Decision Ready	A component has been measured and the resulting decision has been written to the bin selection register.
2	Handler signal drive level	0 = +5V, 1 = +18V.
3	Bin drive signal logic	0 = Asserted line is driven low. 1 = Asserted line is driven high.
4	Selection extender logic	0 = Sets high HI/LOWBAR to 1 for upper 16 bins. 1 = Sets HI/LOWBAR to 0 for upper 1 6 bins.
5	End of sequence logic	0 = Asserted EOS is driven low 1 = Asserted EOS is driven high.
6	Interlock logic	0 = Measurements are enabled with INTOUT set to 0. 1 = Measurements are enabled with INTOUT set to 0.
7	Start of sequence logic.	0 = Measurement or component stepping initiated if SOS driven low 1 = Measurement or component stepping initiated if SOS driven high.

IC5 **Main Status Register.** This 'read only' register is located at address 0+ offset. The bit functions of this register are as follows:

Bit	Function	Comment	Mapping
1	INTOUT	Reflects state of INTOUT line	D0
2	ERR	Set if control logic detects an error	D1
3	SOS	Reflects state of SOS line	D2
4 - 6	Not used	Connected to ground	D3 - D5
7	IRQ	Set to indicate that board generated a request on FIRQ *[Bar]* line	D7
8	Test	Connected to ground. This line used in 'board present' test.	PRESENT *[Bar]*

11.3 LOGIC

The logic section controls the test sequencing and the decision decoding. The functions of the ICs which make up this section are as folows:

IC9 Decodes the least significant four bits of the bin decision into 16 parallel lines.

IC6-8 The component stepping section, ICs 7 and 8 count from 'n' to 0 - to step 'n' components. IC6 provides the reload when 0 is reached, or when a new count is programmed.

IC13b, 14a-c Gating logic to inhibit interrupts to the main processor during stepping of components.

IC11 Provides a reset signal to the bin selection register (IC3) when a reset occurs or when the *[Bar]*SOS line is asserted. This ensures that stepped components are sorted into bin 1.

IC10 Generates interrupts to the main processor under the following conditions:

a. SOS*[Bar]* is driven low, indicating that a component is waiting to be measured.

b. SOS*[Bar]* is driven high before a measurement has been completed (ie, before EOM has been set by the main processor). The handler is in open loop mode.

c. INTOUT is high.

This IC also provides the EOS signal to the handler The line is driven highwhen EOM is set by the main processor and stays high until SOS *[Bar]* is driven low again.

Note. If the interlock is to be disabled, then split-pad SP1 should be made.

11.4 HANDLER INTERFACE

Pcb 30 includes the handler interface. This interface drives the handler signal lines. The functions of the ICs in the handler interface are as follows:

IC21-25 These ICs provide the signal inversion for negative or positive logic.

IC18-20 These two ICs are output signal drivers with open collector outputs. The outputs are pulled up by 47k resistors to either +5 or +18 volts.

IC17 This IC is an input buffer for the SOS*[Bar]* and INTOUT lines. The input is compared with +1.6 or +9 volts to determine the logic state of the lines. These inputs are protected by the diodes clamping them to ground and VS and the 1k series input resistor.

11.5 SIGNAL LEVEL

Pcb 30 includes IC16 and RL1. These components provide the drive levels of either +5V or +18V for the handler interface section. The drive levels are also accessible to the handler via the VS line. This line is fused with a 500mA anti-surge fuse mounted on the interface pcb.

12 CURRENT-TO-VOLTAGE CONVERTER. (PCB 31)

12.1 INTRODUCTION

The 1260 performs current analysis by first converting the current input signals into equivalent voltages and then measuring these with a voltage analyzer. Software is then used to scale the voltage outputs into appropriate current values for display.

The conversion facility is provided by current-to-voltage converter, pcb 31, whilst voltage analysis is achieved using a pcb10. (Sect. 4 refers). The combination (pcbs 10 and 31) is termed the 'current analyzer'. The current analyzer permits current analysis over the range 200pA to 100mA.

Inputs to the current analyzer are via a single BNC. The input amplifier has a floating ground to permit in-circuit measurements with systems which are not ground referenced. In practice this means that the outer of the BNC input connector can be floated by up to ± 0.4V away from ground potential.

Combining a current analyzer with a voltage analyzer permits impedance measurements to be made. Fig. 12.3 is a simplified diagram of the impedance measuring circuit.

12.2 CIRCUIT DESCRIPTION

Fig. 12.1 is a simplified circuit of the current-to-voltage converter.

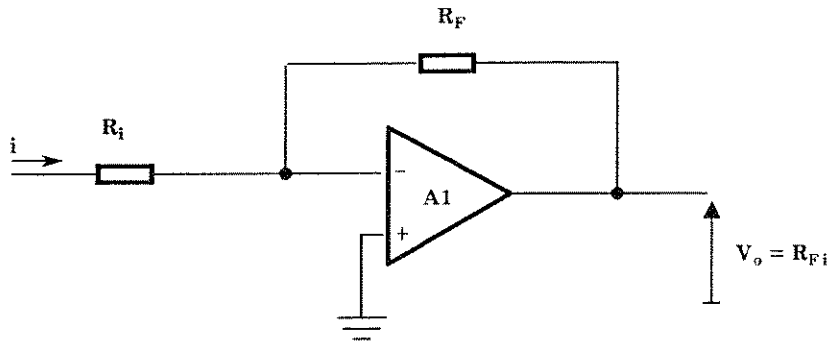


Fig. 12.1 *Current-to-Voltage Converter - Simplified*

Since amplifier A1 takes negligible input current, all the injected signal current flows through the sense resistor R_F. The output voltage is then measured then scaled (via the software) in order to display current. The value of the sense resistor is varied depending on the selected current range. The equivalent output voltage ranges of the I-to-V converter are matched to the input ranges of a pcb 10 voltage analyzer. Values are summarised in Table 12.1

The input impedance of the I-to-V converter is determined by the value of R_i. The values have been chosen to reduce the error voltage appearing at the input to the converter whilst still limiting the input current. (An error voltage would result in current errors which could not be measured).

In practice, the performance required of amplifier A1 cannot be provided by a single device. Fig. 12.2 shows the practical circuit which uses three amplifier stages.

Table 12.1 *I-to-V Converter Input/Output Ranges*

INPUT RANGE (RMS)	SENSE RESISTOR (Ω)	OUTPUT RANGE (RMS)
6μA	5000	30mV
60μA	5000	300mV
600μA	5000	3V
6mV	50	300mV
60mA	50	3V

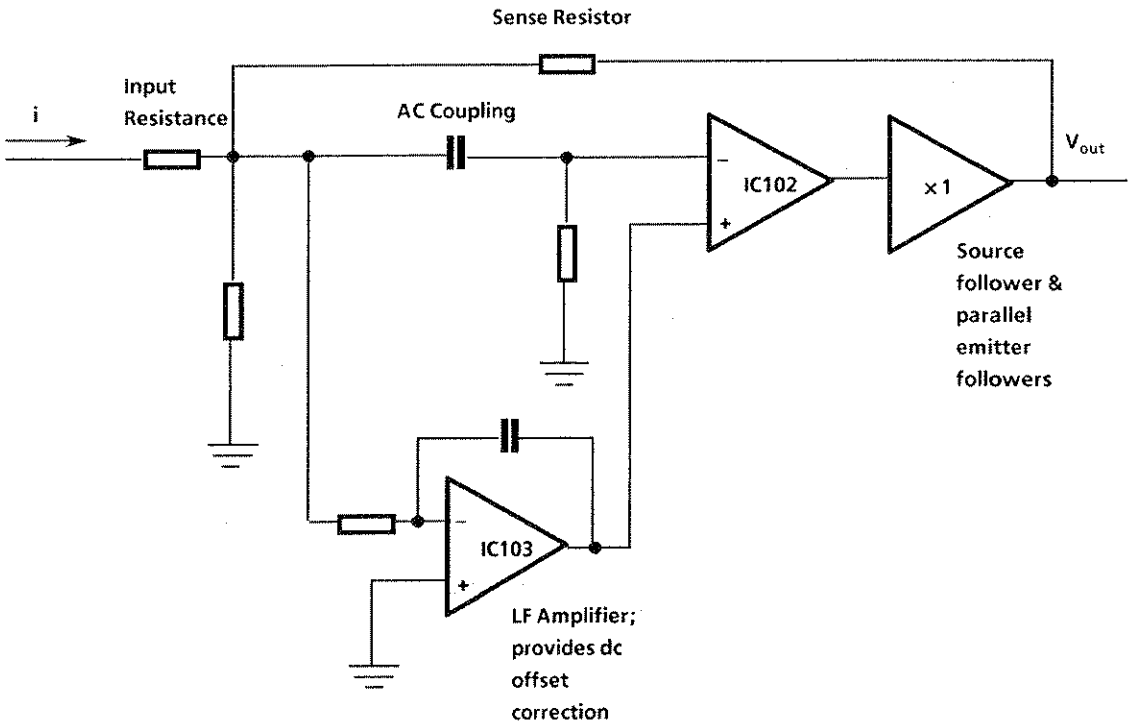


Fig. 12.2 *Current-to-Voltage Converter - Practical Circuit*

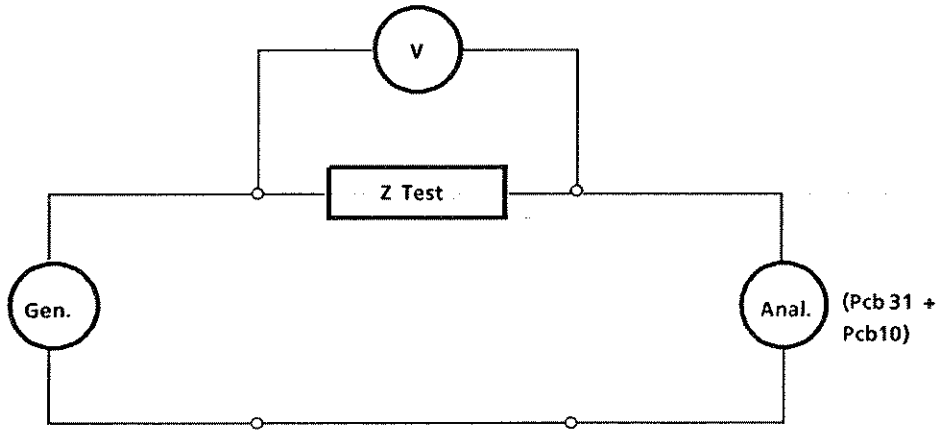


Fig 12.3 *Impedance Measurement Technique*

Chapter 6
Calibration 1255 & 1260

- Part A CALIBRATION OF 1255
- Part B CALIBRATION OF 1260

Chapter 6 Part A
Calibration of 1255

Figures

1 TEST EQUIPMENT

Power Supply Test

- Flash/continuity Tester
- DVM
- Power Supply Load Card 12506003
- Mains-fail test box 12506002
- Variac

Final Calibration

- Flash/continuity tester
- DMM Schlumberger 7060E
- Oscilloscope
- Extender Card 12500508
- Counter timer
- Calibrator Fluke 5200
- Test Set 12606001
- Power Meter W & G EPM-1 with TK-10 Test Head
- Power Supply Floating 0 to 60V

Functional Overcheck

- DMM Schlumberger 7060E
- Counter timer
- Calibrator Fluke 5200
- Test Set 12606001
- Power Meter W & G EPM-1 with TK-10 Test Head
- Silent 700 terminal or equivalent
- Power splitter and 2x50Ω matched terminators

2 POWER SUPPLY TEST

2.1 Take out all the PCBs except PCB 5 and disconnect the display.

2.2 Flash test on mains live and neutral to earth @ 1500V dc.

2.3 Check that the resistance from any of the following points to the earth pin on the mains connector is less than 0.5Ω:

Fan guard
Exposed screws on the rear panel
BNC outers on the rear panel

2.4 Check that the fuse inserted is rated @ 1A (anti-surge).

2.5 Measure the resistance across the link for 115V [this is on thePower Supply Board next to the mains input] checking that with switch set to 115V the resistance is less than 1Ω and with the switch set to 230V the resistance is greater than 20kΩ.

2.6 Set mains select switch to 230V.

2.7 Insert the PSU load card into the SKA9-SKB9 position on theMother Board and set the switches on the load card to off.Connect the 1255 mains lead to the variac o/p set to 230V.

2.8 Switch on the mains and the 1255. Monitor the 5V rail on the load card and adjust the potentiometer nearest the 5V output on the Power Supply to give 5.00V ± 0.01V.

2.9 The new version of the power supply load card does not have aswitch "C". When using this card ignore all references to switch "C" in the following tests:

Check the following voltages (measured on the Power Supply Load Card) with switches A, B, C and D all off:

Voltage	Limits
+ 5V	4.9V to 5.1V
+18V	17.5V to 20V
-18V	-17.5V to -20V
+24V	23.5V to 25.5V

2.10 Repeat test 9 with switch A on.

2.11 Repeat test 9 with switches A, B and C on.

2.12 Set the mains to 252V and repeat tests 9, 10 and 11.

2.13 Set the mains to 198V and repeat tests 9, 10 and 11.

2.14 With switches A, B and C still on, measure the 5V rail and momentarily operate switch D; the 5V rails should be 4.8V. Set switch D off, but leave A, B and C on.

2.15 Momentarily short the 5V to 0V and check that the power supply recovers.

2.16 Connect the 1255 as shown in Figure 1 with the Test Box switches set to "Trigger Normal" and "Supply Switching". Using the oscilloscope, adjust the Test Box Delay so that the 1255 is switched off at the peak of the mains cycles.

2.17 Check that POWER FAIL on PCB 5 is given approximately <10msec after the mains has failed.

2.18 Check that the 5V rail holds up to a minimum of 4.75V for at least 6msec after POWER FAIL is asserted.

2.19 Set the Test Box Switch to "Trigger Invert" and check that there is at least 200msec delay from the point at which the power comes on to the POWER FAIL going back high.

2.20 Switch Off. Replace the fuse by a 2A fuse and set the variac output and the 1255 mains selector to 115V. Switch on and repeat tests 9, 10 and 11. Set the Variac to 126V and repeat paragraphs 9, 10 and 11.

Set the Variac to 90V and repeat paragraphs 9, 10 and 11.

Repeat test 14
Repeat test 15
Repeat test 16

2.21 Switch Off. Replace the 1A fuse and set the 1255 back to 230V operation.

2.22 Replace the rest of the PCBs.

The Power Supply is now fully set up.

3 SET UP PRIOR TO SOAK

This section is not required for this manual.

4 SOAK TEST

This section is not required for this manual.

5 FINAL CALIBRATION

Calibration should be carried out at a constant temperature in the range 17 - 23°C

5.1 SAFETY CHECKS

These checks should be carried out if they have not already been done, as in Section 2. This would occur for example in an old unit if it was being re-calibrated after a period of time or after repair work had been undertaken

5.1.1 Take out all the PCBs except PCB 5 and disconnect the display

5.1.2 Flash test on mains live and neutral to earth @ 1500V dc

5.1.3 Check that the resistance from any of the following points to the earth pin on the mains connector is less than 0.5Ω:

Fan guard
Exposed screws on the rear panel
BNC outers on the rear panel

5.1.4 Check that the fuse inserted is rated @ 1A (anti-surge) for 230V or 2A for 115V operation

5.1.5 Measure the resistance across the link for 115V [this is on the Power Supply Board next to the mains input] checking that with the switch set to 115V the resistance is less than 1Ω and with the switch set to 230V the resistance is greater than 20kΩ.

5.2 PRELIMINARY TEST

Before testing check that the connections are as in figure 1.

5.2.1 Switch on and set the Generator output to give a 3V, 400Hz signal. Connect this to both Channels 1 and 2 and take several measurements displaying the Channel 1 readings. Ensure that the readings on the 1255 are not scattering and that they are 3V±0.3V

5.2.2 Repeat 1 displaying Channel 2

5.2.3 Set the frequency to 100kHz and take several readings to ensure that the result =3V±0.3V and does not scatter by more than 20 bits.

5.2.4 Repeat 3 displaying Channel 1

5.2.5 Leave the unit switched on for half an hour before starting calibration

5.3 LF GENERATOR CALIBRATION (PCB 15)

5.3.1 Switch off, disconnect the cables and put PCB 15 on an extender card. Switch on and set up the following:

SELF-TEST Initialise [TT1]

With a DMM on DCV measure the voltage from TP4 to TP1. Adjust RV203 for 0V± 2mV

Measure the voltage from TP5 to TP1. Check for 0V±10mV

5.3.2 This completes PCB15 calibration. Switch off and refit PCB 15 into its slot and reconnect the cables.

5.4 HF SYNTHESISER CALIBRATION (PCB 16)

5.4.1 Switch off and put PCB 16 on an extender card. NOTE The cable from PCB 15 to PLH must be connected. Switch on and set up the following:

SELF-TEST Initialise [TT1]

5.4.2 Set up the following:

GENERATOR Frequency 66kHz [FR66E3]

With the oscilloscope check that the waveform on TR201 collector (can) is a +5V square wave with period 2.54msec ± 0.1msec.

5.4.3 For status B issue A boards or later issues:

Monitor TP201 with the DVM and set CV401 to obtain a reading of -3V to +0.5V.

For older boards (status A):

With the DVM check that the DC voltage on TP201 lies between -6V and +6V.

5.4.4 Set up the following:

GENERATOR Frequency 20MHz [FR20E6]

Disconnect the cable from PCB 16 PLH and connect a 32KHz ±100Hz 5V ±0.1V rms sine wave to PCB 16 PLH. With a DMM on DCV monitor TP102 wrt ground. Adjust LV101 (under the middle screen) to give a voltage of +10V ±0.4V.

5.4.5 Set up the following:

GENERATOR Frequency 66KHz [FR66E3]

Reconnect the cable from PCB 15 to PCB 16 PLH. With a DMM on DCV monitor TP102 wrt ground. Check the reading is between -6.5V and -9.5V.

5.4.6 This completes PCB16 checks. Switch off and refit PCB 16 into its slot and reconnect all cables.

5.5 ANALYSER (VOLTAGE) CALIBRATION (PCB 10)

NOTE These tests are best carried out with the front panel raised by one hole so that the cables reach

5.5.1 Switch off and fit PCB 10 channel 1 onto an extender card with the screen removed.

Set up the following:

SELF TEST	Initialise		[TT1]
ANALYSER			
NEXT	Input	Diff	[IP1,1]
SINGLE			[SI]

With a DVM set to ohms measure:

Measure	Reading	Comment
Hi to shield	1MΩ ±10kΩ	Input impedance *
Lo to shield	1MΩ ±10kΩ	Input impedance *
Lo shield to TP601	47Ω ±5Ω#	Shield
Hi shield to TP601	47Ω ±5Ω#	Grounded

* Set the 7060 to the 10MΩ range for these readings.
#For issue A PCB's only the resistance is 0Ω ±10Ω.

Set up the following:

ANALYSER			
NEXT	Input	Diff	[OU1,1]
	Outer	Floating	[OU1,1]
	Coupling	AC	[DC1,1]

With a DVM set to ohms measure from:

Hi to shield	o/c	AC coupled
Lo to shield	o/c	AC coupled

Lo shield to TP601 100kΩ ±100Ω Lo floating

5.5.2 Short circuit the Hi and Lo inputs. Ensure that all cables are connected.

Set up the following:

SELF-TEST	Initialise		[TT1]
ANALYSER	Range	30mV	[RA1,1]
	Input	Diff	[IP1,1]
SINGLE			[SI]

5.5.3 Ignore the first reading and error. With a DC DVM measure the following test points wrt TP601.

Measure	Adjust	Limits
TP403	RV401	0V ±200µV
TP404	RV402	0V ±200µV
TP603	RV403	0V ±15mV

5.5.4 Remove the short circuits and check the following test points wrt TP601:-

Measure	Limits
TP403	0V ±3mV
TP404	0V ±3mV

Re-fit the short circuit.

5.5.5 Set up the following:

GENERATOR	Frequency	20MHz	[FR20E6]
SINGLE			[SI]

With a DC DVM measure the following test points wrt TP601.

Measure	Limits
TP602	0V ±1V
TP603	0V ±100mV

5.5.6 Set up the following:

SELF-TEST	Initialise		[TT1]
ANALYSER			
NEXT	Range	300mV	[RA1,2]
	Input (V1)	DIFF	[IP1,1]
DISPLAY	Source	V1	[SO1,0]
RECYCLE			[RE]

Connect a floating power supply, set to 0V, to the Channel 1 inputs as in figure 5. Gradually increase the power supply output until an overload is continuously indicated in the display. Check the input to the 1255 is within the listed limits when this occurs.

Positive	between Hi and shield	+0.52V to +0.58V
Negative	between Hi and shield	-0.52V to -0.58V

5.5.7 Set up the following:

GENERATOR Frequency 10MHz[FR1E7]

Positive	between Hi and shield	+5.6V to +6.8V
Negative	between Hi and shield	-5.6V to -6.8V
Positive	between Lo and shield	+5.6V to +6.8V
Negative	between Lo and shield	-5.6V to -6.8V

5.5.8 Using the power supply set to the following voltages and applied to both Hi and Lo inputs as a common mode voltage to the shield as in figure 7, and check the voltages at the test points listed below with a DC DVM wrt TP601:

Set up the following:

SINGLE [SI]

Input	Measure	Limits
+50V ±1V	D404 cathode	+6.25V to +7.4V
	D408 cathode	+6.25V to +7.4V
-50V ±1V	D404 cathode	-6.25V to -7.4V
	D408 cathode	-6.25V to -7.4V

5.5.9 Switch off and set CV401, CV402 and CV403 to their mid position (CV403 is present only on issue D or later PCB's).

Fit the screen to analyser 1 and calibrate as follows, with the PCB still on an extender card, so as to be able to access the required adjustments.

Set the waveform switch (position 2 of SW1) down to enable the square wave output. Ensure the "apply cal" switch (position 1 of SW1) is in the down position.

Set up the following:

SELF-TEST	Initialise		[TT1]
GENERATOR	Amplitude	2V	[VA2]
ANALYSER	Integration time	0.3Secs	[IS.3]
NEXT	Input (V1)	DIFF	[IP1,1]
	Range (V1)	3V	[RA1,3]
	Outer (V1)	floating	[OU1,1]
DISPLAY	Source	V1	[SO1,0]
	Coords	R,θ	[CV1]
RECYCLE			[RE]

Connect the 1255 generator to the calibrator phase lock.

Connect the calibrator HI output to the channel 1 HI and the calibrator LO to the channel 1 HI shield. Short circuit channel 1 LO to the LO shield. The calibrator LO must not be connected to earth (as in figure 2).

The limits to follow refer to the R value displayed on the 1255 front panel.

Frequency	Range	Input	Amplitude	Adjust/check	Limits
300Hz	3V	Hi	2V	RV701 & SP702/3/4	2.0005V 1.9995V
65kHz	3V	Hi	2V	CV401	2.0005V 1.9995V

For Issues A,B and C :- Remove the short circuit from channel 1 LO and connect the calibrator to channel 1 LO as in figure 3. Set the frequency to 100 kHz on the 300mV range and set CV402 for less than 5mV. Set the frequency to 1MHz and check for less then 5mV. If it is >5mV adjust CV402 to split the error and recheck at 100kHz.

30Hz	300mV	Hi & Lo	2V	check	<3mV

For Issues D :- Remove the short circuit on Channel 1 LO and connect the calibrator to Channel 1 LO as in Figure 3:

100kHz	300mV	HI&LO	2V	CV402 set to <2mV
1MHz	300mV	HI&LO	2V	CV403 set to <5mV

Repeat adjustment of CV402 and CV403 if necessary:

30Hz	300mV	HI&LO	2V	Check	<3mV

5.5.10 Check the channel 1 calibration,as follows, with connections as in figure 2.

Frequency	Range	Input	Cal Amp	Adjust /Check	Limits	Comments
300Hz	3V	Hi	2V	RV701	2.0010V 1.9990V	[RA1,3] [FR300]
300Hz	3V	Hi	3V	check	3.0015V 2.9985V	
300Hz	3V	Hi	0.3V	check	300.3mV 299.7mV	
300Hz	300mV	Hi	300mV	check	300.3mV 299.7mV	[RA1,2]
300Hz	300mV	Hi	30mV	check	30.03mV 29.97mV	
300Hz	30mV	Hi	30mV	check	30.03mV 29.97mV	[RA1,1]
300Hz	30mV	Hi	34mV	check	no overload	
655Hz	3V	Hi	2V	check	2.0010V 1.9990V	[RA1,3] [FR655]
656Hz	3V	Hi	2V	check	2.0010V 1.9990V	[FR656]
656Hz	30mV	Hi	34mV	check	no overload	
3kHz	3V	Hi	2V	check	2.0010V 1.9990V	[FR3E3]
10kHz	3V	Hi	2V	check	2.0020V 1.9980V	[FR1E4]
32kHz	3V	Hi	2V	check	2.0040V 1.9960V	[FR32E3]
65kHz	3V	Hi	2V	check	2.0040V 1.9960V	[FR65E3]
100kHz	3V	Hi	2V	check	2.0200V 1.9800V	[FR1E5]

5.5.11 Set up the following:

SELF-TEST	Initialise		[TT1]
DISPLAY	Source	V1	[SO1,0]
RECYCLE			[RE]

Connect the calibrator HI to channel 1 HI and the calibrator LO th channel 1 HI shield as in figure 2. Set the calibrator to 1MHz and with the phase lock off, switch the calibrator output on and gradually increase the output voltage until the unit indicates an overload.

Check that the calibrator is delivering 4.3 ± 0.5V rms at this point.

Disconnect the calibrator. Replace Analyser 1 in its correct position in the unit card rack.

Switch off, refit PCB 10 into its slot and reconnect all cables.

REPEAT FROM 5.5 FOR CHANNEL 2 REPLACING ALL SET UP INSTRUCTIONS FOR THE CHANNEL 2 EQUIVALENT.

Refit the front panel.

5.5.12 Set the waveform switch (position 2 of SW1) up to disable the square wave output. Ensure the "apply cal" switch (position 1 of SW1) is in the down position. Set up the following:

SELF-TEST	Initialise		[TT1]
GENERATOR	Amplitude	0.75V	[VA.75]
	Frequency	65kHz	[FR65000]
ANALYSER	Integration Time	1sec	[IS1]
DISPLAY	Source	V1	[SO1,0]
	Coord	r.theta	[CV1]
RECYCLE			[RE]

Using the power meter via the 12606801 test set check CH1 high frequency performance either manually or under GPIB control as in following table with the connections made as in figure 6.

Make a note of this reading.

Frequency	**Range**	**Input**	**Atten -14dB**	**Check**	**Limits**	
100kHz	auto	Hi		check	as noted ±3mV	Terminate with 50Ω
200kHz	auto	Hi		check	as noted ±3mV	Terminate with 50Ω
650kHz	auto	Hi		check	as noted ±3mV	Terminate with 50Ω
660kHz	auto	Hi		check	as noted ±4mV	Terminate with 50Ω

Frequency	Range	Input	Atten -14dB	Check	Limits	
1MHz	auto	Hi		check	as noted ±5mV	Terminate with 50Ω
2MHz	auto	Hi		check	as noted ±10mV	Terminate with 50Ω
6.5MHz	auto	Hi		check	as noted ±15mV	Terminate with 50Ω
6.6MHz	auto	Hi		check	as noted ±15mV	Terminate with 50Ω
10MHz	auto	Hi		check	as noted ±30mV	Terminate with 50Ω
20MHz	auto	Hi		check	as noted ±50mV	Terminate with 50Ω

THIS COMPLETES CHANNEL 1 PRE AGREE TEST'S.
REPEAT FROM 5.5.11 FOR CHANNEL 2 REPLACING ALL SET UP INSTRUCTIONS FOR THE CHANNEL 2 EQUIVALENT.

5.6 GENERATOR OUTPUT (PCB 14)

5.6.1 Switch off and put PCB 14 on an extender card. Remove the screen box. Disconnect the cables to SK201 and SK701. Switch on and set up the following:

SELF-TEST Initialise [TT1]

Make the following adjustments using a DMM on DCV to monitor the voltages indicated:

Measure	Adjust	Limits	Comment
Across R531	RV501	110mV ± 10mV	Quiescent I
Gen o/p	RV301*	0V ± 5mV	Output offset
Across R416	RV302*	0V ± 15mV	Output CM

* Note on issue B copper RV301 & 302 are transposed.
* Note on issue D copper SP401 must be made.

5.6.2 Switch off and refit the screen box. Switch on and monitor the output between the generator LO and earth with an oscilloscope. Adjust RV601 for the minimum squarewave between LO and earth across R416.

5.6.3 Fit the cables to SK201 and SK701. Monitor the generator output with a DC DVM and set RV301* for 0V ± 5mV.

5.6.4 Set up the following:

GENERATOR Bias 40V [VB40]

Measure the generator output with DC DVM. Adjust RV202 BD15 for 40V ± 60mV

5.6.5 Set up the following:

GENERATOR Bias -40V [VB-40]

Check the generator output with a DC DVM for -40V ± 200mV note the reading.

5.6.6 Set up the following:

GENERATOR Bias 40V [VB40]

Check the generator output with DC DVM. Split the error between ± 40V with RV202 BD15 for 140V ± 100mV.

5.6.7 Set up the following:

GENERATOR Bias 0V [VB0]
Amplitude 3V [VA3]
SINGLE [SI]

Measure the generator output with an AC DVM. Check for 3V ± 0.1V. Note this reading.

5.6.8 Set up the following:

GENERATOR Frequency 65KHz [FR65E3]

Measure the generator output with an AC DVM. Check for the noted reading ± 0.1V

5.6.9 Set up the following:

GENERATOR Frequency 66KHz [FR66E3]

Measure the generator output with an AC DVM. Check for the noted reading ±0.1V. Check the generator output on the oscilloscope for an undistorted sine wave.

5.6.10 Set up the following:

GENERATOR Amplitude 305mV [VA.305]
Frequency 65KHz [FR65E3]

Measure the generator output with an AC DVM and note this reading.

5.6.11 Set up the following:

GENERATOR Frequency 66KHz [FR66E3]

Adjust RV701 for the noted reading as above ±30mV.

5.6.12 Set up the following:

GENERATOR	Amplitude	.7V	[VA.7]
SWEEP	W Log	100	[SF100]
NEXT	Frequency	1MHz	[FM1E6]
		20MHz	[FX20E6]
NEXT	Enable	log F	[SW2]
RECYCLE			[RE]

Monitor the generator output on an oscilloscope TERMINATED IN 50 ohms over the sweep. Note any high or low points, repeat the sweep adjusting CV301 for the flattest response.

5.6.13 Set up the following:

SELF-TEST	Initialise		[TT1]
RECYCLE			[RE]
GENERATOR	Bias	5V	[VB5]

Short circuit generator output and check for no error.

Set up the following:

GENERATOR Bias -5V [VB-5]

Check for no error.

Set up the following:

GENERATOR Bias 10V [VB10]

Check for generator overload error.

Set up the following:

GENERATOR Bias -10V [VB-10]

Check for generator overload error.

Remove the short circuit.

5.6.14 Connect a power supply positive lead via a 100Ω resistor to the generator lo and the negative to earth (ie channel 1 Hi outer) as in figure 8.

Apply +1V from the power supply and check for no error.

Apply -1V from the power supply and check for no error.

Apply +5V from the power supply and check for common mode error.

Apply -5V from the power supply and check for common mode error.

5.6.15 This completes the PCB 14 checks. Switch off and refit PCB 14 into its slot.

6 AUTO-CALIBRATION PROCEDURE

The auto-calibration of the 1255 analysers can be a single process in which the whole instrument is calibrated from scratch, or a number of 'patch' calibrations to repair a single point (refer to Appendix A). The calibration requires:

1. SCHLUMBERGER CAL. BOX (12606001).
2. W&G power meter.
3. 2 x BNC coax leads of the same length, and as short as possible.
4. 2 x 50Ω feedthrough terminators matched to within 0.1%.
5. LF (up to 1MHz) A.C. calibrator eg. FLUKE 5200.
6. Assorted BNC leads, always kept as short as possible

NOTE The calibration switch box needs to be characterised at 6 monthly intervals. When the W&G power meter is not being used the test head should be connected to the W&G output.

These should be connected together when the cal. box is characterised and not seperated from their calibration unit. The terminators should be marked with a channel number and should always be connected to the 1255 in accordance to their marking.

6.1 FULL CALIBRATION SEQUENCE

If the calibration box has not been characterised within the last six months the procedure in appendix B should be followed. This sets up a set of characterised values (one for each frequency and attenuation setting), which are stored as part of the auto-calibration program on micro-vax. These values compensate for any non-linearities in the frequency response of the calibration box. These characterised values are sent to the 1255 via the commands "CA f" in the following calibration procedure.

For voltage channel calibration, if the auto-calibrationprogram is available the 1255 should be connected to the A.C.calibrator, calibration box (12606001) and the GPIB controller via GPIB cables as in figure 1. The GPIB addresses should be set up and the front panel "Break" key should be pressed on the 1255 The 1255 auto-calibrationprogram should then be run.

The DIL switches on PCB22 are explained in Appendix C.

6.2 INITIALISATION

The unit is put in calibration mode by setting switch SW2 on PCB22 to 'CALIBRATE'. Ensure all eight DIL switches (SW1) on PCB22 are in the up position.

Calibrator Frequency	1255 Command	Reply	Comment
	TT1		Initialises 1255
	CM5		Clears cal. data

6.3 LF VOLTAGE ANALYSER CALIBRATION

Connect the BNC cables to the LF outputs of the calibration box. Connect the 1255 generator output to the calibration box generator input as in figure 2.

6.3.1 Sequence

Select 300mV from the calibrator, and program the cal.box to 0dB attenuation.

6.3.1.1 This section initialises the 1255 for the first pass calibration of the 3V range.

Calibrator Frequency	1255 Command	Reply	Comment
	TT1		Initialises 1255
			Wait 2 secs
	VA1.5		Sets 1.5 volts amplitude
	WF1		Selects square wave
	RA1,3		Calibrating 3 V range
	RA2,3		
	IS5		Integration time
	MS1		Delay for calibrator to settle
	CM0		Normal calibration mode
	SO1,2		Channel 1/Channel 2
	OU1,1		V1 outer floating
	OU2,1		V2 outer floating

6.3.1.2 This section calibrates the 1255 at each of the LF calibration points. A reply of '00' from the unit indicates a successful calibration, '01' is a failure.

Repeat the following sequence for each frequency in Appendix E from 200Hz to 125kHz inclusive.

Calibrator Frequency	1255 Command	Reply	Comment
	CA f		Ideal value for this frequency
f Hz	FR *f*		Sets frequency
	SI	00	1255 calibrated

6.3.1.3 This section sets up the 1255 for the first pass calibration of the 300mV range. Set the calibrator to 150mV output, and programme 0dB attenuation on the cal. box.

RA1,2		Calibrating 300mV range
RA2,2		

6.3.1.4 Repeat section 6.3.1.2

6.3.1.5 This section sets up the 1255 for the second pass calibration of the 3V range. This ensures that the amplitude and phase on the 3V range is matched to the 300mV range for both analysers.

Set the calibrator to 300mV output, and programme 0dB attenuation on the cal. box.

CM3	Select second pass mode
RA1,3	Matching 3V to 300mV
RA2,2	range

6.3.1.6 Repeat section 6.3.1.2

6.3.1.7 This section sets up the 1255 for the first pass calibration of the 30mV range. Set the calibrator to 1.5V output, and programme 34dB attenuation on the cal. box.

CM0	
RA1,1	Calibrating 30mV range
RA2,1	

6.3.1.8 Repeat section 6.3.1.2

6.3.1.9 This section sets up the 1255 for the second pass calibration of the 30mV range. This ensures that the amplitude and phase on the 30mV range is matched to the 300mV range for both analysers.

Set the calibrator to 300mV output, and programme 20dB attenuation on the cal. box.

CM3	
RA1,1	Matching 30mV to 300mV
RA2,2	range

6.3.1.10 Repeat section 6.3.1.2

6.3.1.11 LF Verification

Note: Verify must be done with the generator calibration disabled. Thus the DIL switch should be set to:

A verification of the LF auto-cal should take place in normal mode, after the LF calibration. The initial sequence is:

1. Set the unit to NORMAL (SW2 on PCB22)

2. Issue the following commands:

TT1	Initialise
Wait for initialise to complete, about 2 secs	
IS1	Integration time 1 sec
MS0.5	Measurement delay 0.5secs
SO1,2	Source V1/V2
CV1	Magnitude and phase coordinates
OP2,1	Data Output to GPIB on

3. Then setup as per 3V/3V overcheck (section 7.3.6) and check the points in Appendix E, between 200Hz and 125kHz inclusive, against the limits given at the end of 6.3.1.11.

4. Then setup as per 3V/300mV overcheck (section 7.3.8) and check the points in Appendix E, between 200Hz and 125kHz inclusive, against the limits given below.

5. Then setup as per 300mV/300mV overcheck (section 7.3.9) and check the points in Appendix E, between 200Hz and 125kHz inclusive, against the limits given below.

6. Then setup as per 300mV/30mV overcheck (section 7.3.10) and check the points in Appendix E, between 200Hz and 125kHz inclusive, against the limits given below.

7. Then setup as per 30mV/30mV overcheck (section 7.3.11) and check the points in Appendix E, between 200Hz and 125kHz inclusive, against the limits given below.

Limits

0.9995 =< Magnitude =< 1.0005
-0.05deg =< Phase =< 0.05deg

6.4 HF VOLTAGE ANALYSER CALIBRATION (>125KHZ)

6.4.1 Sequence

6.4.1.1 Connect the unterminated ends of the BNC cables to the HF outputs of the calibration box. Connect the terminated ends of the BNC cables to INPUT V1 and INPUT V2 of the 1255.

NOTE the BNC cables must have matched 50Ω terminators. Connect the 1255 generator output to the calibration box AGC input via an unterminated BNC cable as in figure 6.

Set switch SW2 on PCB22 to 'CALIBRATE'. Ensure all eight DIL switches SW1 on PCB22 are in the up position.

Calibrator Frequency	1255 Command	Reply	Comment
	TT1		Initialises 1255 Wait 2 secs
	VA1		Sets 1 volt amplitude
	IS5		Integration time
	MS20		Delay for cal.box to settle
	CM0		Normal, calibration mode
	SO1,2		Channel 1 / Channel 2
	FR145E3		First calibration point
	SI	01 or 00	Dummy to allow cal.box and W&G to settle

6.4.1.2 This section sets up the 1255 for the first pass calibration of the 3 V range, program the cal. box to attenuate the signal with 14dBs.

RA1,3	Calibrating 3V range
RA2,3	Calibrating 3V range
CA a	Ideal value, obtained via characterisation (refer to Appendix B)

6.4.1.3 This next section calibrates the 1255 at each of the HF calibration points. A reply of '00' from the unit indicates a successful calibration, '01' is a failure.

Repeat the following sequence of instructions for each frequency in Appendix E from 145E3Hz to 20E6Hz. Note, a measurement delay of 20 secs is required for the 145kHz measurement but all the rest only require 5 secs.

Sequence of instructions for the first point:

MS20	-	Delay for first point
FR145E3	-	Frequency
SI	00	Calibrate
MS5	-	Delay for other points
FR *f*	-	Frequency
SI	00	Calibrate

6.4.1.4 This section sets up the 1255 for the first pass calibration of the 300mV range, program the cal. box to attenuate the signal with 20dBs.

RA1,2	Calibrating 300mV range
RA2,2	-
CA b	Ideal value, obtained at characterisation (refer to Appendix B)

6.4.1.5 Repeat section 6.4.1.3.

6.4.1.6 This section sets up the 1255 for the first pass calibration of the 30mV range, program the cal. box to attenuate the signal with 34dBs.

RA1,1	Calibrating 30mV range
RA2,1	
CA c	Ideal value, obtained. at characterisation. (refer to Appendix B)

6.4.1.7 Repeat section 6.4.1.3.

6.4.1.8 This section sets up the 1255 for the second pass calibration of the 3 V range, program the cal. box to attenuate the signal with 14dBs.

CM3	Second pass mode
RA1,3	Calibrating 3 V range
RA2,2	
CA a	Ideal value, obtained. at characterisation. (refer to Appendix B)

6.4.1.9 Repeat section 6.4.1.3.

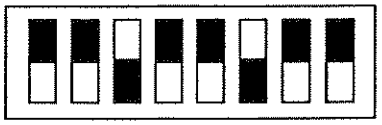
6.4.1.10 This section sets up the 1255 for the second pass calibration of the 30mV range, program the cal. box to attenuate the signal with 34dBs.

RA1,1	Calibrating 30mV range
RA2,2	
CA c	Ideal value, obtained. at characterisation. (refer to Appendix B)

6.4.1.11 Repeat section 6.4.1.3.

6.3.1.12 HF Verification

Note: Verify must be done with the generator calibration disabled. Thus the DIL switch should be set to:



A verification of the HF auto-cal should take place in normal mode, after the HF calibration. The initial sequence is:

1. Set the unit to NORMAL (SW2 on PCB22)

2. Issue the following commands:

TT1	Initialise
Wait for initialise to complete, about 2 secs	
IS1	Integration time 1 sec
MS0.5	Measurement delay 0.5secs
SO1,2	Source V1/V2
CV1	Magnitude and phase coordinates
OP2,1	Data Output to GPIB on

3. Then setup as per 3V/3V overcheck (section 7.3.6) and check the points in Appendix E, between 145kHz and 120MHz inclusive, against the limits given at the end of 6.3.1.11.

4. Then setup as per 3V/300mV overcheck (section 7.3.8) and check the points in Appendix E, between 145kHz and 120MHz inclusive, against the limits given below.

5. Then setup as per 300mV/300mV overcheck (section 7.3.9) and check the points in Appendix E, between 145kHz and 120MHz inclusive, against the limits given below.

6. Then setup as per 300mV/30mV overcheck (section 7.3.10) and check the points in Appendix E, between 145kHz and 120MHz inclusive, against the limits given below.

7. Then setup as per 30mV/30mV overcheck (section 7.3.11) and check the points in Appendix E, between 145kHz and 120MHz inclusive, against the limits given below.

Limits

Frequency =< 1MHz
0.9995 =< Magnitude =< 1.0005
-0.05deg =< Phase =< 0.05deg

Frequency =< 10MHz
0.9975 =< Magnitude =< 1.0025
-0.25deg =< Phase =< 0.25deg

Frequency > 10MHz
0.995 =< Magnitude =< 1.005
-0.5deg =< Phase =< 0.5deg

6.5 GENERATOR CALIBRATION OF 1255

The generator calibration of the 1255 is achieved using its own analysers, so the unit must have had these calibrated.

6.5.1 Connections

Connect a short BNC cable (less than 20cm) to the 1255 generator output, and connect the other end to INPUT V1 hi on the 1255.

6.5.2 Sequence

6.5.2.1 This section initialises the 1255 for the generator calibration. Set switch SW2 on PCB22 to "CALIBRATE". Ensure all eight DIL switches SW1 on PCB22 are in the up position.

Calibrator Frequency	1255 Command	Reply	Comment
	TT1		Initialises 1255
			Wait 2 secs
	VA1		Sets 1 volt amplitude
	RA1,3		Sets 3 V range
	IS10		Integration time
	MS5		Delay for cal.box to settle
	CM4		Generator calibration mode
	SO1,0		Channel 1

6.5.2.2 This next section calibrates the 1255 at each of the HF calibration points. A reply of '00' from the unit indicates a successful calibration, '01' is a failure.

Repeat the following sequence of instructions for all the frequencies in Appendix F.

Calibrator Frequency	1255 Command	Reply	Comment
	FR*f*	-	Frequency
	SI	00	Calibrate

6.6 CONCLUSION

The unit is now calibrated, and requires that the date and place of calibration be stored.

-	PC text (4 chars)	-	Code for the place of calibration: GB-F is SCHLUMBERGER, FARNBOROUGH
-	YR i	-	Year of calibration, eg. 88
-	WK i	-	Week of calibration 1 to 53

Set the calibration switch (SW1 on PCB22) to 'NORMAL', set all the DIL switches (SW2 on PCB22) to the up position and then initialise the instrument.

-	TT1	-	Initialise the 1255

This completes the 1255 Calibration.

7 FUNCTIONAL OVERCHECK

Overcheck should be carried out at a temperature in the range 17-230C

The overcheck can be carried out using either the front panel, the serial interface or the GPIB to input the commands for Section 7.1 onwards. The remote commands corresponding to key entries are given in [ ]; however, the full details of implementing remote operation via the GPIB will depend on which controller is used and are therefore not given here. For serial interface, results will be returned to the VDU or terminal by commanding OP1,1.

The tests can be done either manually following the procedures of Section 7.1 or by using ATE program 12556599 as specified in Section 8.1.

If the analyser or generator accuracy overcheck fails, it may be necessary to recalibrate a single point using the procedure set out in Appendix A, or to repeat the entire calibration procedure.

Ensure that all eight DIL switches on PCB22 (SW1) are in the up position and that the calibration switch (SW2) is set to normal. Also ensure that the keyswitch on the rear panel is set to normal.

7.1 DISPLAY CHECK

Set up the following:

SELF-TEST	Initialise	[TT1]	wait for 2 seconds
SELF-TEST	Test	[TT0]	

7.1.1 Carefully observe the display for missing dots and signs of short circuits between rows as the moving pattern cycles round.

7.1.2 Press Enter, then carefully observe the next pattern for evidence of short circuits between columns.

7.1.3 Press Enter, then carefully observe the pattern of characters to check that each one is correctly displayed.

7.1.4 Press Enter, then press each key in turn terminating with Enter, checking that the 1255 gives the correct response to each key and finishes with the TEST PASS message.

7.2 SERIAL INTERFACE

Connect an RS423 terminal to the 1255 serial interface port, ensure the are both at the same baud rate and type in TT1 (Carriage return). Check that the display indicates INITIALISED.

7.2.1 Command the following using the terminal

```
FR 300
VA  3
SO 1,0
CV  1
RE
```

Connect Channel 1 to the Generator output and note that the 1255 is now taking readings at 300Hz and that the display is being updated with Co-ordinates set to r,theta.

7.2.2 Command OP1,1 and observe that readings are printed on the terminal.

7.2.3 Command OP1,0 and remove the terminal.

7.3 ANALYSER CHECK

set up the following:

SELF-TEST	Initialise		[TT1]
GENERATOR	Frequency	300Hz	[FR300]
	Amplitude	2V	[VA2]
ANALYSER			
NEXT	V1 outer	floating	[OU1,1]
DISPLAY	Source	Ch1	[SO1,0]
	Coords	r theta	[CV1]
RECYCLE			[RE]

7.3.1 Phase lock the Calibrator to the Generator output and connectthe Calibrator output to Channel 1 input, ensuring that the Calibrator Lo output is not connected to ground. Command [WF1] over the GPIB.

Note The calibrator outputs in table 7.4.2 are the nominal values and must be replaced by the characterised value as obtained in appendix D. The characterisation must be repeated at least once every 6 months.

7.3.2 Check that the following voltages are measured correctly on Channel 1

Frequency	**Input Range**	**Calibrator O/P nominal**	**Reading**	**Comment**
310Hz	30mV	200mV	19.96 to 20.04mV	[FR310;RA1,1]
*310Hz	30mV	300mV	No overload indicated	
310Hz	300mV	200mV	199.60 to 200.40mV	[RA1,2]
310Hz	3V	2V	1.9960 to 2.0040mV	[RA1,3]
310Hz	3V	3V	2.9940 to 3.0060V	
310Hz	3V	1V	0.9980 to 1.0020V	
310Hz	3V	0.5V	0.4990 to 0.5010V	
310Hz	3V	0.2V	0.1990 to 0.2010V	
310Hz	3V	0.1V	0.0990 to 0.1010V	
3KHz	30mV	2V	19.96 to 20.04mV	[FR3E3;RA1,1]
* 3KHz	30mV	2.5V	No overload indicated	
* 3KHz	300mV	200mV	199.6 to 200.4mV	[RA1,2]
3KHz	3V	2V	1.9960 to 2.004mV	[RA1,3]
*60KHz	30mV	200mV	19.96 to 20.06mV	[FR6E4;RA1,1]
60KHz	300mV	200mV	199.4 to 200.6mV	[RA1,2]
60KHz	3V	2V	1.9940 to 2.006mV	[RA1,3]
100KHz	30mV	200mV	19.88 to 20.12mV	[FR1E5;RA1,1]
*100KHz	300mV	200mV	198.8 to 201.2mV	[RA1,2]
100KHz	3V	2V	1.988 to 2.012mV	[RA1,3]
145KHz	30mV	200mV	19.88 to 20.12mV	[FR145E3;RA1,1]
*145KHz	300mV	200mV	198.8 to 201.2mV	[RA1,2]
145KHz	3V	2V	1.988 to 2.012mV	[RA1,3]

Repeat for Channel 2.
* = select 20dB attenuator

7.3.3 Common Mode

Apply the signal from the Calibrator output HI to both Hi and Lo terminals of Channel 1 and the calibrator Lo to the shield. Set up the following:

GENERATOR	Frequency	10Hz	[FR10]
	Amplitude	3V	[VA3]
ANALYSER			
NEXT	Input (V1)	DIFF	[IP1,1]
	Range	300mV	[RA1,2]
RECYCLE			[RE]

Command [WF1] over the GPIB. Apply 3 Volts common mode. Check that this common mode signal is rejected for Channel 1 as follows:

Frequency	Input Range	Calibrator O/P	Reading
10Hz	300mV	3V	<3mV

Repeat for Channel2.

7.3.4 Analysers Channel to Channel

Overcheck analyser matching from 1Hz to 100kHz

Connect the generator to channels 1 and 2 via a power splitter as in figure 9.
Set up the following:

SELF-TEST	Initialise		[TT1]
ANALYSER	Int. time	0.3sec	[IS0.3]
DISPLAY	Source	V1/V2	[SO1,2]
SWEEP	Δ log	400pts/swp	[SF400]
NEXT	Frequency	1Hz	[FM1]
		100KHz	[FX1E5]
NEXT	Enable	log f	[SW2]
DATA OP	File	all	[OP3,1]

7.3.5 Learn the following program

LEARN PROG	Learn	1	[#L1]
DATA OUTPUT			
PREV	Stats	par 1	[SX0]
SCALE	Limits	par 1	[LI1]
		0.9985	[LV0,0.9985]
		1.0015	[LV1,1.0015]
LIST FILE			[FO]
PAUSE/CONT			[CP]
DATA OUTPUT			
PREV	Stats	par 2	[SX1]
SCALE	Limits	par 2	[LI2]
		0.2	[LV0,-0.2]
		-0.2	[LV1,0.2]
LIST FILE			[FO]
	Quit		[#Q]

7.3.6 Set up the following

GENERATOR	Amplitude	3V	[VA3]
ANALYSER			
NEXT	Range	3V	[RA1,3]
NEXT	Range	3V	[RA2,3]
RECYCLE			[RE]

7.3.7 When the sweep is over set up the following

EXECUTE	1	[EP1]

Check the display for no failures.

STATUS		
NEXT	Stats	
	read minimum value	[?MI]
	read maximum value	[?MA]

Check these values against the magnitude limits.

PAUSE/CONTINUE	[CP]

Check the display for no failures.

STATUS		
NEXT	Stats	
	read minimum value	[?MI]
	read maximum value	[?MA]

Check these values against the phase limits.

7.3.8 Set up the following

GENERATOR	Amplitude	1.2V	[VA1.2]
ANALYSER			
NEXT	Range	3V	[RA1,3]
NEXT	Range	300mV	[RA2,2]
RECYCLE			[RE]

repeat test 7.3.7

7.3.9 Set up the following

GENERATOR	Amplitude	0.6V	[VA0.6]
ANALYSER			
NEXT	Range	300mV	[RA1,2]
NEXT	Range	300mV	[RA2,2]
RECYCLE			[RE]

repeat test 7.3.7

7.3.10 Set up the following

GENERATOR	Amplitude	0.12V	[VA0.12]
ANALYSER			
NEXT	range	300mV	[RA1,2]
NEXT	range	30mV	[RA2,1]
RECYCLE			[RE]

repeat test 7.3.7

7.3.11 Set up the following:

GENERATOR	Amplitude	0.06V	[VA0.06]
ANALYSER			
NEXT	range	30mV	[RA1,1]
NEXT	range	30mV	[RA2,1]
RECYCLE			[RE]

repeat test 7.3.7.

7.3.12 Overcheck from 100kHz to 1MHz.

SWEEP	Δ lin	100pts/swp	[LF100]
NEXT	Frequency	100kHz	[FM1E5]
		1MHz	[FX1E6]
NEXT	Enable	lin f	[SW1]
DATA OP	File	all	[OP3,1]

Repeat from section 7.3.6 to section 7.3.11.

7.3.13 Overcheck from 1MHz to 10MHz.

SWEEP			
NEXT	Frequency	1MHz	[FM1E6]
		10MHz	[FX1E7]
NEXT	Enable	lin f	[SW1]
DATA OP	File	all	[OP3,1]

learn the following program or edit the limits in the program learnt in section 7.3.5.

LEARN PROG	Learn	1	[#L1]
DATA OUTPUT			
PREV	Stats	par 1	[SX0]
SCALE	Limits	par 1	[LI1]
		0.9925	[LV0,0.9925]
		1.0075	[LV1,1.0075]
LIST FILE			[FO]
PAUSE/CONTINUE			[CP]
DATA OUTPUT			
PREV	Stats	par 2	[SX1]
SCALE	Limits	par 2	[LI2]
		0.75	[LV0,-0.75]
		-0.75	[LV1,0.75]
LIST FILE			[FO]
	Quit		[#Q]

Repeat from section 7.3.6 to section 7.3.11.

7.3.14 Overcheck from 10MHz to 20MHz.

GENERATOR	Amplitude	1V	[VA1]
SWEEP			
NEXT	Frequency	10MHz	[FM1E7]
		20MHz	[FX2E7]
NEXT	Enable	lin f	[SW1]
DATA OP	File	all	[OP3,1]

Learn the following program or edit the limits in the program learnt in section 7.3.5.

LEARN PROG	Learn	1	[#L1]
DATA OUTPUT			
PREV	Stats	par 1	[SX0]
SCALE	Limits	par 1	[LI1]
		0.9625	[LV0,0.9625]
		1.0375	[LV1,1.0375]
LIST FILE			[FO]
PAUSE/CONTINUE			[CP]
DATA OUTPUT			
PREV	Stats	par 2	[SX1]
SCALE	Limits	par 2	[LI2]
		-3.75	[LV0,-3.75]
		3.75	[LV1,3.75]
LIST FILE			[FO]
	Quit		[#Q]

Repeat from section 7.3.8 to section 7.3.11.

7.3.15 Connect the Generator output to the 1255 test box and the analyzers terminated in 50 ohms to the 1255 test box hf channel 1 and channel 2 outputs as in figure 6.

7.3.16 Set up the following:

GENERATOR	Amplitude	1V	[VA1]
ANALYSER			
NEXT	Range	3V	[RA1,3]
NEXT	Range	3V	[RA2,3]
RECYCLE			[RE]

repeat test 7.3.7.

7.3.17 Call up the -14dB attenuator in the calibration box and set up the following:

ANALYSER			
NEXT	Range	3V	[RA1,3]
NEXT	Range	300mV	[RA2,2]
RECYCLE			[RE]

repeat test 7.3.7

7.4 GENERATOR CHECK

7.4.1 Set up the following:

SELF-TEST	Initialise		[TT1]
GENERATOR	Frequency	50mHz	[5E-2]
	Amplitude	1V	[VA1]

7.4.2 Connect the Frequency Counter to the Generator output terminals, program each of the following output frequencies in turn and check that the frequency counter gives the correct reading (measuring period at the lower frequencies):

Frequency	Counter	
50mHz	19.998 to 20.002msec	[FR0.05]
500mHz	1.9998 to 2.0002msec	[FR0.5]
2.5Hz	399.98 to 400.02msec	[FR2.5]
25Hz	24to 26Hz	[FR25]
250Hz	249 to 251Hz	[FR250]
700Hz	699.9 to 700.1Hz	[FR700]
1kHz	0.9999 to 1.0001kHz	[FR1E3]
2kHz	1.9998 to 2.0002kHz	[FR2E3]
3kHz	2.9997 to 3.0003kHz	[FR3E3]
4kHz	3.9996 to 4.0004kHz	[FR4E3]
5kHz	4.9995 to 5.0005kHz	[FR5E3]
6kHz	5.9994 to 6.0006kHz	[FR6E3]
30kHz	29.998 to 30.002kHz	[FR3E4]
50kHz	49.995 to 50.005kHz	[FR5E4]
70KHz	69.993 to 70.007KHz	[FR7E4]
100kHz	99.99 to 100.01kHz	[FR1E5]
600kHz	599.94 to 600.06kHz	[FR6E5]
700KHz	699.93 to 700.07KHz	[FR7E5]
1MHz	0.9999 to 1.0001MHz	[FR1E6]
6MHz	5.9996 to 6.0006MHz	[FR6E6]
7MHz	6.9993 to 7.0007MHz	[FR7E6]
20MHz	19.998 to 20.002MHz	[FR2E7]

Disconnect the Frequency Counter.

7.4.3 Generator kill

Connect a short circuit across the Generator Kill inputs (rear panel) and observe the Generator output on the oscilloscope, the Generator output should drop to zero and an error be displayed.

Release the Generator Kill inputs and observe the output waveform re-commence. Remove the oscilloscope.

7.4.4 Set up the following:

GENERATOR Frequency 300Hz [FR300]

Measure the following Generator outputs on Channel 1 and check that the readings are within the limits stated:

Amplitude	Limits	
3V	2.92 to 3.08V	[VA3]
1V	0.97 to 1.03V	[VA1]
0.8V	0.775 to 0.825V	[VA0.8]
0.6V	0.580 to 0.620V	[VA0.6]
0.4V	0.385 to 0.415V	[VA0.4]
0.2V	0.190 to 0.210V	[VA0.2]
0.1V	0.092 to 0.108V	[VA0.1]
0.02V	0.015 to 0.025V	[VA0.02]
0.01V	0.005 to 0.015V	[VA0.01]

7.4.5 Connect a DVM across the Generator output terminals.

Set the bias voltages (V.Bias) as follows, and for each voltage check that the DVM reading is within the limits:

Bias	**DVM reading**	
40V	39.5 to 40.5V	[VB 40]
20V	19.7 to 20.3V	[VB 20]
10V	9.94 to 10.06V	[VB 10]
7V	6.96 to 7.04V	[VB 7]
3V	2.98 to 3.02V	[VB 3]
1V	0.98 to 1.02V	[VB 1]
0.02V	0.010 to 0.030V	[VB0.02]
0.01V	0.000 to 0.020V	[VB0.01]
0V	-0.010 to 0.010V	[VB 0]
-1V	-0.98 to -1.02V	[VB -1]
-3V	-2.98 to -3.02V	[VB -3]
-7V	-6.96 to -7.04V	[VB -7]
-10V	-9.94 to -10.06V	[VB -10]
-20V	-19.70 to -20.3V	[VB -20]
-40V	-39.5 to -40.5V	[VB -40]

7.4.6 Connect the generator output to channel 1 using a very short cable. Set up the following:

SELF-TEST	Initialise		[TT1]
GENERATOR	Amplitude	1V	[VA1]
SWEEP	ΔLog	100pts	[SF100]
NEXT	frequency	1Hz	[FM1}
		20MHz	[FX20E6]
NEXT	enable	logF	[SW2]
DISPLAY	Source	Ch1	[SO1,0]
	Coords	R,Theta	[CV1]
DATA O/P	FILE	All	[OP3,1]
RECYCLE			[RE]

When the sweep is over check the file for a generator accuracy of:

Programmed output ±5% ±10mV ±1%/MHz above 1MHz

i.e. upper limit = 1V +50mV +10mV +10mV/MHz above 1MHz
lower limit = 1V -50mV -10mV -10mV/MHz above 1MHz

7.4.7 Set up the following:

GENERATOR	Amplitude	0.2V	[VA0.2]
RECYCLE			[RE]

When the sweep is over check the file for a generator accuracy of:

Programmed output ±5% ±10mV ±1%/MHz above 1MHz

i.e. upper limit = 200mV +10mV +10mV +2mV/MHz above 1MHz
lower limit = 200mV -10mV -10mV -2mV/MHz above 1MHz

7.4.8 Set up the following:

SWEEP	Enable	off	[SW0]
GENERATOR	Frequency	100kHz	[FR100E3]
	Amplitude	20mV	[VA0.02]
RECYCLE			[RE]

Check displayed results are in the range 20mV ±5mV

7.4.9 Set up the following

SELF-TEST	Initialise		[TT1]
GENERATOR	Amplitude	3V	[VA3]
	Bias	40.95V	[VB40.95]
ANALYSER			
NEXT	Input	AC	[DC1,1]
NEXT	Input	AC	[DC2,1]
DISPLAY	Coords	R,Theta	[CV1]
RECYCLE			[RE]

Check for no overloads and that the reading is 1±0.002

Set up the following:

DISPLAY	Source	Ch1	[SO1,0]

Check the display reads 3V ±0.15V

7.4.10 Set the keyswitch to Supervisor mode.

Set up the following:

SELF-TEST	Initialise	[TT1]

Set the keyswitch back to normal when the 1255 displays *Initialised* and press BREAK

7.4.11 This completes the overcheck not using ATE program 12556599

This completes the 1255 Overcheck.

8 OVERCHECK USING ATE PROGRAM 12556599

8.1 ATE PROGRAM

Run the checkout program following the instructions specified in 12556599.

8.1.2 Serial Interface.

Equipment: Texas Silent 700 terminal, or equivalent (e.g. VDU) with baud rate set to 300 baud.

8.1.2.1 Connect the terminal to the 1255 serial interface port and type in TT1 (Carriage Return). Check that the display indicates INITIALIZED.

8.1.2.2 Command the following using the terminal:

```
FR  300
VA   3
SO  1,0
CV   1
RE
```

Connect Channel 1 to the Generator Output and note that the 1255 is now taking readings at 300Hz and that the display is being updated with Co-ordinates set to r,theta.

8.1.2.3 Command OP1,1 and observe that readings are printed on the terminal.

8.1.2.4 Command OP1,0 and remove the terminal.

8.1.3 Press: SELF-TEST Initialise [TT1]

This completes the overcheck with ATE program 12556599.

This completes the 1255 Overcheck using ATE Program.

APPENDIX A

SINGLE POINT CALIBRATION

This procedure should be followed to repair any "bad" calibration points.

A.1 General

The 1255 is set to calibration mode by setting switch SW2 on PCB22 to 'CALIBRATE', and initialising the instrument. Ensure the eight DIL switches (SW1) on PCB22 are all in the up position.

The frequency point to be calibrated is selected by programming the generator to the appropriate frequency. This must be one of the calibration frequencies.

The channel being calibrated is selected by the display source, and may be any of Ch1, Ch2, Ch1/Ch2 or Ch2/Ch1. The latter two are the best two as these calibrate both channels from the same measurement, achieving greater point to point accuracy.

The range being calibrated is selected by setting the appropriate analyser range.

The calibration mode must be set, using the CM command. There are six arguments:

0 - Normal, single range calibration. (first pass)
1 - Magnitude only, single range calibration. (first pass)
2 - Phase only, single range calibration.(first pass)
3 - Normal, cross range calibration, used to achieve range to range crossover matching. Both channels must be being calibrated, with one on the 300mV range, and the other on either the 3 V or the 30mV range.The input should be either 300mV or 30mV respectively. (second pass)
4 - Generator calibration.
5 - Vf calibration mode.
6 - Clears the calibration data, CAREFUL.

If the calibration box has not been characterised within the last six months the procedure in appendix B should be followed. This sets up a set of characterised values (one for each frequency and attenuation setting), which are stored as part of the auto-calibration program on micro-vax. These values compensate for any non-linearities in the frequency response of the calibration box. These characterised values are sent to the 1255 via the commands "CA 0,f" in the following calibration procedure.

A.2. An LF single point calibration (≤ 125kHz)

It is always best when calibrating a single point, to calibrate both channels on all three ranges, with a first pass calibration and a second pass calibration. A typical sequence for the 100 kHz calibration point would be:

A.2.1 Connect the unterminated ends of the BNC cables to the LF outputs of the calibration box. Connect the ends of the BNC cables to INPUT V1 and INPUT V2 of the 1255. Connect the 1255 unterminated BNC cable as in figure 2.

Select 300mV from the calibrator, and program the cal. box to 0dB attenuation.

Set switch SW2 on PCB22 to 'CALIBRATE'. Ensure all eight DIL switches (SW1) on PCB22 are in the up position.

Calibrator Frequency	1255 Command	Reply	Comment
	TT1		Initialises 1255
100 kHz	FR100E3		Repairing 100kHz cal. point
	SO1,2		Ch1/Ch2
	VA1.5		Generator amplitude = 1.5V
	IS5		Integration time
	MS5		Delay to allow calibrator to settle
	CM0		Normal first pass
	OU1,1		V1 outer floating
	OU2,1		V2 outer floating
	RA1,3		3 V
	RA2,3		3 V
	CA f		Real value of input magnitude
	SI	00	Calibrate

A.2.2 Select 150mV from the calibrator, and program the cal. box to 0dB attenuation.

RA1,2		300mV
RA2,2		300mV
CA f		Real value of input magnitude
SI	00	Calibrate

A.2.3 Select 300mV from the calibrator, and program the cal. box to 20dB attenuation.

RA1,1		30mV
RA2,1		30mV
CA f		Real value of input magnitude
SI	00	Calibrate

A.2.4 Select 300mV from the calibrator, and program the cal. box to 0dB attenuation.

CM3		Second pass calibration
RA1,3		3 V
RA2,2		300mV
SI	00	Calibrate

A.2.5 Select 300mV from the calibrator, and program the cal. box to 20dB attenuation.

RA1,1		30mV
RA2,2		300mV
SI	00	Calibrate

A.2.6 Set the switch on PCB22 to 'NORMAL'.

TT1		Initialise the 1255

A.3 A HF single point calibration (>125kHz)
A typical sequence for the 1 MHz calibration point would be:

A.3.1 Connect the unterminated ends of the BNC cables to the HF outputs of the calibration box. Connect the terminated ends of the BNC cables to INPUT V1 and INPUT V2 of the 1255.

NOTE The BNC cables must have matched 50Ω terminators. Connect the 1255 generator output to the calibration box generator input via an unterminated BNC cable as in figure 6.

Program the cal. box to 14dB attenuation.

Set switch SW2 on PCB22 to 'CALIBRATE'.

Ensure all eight switches on DIL switch SW1 on PCB22 are in the up position.

Calibrator Frequency	1255 Command	Reply	Comment
	TT1		Initialises 1255
	FR1E6		Repairing 1MHz cal. point
	SO1,2		Ch1/Ch2
	VA1		Generator output
	OP2,1		Output data to GPIB
	MS20		Delay for W&G to settle after power on
	SI	RESULT	The 1255 replies with the result of the measurement, followed by '00' or '01': a total of 6 numbers. These should be ignored
	OP2,0		No data output to GPIB
	IS5		Integration time
	MS5		Delay to allow cal. box to settle
	CM0		Normal first pass
	RA1,3		3 V
	RA2,3		3 V
	CA f		Real value of input magnitude
	SI	00	Calibrate

A.3.2 Program the cal. box to 20dB attenuation.

	RA1,2		300mV
	RA2,2		300mV
	CA f		Real value of input magnitude
	SI	00	Calibrate

A.3.3 Program the cal. box to 34dB attenuation.

RA1,1		30mV
RA2,1		30mV
CA f		Real value of input magnitude
SI	00	Calibrate

A.3.4 Program the cal. box to 14dB attenuation.

CM3		Second pass calibration
RA1,3		3 V
RA2,2		300mV
SI	00	Calibrate

A.3.5 Program the cal. box to 34dB attenuation.

RA1,1		30mV
RA2,2		300mV
SI	00	Calibrate

A.3.6 Set the switch on PCB22 to 'NORMAL'.

TT1		Initialise the 1255

Appendix B

CHARACTERISATION OF CALIBRATION BOX AT LF (<125KHZ)

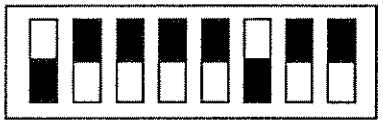
The purpose of this section is to characterise the calibration box at low frequency. The procedure for doing this is to connect the A.C. calibrator directly to the 1255 (i.e. not through the calibration box). Inputs V1 and V2 of the 1255 arethen calibrated on the 300mV range. The 1255 is then switched out of calibration mode and the calibration box is inserted between the A.C. calibrator and the 1255. The same calibration frequency points are measured by the 1255 at three amplitude levels (300mV, 150mV and 30mV) which are the amplitudes used to calibrate the 3V, 300mV and 30mV ranges respectively. This setof results is stored in an array in the controller (micro-vax)and represent the actual voltages which are output by thecalibration box at each frequency and amplitude setting on the A.C. calibrator. These actual calibration levels are sent to the 1255 via the command "CA f" which is refered to in theAuto-calibration procedure.

The result of this procedure is an array of 3*18 characterisation values corresponding to the low frequency calibration points. These are used as the ideal values sent tothe 1255 for the low frequency calibration at 300mV, 150mV and 30mV for the 3 V, 300mV and the 30mV ranges respectively.

B.1 CALIBRATION OF THE THE 300MV RANGE

B.1.1 Connections

1. Connect GPIB to A.C. calibrator, 1255 and the controller
2. Set A.C. calibrator to address 22
   Set A.C. calibrator to remote
3. Set 1255 to talker/listener at address 0
   Set keyswitch to NORMAL
   Set switch on PCB22 to 'CALIBRATE'
   Set DIL switch on PCB22 to:



4. Connect 1255 generator to A.C. calibrator phase-lock input: use an unterminated BNC cable
5. Connect FLUKE output to 1255 Channel 1, high, input: use an unterminated BNC cable

B.1.2 Sequence

B.1.2.1 This section initialises the 1255 for the calibration of channel 1 on the 300mV range. Set the A.C. calibrator to 150mV.

Calibrator Frequency	1255 Command	Reply	Comments
	TT1		Initialises 1255
			Wait 2 secs
	VA3		Sets 3 volts amplitude
	WF1		Selects square wave
	RA1,2		Calibrating 300mV range
	RA2,2		
	IS10		Integration time
	MS5		Delay for FLUKE to settle
	CM0		Normal calibration mode
	SO1,0		Channel 1 only
	CA0.15		Selects ideal value to 150mV

B.1.2.2 This next section calibrates the 1255 at each of the LF calibration points. A reply of '00' from the unit indicates a successful calibration, '01' is a failure.

The following sequence of instructions should be repeated for all frequencies in Appendix E from 200Hz to 125kHz inclusive.

Calibrator Frequency	1255 Command	Reply	Comment
f Hz	FR *f*		Sets frequency
	SI	00	1255 calibrated

B.1.2.3 This section alters the 1255 for the calibration of channel 2 on the 300mV range. Change the output of the FLUKE from channel 1 high to channel 2 high.

SO2,0	Channel 2 only

B.1.2.4 Repeat section B.1.2.2

B.2 CHARACTERISE THE BUFFER

B.2.1 Connections

Connect the 1255 to the calibration box 12556001 as in figure 2.

B.2.2 Sequence

B.2.2.1 This section initialises the 1255 for the characterisation of the buffer by the calibrated 1255 300mV range.

1255	Fluke	Reply	Comments
	TT1		Initialises 1255
			Wait 2 secs
	VA1.5		Sets 1.5 volts amplitude
	RA1,2		Calibrating 300mV range
	RA2,2		
	OU1,1		V1 outer floating
	OU2,1		V2 outer floating
	IS10		Integration time
	MS5		Delay for FLUKE to settle
	SO1,2		Channel 1 / Channel 2
	OP2,1		Output all to GPIB
	OP3,1		Output all to file
	CV1		Coordinates, R,theta
	FC		Clear the file

B.2.2.2 This next section measures the buffer output at each of the LF calibration points at about 300mV: the 3V calibration value. The 1255 replies after each measurement with the frequency, magnitude, phase, error code and limit check result: 5 numbers. These are used to synchronise the controller.

Set the calibration box to 0dB: 300mV from the AC Calibrator.

B.2.2.3 Repeat section B.1.2.2

B.2.2.4 This section reads the measured values of the buffer output for channel 1 and stores them in the characterisation array

SO1,0	Channel 1
FO	List the file

Read in 18 measurement results, storing magnitude as characterisation values for 300mV.

SO2,0	Channel 2
FO	List the file

Read in18 measurements results, averaging magnitude with value already stored for channel 1, and store as ideal value for 300mV

B.2.2.5 This section resets the 1255 to characterise the buffer at 150mV.

SO1,2	Channel 1 / Channel 2
FC	Clear the file

B.2.2.6 This next section measures the buffer output at each of the LF calibration points at about 150mV: the 300mV calibration value. The 1255 replies after each measurement with the frequency, magnitude, phase, error code and limit check result: 5 numbers. These are used to synchronise the controller. Set the calibration box to 0dB: 150mV from the AC Calibrator.

B.2.2.7 Repeat section B.1.2.2

B.2.2.8 This section reads the measured values of the buffer output for channel 1 and stores them in the characterisation array

SO1,0	Channel 1
FO	List the file

Read in 18 measurement results, storing magnitude as characterisation values for 150mV.

SO2,0	Channel 2
FO	List the file

Read in 18 measurements results, averaging magnitude with value already stored for channel 1, and store as ideal value for 150mV

B.2.2.9 This section resets the 1255 to characterise the buffer at 30mV.

SO1,2	Channel 1 / Channel 2
FC	Clear the file

Insert between the buffer and the power splitter an accurate 20dB attenuator, marked so that it is used whenever these characterisation constants are used. Set the calibration box to 20dB: 300mV from the AC calibrator.

B.2.2.10 This next section measures the buffer output at each of the LF calibration points at about 30mV: the 30mV calibration value. The 1255 replies after each measurement with the frequency, magnitude, phase, error code and limit check result : 5 numbers. These are used to synchronise the controller.

B.2.2.11 Repeat section B.1.2.2

B.2.2.12 This section reads the measured values of the buffer output for channel 1 and stores them in the characterisation array

SO1,0	Channel 1
FO	List the file

Read in 18 measurement results, storing magnitude as characterisation values for 30mV.

SO2,0	Channel 2
FO	List the file

Read in 18 measurements results, averaging magnitude with value already stored for channel 1, and store as ideal value for 30mV

B.2.3 TIDY
Set DIL switch on PCB22 to:

TT1 Initialise the 1255

B.3 CHARACTERISATION OF HF CAL. BOX

The purpose of this section is to characterise the HF calibration box to ensure a smooth transition between the LF and HF region. It requires that the LF region be already calibrated.

B.4 SEQUENCE

B.4.1 Connect the unterminated ends of the BNC cables to the HF outputs of the calibration box. Connect the terminated ends of the BNC cables to INPUT V1 and INPUT V2 of the 1255. NOTE the BNC cables must have matched 50Ω terminators. Connect the 1255 generator output to the calibration box AGC input via an unterminated BNC cable.

This section initialises the 1255 for the characterisation of the cal. box at 125kHz. Set switch SW2 on PCB22 to 'NORMAL'. Ensure all eight switches on DIL switch SW1 on PCB22 are in the up position.

Calibrator Frequency	1255 Command	Reply	Comment
	TT1		Initialises 1255
			Wait 2 secs
	VA1		Sets 1 volt amplitude
	FR125E3		Sets 125kHz
	RA1,2		Characterise on 300mV
	RA2,2		range
	IS10		Integration time
	MS5		Delay for cal. box
	SO1,2		Channel 1 / Channel 2
	OP2,1		Output all to GPIB
	CV1		Coordinates, R,theta

B.4.2 To allow the cal. box and the W&G to settle, this dummy measurement is taken.

SI		Measure
		read result

Five numbers are outputted by the 1255, frequency, magnitude, phase, an error code and a limit check result: these can be discarded

B.4.3 Program the cal. box to attenuate the signal by 14dB. This measurement returns the ideal value for calibration of the 3 V range at about 300mV.

SO1,0	Channel 1
SI	Measure
	read result

Five numbers are outputted by the 1255, frequency, magnitude, phase, an error code and a limit check result: save the magnitude.

SO2,0	Channel 2
DO	command result output
	read result

Five numbers are outputted by the 1255, frequency, magnitude, phase, an error code and a limit check result: take the average of Channel1 and Channel2 magnitudes and use this as the characterisation value "a".

B.4.4 Program the cal. box to attenuate the signal by 20dB. This measurement returns the ideal value for calibration of the 300mV range at about 150mV.

SO1,0	Channel 1
SI	Measure
	read result

Five numbers are outputted by the 1255, frequency, magnitude, phase, an error code and a limit check result: save the magnitude.

SO2,0	Channel 2
DO	command result output
	read result

Five numbers are outputted by the 1255, frequency, magnitude, phase, an error code and a limit check result: take the average of Channel1 and Channel2 magnitudes and use this as the characterisation value "b".

B.4.5 Program the cal. box to attenuate the signal by 34dB. This measurement returns the ideal value for calibration of the 30mV range at about 30mV.

SO1,0	Channel 1
SI	Measure
	read result

Five numbers are outputted by the 1255, frequency, magnitude, phase, an error code and a limit check result: save the magnitude.

SO2,0	Channel 2
DO	command result output
	read result

Five numbers are outputted by the 1255, frequency, magnitude, phase, an error code and a limit check result: take the average of Channel 1 and Channel 2 magnitudes and use this as the characterisation value "c".

Appendix C

SWITCHES ON PCB22

NOTE: All switches must be in the up position for normal operation of the 1260. When they are in the down position various diagnostic aids are enabled.

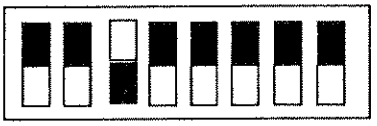
C.1 CALIBRATION CONSTANTS

UP - Analyser calibration constants are enabled
DOWN - Analyser calibration constants are disabled

C.2 SQUARE WAVE OUTPUT

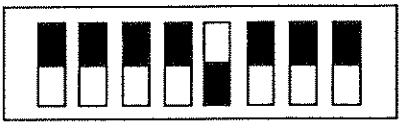
UP - Disable square wave output (<65kHz)
DOWN - Enable square wave output (<65kHz)

C.3 FORCE WAVE BEAT CHECK



UP - Enable "beat" check software
DOWN - Disable "beat" check software

C.4 HETERODYNE SCHEME



UP - Select new heterodyne scheme
DOWN - Select old heterodyne scheme

C.5 GENERATOR CALIBRATION

UP - Enable generator calibration constants
DOWN - Disable generator calibration constants

All other switches are not used.

Appendix D

CALIBRATOR CHARACTERISATION

This requires a calibrated and partially overchecked 1255 (ie. past sections 7.3.4 to 7.3.12). Connect the 1255 to the calibration box and the calibrator as in figure 10.

Set up the following:

SELF-TEST	Initialise		[TT1]
GENERATOR	Amplitude	2Volts	[VA2]
ANALYSER			
NEXT	V1 Outer	floating	[OU1,1]
NEXT	V2 Outer	floating	[OU2,1]
DISPLAY	Coords	r,theta	[CV1]
RECYCLE			[RE]

For each of the frequencies and amplitudes in tables 3.5.5, 3.5.6, 5.5.8, 5.5.9, and 7.3.2 note the transfer function of the calibration box. Then for each of the nominal values in the above tables, the calibrator should be set to the nominal value multiplied by the transfer function for that frequency and amplitude.

ie. For the unit under test to read 2V @ 300Hz the calibrator should be set to:

2V (nominal value) x K (the transfer function for 2V,300Hz)

Appendix E

ANALYSER CALIBRATION POINTS

(Hz)

200	655.35999	655.36	2000
5000	7000	10000	12000
17000	22000	32767.999	32768
48000	55000	65535.999	65536
100E3	125E3	145E3	200E3
300E3	430E3	570E3	600E3
655.35999E3	655.36E3	800E3	1E6
2E6	4E6	6E6	6.5535999E6
6.5536E6	7E6	9E6	10E6
11E6	14E6	16E6	19E6
20E6			

Appendix F

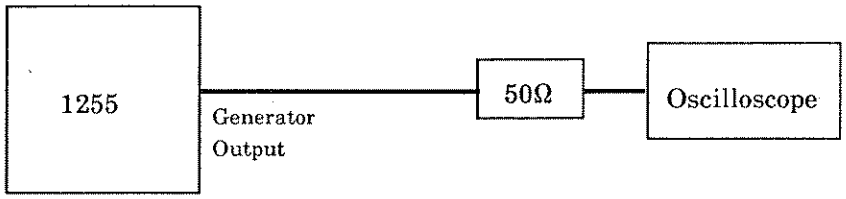
GENERATOR CALIBRATION POINTS

This is the list of generator calibration points.

300Hz
65.535999kHz
65536kHz
800kHz
2MHz
4MHz
7MHz
20MHz

1255 Calibration and Overcheck Diagrams

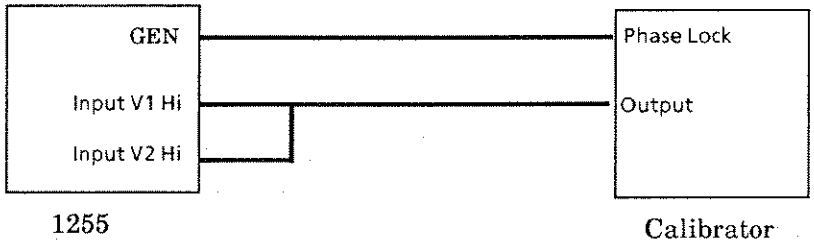
Figure 1. *Generator Flatness Test*



Note: If the oscilloscope has a 50Ω input, this may be used instead of the 50Ω terminator.

Figure 2. *LF analyser set-up / test*

a) Without calibration box



b) With calibration box

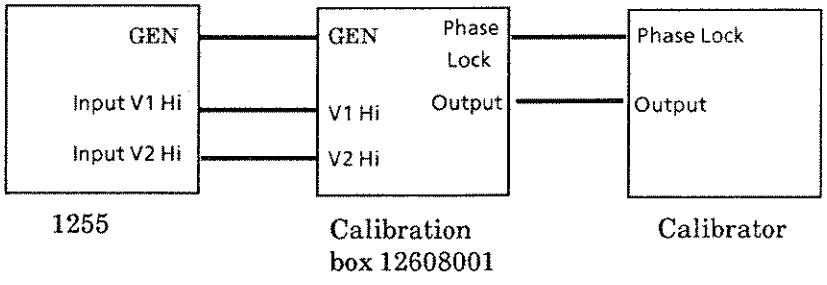
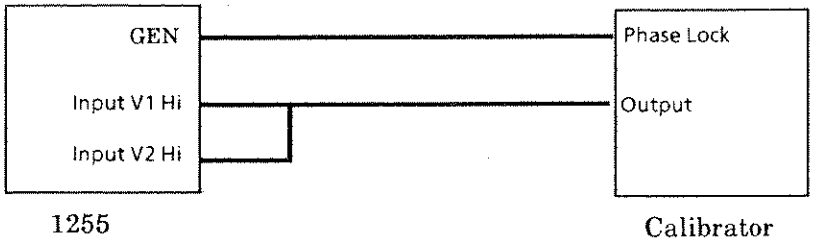


Figure 3. *Analyser LF Common Mode*

a) Without calibration box



b) With calibration box

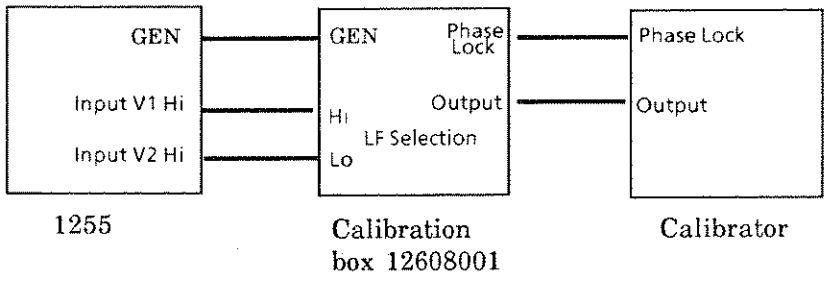


Figure 4. *Cable Connections*

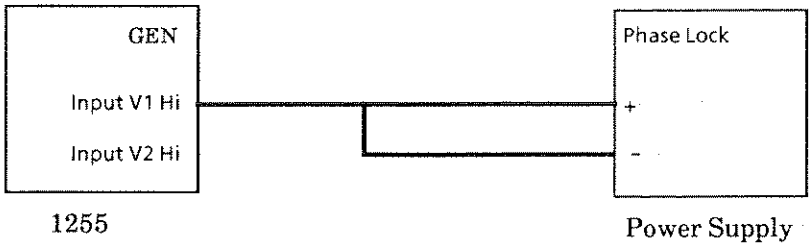
PCB10 (Channel1) SK401 to Input V1 HI
PCB10 (Channel1) SK402 to Input V1 LO

PCB16 PLD to PCB10 (CH1) PL401 (heterodyne cables)
PCB16 PLE to PCB10 (CH2) PL401
PCB16 PLG to PCB14 SK701 (hf signal)
PCB16 PLH to PCB15 SK202 (lf reference)

PCB15 SK201 to PCB14 SK201 (lf output)
NOTE The connections on issue B & C copper are transposed

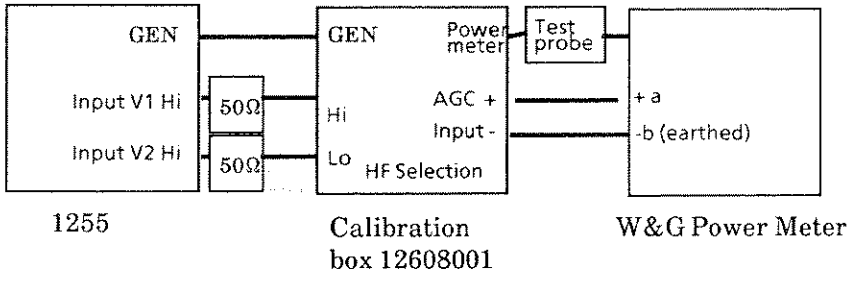
PCB15 SK1 to KILL GEN I/P
PCB22 CON1 to KEY SWITCH

Figure 5. *DC Overload Test*



Note: Hi to shield
The high BNC inner is the input, and the high BNC outer is the shield.

Figure 6. *HF Analyser accuracy set-up test*



The terminators on the1260 inputs are matched to the calibration box and must always be connected according to the identification labels.

The W&G power meter must be turned on with the test probe connected to its own ouput for at least one hour before it is used for calibration. With the W&G connected in this way, the displayed reading should be set to 0dBm on the ±0.2dBm range, by adjusting the set calibration pot with the impedance set to 50Ω 0dBm.
IMPORTANT: the W&G must be left in this state when it is not in use.

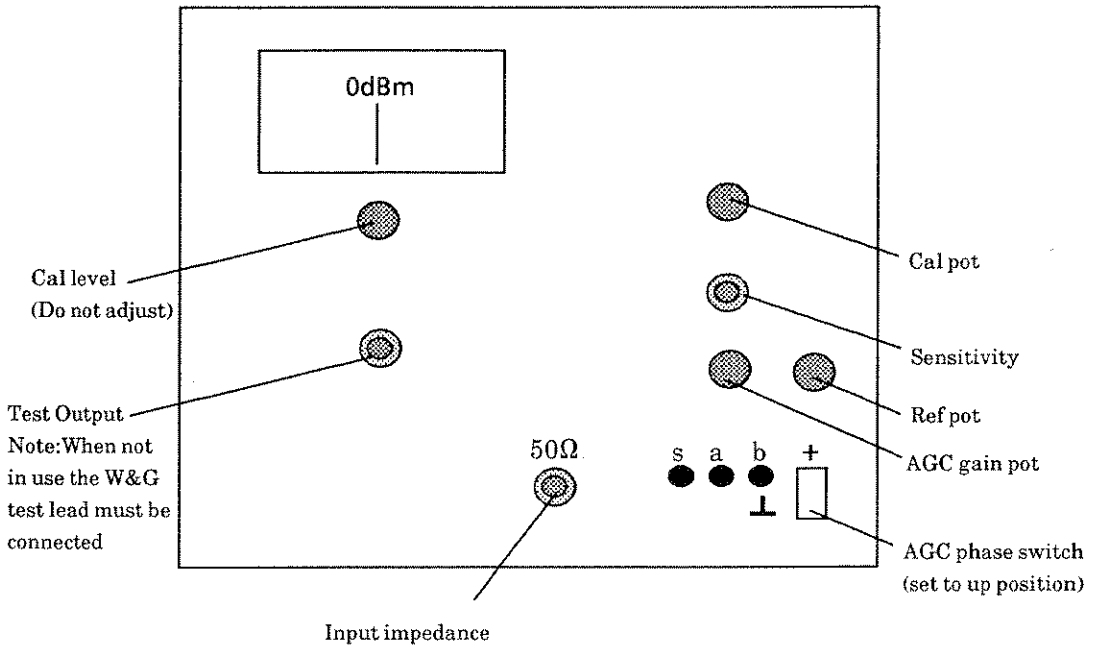
Set the gain of the W&G fully anti-clockwise then move a quarter of a turn back clockwise (ie just off the minimum gain).

To use the W&G, connect the test probe to the calibration box as above and set the 1260 amplitude to 0.7V at 100kHz, and use the reference knob on the W&G to set the W&G to read 0dBm on the ±0.2dBm range (this will usually take place with the knob at the clockwise end of its travel) .The needle will tend to overshoot and may take 20-30 seconds to settle. If it does not move off the end stop increase the gain of the W&G by another quarter of a turn and try the reference pot again.

NOTE: If the gain is set too high the AGC loop will oscillate causing amplitude modulation on the calibration box output.

NOTE: No attempt should be made to calibrate or overcheck unless the W&G is pointing at 0dBm ±0.1dBm and the pointer is not oscillating.

W&G Power Meter Front Panel Layout



NOTE the cal pot should only be set up with the test head connected to the W&G output.

Figure 7. *Analyser Input Protection Test*

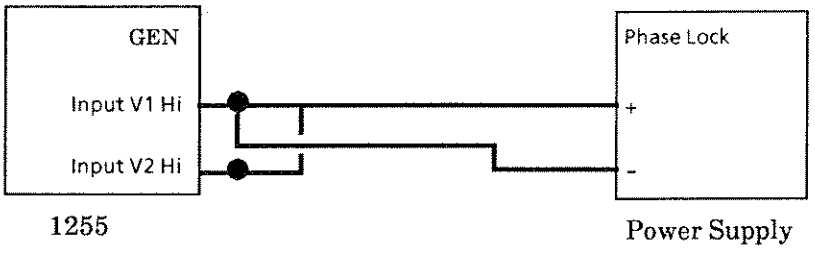


Figure 8. *Generator Common Mode Overload Test*

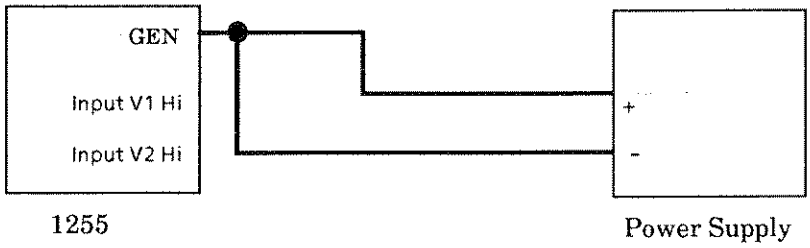
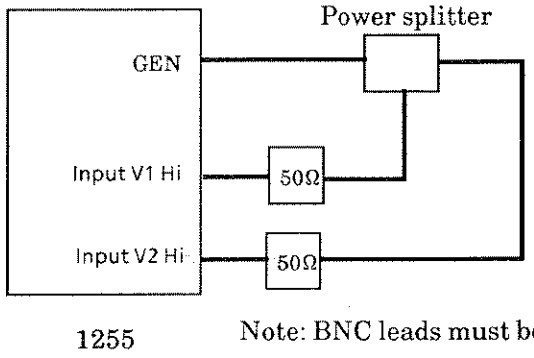


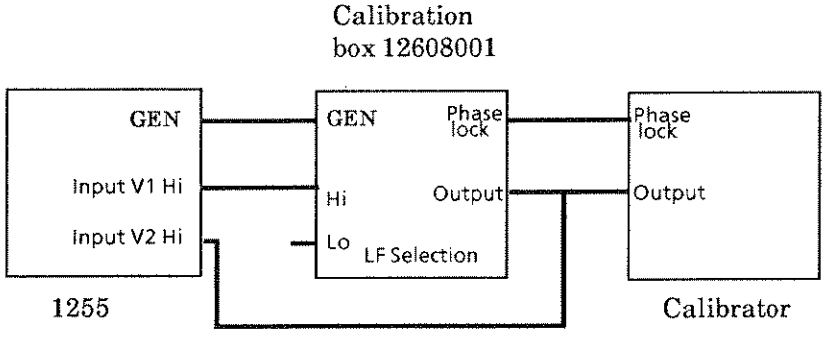
Figure 9. *Analyser range to range using a power splitter*



Note: BNC leads must be the same lenght

50Ω terminators matched to the power splitter better than 0.1%

Figure 10. *Calibrator characterisation*



Chapter 6 Part B
Calibration of 1260

Appendix

Figures

1 TEST EQUIPMENT

Power Supply Test

- Flash/continuity Tester
- DVM
- Power Supply Load Card 12506003
- Mains-fail test box 12506002
- Variac

Final Calibration

- Flash/continuity tester
- DMM Schlumberger 7060E
- Oscilloscope
- Extender Card 12500508
- Counter timer
- Calibrator Fluke 5200
- Test Set 12606001
- Power Meter W & G EPM-1 with TK-10 Test Head
- Power Supply Floating 0 to 60V
- Current cal box 500Ω

Functional Overcheck

- DMM Schlumberger 7060E
- Counter timer
- Calibrator Fluke 5200
- Test Set 12606001
- Power Meter W & G EPM-1 with TK-10 Test Head
- Silent 700 terminal or equivalent
- Power splitter and 2 x 50Ω matched terminators
- 12607A Test Kit

2 POWER SUPPLY TEST

2.1 Take out all the PCBs except PCB 5 and disconnect the display.

2.2 Flash test on power live and neutral to ground @ 1500V dc.

2.3 Check that the resistance from any of the following points to the earth pin on the mains connector is less than 0.5Ω:

Fan guard
Exposed screws on the rear panel
BNC outers on the rear panel

2.4 Check that the fuse inserted is rated @ 1A (anti-surge).

2.5 Measure the resistance across the link for 115V [this is on the Power Supply Board next to the mains input] checking that with switch set to 115V the resistance is less than 1Ω and with the switch set to 230V the resistance is greater than 20kΩ.

2.6 Set mains select switch to 230V.

2.7 Insert the PSU load card into the SKA9-SKB9 position on the Mother Board and set the switches on the load card to off. Connect the 1260 mains lead to the variac O/P set to 230V.

2.8 Switch on the mains and the 1260. Monitor the 5V rail on the load card and adjust the potentiometer nearest the 5V output on the Power Supply to give 5.00V ±0.01V.

2.9 The new version of the power supply load card does not have a switch "C". When using this card ignore all references to switch "C" in the following tests.

Check the following voltages (measured on the Power Supply Load Card) with switches A, B, C and D all off:

Voltage	Limits
+ 5V	4.9V to 5.1V
+18V	17.5V to 20V
−18V	−17.5V to −20V
+24V	23.5V to 25.5V

2.10 Repeat test 9 with switch A on.

2.11 Repeat test 9 with switches A, B and C on.

2.12 Set the power to 252V and repeat tests 9, 10 and 11.

2.13 Set the power to 198V and repeat tests 9, 10 and 11.

2.14 With switches A, B and C still on, measure the 5V rail and momentarily operate switch D; the 5V rails should be 4.8V. Set switch D off, but leave A, B and C on.

2.15 Momentarily short the 5V to 0V and check that the power supply recovers.

2.16 Connect the 1260 as shown in Figure 1 with the Test Box switches set to "Trigger Normal" and "Supply Switching". Using the oscilloscope, adjust the Test Box Delay so that the 1260 is switched off at the peak of the mains cycles.

2.17 Check that POWER FAIL [bar] on PCB 5 is given approximately 10msec after the mains has failed.

2.18 Check that the 5V rail holds up to a minimum of 4.75V for at least 6msec after POWER FAIL [bar] is asserted.

2.19 Set the Test Box Switch to "Trigger Invert" and check that there is at least 200msec delay from the point at which the power comes on to the POWER FAIL [bar] going back high.

2.20 Switch Off. Replace the fuse by a 2A fuse and set the variac output and the 1260 mains selector to 115V. Switch on and repeat tests 9, 10 and 11.

Set the Variac to 126V and repeat paragraphs 9, 10 and 11.

Set the Variac to 90V and repeat paragraphs 9, 10 and 11.

Repeat test 14.

Repeat test 15.

Repeat test 16.

2.21 Switch Off. Replace the 1A fuse and set the 1260 back to 230V operation

2.22 Replace the rest of the PCBs.

The Power Supply is now fully set up.

3 SET UP PRIOR TO SOAK

This section is not required for this manual

4 SOAK PROCEDURE

This section is not required for this manual

5 FINAL CALIBRATION

Calibration should be carried out at a constant temperature in the range 17-23°C.

5.1 SAFETY CHECKS

These checks should be carried out if they have not already been done, as in Section 2. This would occur for example in an old unit if it was being re-calibrated after a period of time or after repair work had been undertaken.

5.1.1 Take out all the PCBs except PCB 5 and disconnect the display.

5.1.2 Flash test on mains live and neutral to earth @ 1500V dc.

5.1.3 Check that the resistance from any of the following points to the earth pin on the mains connector is less than 0.5Ω:

Fan guard
Exposed screws on the rear panel
BNC outers on the rear panel

5.1.4 Check that the fuse inserted is rated @ 1A (anti-surge) for 230V or 2A for 115V operation.

5.1.5 Measure the resistance across the link for 115V [this is on the Power Supply Board next to the mains input] checking that with the switch set to 115V the resistance is less than 1Ω and with the switch set to 230V the resistance is greater than 20kΩ.

5.2 PRELIMINARY TEST

Before testing check that the connections are as in Figure 1.

5.2.1 Switch on and set the Generator output to give a 3V, 400Hz signal. Connect this to both Channels 1 and 2 and take several measurements displaying the Channel 1 readings. Ensure that the readings on the 1260 are not scattering and that they are 3V ±0.3V.

5.2.2 Repeat 1 displaying Channel 2.

5.2.3 Set the frequency to 100kHz and take several readings to ensure that the result =3V ±0.3V and does not scatter by more than 20 bits.

5.2.4 Repeat 3 displaying Channel 1.

5.2.5 Leave the unit switched on for half an hour before starting calibration.

5.3 LF GENERATOR CALIBRATION (PCB 15)

5.3.1 Switch off, disconnect the cables and put PCB 15 on an extender card.

Switch on and set up the following:

SELF-TEST Initialise [TT1]

With a DMM on DCV measure the voltage from TP4 to TP1 Adjust RV203 for 0V ±2mV.

Measure the voltage from TP5 to TP1. Check for 0V ±10mV.

5.3.2 This completes PCB 15 calibration. Switch off and refit PCB 15 into its slot and reconnect the cables.

5.4 HF SYNTHESISER CALIBRATION (PCB 16)

5.4.1 Switch off and put PCB 16 on an extender card.

NOTE: The cable from PCB 15 to PLH must be connected.

Switch on and set up the following:

SELF-TEST	Initialise	[TT1]

5.4.2 Set up the following:

GENERATOR	Frequency	66kHz	[FR66E3]

With the oscilloscope check that the waveform on TR201 collector (can) is a +5V square wave and with a counter/timer check that the period is 2.54msecs ±0.1msecs.

5.4.3 For status B issue A boards or later issues:

Monitor TP201 with the DVM and set CV401 to obtain a reading of –3V to ±0.5V.

For older boards (status A):

With the DVM check that the DC voltage on TP201 lies between –6V and +6V.

5.4.4 Set up the following:

GENERATOR	Frequency	20MHz	[FR20E6]

Disconnect the cable from PCB 16 PLH and connect a 32kHz ± 100Hz 5V ±0.1V rms sine wave to PCB 16 PLH. With a DMM on DCV monitor TP102 wrt ground. Adjust LV101 (under the middle screen) to give a voltage of +10V ±0.4V.

5.4.5 Set up the following:

GENERATOR	Frequency	66kHz	[FR66E3]

Reconnect the cable from PCB 15 to PCB 16 PLH. With a DMM on DCV monitor TP102 wrt ground. Check the reading is between –6.5V and –9.5V.

5.4.6 This completes PCB 16 checks. Switch off and refit PCB 16 into its slot and reconnect all cables.

5.5 ANALYSER (VOLTAGE) CALIBRATION (PCB 10)

NOTE: These tests are best carried out with the front panel raised by one hole so that the cables reach.

5.5.1 Switch off and fit PCB 10 Channel 1 onto an extender card with the screen removed.

Set up the following:

SELF-TEST	Initialise		[TT1]
ANALYSER			
NEXT	Input	Diff	[IP1,1]
SINGLE			[SI]

With a DVM set to Ω measure:

Measure	**Reading**	**Comment**
HI to shield	1MΩ ±10kΩ	Input impedance*
LO to shield	1MΩ ±10kΩ	Input impedance*
LO shield to TP601	47Ω ±5Ω#	Shield
HI shield to TP601	47Ω ±5Ω#	Grounded

*Set the 7060 to the 10MΩ range for these readings.
#For issue A PCB's only the resistance is 0Ω ±10Ω.

Set up the following:

ANALYSER			
NEXT	Input	Single	[IP1,0]

With a DVM set to Ω check that LO to shield is open circuit.

Set up the following:

ANALYSER			
NEXT	Input	Diff	[IP1,1]
	Outer	Floating	[OU1,1]
	Coupling	AC	[DC1,1]

With a DVM set to Ω measure from:

HI to shield	o/c	AC coupled
LO to shield	o/c	AC coupled
LO shield to TP601	100kΩ ±1kΩ	LO floating

5.5.2 Short circuit the HI and LO inputs. Ensure that all cables are connected.

Set up the following:

SELF-TEST	Initialise		[TT1]
ANALYSER	Range	30mV	[RA1,1]
	Input	Diff	[IP1,1]
SINGLE			[SI]

5.5.3 Ignore the first reading and error. With a DC DVM measure the following test points wrt TP601:

Measure	Adjust	Limits
TP403	RV401	0V ±200µV
TP404	RV402	0V ±200µV
TP603	RV403	0V ±15mV

5.5.4 Remove the short circuits and check the following test points wrt TP601:

Measure	Limits
TP403	0V ±3mV
TP404	0V ±3mV

Re-fit the short circuit.

5.5.5 Set up the following:

GENERATOR	Frequency	20MHz	[FR20E6]
SINGLE			[SI]

With a DC DVM measure the following test points wrt TP601:

Measure	Limits
TP602	0V ±1V
TP603	0V ±100mV

5.5.6 Set up the following:

SELF-TEST	Initialise		[TT1]
ANALYSER			
NEXT	Range	300mV	[RA1,2]
	Input (V1)	Single	[IP1,0]
DISPLAY	Source	V1	[SO1,0]
RECYCLE			[RE]

Connect a floating power supply, set to 0V, to the Channel 1 inputs as in Figure 5. Gradually increase the power supply output until an overload is continuously indicated in the display. Check the input to the 1260 is within the listed limits when this occurs.

Positive	between HI and shield	+0.52V to +0.58V
Negative	between HI and shield	−0.52V to −0.58V

5.5.7 Set up the following:

GENERATOR	Frequency	65kHz	[FR65E3]

Positive	between HI and shield	+5.6V to +6.8V
Negative	between HI and shield	−5.6V to −6.8V
Positive	between LO and shield	+5.6V to +6.8V
Negative	between LO and shield	−5.6V to −6.8V

5.5.8 Using the power supply set to the following voltages and applied to both HI and LO inputs as a common mode voltage to the shield as in Figure 7, check the voltages at the test points listed below with a DC DVM wrt TP601:

Set up the following:

SINGLE [SI]

Input	**Measure**	**Limits**
+50V ±1V	D404 cathode	+6.25V to +7.4V
	D408 cathode	+6.25V to +7.4V
−50V ±1V	D404 cathode	−6.25V to −7.4V
	D408 cathode	−6.25V to −7.4V

5.5.9 Switch off and set CV401, CV402 and CV403 to their mid position (CV403 is present only on issue D or later PCB's).

Fit the screen to Analyser 1 and calibrate as follows, with the PCB still on an extender card, so as to be able to access the required adjustments.

Set the waveform switch (position 2 of SW1) down to enable the square wave output. Ensure the "apply cal" switch (position 1 of SW1) is in the down position.

Set up the following:

SELF-TEST	Initialise		[TT1]
GENERATOR	Amplitude	2V	[VA2]
ANALYSER	Integration time	0.3secs	[IS.3]
NEXT	Input (V1)	Diff	[IP1,1]
	Range (V1)	3V	[RA1,3]
	Outer (V1)	Floating	[OU1,1]
DISPLAY	Source	V1	[SO1,0]
	Coords	r, θ	[CV1]
RECYCLE			[RE]

Connect the 1260 generator to the calibrator phase lock. Connect the calibrator HI output to the Channel 1 HI and the calibrator LO to the Channel 1 HI shield. Short circuit Channel 1 LO to the LO shield. The calibrator LO must not be connected to earth (as in Figure 2).

The limits of the following table refer to the R value displayed on 1260 front panel.

Freq	Range	Input	Amplitude	Adjust/Check	Limits
299Hz	3V	HI	2V	RV701 & SP702/3/4	2.0005V 1.9995V
65kHz	3V	HI	2V	CV401	2.0005V 1.9995V

For Issues A,B and C :- Remove the short circuit from channel 1 LO and connect the calibrator to channel 1 LO as in figure 3. Set the frequency to 100 kHz on the 300mV range and set CV402 for less than 5mV. Set the frequency to 1MHz and check for less then 5mV. If it is >5mV adjust CV402 to split the error and recheck at 100kHz.

30Hz	300mV	Hi & Lo	2V	check	<3mV

For Issues D :- Remove the short circuit on Channel 1 LO and connect the calibrator to Channel 1 LO as in Figure 3:

100kHz	300mV	HI&LO	2V	CV402 set to <2mV
1MHz	300mV	HI&LO	2V	CV403 set to <5mV

Repeat adjustment of CV402 and CV403 if necessary:

30Hz	300mV	HI&LO	2V	Check	<3mV

5.5.10 Check the Channel 1 calibration as in the following table with the connections as in Figure 2.

Low frequency checks using phase-locked calibrator

Freq	Range	Input	Cal Amp	Adjust /Check	Limits	Comments
299Hz	3V	HI	2V	RV701	2.0010V 1.9990V	[RA1,3] [FR299]
299Hz	3V	HI	3V	Check	3.0015V 2.9985V	
299Hz	3V	HI	0.3V	Check	300.3mV 299.7mV	
299Hz	300mV	HI	300mV	Check	300.30mV 299.70mV	[RA1,2]
299Hz	300mV	HI	30mV	Check	30.03mV 29.97mV	
299Hz	30mV	HI	30mV	Check	30.030mV 29.970mV	[RA1,1]
299Hz	30mV	HI	34mV	Check	No overload	
655Hz	3V	HI	2V	Check	2.0010V 1.9970V	[RA1,3] [FR655]
656Hz	3V	HI	2V	Check	2.0010V 1.9990V	[FR656]
656Hz	30mV	HI	34mV	Check	No overload	
3kHz	3V	HI	2V	Check	2.0010V 1.9990V	[FR3E3]
10kHz	3V	HI	2V	Check	2.0020V 1.9980V	[FR1E4]
32kHz	3V	HI	2V	Check	2.0040V 1.9960V	[FR32E3]
65kHz	3V	HI	2V	Check	2.0040V 1.9960V	[FR65E3]
100kHz	3V	HI	2V	Check	2.0200V 1.9800V	[FR1E5]

5.5.11 Set up the following:

SELF-TEST	Initialise		[TT1]
DISPLAY	Source	V1	[SO1,0]
RECYCLE			[RE]

Connect the calibrator HI to Channel 1 HI and the calibrator LO to Channel 1 HI shield as in Figure 2. Set the calibrator to 1MHz and with the phase lock off, switch the calibrator output on and gradually increase the output voltage until the unit indicates an overload.

Check that the calibrator is delivering 4.3 $\pm$0.5V rms at this point.

Disconnect the calibrator. Replace Analyser 1 in its correct position in the unit card rack.

Switch off, refit PCB 10 into its slot and reconnect all cables.

REPEAT FROM 5.5 FOR CHANNEL 2 REPLACING ALL SET UP INSTRUCTIONS FOR THE CHANNEL 2 EQUIVALENT.

5.5.12 Replace Channel 2 back into its slot with all cables connected.

5.5.13 Remove Channel 1. Remove Channel 3 and configure this analyser to be Channel 1 by connecting the split pads as below:

De-solder split pads	SP103 and SP114
Solder split pads	SP101 and SP112

Note : On some versions of PCB 10, D401, D402, D405 and D406 may not be fitted, in which case tests 5.5.7 and 5.5.8 will fail.

Place this analyser into the Channel 1 position in the frame. Repeat from 5.5 for this channel as though it is Channel 1.

5.5.14 Remove this analyser and configure it to be Channel 3 by setting the split pads back to normal:

Desolder split pads	SP101 and SP112
Solder split pads	SP103 and SP114

Refit the front panel.

5.5.15 Set the waveform switch (position 2 of SW1) up to disable the square wave output. Ensure the "apply cal" switch (position 1 of SW1) is in the down position.

Set up the following:

SELF-TEST	Initialise		[TT1]
GENERATOR	Amplitude	0.75V	[VA.75]
	Frequency	65kHz	[FR65000]
ANALYSER	Integration time	1sec	[IS1]
DISPLAY	Source	V1	[SO1,0]
	Coord	r,θ	[CV1]
RECYCLE			[RE]

Using the power meter via the 12606001 test set check Channel 1 high frequency performance either manually or under GPIB control as in the following table (with the connections made as in Figure 6).

Make a note of this reading.

High frequency checks using power meter

Freq	Range	Input	Atten -14dB	Check	Limits	Comments
100kHz	auto	HI		Check	As noted ±3mV	Terminate with 50Ω
200kHz	auto	HI		Check	As noted ±3mV	Terminate with 50Ω
650kHz	auto	HI		Check	As noted ±3mV	Terminate with 50Ω
660kHz	auto	HI		Check	As noted ±4mV	Terminate with 50Ω
1MHz	auto	HI		Check	As noted ±5mV	Terminate with 50Ω
2MHz	auto	HI		Check	As noted ±10mV	Terminate with 50Ω
6.5MHz	auto	HI		Check	As noted ±15mV	Terminate with 50Ω
6.6MHz	auto	HI		Check	As noted ±15mV	Terminate with 50Ω
10MHz	auto	HI		Check	As noted ±30mV	Terminate with 50Ω
20MHz	auto	HI		Check	As noted ±50mV	Terminate with 50Ω
32MHz	auto	HI		Check	As noted ±50mV*	Terminate with 50Ω

*Limits are –0 to +100mV for boards fitted with pad5s in position D401,402,405,406.

THIS COMPLETES CHANNEL 1 FINAL CALIBRATION.

5.5.16 REPEAT FROM 5.5.16 FOR CHANNEL 2 REPLACING ALL SET UP INSTRUCTIONS FOR THE CHANNEL 2 EQUIVALENT.

THIS COMPLETES CHANNEL 2 FINAL CALIBRATION.

5.5.17 Remove Channel 1. Remove Channel 3 and configure this analyser to be Channel 1 by connecting the split pads as below:

De-solder split pads	SP103 and SP114
Solder split pads	SP101 and SP112

Place this analyser into the Channel 1 position in the frame. Repeat from 5.5.16 for this channel as though it is Channel 1.

5.5.18 Remove this analyser and configure it to be Channel 3 by setting the split pads back to normal:

De-solder split pads	SP101 and SP112
Solder split pads	SP103 and SP114

For issue A copper:

De-solder and remove D401, D402, D405 and D406. (If fitted.)

For issue B copper:

De-solder the split pads at the junction of:

D401 and D402	(SP401)
D405 and D406	(SP402)

5.5.19 THIS COMPLETES CHANNEL 3 FINAL CALIBRATION.

Replace Channel 1 and Channel 3 back into their normal slots and reconnect all cables.

Set SW1 position 2 on PCB 22 up.

5.6 CURRENT TO VOLTAGE CONVERTER CALIBRATION (PCB 31)

NOTE: These tests should be done with the front panel raised by one hole and with the top screen of BD31 removed.

Ensure that the power cable and the relay drive cables are connected.

5.6.1 Set up the following:

SELF-TEST	Initialise	[TT1]

5.6.2 Use a voltmeter set to DC to measure the voltages on the regulator outputs wrt TP106. The following voltages should be found:

IC105 pin3 +15V ±0.5V
IC106 pin3 −15V ±0.5V

5.6.3 Using a voltmeter set to DC measure across resistor R125 (situated below IC104). Adjust RV101 until the following voltage is measured:

1.2V ±100mV (only the magnitude is important)

5.6.4 Using the voltmeter measure across resistor R103. The following voltage should be found:

1.2V ±100mV (only the magnitude is important)

5.6.5 Monitor the voltage at TP101 wrt TP106 using an oscilloscope set to maximum sensitivity. No high frequency oscillations should be apparent.

5.6.6 Set up the following:

ANALYSER			
PREV	Range	60mA	[RA3,5]

The observed waveform should be 0V as before.

5.6.7 Fit the 500Ω resistor calibration box on to the front panel terminals.

Set up the following:

GENERATOR	Frequency	300Hz	[FR300]
	V.Ampl	1V	[VA1]
ANALYSER			
PREV	Range	6mA	[RA3,4]
DISPLAY	Result	Z1	[SO1,3]
	Coord	Z,θ	[CZ1]
RECYCLE			

Check that the impedance displayed is between 480Ω and 520Ω.

5.6.8 Set up the following:

GENERATOR	V.Ampl	0.1V	[VA0.1]
ANALYSER			
PREV	Range	600µA	[RA3,3]

Check that the impedance displayed is between 480Ω and 520Ω.

5.6.9 This completes the PCB 31 tests. Refit the front panel. Ensure all cables are connected.

5.7 GENERATOR OUTPUT CALIBRATION (PCB 14)

5.7.1 Switch off and put PCB 14 on an extender card. Remove the screen box. Disconnect the cables to SK201 and SK701. Switch on and set up the following:

SELF-TEST	Initialise	[TT1]

Make the following adjustments using a DMM on DCV to monitor the voltages indicated:

Measure	Adjust	Limits	Comment
Across R531	RV501	110mV ±10mV	Quiescent I
Gen O/P	RV301*	0V ±5mV	Output offset
Across R416	RV302*	0V ±5mV	Output CM

*Note on issue B copper RV301 & 302 are transposed.

5.7.2 Switch off and refit the screen box. Switch on and monitor the output between the generator LO and earth with an oscilloscope. Adjust RV601 for the minimum square wave between LO and earth across R416.

5.7.3 Fit the cables to SK201 and SK701. Monitor the generator output with a DC DVM and set RV301* for 0V ±5mV.

5.7.4 Set up the following:

GENERATOR	Bias	40V	[VB40]

Measure the generator output with DC DVM. Adjust RV202 BD15 for 40V ±60mV.

5.7.5 Set up the following:

GENERATOR	Bias	–40V	[VB-40]

Check the generator output with a DC DVM for -40V ±200mV. Note the reading.

5.7.6 Set up the following:

GENERATOR	Bias	40V	[VB40]

Check the generator output with DC DVM. Split the error between ±40V with RV202 BD15 for ±40V ±100mV.

5.7.7 Set up the following:

GENERATOR	Bias	0V	[VB0]
	Amplitude	3V	[VA3]
SINGLE			[SI]

Measure the generator output with an AC DVM. Check for 3V ±0.1V. Note this reading.

5.7.8 Set up the following:

GENERATOR	Frequency	65kHz	[FR65E3]

Measure the generator output with an AC DVM. Check for the noted reading ±0.1V.

5.7.9 Set up the following:

GENERATOR	Frequency	66kHz	[FR66E3]

Measure the generator output with an AC DVM. Check for the noted reading ±0.1V. Check the generator output on the oscilloscope for an undistorted sine wave.

5.7.10 Set up the following:

GENERATOR	Amplitude	305mV	[VA.305]
	Frequency	65kHz	[FR65E3]

Measure the generator output with an AC DVM. Note this reading.

5.7.11 Set up the following:

GENERATOR	Frequency	66kHz	[FR66E3]

Adjust RV701 for the noted reading as above ±30mV.

5.7.12 Set up the following:

GENERATOR	Amplitude	.7V	[VA.7]
SWEEP	Δ log	100pts	[SF100]
NEXT	Frequency	MIN 1MHz	[FM1E6]
		MAX 20MHz	[FX20E6]
NEXT	Enable	log f	[SW2]
RECYCLE			[RE]

Monitor the generator output on an oscilloscope TERMINATED IN 50Ω over the sweep. Note any high or low points, repeat the sweep adjusting CV301 for the flattest response.

5.7.13 Set up the following:

SELF-TEST	Initialise		[TT1]
RECYCLE			[RE]
GENERATOR	Bias	5V	[VB5]

Short circuit generator output and check for no error.

Set up the following:

GENERATOR	Bias	-5V	[VB-5]

Check for no error.

Set up the following:

GENERATOR	Bias	10V	[VB10]

Check for generator overload error.

Set up the following:

GENERATOR	Bias	–10V	[VB-10]

Check for generator overload error.

Remove the short circuit.

5.7.14 Connect a power supply positive lead via a 100Ω resistor to the generator LO and the negative to earth (ie. Channel 1 HI outer) as in Figure 8.

Apply +1V from the power supply and check for no error.

Apply –1V from the power supply and check for no error.

Apply +5V from the power supply and check for common mode error.

Apply –5V from the power supply and check for common mode error.

5.7.15 Set up the following:

GENERATOR	Type	Current	[GT1]
NEXT	I.Bias	100mA	[IB0.1]

Use a DMM set to 200mA current range to measure the generator output. This should be 100mA ±0.5mA.

5.7.16 Set up the following:

GENERATOR			
NEXT	I.Bias	–100mA	[IB-0.1]

Use a DMM set to 200mA current range to measure the generator output. This should be –100mA ±0.5mA.

5.7.17 This completes the final calibration tests. Switch off and refit PCB 14 into its slot.

6 AUTO-CALIBRATION PROCEDURE

The auto-calibration of the 1260 analysers can be a single process in which the whole instrument is calibrated from scratch, or a number of 'patch' calibrations to repair a single point (refer to Appendix A). The calibration requires:

1. Schlumberger calibration box (12606001)
2. W & G power meter
3. 2 x BNC coax leads of the same length, and as short as possible
4. 2 x 50Ω feedthrough terminators matched to within 0.1%
5. LF (up to 1MHz) AC calibrator eg. FLUKE 5200
6. Assorted BNC leads, always kept as short as possible
7. The 12607A Schlumberger test kit

NOTE:

1) The calibration switch box needs to be characterised at 6 monthly intervals.

2) When the W & G power meter is not being used the test head should be connected to the W & G output.

3) Items 1-6 should be connected together when the calibration box is characterised, and not separated from their calibration unit. The terminators should be marked with a channel number, and should always be connected to the 1260 in accordance to their marking.

4) It is advisable, when using the 50kΩ resistor box in the 12607A test kit above 1MHz, to stay at a distance of 1m or more from the unit. This requirement is a result of the sensitivity of the phase shift in such a large resistor to changes in the parasitic capacitance.

6.1 FULL CALIBRATION SEQUENCE

If the calibration box has not been characterised within the last six months the procedure in Appendix B should be followed. This sets up a set of characterised values (one for each frequency and attenuation setting), which are stored as part of the auto-calibration program on micro-vax. These values compensate for any non-linearities in the frequency response of the calibration box. These characterised values are sent to the 1260 via the commands "CA 0,f" in the following calibration procedure.

For voltage channel calibration, if the auto-calibration program is available the 1260 should be connected to the AC calibrator, calibration box (12606001) and the GPIB controller via GPIB cables as in Figure 2. The GPIB addresses should be set up and the front panel "Break" key should be pressed on the 1260. The 1260 auto-calibration program should then be run.

The DIL switches on PCB 22 are explained in Appendix C.

6.2 INITIALISATION

The unit is put in calibration mode by setting switch SW2 on PCB 22 to 'CALIBRATE'. Ensure all eight DIL switches (SW1) on PCB 22 are in the up position.

Calibrator Frequency	1260 Command	Reply	Comment
-	TT1	-	Initialises 1260
-	CM5	-	Clears cal data

6.3 LF VOLTAGE ANALYSER CALIBRATION

Connect the BNC cables to the LF outputs of the calibration box. Connect the 1260 generator output to the calibration box generator input as in Figure 2.

6.3.1 Sequence

Select 300mV from the calibrator, and program the calibration box to 0dB attenuation.

6.3.1.1 This section initialises the 1260 for the first pass calibration of the 3V range.

Calibrator Frequency	1260 Command	Reply	Comment
-	TT1	-	Initialises 1260
-	-	-	Wait 2secs
-	VA1.5	-	Sets 1.5V amplitude
-	WF1	-	Selects square wave
-	RA1,3	-	Calibrating 3V range
-	RA2,3	-	
-	IS5	-	Integration time
-	MS1	-	Delay for cal box to settle
-	CM0	-	Normal calibration mode
-	SO1,2	-	Channel 1/Channel 2
-	OU1,1	-	V1 outer floating
-	OU2,1	-	V2 outer floating

6.3.1.2 This section calibrates the 1260 at each of the LF calibration points. A reply of '00' from the unit indicates a successful calibration, '01' is a failure.

Repeat the following sequence for each frequency in Appendix G from 200Hz to 125kHz inclusive.

Calibrator Frequency	1260 Command	Reply	Comment
-	CA 0,*f*	-	Ideal value for this frequency
*f*Hz	FR *f*	-	Sets frequency
-	SI	00	1260 calibrated

6.3.1.3 This section sets up the 1260 for the first pass calibration of the 300mV range. Set the calibrator to 150mV output, and program 0dB attenuation on the calibration box.

Calibrator Frequency	1260 Command	Reply	Comment
-	RA1,2	-	Calibrating 300mV range
-	RA2,2	-	

6.3.1.4 Repeat Section 6.3.1.2.

6.3.1.5 This section sets up the 1260 for the second pass calibration of the 3V range. This ensures that the amplitude and phase on the 3V range is matched to the 300mV range for both analysers.

Set the calibrator to 300mV output, and program 0dB attenuation on the calibration box.

Calibrator Frequency	1260 Command	Reply	Comment
-	CM3	-	Select second pass mode
-	RA1,3	-	Matching 3V to 300mV range
-	RA2,2	-	

6.3.1.6 Repeat Section 6.3.1.2.

6.3.1.7 This section sets up the 1260 for the first pass calibration of the 30mV range. Set the calibrator to 1.5V output, and program 34dB attenuation on the calibration box.

Calibrator Frequency	1260 Command	Reply	Comment
-	CM0	-	
-	RA1,1	-	Calibrating 30mV range
-	RA2,1	-	

6.3.1.8 Repeat Section 6.3.1.2.

6.3.1.9 This section sets up the 1260 for the second pass calibration of the 30mV range. This ensures that the amplitude and phase on the 30mV range is matched to the 300mV range for both analysers.

Set the calibrator to 1.5V output, and program 34dB attenuation on the cal box.

Calibrator Frequency	1260 Command	Reply	Comment
-	CM3	-	
-	RA1,1	-	Matching 30mV to 300mV range
-	RA2,2	-	

6.3.1.10 Repeat Section 6.3.1.2.

6.3.1.11 LF Verification

NOTE: Verify must be done with the generator calibration disabled. Thus the DIL switch should be set to:

A verification of the LF auto-cal should take place in normal mode, after the LF calibration mode.

The initialise sequence is:

1. Set the unit to NORMAL (SW2 on PCB 22).

2. Issue the following commands:

TT1	Initialise
Wait for initialise to complete, about 2secs	
IS1	Integration time 1sec
MS0.5	Measurement delay of 0.5secs
SO1,2	Source V1/V2
CV1	Magnitude and phase coordinates
OP2,1	Data output to GPIB on

3. Then set up as per 3V/3V overcheck (Section 7.3.6) and check the points in Appendix G, between 200Hz and 125kHz inclusive, against the limits given below.

4. Then set up as per 3V/300mV overcheck (Section 7.3.8) and check the points in Appendix G, between 200Hz and 125kHz inclusive, against the limits given below.

5. Then set up as per 300mV/300mV overcheck (Section 7.3.9) and check the points in Appendix G, between 200Hz and 125kHz inclusive, against the limits given below.

6. Then set up as per 300mV/30mV overcheck (Section 7.3.10) and check the points in Appendix G, between 200Hz and 125kHz inclusive, against the limits given below.

7. Then set up as per 30mV/30mV overcheck (Section 7.3.11) and check the points in Appendix G, between 200Hz and 125kHz inclusive, against the limits given below.

   Limits:

   $0.9995 =< \text{Magnitude} =< 1.0005$
   $-0.05° =< \text{Phase} =< +0.05°$

6.4 HF VOLTAGE ANALYSER CALIBRATION (>125kHz)

6.4.1 Sequence

6.4.1.1 Connect the unterminated ends of the BNC cables to the HF outputs of the calibration box. Connect the terminated ends of the BNC cables to INPUT V1 and INPUT V2 of the 1260. Note the BNC cables must have matched 50Ω terminators. Connect the 1260 generator output to the calibration box AGC input via an unterminated BNC cable as in Figure 6.

Set switch SW2 on PCB 22 to 'CALIBRATE'. Ensure all eight DIL switches SW1 on PCB 22 are in the up position.

Calibrator Frequency	1260 Command	Reply	Comment
-	TT1	-	Initialises 1260
-	-	-	Wait 2secs
-	VA1	-	Sets 1V amplitude
-	IS5	-	Integration time
-	MS20	-	Delay for cal box to settle
-	CM0	-	Normal calibration mode
-	SO1,2	-	Channel 1 / Channel 2
-	FR145E3	-	First calibration point
-	SI	01 or 00	Dummy to allow cal box and W & G to settle

6.4.1.2 This section sets up the 1260 for the first pass calibration of the 3V range, program the cal box to attenuate the signal with 14dB.

Calibrator Frequency	1260 Command	Reply	Comment
-	RA1,3	-	Calibrating 3V range
-	RA2,3	-	Calibrating 3V range
-	CA 0,a	-	Ideal value, obtained via characterisation (refer to Appendix B)

6.4.1.3 This next section calibrates the 1260 at each of the HF calibration points. A reply of '00' from the unit indicates a successful calibration, '01' is a failure.

Repeat the following sequence of instructions for each frequency in Appendix G from 145E3Hz to 32E6Hz. Note a measurement delay of 20secs is required for the 145kHz measurement but all the rest only require 5secs.

Sequence of instructions for first point:

Calibrator Frequency	1260 Command	Reply	Comment
-	MS20	-	Delay for first point
-	FR145E3	-	Frequency
-	SI	00	Calibrate
-	MS5	-	Delay for other points

Sequence of instructions for the rest of the points:

Calibrator Frequency	1260 Command	Reply	Comment
-	FR f	-	Frequency
-	SI	00	Calibrate

6.4.1.4 This section sets up the 1260 for the first pass calibration of the 300mV range, program the calibration box to attenuate the signal with 20dB.

Calibrator Frequency	1260 Command	Reply	Comment
-	RA1,2	-	Calibrating 300mV range
-	RA2,2	-	
-	CA 0,b	-	Ideal value, obtained at characterisation (refer to Appendix B)

6.4.1.5 Repeat Section 6.4.1.3.

6.4.1.6 This section sets up the 1260 for the first pass calibration of the 30mV range, program the calibration box to attenuate the signal with 34dB.

Calibrator Frequency	1260 Command	Reply	Comment
-	RA1,1	-	Calibrating 30mV range
-	RA2,1	-	
-	CA 0,c	-	Ideal value, obtained at characterisation (refer to Appendix B)

6.4.1.7 Repeat Section 6.4.1.3.

6.4.1.8 This section sets up the 1260 for the second pass calibration of the 3V range, program the calibration box to attenuate the signal with 14dB.

Calibrator Frequency	1260 Command	Reply	Comment
-	CM3	-	Second pass mode
-	RA1,3	-	Calibrating 3V range
-	RA2,2	-	
-	CA 0,a	-	Ideal value, obtained at characterisation (refer to Appendix B)

6.4.1.9 Repeat Section 6.4.1.3.

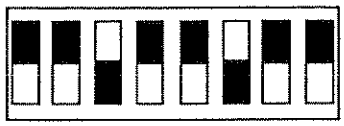
6.4.1.10 This section sets up the 1260 for the second pass calibration of the 30mV range, program the calibration box to attenuate the signal with 34dB.

Calibrator Frequency	1260 Command	Reply	Comment
-	RA1,1	-	Calibrating 30mV range
-	RA2,2	-	
-	CA 0,c	-	Ideal value, obtained at characterisation (refer to Appendix B)

6.4.1.11 Repeat Section 6.4.1.3.

6.4.1.12 HF Verification

NOTE: Verify must be done with the generator calibration disabled. Thus the DIL switch should be set to:



A verification of the HF auto-cal should take place in normal mode, after the HF calibration mode. The initialise sequence is:

1. Set the unit to NORMAL (SW2 on PCB 22).

2. Issue the following commands:

TT1	Initialise
Wait for initialise to complete, about 3secs	
IS1	Integration time 1sec
MS0.5	Measurement delay of 0.5secs
SO1,2	Source V1/V2
CV1	Magnitude and phase coordinates
OP2,1	Data output to GPIB on

3. Then set up as per 3V/3V overcheck (Section 7.3.6) and check the points in Appendix G, between 145kHz and 32MHz inclusive, against the limits given below.

4. Then set up as per 3V/300mV overcheck (Section 7.3.8) and check the points in Appendix G, between 145kHz and 32MHz inclusive, against the limits given below.

5. Then set up as per 300mV/300mV overcheck (Section 7.3.9) and check the points in Appendix G, between 145kHz and 32MHz inclusive, against the limits given below.

6. Then set up as per 300mV/30mV overcheck (Section 7.3.10) and check the points in Appendix G, between 145kHz and 32MHz inclusive, against the limits given below.

7. Then set up as per 30mV/30mV overcheck (Section 7.3.11) and check the points in Appendix G, between 145kHz and 32MHz inclusive, against the limits given below.

Limits:

Frequency =< 1MHz
0.9995 =< Magnitude =< 1.0005
-0.05° =< Phase =< +0.05°

Frequency =< 10MHz
0.9975 =< Magnitude =< 1.0025
-0.25° =< Phase =< +0.25°

Frequency => 10MHz
0.995 =< Magnitude =< 1.005
-0.5° =< Phase =< +0.5°

6.5 VOLTAGE GENERATOR CALIBRATION OF 1260

The generator calibration of the 1260 is achieved using its own analysers, so the unit must have had these calibrated.

6.5.1 Connections

Connect a short BNC cable (less than 20cm) to the 1260 generator output, and connect the other end to INPUT V1 HI on the 1260.

6.5.2 Sequence

6.5.2.1 This section initialises the 1260 for the generator calibration. Set switch SW2 on PCB 22 to 'CALIBRATE'. Ensure all eight DIL switches SW1 on PCB 22 are in the up position.

Calibrator Frequency	1260 Command	Reply	Comment
-	TT1	-	Initialises 1260
-	-	-	Wait 2secs
-	VA1	-	Sets 1V amplitude
-	RA1,3	-	Sets 3V range
-	IS10	-	Integration time
-	MS5	-	Delay for cal box to settle
-	CM4	-	Generator calibration mode
-	SO1,0	-	Channel 1

6.5.2.2 This next section calibrates the 1260 at each of the generator calibration points. A reply of '00' from the unit indicates a successful calibration, '01' is a failure.

Repeat the following sequence of instructions for all the frequencies in Appendix H.

Calibrator Frequency	1260 Command	Reply	Comment
-	FR f	-	Frequency
-	SI	00	Calibrate

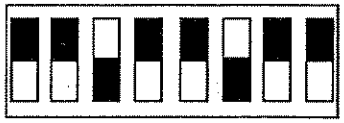
6.6 CURRENT ANALYSER CALIBRATION

6.6.1 Sequence

The current analyser calibration relies on the voltage analysers and generator being calibrated. The first step is to accurately calibrate the 6mA range, and then this is used to characterise the resistors used for the other ranges. If the HP9825 programs for the current calibration are available these should be used.

Set the 1260 GPIB to talker/listener mode. Ensure that the keyswitch is set to normal. Set SW2 on PCB 22 to calibrate and set the switches on SW1 to:

50Ω box, 6mA range



6.6.1.1 This section initialises the 1260 for the first stage in the calibration of the 6mA range, using the 50Ω resistor to calibrate magnitude and phase. Connect the 50Ω resistor box to the 1260.

1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
SO3,0	-	Current calibration
IP1,1	-	Differential input
OU1,0	-	Outer grounded
IS3	-	3secs integration time
MS1	-	1sec delay
RA1,2	-	Using 300mV range
RA3,4	-	Calibrating 6mA range
VA0.3	-	300mV generator amplitude
CA0,50	-	50Ω magnitude
CA1,0	-	0° phase

6.6.1.2 This section calibrates the 1260 on the 6mA range up to 22kHz. Each measurement replies by a '00' for a pass, or a '01' for a failure.

The following sequence of instructions should be executed for all the frequencies in Appendix G from 200Hz to 22E3Hz inclusive.

1260 Command	Reply	Comment
FR f	-	Sets frequency
SI	00	1260 calibrated

6.6.1.3 This section initialises the 1260 for a verification of the calibration points just calibrated. Set SW2 on PCB 22 to normal and set the switches on SW1 to:

The points are checked to 25% of the customer specification, ie. 0.025% and 0.025°.

1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
IS1	-	1sec integration time
OP2,1	-	All data to the GPIB
CZ1	-	Magnitude and phase coordinates
RA1,2	-	Using 300mV range
RA3,4	-	Calibrating 6mA range
VA0.3	-	300mV generator amplitude

6.6.1.4 This section verifies the 1260 on the 6mA range up to 22kHz.

The following instructions should be executed for all frequencies in Appendix G in the range 200Hz to 22E3Hz.

1260 Command	Reply	Comment
FR f	-	Sets frequency
SI	*	Verify calibration

*Each measurement replies with the results, five floating point numbers:

Frequency
Magnitude
Phase
Error
Limit

Each result must be checked, first for no error (Error = 0), and then against the following limits:

49.9875 =< Magnitude =< 50.0125
-0.025° =< Phase =< +0.025°

6.6.1.5 This section initialises the 1260 for the second stage in the 6mA current calibration. This stage uses the 50Ω resistor box to calibrate the magnitude only up to 2MHz. Set SW2 on PCB 22 to calibrate and set the switches on SW1 to:

50Ω box, 6mA range

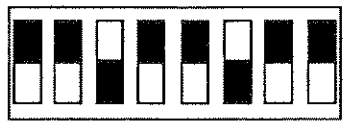
1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
CM2	-	Magnitude only
SO3,0	-	Current calibration
IP1,1	-	Differential input
OU1,0	-	Outer grounded
IS3	-	3secs integration time
MS1	-	1sec delay
RA1,2	-	Using 300mV range
RA3,4	-	Calibrating 6mA range
VA0.3	-	300mV generator amplitude
CA0,50	-	50Ω magnitude

6.6.1.6 This section calibrates the 1260 magnitude on the 6mA range from 32.767999kHz to 2MHz. Each measurement replies by a '00' for a pass, or a '01' for a failure.

The following instructions should be executed for all frequencies in Appendix G in the range 32767.999Hz to 2E6Hz inclusive.

1260 Command	Reply	Comment
FR f	-	Sets frequency
SI	00	1260 calibrated

6.6.1.7 This section initialises the 1260 for a verification of the calibration points just calibrated. Set SW2 on PCB 22 to normal and set the switches on SW1 to:



The points are checked to 25% of the customer specification, ie. 0.025% below 100kHz, 0.05% below 1MHZ and 0.25% below 10MHz.

1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
IS1	-	1sec integration time
OP2,1	-	All data to the GPIB
CZ1	-	Magnitude and phase coordinates
RA1,2	-	Using 300mV range
RA3,4	-	Calibrating 6mA range
VA0.3	-	300mV generator amplitude

6.6.1.8 This section verifies the 1260 magnitude on the 6mA range between 32.767999kHz and 2MHz.

The following instructions should be executed for all frequencies in Appendix G in the range 32767.999Hz to 2E6Hz inclusive.

1260 Command	Reply	Comment
FR f	-	Sets frequency
SI	*	Verify calibration

*Each measurement replies with the results, five floating point numbers:

Frequency
Magnitude
Phase
Error
Limit

Each result must be checked, first for no error (Error = 0), and then against the following limits:

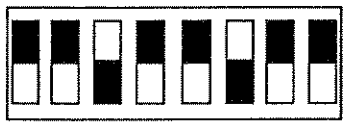
Frequency =< 100kHz
49.9875 =< Magnitude =< 50.0125

Frequency =< 1MHz
49.975 =< Magnitude =< 50.025

Frequency =< 10MHz
49.875 =< Magnitude =< 50.125

6.6.1.9 This section initialises the 1260 for the third stage in the 6mA current calibration. This stage uses the 12.2nF capacitor box to calibrate the phase only up to 200kHz. Set SW2 on PCB 22 to calibrate and set the switches on SW1 to:

12.2nF, 6mA range



Connect the 12.2nF capacitor box to the 1260.

1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
CM1	-	Phase only
SO3,0	-	Current calibration
IP1,1	-	Differential input
OU1,0	-	Outer grounded
IS3	-	3secs integration time
MS1	-	1sec delay
RA1,2	-	Using 300mV range
RA3,4	-	Calibrating 6mA range
VA0.36	-	360mV generator amplitude
CA1,-90	-	-90° phase

6.6.1.10 This section calibrates the 1260 phase on the 6mA range from 32.767999kHz to 200kHz. Each measurement replies by a '00' for a pass, or a '01' for a failure.

The following instructions should be executed for all frequencies in Appendix G in the range 32767.999Hz to 200E3Hz inclusive.

1260 Command	Reply	Comment
FR f	-	Sets frequency
SI	00	1260 calibrated

6.6.1.11 This section initialises the 1260 for a verification of the calibration points just calibrated. Set SW2 on PCB 22 to normal and set the switches on SW1 to:

The points are checked to 25% of the customer specification, ie. 0.025° below 100kHz and 0.05° below 1MHz.

1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
IS1	-	1sec integration time
OP2,1	-	All data to the GPIB
CZ1	-	Magnitude and phase coordinates
RA1,2	-	Using 300mV range
RA3,4	-	Calibrating 6mA range
VA0.36	-	360mV generator amplitude

6.6.1.12 This section verifies the 1260 phase on the 6mA range between 32.767999kHz and 200kHz.

The following instructions should be executed for all frequencies in Appendix G in the range 32767.999Hz to 200E3Hz inclusive.

1260 Command	Reply	Comment
FR f	-	Sets frequency
SI	*	Verify calibration

*Each measurement replies with the results, five floating point numbers:

Frequency
Magnitude
Phase
Error
Limit

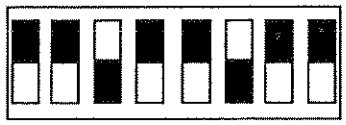
Each result must be checked, first for no error (Error = 0), and then against the following limits:

Frequency =< 100kHz
–90.025 =< Phase =< –89.975

Frequency =< 1MHz
–90.05 =< Phase =< –89.95

6.6.1.13 This section initialises the 1260 for the fourth stage in the 6mA current calibration. This stage uses the 2.2nF capacitor box to calibrate the phase only up to 2MHz. Set SW2 on PCB 22 to calibrate and set the switches on SW1 to:

2.2nF, 6mA range



Connect the 2.2nF capacitor box to the 1260.

1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
CM1	-	Phase only
SO3,0	-	Current calibration
IP1,1	-	Differential input
OU1,0	-	Outer grounded
IS3	-	3secs integration time
MS1	-	1sec delay
RA1,2	-	Using 300mV range
RA3,4	-	Calibrating 6mA range
VA0.22	-	220mV generator amplitude
CA1,-90	-	-90° phase

6.6.1.14 This section calibrates the 1260 phase on the 6mA range from 200kHz to 2MHz. Each measurement replies by a '00' for a pass, or a '01' for a failure.

The following instructions should be executed for all frequencies in Appendix G in the range 200E3Hz to 2E6Hz inclusive.

1260 Command	Reply	Comment
FR f	-	Sets frequency
SI	00	1260 calibrated

6.6.1.15 This section initialises the 1260 for a verification of the calibration points just calibrated. Set SW2 on PCB 22 to normal and set the switches on SW1 to:

The points are checked to 25% of the customer specification, ie. 0.05° below 1MHz and 0.25° below 10MHz.

1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
IS1	-	1sec integration time
OP2,1	-	All data to the GPIB
CZ1	-	Magnitude and phase coordinates
RA1,2	-	Using 300mV range
RA3,4	-	Calibrating 6mA range
VA0.22	-	220mV generator amplitude

6.6.1.16 This section verifies the 1260 phase on the 6mA range between 200kHz and 2MHz.

The following instructions should be executed for all frequencies in Appendix G in the range 200E3Hz to 2E6Hz inclusive.

1260 Command	Reply	Comment
FR f	-	Sets frequency
SI	*	Verify calibration

*Each measurement replies with the results, five floating point numbers:

Frequency
Magnitude
Phase
Error
Limit

Each result must be checked, first for no error (Error = 0), and then against the following limits:

Frequency =< 1MHz:
-90.05 =< Phase =< -89.95

Frequency =< 10MHz:
-90.25 =< Phase =< -89.75

6.6.1.17 This section characterises the RC network box. For this, the 1260 must have been calibrated on the 6mA range up to 2MHz in magnitude and phase. Connect the RC network box to the 1260. Set SW2 on PCB 22 to normal.

1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
IS3	-	3secs integration time
MS1	-	1sec delay
OP2,1	-	All data to the GPIB
FR2E6	-	Frequency set to 2MHz
VA0.5	-	500mV generator amplitude
RA1,2	-	Using 300mV range
RA3,4	-	Calibrating 6mA range
SI	*	Measure the RC network

The measurement replies with the following five floating point numbers:

Frequency
Capacitance
Resistance
Error
Limit

The Error must be 0. The Capacitance, C, and the Resistance, R, must be saved. These will be used to calculate the calibration values for the RC network box, according to the following formulae:

$$\text{Magnitude} = \frac{R}{\sqrt{(1+\omega^2R^2C^2)}}$$

$$\text{Phase} = -\arctan(\omega RC)$$

where ω = 2π*frequency
R approx = 5kΩ
C approx = 100pF

6.6.1.18 This section initialises the 1260 for the final stage in the 6mA current calibration. This stage uses the RC network box to calibrate the magnitude and phase up to 32MHz. The RC network must have been characterised, as in the previous section. Set SW2 on PCB 22 to calibrate and set the switches on SW1 to:

Network, 6mA range

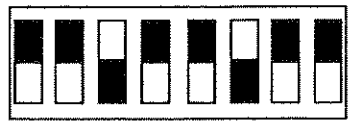
1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
SO3,0	-	Current calibration
IP1,1	-	Differential input
OU1,0	-	Outer grounded
IS3	-	3sec integration time
MS1	-	1sec delay
RA1,2	-	Using 300mV range
RA3,4	-	Calibrating 6mA range
VA0.22	-	220mV generator amplitude

6.6.1.19 This section calibrates the 1260 magnitude and phase on the 6mA range from 4MHz to 32MHz. Each measurement replies by a '00' for a pass, or a '01' for a failure. The calibration values, Z and θ, are the calculated magnitude and phase (see previous section).

The following instructions should be executed for all frequencies in Appendix G in the range 4E6Hz to 32E6Hz inclusive.

1260 Command	Reply	Comment
FR f	-	Sets frequency
CA0,Z	-	Sets magnitude calibration value
CA1,θ	-	Sets phase calibration value
SI	00	1260 calibrated

6.6.1.20 This section initialises the 1260 for a verification of the calibration points just calibrated. Set SW2 on PCB 22 to normal and set the switches on SW1 to:



The points are checked to 25% of the customer specification, ie. 0.25% and 0.25° below 10MHz and 2.5% and 2.5° below 32MHz

1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
IS1	-	1sec integration time
OP2,1	-	All data to the GPIB
CZ1	-	Magnitude and phase coordinates
RA1,2	-	Using 300mV range
RA3,4	-	Calibrating 6mA range
VA0.22	-	220mV generator amplitude

6.6.1.21 This section verifies the 1260 magnitude and phase on the 6mA range between 4MHz and 32MHz. It requires the characterisation data derived in Section 6.6.1.17 for the RC network box.

The following instructions should be executed for all frequencies in Appendix G in the range 4E6Hz to 32E6Hz inclusive.

1260 Command	Reply	Comment
FR f	-	Sets frequency
SI	*	Verify calibration

*Each measurement replies with the results, five floating point numbers:

Frequency
Magnitude
Phase
Error
Limit

Each result must be checked, first for no error (Error = 0), and then against the following limits:

Frequency =< 10MHz:
0.9975*Z =< Magnitude =< 1.0025*Z
θ-0.25 =< Phase =< θ+0.25

Frequency =< 32MHz:
0.975*Z =< Magnitude =< 1.025*Z
θ-2.5 =< Phase =< θ+2.5

Given, $Z = \frac{R}{\sqrt{(1+\omega^2R^2C^2)}}$

And, $\theta = -\arctan(\omega RC)$

where $\omega = 2\pi$*frequency

6.6.1.22 This section initialises the 1260 for the characterisation of the 5Ω resistor by the calibrated 6mA range. Connect the 5Ω resistor box to the 1260.

1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
CZ1	-	Magnitude and phase coordinates
OP2,1	-	All data to the GPIB
IS3	-	3secs integration time
MS1	-	1sec delay
RA1,1	-	Using 30mV range
RA3,4	-	Using 6mA range
VA0.2	-	Generator 200mV

6.6.1.23 This section characterises a resistance box.

The following instructions should be executed for all frequencies in Appendix G in the range 200Hz to 32E6Hz inclusive.

1260 Command	Reply	Comment
FR f	-	Sets frequency
SI	*	Characterise this frequency

*Each measurement replies with the results, five floating point numbers:

Frequency
Magnitude
Phase
Error
Limit

Each result must first be checked for no error (Error = 0). If no error has occurred the Magnitude and Phase results must be saved in an array as the characterisation values for the resistance box.

6.6.1.24 This section initialises the 1260 for the calibration of the 60mA range, using the characterisation values found in the previous section for the 5Ω resistor. Set SW2 on PCB 22 to calibrate and set the switches on SW1 to:

5Ω box, 60mA range

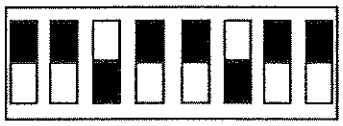
1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
SO3,0	-	Current calibration
IP1,1	-	Differential input
OU1,0	-	Outers grounded
IS3	-	3secs integration time
MS1	-	1sec delay
RA1,2	-	Using 300mV range
RA3,5	-	Using 60mA range
VA1	-	Generator 1V

6.6.1.25 This section calibrates a current range, using magnitude and phase characterisation values Z and θ, appropriate to the current range, and resistor box used. The unit replies with '00' for a pass, '01' for a failure.

The following instructions should be executed for all frequencies in Appendix G in the range 200Hz to 32E6Hz inclusive.

1260 Command	Reply	Comment
FR f	-	Sets frequency
CA0,Z	-	Sets magnitude calibration value
CA1,θ	-	Sets phase calibration value
SI	00	1260 calibrated

6.6.1.26 This section initialises the 1260 for the verification of the points just calibrated. Set SW2 on PCB 22 to normal and set the switches on SW1 to:



1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
IS1	-	1sec integration time
OP2,1	-	All data to the GPIB
CZ1	-	Magnitude and phase coordinates
RA1,2	-	Using 300mV range
RA3,5	-	Using 60mA range
VA1	-	Generator 1V

6.6.1.27 This section verifies a current range. The points are checked to 25% of the customer specification, ie. 0.025% and 0.025° below 100kHz, 0.05% and 0.05° below 1MHz, 0.25% and 0.25° below 10MHz, and 2.5% and 2.5° above 10MHz.

The following instructions should be executed for all frequencies in Appendix G in the range 200Hz to 32E6Hz inclusive.

1260 Command	Reply	Comment
FR f	-	Sets frequency
SI	*	Verify calibration

*Each measurement replies with the results, five floating point numbers:

Frequency
Magnitude
Phase
Error
Limit

The Magnitude and Phase results must be compared with the following limits:

Frequency =< 100kHz:
0.99975*Z =< Magnitude =< 1.00025*Z
θ-0.025° =< Phase =< θ+0.025°

Frequency =< 1MHz:
0.9995*Z =< Magnitude =< 1.0005*Z
θ-0.05° =< Phase =< θ+0.05°

Frequency =< 10MHz:
0.9975*Z =< Magnitude =< 1.0025*Z
θ-0.25° =< Phase =< θ+0.25°

Frequency => 10MHz:
0.975*Z =< Magnitude =< 1.025*Z
θ-2.5° =< Phase =< θ+2.5°

6.6.1.28 This section initialises the 1260 for the characterisation of the 500Ω resistor by the calibrated 6mA range. Connect the 500Ω resistor box to the 1260.

1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
CZ1	-	Magnitude and phase coordinates
OP2,1	-	All data to the GPIB
IS3	-	3secs integration time
MS1	-	1sec delay
RA1,3	-	Using 3V range
RA3,4	-	Using 6mA range
VA1	-	Generator 1V

6.6.1.29 Repeat Section 6.6.1.23.

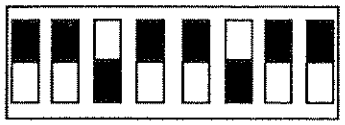
6.6.1.30 This section initialises the 1260 for the calibration of the 600μA range, using the characterisation values found in the previous section for the 500Ω resistor. Set SW2 on PCB 22 to calibrate and set the switches on SW1 to:

500Ω box, 600μA range

1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
SO3,0	-	Current calibration
IP1,1	-	Differential input
OU1,0	-	Outer grounded
IS3	-	3sec sintegration time
MS1	-	1sec delay
RA1,2	-	Using 300mV range
RA3,3	-	Using 600μA range
VA0.2	-	Generator 200mV

6.6.1.31 Repeat Section 6.6.1.25 using the characterisation values for the 500Ω resistor box.

6.6.1.32 This section initialises the 1260 for the verification of the points just calibrated. Set SW2 on PCB 22 to normal and set the switches on SW1 to:



1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
IS1	-	1sec integration time
OP2,1	-	All data to the GPIB
CZ1	-	Magnitude and phase coordinates
RA1,2	-	Using 300mV range
RA3,3	-	Using 600µA range
VA0.2	-	Generator 200mV

6.6.1.33 Repeat Section 6.6.1.27 using the characterisation values for the 500Ω resistor box.

6.6.1.34 This section initialises the 1260 for the characterisation of the 5kΩ resistor by the calibrated 600µA range. Connect the 5kΩ resistor box to the 1260.

1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
CZ1	-	Magnitude and phase coordinates
OP2,1	-	All data to the GPIB
IS3	-	3secs integration time
MS1	-	1sec delay
RA1,3	-	Using 3V range
RA3,3	-	Using 600µA range
VA1	-	Generator 1V

6.6.1.35 This section characterises a resistance box.

The following instructions should be executed for all frequencies in Appendix G in the range 200Hz to 10E6Hz inclusive.

1260 Command	Reply	Comment
FR f	-	Sets frequency
SI	*	Characterise this frequency

*Each measurement replies with the results, five floating point numbers:

Frequency
Magnitude
Phase
Error
Limit

Each result must first be checked for no error (Error = 0). If no error has occurred the Magnitude and Phase results must be saved in an array as the characterisation values for the resistance box.

6.6.1.36 This section initialises the 1260 for the calibration of the 60µA range, using the characterisation values found in the previous section for the 5kΩ resistor. Set SW2 on PCB 22 to calibrate and set the switches on SW1 to:

5kΩ box, 60µA range

1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
SO3,0	-	Current calibration
IP1,1	-	Differential input
OU1,0	-	Outer grounded
IS3	-	3secs integration time
MS1	-	1sec delay
RA1,2	-	Using 300mV range
RA3,2	-	Using 60µA range
VA0.2	-	Generator 200mV

6.6.1.37 This section calibrates a current range, using the magnitude and phase characterisation values, Z and θ, appropriate to the current range, and resistor box used. The unit replies with '00' for a pass, '01' for a failure.

The following instructions should be executed for all frequencies in Appendix G in the range 200Hz to 10E6Hz inclusive.

1260 Command	Reply	Comment
FR f	-	Sets frequency
CA0,Z	-	Sets magnitude calibration value
CA1,J	-	Sets phase calibration value
SI	00	1260 calibrated

6.6.1.38 This section initialises the 1260 for the verification of the points just calibrated. Set SW2 on PCB 22 to normal and set the switches on SW1 to:

1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
IS1	-	1sec integration time
OP2,1	-	All data to the GPIB
CZ1	-	Magnitude and phase coordinates
RA1,2	-	Using 300mV range
RA3,2	-	Using 60μA range
VA0.2	-	Generator 200mV

6.6.1.39 This section verifies a current range. The points are checked to 25% of the customer specification, ie. 0.025% and 0.025° below 100kHz, 0.05% and 0.05° below 1MHz, 0.25% and 0.25° below 10MHz, and 2.5% and 2.5° above 10MHz.

The following instructions should be executed for all frequencies in Appendix G in the range 200Hz to 10E6Hz inclusive.

1260

Command	**Reply**	**Comment**
FR f	-	Sets frequency
SI	*	Verify calibration

*Each measurement replies with the results, five floating point numbers:

Frequency
Magnitude
Phase
Error
Limit

The Magnitude and Phase results must be compared with the following limits:

Frequency =< 100kHz:
0.99975*Z =< Magnitude =< 1.00025*Z
θ-0.025° =< Phase =< θ+0.025°

Frequency =< 1MHz:
0.9995*Z =< Magnitude =< 1.0005*Z
θ-0.05° =< Phase =< θ+0.05°

Frequency =< 10MHz:
0.9975*Z =< Magnitude =< 1.0025*Z
θ-0.25° =< Phase =< θ+0.25°

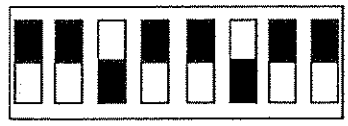
6.6.1.40 This section initialises the 1260 for the characterisation of the 50kΩ resistor by the calibrated 60µA range. Connect the 50kΩ resistor box to the 1260.

1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
CZ1	-	Magnitude and phase coordinates
OP2,1	-	All data to the GPIB
IS3	-	3secs integration time
MS1	-	1sec delay
RA1,3	-	Using 3V range
RA3,2	-	Using 60µA range
VA1	-	Generator 1V

6.6.1.41 Repeat Section 6.6.1.35.

6.6.1.42 **This section initialises the 1260 for the calibration of the 6µA range, using the** characterisation values found in the previous section for the 50kΩ resistor. Set SW2 on PCB 22 to calibrate and set the switches on SW1 to:

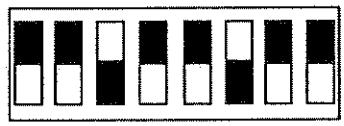
50kΩ box, 6µA range



1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
SO3,0	-	Current calibration
IP1,1	-	Differential input
OU1,0	-	Outer grounded
IS3	-	3secs integration time
MS1	-	1sec delay
RA1,2	-	Using 300mV range
RA3,1	-	Using 6µA range
VA0.2	-	Generator 200mV

6.6.1.43 Repeat Section 6.6.1.37 using the characterisation values for the 50kΩ resistor box.

6.6.1.44 This section initialises the 1260 for the verification of the points just calibrated. Set SW2 on PCB 22 to normal and set the switches on SW1 to:



1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
IS1	-	1sec integration time
OP2,1	-	All data to the GPIB
CZ1	-	Magnitude and phase coordinates
RA1,2	-	Using 300mV range
RA3,1	-	Using 6μA range
VA0.2	-	Generator 200mV

6.6.1.45 Repeat Section 6.6.1.39 using the characterisation values for the 50kΩ resistor box.

6.7 CURRENT GENERATOR CALIBRATION

6.7.1 Connections

Connect a short BNC cable (less than 20cm) to the 1260 generator output, and connect the other end to INPUT I on the 1260.

6.7.2 Sequence

6.7.2.1 This section initialises the 1260 for the generator calibration. It assumes that the 60mA current range is calibrated. Set switch SW2 on PCB 22 to 'CALIBRATE'. Ensure all eight DIL switches SW1 on PCB 22 are in the up position.

1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
VA0	-	Sets 0V amplitude
IA0.02	-	Sets 20mA amplitude
GT1	-	Selects current generator
RA3,5	-	Sets 60mA range
IS10	-	Integration time
MS5	-	Delay for cal box to settle
CM4	-	Generator calibration mode
SO3,0	-	Current channel

6.7.2.2 This next section calibrates the 1260 at each of the generator calibration points. A reply of '00' from the unit indicates a successful calibration, '01' is a failure.

Repeat the following sequence of instructions for all frequencies in Appendix H.

1260 Command	Reply	Comment
FR f	-	Frequency
SI	00	Calibrate

6.8 CONCLUSION

The unit is now calibrated, and requires that the date and place of calibration be stored.

Calibrator Frequency	1260 Command	Reply	Comment
-	PC text (4 chars)	-	Code for the place of calibration: GB-F is SCHLUMBERGER, FARNBOROUGH.
-	YR i	-	Year of calibration, eg. 87
-	WK i	-	Week of calibration 1 to 53

Set the calibration switch (SW1 on PCB 22) to 'NORMAL', set all the DIL switches (SW2 on PCB 22) to the up position and then initialise the instrument.

Calibrator Frequency	1260 Command	Reply	Comment
-	TT1	-	Initialise the 1260

This completes the 1260 Calibration.

7 FUNCTIONAL OVERCHECK

Any failure, except that of the current analyser or generator, during the overcheck that requires component changes or re-calibration, necessitates a re-run of the full overcheck.

A failure of the current analyser that requires component changes or re-calibration can be re-overchecked for the current analyser overcheck only.

A failure of the generator that requires component changes or re-calibration can be re-overchecked for the generator overcheck only.

Overcheck should be carried out at a temperature in the range 17-23°C.

The overcheck can be carried out using either the front panel, the serial interface or the GPIB to input the commands for Section 7.1 onwards. The remote commands corresponding to key entries are given in [ ]; however, the full details of implementing remote operation via the GPIB will depend on which controller is used and are therefore not given here. For serial interface, results will be returned to the VDU or terminal by commanding OP1,1.

If the analyser or generator accuracy overcheck fails, it may be necessary to recalibrate a single point using the procedure set out in Appendix A, or to repeat the entire calibration procedure.

Ensure that all eight DIL switches on PCB 22 (SW1) are in the up position and that the calibration switch (SW2) is set to normal. Also ensure that the keyswitch on the rear panel is set to normal.

7.1 DISPLAY CHECK

Set up the following:

SELF-TEST	Initialise	[TT1]
wait for 2secs		
SELF-TEST	Test	[TT0]

7.1.1 Carefully observe the display for missing dots and signs of short circuits between rows as the moving pattern cycles round.

7.1.2 Press Enter, then carefully observe the next pattern for evidence of short circuits between columns.

7.1.3 Press Enter, then carefully observe the pattern of characters to check that each one is correctly displayed.

7.1.4 Press Enter, then press each key in turn terminating with Enter, checking that the 1260 gives the correct response to each key and finishes with the TEST PASS message.

The tests can be done either manually following the procedures of Section 7.2 or by using ATS program 12606599 as specified in Section 8.1.

7.2 SERIAL INTERFACE CHECK

Connect an RS423 terminal to the 1260 serial interface port, ensure the are both at the same baud rate and type in TT1 (Carriage return). Check that the display indicates INITIALISED.

7.2.1 Command the following using the terminal:

FR 299
VA 3
SO 1,0
CV 1
RE

Connect Channel 1 to the Generator output and note that the 1260 is now taking readings at 299Hz and that the display is being updated with Co-ordinates set to r,θ.

7.2.2 Command OP1,1 and observe that readings are printed on the terminal.

7.2.3 Command OP1,0 and remove the terminal.

7.3 ANALYSER CHECK

Set up the following:

SELF-TEST	Initialise		[TT1]
GENERATOR	Frequency	299Hz	[FR299]
	Amplitude	2V	[VA2]
ANALYSER			
NEXT	V1 outer	Floating	[OU1,1]
	V1 input	Single	[IP1,0]
DISPLAY	Source	Ch1	[SO1,0]
	Coords	r,θ	[CV1]
RECYCLE			[RE]

7.3.1 Phase lock the Calibrator to the Generator output and connect the Calibrator output to Channel 1 input, ensuring that the Calibrator LO output is not connected to ground. Command [WF1] over the GPIB.

Note the calibrator outputs in section 7.3.2 are the nominal values and must be replaced by the characterised value as obtained in Appendix D. The characterisation must be repeated at least once every six months.

7.3.2 Check that the following voltages are measured correctly on Channel 1:

Freq	Input Range	Calibrator O/P Nominal	Reading	Comment
299Hz	30mV	1V	19.9 to 20.1mV	[FR299;RA1,1]*
299Hz	30mV	1.5V	No overload indicated	*
299Hz	300mV	200mV	199.60 to 200.40mV	[RA1,2]
299Hz	3V	2V	1.9960 to 2.0040mV	[RA1,3]
299Hz	3V	3V	2.9940 to 3.0060V	
299Hz	3V	1V	0.9980 to 1.0020V	
299Hz	3V	0.5V	0.4990 to 0.5010V	
299Hz	3V	0.2V	0.1990 to 0.2010V	
299Hz	3V	0.1V	0.0990 to 0.1010V	
3kHz	30mV	1V	19.9 to 20.1mV	[FR3E3:RA1,1]*
3kHz	30mV	1.5V	No overload indicated	*
3kHz	300mV	200mV	199.6 to 200.4mV	[RA1,2]
3kHz	3V	2V	1.9960 to 2.004mV	[RA1,3]
60kHz	30mV	1V	19.9 to 20.1mV	[FR6E4;RA1,1]*
60kHz	300mV	200mV	199.4 to 200.6mV	[RA1,2]
60kHz	3V	2V	1.9940 to 2.006mV	[RA1,3]
100kHz	30mV	1V	19.85 to 20.15mV	[FR1E5:RA1,1]*
100kHz	300mV	200mV	198.8 to 201.2mV	[RA1,2]
100kHz	3V	2V	1.988 to 2.012mV	[RA1,3]
145kHz	30mV	1V	19.85 to 20.15mV	[FR145E3;RA1,1]*
145kHz	300mV	200mV	198.8 to 201.2mV	[RA1,2]
145kHz	3V	2V	1.988 to 2.012mV	[RA1,3]

Repeat for Channel 2. *Select 34dB attenuator.

7.3.3 Common Mode

Apply the signal from the calibrator output HI to both HI and LO terminals of Channel 1 and the calibrator LO to the shield.

Set up the following:

GENERATOR	Frequency	10Hz	[FR10]
	Amplitude	3V	[VA3]
ANALYSER			
NEXT	Input (V1)	Diff	[IP1,1]
	Range	300mV	[RA1,2]
RECYCLE			[RE]

Command [WF1] over the GPIB. Apply 3V common mode. Check that this common mode signal is rejected for Channel 1 as follows:

Freq	Input Range	Calibrator O/P	Reading
10Hz	300mV	3V	<3mV

Repeat for Channel 2.

7.3.4 ANALYSERS CHANNEL TO CHANNEL

Overcheck analyser matching from 1Hz to 100kHz

Connect the generator to Channels 1 and 2 via a power splitter as in Figure 9.

Set up the following:

SELF-TEST	Initialise		[TT1]
ANALYSER	Int time	0.3sec	[IS0.3]
DISPLAY	Source	V1/V2	[SO1,2]
SWEEP	Δ log	400pts/swp	[SF400]
NEXT	Frequency	1Hz	[FM1]
		100kHz	[FX1E5]
NEXT	Enable	log f	[SW2]
DATA OUTPUT	File	all	[OP3,1]

7.3.5 Learn the following program:

LEARN PROG	Learn	1	[#L1]
DATA OUTPUT			
PREV	Stats	par1	[SX0]
SCALE	Limits	par1	[LI1]
		0.9985	[LV0,0.9985]
		1.0015	[LV1,1.0015]
LIST FILE			[FO]
PAUSE/CONTINUE			[CP]
DATA OUTPUT			
PREV	Stats	par2	[SX1]
SCALE	Limits	par2	[LI2]
		0.2	[LV0,-0.2]
		-0.2	[LV1,0.2]
LIST FILE			[FO]
	Quit		[#Q]

7.3.6 Set up the following:

GENERATOR	Amplitude	3V	[VA3]
ANALYSER			
NEXT	Range	3V	[RA1,3]
NEXT	Range	3V	[RA2,3]
RECYCLE			[RE]

7.3.7 When the sweep is over set up the following:

EXECUTE	1	[EP1]

Check the display for no failures.

STATUS		
NEXT	Stats	
	Read minimum value	[?MI]
	Read maximum value	[?MA]

Check these values against the magnitude limits.

PAUSE/CONTINUE [CP]

Check the display for no failures.

STATUS		
NEXT	Stats	
	Read minimum value	[?MI]
	Read maximum value	[?MA]

Check these values against the phase limits.

7.3.8 Set up the following:

GENERATOR	Amplitude	1.2V	[VA1.2]
ANALYSER			
NEXT	Range	3V	[RA1,3]
NEXT	Range	300mV	[RA2,2]
RECYCLE			[RE]

Repeat test 7.3.7.

7.3.9 Set up the following:

GENERATOR	Amplitude	0.6V	[VA0.6]
ANALYSER			
NEXT	Range	300mV	[RA1,2]
NEXT	Range	300mV	[RA2,2]
RECYCLE			[RE]

Repeat test 7.3.7.

7.3.10 Set up the following:

GENERATOR	Amplitude	0.12V	[VA0.12]
ANALYSER			
NEXT	Range	300mV	[RA1,2]
NEXT	Range	30mV	[RA2,1]
RECYCLE			[RE]

Repeat test 7.3.7.

7.3.11 Set up the following:

GENERATOR	Amplitude	0.06V	[VA0.06]
ANALYSER			
NEXT	Range	30mV	[RA1,1]
NEXT	Range	30mV	[RA2,1]
RECYCLE			[RE]

Repeat test 7.3.7.

7.3.12 Overcheck from 100kHz to 1MHz:

SWEEP	Δ lin	100pts/swp	[LF100]
NEXT	Frequency	100kHz	[FM1E5]
		1MHz	[FX1E6]
NEXT	Enable	lin f	[SW1]
DATA OUTPUT	File	all	[OP3,1]

Repeat from Section 7.3.6 to Section 7.3.11.

7.3.13 Overcheck from 1MHz to 10MHz:

SWEEP			
NEXT	Frequency	1MHz	[FM1E6]
		10MHz	[FX1E7]
NEXT	Enable	lin f	[SW1]
DATA OUTPUT	File	all	[OP3,1]

Learn the following program or edit the limits in the program learnt in Section 7.3.5.

LEARN PROG	Learn	1	[#L1]
DATA OUTPUT			
PREV	Stats	par1	[SX0]
SCALE	Limits	par1	[LI1]
		0.9925	[LV0,0.9925]
		1.0075	[LV1,1.0075]
LIST FILE			[FO]
PAUSE/CONTINUE			[CP]
DATA OUTPUT			
PREV	Stats	par2	[SX1]
SCALE	Limits	par2	[LI2]
		0.75	[LV0,-0.75]
		–0.75	[LV1,0.75]
LIST FILE			[FO]
	Quit		[#Q]

Repeat from Section 7.3.6 to Section 7.3.11.

7.3.14 Overcheck from 10MHz to 32MHz:

GENERATOR	Amplitude	1V	[VA1]
SWEEP			
NEXT	Frequency	10MHz	[FM1E7]
		32MHz	[FX3.2E7]
NEXT	Enable	lin f	[SW1]
DATA OUTPUT	File	all	[OP3,1]

Learn the following program or edit the limits in the program learnt in Section 7.3.5.

LEARN PROG	Learn	1	[#L1]
DATA OUTPUT			
PREV	Stats	par1	[SX0]
SCALE	Limits	par1	[LI1]
		0.9625	[LV0,0.9625]
		1.0375	[LV1,1.0375]

LIST FILE			[FO]
PAUSE/CONTINUE			[CP]
DATA OUTPUT			
PREV	Stats	par2	[SX1]
SCALE	Limits	par2	[LI2]
		–3.75	[LV0,-3.75]
		3.75	[LV1,3.75]
LIST FILE			[FO]
	Quit		[#Q]

Repeat from Section 7.3.9 to Section 7.3.11.

7.3.15 Connect the generator output to the 1260 test box and the analysers terminated in 50Ω to the 1260 test box hf Channel 1 and Channel 2 outputs as in Figure 6.

7.3.16 Set up the following:

GENERATOR	Amplitude	1V	[VA1]
ANALYSER			
NEXT	Range	3V	[RA1,3]
NEXT	Range	3V	[RA2,3]
RECYCLE			[RE]

Repeat test 7.3.7.

7.3.17 Call up the –14dB attenuator in the calibration box and set up the following:

ANALYSER			
NEXT	Range	3V	[RA1,3]
NEXT	Range	300mV	[RA2,2]
RECYCLE			[RE]

Repeat test 7.3.7.

7.3.18 CURRENT ANALYSER

This overcheck uses the resistor boxes used in the calibration to overcheck the current analyser. The voltage analysers and generator must be calibrated. If the HP9825 program is available, this should be used.

7.3.18.1 This section initialises the 1260 for the overcheck on the 6mA range in the frequency range up to 22kHz, using the 50Ω resistor box for magnitude and phase. The check is made to 100% of the customer specification, ie. 0.1% and 0.1°. Set SW2 on PCB 22 to normal, and connect the 50Ω resistor box to the 1260.

1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
IS1	-	1sec integration time
OP2,1	-	All data to the GPIB
CZ1	-	Magnitude and phase coordinates
RA3,4	-	Overchecking the 6mA range
SW2	-	Log frequency sweep
FM1	-	From 1Hz
FX22E3	-	To 22kHz

7.3.18.2 This section overchecks the 6mA range at the top of the range.

1260 Command	Reply	Comment
VA0.6	-	Selects 600mV amplitude
-	-	The following loop is repeated 200 times
SI	*	Overchecking

*The results come in the form of five floating point numbers:

Frequency
Magnitude
Phase
Error
Limit

The magnitude and phase should be checked against the following limits:

49.95 =< Magnitude =< 50.05
-0.1° =< Phase =< +0.1°

7.3.18.3 This section overchecks the 6mA range at the bottom of the range.

1260 Command	Reply	Comment
VA0.06	-	Selects 60mV amplitude
-	-	The following loop is repeated 200 times
SI	*	Overchecking

*The results come in the form of five floating point numbers:

Frequency
Magnitude
Phase
Error
Limit

The magnitude and phase should be checked against the following limits:

49.95 =< Magnitude =< 50.05
-0.1° =< Phase =< +0.1°

7.3.18.4 This section initialises the 1260 for the overcheck on the 6mA range in the frequency range 22kHz to 2MHz, using the 50Ω resistor box for magnitude only. The check is made to 100% of the customer specification, ie. 0.1% below 100kHz, 0.2% below 1MHz and 1% below 10MHz. Set SW2 on PCB 22 to normal, and connect the 50Ω resistor box to the 1260.

1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
IS1	-	1sec integration time
OP2,1	-	All data to the GPIB
CZ1	-	Magnitude and phase coordinates
RA3,4	-	Overchecking the 6mA range
SW2	-	Log frequency sweep
FM22E3	-	From 22kHz
FX2E6	-	To 2MHz

7.3.18.5 This section overchecks the 6mA range at the top of the range.

1260 Command	Reply	Comment
VA0.6	-	Selects 600mV amplitude
-	-	The following loop is repeated 200 times
SI	*	Overchecking

*The results come in the form of five floating point numbers:

Frequency
Magnitude
Phase
Error
Limit

The magnitude should be checked against the following limits:

Frequency =< 100kHz:
49.95 =< Magnitude =< 50.05

Frequency =< 1MHz:
49.9 =< Magnitude =< 50.1

Frequency =< 10MHz:
49.5 =< Magnitude =< 50.5

7.3.18.6 This section overchecks the 6mA range at the bottom of the range.

1260 Command	Reply	Comment
VA0.06	-	Selects 60mV amplitude
-	-	The following loop is repeated 200 times
SI	*	Overchecking

*The results come in the form of five floating point numbers:

Frequency
Magnitude
Phase
Error
Limit

The magnitude should be checked against the following limits:

Frequency =< 100kHz:
49.95 =< Magnitude =< 50.05

Frequency =< 1MHz:
49.9 =< Magnitude =< 50.1

Frequency =< 10MHz:
49.5 =< Magnitude =< 50.5

7.3.18.7 This section initialises the 1260 for the overcheck on the 6mA range in the frequency range 22kHz to 200kHz, using the 12.2nF capacitor box for phase only. The check is made to 100% of the customer specification, ie. 0.1° below 100kHz, 0.2° below 1MHz and 1° below 10MHz. Set SW2 on PCB 22 to normal, and connect the 12.2nF capacitor box to the 1260.

1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
IS1	-	1sec integration time
OP2,1	-	All data to the GPIB
CZ1	-	Magnitude and phase coordinates
RA3,4	-	Overchecking the 6mA range
SW2	-	Log frequency sweep
FM22E3	-	From 22kHz
FX2E5	-	To 200kHz
VA0.36	-	Amplitude 360mV

7.3.18.8 This section overchecks a current range.

1260 Command	Reply	Comment
-	-	The following loop is repeated 200 times
SI	*	Overchecking

*The results come in the form of five floating point numbers:

Frequency
Magnitude
Phase
Error
Limit

The phase should be checked against the following limits:

Frequency = < 100kHz:
−0.1° = < Phase = < +0.1°

Frequency = < 1MHz:
−0.2° = < Phase = < +0.2°

Frequency = < 10MHz:
−1° = < Phase = < +1°

7.3.18.9 This section initialises the 1260 for the overcheck on the 6mA range in the frequency range 200kHz to 2MHz, using the 2.2nF capacitor box for phase only. The check is made to 100% of the customer specification, ie. 0.2° below 1MHz and 1° below 10MHz. Set SW2 on PCB 22 to normal, and connect the 2.2nF capacitor box to the 1260.

1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
IS1	-	1sec integration time
OP2,1	-	All data to the GPIB
CZ1	-	Magnitude and phase coordinates
RA3,4	-	Overchecking the 6mA range
SW2	-	Log frequency sweep
FM2E5	-	From 200kHz
FX2E6	-	To 2MHz
VA0.22	-	Amplitude 220mV

7.3.18.10 Repeat Section 7.3.18.8.

7.3.18.11 The overcheck for the range 2MHz to 32MHz requires the RC network to be characterised. Repeat Section 6.6.1.17.

7.3.18.12 This section initialises the 1260 for the overcheck of the range 2MHz to 32MHz, using the RC network box for magnitude and phase. The points are checked to 100% of the customer specification, ie. 1% and 1° below 10MHz and 10% and 10° below 32MHz. Set SW2 on PCB 22 to normal, and connect the RC network box.

1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
IS1	-	1sec integration time
OP2,1	-	All data to the GPIB
CZ1	-	Magnitude and phase coordinates
RA3,4	-	Overchecking the 6mA range
SW2	-	Log frequency sweep
FM2E6	-	From 2MHz
FX32E6	-	To 32MHz
VA0.22	-	220mV generator amplitude

7.3.18.13 This section overchecks the 6mA range.

1260 Command	Reply	Comment
-	-	The following loop is repeated 200 times
SI	*	Overchecking

*Each measurement replies with the results, five floating point numbers:

Frequency
Magnitude
Phase
Error
Limit

Each result must be checked against the following limits:

Frequency $=<$ 10MHz:
$0.99*Z =<$ Magnitude $=< 1.01*Z$
$\theta-1° =<$ Phase $=< \theta+1°$

Frequency $=<$ 32MHz:
$0.9*Z =<$ Magnitude $=< 1.1*Z$
$\theta-10° =<$ Phase $=< \theta+10°$

Given, $Z = \dfrac{R}{\sqrt{(1+\omega^2R^2C^2)}}$

And, $\theta = -\arctan(\omega RC)$

where $\omega = 2\pi*\text{frequency}$

7.3.18.14 This section initialises the 1260 for the 60mA overcheck. This is done by normalising the 5Ω resistor box on the 6mA range, and examining the normalised results of two sweeps, one in the middle of the 60mA range, and one at the bottom. Set SW2 on PCB 22 to normal and connect the 5Ω resistor box. The results are checked to 100% of the customer specification, ie. 0.1% and 0.1° below 100kHz, 0.2% and 0.2° below 1MHz, 1% and 1° below 10MHz and 10% and 10° above 10MHz.

1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
IS1	-	1sec integration time
CZ1	-	Magnitude and phase coordinates
SW2	-	Log frequency sweep
FM10	-	From 10Hz
FX32E6	-	To 32MHz
SF240	-	240 point sweep
VA0.15	-	150mV generator amplitude
RA3,4	-	Normalising to the 6mA range

7.3.18.15 This section evaluates normalisation constants. This is best achieved by setting the 1260 to request service from the controller at the end of the normalising sweep as shown. It could also be done by reading in the result of each measurement, and counting the 240 measurements in the sweep.

1260 Command	Reply	Comment
*SRE4	-	Sets the 1260 to interrupt at the end of sweep
NO2	-	Evaluate normalisation values
-	-	And now wait for the end of sweep RQS from the 1260

7.3.18.16 This section sets the 1260 up to carry out the middle of range normalised overcheck.

1260 Command	Reply	Comment
OP2,1	-	All results to the GPIB
RA3,5	-	Overchecking the 60mA range
VA1	-	1V amplitude, gives approx 17mA

7.3.18.17 This section overchecks the normalised sweep range.

1260 Command	Reply	Comment
-	-	The following loop is repeated 240 times
SI	*	Overchecking

*Each measurement replies with the results, five floating point numbers:

Frequency
Magnitude
Phase
Error
Limit

Each result must be checked against the following limits:

Frequency =< 100kHz:
0.999 =< Magnitude =< 1.001
-0.1° =< Phase =< +0.1°

Frequency =< 1MHz:
0.998 =< Magnitude =< 1.002
-0.2° =< Phase =< +0.2°

Frequency =< 10MHz:
0.99 =< Magnitude =< 1.01
-1° =< Phase =< +1°

Frequency =< 32MHz:
0.9 =< Magnitude =< 1.1
-10° =< Phase =< +10°

7.3.18.18 This section sets the 1260 up to carry out the bottom of range normalised overcheck.

1260 Command	Reply	Comment
VA0.35	-	350mV amplitude, gives approx 6.25mA

7.3.18.19 Repeat Section 7.3.18.17.

7.3.18.20 This section initialises the 1260 for the 600µA overcheck. This is done by normalising the 500Ω resistor box on the 6mA range, and examining the normalised results of two sweeps, one in the middle of the 600µA range, and one at the bottom. Set SW2 on PCB 22 to normal and connect the 500Ω resistor box. The results are checked to 100% of the customer specification, ie. 0.1% and 0.1° below 100kHz, 0.2% and 0.2° below 1MHz, 1% and 1° below 10MHz and 10% and 10° above 10MHz.

1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
IS1	-	1sec integration time
CZ1	-	Magnitude and phase coordinates
SW2	-	Log frequency sweep
FM10	-	From 10Hz
FX32E6	-	To 32MHz
SF240	-	240 point sweep
VA1	-	1V generator amplitude
RA3,4	-	Normalising to the 6mA range

7.3.18.21 Repeat Section 7.3.18.15.

7.3.18.22 This section sets the 1260 up to carry out the middle of range normalised overcheck.

1260 Command	Reply	Comment
OP2,1	-	All results to the GPIB
RA3,3	-	Overchecking the 600µA range
VA0.17	-	170mV amplitude, gives approx 310µA

7.3.18.23 Repeat Section 7.3.18.17.

7.3.18.24 This section sets the 1260 up to carry out the bottom of range normalised overcheck.

1260 Command	Reply	Comment
VA0.035	-	35mV amplitude, gives approx 60µA

7.3.18.25 Repeat Section 7.3.18.17.

7.3.18.26 This section initialises the 1260 for the 60µA overcheck. This is done by normalising the 5kΩ resistor box on the 600µA range, and examining the normalised results of two sweeps, one in the middle of the 60µA range, and one at the bottom. Set SW2 on PCB 22 to normal and connect the 5kΩ resistor box. The results are checked to 100% of the customer specification, ie. 0.1% and 0.1° below 100kHz, 0.2% and 0.2° below 1MHz, 1% and 1° below 10MHz and 10% and 10° above 10MHz.

1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
IS1	-	1sec integration time
CZ1	-	Magnitude and phase coordinates
SW2	-	Log frequency sweep
FM10	-	From 10Hz
FX10E6	-	To 10MHz
SF240	-	240 point sweep
VA1	-	1V generator amplitude
RA3,3	-	Normalising to the 600µA range

7.3.18.27 Repeat Section 7.3.18.15.

7.3.18.28 This section sets the 1260 up to carry out the middle of range normalised overcheck.

1260 Command	Reply	Comment
OP2,1	-	All results to the GPIB
RA3,2	-	Overchecking the 60µA range
VA0.17	-	170mV amplitude, gives approx 33µA

7.3.18.29 Repeat Section 7.3.18.17.

7.3.18.30 This section sets the 1260 up to carry out the bottom of range normalised overcheck.

1260 Command	Reply	Comment
VA0.035	-	35mV amplitude, gives approx 6.4µA

7.3.18.31 Repeat Section 7.3.18.17.

7.3.18.32 This section initialises the 1260 for the 6µA overcheck. This is done by normalising the 50kΩ resistor box on the 60µA range, and examining the normalised results of two sweeps, one in the middle of the 6µA range, and one at the bottom. Set SW2 on PCB 22 to normal and connect the 50kΩ resistor box. The results are checked to 100% of the customer specification, ie. 0.1% and 0.1° below 100kHz, 0.2% and 0.2° below 1MHz, 1% and 1° below 10MHz and 10% and 10° above 10MHz.

1260 Command	Reply	Comment
TT1	-	Initialises 1260
-	-	Wait 2secs
IS1	-	1sec integration time
CZ1	-	Magnitude and phase coordinates
SW2	-	Log frequency sweep
FM10	-	From 10Hz
FX10E6	-	To 10MHz
SF240	-	240 point sweep
VA1	-	1V generator amplitude
RA3,2	-	Normalising to the 60µA range

7.3.18.33 Repeat Section 7.3.18.15.

7.3.18.34 This section sets the 1260 up to carry out the middle of range normalised overcheck.

1260 Command	Reply	Comment
OP2,1	-	All results to the GPIB
RA3,1	-	Overchecking the 6µA range
VA0.17	-	170mV amplitude, gives approx 3.4µA

7.3.18.35 Repeat Section 7.7.18.17.

7.3.18.36 This section sets the 1260 up to carry out the bottom of range normalised overcheck.

1260 Command	Reply	Comment
VA0.035	-	35mV amplitude, gives approx 660nA

7.3.18.37 Repeat Section 7.3.18.17.

7.4 GENERATOR CHECK

7.4.1 Set up the following:

SELF-TEST	Initialise		[TT1]
GENERATOR	Frequency	50MHz	[5E-2]
	Amplitude	1V	[VA1]

7.4.2 Connect the Frequency Counter to the generator output terminals, program each of the following output frequencies in turn and check that the frequency counter gives the correct reading (measuring period at the lower frequencies):

Frequency	**Counter**	
50mHz	19.998 to 20.002sec	[FR0.05]
500mHz	1.9998 to 2.0002sec	[FR0.5]
2.5Hz	399.98 to 400.02msec	[FR2.5]
25Hz	24 to 26Hz	[FR25]
250Hz	249 to 251Hz	[FR250]
700Hz	699.9 to 700.1Hz	[FR700]
1kHz	0.9999 to 1.0001kHz	[FR1E3]
2kHz	1.9998 to 2.0002kHz	[FR2E3]
3kHz	2.9997 to 3.0003kHz	[FR3E3]
4kHz	3.9996 to 4.0004kHz	[FR4E3]
5kHz	4.9995 to 5.0005kHz	[FR5E3]
6kHz	5.9994 to 6.0006kHz	[FR6E3]
30kHz	29.998 to 30.002kHz	[FR3E4]
50kHz	49.995 to 50.005kHz	[FR5E4]
70kHz	69.993 to 70.007kHz	[FR7E4]
100kHz	99.99 to 100.01kHz	[FR1E5]
600kHz	599.94 to 600.06kHz	[FR6E5]
700kHz	699.93 to 700.07kHz	[FR7E5]
1MHz	0.9999 to 1.0001MHz	[FR1E6]
6MHz	5.9994 to 6.0006MHz	[FR6E6]
7MHz	6.9993 to 7.0007MHz	[FR7E6]
20MHz	19.998 to 20.002MHz	[FR2E7]
32MHz	31.9968 to 32.0032MHz	[FR3.2E7]

Disconnect the Frequency Counter.

7.4.3 Generator Kill

Connect a short circuit across the generator kill inputs (rear panel) and observe the generator output on the oscilloscope, the generator output should drop to zero and an error be displayed.

Release the generator kill inputs and observe the output waveform re-commence. Remove the oscilloscope.

7.4.4 Set up the following:

GENERATOR	Frequency	300Hz	[FR300]
DISPLAY	Result	V1	[SO1,0]
ANALYSER			
NEXT	Input	Single	[IP1,0]

Measure the following generator outputs on Channel 1 and check that the readings are within the limits stated:

GENERATOR	V.Ampl	*Volts	[VA*]

***Amplitude**	**Limits**	
3V	2.92 to 3.08V	[VA3]
1V	0.97 to 1.03V	[VA1]
0.8V	0.775 to 0.825V	[VA0.8]
0.6V	0.580 to 0.620V	[VA0.6]
0.4V	0.385 to 0.415V	[VA0.4]
0.2V	0.190 to 0.210V	[VA0.2]
0.1V	0.092 to 0.108V	[VA0.1]
0.02V	0.015 to 0.025V	[VA0.02]
0.01V	0.005 to 0.015V	[VA0.01]

7.4.5 Connect a DVM across the generator output terminals and set up the following:

GENERATOR	V.Ampl	0V	[VA0]

Set the bias voltages (V.Bias) as follows, and for each voltage check that the DVM reading is within the limits:

GENERATOR	V.Bias	*Volts	[VB*]

***Bias**	**DVM Reading**	
40V	39.5 to 40.5V	[VB 40]
20V	19.7 to 20.3V	[VB 20]
10V	9.94 to 10.06V	[VB 10]
7V	6.96 to 7.04V	[VB 7]
3V	2.98 to 3.02V	[VB 3]
1V	0.98 to 1.02V	[VB 1]
0.02V	0.010 to 0.030V	[VB0.02]
0.01V	0.000 to 0.020V	[VB0.01]
0V	-0.010 to 0.010V	[VB 0]
-1V	-0.98 to -1.02V	[VB -1]
-3V	-2.98 to -3.02V	[VB -3]
-7V	-6.96 to -7.04V	[VB -7]
-10V	-9.94 to -10.06V	[VB -10]
-20V	-19.70 to -20.3V	[VB -20]
-40V	-39.5 to -40.5V	[VB -40]

7.4.6 Connect the generator output to the current input and set up the following:

GENERATOR	Type	Current	[GT1]
DISPLAY	Result	I	[SO3,0]

Program the generator current output as below and measure the on the current channel. Check that the readings are within the limits stated:

GENERATOR			
NEXT	I.Ampl	*Amps	[IA *]

***Amplitude**	**DVM Reading**	
60mA	58.5mA to 61.5mA	[IA0.06]
10mA	9.65mA to 10.35mA	[IA0.01]
100µA	0mA to 200µA	[IA1E-4]
0µA	0mA to 100µA	[IA0]

7.4.7 Connect a DVM across the generator output terminals.

GENERATOR			
NEXT	I.Ampl	0Amps	[IA0]

Program the bias current as follows, and for each current check that the DVM reading is within the limits:

GENERATOR			
NEXT	I.Bias	*Amps	[IB*]

***Bias**	**DVM Reading**	
100mA	99mA to 101mA	[IB0.1]
50mA	49.5mA to 50.5mA	[IB0.05]
200µA	0µA to 400µA	[IB2E-4]
0mA	–200µA to 200µA	[IB0]
–200µA	–400µA to 0µA	[IB-2E-4]
–50mA	–50.5mA to –49.5mA	[IB-0.05]
–100mA	–101mA to –99mA	[IB-0.1]

7.4.8 Connect the generator to Channel 1 using a very short cable.

Set up the following:

SELF-TEST	Initialise		[TT1]
GENERATOR	Amplitude	1V	[VA1]
ANALYSER	Meas delay	1sec	[MS1]
	Int time	0.5sec	[IS0.5]
SWEEP	Δ log	100pts	[SF100]
NEXT	Frequency	1Hz	[FM1]
		32MHz	[FX32E6]
NEXT	Enable	log f	[SW2]
DISPLAY	Source	Ch1	[SO1,0]
	Coords	r,θ	[CV1]
DATA OUTPUT	File	all	[OP3,1]
RECYCLE			[RE]

When the sweep is over, check the file for a generator accuracy of:

Programmed output ±5% ±10mV ±1%/MHz above 1MHz

ie. upper limit = 1V +50mV +10mV +10mV/MHz above 1MHz
lower limit = 1V −50mV −10mV −10mV/MHz above 1MHz

7.4.9 Set up the following:

GENERATOR	Amplitude	0.2V	[VA0.2]
RECYCLE			[RE]

When the sweep is over, check the file for a generator accuracy of:

Programmed output ±5% ±10mV ±1%/MHz above 1MHz

ie. upper limit = 200mV +10mV +10mV +2mV/MHz above 1MHz
lower limit = 200mV −10mV −10mV −2mV/MHz above 1MHz

7.4.10 Set up the following:

SWEEP	Enable	off	[SW0]
GENERATOR	Frequency	100kHz	[FR100E3]
	Amplitude	20mV	[VA0.02]
RECYCLE			[RE]

Check displayed results are in the range 20mV ±5mV.

7.4.11 Set up the following:

SELF-TEST	Initialise	[TT1]	
GENERATOR	Amplitude	3V	[VA3]
	Bias	40.95V	[VB40.95]
ANALYSER			
NEXT	Input	AC	[DC1,1]
NEXT	Input	AC	[DC2,1]
DISPLAY	Source	V1/V2	[SO1,2]
		r,θ	[CV1]
RECYCLE			[RE]

Check for no overloads and that the reading is 1 ±0.002.

Set up the following:

DISPLAY	Source	Ch1	[SO1,0]

Check the display reads 3V ±0.15V.

7.4.12 Set the keyswitch to Supervisor mode.

Set up the following:

SELF-TEST	Initialise	[TT1]

Set the keyswitch back to normal when the 1260 displays "Initialised" and press BREAK.

7.4.13 This completes the overcheck not using ATS program 12606599.

This completes the 1260 Overcheck.

8 OVERCHECK USING ATS PROGRAM 12606599B

8.1 ATS PROGRAM

Run the checkout program following the instructions specified in 12606599B.

8.1.2 Serial Interface

Equipment: Texas Silent 700 terminal, or equivalent (eg. VDU) with baud rate set to 300 baud

8.1.2.1 Connect the terminal to the 1260 serial interface port and type in TT1 (Carriage Return). Check that the display indicates "Initialised".

8.1.2.2 Command the following using the terminal:

```
FR   300
VA   3
SO   1,0
CV   1
RE
```

Connect Channel 1 to the generator output and note that the 1260 is now taking readings at 300Hz and that the display is being updated with coordinates set to r, θ.

8.1.2.3 Command OP1,1 and observe that readings are printed on the terminal.

8.1.2.4 Command OP1,0 and remove the terminal.

8.1.3 Press:

SELF-TEST Initialise [TT1]

This completes the overcheck with ATS program 12606599B.

This completes the 1260 Overcheck using ATE Program.

8.2 CURRENT GENERATOR

If the HP9825 program is available, this should be used. Otherwise, the procedure is as follows:

8.2.1 Connect the generator to the current analyser using a very short cable.

Set up the following:

SELF-TEST	Initialise		[TT1]
GENERATOR	Amplitude	20mA	[IA0.02]
GENERATOR	Type	Current	[GT1]
SWEEP	Δ log	100pts	[SF100]
NEXT	frequency	1Hz	[FM1]
		32MHz	[FX32E6]
NEXT	enable	log f	[SW2]
DISPLAY	Source	I	[SO3,0]
	Coords	r,θ	[CI1]
RECYCLE			[RE]

When the sweep is over check the file for a generator accuracy of:

Programmed output ±5% ±200μA ±1%/MHz above 1MHz

ie. upper limit = 20mA +1mA +200μA +200μA/MHz above 1MHz
lower limit = 20mA –1mA –200μA –200μA/MHz above 1MHz

8.2.2 Set up the following

GENERATOR	Amplitude	1mA	[IA1E-3]
RECYCLE			[RE]

When the sweep is over, check the file for a generator accuracy of:

Programmed output ±5% ±200μA ±1%/MHz above 1MHz

ie. upper limit = 1mA +50μA +200μA +10μA/MHz above 1MHz
lower limit = 1mA –50μA –200μA –10μA/MHz above 1MHz

APPENDIX A

1 SINGLE POINT CALIBRATION

This procedure should be followed to repair any "bad" calibration points.

1.1 GENERAL

The 1260 is set to calibration mode by setting switch SW2 on PCB 22 to 'CALIBRATE', and initialising the instrument Ensure the eight DIL switches (SW1) on PCB 22 are all in the up position.

The frequency point to be calibrated is selected by programming the generator to the appropriate frequency. This must be one of the calibration frequencies.

The channel being calibrated is selected by the display source, and may be any of Ch1, Ch2, Ch1/Ch2 or Ch2/Ch1. The latter two are the best two as these calibrate both channels from the same measurement, achieving greater point to point accuracy.

The range being calibrated is selected by setting the appropriate analyser range.

The calibration mode must be set, using the CM command. There are six arguments:

0 - Normal, single range calibration (first pass).
1 - Magnitude only, single range calibration (first pass).
2 - Phase only, single range calibration (first pass).
3 - Normal, cross range calibration, used to achieve range-to-range crossover matching. Both channels must be being calibrated, with one on the 300mV range, and the other on either the 3V or the 30mV range The input should be either 300mV or 30mV respectively (second pass)
4 - Generator calibration.
5 - VF calibration mode.
6 - Clears the calibration data, CAREFUL.

If the calibration box has not been characterised within the last six months the procedure in Appendix B should be followed. This sets up a set of characterised values (one for each frequency and attenuation setting), which are stored as part of the auto-calibration program on micro-vax. These values compensate for any non-linearities in the frequency response of the calibration box. These characterised values are sent to the 1260 via the commands "CA 0,f" in the following calibration procedure.

1.2 A LF SINGLE POINT CALIBRATION (≤125kHz)

It is always best when calibrating a single point, to calibrate both channels on all three ranges, with a first pass calibration and a second pass calibration. A typical sequence for the 100kHz calibration point would be:

1.2.1 Connect the unterminated ends of the BNC cables to the LF outputs of the calibration box. Connect the ends of the BNC cables to INPUT V1 and INPUT V2 of the 1260. Connect the 1260 generator output to the calibration box phase lock input via an unterminated BNC cable as in Figure 2.

Select 300mV from the calibrator, and program the calibration box to 0dB attenuation.

Set switch SW2 on PCB 22 to 'CALIBRATE'. Ensure all eight DIL switches (SW1) on PCB 22 are in the up position.

Calibrator Frequency	1260 Command	Reply	Comment
-	TT1	-	Initialises 1260
100kHz	FR100E3	-	Repairing 100kHz cal point
-	SO1,2	-	Ch1/Ch2
-	VA1.5	-	Generator Amplitude = 1.5V
-	IS5	-	Integration time
-	MS5	-	Delay to allow calibrator to settle
-	CM0	-	Normal first pass
-	OU1,1	-	V1 outer floating
-	OU2,1	-	V2 outer floating
-	RA1,3	-	3V
-	RA2,3	-	3V
-	CA 0,f	-	Real value of input magnitude
-	SI	00	Calibrate

1.2.2 Select 150mV from the calibrator, and program the calibration box to 0dB attenuation.

Calibrator Frequency	1260 Command	Reply	Comment
-	RA1,2	-	300mV
-	RA2,2	-	300mV
-	CA 0,f	-	Real value of input magnitude
-	SI	00	Calibrate

1.2.3 Select 300mV from the calibrator, and program the calibration box to 20dB attenuation.

Calibrator Frequency	1260 Command	Reply	Comment
-	RA1,1	-	30mV
-	RA2,1	-	30mV
-	CA 0,f	-	Real value of input magnitude
-	SI	00	Calibrate

1.2.4 Select 300mV from the calibrator, and program the calibration box to 0dB attenuation.

Calibrator Frequency	1260 Command	Reply	Comment
-	CM3	-	Second pass calibration
-	RA1,3	-	3V
-	RA2,2	-	300mV
-	SI	00	Calibrate

1.2.5 Select 300mV from the calibrator, and program the calibration box to 20dB attenuation.

Calibrator Frequency	1260 Command	Reply	Comment
-	RA1,1	-	30mV
-	RA2,2	-	300mV
-	SI	00	Calibrate

1.2.6 Set the switch on PCB 22 to 'NORMAL'.

Calibrator Frequency	1260 Command	Reply	Comment
-	TT1	-	Initialise the 1260

1.3 A HF SINGLE POINT CALIBRATION (>125kHz)

A typical sequence for the 1MHz calibration point would be:

1.3.1 Connect the unterminated ends of the BNC cables to the HF outputs of the calibration box. Connect the ends of the BNC cables to INPUT V1 and INPUT V2 of the 1260. Note the BNC cables must have matched 50Ω terminators. Connect the 1260 generator output to the calibration box generator input via an unterminated BNC cable as in Figure 6.

Program the calibration box to 14dB attenuation.

Set switch SW2 on PCB 22 to 'CALIBRATE'. Ensure all eight DIL switches (SW1) on PCB 22 are in the up position.

Calibrator Frequency	1260 Command	Reply	Comment
-	TT1	-	Initialises 1260
1MHz	FR1E6	-	Repairing 1MHz cal point
-	SO1,2	-	Ch1/Ch2
-	VA1	-	Generator output
-	OP2,1	-	Output data to GPIB
-	MS20	-	Delay for W&G to settle after power on
-	SI	RESULT	The 1260 replies with the result of the measurement, followed by '00' or '01': a total of 6 numbers. These should be ignored
-	OP2,0	-	No data output to GPIB
-	IS5	-	Integration time
-	MS5	-	Delay to allow cal box to settle
-	CM0	-	Normal first pass
-	RA1,3	-	3V
-	RA2,3	-	3V
-	CA 0,f	-	Real value of input magnitude
-	SI	00	Calibrate

1.3.2 Program the calibration box to 20dB attenuation.

Calibrator Frequency	1260 Command	Reply	Comment
-	RA1,2	-	300mV
-	RA2,2	-	300mV
-	CA 0,f	-	Real value of input magnitude
-	SI	00	Calibrate

1.3.3 Program the calibration box to 34dB attenuation.

Calibrator Frequency	1260 Command	Reply	Comment
-	RA1,1	-	30mV
-	RA2,1	-	30mV
-	CA 0,f	-	Real value of input magnitude
-	SI	00	Calibrate

1.3.4 Program the calibration box to 14dB attenuation.

Calibrator Frequency	1260 Command	Reply	Comment
-	CM3	-	Second pass calibration
-	RA1,3	-	3 V
-	RA2,2	-	300mV
-	SI	00	Calibrate

1.3.5 Program the calibration box to 34dB attenuation.

Calibrator Frequency	1260 Command	Reply	Comment
-	RA1,1	-	30mV
-	RA2,2	-	300mV
-	SI	00	Calibrate

1.3.6 Set the switch on PCB 22 to 'NORMAL'.

Calibrator Frequency	1260 Command	Reply	Comment
-	TT1	-	Initialise the 1260

APPENDIX B

1 CHARACTERISATION OF CALIBRATION BOX AT LF (<125kHz)

The purpose of this section is to characterise the calibration box at low frequency. The procedure for doing this is to connect the AC calibrator directly to the 1260 (ie. not through the calibration box). Inputs V1 and V2 of the 1260 are then calibrated on the 300mV range. The 1260 is then switched out of calibration mode and the calibration box is inserted between the AC calibrator and the 1260. The same calibration frequency points are measured by the 1260 at three amplitude levels (300mV, 150mV and 30mV) which are the amplitudes used to calibrate the 3V, 300mV and 30mV ranges respectively. This set of results is stored in an array in the controller (micro-vax) and represent the actual voltages which are output by the calibration box at each frequency and amplitude setting on the AC calibrator. These actual calibration levels are sent to the 1260 via the command "CA 0,f" which is referred to in the Auto-calibration procedure.

The result of this procedure is an array of 3*18 characterisation values corresponding to the low frequency calibration points. These are used as the ideal values sent to the 1260 for the low frequency calibration at 300mV, 150mV and 30mV for the 3V, 300mV and the 30mV ranges respectively.

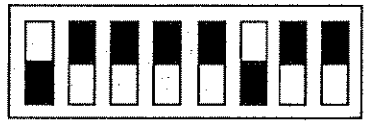
1.1 CALIBRATION OF THE 300mV RANGE

1.1.1 Connections

1. Connect GPIB to FLUKE AC calibrator,1260 and the controller.

2. Set AC calibrator to address 22.
   Set AC calibrator to remote.

3. Set 1260 to talker/listener at address 0.
   Set keyswitch to NORMAL.
   Set switch on PCB 22 to 'CALIBRATE'.
   Set DIL switch on PCB 22 to:



4. Connect 1260 generator to AC calibrator phase lock input: use an unterminated BNC cable.

5. Connect FLUKE output to 1260 Channel 1, high, input: use an unterminated BNC cable.

1.1.2 Sequence

1.1.2.1 This section initialises the 1260 for the calibration of Channel 1 on the 300mV range. Set the A.C. calibrator to 150mV.

Calibrator Frequency	1260 Command	Reply	Comment
-	TT1	-	Initialises 1260
-	-	-	Wait 2secs
-	VA3	-	Sets 3V amplitude
-	WF1	-	Selects square wave
-	RA1,2	-	Calibrating 300mV range
-	RA2,2	-	
-	IS10	-	Integration time
-	MS5	-	Delay for FLUKE to settle
-	CM0	-	Normal calibration mode
-	SO1,0	-	Channel 1 only
-	CA0.15	-	Selects ideal value to 150mV

1.1.2.2 This next section calibrates the 1260 at each of the LF calibration points. A reply of '00' from the unit indicates a successful calibration, '01' is a failure.

The following sequence of instructions should be repeated for all frequencies in Appendix G from 200Hz to 125kHz inclusive.

Calibrator Frequency	1260 Command	Reply	Comment
f Hz	FR f	-	Sets frequency
	SI	00	1260 calibrated

1.1.2.3 This section alters the 1260 for the calibration of Channel 2 on the 300mV range. Change the output of the FLUKE from Channel 1 high to Channel 2 high.

Calibrator Frequency	1260 Command	Reply	Comment
-	SO2,0	-	Channel 2 only

1.1.2.4 Repeat Section 1.1.2.2

1.2 CHARACTERISE THE BUFFER

1.2.1 Connections

Connect the 1260 to the calibration box 12606001 as in Figure 2.

1.2.2 Sequence

1.2.2.1 This section initialises the 1260 for the characterisation of the buffer by the calibrated 1260 300mV range.

Calibrator Frequency	1260 Command	Reply	Comment
	TT1	-	Initialises 1260
	-	-	Wait 2secs
	VA1.5	-	Sets 1.5V amplitude
	RA1,2	-	Calibrating 300mV range
	RA2,2	-	
	OU1,1	-	V1 outer floating
	OU2,1	-	V2 outer floating
	IS10	-	Integration time
	MS5	-	Delay for FLUKE to settle
	SO1,2	-	Channel 1/Channel 2
	OP2,1	-	Output all to GPIB
	OP3,1	-	Output all to file
	CV1	-	Coordinates, R,θ
	FC	-	Clear the file

1.2.2.2 This next section measures the buffer output at each of the LF calibration points at about 300mV: the 3V calibration value. The 1260 replies after each measurement with the frequency, magnitude, phase, error code and limit check result: five numbers. These are used to synchronise the controller. Set the calibration box to 0dB: 300mV from the AC calibrator.

1.2.2.3 Repeat Section 1.1.2.2.

1.2.2.4 This section reads the measured values of the buffer output for Channel 1 and stores them in the characterisation array.

Calibrator Frequency	1260 Command	Reply	Comment
	SO1,0	-	Channel 1
	FO	-	List the file

Read in 18 measurement results, storing magnitude as characterisation values for 300mV.

Calibrator Frequency	1260 Command	Reply	Comment
	SO2,0	-	Channel 2
	FO	-	List the file

Read in 18 measurements results, averaging magnitude with value already stored for Channel 1, and store as ideal value for 300mV.

1.2.2.5 This section resets the 1260 to characterise the buffer at 150mV.

Calibrator Frequency	1260 Command	Reply	Comment
	SO1,2	-	Channel 1/Channel 2
	FC	-	Clear the file

1.2.2.6 This next section measures the buffer output at each of the LF calibration points at about 150mV: the 300mV calibration value. The 1260 replies after each measurement with the frequency, magnitude, phase, error code and limit check result: five numbers. These are used to synchronise the controller. Set the calibration box to 0dB: 150mV from the AC calibrator.

1.2.2.7 Repeat Section 1.1.2.2.

1.2.2.8 This section reads the measured values of the buffer output for Channel 1 and stores them in the characterisation array.

Calibrator Frequency	1260 Command	Reply	Comment
	SO1,0	-	Channel 1
	FO	-	List the file

Read in 18 measurement results, storing magnitude as characterisation values for 150mV.

Calibrator Frequency	1260 Command	Reply	Comment
	SO2,0	-	Channel 2
	FO	-	List the file

Read in 18 measurements results, averaging magnitude with value already stored for Channel 1, and store as ideal value for 150mV.

1.2.2.9 This section resets the 1260 to characterise the buffer at 30mV.

Calibrator Frequency	1260 Command	Reply	Comment
	SO1,2	-	Channel 1/Channel 2
	FC	-	Clear the file

Insert between the buffer and the power splitter an accurate 20dB attenuator, marked so that it is used whenever these characterisation constants are used. Set the calibration box to 20dB: 300mV from the AC calibrator.

1.2.2.10 This next section measures the buffer output at each of the LF calibration points at about 30mV: the 30mV calibration value. The 1260 replies after each measurement with the frequency, magnitude, phase, error code and limit check result: five numbers. These are used to synchronise the controller.

1.2.2.11 Repeat Section 1.1.2.2.

1.2.2.12 This section reads the measured values of the buffer output for Channel 1 and stores them in the characterisation array.

Calibrator Frequency	1260 Command	Reply	Comment
	SO1,0	-	Channel 1
	FO	-	List the file

Read in 18 measurement results, storing magnitude as characterisation values for 30mV.

Calibrator Frequency	1260 Command	Reply	Comment
	SO2,0	-	Channel 2
	FO	-	List the file

Read in 18 measurements results, averaging magnitude with value already stored for Channel 1, and store as ideal value for 30mV.

1.2.3 **Tidy**

Set DIL switch on PCB 22 to:

Calibrator Frequency	1260 Command	Reply	Comment
	TT1	-	Initialise the 1260

1.3 CHARACTERISATION OF HF CALIBRATION BOX

The purpose of this section is to characterise the HF calibration box to ensure a smooth transition between the LF and HF region. It requires that the LF region be already calibrated.

1.4 SEQUENCE

1.4.1 Connect the unterminated ends of the BNC cables to the HF outputs of the calibration box. Connect the ends of the BNC cables to INPUT V1 and INPUT V2 of the 1260. Note the BNC cables must have matched 50Ω terminators. Connect the 1260 generator output to the calibration box AGC input via an unterminated BNC cable.

This section initialises the 1260 for the characterisation of the calibration box at 125kHz. Set switch SW2 on PCB 22 to 'NORMAL'. Ensure all eight DIL switches (SW1) on PCB 22 are in the up position.

Calibrator Frequency	1260 Command	Reply	Comment
-	TT1	-	Initialises 1260
-	-	-	Wait 2secs
-	VA1	-	Sets 1V amplitude
-	FR125E3	-	Sets 125kHz
-	RA1,2	-	Characterise on 300mV
-	RA2,2	-	range
-	IS10	-	Integration time
-	MS5	-	Delay for cal box
-	SO1,2	-	Channel 1/Channel 2
-	OP2,1	-	Output all to GPIB
-	CV1	-	Coordinates, R,θ

1.4.2 To allow the calibration box and the W & G to settle, this dummy measurement is taken.

Calibrator Frequency	1260 Command	Reply	Comment
-	SI	-	Measure
-	-	-	Read result

Five numbers are outputted by the 1260, frequency, magnitude, phase, an error code and a limit check result: these can be discarded.

1.4.3 Program the calibration box to attenuate the signal by 14dB. This measurement returns the ideal value for calibration of the 3V range at about 300mV.

Calibrator Frequency	1260 Command	Reply	Comment
-	SO1,0	-	Channel 1
-	SI	-	Measure
-	-	-	Read result

Five numbers are outputted by the 1260, frequency, magnitude, phase, an error code and a limit check result: save the magnitude.

Calibrator Frequency	1260 Command	Reply	Comment
-	SO2,0	-	Channel 2
-	DO	-	Command result output
-	-	-	Read result

Five numbers are outputted by the 1260, frequency, magnitude, phase, an error code and a limit check result: take the average of Channel 1 and Channel 2 magnitudes and use this as the characterisation value "a".

1.4.4 Program the calibration box to attenuate the signal by 20dB. This measurement returns the ideal value for calibration of the 300mV range at about 150mV.

Calibrator Frequency	1260 Command	Reply	Comment
-	SO1,0	-	Channel 1
-	SI	-	Measure
-	-	-	Read result

Five numbers are outputted by the 1260, frequency, magnitude, phase, an error code and a limit check result: save the magnitude.

Calibrator Frequency	1260 Command	Reply	Comment
-	SO2,0	-	Channel 2
-	DO	-	Command result output
-	-	-	Read result

Five numbers are outputted by the 1260, frequency, magnitude, phase, an error code and a limit check result: take the average of Channel 1 and Channel 2 magnitudes and use this as the characterisation value "b".

1.4.5 Program the calibration box to attenuate the signal by 34dB. This measurement returns the ideal value for calibration of the 30mV range at about 30mV.

Calibrator Frequency	1260 Command	Reply	Comment
-	SO1,0	-	Channel 1
-	SI	-	Measure
-	-	-	Read result

Five numbers are outputted by the 1260, frequency, magnitude, phase, an error code and a limit check result: save the magnitude.

Calibrator Frequency	**1260 Command**	**Reply**	**Comment**
-	SO2,0	-	Channel 2
-	DO	-	Command result output
-	-	-	Read result

Five numbers are outputted by the 1260, frequency, magnitude, phase, an error code and a limit check result: take the average of Channel 1 and Channel 2 magnitudes and use this as the characterisation value "c".

APPENDIX C

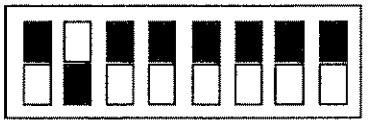
1 SWITCHES ON PCB 22

NOTE: All switches must be in the up position for normal operation of the 1260. When they are in the down position various diagnostic aids are enabled.

1.1 CALIBRATION CONSTANTS

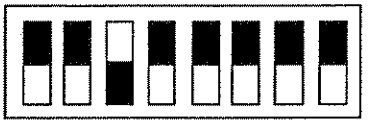
UP - Analyser calibration constants are enabled
DOWN - Analyser calibration constants are disabled

1.2 SQUARE WAVE OUTPUT



UP - Disable square wave output (<65kHz)
DOWN - Enable square wave output (<65kHz)

1.3 FORCE WAVE BEAT CHECK



UP - Enable "beat" check software
DOWN - Disable "beat" check software

1.4 HETERODYNE SCHEME

UP - Select new heterodyne scheme
DOWN - Select old heterodyne scheme

1.5 GENERATOR CALIBRATION

UP - Enable generator calibration constants
DOWN - Disable generator calibration constants

1.6 60µA AND 6µA RANGES

UP - Disable the 60µA and 6µA ranges above 10MHz
DOWN - Enable the 60µA and 6µA ranges above 10MHz

All other switches are not used.

APPENDIX D

CALIBRATOR CHARACTERISATION

This requires a calibrated and partially overchecked 1260 (ie. past Sections 7.3.4 to 7.3.12).

Connect the 1260 to the calibration box and the calibrator as in Figure 10.

Set up the following:

SELF-TEST	Initialise		[TT1]
GENERATOR	Amplitude	2V	[VA2]
ANALYSER			
NEXT	V1 Outer	Floating	[OU1,1]
NEXT	V2 Outer	Floating	[OU2,1]
DISPLAY	Coords	r,θ	[CV1]
RECYCLE			[RE]

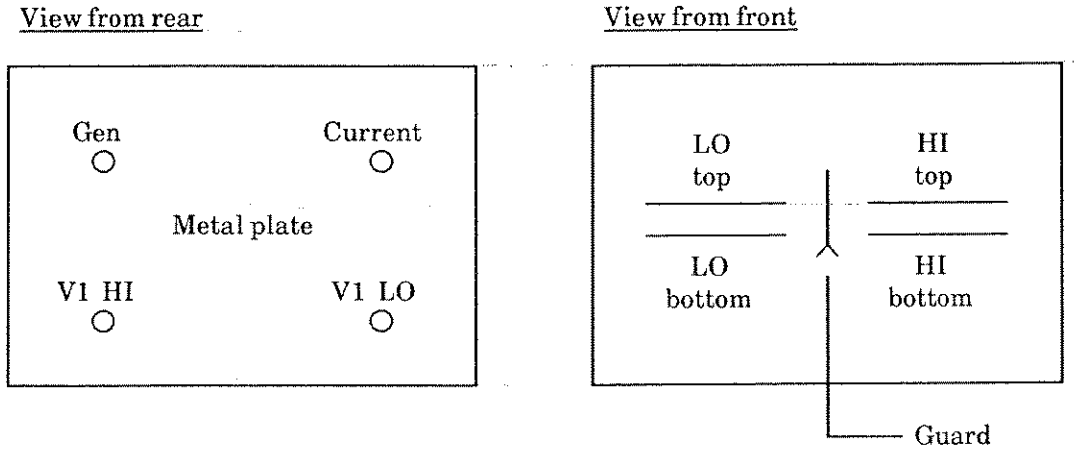
For each of the frequencies and amplitudes in Tables 3.5.5, 3.5.6, 5.5.8, 5.5.9, and 7.3.2 note the transfer function of the calibration box. Then for each of the nominal values in the above tables, the calibrator should be set to the nominal value multiplied by the transfer function for that frequency and amplitude.

ie. For the unit under test to read 2V @ 300Hz the calibrator should be set to:

2V (nominal value) x K (the transfer function for 2V, 300Hz)

APPENDIX E

12601 COMPONENT TEST MODULE



Insert a non-conductive spacer between the top and bottom metal jaws on both HI and LO.

Use a DMM set to Ωs in the following tests.

Check that the resistance measured between the metal plate on the rear and each of the BNC outers is $<1.5\Omega$.

Check that the resistance measured between the metal plate on the rear and the guard is $<1.5\Omega$.

Check that the resistance measured from point-to-point is as indicated in the table below.

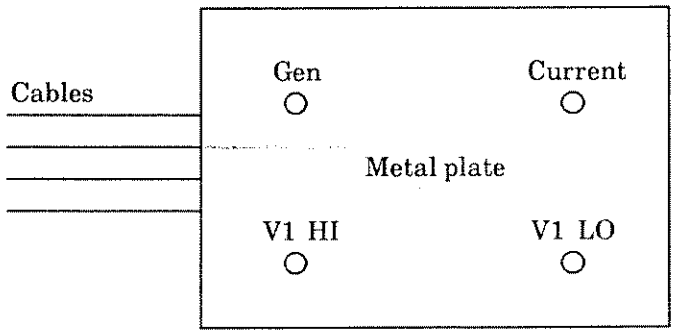
	HI		LO	
	Top	Bottom	Top	Bottom
Gen inner	$<1.5\Omega$	o/c	o/c	o/c
Current inner	o/c	o/c	$<1.5\Omega$	o/c
V1 HI inner	o/c	$<1.5\Omega$	o/c	o/c
V1 LO inner	o/c	o/c	o/c	$<1.5\Omega$

o/c = open circuit

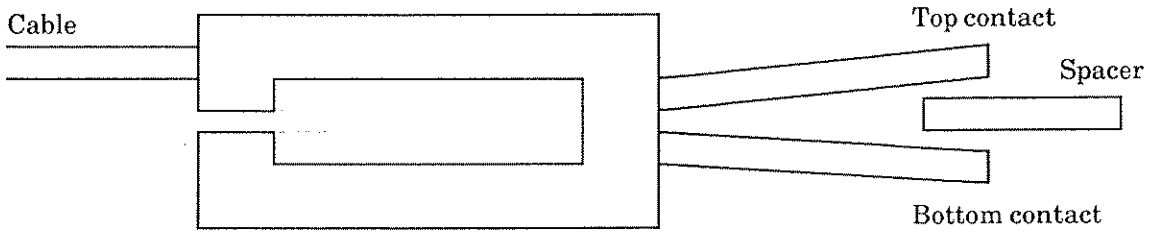
APPENDIX F

12603 IN-CIRCUIT COMPONENT TEST MODULE

View from rear



Test clip



Insert non-conductive spacers between the jaws on the two large test clips.

Use a DMM set to ohms in the following tests.

Check that the metal plate is not connected to any of the BNC outers.

Check that the resistance measured from point-to-point is as indicated in the table below.

	HI Cable (red sleeve)		LO Cable (no sleeve)	
	Top	Bottom	Top	Bottom
Gen inner	<1.5Ω	o/c	o/c	o/c
Current inner	o/c	o/c	<1.5Ω	o/c
V1 HI inner	o/c	<1.5Ω	o/c	o/c
V1 LO inner	o/c	o/c	o/c	<1.5Ω

o/c = open circuit

Check that the BNC outers are connected as indicated in this table.

	HI Cable (red sleeve)	LO Cable (no sleeve)
	Guard Clip	Guard Clip
Gen outer	<1.5Ω	o/c
Current outer	o/c	<1.5Ω
V1 HI outer	<1.5Ω	o/c
V1 LO outer	o/c	<1.5Ω

o/c = open circuit

APPENDIX G

ANALYSER CALIBRATION POINTS

(Hz)

10	299.99999	300	655.35999
655.36	2E3	5E3	6.5535999E3
6.5536E3	7E3	10E3	17E3
22E3	32.767999E3	32.768E3	48E3
55E3	65.535999E3	65.536E3	100E3
125E3	145E3	200E3	300E3
430E3	570E3	600E3	800E3
1E6	2E6	4E6	6E6
7E6	8E6	9E6	10E6
11E6	14E6	16E6	19E6
20E6	22.5E6	26E6	29.5E6
32E6			

APPENDIX H

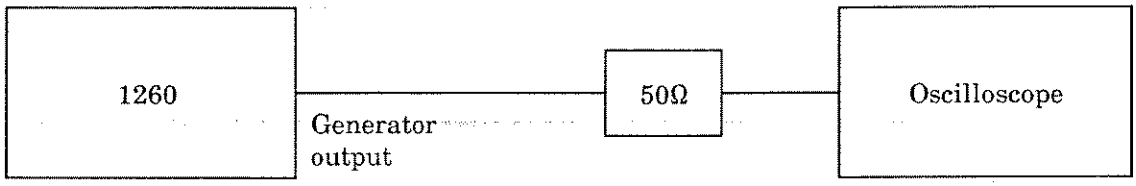
GENERATOR CALIBRATION POINTS

This is the list of generator calibration points:

300Hz
65.535999kHz
65.536kHz
800kHz
2MHz
4MHz
7MHz
20MHz
26MHz
32MHz

1260 Calibration and Overcheck Diagrams

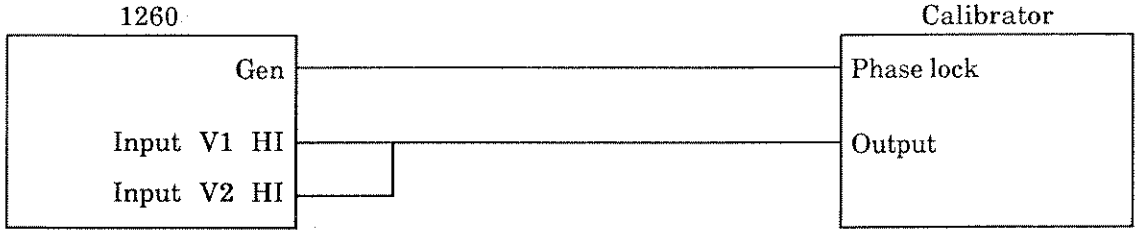
Figure 1 *Generator Flatness Test*



NOTE: If the oscilloscope has a 50Ω input, this may be used instead of the 50Ω terminator.

Figure 2 *LF Analyser Set Up Test*

b) Without calibration box



b) With calibration box

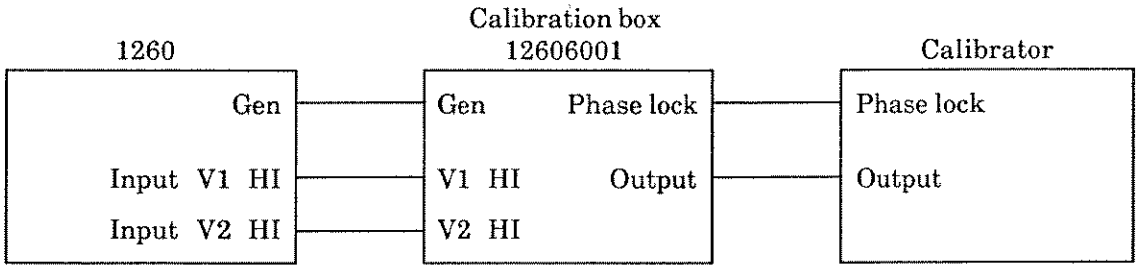
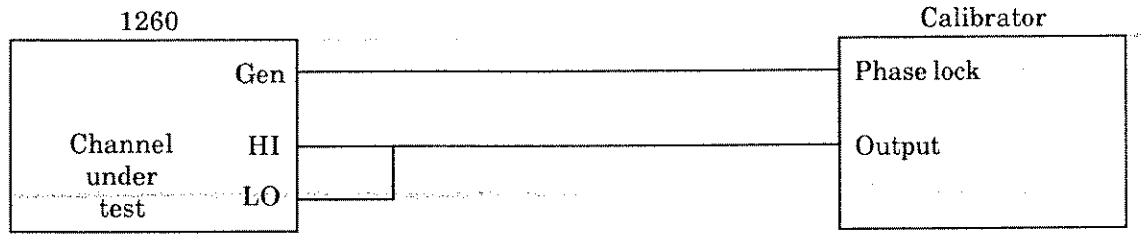


Figure 3 *Analyser LF Common Mode*

a) Without calibration box



b) With calibration box

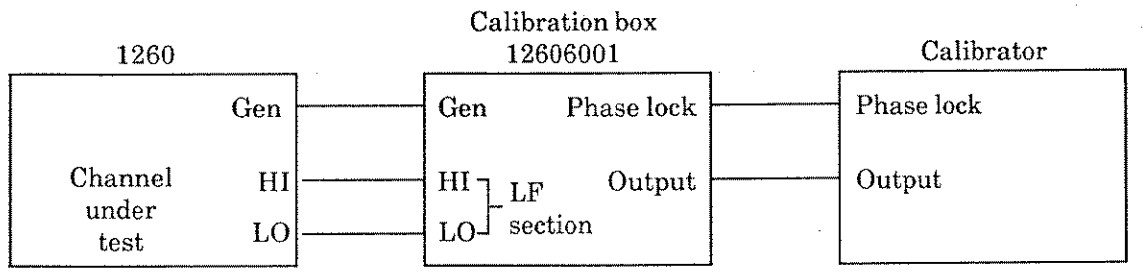


Figure 4 *Cable Connections*

PCB 14 SK501 to Gen Output
PCB 31 SK101 to Input I

PCB 10 (Channel 1) SK401 to Input V1 HI
PCB 10 (Channel 1) SK402 to Input V1 LO
PCB 10 (Channel 2) SK401 to Input V2 HI
PCB 10 (Channel 2) SK402 to Input V2 LO

PCB 10 (Current) SK401 to PCB 31 SK102
PCB 10 (Current) SK402 no connection

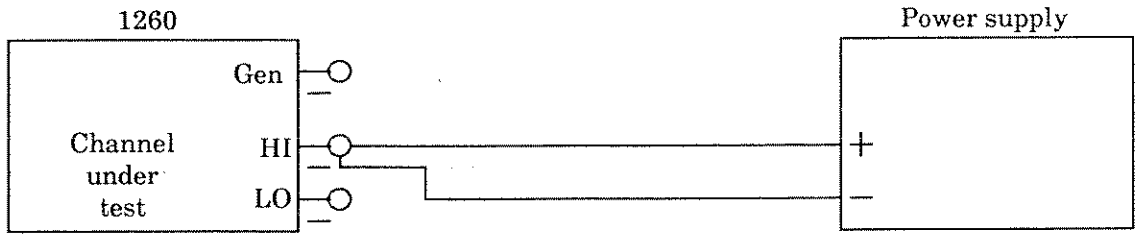
PCB 16 PLD to PCB 10 (CH1) PL401 (heterodyne cables)
PCB 16 PLE to PCB 10 (CH2) PL401
PCB 16 PLF to PCB 10 (Current) PL401

PCB 16 PLG to PCB 14 SK701 (HF signal)
PCB 16 PLH to PCB 15 SK202 (LF reference)
PCB 15 SK201 to PCB 14 SK201 (LF output)

***NOTE: The connections on issue B & C copper are transposed.

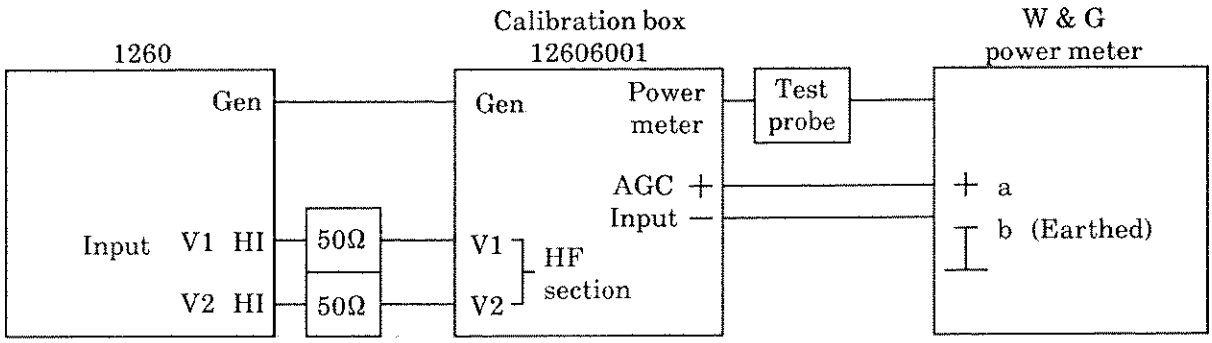
PCB 15 SK401 to PCB 31 SK103 (power supply)
PCB 15 SK202 to PCB 31 SK104 (relay drive)
PCB 15 SK1 to KILL GEN INPUT
PCB 22 CON1 to KEY SWITCH

Figure 5 *DC Overload Test*



NOTE: HI to shield
The high BNC inner is the input, and the high BNC outer is the shield.

Figure 6 *HF Analyser Accuracy Set Up Test*



The terminators on the 1260 inputs are matched to the calibration box and must always be connected according to the identification labels.

The W & G power meter must be turned on with the test probe connected to its own ouput for at least one hour before it is used for calibration. With the W & G connected in this way, the displayed reading should be set to 0dBm on the ±0.2dBm range, by adjusting the set calibration pot with the impedance set to 50Ω 0dBm. IMPORTANT: The W & G must be left in this state when it is not in use.

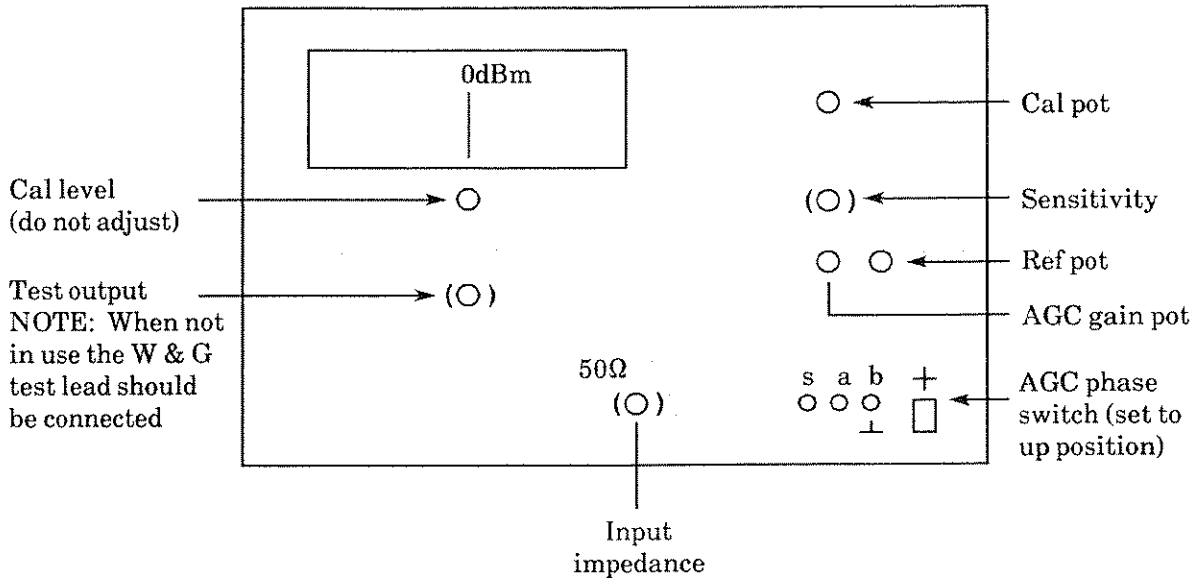
Set the gain of the W & G fully anti-clockwise then move a quarter of a turn back clockwise (ie. just off the minimum gain).

To use the W & G, connect the test probe to the calibration box as above and set the 1260 amplitude to 0.7V at 100kHz, and use the reference knob on the W & G to set the W & G to read 0dBm on the ±0.2dBm range (this will usually take place with the knob at the clockwise end of its travel). The needle will tend to overshoot and may take 20-30secs to settle. If it does not move off the end stop increase the gain of the W & G by another quarter of a turn and try the reference pot again.

NOTE: If the gain is set too high the AGC loop will oscillate causing amplitude modulation on the calibration box output.

No attempt should be made to calibrate or overcheck unless the W & G is pointing at 0dBm ±0.1dBm and the pointer is not oscillating.

W & G Power Meter Front Panel Layout



NOTE: The cal pot should only be set up with the test head connected to the W & G output.

Figure 7 *Analyser Input Protection Test*

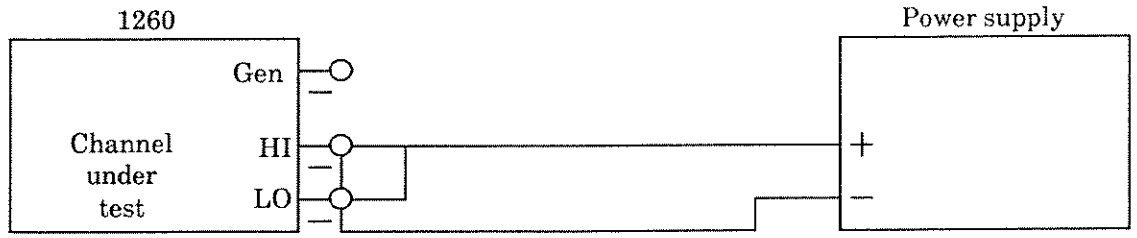


Figure 8 *Generator Common Mode Overload Test*

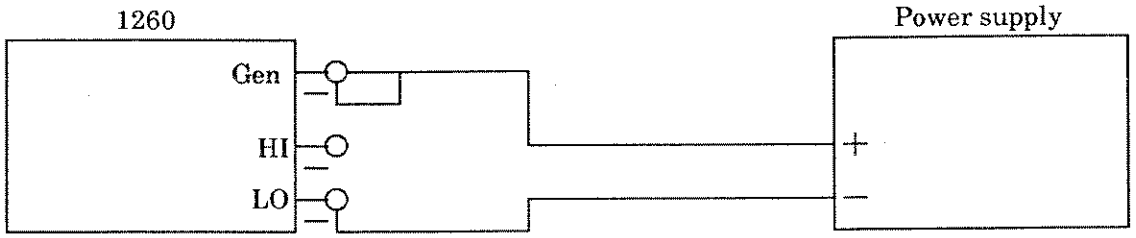
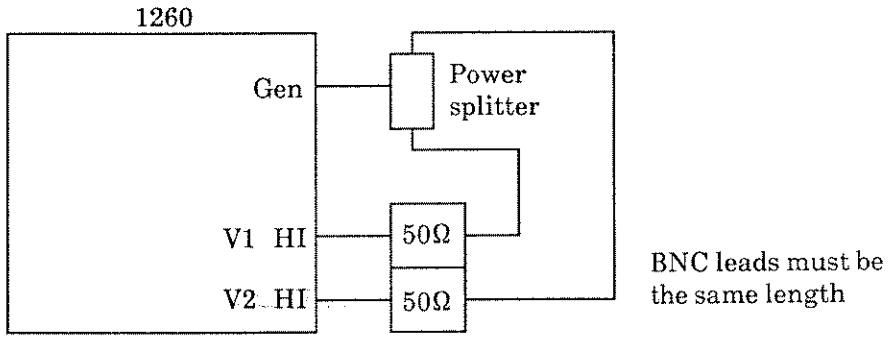


Figure 9 *Analyser Range-to-Range using a Power Splitter*



50Ω terminators matched to the power splitter better than 0.1%.

Figure 10 *Calibrator Characterisation*