BASLER A620f

USER'S MANUAL

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BASLER
VISION TECHNOLOGIES

For customers in the U.S.A.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

You are cautioned that any changes or modifications not expressly approved in this manual could void your authority to operate this equipment.

The shielded interface cable recommended in this manual must be used with this equipment in order to comply with the limits for a computing device pursuant to Subpart J of Part 15 of FCC Rules.

For customers in Canada

This apparatus complies with the Class A limits for radio noise emissions set out in Radio Interference Regulations.

Pour utilisateurs au Canada

Cet appareil est conforme aux normes Classe A pour bruits radioélectriques, spécifiées dans le Règlement sur le brouillage radioélectrique.

Life Support Applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Basler customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Basler for any damages resulting from such improper use or sale.

Warranty Note

Do not open the housing of the camera. The warranty becomes void if the housing is opened.

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Table of Contents

4 Configuring the Camera

5 Image Data Formats and Structures

1 Introduction

1.1 Documentation Applicability

This User's Manual applies to cameras with a firmware ID number of 32.

Cameras with a lower or a higher firmware ID number may have fewer features or have more features than described in this manual. Features on cameras with a lower or a higher firmware ID number may not operate exactly as described in this manual.

An easy way to see the firmware ID number for an **A620f** camera is by using the BCAM Viewer included with the Basler BCAM 1394 driver. To see the firmware ID number:

1. Attach your camera to a computer equipped with the BCAM 1394 driver.
2. Double click the BCAM Viewer icon on your desktop or click Start ⇒ All Programs ⇒ Basler Vision Technologies ⇒ BCAM 1394 ⇒ BCAM Viewer. The viewer program window will open.
3. Find the camera name in the Bus Viewer panel that appears on the left side of the window and click on the camera name.
4. Click on the  icon in the tool bar at the top of the window.
5. A properties window similar to the one shown in Figure 1-1 will open. Use the figure as a guide to find the firmware ID number.

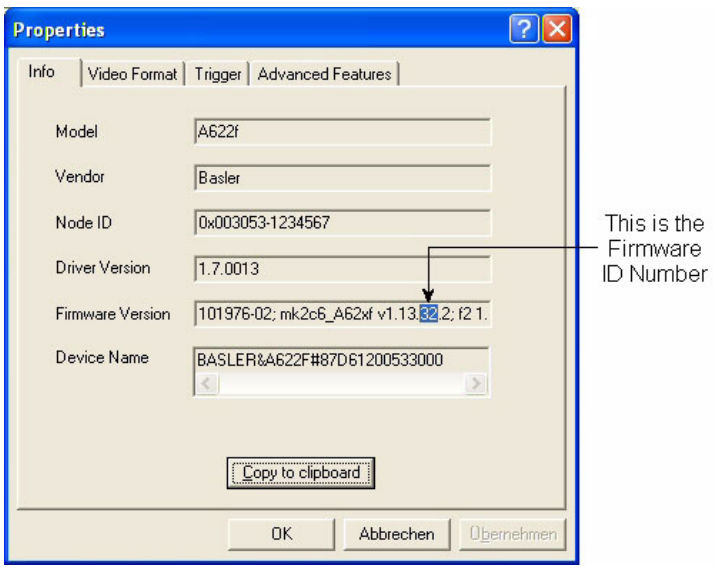


Figure 1-1: BCAM Properties Window

	You can also access the firmware ID number by using the Extended Version Information smart feature. See Section 6.7.7 for more information.

1.2 Camera Models

Currently only one model of the camera is available and this model is designated as the **A622f**. The **A622f** is only available in monochrome. Throughout this User's Manual, the camera will be referred to as the **A620f** (this is the camera family designation).

1.3 Performance Specifications

Specification	A622f
Sensor Type	IBIS5A-1300 - 2/3 inch, CMOS, Global Shutter
Pixels	1280 (H) x 1024 (V)
Pixel Size	6.7 µm (H) x 6.7 µm (V)
Max. Frame Rate (at full resolution)	25.0 fps in 8 bit output modes 12.5 fps in 16 bit output modes (The exposure time setting significantly affects the frame rate. See Section 3.3.2 for details.)
Video Output Formats	Mono 8 (8 bits/pixel) Mono 16 (16 bits/pixel - 10 bits are effective) Pseudo YUV 4:2:2 (16 bits/pix avg.)* * See Section 3.12.1 for more details.
Gain and Brightness	Programmable via the IEEE 1394 bus
Exposure Time Control	Programmable via the IEEE 1394 bus
Synchronization	External via External Trigger signal
Power Requirements	+8.0 to +36.0 VDC (+12 VDC nominal), < 1% ripple 2.3 W max @ 12 VDC (typical) supplied via 1394 cable
I/O Electrical Characteristics	Inputs: opto-isolated, 5 VDC nominal, 10 mA nominal Outputs: opto-isolated, 2 to 48 VDC maximum forward voltage, 100 mA max collector current See Sections 2.5.1 and 2.5.2 for more details.
Max. Cable Lengths	1394: 4.5 meters I/O: 10 meters See Section 2.2 for more details.
Lens Adapter	C-mount
Housing Size (L x W x H)	Not including lens adapter: 59.0 mm x 44 mm x 29 mm Including C-mount adapter: 67.3 mm x 44 mm x 29 mm
Weight	< 100 g (typical)
Conformity	CE, FCC

Table 1-1: **A620f** Performance Specifications

1.4 Spectral Response

The spectral response for the **A620f** monochrome camera is shown in Figure 1-2.

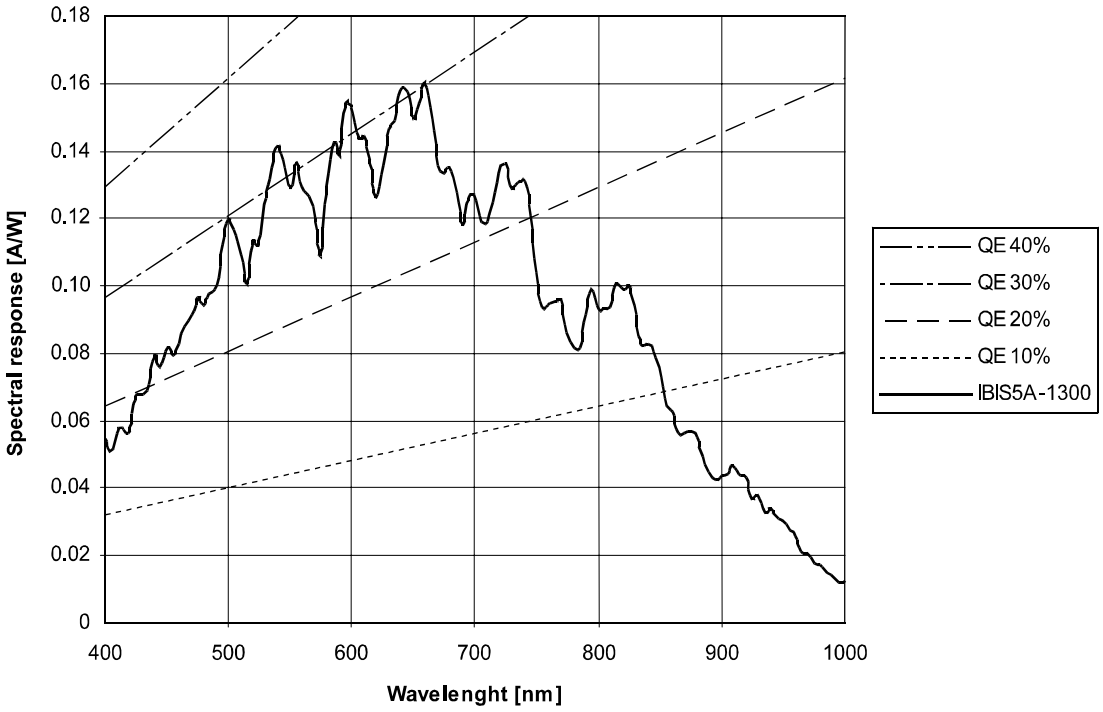


Figure 1-2: **A620f** Spectral Response

	The spectral response curve excludes lens characteristics and light source characteristics.

1.5 Environmental Requirements

1.5.1 Temperature and Humidity

Housing temperature during operation:	0° C … + 50° C (+ 32° F … + 122° F)
Humidity during operation:	20% … 80%, relative, non-condensing

1.5.2 Ventilation

Allow sufficient air circulation around the camera to prevent internal heat build-up in your system and to keep the housing temperature below 50° C. Additional cooling devices such as fans or heat sinks are not normally required but should be provided if necessary.

1.6 Precautions

To ensure that your warranty remains in force:

Read the manual

Read the manual carefully before using the camera!

Keep foreign matter outside of the camera

Do not open the casing. Touching internal components may damage them.

Be careful not to allow liquid, flammable, or metallic material inside the camera housing. If operated with any foreign matter inside, the camera may fail or cause a fire.

Electromagnetic Fields

Do not operate the camera in the vicinity of strong electromagnetic fields. Avoid electrostatic charging.

Transporting

Transport the camera in its original packaging only. Do not discard the packaging.

Cleaning

Avoid cleaning the surface of the CMOS sensor if possible. If you must clean it, use a soft, lint free cloth dampened with a small quantity of high quality window cleaner. Because electrostatic discharge can damage the CMOS sensor, you must use a cloth that will not generate static during cleaning (cotton is a good choice).

To clean the surface of the camera housing, use a soft, dry cloth. To remove severe stains, use a soft cloth dampened with a small quantity of neutral detergent, then wipe dry.

Do not use volatile solvents such as benzine and thinners; they can damage the surface finish.

2 Camera Interface

2.1 Connections

2.1.1 General Description

The **A620f** is interfaced to external circuitry via an IEEE 1394 socket and a 10 pin RJ-45 jack located on the back of the housing. Figure 2-1 shows the location of the two connectors.

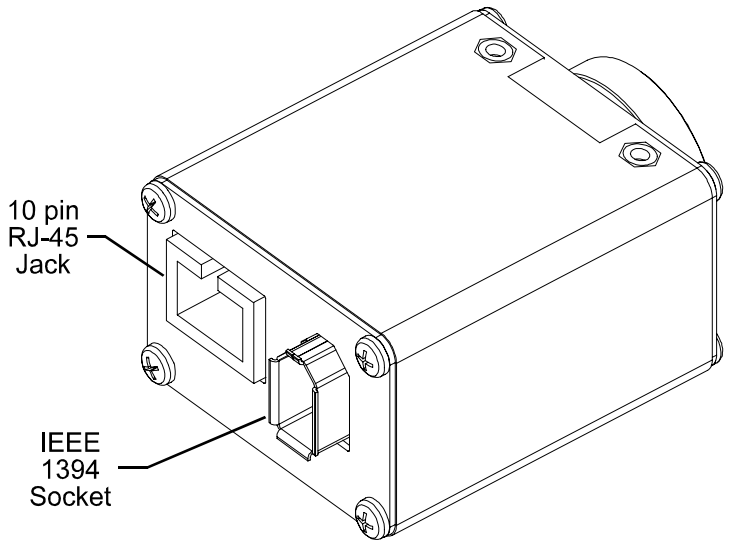


Figure 2-1: Camera Connectors

2.1.2 Pin Assignments

The IEEE 1394 socket is used to supply power to the camera and to interface video data and control signals. The pin assignments for the socket are shown in Table 2-1.

Pin	Signal
1	Power Input (+8.0 to +36.0 VDC)
2	DC Gnd
3	TPB -
4	TPB +
5	TPA -
6	TPA +

Table 2-1: Pin Assignments for the IEEE 1394 Socket

The RJ-45 jack is used to access the four physical input ports and four physical output ports on the camera. The pin assignments for the jack are shown in Table 2-2.

Pin	Designation
1	Output Port 3 -
2	Output Port 2 -
3	Output Port 1 -
4	Output Port 0 -
5	Input Port 0 +
6	In Gnd Comm
7	Out VCC Comm
8	Input Port 2 +
9	Input Port 1 +
10	Input Port 3 +

Table 2-2: Pin Assignments for the RJ-45 jack

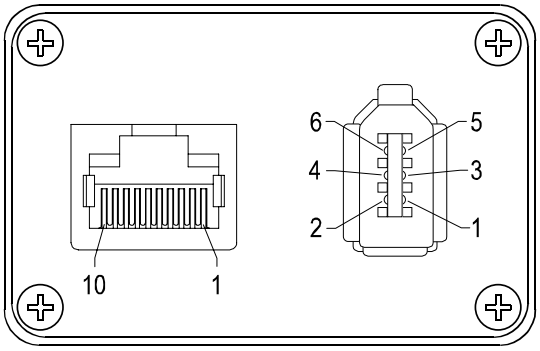


Figure 2-2: **A620f** Pin Numbering

The camera housing is connected to the cable shields and coupled to signal ground through an RC network (see Figure 2-3 for more details).

2.1.3 Connector Types

The 6-pin connector on the camera is a standard IEEE-1394 socket.

The 10-pin connector on the camera is an RJ-45 jack.

Caution!

The plug that you insert into the camera's RJ-45 jack must have 10 pins. Inserting a smaller plug, such as one with 8 pins or 4 pins, can damage the pins in the RJ-45 jack on the camera.

2.2 Cables

The maximum length specified in the IEEE 1394 standard for the cable used between the camera and the adapter in your PC or between the camera and a 1394 hub is 4.5 meters. Shielded IEEE 1394 cables must be used.

Basler has successfully tested a 10 meter IEEE 1394 cable and we offer this cable for sale. Since the 10 meter cable length is outside of the 1394 standard, we cannot guarantee that it will work properly in all applications and environments. If you want to use the 10 meter cable, we suggest that you order a cable and test it in your environment.

The maximum length of the I/O cable is at least 10 meters. The cable must be shielded and must be constructed with twisted pair wire. Close proximity to strong magnetic fields should be avoided.

2.3 Camera Power

Power must be supplied to the camera via the IEEE 1394 cable. Nominal input voltage is +12.0 VDC, however, the camera will operate properly on any input voltage from +8.0 VDC to +36.0 VDC as specified in the IEEE 1394 standard. Maximum power consumption for the **A620f** is 2.3 W at 12 VDC. Ripple must be less than 1%.

Caution!

Use only standard IEEE 1394 connectors.

The polarity of the input power to the camera must be as shown in Table 2-1. **Do not** reverse the input power polarity. Reversing the polarity will damage the camera.

2.4 IEEE 1394 Device Information

The **A620f** uses an IEEE 1394a - 2000 compliant physical layer device to transmit pixel data. Detailed spec sheets for devices of this type are available at the Texas Instruments web site (www.ti.com).

2.5 Input and Output Ports

2.5.1 Input Ports

A620f cameras are equipped with four physical input ports designated as Input Port 0, Input Port 1, Input Port 2, and Input Port 3. The input ports are accessed via the 10 pin RJ-45 jack on the back of the camera. See Table 2-2 and Figure 2-2 for input port pin assignments and pin numbering.

As shown in the schematic in Figure 2-3, each input port is opto-isolated. The nominal input voltage for the LED in the opto-coupler is 5.0 VDC (± 1.0). The input current for the LED is 5 to 15 mA with 10 mA recommended.

For each input port, a current between 5 and 15 mA means a logical one. A current of less than 0.1 mA means a logical zero.

By default, Input Port 0 is assigned to receive an external trigger (ExTrig) signal that can be used to control the start of exposure. For more information about the ExTrig signal and for information on assigning the ExTrig signal to a different input port, see Section 3.3.5.

As stated above, the nominal input voltage for the LED on each input is +5 VDC. If a 560 Ohm resistor is added to the positive line for an input, the input voltage can be 12 VDC. If a 1.2 or 1.5 kOhm resistor is added to the positive line for an input, the input voltage can be 24 VDC.

2.5.2 Output Ports

A620f cameras are equipped with four physical output ports designated as Output Port 0, Output Port 1, Output Port 2, and Output Port 3. The output ports are accessed via the 10 pin RJ-45 jack on the back of the camera. See Table 2-2 and Figure 2-2 for output port pin assignments and pin numbering.

As shown in the schematic in Figure 2-3, each output port is opto-isolated. The minimum forward voltage is 2 VDC, the maximum forward voltage is 48 VDC, the maximum reverse voltage is 6 VDC, and the maximum collector current is 100 mA.

A conducting transistor means a logical one and a non-conducting transistor means a logical zero.

By default, Output Port 0 is assigned to transmit an integration enabled (IntEn) signal that indicates when exposure is taking place. For more information about the IntEn signal, see Section 3.5.

By default, Output Port 1 is assigned to transmit a trigger ready (TrigRdy) signal that goes high to indicate the earliest point at which exposure start for the next frame can be triggered. For more information about the TrigRdy signal, see Section 3.4.

The assignment of camera output signals to physical output ports can be changed by the user. See Section 6.7.10 for more information about configuring output ports.

By default, output ports 0, 1, and 2 are set to a low state after power on. Output port 3 is initially set to low but will go high approximately 100 to 300 ms after power on. Output port 3 will remain high for approximately 750 ms and will then reset to low.

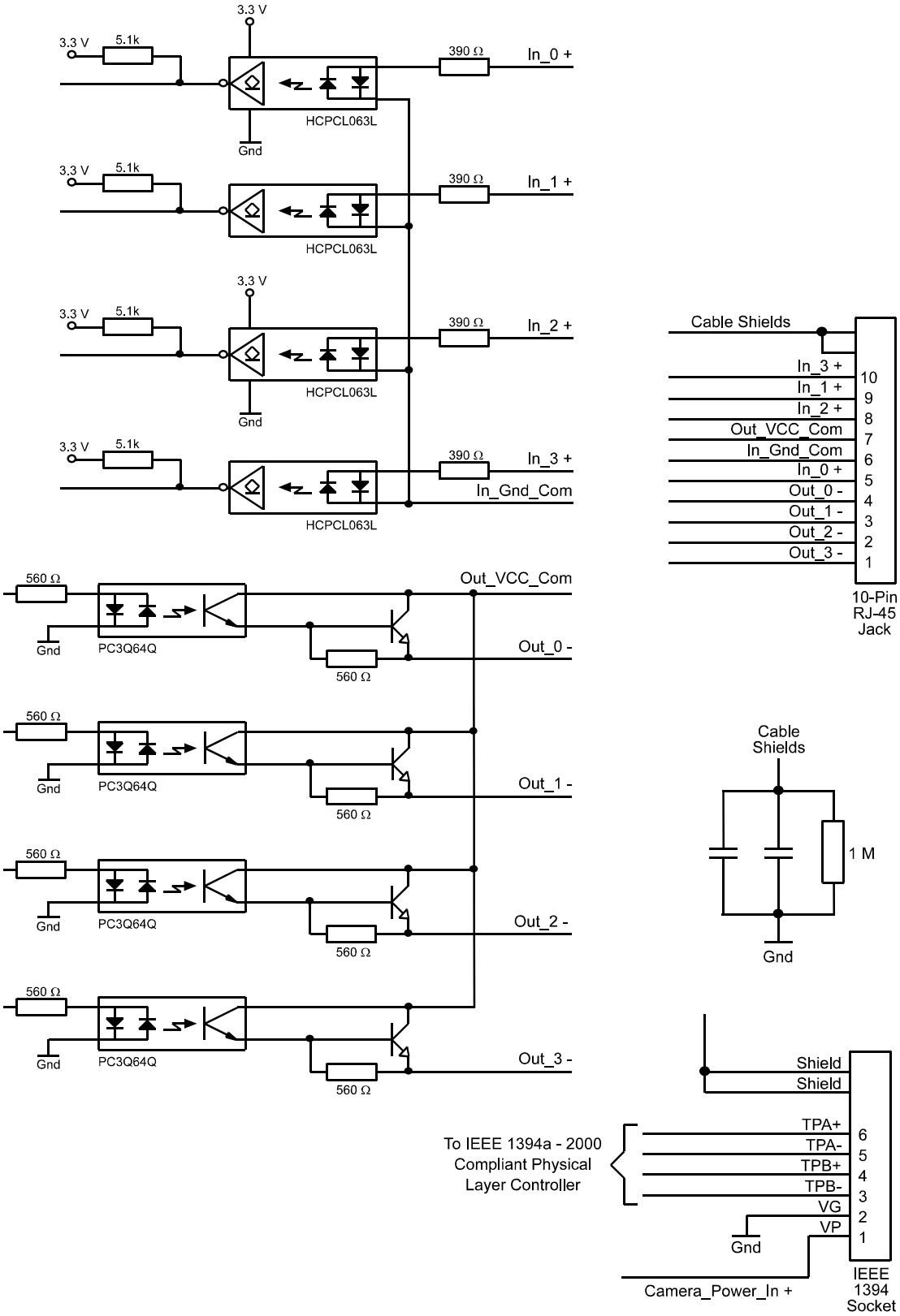


Figure 2-3: I/O Schematic

2.5.3 Typical Input Circuits

Figure 2-4 shows a typical 5 VDC circuit you can use to input a signal into the camera. In Figure 2-4, the signal is applied to input port 1.

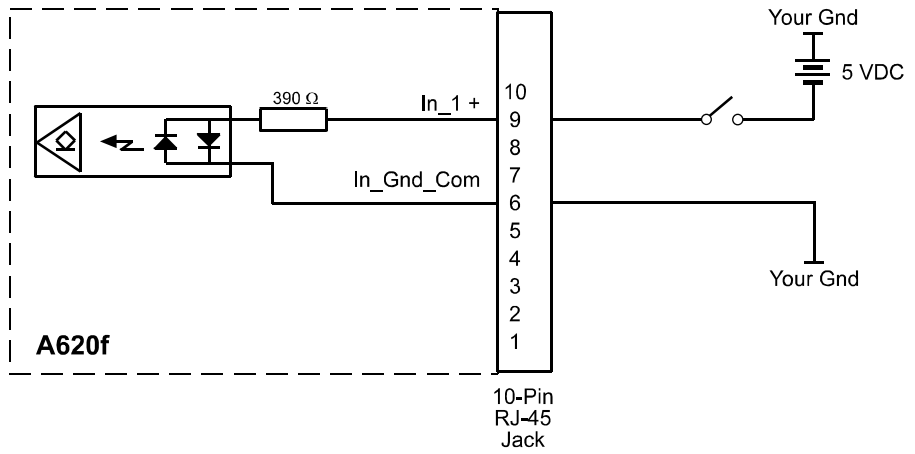


Figure 2-4: Typical 5 VDC Input Circuit

Figure 2-5 shows a typical 24 VDC circuit you can use to input a signal into the camera. Notice that an external 1.2 k resistor has been added to the circuit. This will result in approximately 15 mA being applied to the input. In Figure 2-5, the signal is applied to input port 3.

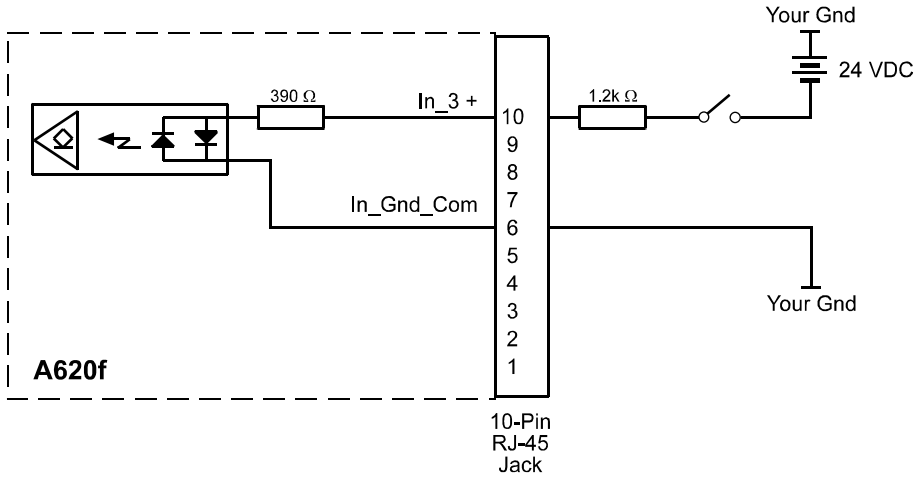


Figure 2-5: Typical 24 VDC Input Circuit

2.5.4 Typical Output Circuits

Figure 2-6 shows a typical circuit you can use to monitor an output port with a voltage signal. The circuit in Figure 2-6 is monitoring camera output port 1.

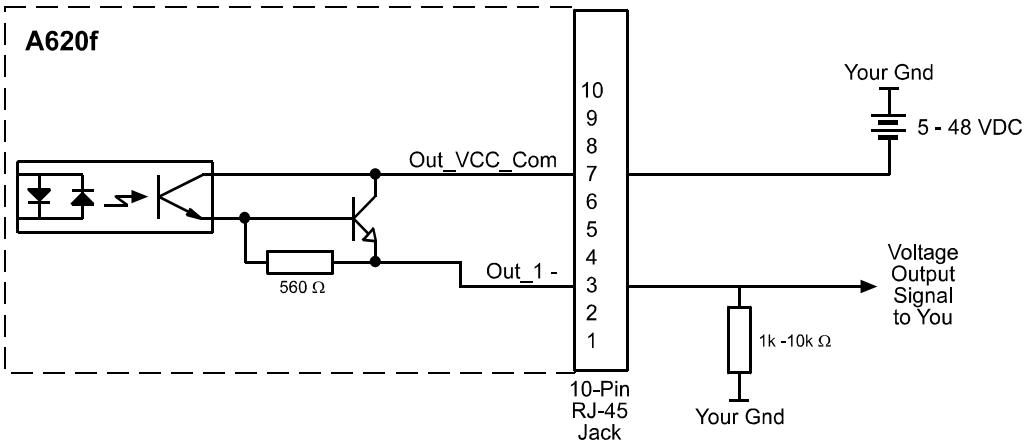


Figure 2-6: Typical Voltage Output Circuit

Figure 2-7 shows a typical circuit you can use to monitor an output port with a LED or an optocoupler. In this example, the voltage for the external circuit is 24 VDC. Current in the circuit is limited to approximately 10 mA by an external 2.2k resistor. The circuit in Figure 2-7 is monitoring camera output port 2.

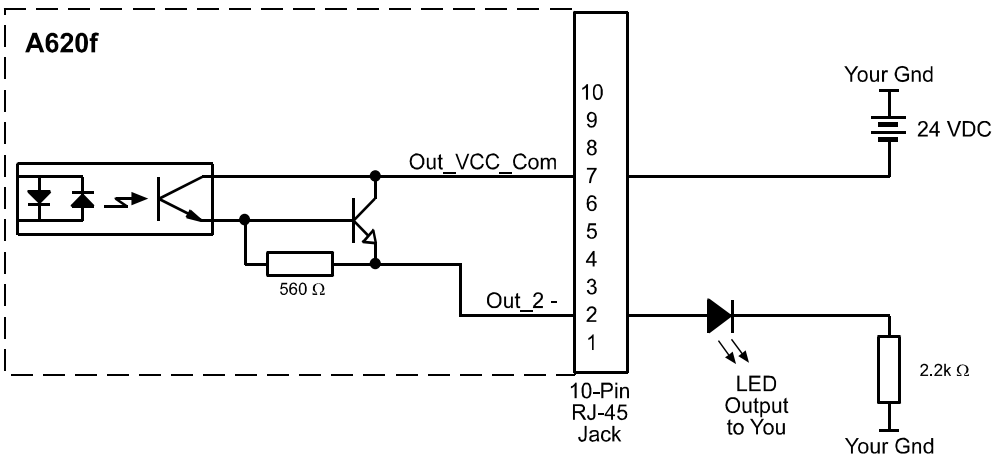


Figure 2-7: Typical LED Output Signal

3 Basic Operation and Standard Features

3.1 Functional Description

3.1.1 Overview

A620f area scan cameras employ a CMOS-sensor chip which provides features such as a global shutter and electronic exposure time control.

Normally, exposure time and charge readout are controlled by values transmitted to the camera's control registers via the IEEE 1394 interface. Control registers are available to set exposure time and frame rate. There are also control registers available to set the camera for single frame capture or continuous frame capture.

Exposure start can also be controlled via an externally generated trigger (ExTrig) signal. The ExTrig signal facilitates periodic or non-periodic start of exposure. When exposure start is controlled by a rising ExTrig signal and the camera is set for the programmable exposure mode, exposure begins when the trigger signal goes high and continues for a pre-programmed period of time. Accumulated charges are read out when the programmed exposure time ends.

The pixels can be connected to a bus and there is one bus per vertical column. At readout, the pixels are addressed row-wise by closing a switch that connects each pixel in the addressed row to the column buses. As the charges from the pixels leave the column buses, they are converted to voltages and pass through the column amplifiers.

From the column amplifiers, the voltages enter an analog multiplexer that acts along with the X-Addressing circuitry as a shift register. As the voltages are clocked out of the shift register, they pass through an output amplifier and they are digitized by a 12 bit analog-to-digital converter (ADC). The digitized video data next moves through a processing block in the FPGA that uses the 12 bit data to perform image correction functions and to perform the gain and offset functions. The output from the processing block is pixel data at 10 bit depth. After processing, the data is directed into an image buffer.

The data leaves the image buffer and passes back through the FPGA to a 1394 link layer controller where it is assembled into data packets that comply with version 1.31 of the "1394 - based Digital Camera Specification" (DCAM) issued by the 1394 Trade Association. The packets are passed to a 1394 physical layer controller which transmits them isochronously to a 1394 interface board in the host PC. The physical and link layer controllers also handle transmission and receipt of asynchronous data such as programming commands.

The image buffer between the sensor and the link layer controller allows data to be read out of the sensor at a rate that is independent of the of the data transmission rate between the camera and the host computer. This ensures that the data transmission rate has no influence on image quality.

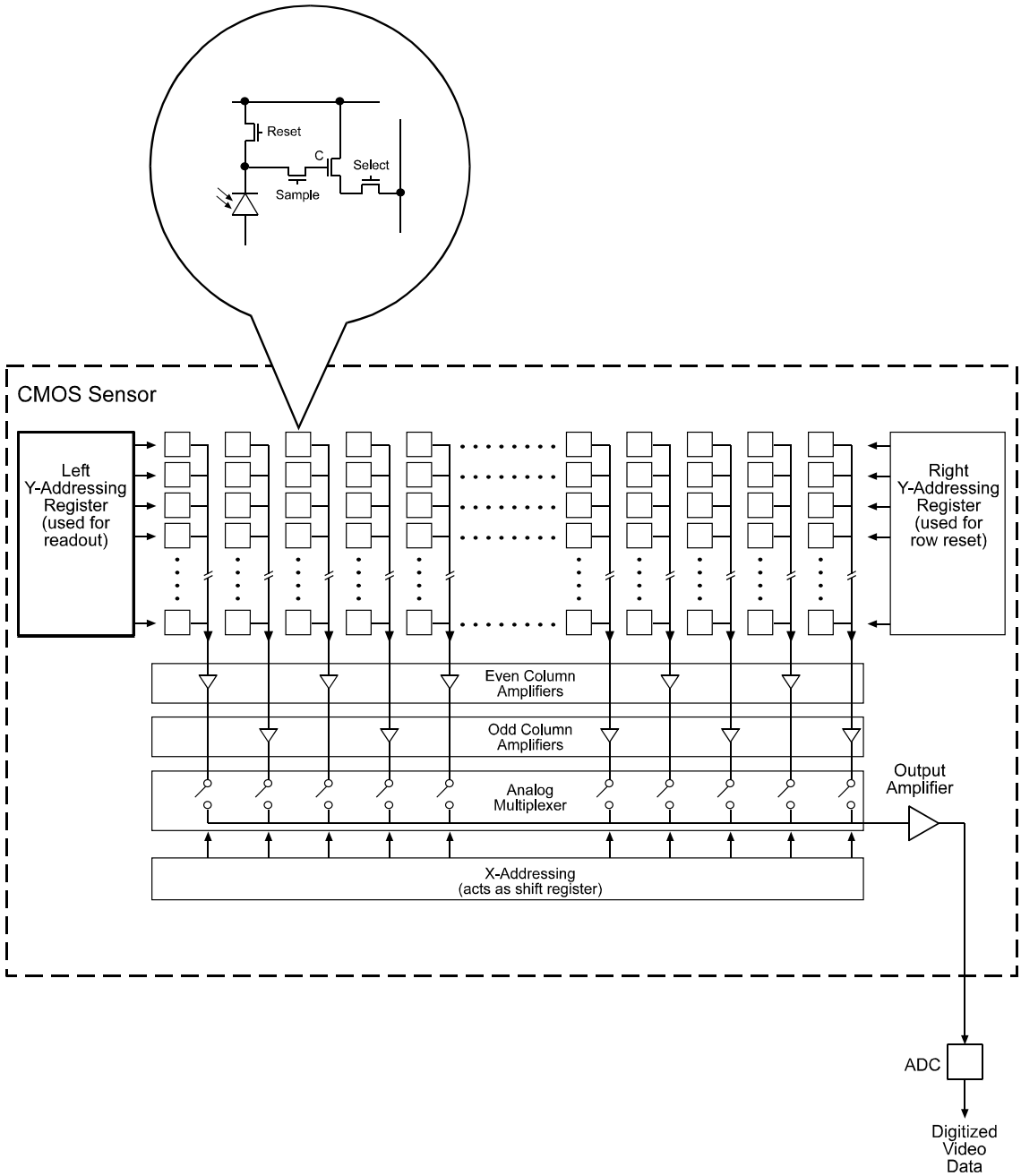


Figure 3-1: **A620f** Sensor Architecture

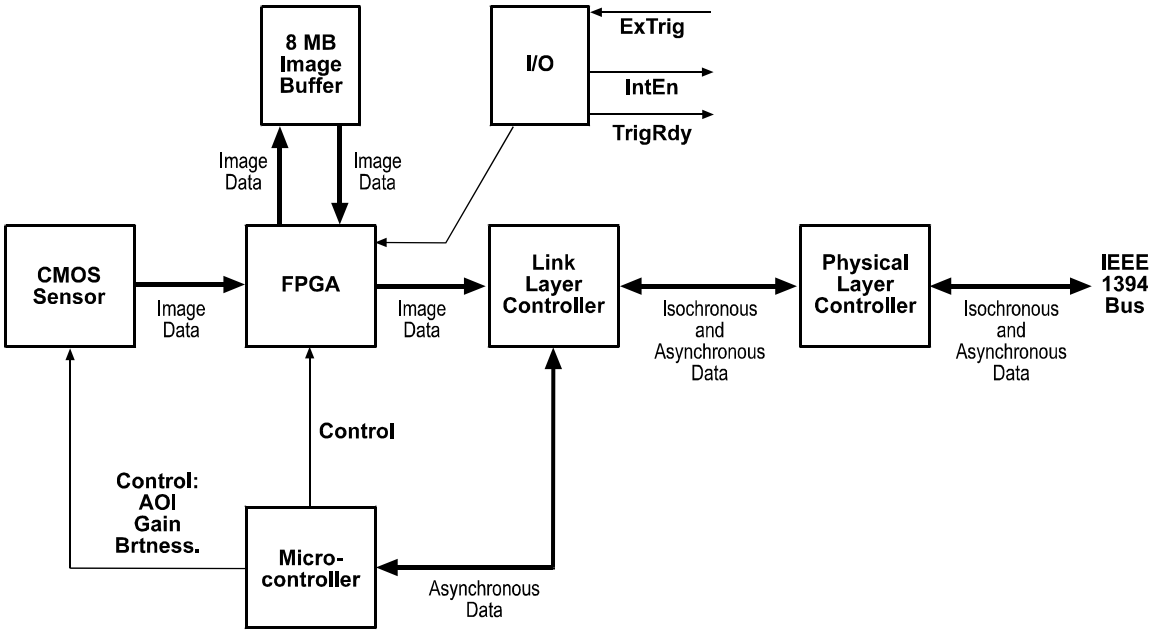


Figure 3-2: Block Diagram

3.2 Camera Initialization Period

Whenever the camera is powered on or is reset, it needs six seconds to complete its internal initialization process. The camera cannot capture images during the initialization period. If image capture is triggered during initialization, the camera will store the last received capture request. When initialization is complete, the last received capture request will be performed. Any other capture requests received during initialization will be ignored.

When initialization is complete, the camera will begin normal operation.

3.3 Exposure Control

3.3.1 Setting the Exposure Time

Exposure time is determined by a combination of two values. The first is the setting in the Value field of the Shutter control register (see page 4-24). The second is the Shutter Time Base. Exposure time is determined by the product of these two values:

Exposure Time = (Shutter Value Setting) x (Shutter Time Base)

The shutter time base is fixed at 20 µs. Exposure time is adjusted by changing the setting in the Value field of the Shutter control register. The shutter value setting can range from 1 to 4095 (0x001 to 0xFFF). So if the Value field of the Shutter register is set to 100 (0x064), for example, the exposure time will be 100 x 20 µs or 2000 µs.

If you are operating the camera at a standard frame rate, you can determine the maximum shutter setting for that frame rate by reading the Max Value field of the Shutter Inquiry register (see page 4-16).

3.3.2 Effect of the Exposure Time Setting on the Camera's Maximum Frame Rate

The capture of a single frame (image) is a two part process. First, the pixels in the camera's sensor must be exposed to light for some period of time. Second, after exposure is complete, the charges accumulated by the pixels during the exposure must be read out of the sensor and into the camera's image buffer. With the sensor used in **A620f** cameras, the exposure of a new frame can not begin until the readout of the previously captured frame is complete. This situation is illustrated in Figure 3-3.

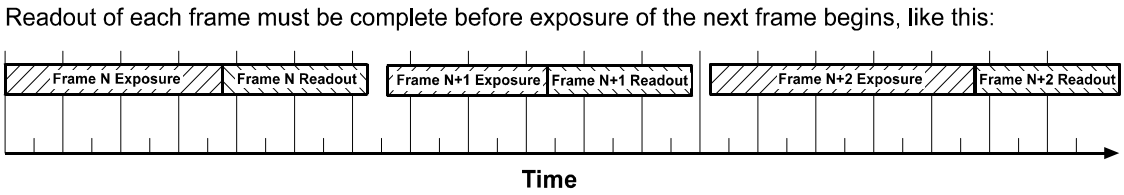


Figure 3-3: Frame Capture Sequence

A result of this sensor characteristic is that the exposure time setting will have a very direct effect on the camera's maximum allowed frame rate. At longer exposure times, the camera's maximum frame rate will be lower.

The formula on page 3-5 lets you calculate the camera's maximum frame rate at full resolution for a given exposure time. This is useful if you know the exposure time you want to use and you want to determine the maximum frame rate you can achieve with that exposure time.

The formula on page 3-6 lets you calculate the camera's maximum exposure time for a given frame rate at full resolution. This is useful if you know the frame rate and you want to determine the maximum exposure time you can use at that frame rate.

A camera signal called "trigger ready" indicates when sensor readout is complete and it is safe to begin the next exposure. See Section 3.4 for more information on the trigger ready signal.

Calculating the Maximum Frame Rate for a Given Exposure Time

To determine the camera's maximum allowed frame rate at a given exposure time, use the formula below. This formula applies when the camera is set for full resolution.

$$\text{Max frames/s} = \frac{1}{\text{Exposure time in seconds} + 0.0376}$$

When the camera is operating at full resolution and 8 bit output, the 1394 bus capacity limits the maximum frame rate to 25 fps. If the formula returns a value higher than 25, the maximum will frame rate will be limited to 25.

When the camera is operating at full resolution and 16 bit output, the 1394 bus capacity limits the maximum frame rate to 12.5 fps. If the formula returns a value higher than 12.5, the maximum will frame rate will be limited to 12.5.

Example 1

Assume that the camera is set for full resolution, 8 bit output and an exposure time of 6.50 ms.

$$\text{Max frames/s} = \frac{1}{0.0065 + 0.0376}$$

Max frame/s = 22.7

The maximum allowed frame rate in this case is 22.7 frames per second.

Example 2

Assume that the camera is set for full resolution, 8 bit output and an exposure time of 1.10 ms.

$$\text{Max frames/s} = \frac{1}{0.0011 + 0.0376}$$

Max frames/s = 25.9

The formula returns a value of 25.9 fps, but the 1394 bus capacity limits the maximum frame rate at full resolution with 8 bit output to 25 fps. **So in this case, the maximum allowed frame rate is 25 fps.**

The information on this page is valid when you are operating the camera at full resolution. If you use the camera's AOI feature to reduce the resolution, you can operate the camera at higher frame rates. See Section 3.7 for more information about the AOI feature.

Calculating the Maximum Exposure Time for a Given Frame Rate

To determine the camera's maximum allowed exposure time at a given frame rate, use the formula below. This formula applies when the camera is set for full resolution.

$$\text{Max exposure time in seconds} = \frac{1}{\text{Frame rate}} - 0.0376$$

Example

Assume that you will be operating the camera at 22.0 frames per second and that you want to know the maximum exposure time you can use at this frame rate.

$$\text{Max exposure time in seconds} = \frac{1}{22.0} - 0.0376$$

$$\text{Max exposure time in seconds} = 0.0079$$

The maximum allowed exposure time is this case is 7.9 ms.

The information on this page is valid when you are operating the camera at full resolution. If you use the camera's AOI feature to reduce the resolution, this calculation will be different. See Section 3.7 for more information about the AOI feature.

3.3.3 Controlling Exposure Start with “Shot” Commands via the 1394 Interface

Exposure start can be controlled by sending “shot” commands directly to the camera via the 1394 bus. In this case, a software trigger or an external trigger (ExTrig) signal is not used. When exposure start is controlled with shot commands via the 1394 bus, two modes of operation are available: one-shot and continuous-shot.

One-Shot Operation

In one-shot operation, the camera exposes and transmits a single image. Exposure begins after the One Shot field of the One Shot/Multi Shot control register is set to 1 (see page 4-21). Exposure time is determined by the shutter settings described in Section 3.3.1.

The One Shot field is self cleared after transmission of the image data.

Continuous-Shot Operation

In continuous-shot operation, the camera continuously exposes and transmits images. The exposure of the first image begins after the Continuous Shot field of the ISO En/Continuous Shot control register is set to 1 (see page 4-21). The exposure time for each image is determined by the shutter settings described in Section 3.3.1. The start of exposure on the second and subsequent images is automatically controlled by the camera.

If the camera is operating in video Format 0, Format 1 or Format 2, the rate at which images will be captured and transmitted is determined by the setting in the Frame Rate field of the Current Video Frame Rate/Revision control register (see page 4-19).

If the camera is operating in video Format 7, the rate at which images will be captured and transmitted is determined by the setting in the Bytes per Packet field of the Bytes per Packet control register (see Section 3.12.2 and page 4-33).

Image exposure and transmission stop after the Continuous Shot field of the ISO En/Continuous Shot control register is set to 0.

These explanations of exposure start are included to give the user a basic insight into the interactions of the camera’s registers. Typically, IEEE 1394 cameras are used with a driver which includes an interface that allows the user to parameterize and operate the camera without directly setting registers. The Basler BCAM 1394 Camera Driver, for example, has both a simple Windows® interface and a programmer’s API for parameterizing and operating the camera.

3.3.4 Controlling Exposure Start with a Software Trigger

Exposure start can be controlled by sending a software trigger command to the camera via the 1394 bus. The Trigger Mode control register (see page 4-26) is used to enable the ability to start image exposure with a software trigger. The Software Trigger control register (see page 4-22) is used to set the software trigger.

If you are triggering the camera with a software trigger, only the programmable exposure mode is available. In programmable mode, exposure starts when the Trigger field of the Software Trigger control register is set to 1. The length of the exposure is determined by the shutter settings described in Section 3.3.1. The Trigger field will self clear shortly after exposure start. Figure 3-4 illustrates programmable exposure with a software trigger.

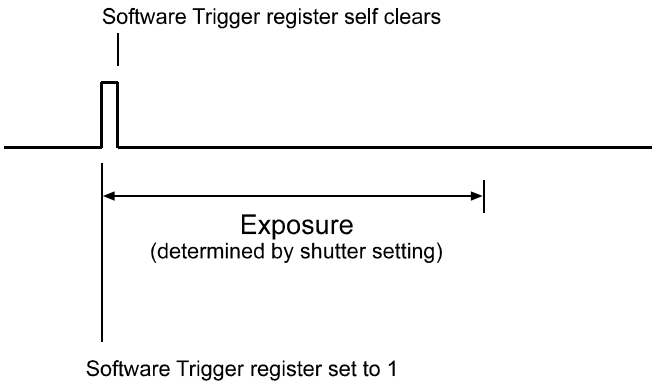


Figure 3-4: Programmable Exposure with a Software Trigger

Enabling the Software Trigger Feature

To enable the software trigger feature:

- Set the On/Off field of the Trigger Mode control register to 1 to enable triggering.
- Set the Trigger Source field of the Trigger Mode control register to 7 to select software triggering.
- Set the Trigger Mode field of the Trigger Mode control register to 0 to select the programmable exposure mode.

Using the Software Trigger Feature

To use the software trigger feature, the camera must be set for continuous-shot operation. If more precise control of exposure start time is desired, you should also monitor the Trigger Ready signal and you must base the timing of the software trigger on the state of the Trigger Ready signal. (See Section 3.4 for more information on the Trigger Ready signal.)

The following descriptions assume that you are using a software trigger to start exposure and that you are monitoring the Trigger Ready signal.

Software Trigger / Continuous-Shot Operation

In Software Trigger/Continuous-shot operation, a “Continuous Shot Command” is used to prepare the camera to capture multiple images. With this method of operation, exposure will begin when the Trigger field of the Software Trigger control register is set to 1. To use this operating method, follow this sequence:

1. Use the shutter settings described in Section 3.3.1 to set your desired exposure time.
2. Set the Continuous Shot field of the ISO En/Continuous Shot control register to 1 (see page 4-21).
3. Check the state of the TrigRdy signal:
   a) If TrigRdy is high, you can set the Trigger field of the Software Trigger register to 1 when desired.
   b) If TrigRdy is low, wait until TrigRdy goes high and then set the Trigger field to 1 when desired.
4. When the Trigger field is set to 1, exposure will begin. (Note that the Trigger field self-clears shortly after exposure begins.)
5. Exposure will continue for the length of time specified in step 1.
6. At the end of the specified exposure time, readout and transmission of the captured image will take place.
7. Repeat steps 3 and 4 each time that you want to begin exposure and capture an image.
8. To disable continuous-shot operation, set the Continuous Shot field in the ISO En/ Continuous Shot control register to 0.

The Software Trigger register and the Trigger Source field of the Trigger Mode control register are defined in version 1.31 of the IIDC specification.

Because the software trigger feature is so new, the Basler BCAM 1394 Driver does not yet include a method call to access this feature. As a work-around, you can use the techniques described in the tutorial for the Basler Smart Features Framework Software to directly read from or write to the Software Trigger and Trigger Mode registers. The Smart Features Framework Software is available on the Basler web site. To download the software go to:

http://www.baslerweb.com/popups/popup_en_1825.php

Why Use the Software Trigger?

At first glance, using the software trigger feature to start image exposure appears to be equivalent to just issuing a one-shot command as described in Section 3.3.3. The difference is in the way the camera reacts to each method. With a one-shot command, there will be some delay between the One Shot field of the One Shot/Multi Shot control register being set to 1 and the actual start of exposure time. This delay is required so that the camera can be properly set up to react to the receipt of the one-shot command. With the software trigger method, there is no delay between the Trigger field being set to 1 and the start of exposure. Exposure begins immediately when the field value is set. So the advantage of the software trigger feature is that it gives you more precise control of exposure start.

3.3.5 Controlling Exposure Start with an ExTrig Signal

The external trigger (ExTrig) input signal can be used to control the start of exposure. A rising edge or a falling edge of the signal can be used to trigger exposure start. The Trigger Mode control register (see page 4-26) is used to enable ExTrig exposure start control, to select rising or falling edge triggering, and to assign a physical input port to receive the ExTrig signal.

The ExTrig signal can be periodic or non-periodic. When the camera is operating under control of an ExTrig signal, the period of the ExTrig signal determines the camera's frame rate:

$$\frac{1}{\text{ExTrig period in seconds}} = \text{Frames/s}$$

For example, if you are operating a camera with an ExTrig signal period of 60 ms:

$$\frac{1}{0.060\ \text{s}} = 16.7\ \text{Frames/s}$$

So in this case, the frame rate is 16.7 frames/s.

The minimum high time for a rising edge trigger (or low time for a falling edge trigger) is 1 µs.

Exposure Modes

If you are triggering the camera with an ExTrig signal, two exposure modes are available, programmable mode and level controlled mode.

Programmable Exposure Mode

When programmable mode is selected, the length of the exposure is determined by the shutter settings described in Section 3.3.1. If the camera is set for rising edge triggering, exposure starts when the ExTrig signal rises. If the camera is set for falling edge triggering, exposure starts when the ExTrig signal falls. Figure 3-5 illustrates programmable exposure with the camera set for rising edge triggering.

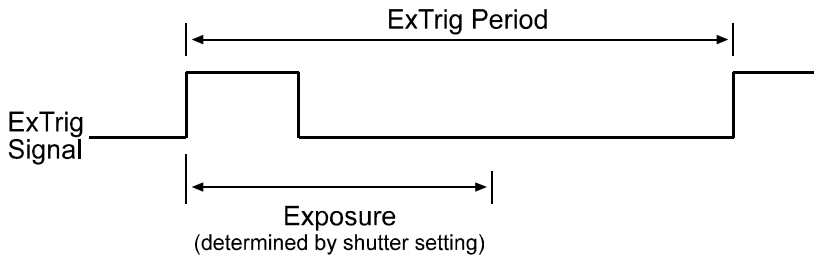


Figure 3-5: Programmable Exposure with Rising Edge Triggering

Level Controlled Exposure Mode

When level controlled mode is selected, the length of the exposure will be determined by the ExTrig signal alone. If the camera is set for rising edge triggering, exposure begins when the ExTrig signal rises and continues until the ExTrig signal falls. If the camera is set for falling edge triggering, exposure begins when the ExTrig signal falls and continues until the ExTrig signal rises. Figure 3-6 illustrates level controlled exposure with the camera set for rising edge triggering.

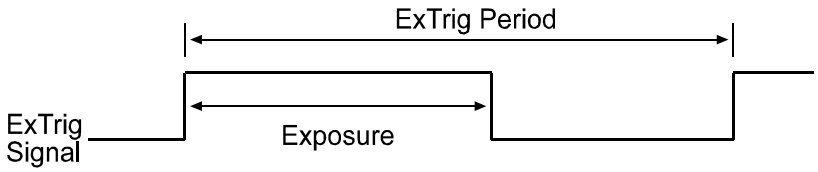


Figure 3-6: Level Controlled Exposure with Rising Edge Triggering

Enabling the External Trigger Feature

To enable the external trigger feature:

- Set the On/Off field of the Trigger Mode control register to 1 to enable triggering.
- Set the Trigger Polarity field of the Trigger Mode control register to 0 to select falling edge triggering or 1 to select rising edge triggering.
- Set the Trigger Mode field of the Trigger Mode control register to 0 to select the programmable exposure mode or 1 to select the level controlled exposure mode.
- Set the Trigger Source field in the Trigger Mode control register to select which one of the four physical input ports on the camera will be used to receive the external trigger signal:
  - Set the Trigger Source field to 0 to select physical input port 0 to receive the ExTrig signal.
  - Set the Trigger Source field to 1 to select physical input port 1 to receive the ExTrig signal.
  - Set the Trigger Source field to 2 to select physical input port 2 to receive the ExTrig signal.
  - Set the Trigger Source field to 3 to select physical input port 3 to receive the ExTrig signal.

The default setting is for physical input port 0 to receive the ExTrig signal. Refer to Sections 2.1.2 and 2.5.1 for a description of the physical and electrical characteristics of the physical input ports.

The Trigger Source field of the Trigger Mode register is defined in version 1.31 of the IIDC specification.

Because the Trigger Source feature is so new, the Basler BCAM 1394 Driver does not yet include a method call to access this feature. As a work-around, you can use the techniques described in the tutorial for the Basler Smart Features Framework Software to directly read from or write to the Trigger Source field. The Smart Features Framework Software is available on the Basler web site. To download the software go to:

http://www.baslerweb.com/popups/popup_en_1825.php

The ExTrig signal must be used in combination with a one-shot or a continuous-shot command. If more precise control of exposure start time is desired, you must also monitor the Trigger Ready signal and you must base the timing of the ExTrig signal on the state of the Trigger Ready signal. (See Section 3.3.6 for recommended methods for using the signals)

The following descriptions assume that the ExTrig signal is set for rising edge triggering and the programmable exposure mode.

ExTrig/One-Shot Operation

In ExTrig/One-shot operation, a “One Shot Command” is used to prepare the camera to capture a single image. When the ExTrig signal rises, exposure will begin. To use this operating method, follow this sequence:

1. Use the shutter settings described in Section 3.3.1 to set your desired exposure time.
2. Set the One Shot field of the One Shot/Multi Shot control register to 1.
3. Check the state of the TrigRdy signal:
   a) If TrigRdy is high, you can toggle ExTrig when desired.
   b) If TrigRdy is low, wait until TrigRdy goes high and then toggle ExTrig when desired. (See Section 3.4 for more about TrigRdy.)
4. When ExTrig rises, exposure will begin. Exposure will continue for the length of time specified in the Shutter control register.
5. At the end of the specified exposure time, readout and transmission of the captured image will take place.

The One Shot field of the One Shot/Multi Shot control register is self cleared after image transmission.

ExTrig/Continuous-Shot Operation

In ExTrig/Continuous-shot operation, a “Continuous Shot Command” is used to prepare the camera to capture multiple images. With this method of operation, exposure will begin on each rising edge of the ExTrig signal. To use this operating method, follow this sequence:

1. Use the shutter settings described in Section 3.3.1 to set your desired exposure time.
2. Set the Continuous Shot field of the ISO En/Continuous Shot control register to 1 (see page 4-21).
3. Check the state of the TrigRdy signal:
   a) If TrigRdy is high, you can toggle ExTrig when desired.
   b) If TrigRdy is low, wait until TrigRdy goes high and then toggle ExTrig when desired. (See Section 3.4 for more about TrigRdy.)
4. When ExTrig rises, exposure will begin. Exposure will continue for the length of time specified in the Shutter control register.
5. At the end of the specified exposure time, readout and transmission of the captured image will take place.
6. Repeat steps 3 and 4 each time that you want to begin exposure and capture an image.
7. To disable continuous-shot operation, set the Continuous Shot field in the ISO En/ Continuous Shot control register to 0.

These explanations of exposure start are included to give the user a basic insight into the interactions of the camera's registers. Typically, IEEE 1394 cameras are used with a driver which includes an interface that allows the user to parameterize and operate the camera without directly setting registers. The Basler BCAM 1394 Camera Driver, for example, has both a simple Windows® interface and a programmer's API for parameterizing and operating the camera.

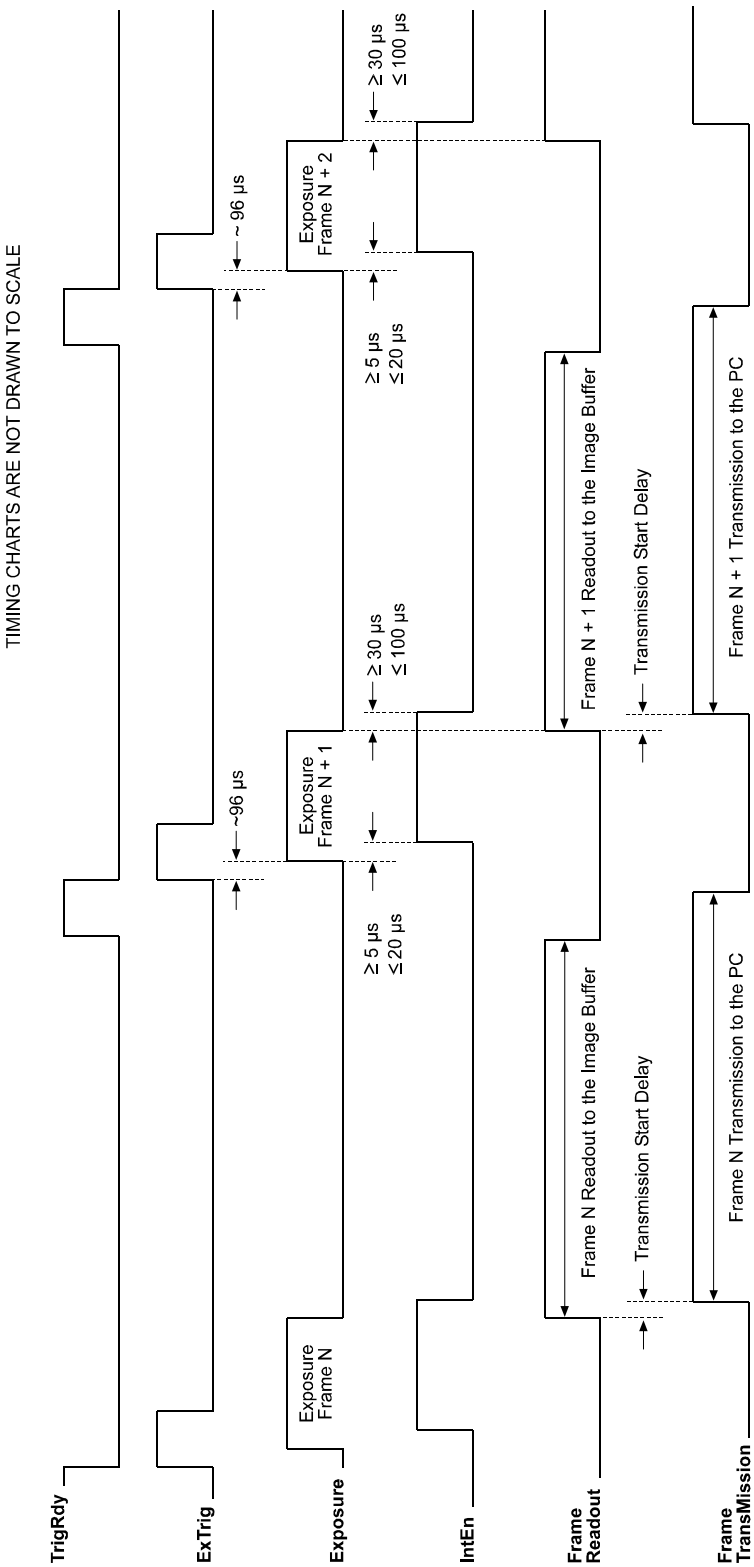


Figure 3-7: Exposure Start Controlled with an ExTrig Signal

3.3.6 Recommended Method for Controlling Exposure Start

The camera can be programmed to begin exposure on a rising edge or on a falling edge of an ExTrig signal. Also, two modes of exposure control are available: programmable and level controlled (see Section 3.3.5). For this illustration, we are assuming that a rising edge trigger and the programmable exposure mode are used.

If a camera user requires close control of exposure start, there are several general guidelines that must be followed:

- The camera should be placed in continuous-shot mode.
- The user must use an external trigger (ExTrig) signal to start exposure.
- The user must monitor the trigger ready (TrigRdy) signal.
- A rising edge of the ExTrig signal must only occur when the TrigRdy signal is high.

Assuming that these general guidelines are followed, the reaction of the camera to a rising external trigger signal will be as shown in:

- The start of exposure will typically occur 96 µs after the rise of the ExTrig signal as shown in Figure 3-7.
- The integrate enabled (IntEn) signal will rise between 5 and 20 µs after the start of exposure.

  (The delay between the start of exposure and the rise of the IntEn signal will be in a range from 5 to 20 µs. The delay will vary slightly from camera to camera, but for any given camera, the delay will be consistent from exposure to exposure. For example, if a given camera has 7 µs delay, the delay will consistently be 7 µs for each exposure.)
- The actual length of exposure will be equal to the programmed exposure time.
- The IntEn signal will fall between 30 and 100 µs after the end of exposure.

  (The delay between the end of exposure and the fall of the IntEn signal will be in a range from 30 to 100 µs. The delay will vary slightly from camera to camera, but for any given camera, the delay will be consistent from exposure to exposure. For example, if a given camera has 10 µs delay, the delay will consistently be 10 µs for each exposure.)

3.3.7 Frame Buffering

As shown in Figure 3-7, after each image is captured, the camera begins reading out the captured image data from the CMOS sensor into a buffer in the camera. When the camera has determined that a sufficient amount of image data has accumulated in the buffer, it will begin transmitting the image data from the camera to the host PC.

This buffering technique avoids the need to exactly synchronize the clock used for sensor readout with the clock used for data transmission over the IEEE 1394 bus. The camera will begin transmitting data when it has determined that it can safely do so without over-running or under-running the buffer. This buffering technique is also an important element in achieving the highest possible frame rate with the best image quality.

The **frame readout time** is the amount of time it takes to read out a captured image from the CMOS sensor into the image buffer.

The **frame transmission time** is the amount of time it takes to transmit the captured image from the buffer in the camera to the host PC via the IEEE 1394 bus.

The **transmission start delay** is the amount of time between the point where the camera begins reading out a captured image into the buffer to the point where it begins transmitting the data for the captured image from the buffer to the host PC.

You can calculate the frame readout time with this formula:

$$\text{Frame Readout Time in µs} = \frac{[(159 + \text{AOI Width}) \times (\text{AOI Height} + 1)] + 4157}{39321000}$$

If you are operating the camera in an 8 bit output mode, you can calculate the frame transmission time with this formula:

$$\text{Frame Transmission Time in µs} = \left\lceil \frac{\text{AOI Width} \times \text{AOI Height}}{\text{Bytes per Packet}} \right\rceil \times 125$$

Note that the quantity inside of the brackets should be rounded up to the next integer.

If you are operating the camera in a 16 bit output mode, you can calculate the frame transmission time with this formula:

$$\text{Frame Transmission Time in µs} = \left\lceil \frac{\text{AOI Width} \times \text{AOI Height} \times 2}{\text{Bytes per Packet}} \right\rceil \times 125$$

Note that the quantity inside of the brackets should be rounded up to the next integer.

To calculate the transmission start delay, use the following information:

If the frame transmission time is greater than the frame readout time:

Start Delay in µs = 125

If the frame transmission time is less than the frame readout time:

Start Delay in µs = (Readout Time - Transmission Time) + 125

3.4 Trigger Ready Signal

The trigger ready signal is not defined in the 1394 Trade Association Digital Camera Specification. Trigger ready is a patented feature of Basler cameras that allows our cameras to have optimized timings.

As mentioned in Section 3.3.2, the start of exposure of a new frame must not occur until the camera has completely finished readout of the previously captured frame. During normal operation, the camera constantly monitors the state of the sensor and generates a “trigger ready” (TrigRdy) signal. As shown in Figure 3-8, the trigger ready signal will go low when the exposure of each frame is started and will go high when frame readout is complete and it is safe for the next exposure to begin.

If you are triggering exposure with shot commands, a software trigger or and ExSync signal, you can avoid over-triggering the camera by monitoring the TrigRdy signal and only triggering the camera when the signal is high. (Over-triggering the camera means that you are attempting to trigger image capture at a rate that is higher than the maximum allowed with the current camera settings.)

You can ensure that you are operating the camera at the maximum allowed frame rate for the current camera settings by monitoring the TrigRdy signal and immediately triggering image capture each time you see the signal go high.

By default, the TrigRdy signal is assigned to physical output port 1 on the camera. See Section 2.5.2 for a description of the electrical characteristics of the camera’s physical output ports.

The assignment of the TrigRdy signal to a physical output port can be changed. See Section 6.7.10 for more information on changing the assignment of camera output signals to physical output ports.

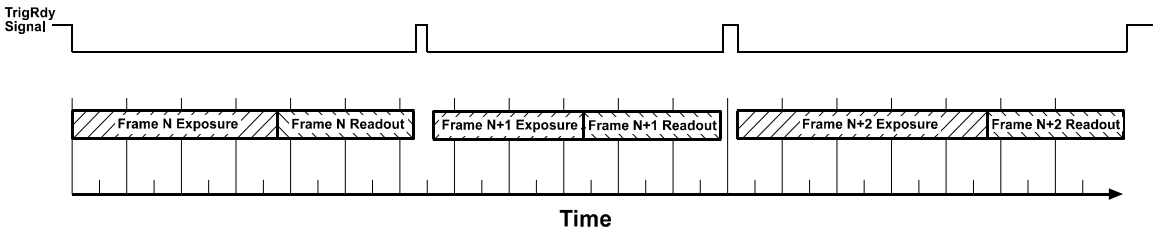


Figure 3-8: Trigger Ready Signal

If you attempt to start an exposure when the trigger ready signal is low, the camera will delay the start of exposure until the next rise of the signal. This prevents you from running the camera faster than the maximum rate and avoids dropping frames.

If the camera is in continuous shot mode and external triggering is disabled, the trigger ready output signal will not be present.

3.5 Integrate Enabled Signal

The Integrate Enabled (IntEn) signal goes high when exposure begins and goes low when exposure ends. This signal can be used as a flash trigger and is also useful when you are operating a system where either the camera or the object being imaged is movable. For example, assume that the camera is mounted on an arm mechanism and that the mechanism can move the camera to view different portions of a product assembly. Typically, you do not want the camera to move during exposure. In this case, you can monitor the IntEn signal to know when exposure is taking place and thus know when to avoid moving the camera.

By default, the IntEn signal is assigned to physical output port 0 on the camera. See Section 2.5.2 for a description of the electrical characteristics of the camera's physical output ports.

The assignment of the IntEn signal to a physical output port can be changed. See Section 6.7.10 for more information on changing the assignment of camera output signals to physical output ports.

When you use the integrate enabled signal, be aware that there is a delay in the rise and the fall of the signal in relation to the start and the end of exposure. See Figure 3-7 for details.

3.6 Gain and Brightness

3.6.1 Gain

On **A620f** cameras, the gain function is accomplished by applying a digital multiplier to the output from the camera's sensor. The size of the multiplier depends on the setting in the Value field of the Gain control register (see page 4-25). Increasing the setting will increase the gain and will increase the camera's response to light as shown in Figure 3-9.

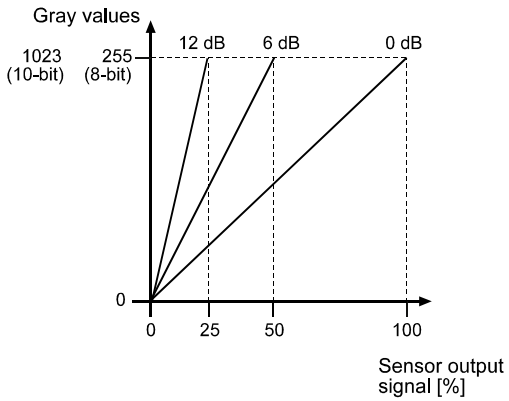


Figure 3-9: Gain

An increase in the gain setting can be useful when at your brightest exposure, a gray value of less than 255 (when the camera is set for 8 bit output) or less than 1023 (when the camera is set for 16 bit output with 10 bits effective) is achieved. For example, if the camera is set for 8 bit output and gray values no higher than 127 were achieved with bright light, you could increase the gain setting so that the camera is operating at 6 dB (an multiplication factor of 2) and see an increase in gray values to 254.

The range of valid settings for the Gain control register varies depending on whether the camera is set to output 8 bits per pixel or 16 bits per pixel.

Gain Settings with Camera Set for 8 Bit Output

When the camera is set to output 8 bits per pixel, the settings in the Gain control register can range from 0 (0x000) to 740 (0x2E4). The default gain setting when the camera is set for 8 bit output is 150 (0x096). To determine the dB of gain that you will see at a particular decimal setting, use the following formula:

$$\text{Gain} = 20 \log_{10}\left(\frac{\text{Register Setting (decimal)}}{80} + 1\right)$$

Typical settings and the resulting amplification are shown in Table 3-1.

Decimal	Hex	dB	Multiplication Factor	Decimal	Hex	dB	Multiplication Factor
0	0x000	0.0	x 1.0	425	0x1A9	16.0	x 6.3
125	0x07D	8.2	x 2.6	525	0x20D	17.6	x 7.6
225	0x0E1	11.6	x 3.8	625	0x271	18.9	x 8.8
325	0x145	14.1	x 5.1	740	0x2E4	20.2	x 10.3

Table 3-1: Gain Settings with 8 Bit Output

Gain Settings with Camera Set for 16 Bit Output

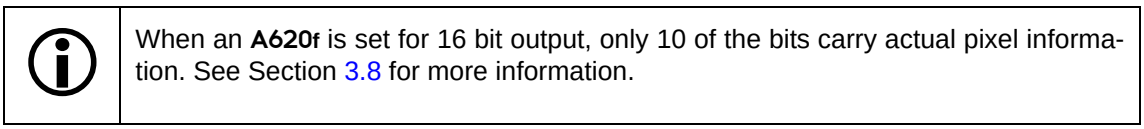
When the camera is set to output 16 bits per pixel, the settings in the Gain control register can range from 0 (0x000) to 125 (0x07D). The default gain setting when the camera is set for 16 bit output is 0 (0x000). To determine the dB of gain that you will see at a particular decimal setting, use the following formula:

$$\text{Gain} = 20 \log_{10} \left(\frac{\text{Register Setting (decimal)}}{80} + 1 \right)$$

Typical settings and the resulting amplification are shown in Table 3-2.

Decimal	Hex	dB	Multiplication Factor	Decimal	Hex	dB	Multiplication Factor
0	0x000	0.0	x 1.0	75	0x048	5.7	x 1.9
25	0x019	2.4	x 1.3	100	0x064	7.0	x 2.3
50	0x032	4.2	x 1.6	125	0x07D	8.2	x 2.6

Table 3-2: Gain Settings with 16 Bit Output



When an **A620f** is set for 16 bit output, only 10 of the bits carry actual pixel information. See Section 3.8 for more information.

3.6.2 Setting the Brightness

The camera's brightness is changed by setting the Value field of the Brightness control register (see page 4-23). The setting can range on a decimal scale from 0 to 255 (0x000 to 0x0FF). The default is typically 8 (0x008). The actual default may vary slightly from camera to camera. Settings below the default decrease the brightness and settings above the default increase the brightness.

The effect of a change in the brightness setting varies depending on whether the camera is set to output 8 bits per pixel or 16 bits per pixel. When the camera is set for 8 bit output, increasing the brightness setting by 4 results in an increase of 1 in the gray values output by the camera. When the camera is set for 16 bit output, increasing the brightness setting by 1 results in a increase of 1 in the gray values output by the camera.

3.7 Area of Interest (AOI)

The area of interest (AOI) feature allows you to specify a portion of the CMOS array and during operation, only the pixel information from the specified portion of the array is transmitted out of the camera.

The area of interest is referenced to the top left corner of the CMOS array. The top left corner is designated as column 0 and row 0 as shown in Figure 3-10.

The location and size of the area of interest is defined by declaring a left-most column, a width, a top row and a height. For example, suppose that you specify the left column as 10, the width as 16, the top row as 4 and the height as 10. The area of the array that is bounded by these settings is shown in Figure 3-10.

The camera will only transmit pixel data from within the area defined by your settings. Information from the pixels outside of the area of interest is discarded.

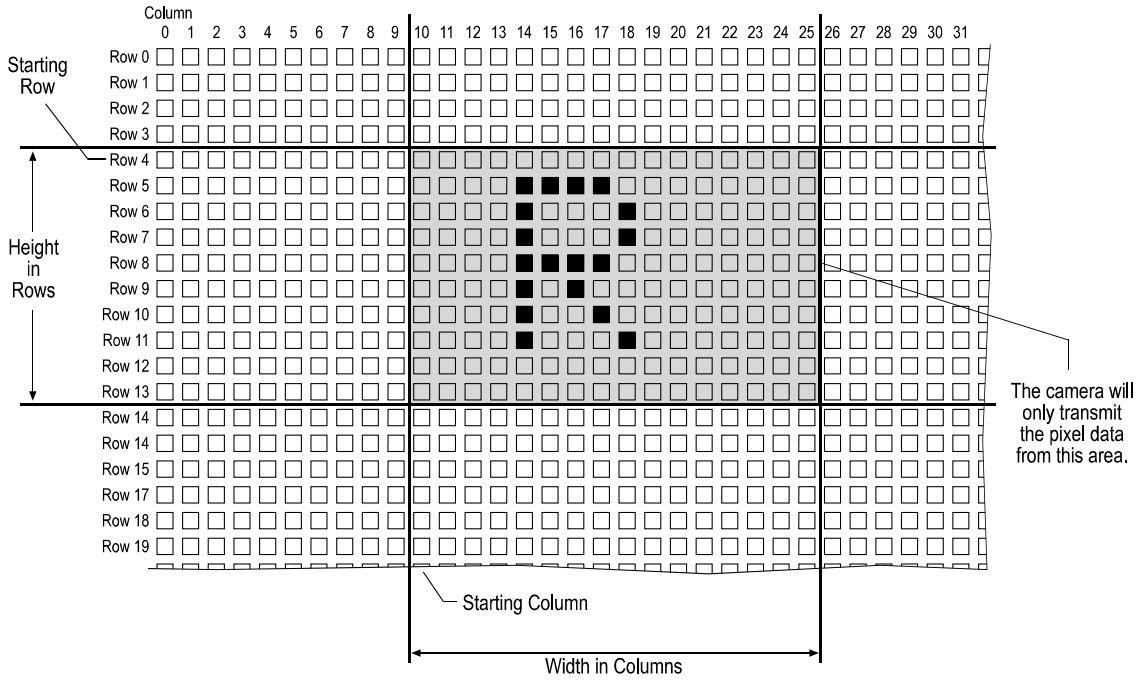


Figure 3-10: Area of Interest

The AOI feature is enabled by setting the camera to operate in Format 7, Mode 0. This is accomplished by setting the Format field of the Current Video Format control register (see page 4-20) to 7 and the Mode field of the Current Video Mode control register to 0.

The location of the area of interest is defined by setting a value for the Left field and a value for the Top field of the Image Position control register for Format 7, Mode 0 (see page 4-29). The size of the area of interest is defined by setting a value for the Width field and a value for the Height field of the Image Size control register for Format 7, Mode 0.

To use the entire CMOS array in **A620f** monochrome cameras, set the value for Left to 0, the value for Top to 0, the value for Width to 1280 and the value for Height to 1024.

The sum of the setting for *Left* plus the setting for *Width* must not exceed 1280.

The sum of the setting for *Top* plus the setting for *Height* must not exceed 1024.

The setting for the *Starting Column* must be zero or a multiple of 4, i.e., 0, 4, 8, 12, etc.

The setting for the *Width* must be a multiple of 4, i.e., 4, 8, 12, 16, etc.

3.7.1 Changing AOI Parameters “On-the-Fly”

Making AOI parameter changes “on-the-fly” means making the parameter changes while the camera is capturing images continuously. On-the-fly changes are only allowed for the parameters that determine the position of the AOI, i.e., the parameters for Top and Left. Changes to the AOI size are not allowed on-the-fly.

The camera’s response to an on-the-fly change in the AOI position will take effect on the next trigger after the changes are received by the camera.

3.7.2 Changes to the Frame Rate With AOI

In general, the maximum frame rate for **A620f** cameras increases as the size of the AOI decreases. However, the maximum frame rate can also be limited by three factors:

- The exposure time plus the amount of time it takes to read out a captured image from the image sensor to the frame buffer.
- The amount of time it takes to transmit an image from the frame buffer to the PC via the IEEE 1394 bus.
- Whether the camera is set for an 8 bit output mode or for a 16 bit output mode.

The descriptions on the next two pages illustrate how to determine the maximum allowed frame rate when your camera is set for 8 bit output and when it is set for 16 bit output.

Determining the Maximum Frame Rate with 8 Bit Output

When your camera is set to an 8 bit output mode, you can use the formulas below to determine the maximum frame rate for a given AOI. These formulas take your AOI size into account plus the other factors that can limit the frame rate. The formula that returns the lowest value will determine the maximum frame rate for the given AOI.

Formula 1

$$\text{Max frames/s} = \frac{1}{\frac{[(159 + \text{AOI Width}) \times (\text{AOI Height} + 1)] + 4157}{39321000} + \text{Exposure Time in Seconds}}$$

Formula 2:

$$\text{Max frames/s} = \frac{1}{\left[\frac{(\text{AOI Width} \times \text{AOI Height})}{\text{Bytes per Packet}}\right] \times 0.000125}$$

The quantity inside the bracket symbols should be rounded up to the nearest integer.

Example

Assume that your AOI is set for 100 columns wide and 110 rows high and that your exposure time is set for 3.1 ms. Also assume that the bytes per packet is set to 4096.

The number of number of bytes per packet is set in the Format 7, Mode 0 Byte Per Packet control register. In this example, we assume that the bytes per packet is set to the maximum. See page 4-33 and Section 3.12.2 for more information.

Formula 1:

$$\text{Max frames/s} = \frac{1}{\frac{[(159 + 100) \times (110 + 1)] + 4157}{39321000} + 0.00310}$$

Max frames/s = 254.0

Formula 2:

$$\text{Max frames/s} = \frac{1}{\left[\frac{(100 \times 110)}{4096}\right] \times 0.000125}$$

Max frames/s = 2666.7

Formula 1 returns the lowest value. So in this case, the maximum frame rate would be 261 frames per second.

Determining the Maximum Frame Rate with 16 Bit Output

When your camera is set to an 16 bit output mode, you can use the formulas below to determine the maximum frame rate for a given AOI. These formulas take your AOI size into account plus the other factors that can limit the frame rate. The formula that returns the lowest value will determine the maximum frame rate for the given AOI.

Formula 1

$$\text{Max frames/s} = \frac{1}{\frac{[(159 + \text{AOI Width}) \times (\text{AOI Height} + 1)] + 4157}{39321000} + \text{Exposure Time in Seconds}}$$

Formula 2:

$$\text{Max frames/s} = \frac{1}{\left\lceil \frac{(\text{AOI Width} \times \text{AOI Height} \times 2)}{\text{Bytes per Packet}} \right\rceil \times 0.000125}$$

The quantity inside the bracket symbols should be rounded up to the nearest integer.

Example

Assume that your AOI is set for 200 columns wide and 210 rows high and that your exposure time is set for 4.2 ms. Also assume that the bytes per packet is set to 4096.

The number of number of bytes per packet is set in the Format 7 Bytes Per Packet control register. In this example, we assume that the bytes per packet is set to the maximum. See Section 3.12.2 for more information.

Formula 1:

$$\text{Max frames/s} = \frac{1}{\frac{[(159 + 200) \times (210 + 1)] + 4157}{39321000} + 0.00420}$$

Max frames/s = 160.5

Formula 2:

$$\text{Max frames/s} = \frac{1}{\left\lceil \frac{(200 \times 210 \times 2)}{4096} \right\rceil \times 0.000125}$$

Max frames/s = 381.0

Formula 1 returns the lowest value. So in this case, the maximum frame rate would be 160.5 frames per second.

3.8 Selectable 8 or 10 Bit Pixel Depth

A620f cameras can be set to output pixel data at either 8 bit depth or 10 bit depth. (With 10 bit depth, the camera outputs 16 bits per pixel but only 10 bits are effective.)

For 8 Bit Depth

The method used to set the camera for 8 bit depth depends on whether you are operating the camera in a standard video format and mode or if you are operating the camera in Format 7, Mode 0.

If you want to operate the camera at 8 bit depth in a standard format and mode:

- Refer to Section 3.12.1 and select one of the available 8 bit video format / mode / frame rate combinations from the list.
- Set the Current Video Format, Current Video Mode and Current Video Frame Rate registers (see pages 4-19 and 4-20) to the appropriate values for the combination you selected.

If you want to operate the camera at 8 bit depth in Format 7, Mode 0:

- Set the Current Video Format and Current Video Mode registers (see pages 4-19 and 4-20) for Format 7 and Mode 0.
- Set the Color Coding ID field of the Format 7, Mode 0 register to the ID for Mono 8 (see Section 3.12.2 and page 4-29). With this ID set, the camera outputs 8 bits per pixel.

For 10 Bit Depth

The method used to set the camera for 10 bit depth depends on whether you are operating the camera in a standard video format and mode or if you are operating the camera in Format 7, Mode 0.

If you want to operate the camera at 10 bit depth in a standard format and mode:

- Refer to Section 3.12.1 and select one of the available 16 bit video format / mode / frame rate combinations from the list. (When the camera is set for 16 bit output, it outputs 16 bits but only 10 bits are effective.)
- Set the Current Video Format, Current Video Mode and Current Video Frame Rate registers (see pages 4-19 and 4-20) to the appropriate values for the combination you selected.

If you want to operate the camera at 10 bit depth in Format 7, Mode 0:

- Set the Current Video Format and Current Video Mode registers (see pages 4-19 and 4-20) for Format 7 and Mode 0.
- Set the Color Coding ID field of the Format 7, Mode 0 register to the ID for Mono 16 (see Section 3.12.2 and page 4-29). With this ID set, the camera outputs 16 bits per pixel but only 10 bits are effective.

When an **A620f** is set to output 16 bits per pixel, only 10 of the bits for each pixel carry actual pixel information. The 10 effective bits fill from the LSB and the unused bits are filled with zeros. Pixel data is stored in the PC memory in little endian format, i.e., the low byte for each pixel is stored at the lower address and the high byte is stored at the neighboring higher address.

3.9 Corrections for Sensor Characteristics

The Basler engineering team used its extensive experience to build in corrections for some of the characteristics exhibited by the sensor used in **A620f** cameras. The result is a camera that produces good image quality under normal conditions especially when compared to competitive cameras with the same sensor. Some of the corrections made on the **A620f** include:

- Fixed pattern noise correction via a calculated offset map.
- Correction for odd/even pixel mismatch that could be caused by the two banks of column amplifiers used in the camera's sensor.
- Compensation for the drift in sensor offset that could be caused by temperature variation in the camera's environment.

Even though the corrections included in the camera produce good image quality under normal conditions, two undesirable effects may still be exhibited when the camera is operated under extreme conditions. The first is a shutter efficiency effect and the second is a dark signal non-uniformity effect.

Shutter Efficiency

Under some extreme conditions, such as when the camera is set for full resolution, a shutter setting less than 50 and the lighting is very bright and continuous, the sensor's electronic shutter does not "close" efficiently. In these situations, after the normal exposure time is complete, the pixels will continue to expose slightly during sensor readout. This causes the pixel values in captured images to be higher at the bottom and lower at the top and the images will appear light at the bottom and dark at the top.

The amount of unwanted exposure that will occur during readout depends on the brightness of the light source and the ratio of the sensor readout time to the integration time. The effect will be most noticeable when images are captured with a combination of a large AOI, bright lighting and a short exposure time. Using smaller AOIs decreases the sensor readout time and minimizes the effect.

A recommended work around for the shutter efficiency effect is to use flash lighting that is bright during the sensor's normal exposure time and dark during sensor readout.

DSNU

At shutter settings of approximately 200 or less, the dark signal non-uniformity (DSNU) characteristics of the sensor have no effect on the image. At shutter settings above 200, DSNU begins to have an effect and the effect increases as the shutter setting is increased. At very high shutter settings, the effect of DSNU may become apparent in captured images. The DSNU effect becomes more noticeable at high gain settings, when the camera is operating in higher temperature environments and the sensor gets hot, or when the camera is set for a 16 bit output mode.

The effect of DSNU is usually described as "white spots" or "hot spots", i.e., some pixels appear lighter than they should be.

3.10 Strobe Control Output Signals

A620f cameras include a feature designed to help you control strobe lighting. The feature allows a user to enable and parameterize up to four strobe control output signals. The signals are designated as Strobe 0, Strobe 1, Strobe 2, and Strobe 3.

Enabling the Strobe Control Feature

The Strobe Signal control registers (see pages 4-38 and 4-39) are used to enable and parameterize the strobe output signals. To enable and parameterize the Strobe 0 signal:

- Set the value in the On/Off field of the Strobe 0 Control register to 1.
- Set the value in the Signal Polarity field to 0 for a low active signal or 1 for a high active signal as desired.
- Set the Delay Value field. The setting in this field will determine the time between the start of image exposure and when the strobe signal changes state as shown in Figure 3-11.

  The delay can be set to a value between 0 (0x000) and 4095 (0xFFF). The units for the delay are 1/1024 ms. For example, if the delay was set to 100 (0x064), the delay time would be 100/1024 ms (or approximately 97.7 µs).
- Set the Duration Value field. The setting in this field will determine the duration of the strobe signal as shown in Figure 3-11.

  The duration can be set to a value between 0 (0x000) and 4095 (0xFFF). The units for the duration are 1/1024 ms.

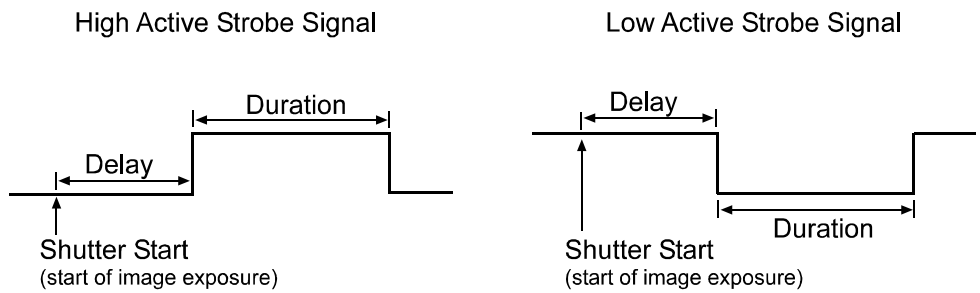


Figure 3-11: Strobe Signal

Once the Strobe 0 output signal has been enabled and parameterized, **it must be assigned to a physical output port on the camera**. The Strobe 0 signal can only be assigned to physical output port 0. See Section 6.7.10 for information on assigning output signals to physical output ports.

The Strobe 1 Control register is used to enable and parameterize the Strobe 1 output signal. The register is used in similar fashion as described for Strobe 0. Once the Strobe 1 output signal has been enabled and parameterized, it must be assigned to a physical output port on the camera. The Strobe 1 signal can only be assigned to physical output port 1.

The Strobe 2 and Strobe 3 output signals are also enabled, parameterized and assigned to a physical output port in similar fashion to Strobe 0.

If you start an image exposure and the strobe signal for the previously captured image is still running, the running strobe signal ends immediately and the next delay and duration begin.

The Strobe Control Output Signal registers are defined in version 1.31 of the IIDC specification.

Because the strobe control output signal feature is so new, the Basler BCAM 1394 Driver does not yet include a method call to access this feature. As a work-around, you can use the techniques described in the tutorial for the Basler Smart Features Framework Software to directly read from or write to the strobe control output signal registers. The Smart Features Framework Software is available on the Basler web site. To download the software go to:

http://www.baslerweb.com/popups/popup_en_1825.php

3.11 Parallel Input/Output Control

A parallel I/O control feature is available on **A620f** cameras. The feature allows a user to set the state of the four physical output ports on the camera and to read the state of the four physical input ports.

To set state of the four physical output ports, write values to the fields in the PIO Output register (see page 4-36):

- The value in the Port 0 Out field sets the state of physical output port 0.
- The value in the Port 1 Out field sets the state of physical output port 1.
- The value in the Port 2 Out field sets the state of physical output port 2.
- The value in the Port 3 Out field sets the state of physical output port 3.

Writing to the PIO Output register will only set the state of physical output ports that are configured as “User set.” For any output ports not configured as user set, the bit settings in this register will be ignored. See Section 6.7.10 for information on configuring physical output ports.

To determine the current state of the four physical input ports, read the values in the PIO Input register fields (see page 4-36):

- The value in the Port 0 In field indicates the current state of physical input port 0.
- The value in the Port 1 In field indicates the current state of physical input port 1.
- The value in the Port 2 In field indicates the current state of physical input port 2.
- The value in the Port 3 In field indicates the current state of physical input port 3.

The PIO Control registers are defined in version 1.31 of the IIDC specification.

Because the PIO control feature is so new, the Basler BCAM 1394 Driver does not yet include a method call to access this feature. As a work-around, you can use the techniques described in the tutorial for the Basler Smart Features Framework Software to directly read from or write to the PIO registers. The Smart Features Framework Software is available on the Basler web site. To download the software go to:

http://www.baslerweb.com/popups/popup_en_1825.php

3.12 Available Video Formats, Modes & Frame Rates

3.12.1 Standard Formats, Modes and Frame Rates

The following standard video formats, modes and frame rates are available on **A620f** cameras:

Format 0, Mode 1, Frame Rate 0 (320 x 240, YUV 4:2:2, 16 bits/pixel avg, 1.875 fps)

Format 0, Mode 1, Frame Rate 1 (320 x 240, YUV 4:2:2, 16 bits/pixel avg, 3.75 fps)

Format 0, Mode 1, Frame Rate 2 (320 x 240, YUV 4:2:2, 16 bits/pixel avg, 7.5 fps)

Format 0, Mode 1, Frame Rate 3 (320 x 240, YUV 4:2:2, 16 bits/pixel avg, 15 fps)

Format 0, Mode 1, Frame Rate 4 (320 x 240, YUV 4:2:2, 16 bits/pixel avg, 30 fps)

Format 0, Mode 1, Frame Rate 5 (320 x 240, YUV 4:2:2, 16 bits/pixel avg, 60 fps)

YUV 4:2:2 output is normally associated with color cameras, but in this case, it is available on **A620f** monochrome cameras. When an **A620f** is set for YUV 4:2:2, its output will be in the YUV 4:2:2 format but the output will be monochrome, not color. This monochrome version of the YUV 4:2:2 format is provided so that the camera can be used with Windows XP accessories such as Movie Maker.

Format 0, Mode 5, Frame Rate 0 (640 x 480, Y Mono, 8 bits/pixel, 1.875 fps)

Format 0, Mode 5, Frame Rate 1 (640 x 480, Y Mono, 8 bits/pixel, 3.75 fps)

Format 0, Mode 5, Frame Rate 2 (640 x 480, Y Mono, 8 bits/pixel, 7.5 fps)

Format 0, Mode 5, Frame Rate 3 (640 x 480, Y Mono, 8 bits/pixel, 15 fps)

Format 0, Mode 5, Frame Rate 4 (640 x 480, Y Mono, 8 bits/pixel, 30 fps)

Format 0, Mode 5, Frame Rate 5 (640 x 480, Y Mono, 8 bits/pixel, 60 fps)

Format 0, Mode 6, Frame Rate 0 (640 x 480, Y Mono, 16 bits/pixel, 1.875 fps)

Format 0, Mode 6, Frame Rate 1 (640 x 480, Y Mono, 16 bits/pixel, 3.75 fps)

Format 0, Mode 6, Frame Rate 2 (640 x 480, Y Mono, 16 bits/pixel, 7.5 fps)

Format 0, Mode 6, Frame Rate 3 (640 x 480, Y Mono, 16 bits/pixel, 15 fps)

Format 0, Mode 6, Frame Rate 4 (640 x 480, Y Mono, 16 bits/pixel, 30 fps)

When an **A620f** is set for a standard mono mode that outputs 16 bits per pixel, the camera outputs 16 bits for each pixel but only 10 of the bits carry actual pixel information. The 10 effective bits fill from the LSB and the unused bits are filled with zeros. Pixel data is stored in the PC memory in little endian format, i.e., the low byte for each pixel is stored at the lower address and the high byte is stored at the neighboring higher address.

Format 1, Mode 2, Frame Rate 2 (800 x 600, Y Mono, 8 bits/pixel, 7.5 fps)
Format 1, Mode 2, Frame Rate 3 (800 x 600, Y Mono, 8 bits/pixel, 15 fps)
Format 1, Mode 2, Frame Rate 4 (800 x 600, Y Mono, 8 bits/pixel, 30 fps)
Format 1, Mode 2, Frame Rate 5 (800 x 600, Y Mono, 8 bits/pixel, 60 fps)

Format 1, Mode 5, Frame Rate 1 (1024 x 768, Y Mono, 8 bits/pixel, 3.75 fps)
Format 1, Mode 5, Frame Rate 2 (1024 x 768, Y Mono, 8 bits/pixel, 7.5 fps)
Format 1, Mode 5, Frame Rate 3 (1024 x 768, Y Mono, 8 bits/pixel, 15 fps)
Format 1, Mode 5, Frame Rate 4 (1024 x 768, Y Mono, 8 bits/pixel, 30 fps)

Format 1, Mode 6, Frame Rate 1 (800 x 600, Y Mono, 16 bits/pixel, 3.75 fps)
Format 1, Mode 6, Frame Rate 2 (800 x 600, Y Mono, 16 bits/pixel, 7.5 fps)
Format 1, Mode 6, Frame Rate 3 (800 x 600, Y Mono, 16 bits/pixel, 15 fps)
Format 1, Mode 6, Frame Rate 4 (800 x 600, Y Mono, 16 bits/pixel, 30 fps)

Format 1, Mode 7, Frame Rate 1 (1024 x 768, Y Mono, 16 bits/pixel, 3.75 fps)
Format 1, Mode 7, Frame Rate 2 (1024 x 768, Y Mono, 16 bits/pixel, 7.5 fps)
Format 1, Mode 7, Frame Rate 3 (1024 x 768, Y Mono, 16 bits/pixel, 15 fps)

Format 2, Mode 2, Frame Rate 0 (1280 x 960, Y Mono, 8 bits/pixel, 1.875 fps)
Format 2, Mode 2, Frame Rate 1 (1280 x 960, Y Mono, 8 bits/pixel, 3.75 fps)
Format 2, Mode 2, Frame Rate 2 (1280 x 960, Y Mono, 8 bits/pixel, 7.5 fps)
Format 2, Mode 2, Frame Rate 3 (1280 x 960, Y Mono, 8 bits/pixel, 15 fps

Format 2, Mode 6, Frame Rate 0 (1280 x 960, Y Mono, 16 bits/pixel, 1.875 fps)
Format 2, Mode 6, Frame Rate 1 (1280 x 960, Y Mono, 16 bits/pixel, 3.75 fps)
Format 2, Mode 6, Frame Rate 2 (1280 x 960, Y Mono, 16 bits/pixel, 7.5 fps)

When an **A620f** is set for a standard format and mode, the image area will be centered on the sensor.

3.12.2 Customizable Formats and Modes

Format 7, Mode 0 is available on **A620f** cameras.

Format 7, Mode 0

Format 7, Mode 0 is used to enable and set up the area of interest (AOI) feature described in Section 3.7. Format 7, Mode 0 is parameterized by using the Format 7, Mode 0 control and status registers (see pages 4-29 to 4-35).

When the camera is operating in Format 7, Mode 0, the frame rate can be adjusted by setting the number of bytes transmitted in each packet. The number of bytes per packet is set by the Bytes Per Packet field of the Bytes Per Packet register.

The value that appears in the Max Bytes Per Packet field of the Packet Para Inquiry register will show the maximum allowed bytes per packet setting given the current AOI settings. When the bytes per packet is set to the maximum, the camera will transmit frames at its maximum specified rate. By default, the AOI is set to use the full sensor area and the bytes per packet is set to 4096.

If you set the bytes per packet to a value lower than the maximum, the camera will transmit frames at a lower rate. The rate is calculated by the formula:

$$\text{Frames/s} = \frac{1}{\text{Packets per Frame} \times 125\ \mu\text{s}}$$

Keep in mind that when you lower the bytes per packet setting, the number of bytes needed to transmit a frame (the packets per frame) will increase. Due to limitations in the DCAM structure, a maximum of 4095 packets per frame is allowed. If you set the bytes per packet too low, the number of packets per frame will exceed the 4095 packet limit and the camera will not transmit frames properly.

When the camera is operating in Format 7, the Current Video Frame Rate control register is not used and has no effect on camera operation.

Color Codings

In Format 7, Mode 0, the Mono 8 and Mono 16 color codings are available.

When the **Mono 8** ID is set in the Coding ID field of the Color Coding ID register for Format 7, Mode 0, the camera outputs 8 bits per pixel.

When the **Mono 16** ID is set in the Coding ID field of the Color Coding ID register for Format 7, Mode 0, the camera outputs 16 bits per pixel but only 10 bits are effective. The effective pixel data fills from the LSB and the unused bits are filled with zeros. Pixel data is stored in the PC memory in little endian format, i.e., the low byte for each pixel is stored at the lower address and the high byte is stored at the neighboring higher address.

When the camera is set for Mono 16, the maximum frame rate at full resolution is 12.5 fps.

Color code definitions can vary from camera model to camera model. This is especially true for older models of Basler cameras.

3.13 Error Flags

A620f cameras support the following error flags:

- Error flags that indicate whether the current trigger, shutter, gain and brightness settings are outside the specified range of allowed values. These error flags are set in the Trigger, Shutter, Gain and Brightness fields of the Feature Control Error Status High register (see page 4-27).
- An error flag that indicates whether the current combination of the following settings is acceptable to the camera:
  - Video format
  - Mode
  - Frame rate
  - ISO speed

  This error flag is available for Format 0, Format 1 and Format 2 only and is set in the Status field of the Vmode Error Status register (see page 4-21).
- An error flag that indicates whether the current combination of the following settings is acceptable to the camera:
  - Image position
  - Image size
  - Color Coding ID
  - ISO speed

  This error flag is available for Format 7 only.

  If you are operating the camera in Format 7 Mode_0, the flag is set in the Error Flag 1 field of the Value Setting register for Format 7 Mode_0 (see page 4-35).
- An error flag that indicates whether the current bytes per packet setting is acceptable to the camera.

  This error flag is available for Format 7 only.

  If you are operating the camera in Format 7 Mode_0, the flag is set in the Error Flag 2 field of the Value Setting register for Format 7 Mode_0 (see page 4-35).

The error flag registers are defined in version 1.31 of the IIDC specification.

4 Configuring the Camera

The **A620f** is configured by setting status and control registers as described in the “1394-Based Digital Camera Specification” issued by the 1394 Trade Association. The specification is commonly referred to as the “DCAM standard” or the “IIDC” standard.” It is available at the 1394 Trade Association’s web site: www.1394ta.org. Except where noted, all registers conform to version 1.31 of the DCAM standard.

If you are creating your own driver to operate the camera, Sections 4.1 through 4.4 provide the basic information you need about the registers implemented in the camera along with some information about read/write capabilities and the image data format.

The DCAM standard also outlines a set of “Advanced Features” registers. These registers can be used to implement vendor unique features not defined in the standard. The Basler “Smart Features Framework” takes advantage of these registers to implement features such as a frame counter and test images. See Section 6 for more information.

The BCAM Driver

A fully functional driver is available for Basler IEEE 1394 cameras such as the **A620f**. The Basler BCAM 1394 Driver/Software Development Kit includes an API that allows a C++ programmer to easily integrate camera configuration and operating functions into your system control software. The driver also includes a Windows® based viewer program that provides camera users with quick and simple tools for changing camera settings and viewing captured images.

The BCAM 1394 Driver/SDK comes with comprehensive documentation including a programmer’s guide and code samples. For more information, visit the Basler web site at: www.basler-vc.com.

4.1 Block Read and Write Capabilities

The camera supports block reads and block writes. If you do a single read or a block read, the camera will return a 0 for all non-existent registers. If you do a single write to a non-existent register or a block write that includes non-existent registers, the writes to non-existent registers will have no effect on camera operation.

Block reads or writes are limited to a payload of 32 quadlets.

4.2 Changing the Video Format setting

Whenever the Video Format setting is changed, you should also do the following:

If the Video Format is changed from Format 7 to Format 0, you should also check the Video Mode and the Video Frame Rate settings (see page 4-20). If necessary, change the Mode and Frame Rate settings so that they are compatible with Format 0.

If the Video Format is changed from Format 0 to Format 7, you should also check the Video Mode, the Image Position, the Image Size and the Bytes Per Packet settings (see pages 4-20 and 4-29). If necessary, change the Mode, Position, Size and Bytes per Packet settings so that they are compatible with Format 7.

4.3 Configuration ROM

The configuration ROM in the **A620f** is compliant with the DCAM specification V 1.31.

4.4 Implemented Standard Registers

This section includes a description of all DCAM standard registers implemented in the **A620f**.

4.4.1 Inquiry Registers

The base address for all inquiry registers is:

Bus ID, Node ID, FFFF F0F0 0000

In each inquiry register description, an “Offset from Base Address” is provided. This a byte offset from the above base address. The address of an inquiry register equals the above base address plus the indicated offset.

Values are stated in decimal format except when marked 0x. Values marked as 0x (e.g., 0x123) are in hexadecimal format. **Bit 0 in each register is the most significant bit.**

4.4.1.1 Initialize Inquiry Register

Register Name:		Camera Initialize
Offset from Base Address:		0x000
Field	**Bit**	**Description**
Initialize	0	If you set this bit to 1, the camera will reset itself, break any state lock, and re-initialize itself to factory settings. The bit is self cleared.
---	1 ... 31	Reserved

4.4.1.2 Inquiry Registers for Video Formats

Each bit in the video format inquiry register indicates the availability of a specific format.
0 = format not available 1 = format available

Register Name:		Video Format Inquiry	
Offset from Base Address:		0x100	
Field Name	**Bit**	**Description**	**A620f Value**
Format 0	0	VGA non-compressed format	1
Format 1	1	Super VGA non-compressed format (1)	1
Format 2	2	Super VGA non-compressed format (2)	1
Format x	3 ... 5	Reserved	---
Format 6	6	Still image format	0
Format 7	7	Partial image size format	1
---	8 ... 31	Reserved	---

4.4.1.3 Inquiry Registers for Video Modes

Each bit in the video mode inquiry register indicates the availability of a specific video format and mode combination (e.g., Format 0, Mode 0).

0 = not available 1 = available

Register Name:		Video Mode Inquiry for Format 0	
Offset from Base Address:		0x180	
Field	**Bit**	**Description**	**A620f Value**
Mode 0	0	160 x 120, YUV 4:4:4, 24 bits/pixel	0
Mode 1	1	320 x 240, YUV 4:2:2, 16 bits/pixel **Note:** The A620f supports a pseudo form of Format 0, Mode 1 (see Section 3.12.1 for more information).	1
Mode 2	2	640 x 480, YUV 4:1:1, 12 bits/pixel	0
Mode 3	3	640 x 480, YUV 4:2:2, 16 bits/pixel	0
Mode 4	4	640 x 480, RGB, 24 bits/pixel	0
Mode 5	5	640 x 480, Y Mono, 8 bits/pixel	1
Mode 6	6	640 x 480, Y Mono, 16 bits/pixel	1
Mode x	7	Reserved for another mode	---
---	8 ... 31	Reserved	---

Register Name:		Video Mode Inquiry for Format 1	
Offset from Base Address:		0x184	
Field	**Bit**	**Description**	**A620f Value**
Mode 0	0	800 x 600, YUV 4:2:2, 16 bits/pixel	0
Mode 1	1	800 x 600, RGB, 24 bits/pixel	0
Mode 2	2	800 x 600, Y Mono, 8 bits/pixel	1
Mode 3	3	1024 x 768, YUV 4:2:2, 16 bits/pixel	0
Mode 4	4	1024 x 768, RGB, 24 bits/pixel	0
Mode 5	5	1024 x 768, Y Mono, 8 bits/pixel	1
Mode 6	6	800 x 600, Y Mono 16, 16 bits/pixel	1
Mode 7	7	1024 x 768, Y Mono, 16 bits/pixel	1
---	8 ... 31	Reserved	---

Register Name:		Video Mode Inquiry for Format 2	
Offset from Base Address:		0x188	
Field	**Bit**	**Description**	**A620f Value**
Mode 0	0	1280 x 960, YUV 4:2:2, 16 bits/pixel	0
Mode 1	1	1280 x 960, RGB, 24 bits/pixel	0
Mode 2	2	1280 x 960, Y Mono, bits/pixel	1
Mode 3	3	1600 x 1200, YUV 4:2:2, 16 bits/pixel	0
Mode 4	4	1600 x 1200, RGB, 24 bits/pixel	0
Mode 5	5	1600 x 1200, Y Mono, 8 bits/pixel	0
Mode 6	6	1280 x 960, Y Mono, 16 bits/pixel	1
Mode 7	7	1600 x 1200, Y Mono, 16 bits/pixel	0
---	8 ... 31	Reserved	---

Register Name:		Video Mode Inquiry for Format 7	
Offset from Base Address:		0x19C	
Field	**Bit**	**Description**	**A620f Value**
Mode 0	0	Format 7, Mode 0	1
Mode 1	1	Format 7, Mode 1	0
Mode 2	2	Format 7, Mode 2	0
Mode 3	3	Format 7, Mode 3	0
Mode 4	4	Format 7, Mode 4	0
Mode 5	5	Format 7, Mode 5	0
Mode 6	6	Format 7, Mode 6	0
Mode 7	7	Format 7, Mode 7	0
---	8 ... 31	Reserved	0

4.4.1.4 Inquiry Registers for Video Frame Rates

Each bit in the video frame rates inquiry register indicates the availability of a specific video format, mode, frame rate combination (e.g., Format 0, Mode 0, Frame Rate 0).

0 = format not available 1 = format available

Register Name:		Video Frame Rate Inquiry for Format 0, Mode 1	
Offset from Base Address:		0x204	
Field	**Bit**	**Description**	**A620f Value**
Frame Rate 0	0	1.875 fps standard frame rate	1
Frame Rate 1	1	3.75 fps standard frame rate	1
Frame Rate 2	2	7.5 fps standard frame rate	1
Frame Rate 3	3	15 fps standard frame rate	1
Frame Rate 4	4	30 fps standard frame rate	1
Frame Rate 5	5	60 fps standard frame rate	1
Frame Rate 6	6	120 fps standard frame rate	0
Frame Rate 7	7	240 fps standard frame rate	0
---	8 ... 31	Reserved	---

Register Name:		Video Frame Rate Inquiry for Format 0, Mode 5	
Offset from Base Address:		0x214	
Field	**Bit**	**Description**	**A620f Value**
Frame Rate 0	0	1.875 fps standard frame rate	1
Frame Rate 1	1	3.75 fps standard frame rate	1
Frame Rate 2	2	7.5 fps standard frame rate	1
Frame Rate 3	3	15 fps standard frame rate	1
Frame Rate 4	4	30 fps standard frame rate	1
Frame Rate 5	5	60 fps standard frame rate	1
Frame Rate 6	6	120 fps standard frame rate	0
Frame Rate 7	7	240 fps standard frame rate	0
---	8 ... 31	Reserved	---

Register Name:		Video Frame Rate Inquiry for Format 0, Mode 6	
Offset from Base Address:		0x218	
Field	**Bit**	**Description**	**A620f Value**
Frame Rate 0	0	1.875 fps standard frame rate	1
Frame Rate 1	1	3.75 fps standard frame rate	1
Frame Rate 2	2	7.5 fps standard frame rate	1
Frame Rate 3	3	15 fps standard frame rate	1
Frame Rate 4	4	30 fps standard frame rate	1
Frame Rate 5	5	60 fps standard frame rate	0
Frame Rate 6	6	120 fps standard frame rate	0
Frame Rate 7	7	240 fps standard frame rate	0
---	8 ... 31	Reserved	---

Register Name:		Video Frame Rate Inquiry for Format 1, Mode 2	
Offset from Base Address:		0x228	
Field	**Bit**	**Description**	**A620f Value**
Frame Rate 0	0	1.875 fps standard frame rate	0
Frame Rate 1	1	3.75 fps standard frame rate	0
Frame Rate 2	2	7.5 fps standard frame rate	1
Frame Rate 3	3	15 fps standard frame rate	1
Frame Rate 4	4	30 fps standard frame rate	1
Frame Rate 5	5	60 fps standard frame rate	1
Frame Rate 6	6	120 fps standard frame rate	0
Frame Rate 7	7	240 fps standard frame rate	0
---	8 ... 31	Reserved	---

Register Name:		Video Frame Rate Inquiry for Format 1, Mode 5	
Offset from Base Address:		0x234	
Field	**Bit**	**Description**	**A620f Value**
Frame Rate 0	0	1.875 fps standard frame rate	0
Frame Rate 1	1	3.75 fps standard frame rate	1
Frame Rate 2	2	7.5 fps standard frame rate	1
Frame Rate 3	3	15 fps standard frame rate	1
Frame Rate 4	4	30 fps standard frame rate	1
Frame Rate 5	5	60 fps standard frame rate	0
Frame Rate 6	6	120 fps standard frame rate	0
Frame Rate 7	7	240 fps standard frame rate	0
---	8 ... 31	Reserved	---

Register Name:		Video Frame Rate Inquiry for Format 1, Mode 6	
Offset from Base Address:		0x238	
Field	**Bit**	**Description**	**A620f Value**
Frame Rate 0	0	1.875 fps standard frame rate	0
Frame Rate 1	1	3.75 fps standard frame rate	1
Frame Rate 2	2	7.5 fps standard frame rate	1
Frame Rate 3	3	15 fps standard frame rate	1
Frame Rate 4	4	30 fps standard frame rate	1
Frame Rate 5	5	60 fps standard frame rate	0
Frame Rate 6	6	120 fps standard frame rate	0
Frame Rate 7	7	240 fps standard frame rate	0
---	8 ... 31	Reserved	---

Register Name:		Video Frame Rate Inquiry for Format 1, Mode 7	
Offset from Base Address:		0x23C	
Field	**Bit**	**Description**	**A620f Value**
Frame Rate 0	0	1.875 fps standard frame rate	0
Frame Rate 1	1	3.75 fps standard frame rate	1
Frame Rate 2	2	7.5 fps standard frame rate	1
Frame Rate 3	3	15 fps standard frame rate	1
Frame Rate 4	4	30 fps standard frame rate	0
Frame Rate 5	5	60 fps standard frame rate	0
Frame Rate 6	6	120 fps standard frame rate	0
Frame Rate 7	7	240 fps standard frame rate	0
---	8 ... 31	Reserved	---

Register Name:		Video Frame Rate Inquiry for Format 2, Mode 2	
Offset from Base Address:		0x248	
Field	**Bit**	**Description**	**A620f Value**
Frame Rate 0	0	1.875 fps standard frame rate	1
Frame Rate 1	1	3.75 fps standard frame rate	1
Frame Rate 2	2	7.5 fps standard frame rate	1
Frame Rate 3	3	15 fps standard frame rate	1
Frame Rate 4	4	30 fps standard frame rate	0
Frame Rate 5	5	60 fps standard frame rate	0
Frame Rate 6	6	120 fps standard frame rate	0
Frame Rate 7	7	Reserved	---
----	8 ... 31	Reserved	---

Register Name:		Video Frame Rate Inquiry for Format 2, Mode 6	
Offset from Base Address:		0x258	
Field	**Bit**	**Description**	**A620f Value**
Frame Rate 0	0	1.875 fps standard frame rate	1
Frame Rate 1	1	3.75 fps standard frame rate	1
Frame Rate 2	2	7.5 fps standard frame rate	1
Frame Rate 3	3	15 fps standard frame rate	0
Frame Rate 4	4	30 fps standard frame rate	0
Frame Rate 5	5	60 fps standard frame rate	0
Frame Rate 6	6	Reserved	---
Frame Rate 7	7	Reserved	---
---	8 ... 31	Reserved	---

4.4.1.5 Inquiry Registers for Format 7 CSR Offsets

Register Name:		Video CSR Inquiry for Format 7, Mode 0
Offset from Base Address:		0x2E0
Field	**Bit**	**Description**
Mode 0	0 ... 31	Indicates the quadlet offset from the base address of the initial register space for the Format 7, Mode 0 Control and Status Register (CSR). (The A620f supports Format 7, Mode 0)

4.4.1.6 Inquiry Register for Basic Functions

Each bit in the basic function inquiry register indicates the availability of a specific basic function.

0 = function not available 1 = function available

(The memory channel bits are an exception. Refer to the description below.)

Register Name:		Basic Function Inquiry	
Offset from Base Address:		0x400	
Field	**Bit**	**Description**	**A620f Value**
Advanced Feature Inq	0	Advanced (vendor unique) features availability	1
Vmode Error Status Inq	1	VMode Error Status register availability	1
Feature Control Error Status Register Inq	2	Feature Control Error Status register availability	1
Optional Function CSR Inq	3	Optional Function Control and Status register availability	1
---	4 ... 7	Reserved	---
1394.b Mode Capability	8	IEEE 1394b capability	0
---	9 ... 15	Reserved	---
Camera Power Ctrl.	16	Power on/off capability	0
---	17 ... 18	Reserved	---
One Shot Inq	19	“One Shot” image capture mode availability	1
Multi Shot Inq	20	“Multi Shot” image capture mode availability	0
---	21 ... 27	Reserved	---
Memory Channels	28 ... 31	Indicates the maximum memory channel number available. If these bits are set to 0, the camera **does not** support memory channels.	0

4.4.1.7 Inquiry Register for Feature Presence

Each bit in the feature presence inquiry registers indicates the availability of a camera feature or optional function. Note that changing the video format or video mode may change the availability of a feature.

0 = feature not available 1 = feature available

Register Name:		Feature High Inquiry	
Offset from Base Address:		0x404	
Field	**Bit**	**Description**	**A62fF Value**
Brightness	0	Brightness control availability	1
Auto Exposure	1	Auto exposure control availability	0
Sharpness	2	Sharpness control availability	0
White Balance	3	White balance control availability	0
Hue	4	Hue control availability	0
Saturation	5	Saturation control availability	0
Gamma	6	Gamma control availability	0
Shutter	7	Shutter speed control availability	1
Gain	8	Gain control availability	1
Iris	9	Iris control availability	0
Focus	10	Focus control availability	0
Temperature	11	Temperature control availability	0
Trigger	12	Trigger control availability	1
Trigger Delay Control	13	Trigger delay control availability	0
White Shading	14	White shading control availability	0
Frame Rate	15	Frame rate prioritization control availability	0
---	16 ... 31	Reserved	---

Register Name:		Feature Low Inquiry	
Offset from Base Address:		0x408	
Field	**Bit**	**Description**	**A620f Value**
Zoom	0	Zoom control availability	0
Pan	1	Pan control availability	0
Tilt	2	Tilt control availability	0
Optical Filter	3	Optical filter control availability	0
---	4 ... 15	Reserved	0
Capture Size	16	Format 6 capture size availability	0
Capture Quality	17	Format 6 capture quality availability	0
---	18 ... 31	Reserved	---

Register Name:		Optional Function Inquiry	
Offset from Base Address:		0x40C	
Field	**Bit**	**Description**	**A620f Values**
---	0	Reserved	---
PIO	1	Parallel input/output control availability	1
SIO	2	Serial input/output control availability	0
Strobe Output	3	Strobe output control availability	1
---	4 ... 31	Reserved	---

Register Name:		Advanced Features Inquiry
Offset from Base Address:		0x480
Field	**Bit**	**Description**
Advanced Feature Quadlet Offset	0 ... 31	Indicates the quadlet offset from the base address of the initial register space for the advanced features Control and Status Registers (CSR). The A620f supports advanced (vendor unique) features.

Register Name:		PIO Control CSR Inquiry
Offset from Base Address:		0x484
Field	**Bit**	**Description**
PIO Control Quadlet Offset	0 ... 31	Indicates the quadlet offset from the base address of the initial register space for the PIO Control and Status Registers (CSR). The A620f supports PIO control.

Register Name:		Strobe Output CSR Inquiry
Offset from Base Address:		0x48C
Field	**Bit**	**Description**
Strobe Output Quadlet Offset	0 ... 31	Indicates the quadlet offset from the base address of the initial register space for the strobe output Control and Status Registers (CSR). The A620f supports strobe output control.

4.4.1.8 Inquiry Registers for Feature Elements

The feature element inquiry registers indicates the availability of elements, modes, maximum and minimum values for features. Note that changing the video format or video mode may change the availability of a feature element.

0 = element not available 1 = element available

Register Name:		Brightness Inquiry	
Offset from Base Address:		0x500	
Field	**Bit**	**Description**	**A620f Value**
Presence Inq	0	Brightness control feature is present	1
Abs Control Inq	1	Brightness can be set with an absolute value	0
---	2	Reserved	---
One Push Inq	3	One push auto mode is present	0
Read Out Inq	4	The brightness value can be read	1
On/Off Inq	5	Brightness control can be switched on/off	0
Auto Inq	6	A brightness auto control mode is present	0
Manual Inq	7	The brightness value can be set manually	1
Min Value	8 ... 19	Minimum value for brightness	0
Max Value	20 ... 31	Maximum value for brightness	255

Register Name:		Shutter Inquiry	
Offset from Base Address:		0x51C	
Field	**Bit**	**Description**	**A620f Value**
Presence Inq	0	Shutter control feature is present	1
Abs Control Inq	1	Shutter can be set with an absolute value	0
---	2	Reserved	---
One Push Inq	3	One push auto mode is present	0
Read Out Inq	4	The shutter value can be read	1
On/Off Inq	5	Shutter control can be switched on/off	0
Auto Inq	6	A shutter auto control mode is present	0
Manual Inq	7	The shutter value can be set manually	1
Min Value	8 ... 19	Minimum value for shutter	1
Max Value	20 ... 31	Maximum value for shutter	For Format 0, Format 1 or Format 2, depends on the format, mode and frame rate settings. In Format 7, the maximum is 4095.

Register Name:		Gain Inquiry	
Offset from Base Address:		0x520	
Field	**Bit**	**Description**	**A620f Value**
Presence Inq	0	Gain control feature is present	1
Abs Control Inq	1	Gain can be set with an absolute value	0
---	2	Reserved	---
One Push Inq	3	One push auto mode is present	0
Read Out Inq	4	The gain value can be read	1
On/Off Inq	5	Gain control can be switched on/off	0
Auto Inq	6	A gain auto control mode is present	0
Manual Inq	7	The gain value can be set manually	1
Min Value	8 ... 19	Minimum value for gain	0
Max Value	20 ... 31	Maximum value for gain	When the camera is set to output 8 bits per pixel, max = 740 When the camera is set to output 16 bits per pixel, max = 125

Register Name:		Trigger Inquiry	
Offset from Base Address:		0x530	
Field	**Bit**	**Description**	**A620f Value**
Presence Inq	0	Trigger control feature is present	1
Abs Control Inq	1	Trigger can be set with an absolute value	0
---	2 ... 3	Reserved	---
Read Out Inq	4	The trigger value can be read	1
On/Off Inq	5	Trigger control can be switched on/off	1
Polarity Inq	6	The trigger input polarity can be changed	1
Value Read	7	The raw trigger input can be read	1
Trigger Source 0 Inq	8	Trigger source 0 is present (ID = 0)	1
Trigger Source 1 Inq	9	Trigger source 1 is present (ID = 1)	1
Trigger Source 2 Inq	10	Trigger source 2 is present (ID = 2)	1
Trigger Source 3 Inq	11	Trigger source 3 is present (ID = 3)	1
---	12 ... 14	Reserved	---
Software Trigger Inq	15	Software trigger is present (ID = 7)	1
Trigger Mode 0 Inq	16	Trigger mode 0 is present	1
Trigger Mode 1 Inq	17	Trigger mode 1 is present	1
Trigger Mode 2 Inq	18	Trigger mode 2 is present	0
Trigger Mode 3 Inq	19	Trigger mode 3 is present	0
Trigger Mode 4 Inq	20	Trigger mode 4 is present	0
Trigger Mode 5 Inq	21	Trigger mode 5 is present	0
---	22 ... 29	Reserved	---
Trigger Mode 14 Inq	30	Trigger mode 14 is present (Vendor unique trigger mode 0)	0
Trigger Mode 15 Inq	31	Trigger mode 15 is present (Vendor unique trigger mode 1)	0

4.4.2 Control and Status Registers

The base address for all camera control and status registers is:

Bus ID, Node ID, FFFF F0F0 0000

In each control and status register description, an “Offset from the Base Address” is provided. This a byte offset from the above base address. The address of a control and status register equals the above base address plus the indicated offset.

Values are stated in decimal format except when marked 0x. Values marked as 0x (e.g., 0x123) are in hexadecimal format. **Bit 0 in each register is the most significant bit.**

4.4.2.1 Control and Status Registers for Basic Camera Operation

Register Name:		Current Video Frame Rate / Revision
Offset from Base Address:		0x600
Field	**Bit**	**Description**
Frame Rate / Revision	0 ... 2	If the camera is set for video Format 0, 1 or 2, this field sets the current video frame rate. 0 = frame rate 0 4 = frame rate 4 1 = frame rate 1 5 = frame rate 5 2 = frame rate 2 6 = frame rate 6 3 = frame rate 3 7 = frame rate 7 Default = 0 Check Section 3.12 to determine the standard frame rates supported by the A620f. If the camera is set for Format 7, the setting in this field is ignored. If the camera is set for Format 6, this field sets the current revision. (The A620f does not support Format 6.)
---	3 ... 31	Reserved

Register Name:		Current Video Mode
Offset from Base Address:		0x604
Field	**Bit**	**Description**
Mode	0 ... 2	This field sets the current video mode. 0 = mode 0 4 = mode 4 1 = mode 1 5 = mode 5 2 = mode 2 6 = mode 6 3 = mode 3 7 = mode 7 Default = 0 Check Section 3.12 to determine the video modes supported by the A620f.
---	3 ... 31	Reserved

Register Name:		Current Video Format
Offset from Base Address:		0x608
Field	**Bit**	**Description**
Format	0 ... 2	This field sets the current video format. 0 = format 0 6 = format 6 1 = format 1 7 = format 7 2 = format 2 Default = 7 Check Section 3.12 to determine the video formats supported on the A620f.
---	3 ... 31	Reserved

Register Name:		ISO
Offset from Base Address:		0x60C
Field	**Bit**	**Description**
ISO Channel L	0 ... 3	Sets the isochronous channel number for video transmission for the legacy mode. 0 = channel 0 6 = channel 6 11 = channel 11 1 = channel 1 7 = channel 7 12 = channel 12 2 = channel 2 8 = channel 8 13 = channel 13 3 = channel 3 9 = channel 9 14 = channel 14 4 = channel 4 10 = channel 10 15 = channel 15 5 = channel 5 Default = 0
---	4 ... 5	Reserved
Iso Speed L	6 ... 7	Sets the isochronous transmit speed code for the legacy mode. 0 = 100 M 1 = 200 M 2 = 400 M Default = 2
---	8 ... 15	Reserved
Operation Mode	16	Sets the 1394 operation mode. 0 = Legacy 1 = 1394.b Default = 0 The A620f does not support 1394b.
---	17	Reserved
Iso Channel B	18 ... 23	Not supported on the A602f.
---	24 ... 28	Reserved
Iso Speed B	29 ... 31	Not supported on the A620f.

Register Name:		ISO EN / Continuous Shot
Offset from Base Address:		0x614
Field	**Bit**	**Description**
Continuous Shot	0	When the camera is set for video Format 0, Format 1, Format 2 or Format 7, this field controls the “continuous shot” video transmission mode. 1 = start “continuous shot” transmission 0 = stop “continuous shot” transmission Default = 0
---	1 ... 31	Reserved

Register Name:		One Shot / Multi Shot
Offset from Base Address:		0x61C
Field	**Bit**	**Description**
One Shot	0	When the camera is set for video Format 0, Format 1, Format 2 or Format 7, this field controls the “one shot” video transmission mode. 1 = transmit one frame of video data (Field is self cleared after transmission.) Default = 0
Multi Shot	1	Multi shot is not supported on the A620f.
---	2 ... 15	Reserved
Count Number	16 ... 31	The count number for multi shot is not supported on the A620f.

Register Name:		VMode Error Status
Offset from Base Address:		0x628
Field	**Bit**	**Description**
Status	0	Used only when the camera is set for a standard format (not Format 7). This field will be updated each time the video format, mode, frame rate or ISO speed setting is changed. The value in this field indicates whether the current combination of video format, mode, frame rate and ISO speed settings is acceptable to the camera. 0 = the combination is OK, image capture can be started 1 = the combination is not OK, image capture can not be started This field is read only.
---	1 ... 31	Reserved

Register Name:		Software Trigger
Offset from Base Address:		0x62C
Field	**Bit**	**Description**
Trigger	0	When the Trigger Source field of the Trigger Mode register (see page 4-26) is set for a software trigger, this field controls the software trigger. 0 = reset the software trigger 1 = set the software trigger (If the Trigger Mode field of the Trigger Mode register is set to 0, this field will self clear.)
---	1 ... 31	Reserved

Register Name:		Data Depth
Offset from Base Address:		0x630
Field	**Bit**	**Description**
Depth	0 ... 7	Indicates the effective depth of the data in the transmitted images. Depends on the current format and mode settings. Also depends on the Color Coding ID if the camera is set for Format 7. This field is read only. **Camera set for:** — **Effective data depth indicated:** Mono 8 output — 8 bits/pixel Mono 16 output — 10 bits/pixel
---	8 ... 31	Reserved

4.4.2.2 Control and Status Registers for Features

Register Name:		Brightness
Offset from Base Address:		0x800
Field	**Bit**	**Description**
Presence Inq	0	Indicates the presence of the brightness control feature. The value will be 1 on all A620f cameras, indicating that brightness control is available. This field is read only.
Abs Control	1	Determines whether the brightness will be controlled by the Value field of this register or by the Absolute Value CSR for brightness. The value will be 0, indicating that brightness can only be controlled by the Value field of this register. Absolute value control is not available on A620f cameras. This field is read only.
---	2 ... 4	Reserved
One Push	5	Sets “One Push” operation. The value will be 0, indicating that one push is not in operation. One push operation is not available on A620f cameras. This field is read only.
On / Off	6	Sets whether brightness control is on or off. The value will be 1, indicating that brightness control is on. The brightness control feature can’t be switched off on A620f cameras. This field is read only.
A / M Mode	7	Sets whether the camera is in automatic or manual brightness control mode. The value will be 0, indicating that brightness control is in manual mode. Automatic brightness control is not available on A620f cameras. This field is read only.
---	8 ... 19	Reserved
Value	20 ... 31	Sets the brightness. The brightness value can range from 0 to 255. Default = 8 The effect of a change in the brightness value varies depending on whether the camera is set to output 8 bits per pixel or 16 bits per pixel. When the camera is set for 8 bit output, increasing the brightness value by 4 results in an increase of 1 in the digital values output by the camera. When the camera is set for 16 bit output, increasing the brightness value by 1 results in a increase of 1 in the digital values output by the camera.

Register Name:		Shutter
Offset from Base Address:		0x81C
Field	**Bit**	**Description**
Presence Inq	0	Indicates the presence of the shutter control feature. The value will be 1 on all A620f cameras, indicating that shutter control is available. This field is read only.
Abs Control	1	Determines whether the shutter will be controlled by the Value field of this register or by the Absolute Value CSR for the shutter. The value will be 0, indicating that the shutter can only be controlled by the Value field of this register. Absolute value control is not available on A620f cameras. This field is read only.
---	2 ... 4	Reserved
One Push	5	Sets “One Push” operation. The value will be 0, indicating that one push is not in operation. One push operation is not available on A620f cameras. This field is read only.
On / Off	6	Sets whether shutter control is on or off. The value will be 1, indicating that shutter control is on. The shutter control feature can’t be switched off on A620f cameras. This field is read only.
A / M Mode	7	Sets whether the camera is in automatic or manual shutter control mode. The value will be 0, indicating that shutter control is in manual mode. Automatic shutter control is not available on A620f cameras. This field is read only.
---	8 ... 19	Reserved
Value	20 ... 31	Sets the shutter. The shutter value can range from 1 to 4095. Exposure time = (Value in this field) x 20 µs Default = 200 See Section 3.3 for more information on the effect of the shutter value.

Register Name:		Gain
Offset from Base Address:		0x820
Field	**Bit**	**Description**
Presence Inq	0	Indicates the presence of the gain control feature. The value will be 1 on all A620f cameras, indicating that gain control is available. This field is read only.
Abs Control	1	Determines whether the gain will be controlled by the Value field of this register or by the Absolute Value CSR for gain. The value will be 0, indicating that gain can only be controlled by the Value field of this register. Absolute value control is not available on A620f cameras. This field is read only.
---	2 ... 4	Reserved
One Push	5	Sets “One Push” operation. The value will be 0, indicating that one push is not in operation. One push operation is not available on A620f cameras. This field is read only.
On / Off	6	Sets whether gain control is on or off. The value will be 1, indicating that gain control is on. The gain control feature can’t be switched off on A620f cameras. This field is read only.
A / M Mode	7	Sets whether the camera is in automatic or manual gain control mode. The value will be 0, indicating that gain control is in manual mode. Automatic gain control is not available on A620f cameras. This field is read only.
---	8 ... 19	Reserved
Value	20 ... 31	Sets the gain. The available range of gain values varies depending on whether the camera is set to output 8 bits per pixel or 16 bits per pixel. If the camera is set for 8 bit output, the gain value can range from 0 to 740. If the camera is set for 16 bit output, the gain value can range from 0 to 125. A value of 0 results in a gain of 0 dB. A value of 125 results in a gain of 8.2 dB. A value of 740 results in a gain of 20.2 dB. Default = 150 when the camera is set for 8 bit output and 0 when the camera is set for 16 bit output.

Register Name:		Trigger Mode
Offset from Base Address:		0x830
Field	**Bit**	**Description**
Presence Inq	0	Indicates the presence of the trigger mode control feature. The value will be 1 on all A620f cameras, indicating that trigger mode control is available. This field is read only.
Abs Control	1	Determines whether the trigger mode will be controlled by the Value field of this register or by the Absolute Value CSR for the trigger mode. The value will be 0, indicating that the trigger mode can only be controlled by the Value field of this register. Absolute value control is not available on A620f cameras. This field is read only.
---	2 ... 5	Reserved
On / Off	6	Sets whether trigger mode control is on or off. The value will be 1, indicating that trigger mode control is on. The trigger mode control feature can't be switched off on A620f cameras. This field is read only.
Trigger Polarity	7	Sets the trigger polarity when the camera is using a hardware trigger. 0 = low active input 1 = high active input Default = 1
Trigger Source	8 ... 10	Sets the trigger source. 0 = External trigger signal applied to physical input port 0 1 = External trigger signal applied to physical input port 1 2 = External trigger signal applied to physical input port 2 3 = External trigger signal applied to physical input port 3 7 = Software trigger Default = 0
Trigger Value	11	Not used on the A620f. This bit should be ignored.
Trigger Mode	12 ... 15	Sets the trigger mode. 0 = mode 0 (programmable mode) 1 = mode 1 (level mode) Default = 1 When an external trigger signal is used, mode 0 and mode 1 are both valid. When a software trigger is used, only mode 0 is valid. (See Section 3.3 for more information on exposure modes.)
---	16 ... 19	Reserved
Parameter	20 ... 31	Not used on the A620f. These bits should be ignored.

4.4.2.3 Error Status Registers for Feature Control

As defined in the IIDC specification, each field in this register is an error or warning flag for the corresponding feature control register. If a bit = 1, the mode and/or value of the corresponding feature control register has an error or warning. If a bit = 0, no error or warning is present. Each field in this register will be updated whenever the corresponding feature control register is updated. If a bit = 1, we strongly recommend checking the corresponding control register.

On **A620f** cameras, a feature's bit will become 1 when the feature's setting is outside the specified range of allowed settings, that is, the setting is lower than the allowed minimum or higher than the allowed maximum. If this situation occurs, **A620f** cameras will continue image capture and you will see the undesired effects that result from the setting.

Register Name:		Feature Control Error Status High
Offset from Base Address:		0x640
Field	**Bit**	**Description**
Brightness	0	Indicates a brightness control error. 0 = no error present 1 = A setting in the brightness control register (see page 4-23) is outside of the allowed range This field is read only.
Auto Exposure	1	Not used on the A620f. This bit should be ignored.
Sharpness	2	Not used on the A620f. This bit should be ignored.
White Balance	3	Not used on the A620f. This bit should be ignored.
Hue	4	Not used on the A620f. This bit should be ignored.
Saturation	5	Not used on the A620f. This bit should be ignored.
Gamma	6	Not used on the A620f. This bit should be ignored.
Shutter	7	Indicates a shutter control error. 0 = no error present 1 = A setting in the shutter control register (see page 4-24) is outside of the allowed range This field is read only.
Gain	8	Indicates a gain control error. 0 = no error present 1 = A setting in the gain control register (see page 4-25) is outside of the allowed range This field is read only.
Iris	9	Not used on the A620f. This bit should be ignored.
Focus	10	Not used on the A620f. This bit should be ignored.
Temperature	11	Not used on the A620f. This bit should be ignored.

Field	Bit	Description
Trigger	12	Indicates a trigger mode control error. 0 = no error present 1 = A setting in the trigger mode control register (see page 4-26) is outside of the allowed range This field is read only.
Trigger Delay	13	Not used on the A620f. This bit should be ignored.
White Shading	14	Not used on the A620f. This bit should be ignored.
Frame Rate	15	Not used on the A620f. This bit should be ignored.
---	16 ... 31	Reserved

Register Name:		Feature Control Error Status Low
Offset from Base Address:		0x644
Field	**Bit**	**Description**
Zoom	0	Not used on the A620f. This bit should be ignored.
Pan	1	Not used on the A620f. This bit should be ignored.
Tilt	2	Not used on the A620f. This bit should be ignored.
Optical Filter	3	Not used on the A620f. This bit should be ignored.
---	4 ... 15	Reserved
Capture Size	16	Not used on the A620f. This bit should be ignored.
Capture Quality	17	Not used on the A620f. This bit should be ignored.
---	18 ... 31	Reserved

4.4.2.4 Control and Status Registers for Format 7, Mode 0

Format 7, Mode 0 is available on all **A620f** cameras. The base address for each Format 7, Mode 0 camera control register is:

Bus ID, Node ID, FFFF F1F0 0000

In each Format 7, Mode 0 register description, an “Offset from the Base Address” is provided. This is a byte offset from the above base address. The address of a Format 7, Mode 0 register equals the above base address plus the indicated offset.

Values are stated in decimal format except when marked 0x. Values marked as 0x (e.g., 0x123) are in hexadecimal format. **Bit 0 in each register is the most significant bit.**

Register Name:		Max Image Size Inquiry
Offset from Base Address:		0x000
Field	**Bit**	**Description**
Hmax	0 ... 15	Indicates the maximum horizontal image size in pixels. Hmax = 1280
Vmax	16 ... 31	Indicates the maximum vertical image size in pixels. Vmax = 1024

Register Name:		Unit Size Inquiry
Offset from Base Address:		0x004
Field	**Bit**	**Description**
Hunit	0 ... 15	Indicates the increment in columns for adjusting the area of interest width (see Section 3.7). For example, if the Hunit is 2, the width should be set in increments of 2. Hunit = 4
Vunit	16 ... 31	Indicates the increment in rows for adjusting the area of interest height (see Section 3.7). For example, if the Vunit is 1, the height should be set in increments of 1. Vunit = 1

Register Name:		Image Position
Offset from Base Address:		0x008
Field Name:	**Bit**	**Description**
Left	0 ... 15	Sets the left (starting) column of pixels for the area of interest (see Section 3.7). Default = 0
Top	16 ... 31	Sets the top row of pixels for the area of interest (see Section 3.7). Default = 0

Register Name:		Image Size
Offset from Base Address:		0x00C
Field	**Bit**	**Description**
Width	0 ... 15	Sets the width in columns for the area of interest (see Section 3.7). Default = 1280
Height	16 ... 31	Sets the height in rows for the area of interest (see Section 3.7). Default = 1024

Register Name:		Color Coding ID
Offset from Base Address:		0x010
Field	**Bit**	**Description**
Coding ID	0 ... 7	Sets the color coding. Valid color codings are listed in the Color Coding Inquiry register (see the next register description). Default = ID 0
---	8 ... 31	Reserved

Register Name:		Color Coding Inquiry	
Offset from Base Address:		0x14	
Field Name:	**Bit**	**Description**	**A620f Value ***
Mono 8	0	Y only, 8 bits, non-compressed (ID = 0)	1
4:1:1 YUV8	1	4:4:1 YUV, 8 bits/component, non-compressed (ID = 1)	0
4:2:2 YUV 8	2	4:2:2 YUV, 8 bits/component, non-compressed (ID = 2)	0
4:4:4 YUV 8	3	4:4:4 YUV, 8 bits/component , non-compressed (ID = 3)	0
RGB 8	4	RGB, 8 bits/component, non-compressed (ID = 4)	0
Mono 16	5	Y only, 16 bits, non-compressed (unsigned integer) (ID = 5)	1
RGB 16	6	RGB, 16 bits/component, non-compressed (unsigned integer) (ID = 6)	0
Signed Mono 16	7	Y only, 16 bits, non-compressed (signed integer) (ID = 7)	0
Signed RGB 16	8	RGB, 16 bits/component, non-compressed (signed integer) (ID = 8)	0
Raw 8	9	8 bit, raw data output from a color filter sensor (ID = 9)	0
Raw 16	10	16 bit, raw data output from a color filter sensor (ID = 10)	0
---	11 ... 31	Reserved	---

* If a bit is set to 0, the A620f does not support this color coding ID
If a bit is set to 1, the A620f supports this color coding ID

Register Name:		Pixel Number Inquiry
Offset from Base Address:		0x034
Field	**Bit**	**Description**
Pixels Per Frame	0 ... 31	Indicates the total number of pixels per frame. The value in this register depends on settings in the Format 7, Mode 0 Image Size register (see page 4-30).

Register Name:		Total Bytes High Inquiry
Offset from Base Address:		0x038
Field	**Bit**	**Description**
Bytes Per Frame High	0 ... 31	Indicates the higher quadlet of the total bytes of image data per frame. The value in this register depends on settings in the Format 7, Mode 0 Image Size and Color Coding ID registers (see page 4-30). The value in this register includes image data, padding bytes and any data added by enabled smart features (see Section 6).

Register Name:		Total Bytes Low Inquiry
Offset from Base Address:		0x03C
Field	**Bit**	**Description**
Bytes Per Frame Low	0 ... 31	Indicates the lower quadlet of the total bytes of image data per frame. The value in this register depends on settings in the Format 7, Mode 0 Image Size and Color Coding ID registers (see page 4-30). The value in this register includes image data, padding bytes and any data added by enabled smart features (see Section 6).

Register Name:		Packet Para Inquiry
Offset from Base Address:		0x040
Field	**Bit**	**Description**
Unit Bytes Per Packet	0 ... 15	Indicates the increment for setting the Bytes per Packet field of the Bytes per Packet register (see page 4-33). 4 = the increment for setting the bytes per packet on the A620f.
Max Bytes Per Packet	16 ... 31	Indicates the maximum bytes per packet. 4096 = the maximum bytes per packet for the A620f.

Register Name:		Bytes Per Packet
Offset from Base Address:		0x044
Field	**Bit**	**Description**
Bytes Per Packet	0 ... 15	Sets the number of bytes per packet (the packet size). **Note:** When you lower the bytes per packet setting, the number of packets needed to transmit a frame (the packets per frame) will increase. Due to limitations in the DCAM structure, a maximum of 4095 packets per frame is allowed. If you set the bytes per packet too low, the number of packets per frame will exceed the 4095 packet limit and the camera will not transmit frames properly.
Rec Byte Per Packet	16 ... 31	Indicates the minimum bytes per packet needed to achieve the highest possible frame rate with the current camera settings. The recommended bytes per packet field is updated whenever the Format 7 settings are changed.

Register Name:		Packets Per Frame Inquiry
Offset from Base Address:		0x048
Field	**Bit**	**Description**
Packets Per Frame	0 ... 31	Indicates the total packets per frame. The value in this register depends on settings in the Format 7, Mode 0 Image Size and Color Coding ID registers (see page 4-30) and on the setting in the Format 7, Mode 0 Bytes per Packet register (see above). The value in this register includes image data, padding bytes and any data added by enabled smart features (see Section 6).

Register Name:		Unit Position Inquiry
Offset from Base Address:		0x04C
Field	**Bit**	**Description**
Hposunit	0 ... 15	Indicates the increment in columns for adjusting the area of interest starting column (see Section 3.7). For example, if the Hposunit is 2, the starting column should be adjusted in increments of 2. Hposunit = 4
Vposunit	16 ... 31	Indicates the increment in rows for adjusting the area of interest starting row (see Section 3.7). For example, if the Vposunit is 1, the starting row should be adjusted in increments of 1. Vposunit = 1

Register Name:		Frame Interval Inquiry
Offset from Base Address:		0x050
Field	**Bit**	**Description**
Frame Interval	0 ... 31	Indicates the current frame period in seconds. This value will be updated when you adjust any register that affects the frame period. The value in this register is a standard IEEE-754 single precision (32 bit) floating point number.

Register Name:		Data Depth Inquiry
Offset from Base Address:		0x054
Field	**Bit**	**Description**
Data Depth	0 ... 7	Indicates the effective depth of the data in the transmitted images. The value in this register depends on the setting in the Format 7, Mode 0 Color Coding ID register (see page 4-30). This field is read only. **Color Coding ID setting:** — **Effective data depth indicated:** ID = 0 (Mono 8) — 8 bits/pixel ID = 5 (Mono 16) — 10 bits/pixel
---	8 ... 31	Reserved

Register Name:		Value Setting
Offset from Base Address:		0x07C
Field	**Bit**	**Description**
Presence Inq	0	Indicates whether the fields in this register are valid. 0 = not valid 1 = valid The fields in this register are valid on the A620f. The Presence Inq field is read only.
Setting 1	1	On the A620f, this field is not relevant and should be ignored. (On the A620f, updates to the register values monitored by this field are performed automatically.)
---	2 ... 7	Reserved
Error Flag 1	8	Indicates whether the combination of the values in the ISO Speed register and in the Format 7 Mode 0 Image Position, Image Size and Color Coding ID registers and is acceptable. 0 = acceptable 1 = not acceptable and no image capture can be started
Error Flag 2	9	Indicates whether the value in the Bytes per Packet register is acceptable. 0 = acceptable 1 = not acceptable and no image capture can be started This field is updated whenever a value is written in the Bytes per Packet register.
---	10 ... 31	Reserved

4.4.2.5 Control and Status Registers for the PIO Control Function

The base address for the PIO Control Function control and status registers is:

Bus ID, Node ID, FFFF F2F0 00C8

In each PIO register description, an “Offset the from Base Address” is provided. This a byte offset from the above base address. The address of a PIO register equals the above base address plus the indicated offset.

Values are stated in decimal format except when marked 0x. Values marked as 0x (e.g., 0x123) are in hexadecimal format. **Bit 0 in each register is the most significant bit.**

Register Name:		PIO Output
Offset from Base Address:		0x000
Field	**Bit**	**Description**
---	0 ... 27	Reserved
Port 3 Out	28	Sets the state of physical output port 3. 0 = low 1 = high
Port 2 Out	29	Sets the state of physical output port 2. 0 = low 1 = high
Port 1 Out	30	Sets the state of physical output port 1. 0 = low 1 = high
Port 0 Out	31	Sets the state of physical output port 0. 0 = low 1 = high

The PIO Output register can only set the state of a physical output port if that port is configured as “User Set” (see Section 6.7.10). For any output port not configured as user set, the bit setting in the PIO Output register will be ignored.

Register Name:		PIO Input
Offset from Base Address:		0x004
Field	**Bit**	**Description**
---	0 ... 27	Reserved
Port 3 In	28	Indicates the current state of physical input port 3. 0 = low 1 = high
Port 2 In	29	Indicates the current state of physical input port 2. 0 = low 1 = high
Port 1 In	30	Indicates the current state of physical input port 1. 0 = low 1 = high
Port 0 In	31	Indicates the current state of physical input port 0. 0 = low 1 = high

4.4.2.6 Control and Status Registers for the Strobe Signal Function

The base address for the Strobe Signal control and status registers is:

Bus ID, Node ID, FFFF F2F0 0300

In each Strobe Signal register description, an “Offset from the Base Address” is provided. This a byte offset from the above base address. The address of a strobe signal register equals the above base address plus the indicated offset.

Values are stated in decimal format except when marked 0x. Values marked as 0x (e.g., 0x123) are in hexadecimal format. **Bit 0 in each register is the most significant bit.**

Register Name:		Strobe Control Inquiry	
Offset from Base Address:		0x000	
Field	**Bit**	**Description**	**A620f Value ***
Strobe 0 Inq	0	Presence of the Strobe 0 signal feature	1
Strobe 1 Inq	1	Presence of the Strobe 1 signal feature	1
Strobe 2 Inq	2	Presence of the Strobe 2 signal feature	1
Strobe 3 Inq	3	Presence of the Strobe 3 signal feature	1
---.	4 ... 31	Reserved	---

Register Name:		Strobe 0 Inquiry	
Offset from Base Address:		0x100	
Field	**Bit**	**Description**	**A620f Value ***
Presence Inq	0	Strobe 0 signal feature is present	1
---	1 ... 3	Reserved	---
Read Out Inq	4	The Strobe 0 value can be read	1
On/Off Inq	5	Strobe 0 control can be switched on/off	1
Polarity Inq	6	Strobe 0 polarity can be changed	1
---.	7	Reserved	---
Min Value	8 ... 19	Minimum value for Strobe 0 controls	0
Max Value	20 ... 31	Maximum value for Strobe 0 controls	4095

* If a bit is set to 0, the A620f does not support this feature
If a bit is set to 1, the A620f supports this feature

Register Name:		Strobe 1 Inquiry	
Offset from Base Address:		0x104	
Field	**Bit**	**Description**	**A620f Value**
Same definitions and values as Strobe 0 Inq			

Register Name:		Strobe 2 Inquiry	
Offset from Base Address:		0x108	
Field	**Bit**	**Description**	**A620f Value**
Same definitions and values as Strobe 0 Inq			

Register Name:		Strobe 3 Inquiry	
Offset from Base Address:		0x10C	
Field	**Bit**	**Description**	**A620f Value**
Same definitions and values as Strobe 0 Inq			

Register Name:		Strobe 0 Control
Offset from Base Address:		0x200
Field	**Bit**	**Description**
Presence Inq	0	Indicates the presence of the Strobe 0 signal control feature. 0 = not available 1 = available The Strobe 0 control feature is available on the A620f. This field is read only.
---	1 ... 5	Reserved
On / Off	6	Sets whether the Strobe 0 signal is on or off. 0 = off 1 = on Default = 0 If this bit is 0, all other fields in this register are read only.
Signal Polarity	7	Sets the polarity of the Strobe 0 signal. 0 = low active 1 = high active Default = 1
Delay Value	8 ... 19	Sets the delay time for the Strobe 0 signal (see Section 3.10). The delay value can range from 0 to 4095. The units for the delay are 1/1024 ms. For example, if the delay setting is 100, the delay will be 100/1024 ms (~ 97.7 µs).
Duration Value	20 ... 31	Sets the duration for the Strobe 0 signal (see Section 3.10). The duration value can range from 0 to 4095. The units for the delay are 1/1024 ms.

Register Name:		Strobe 1 Control
Offset from Base Address:		0x204
Field	**Bit**	**Description**
Same definitions and values as Strobe 0 Control.		

Register Name:		Strobe 2 Control
Offset from Base Address:		0x208
Field	**Bit**	**Description**
Same definitions and values as Strobe 0 Control.		

Register Name:		Strobe 3 Control
Offset from Base Address:		0x20C
Field	**Bit**	**Description**
Same definitions and values as Strobe 0 Control.		

If a strobe signal is on, the signal will only be present on the associated output port if the output port is configured for “strobe.” For example, if the Strobe 0 signal is on, the signal will only be present on physical output port 0 if the port is configured for “strobe”. If the Strobe 1 signal is on, the signal will only be present on physical output port 1 if the port is configured for “strobe”. Etc.

See Section 6.7.10 for more information about configuring the output ports.

4.4.3 Advanced Features Registers

The base address for all advanced features registers is:

Bus ID, Node ID, FFFF F2F0 0000

The first eight quadlets of the advanced features register space is designated as the advanced features “Access Control Register” as described in the table below.

Values are stated in decimal format except when marked 0x. Values marked as 0x (e.g., 0x123) are in hexadecimal format. **Bit 0 in each register is the most significant bit.**

Register Name:		Special Features Access Control Register
Offset from Base Address:		0x000
Field	**Bit**	**Description**
Feature ID High	0 ... 31	On the A620f, the value for Feature ID High field is: 0x0030 533B
Feature ID Low	32 ... 47	On the A620f, the value for Feature ID Low field is: 0x73C3
0xF	48 ... 51	This value for this field always 0xF.
Time Out	52 ... 63	On the A620f, the value for Time Out field is: 0x000

On the **A620f**, all advanced features registers, including the Access Control register, have been made part of Basler’s Smart Features Framework (SFF). See Section 6 for a detailed explanation of using the SFF framework to access advanced features. (Section 6.5.1 contains specific information about using the Access Control register.)

5 Image Data Formats and Structures

5.1 Image Data Basics

Image data is transmitted as isochronous data packets according to the “1394 - based Digital Camera Specification” (DCAM) issued by the 1394 Trade Association (see the trade association’s web site: www.1394ta.org). The first packet of each frame is identified by a 1 in the sync bit of the packet header.

5.1.1 Pixel Transmission Sequence

Pixel is transmitted from the camera in the following sequence:

Row 0/Pixel 0, Row 0/Pixel 1, Row 0/Pixel 2 ... Row 0/Pixel 1278, Row 0/Pixel 1279.

Row 1/Pixel 0, Row 1/Pixel 1, Row 1/Pixel 2 ... Row 1/Pixel 1278, Row 1/Pixel 1279.

Row 2/Pixel 0, Row 2/Pixel 1, Row 2/Pixel 2 ... Row 2/Pixel 1278, Row 2/Pixel 1279.

-
-
-

Row 1021/Pixel 0, Row 1021/Pixel 1, Row 1021/Pixel 2 ... Row 1021/ Pixel 1278, Row 1021/Pixel 1279

Row 1022/Pixel 0, Row 1022/Pixel 1, Row 1022/Pixel 2 ... Row 1022/ Pixel 1278, Row 1022/Pixel 1279

Row 1023/Pixel 0, Row 1023/Pixel 1, Row 1023/Pixel 2 ... Row 1023/ Pixel 1278, Row 1023/Pixel 1279

(This sequence assumes that the camera is set for full resolution.)

5.2 Packet Payload Charts for Standard Format, Mode and Frame Rate Combinations on the A620f

The following charts describe the packet payload for each standard format/mode/framerate combination available on the A620f. This information is especially useful when calculating the camera's bandwidth usage.

5.2.1 Format 0, Mode 1

(320 x 240, YUV 4:2:2, 16 bits/pixel avg)

Frame Rate	1.875 fps	3.75 fps	7.5 fps	15 fps	30 fps	60 fps
Lines per Packet	1/16	1/8	1/4	1/2	1	2
Pixels per Packet	20	40	80	160	320	640
Bytes per Packet	40	80	160	320	640	1280

5.2.2 Format 0, Mode 5

(640 x 480, Y Mono, 8 bits/pixel)

Frame Rate	1.875 fps	3.75 fps	7.5 fps	15 fps	30 fps	60 fps
Lines per Packet	1/8	1/4	1/2	1	2	4
Pixels per Packet	80	160	320	640	1280	2560
Bytes per Packet	80	160	320	640	1280	2560

5.2.3 Format 0, Mode 6

(640 x 480, Y Mono, 16 bits/pixel)

Frame Rate	1.875 fps	3.75 fps	7.5 fps	15 fps	30 fps
Lines per Packet	1/8	1/4	1/2	1	2
Pixels per Packet	80	160	320	640	1280
Bytes per Packet	160	320	640	1280	2560

5.2.4 Format 1, Mode 2

(800 x 600, Y Mono, 8 bits/pixel)

Frame Rate	7.5 fps	15 fps	30 fps	60 fps
Lines per Packet	5/8	5/4	5/2	5
Pixels per Packet	500	1000	2000	4000
Bytes per Packet	500	100	2000	4000

5.2.5 Format 1, Mode 5

(1024 x 768, Y Mono, bits/pixel)

Frame Rate	3.75 fps	7.5 fps	15 fps	30 fps
Lines per Packet	3/8	3/4	3/2	3
Pixels per Packet	384	768	1536	3072
Bytes per Packet	384	768	1536	3072

5.2.6 Format 1, Mode 6

(800 x 600, Y Mono, 16 bits/pixel)

Frame Rate	3.75 fps	7.5 fps	15 fps	30 fps
Lines per Packet	5/16	5/8	5/4	5/2
Pixels per Packet	250	500	1000	2000
Bytes per Packet	500	1000	2000	4000

5.2.7 Format 1, Mode 7

(1024 x 768, Y Mono, 16 bits/pixel)

Frame Rate	3.75 fps	7.5 fps	15 fps
Lines per Packet	3/8	3/4	3/2
Pixels per Packet	384	768	1536
Bytes per Packet	768	1536	3072

5.2.8 Format 2, Mode 2

(1280 x 960, Y Mono, bits/pixel)

Frame Rate	1.875 fps	3.75 fps	7.5 fps	15 fps
Lines per Packet	1/4	1/2	1	2
Pixels per Packet	320	640	1280	2560
Bytes per Packet	320	640	1280	2560

5.2.9 Format 2, Mode 6

(1280 x 960, Y Mono 16, bits/pixel)

Frame Rate	1.875 fps	3.75 fps	7.5 fps
Lines per Packet	1/4	1/2	1
Pixels per Packet	320	640	1280
Bytes per Packet	640	1280	2560

5.3 Image Data Formats

5.3.1 Data Format with the Camera Set for YUV 4:2:2 Output

The table below describes how the data for a received frame will be ordered in the image buffer in your PC.

The following standards are used in the table:

P_0 = the first pixel transmitted by the camera

P_n = the last pixel transmitted by the camera

B_0 = the first byte in the buffer

B_m = the last byte in the buffer

Byte	Data
B_0	U value for P_0
B_1	Y value for P_0
B_2	V Value for P_0
B_3	Y value for P_1
B_4	U value for P_2
B_5	Y value for P_2
B_6	V Value for P_2
B_7	Y value for P_3
B_8	U value for P_4
B_9	Y value for P_4
B_{10}	V Value for P_4
B_{11}	Y value for P_5
•	•
•	•
•	•
B_{m-7}	U value for P_{n-3}
B_{m-6}	Y value for P_{n-3}
B_{m-5}	V Value for P_{n-3}
B_{m-4}	Y value for P_{n-2}
B_{m-3}	U value for P_{n-1}
B_{m-2}	Y value for P_{n-1}
B_{m-1}	V Value for P_{n-1}
B_m	Y value for P_n

5.3.2 Data Format with the Camera Set for Y Mono 8 Output

The table below describes how the data for a received frame will be ordered in the image buffer in your PC.

The following standards are used in the table:

P_0 = the first pixel transmitted by the camera

P_n = the last pixel transmitted by the camera

B_0 = the first byte in the buffer

B_m = the last byte in the buffer

Byte	Data
B_0	Y value for P_0
B_1	Y value for P_1
B_2	Y value for P_2
B_3	Y value for P_3
B_4	Y value for P_4
B_5	Y value for P_5
B_6	Y value for P_6
B_7	Y value for P_7
•	•
•	•
•	•
B_{m-3}	Y value for P_{n-3}
B_{m-2}	Y value for P_{n-2}
B_{m-1}	Y value for P_{n-1}
B_m	Y value for P_n

5.3.3 Data Format with the Camera Set for Y Mono 16 Output

The table below describes how the data for a received frame will be ordered in the image buffer in your PC.

The following standards are used in the table:

P_0 = the first pixel transmitted by the camera

P_n = the last pixel transmitted by the camera

B_0 = the first byte in the buffer

B_m = the last byte in the buffer

Byte	Data
B_0	Low byte of Y value for P_0
B_1	High byte of Y value for P_0
B_2	Low byte of Y value for P_1
B_3	High byte of Y value for P_1
B_4	Low byte of Y value for P_2
B_5	High byte of Y value for P_2
B_6	Low byte of Y value for P_3
B_7	High byte of Y value for P_3
B_8	Low byte of Y value for P_4
B_9	High byte of Y value for P_4
B_{10}	Low byte of Y value for P_5
B_{11}	High byte of Y value for P_5
•	•
•	•
•	•
B_{m-7}	Low byte of Y value for P_{n-3}
B_{m-6}	High byte of Y value for P_{n-3}
B_{m-5}	Low byte of Y value for P_{n-2}
B_{m-4}	High byte of Y value for P_{n-2}
B_{m-3}	Low byte of Y value for P_{n-1}
B_{m-2}	High byte of Y value for P_{n-1}
B_{m-1}	Low byte of Y value for P_n
B_m	High byte of Y value for P_n

As shown in the table above, when the camera is set for 16 bit output, data is placed in the image buffer in **little endian format**. (The DCAM standard specifies big endian format for 16 bit output, but we do not follow this recommendation. We use little endian format so that 16 bit data can be processed more effectively on little endian hardware such as Intel® processor based PCs.)

When the camera is set for 16 bit output, 16 bits of data will be transmitted for each pixel but only 10 bits are effective (see Section 3.8).

5.4 Image Data Structure

5.4.1 Data Structure for a Y (Mono 8) Component

The data output for a Y (mono 8) component is 8 bit data of the “unsigned char” type. The range of data values for a Y mono component and the corresponding indicated signal levels are shown below.

This Data Value (Hexadecimal)	Indicates This Signal Level (Decimal)
0xFF	255
0xFE	254
●	●
●	●
●	●
0x01	1
0x00	0

5.4.2 Data Structure for a U or a V Component

The data output for a U or a V component is 8 bit data of the “straight binary” type. The range of data values for a U or a V component and the corresponding indicated signal levels are shown below.

This Data Value (Hexadecimal)	Indicates This Signal Level (Decimal)
0xFF	127
0xFE	126
●	●
●	●
●	●
0x81	1
0x80	0
0x7F	-1
●	●
●	●
●	●
0x01	-127
0x00	-128

The signal level of a U component or a V component can range from -128 to +127 (decimal). Notice that the data values have been arranged to represent the full signal level range.

5.4.3 Data Structure for a Y (Mono 16) Component

The data output for a Y (mono 16) component is 16 bit data of the “unsigned short (little endian)” type. The range of data values for a Y mono component and the corresponding indicated signal levels are shown below.

This Data Value (Hexadecimal)	Indicates This Signal Level (Decimal)
0x03FF	1023
0x03FE	1022
•	•
•	•
•	•
0x0001	1
0x0000	0

Normally, the data values for a 16 bit component would range from 0x0000 to 0xFFFF. However, when an A600f camera is set for 16 bit output, only 10 bits are effective. Therefore, the highest data value you will see is 0x03FF indicating a signal level of 1023.

6 Smart Features and the Smart Features Framework

6.1 What are Smart Features

Smart features are features unique to Basler cameras. Test Images, the Cycle Time Stamp, and the CRC (Cyclic Redundancy Check) Checksum are examples of Basler smart features.

In some cases, enabling a smart feature will simply change the behavior of the camera. The Test Image feature is a good example of this type of smart feature. When the Test Image feature is enabled, the camera outputs a test image rather than a captured image.

When certain smart features are enabled, the camera actually develops some sort of information about each image that it acquires. In these cases, the information is added to each image as trailing data when the image is transmitted from the camera. Examples of this type of smart feature are the Cycle Time Stamp feature and the CRC Checksum. When the Cycle Time Stamp feature is enabled, after an image is captured, the camera determines when the acquisition occurred and develops a cycle time stamp for the image. And if the CRC Checksum feature is enabled, the camera calculates a checksum for the image. The cycle time stamp and checksum are added as trailing data to each image as the image is transmitted from the camera.

6.2 What is the Smart Features Framework

The first component of the Smart Features Framework (SFF) is a mechanism that allows you to enable and to parametrize smart features. This mechanism is essentially an extension of the register structure defined in the DCAM specification for use with “Advanced Features.” The SFF establishes a register for each smart feature. By setting bits within the register for a particular smart feature, you can enable the feature and control how the feature operates.

When certain smart features are enabled, the camera actually develops some sort of data about each image that it acquires. For example, when the Cycle Time Stamp feature is enabled, the camera creates a time stamp for each image based on when the image exposure started. In the cases where a smart feature develops some sort of data about a captured image, the smart feature’s data is added as trailing data to each image as the image is transmitted from the camera.

The SFF provides a mechanism for parsing the smart features data added to images transmitted out of the camera by assigning a unique identifier (GUID) to each smart feature. Whenever the camera adds data for a smart feature to an image, it includes the GUID for the smart feature as

part of the added data. The GUIDs are especially useful when you enable several smart features that add data to the image stream. The GUIDs make it possible to identify which portion of the added data is the result of each enabled smart feature. Refer to Sections 6.6 and 6.7 for detailed information about getting smart features results.

6.3 What do I Need to Use Smart Features

To use smart features you will need:

- A camera that supports smart features. Not all camera models support smart features. And with some camera models that do support smart features, you may find that older cameras may not support all available smart features or may not support smart features at all. Section 6.5 contains information about checking a camera to see if it supports smart features.
- A method of accessing the camera's DCAM register structure. We strongly recommend that you use the Basler BCAM 1394 Driver (V1.7 or higher) along with the Basler Smart Features Framework software to access the registers. (See Section 6.4 for more information about the SFF Software.)

We strongly recommend that you use the Basler BCAM 1394 driver. However, any driver that can get images in Format 7 and that provides access to the DCAM registers can be used to work with smart features. If you do use a different driver, you can adapt the access techniques described in the SFF Software tutorial (see Section 6.4) to the driver you are using.

You should be aware that drivers other than the Basler BCAM driver have not been tested with smart features.

6.4 What is the Smart Features Framework Software?

A Smart Features Framework Software (SFF Software) package is available from Basler. The SFF Software has two major components:

- An SFF Viewer. The viewer is a Windows® based tool that allows you to easily enable and disable smart features, parameterize the camera, capture and view images, and view smart features results.
- An SFF Tutorial. The tutorial explains how to access the cameras smart features from within your own applications. The tutorial is based on the assumption that you are using the Basler BCAM 1394 driver with your camera.

The SFF software package is available for download at the Basler web site. To download the software, go to:

http://www.baslerweb.com/popups/popup_en_1825.php

The SFF Viewer will only work on PCs that have the BCAM driver V1.7 or higher installed.

6.5 Enabling and Parameterizing Smart Features

The camera provides a control and status register (CSR) for each smart feature (see Sect 6.7 for details of each feature and its CSR). To enable and parameterize a smart feature, the following steps must be performed:

1. Check to see if the camera supports smart features.
2. Ask the camera for the address of the CSR for the desired smart feature.
3. Enable and parameterize the desired smart features.

The next two sections describe steps 1 and 2. The layout of the registers used to enable and parameterize the smart features is described in section 6.7.

6.5.1 Checking to see if the Camera Supports Smart Features

Smart features are vendor unique. Such features are referred to in the 1394 Trade Association DCAM standard as advanced features. The DCAM standard specifies how vendors should implement advanced features. According to the standard, advanced features must be unlocked (that is, enabled) by writing an advanced features set identifier (Feature ID) and a time-out value to the Advanced Features Access Control Register. The Feature ID associated with Basler smart features is 0x0030 533B 73C3. From the point of view of the DCAM standard, smart features are a set of advanced DCAM features.

For Basler cameras, unlocking advanced features is not strictly necessary because all implemented smart features are always available. However, the unlock mechanism is also used to check to see if a camera supports vendor unique features such as smart features. If a device doesn't recognize a Feature ID written to the Access Control Register, a value of 0xFFFF FFFF FFFF FFFF will be read back from the ACR. This value indicates that the device does not implement the feature set associated with that Feature ID.

Assuming that the address of the Advanced Features Access Control Register is 0xFFFF F2F0 0000, perform the following steps to see if a camera is smart features capable:

1. Write the quadlet data 0x0030 533B to 0xFFFF F2F0 0000
2. Write quadlet data 0x73C3 F000* to 0xFFFF F2F0 0004
3. Read quadlet data from 0xFFFF F2F0 0000 and 0xFFFF F2F0 0004. If at least one of the read operations returns a value that is not equal to 0xFFFF FFFF, the camera supports smart features. If both read operations return 0xFFFF FFFF, the camera does not support smart features.

Note that instead of performing two single quadlet write operations, a block write can be performed.

* The last three zeros in this quadlet represent a timeout value. When the time out value is "000" as it is on the A620f, it means that advanced features are always available.

6.5.2 Determining the Address of a Smart Feature's CSR

The control and status register (CSR) for each smart feature is identified by a 128 bit Globally Unique Identifier (GUID). GUIDs are also known as UUIDs (Universal Unique Identifier).

A GUID consists of:

- One 32 bit number (D1)
- Two 16 bit numbers (D2, D3)
- A sequence of 8 bytes (D4[0] - D4[7])

GUID example:

CA8A916A - 14A4 - 4D8E - BBC9 - 93DF50495C16

(D1) (D2) (D3) (D4[0] - D4[1]) (D4[2] - D4[7])

Section 6.7 describes the standard smart features available on **A620f** cameras. Each smart feature description includes the GUID assigned to the feature's CSR.

To determine the starting address of a smart feature's CSR, the feature's CSR GUID must be written to the Smart Features Inquiry register. The Smart Features Inquiry register's offset relative to the Advanced Features Access Control Register is 0x10. If the camera recognizes the GUID as the CSR GUID for an implemented smart feature, the address of CSR for the feature can be read from the Smart Features Address Register at offset 0x20. If the feature isn't supported by the device, a value of 0x0 will be read from the Smart Features Address Register.

Smart Features Inquiry Register Layout

	Bit			
Offset	0-7	8-15	16-23	24-31
10h	D1			
14h	D3		D2	
18h	D4[3]	D4[2]	D4[1]	D4[0]
1ch	D4[7]	D4[6]	D4[5]	D4[4]

Smart Features Address Register Layout

	Bit			
Offset	0-7	8-15	16-23	24-31
20h	Address Low			
24h	Address High			

Example

Determine the address of the “CRC Checksum” smart feature which has a CSR GUID of:

3B34004E - 1B84 - 11D8 - 83B3 - 00105A5BAE55

D1: 0x3B34 004E

D2: 0x1B84

D3: 0x11D8

D4[0]: 0x83

D4[1]: 0xB3

D4[2]: 0x00

D4[3]: 0x10

D4[4]: 0x5A

D4[5]: 0x5B

D4[6]: 0xAE

D4[7]: 0x55

Step 1: Write the CSR GUID to the Smart Features Inquiry register

Assuming that the address for the Access Control register is 0xFFFF F2F0 0000, perform the following quadlet write operations to the Smart Features Inquiry register

a. Write quadlet data 0x3B34 004E to 0xFFFF F2F0 0010 (D1)

b. Write quadlet data 0x11D8 1B84 to 0xFFFF F2F0 0014 (D3 | D2)

c. Write quadlet data 0x1000 B383 to 0xFFFF F2F0 0018 (D4[3] | D[0])

d. Write quadlet data 0x55AE 5B5A to 0xFFFF F2F0 001C (D4[7] | D[4])

Instead of performing four quadlet write operations, one block write operation can be performed.

Step 2: Read the start address for the smart feature from the Smart Feature Address register

a. Read quadlet data from 0xFFFF F2F0 0020 (Address Low)

b. Read quadlet data from 0xFFFF F2F0 0024 (Address High)

If both Address Low and Address High return zero, the camera doesn’t support the CRC checksum feature. Assuming the read operations yielded Address Low = 0xF2F0 0038 and Address High = 0x0000 FFFF, the CRC Checksum feature CSR’s address is 0xFFFF F2F0 0038.

6.5.3 Enabling and Parameterizing a Smart Feature

Once you have determined the starting address of the control and status register (CSR) for your desired smart feature, you are ready to enable and parameterize the feature by setting bits within the CSR.

Section 6.7 describes the standard smart features available on **A620f** cameras. Each smart features description includes an explanation of what the feature does and an explanation of the parameters associated with the feature. The descriptions also include a detailed layout of how the bits contained within the feature's CSR relate to the parameters for the feature. After reading the description of your desired smart feature, you can enable and parameterize the feature by setting the appropriate bits within the CSR.

6.6 Getting Smart Features Results

In many cases, activating a smart feature results in additional data that must be transmitted by the camera, i.e., the results of the smart feature. The results of a smart feature will be appended to the image data so that each frame contains both image data and smart features results.

Before using any of the smart features that add information to the image data, the extended data stream feature must be enabled. The extended data stream is in itself a smart feature. When the extended data stream feature is enabled, information such as the height of the image, the width of the image, and the AOI size is added to each image's basic pixel data. Disabling the extended data stream feature switches off all smart features that add information to the image data stream.

The extended data stream feature and any other smart features which add information to the image data stream will only work when the camera is set for video Format 7. For other video formats, enabling the extended data stream feature or any of the other smart features that normally add data to the image stream does not affect the image data stream; the camera only sends the basic image data without any added information.

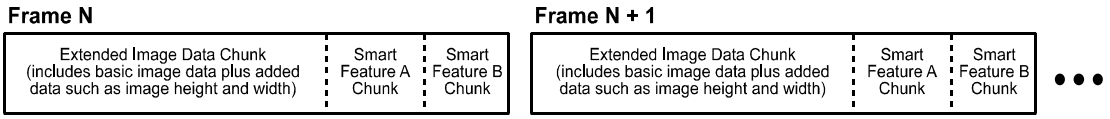


Figure 6-1: Image Data Stream with Smart Features Enabled

As illustrated in Figure 6-1, when smart features are enabled, each image frame consists of "chunks." For example, the frame may include a chunk which contains the extended image data (the basic image data plus the added height, width, etc. information), a chunk which contains the results for the frame counter smart feature, a chunk which contains the results for the cycle time stamp smart feature, etc. Table 6-1 describes the general structure of a chunk.

Position	Name	Description
0	Data [K Bytes]	The data that the chunk is transporting.
K	Chunk GUID [16 Bytes]	Identifies the type of chunk and the smart feature associated with the chunk. (Note that a smart feature's chuck GUID is not the same as its CSR GUID.)
K+16	Length [4 Bytes]	The chunk's total length in bytes.
K+20	Inverted Length [4 Bytes]	The bitwise complement of the length.

Table 6-1: General Structure of a Chunk

Each chunk ends with a four byte unsigned integer indicating the length of the chunk and four bytes which indicate the bitwise complement of the length. Transferring both the chunk length and the bitwise complement of the length serves as a mechanism to detect transmission errors. If the last four bytes of a chunk aren't the bitwise complement of the preceding four bytes, the chunk's length information isn't valid and this indicates that a transmission error occurred.

There are different types of chunks, for example, the chunk that is added when the cycle time stamp smart feature is enabled and the chunk that is added when the frame counter smart feature is enabled. Although most chunks follow the general structure described in Table 6-1, each type of chunk has unique aspects to its layout. To allow you to distinguish between the chunks, each chunk carries a “chunk GUID”. The GUID for each chunk is transferred just before the chunk’s length information. If you look through the descriptions of the smart features in Section 6.7, you will notice that for smart features which add a chunk to the image data stream, there is a description of the layout of the chunk and the chunk GUID associated with the chunk.

A chunk’s length field contains the chunk’s total length in bytes. The GUID, the length, and the inverted length are included as part of the total chunk length.

By appending length information and a chunk GUID to each chunk, the camera sends a self-describing data stream and allows easy navigation through the individual chunks that make up a complete image data frame.

Don’t confuse CSR GUIDs with chunk GUIDs:

- Each smart feature has a control and status register (CSR) associated with it and each CSR has a unique “CSR GUID” assigned to the register. The CSR GUIDs are used to help you keep track of which CSR is associated with each smart feature.
- Any smart feature that adds a “chunk” of data to the image data stream also has a unique “chunk GUID” assigned to the feature. The chunk GUID will be included the chunk of data that a smart feature adds to the image data. The chunk GUIDs let you determine which smart feature is associated with each added chunk in the image data stream.

The CRC Checksum is an exception to the general structure of a chunk. See Section 6.7.5 for more information.

6.6.1 How Big a Buffer Do I Need?

When smart features that add data to the image are enabled, the size of each transmitted frame will be larger than you would normally expect for a frame which contains only image data. To determine the size of the buffer that you will need to hold an image with appended smart features data, check the Total Bytes High Inquiry and Total Bytes Low Inquiry registers of the Format 7 mode you are currently using. Make sure to check these registers after all smart features have been enabled and all other settings affecting the image size have been completed. The size information in these registers will allow you to properly set up buffers to receive the transmitted images.

6.7 Standard Smart Features on the A620f

6.7.1 Extended Data Stream

The extended data stream feature has two functions:

- When it is enabled, information such as image height, image width, and AOI size is added to the basic pixel data for each image.
- It must be enabled before you can use any other smart feature that adds information to the image data stream.

With the extended data stream feature enabled, the basic pixel data for each image and the added information such as the image height and width are included in an “extended data chunk”. Refer to the extended data chunk layout below for a complete description of the information included in the extended data chunk.

The extended data stream feature must be enabled in order to use any of the other smart feature that adds information to the image data stream. Disabling the extended data stream feature switches off all smart features that add information to the image data stream.

The extended data stream feature and any other smart features which add information to the image data stream will only work when the camera is set for video Format 7.

Control and Status Register for the Extended Data Stream Feature

Register Name:	Extended Data Stream	
Address:	See “Determining the Address of Smart Features CSRs” on page 6-4.	
CSR GUID:	4E7ABCB0 - 1B84 - 11D8 - 9651 - 00105A5BAE55	
Field	**Bit**	**Description**
Presence Inq (Read only)	0	Presence of this feature 0: Not Available 1: Available
----	1 ... 30	Reserved
Enable (Read / write)	31	Enable / Disable this feature 0: Disable 1: Enable

Extended Data Chunk Layout

Position	**Name**	**Description**
0	Pixel Data [K Bytes]	The pixel data from the captured image
K	Gap [M Bytes]	For technical reasons, there might be a gap between the pixel data and the other data in the extended image data.

K + M	Stride [4 Bytes]	Signed integer. Indicates the number of bytes needed to advance from the beginning of one row in an image to the beginning of the next row.
K + M + 4	Reserved [3 Bytes]	-----
K + M + 7	Data Depth [1 Byte]	Effective data depth in bits of the pixels in the image.
K + M + 8	Top [2 Bytes]	Y coordinate of the top left corner of the current area of interest (AOI).
K + M + 10	Left [2 Bytes]	X coordinate of the top left corner of the current AOI.
K + M + 12	Height [2 Bytes]	Height in pixels of the current AOI.
K + M + 14	Width [2 Bytes]	Width in pixels of the current AOI.
K + M + 16	Reserved [3 Bytes]	-----
K + M + 19	Color Coding ID [1 Byte]	Color coding ID which describes the pixel data format. See Section 3.12 and page 4-30.
K + M + 20	Reserved [3 Bytes]	-----
K + M + 23	Color Filter ID [1 Byte]	For color cameras, describes the orientation of the color filter to the current AOI. Not used on A620f cameras.
K + M + 24	Chunk GUID [16 Bytes]	94ED7C88 - 1C0F - 11D8 - 82E0 - 00105A5BAE55
K + M + 40	Chunk Length [4 Bytes]	This chunk's total length in bytes.
K + M + 44	Inverted Chunk Length [4 Bytes]	The bitwise complement of the chunk length.

6.7.2 Frame Counter

The frame counter feature numbers images sequentially as they are captured. The counter starts at 0 and wraps at 4294967296 (operating continuously at 100 frames per second, it would take the counter about 500 days to wrap). The counter increments by one for each captured frame. Whenever the camera is powered off, the counter will reset to 0.

Note that if the camera is in continuous shot mode and continuous capture is stopped, up to two numbers in the counting sequence may be skipped. This happens due to the internal image buffering scheme used in the camera.

The extended data stream feature (see Section 6.7.1) must be enabled in order to use the frame counter feature or any of the other smart feature that adds information to the image data stream. Disabling the extended data stream feature switches off all smart features that add information to the image data stream.

The frame counter feature will only work when the camera is set for video Format 7.

Control and Status Register for the Frame Counter Feature

Register Name:	Frame Counter	
Address:	See “Determining the Address of Smart Features CSRs” on page 6-4.	
CSR GUID:	4433C4A4 - 1B84 - 11D8 - 86B2 - 00105A5BAE55	
Field	**Bit**	**Description**
Presence Inq (Read only)	0	Presence of this feature 0: Not Available 1: Available
----	1 ... 30	Reserved
Enable (Read / write)	31	Enable / Disable this feature 0: Disable 1: Enable

Frame Counter Chunk Layout

Position	Name	Description
0	Counter [4 Bytes]	The frame counter.
4	Chunk GUID [16 Bytes]	8C5DB844 - 1C0F - 11D8 - 965F - 00105A5BAE55
20	Chunk Length [4 bytes]	This chunk’s total length in bytes.
24	Inverted Chunk Length [4 bytes]	The bitwise complement of the chunk length.

6.7.3 Cycle Time Stamp

The cycle time stamp feature adds a chunk to each image frame containing the value of the counters for the IEEE 1394 bus cycle timer. The counters are sampled at the start of exposure of each image.

The extended data stream feature (see Section 6.7.1) must be enabled in order to use the cycle time stamp feature or any of the other smart feature that adds information to the image data stream. Disabling the extended data stream feature switches off all smart features that add information to the image data stream.

The cycle time stamp feature will only work when the camera is set for video Format 7.

Control and Status Register for the Cycle Time Stamp Feature

Register Name:	Cycle Time Stamp	
Address:	See “Determining the Address of Smart Features CSRs” on page 6-4.	
CSR GUID:	5590D58E - 1B84 - 11D8 - 8447 - 00105A5BAE55	
Field	**Bit**	**Description**
Presence Inq (Read only)	0	Presence of this feature 0: Not Available 1: Available
----	1 ... 30	Reserved
Enable (Read / write)	31	Enable / Disable this feature 0: Disable 1: Enable

Cycle Time Stamp Chunk Layout

Position	**Name**	**Description**		
0	Cycle Time Stamp [4 Bytes]	**Field**	**Bit**	**Description**
		Second Count	0 ... 6	Counts the seconds. Wraps to zero after 127 seconds.
		Cycle Count	7 ... 19	Counts the 125 µs isochronous bus cycles. Wraps to zero after counting to 7999.
		Cycle Offset	20 ... 31	Counts at 24.576 MHz and wraps to zero after counting to 3071 (resulting in a 125 µs cycle)
4	Chunk GUID [16 Bytes]	994DD430 - 1C0F - 11D8 - 8F6B - 00105A5BAE55		
20	Chunk Length [4 Bytes]	This chunk’s total length in bytes.		
24	Inverted Chunk Length [4 Bytes]	The bitwise complement of the chunk length.		

6.7.4 DCAM Values

The DCAM values feature adds a chunk to each image frame containing the current settings for some standard DCAM features. The settings are sampled at the start of exposure of each image.

The extended data stream feature (see Section 6.7.1) must be enabled in order to use the DCAM values feature or any of the other smart feature that adds information to the image data stream. Disabling the extended data stream feature switches off all smart features that add information to the image data stream.

The DCAM values feature will only work when the camera is set for video Format 7.

Control and Status Register for the DCAM Values Feature

Register Name:	DCAM Values	
Address:	See “Determining the Address of Smart Features CSRs” on page 6-4.	
CSR GUID:	494DE528 - 1B84 - 11D8 - 8A0C - 00105A5BAE55	
Field	**Bit**	**Description**
Presence Inq (Read only)	0	Presence of this feature 0: Not Available 1: Available
----	1 ... 30	Reserved
Enable (Read / write)	31	Enable / Disable this feature 0: Disable 1: Enable

DCAM Values Chunk Layout

Position	Name	Description		
0	Gain CSR [4 Bytes]	Content of the DCAM Gain CSR		
		Field	**Bit**	**Description**
		Presence Inq	0	Presence of this feature If 0, the DCAM feature is not available and all of its values should be ignored
		Abs Control	1	Absolute control mode If 1, the DCAM feature is in absolute control mode and the current value can be read from the Absolute Value CSR. Otherwise, the Value field holds the current raw value setting.
		-----	2 ... 4	reserved
		One Push	5	If 1, a one push operation was in progress.
		ON OFF	6	0: The feature was disabled, ignore the value 1: The feature was enabled
		A/M Mode	7	0: The feature was in manual control mode 1: The feature was in auto control mode
		--	8 ... 19	Reserved
		Value	20 ... 31	Value of the feature
4	Gain Absolute Value CSR [4 Bytes]	**Field**	**Bit**	**Description**
		Abs Value	0 ... 31	Floating point value with IEEE/real*4 format Unit: dB
8	Shutter CSR [4 bytes]	Content of the DCAM Shutter CSR Same layout as the GAIN CSR		
12	Shutter Absolute Value CSR [4 Bytes]	**Field**	**Bit**	**Description**
		Abs Value	0 ... 31	Floating point value with IEEE/real*4 format Unit: seconds
16	Gamma CSR [4 bytes]	Content of the DCAM Gamma CSR Same layout as the Gain CSR		
20	Gamma Absolute Value CSR [4 Bytes]	**Field**	**Bit**	**Description**
		Abs Value	0 ... 31	Floating point value with IEEE/real*4 format Unit: dB

24	White Balance CSR [4 Bytes]	Content of the DCAM White Balance CSR		
		Field	**Bit**	**Description**
		Presence Inq	0	Presence of this feature If 0, the DCAM feature is not available and all of its values should be ignored
		Abs Control	1	Absolute control mode If 1, the DCAM feature is in absolute control mode and the current value can be read from the Absolute Value CSR. Otherwise, the Value field holds the current raw value setting.
		-----	2 ... 4	reserved
		One Push	5	If 1, a one push operation was in progress.
		ON OFF	6	0: The feature was disabled, ignore the value 1: The feature was enabled
		A/M Mode	7	0: The feature was in manual control mode 1: The feature was in auto control mode
		Blue Value	8 ... 19	Blue value
		Red Value	20 ... 31	Red Value
28	White Balance Absolute Value CSR [4 Bytes]	**Field**	**Bit**	**Description**
		Abs Value	0 ... 31	Floating point value with IEEE/real*4 format Unit: K (Kelvin)
32	Brightness CSR [4 bytes]	Content of the DCAM Brightness CSR Same layout as the Gain CSR		
36	Brightness Absolute Value CSR [4 Bytes]	**Field**	**Bit**	**Description**
		Abs Value	0 ... 31	Floating point value with IEEE/real*4 format Unit: %
40	Chunk GUID [16 Bytes]	911C8982 - 1C0F - 11D8 - 8AF0 - 00105A5BAE55		
56	Chunk Length [4 bytes]	This chunk's total length in bytes.		
60	Inverted Chunk Length [4 bytes]	The bitwise complement of the chunk length.		

6.7.5 CRC Checksum

The CRC (Cyclic Redundancy Check) Checksum feature adds a chunk to each image frame containing a 16 bit CRC checksum calculated using the Z-modem method. The CRC Checksum chunk is always the last chunk added to the image data stream and the chunk is always 32 bits in size. As shown in Figure 6-2, the checksum is calculated using all of the image data and all of the appended chunks except for the checksum itself.

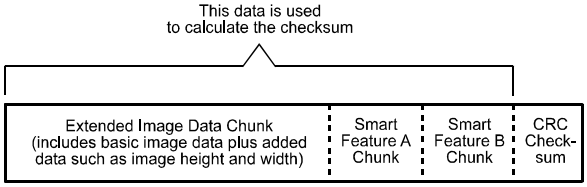


Figure 6-2: Data Used for the Checksum Calculation

The extended data stream feature (see Section 6.7.1) must be enabled in order to use the CRC Checksum feature or any of the other smart feature that adds information to the image data stream. Disabling the extended data stream feature switches off all smart features that add information to the image data stream.

The CRC Checksum feature will only work when the camera is set for video Format 7.

The data transmission method used on **A620f** cameras is extremely reliable. The CRC Checksum feature is included on the camera because CRC checksums are so commonly used with data transmission applications.

Control and Status Register for the CRC Checksum Feature

Register Name:	CRC Checksum	
Address:	See “Determining the Address of Smart Features CSRs” on page 6-4.	
CSR GUID:	3B34004E - 1B84 - 11D8 - 83B3 - 00105A5BAE55	
Field	**Bit**	**Description**
Presence Inq (Read only)	0	Presence of this feature 0: Not Available 1: Available
----	1 ... 30	Reserved
Enable (Read / write)	31	Enable / Disable this feature 0: Disable 1: Enable

CRC Checksum Chunk Layout

The CRC checksum is an exception to the normal chunk structure. The CRC chunk is always 32 bits wide and is always the last chunk appended to the image data. The lower 16 bits of the chunk are filled with the checksum and the upper 16 bits of the chunk are filled with zeros.

Bit	Description
0 ... 7	CRC Checksum low byte
8 ... 15	CRC Checksum high byte
16 ... 23	0x00
24 ... 31	0x00

Using the Checksum to Check the Data Integrity

When the checksum smart feature is enabled, the following two C functions can be used to check if an acquired frame contains a valid CRC checksum. The user must pass the acquired image buffer and the buffer's length in bytes to the CheckBuffer() function. The CheckBuffer() function uses the CRC16() function to calculate the checksum.

These two samples are intended to aid you in developing the code for your application. They are provided solely as examples.

```
/** \brief Calculates a 16 bit CRC checksum
  * \param pData Pointer to the data buffer
  * \param nbyLength Size of the buffer in bytes
  * \return The CRC checksum
  */
unsigned short CRC16(const unsigned char *pData, unsigned long nbyLength )
{
      unsigned long i, j, c, bit;
      unsigned long crc = 0;
      for (i=0; i<nbyLength; i++) {
            c = (unsigned long)*pData++;
            for (j=0x80; j; j>>=1) {
                  bit = crc & 0x8000;
                  crc <<= 1;
                  if (c & j) bit^= 0x8000;
                  if (bit) crc^= 0x1021;
            }
      }
      return (unsigned short) (crc & 0xffff);
}
```

```
/** \brief Verifies a frame buffer's CRC checksum
  * \param pData Pointer to the frame
  * \param nbyLength Size of frame in bytes
  * \return 1, if the check succeeds, 0 otherwise
  */
int CheckBuffer(const unsigned char* pData, unsigned long nbyLength )
{
      unsigned long nCurrentCRC, nDesiredCRC;
      /* Calculate the CRC checksum of the buffer. Don't take the last four bytes
         containing the checksum into account */
      nCurrentCRC = CRC16(pData, nbyLength - sizeof( unsigned long ) );
      /* Retrieve the desired CRC value from the data buffer */
      nDesiredCRC =  ((unsigned long*) pData)[ nbyLength / sizeof ( unsigned long ) - 1];
      /* Return TRUE if they are equal */
      return nCurrentCRC == nDesiredCRC;
}
```

6.7.6 Test Images

A620f cameras include a test image mode as a smart feature. The test image mode is used to check the camera's basic functionality and its ability to transmit an image via the video data cable. The test image mode can be used for service purposes and for failure diagnostics. In test mode, the image is generated with a software program and the camera's digital devices and does not use the optics, the CMOS pixel array, or the ADCs. Test images one, two, and three are available on all **A620f** cameras.

When a test image is active, the gain, brightness, and exposure time have no effect on the image.

The test image smart feature does not add information to the image data stream and can be enabled even when the extended data stream feature (see Section 6.7.1) is disabled.

The test image feature will work when the camera is set for any valid video format.

Test Image one

As shown in Figure 6-3, test image one consists of rows with several gray scale gradients ranging from 0 to 255. Assuming that the camera is operating at full 1280 x 1024 resolution and is set for a monochrome, 8 bit output mode, when the test images are generated:

- row 0 starts with a gray value of 1 for the first pixel,
- row 1 starts with a value of 2 for the first pixel,
- row 2 starts with a gray vale of 3 for the first pixel, and so on.

(If the camera is operating at a lower resolution when the test images are generated, the basic appearance of the test pattern will be similar to Figure 6-3, but the starting pixel values on each row will not be as described above.)

The mathematical expression for test image one is:

$$\text{grayvalue} = [\, x + y + 1 \,] \text{ MOD256}$$

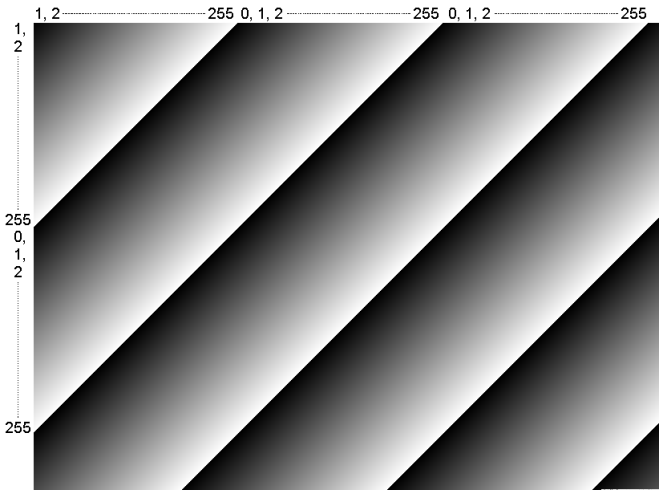


Figure 6-3: Test Image One

Test Image Two

As shown in Figure 6-4, test image two consists of rows with several gray scale gradients ranging from 0 to 255. Assuming that the camera is operating at full 1280 x 1024 resolution and is set for a monochrome, 8 bit output mode, when the test images are generated:

- rows 0, 1, and 2 start with a gray value of 0 for the first pixel,
- rows 3, 4, 5, and 6 start with a gray value of 1 for the first pixel,
- rows 7, 8, 9, and 10 start with a gray value of 2 on the first pixel, and so on.

(If the camera is operating at a lower resolution when the test images are generated, the basic appearance of the test pattern will be similar to Figure 6-4, but the staring pixel values on each row will not be as described above.)

The mathematical expression for test image two is:

$$\text{grayvalue} = \frac{[x + y + 1]}{4} \text{ MOD } 256, \quad \text{round off all values}$$

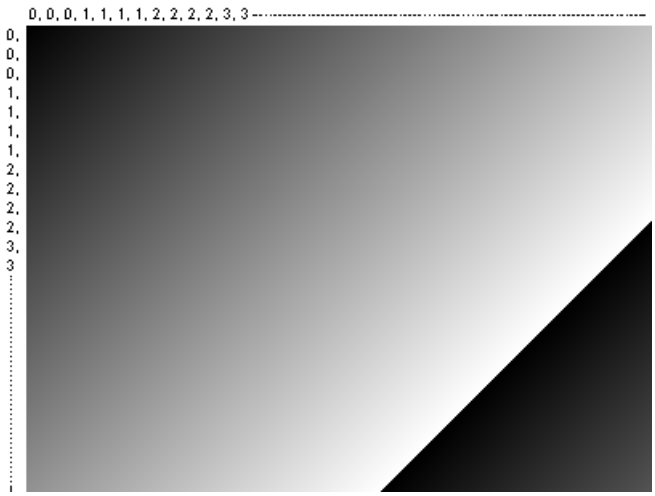


Figure 6-4: Test Image Two

Test Image Three

Test image three is similar to test image one but it is not stationary. The image moves by 1 pixel from right to left whenever a one-shot or a continuous-shot command signal is sent to the camera.

Control and Status Register for the Test Image Feature

Register Name:	Test Images	
Address:	See “Determining the Address of Smart Features CSRs” on page 6-4.	
CSR GUID:	2A411342 - C0CA - 4368 - B46E - EE5DEEBF0548	
Field	**Bit**	**Description**
Presence Inq (Read only)	0	Presence of this feature 0: Not Available 1: Available
-----	1 ... 7	Reserved
Image Inq 1 (Read only)	8	Presence of test image 1 0: Not Available 1: Available
Image Inq 2 (Read only)	9	Presence of test image 2 0: Not Available 1: Available
Image Inq 3 (Read only)	10	Presence of test image 3 0: Not Available 1: Available
Image Inq 4 (Read only)	11	Presence of test image 4 0: Not Available 1: Available
Image Inq 5 (Read only)	12	Presence of test image 5 0: Not Available 1: Available
Image Inq 6 (Read only)	13	Presence of test image 6 0: Not Available 1: Available
Image Inq 7 (Read only)	14	Presence of test image 7 0: Not Available 1: Available
-----	15	Reserved
Image On (Read / write)	16 ... 18	0: No test image active 1: Test image 1 active 2: Test image 2 active 3: Test image 3 active
-----	19 ... 31	Reserved

6.7.7 Extended Version Information

A620f cameras include a register that contains version numbers for the camera's internal software. For troubleshooting purposes, Basler technical support may ask you to read this register and to supply the results.

The extended version information smart feature does not add information to the image data stream and can be accessed even when the extended data stream feature (see Section 6.7.1) is disabled.

The extended version feature will work when the camera is set for any valid video format.

Control and Status Register for the Extended Version Information Feature

Register Name:	Extended Version Information	
Address:	See "Determining the Address of Smart Features CSRs" on page 6-4.	
CSR GUID:	2B2D8714 - C15E - 4176 - A235 - 6EF843D747B4	
Field	**Bit**	**Description**
Presence Inq (Read only)	0	Presence of this feature 0: Not Available 1: Available
-----	1 ... 7	Reserved
Length	8 ... 15	Specifies the length in quadlets of the "string" field.
-----	16 ... 31	Reserved
Version Info	n Bytes	An ASCII character string that includes the version numbers for the camera's internal software. The length of this string field is equal to the number of quadlets given in the "length" field above.

The ASCII character string in the Version Info field contains the camera's "firmware ID" number. You can read the string to determine your camera's firmware ID. The ID number's position in the string is described in Section 1.1.

6.7.8 Lookup Table

A620f cameras have a sensor that provides pixel data at 12 bit depth. Internally, the camera has a processing block that uses the 12 bit data to perform image correction functions and to perform the gain and offset functions. The output from the processing block is 10 bit pixel data. As mentioned in Section 3.8, the camera can be set to transmit the output from the processing block at either 10 bit depth or at 8 bit depth.

When the camera is set for 8 bit pixel depth, it normally just drops the two least significant bits (LSBs) for each pixel and only transmits pixel data at 8 bit depth. The **A620f** includes a smart feature that lets you use a custom lookup table to map the 10 bit pixel values output from the processing block to the 8 bit values that will be transmitted from the camera rather than just dropping the two LSBs. The lookup table is essentially just a list of 1024 values. Each value in the table represents the 8 bit value that will be transmitted out of the camera when the processing block reports a particular 10 bit value for a pixel. The first number in the table represents the 8 bit value that will be transmitted out of the camera when the processing block reports that a pixel has a value of 0. The second number in the table represents the 8 bit value that will be transmitted out of the camera when the processing block reports that a pixel has a value of 1. The third number in the table represents the 8 bit value that will be transmitted out of the camera when the processing block reports that a pixel has a value of 2. And so on.

The advantage of the lookup table feature is that it allows the user to customize the response curve of the camera. The graphs below represent the contents of two typical lookup tables. The first graph is for a lookup table where the values are arranged so that the output of the camera increases linearly as the sensor output increases. The second graph is for a lookup table where the values are arranged so that the camera output increases quickly as the sensor output moves from 0 through 511 and increases gradually as the sensor output moves from 512 through 1023.

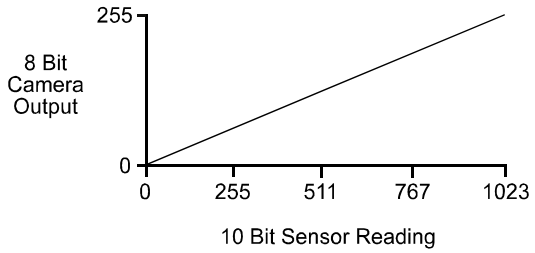


Figure 6-5: LUT with Values Mapped in a Linear Fashion

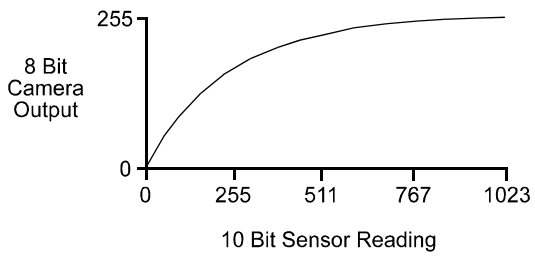


Figure 6-6: LUT with Values Mapped for Higher Camera Output at Low Sensor Readings

Please look at the next page and examine the layout of the control and status register for the lookup table smart feature. You will notice that the first two quadlets of the register include bits that allow you to check for this feature's presence and to enable or disable the feature. These initial two quadlets are followed by 1024 quadlets. The 1024 quadlets contain the values that make up the customized lookup table.

The lookup table smart feature can only be used when the camera is set to output pixel data at 8 bit depth.

The camera's processing block provides the 10 bit depth pixel values that will be input into the lookup table. Since the processing block performs the camera's gain and offset functions, the gain and offset settings will affect the image even when the lookup table smart feature is enabled.

When the lookup table feature is enabled, the maximum allowed gain setting is 740 (0x2E4). However, we strongly recommend that when using the lookup table feature, you limit the gain setting to a maximum of 125 (0x07D). Setting the gain to 125 or less guarantees that the full range of 10 bit input values will be available for mapping to 8 bit values.

The lookup table smart feature does not add information to the image data stream and can be accessed even when the extended data stream feature (see Section 6.7.1) is disabled.

When you enable the lookup table feature, the 1024 quadlets that represent the lookup table are automatically populated with default values. If you want use a customized lookup table you must:

1. Use the Control and Status Register (CSR) for the lookup table feature to enable the feature.
2. Use the lookup table CSR to load the values for the customized lookup table.

The lookup table feature will work when the camera is set for any valid video format.

Control and Status Register for the Lookup Table Feature

Register Name:	Lookup Table		
Address:	See “Determining the Address of Smart Features CSRs” on page 6-4.		
CSR GUID”	B28C667C - DF9D - 11D7 - 8693 - 000C6E0BD1B0		
Position	**Field**	**Bit**	**Description**
0	Presence Inq (Read only)	0	Presence of this feature 0: Not Available 1: Available
	-----	1 ... 30	Reserved
	Enable (Read / write)	31	Enable / Disable this feature 0: Disable 1: Enable
4	In Depth Inq (Read only)	0 ... 15	Bit depth of the pixel data reported by the sensor.
	Out Depth Inq (Read only)	16 ... 31	Bit depth of the pixel data transmitted from the camera.
8	Quadlet 0 (Read / write)	1 Quadlet	Defines the 8 bit value that will be transmitted from the camera when the 10 bit pixel value from the sensor is 0. (The 8 LSBs of the quadlet carry the data for the field. The 24 MSBs are all zeros.)
12	Quadlet 1 (Read / write)	1 Quadlet	Defines the 8 bit value that will be transmitted from the camera when the 10 bit pixel value reported from the sensor is 1.
16	Quadlet 2 (Read / write)	1 Quadlet	Defines the 8 bit value that will be transmitted from the camera when the 10 bit pixel value reported from the sensor is 2.
•	•	•	•
•	•	•	•
•	•	•	•
4096	Quadlet 1022 (Read / write)	1 Quadlet	Defines the 8 bit value that will be transmitted from the camera when the 10 bit pixel value reported from the sensor is 1022.
4100	Quadlet 1023 (Read / write)	1 Quadlet	Defines the 8 bit value that will be transmitted from the camera when the 10 bit pixel value reported from the sensor is 1023.

Using the SFF Viewer to Upload a Lookup Table

The Configurator window in the Basler SFF Viewer (see Section 6.4) includes an *Upload* button that can be used to easily load a file containing a customized lookup table into the camera. The file must be plain text and must be formatted correctly. The file must have 1024 lines with each line containing two comma-separated values. The first value on each line represents a 10 bit pixel reading from the sensor and the second value represents the corresponding 8 bit output that will be transmitted from the camera.

The sample below shows part of a typical text file for a lookup table. Assuming that you have enabled the lookup table feature on your camera and used the *Upload* button to load a file similar to the sample into the camera:

- If the sensor reports that a pixel has a value of 1, the camera will output a value of 0.
- If the sensor reports that a pixel has a value of 6, the camera will output a value of 1.
- If the sensor reports that a pixel has a value of 1019, the camera will output a value of 254.

```
0,0
1,0
2,0
3,0
4,1
5,1
6,1
7,1
8,2
9,2
10,2
11,2
12,3
13,3
14,3
15,3
16,4
17,4
18,4
19,4
20,5
21,5
...
1010,252
1011,252
1012,253
1013,253
1014,253
1015,253
1016,254
1017,254
1018,254
1019,254
1020,255
1021,255
1022,255
1023,255
```

Figure 6-7: Sample Text File for Use With *Upload* Button

6.7.9 Trigger Flag and Trigger Counter

A620f cameras include a trigger flag and trigger counter feature. The trigger counter increments by one each time an image capture is triggered regardless of whether the trigger is internal (one shot or continuous shot commands) or is external (hardware or software trigger). Triggers that occur when the camera is not ready are discarded and not counted. The trigger counter wraps to zero after 65535 is reached.

If one or more triggers has been detected since the last time the Trigger Flag field was read, the trigger flag is set to one. The flag self clears with each read access.

Writes to the Trigger Count or Trigger Flag fields are ignored.

The counter field or the flag field can be polled by your camera control software to detect the receipt of a trigger signal by the camera. The camera control software can react synchronously to each trigger signal received. By using the results of the polling to know when a trigger signal is received by the camera, you can eliminate the need for a hard wired signal from the hardware device that is issuing the trigger. Keep in mind that your degree of precision depends on your polling frequency and the 1394 bus latency.

The trigger flag and trigger counter smart feature does not add information to the image data stream and can be accessed even when the extended data stream feature (see Section 6.7.1) is disabled.

The trigger flag and counter feature is always enabled regardless of the video format.

Control and Status Register for the Trigger Flag and Counter Feature

Register Name:	Trigger Flag and Counter		
Address:	See “Determining the Address of Smart Features CSRs” on page 6-4.		
CSR GUID:	16C31A78 - 3F75 - 11D8 - 94EC - 00105A5BAE55		
Position	**Field**	**Bit**	**Description**
0	Presence Inq (Read only)	0	Presence of this feature 0: Not Available 1: Available
	-----	1 ... 15	Reserved
	Trigger Count (Read only)	16 ... 31	The trigger counter increments by one each time an image capture is triggered. The counter is reset at power on or when an initialize command is issued.
4	-----	0 ... 30	Reserved
	Trigger Flag (Read only)	31	The flag is set to 1 by each trigger. It is cleared by a read access to this register.

6.7.10 Output Port Configuration

A620f cameras are equipped with four physical output ports designated as Output Port 0, Output Port 1, Output Port 2, and Output Port 3. The output port configuration feature can be used to change the assignment of camera output signals (such as Integrate Enabled and Trigger Ready) to the physical output ports.

As shown on pages 6-29 and 6-30, there is a control and status register (CSR) for each physical output port. The Source Select field in each register is used to assign a camera signal to the associated output port. For example, the Source Select field in the register for Output Port 0 is used to assign a camera output signal to physical output port 0.

Each physical output port can be unassigned or it can have one and only one camera output signal assigned to it.

You can assign a camera output signal to more than one physical output port. For example, the Trigger Ready signal could be assigned to both physical output port 0 and physical output port 1.

The Source Select field can also be used to designate an output port as “user set.” If an output port is designated as user set, its state can be set to high or low by using the User Setting field in the CSR for the port.

The Invert field can be used to invert the signal before it is applied to the output port and the Monitor field can be used to check the current state of the output port.

When using the output port configuration feature, you should follow this sequence:

1. Read the Presence Inq field and the Source Select Inq field for the physical port you want to work with. Determine whether the port configuration feature is available for the port and if the source for the port is selectable.
2. Use the Source Select field to select a source for the output port.
(If you select “User set” as the source, the state of the physical output port may change when you set the bits in the Source Select field. This is an artifact of the camera design.)
3. Check the Monitor Inq, Invert Inq, and User Setting Inq fields. The state of these fields will tell you if the Monitor, Invert, and User Setting fields are available. (The availability of the Monitor, Invert, and User Setting fields will vary depending on the selected source.)
4. If the Invert field is available, set the field as desired.
5. If you selected “User set” as the source, use the User Setting field to set the state of the output as desired.
6. If the Monitor field is available, use the field as desired to check the current state of the output.

The output port configuration smart feature does not add information to the image data stream and can be accessed even when the extended data stream feature (see Section 6.7.1) is disabled.

The output port configuration feature is always enabled regardless of the video format.

By default, the Integrate Enabled signal is assigned to physical output port 0 and the Trigger Ready Signal is assigned to physical output port 1.

Control and Status Registers for the Output Port Configuration Feature

Register Name:	Output Port 0 Configuration		
Address:	See “Determining the Address of Smart Features CSRs” on page 6-4.		
CSR GUID:	5A889D7E - 41E5 - 11D8 - 845B - 00105A5BAE55		
Position	**Field**	**Bit**	**Description**
0	Presence Inq (Read only)	0	Presence of the output port 0 configuration feature 0: Not Available 1: Available
	Monitor Inq (Read only)	1	Presence of the monitor field 0: Not Available 1: Available
	Invert Inq (Read only)	2	Presence of the invert field 0: Not Available 1: Available
	User Setting Inq (Read only)	3	Presence of the user setting field 0: Not Available 1: Available
	-----	4 ... 26	Reserved
	Source Select (Read / write)	27 ... 31	Write a value to select a source signal for output port 0: 0: Integrate Enabled signal 1: Trigger Ready signal 3: User set (state can be set with the User Setting field described below) 4: Strobe
4	Source Select Inq (Read only)	0 ... 31	If bit *n* is set, then value *n* is valid for use in the Source Select field. For example, if bit 0 is set, then 0 is a valid value for use in the Source Select field. If bit 1 is set, then 1 is a valid value for use in the Source Select field. Etc.
8	-----	0 ... 30	Reserved
	Monitor (Read only)	31	Shows the current state of the output: 0: Low (non-conducting) 1: High (conducting)
12	-----	0 ... 30	Reserved
	Invert (Read / write)	31	Enables signal inversion: 0: Do not invert 1: Invert
16	-----	0 ... 30	Reserved
	User Setting (Read / write)	31	If the Source Select field is set to “user set”, this field sets the state of the output: 0: Low (non-conducting) 1: High (conducting) (Sets the state of the output before the inverter.)
20	-----	0 ... 31	Reserved

Register Name:	Output Port 1 Configuration		
Address:	See “Determining the Address of Smart Features CSRs” on page 6-4?.		
CSR GUID:	949D820A - 4513 - 11D8 - 9EB1 - 00105A5BAE55		
Position	**Field**	**Bit**	**Description**
0	Same as port 0.		
4	Same as port 0.		
8	Same as port 0.		
12	Same as port 0.		
16	Same as port 0.		
20	Same as port 0.		

Register Name:	Output Port 2 Configuration		
Address:	See “Determining the Address of Smart Features CSRs” on page 6-4.		
CSR GUID:	C14E5072 - 4513 - 11D8 - 81F3 - 00105A5BAE55		
Position	**Field**	**Bit**	**Description**
0	Same as port 0.		
4	Same as port 0.		
8	Same as port 0.		
12	Same as port 0.		
16	Same as port 0.		
20	Same as port 0.		

Register Name:	Output Port 3 Configuration		
Address:	See “Determining the Address of Smart Features CSRs” on page 6-4.		
CSR GUID:	E79233CA - 4513 - 11D8 - 9B9A - 00105A5BAE55		
Position	**Field**	**Bit**	**Description**
0	Same as port 0.		
4	Same as port 0.		
8	Same as port 0.		
12	Same as port 0.		
16	Same as port 0.		
20	Same as port 0.		

6.8 Customized Smart Features

The Basler **A620f** has significant processing capabilities and Basler can accommodate customer requests for customized smart features. A great advantage of the smart features framework is that it serves as a standardized platform for parameterizing any customized smart feature and for returning the results from the feature.

The Basler camera development team is ready and able to handle requests for customized smart features. The cost to the customer for adding a customized smart feature to the **A620f** will depend on the complexity of algorithm, software, and firmware development, of incorporating the feature within the smart features framework, and of testing to ensure that the feature meets specifications. Please contact your Basler sales representative for more details about customized smart features.

7 Mechanical Considerations

The **A620f** camera housing is manufactured with high precision. Planar, parallel, and angular sides guarantee precise mounting with high repeatability.

Caution!

The camera is shipped with a cap on the lens mount. To avoid collecting dust on the sensor, make sure that at all times either the cap is in place or a lens is mounted on the camera.

7.1 Camera Dimensions and Mounting Facilities

The dimensions for **A620f** cameras are as shown in Figure 7-1.

A620f cameras are equipped with four M3 mounting holes on the bottom and two M3 mounting holes on the top as indicated in the drawings.

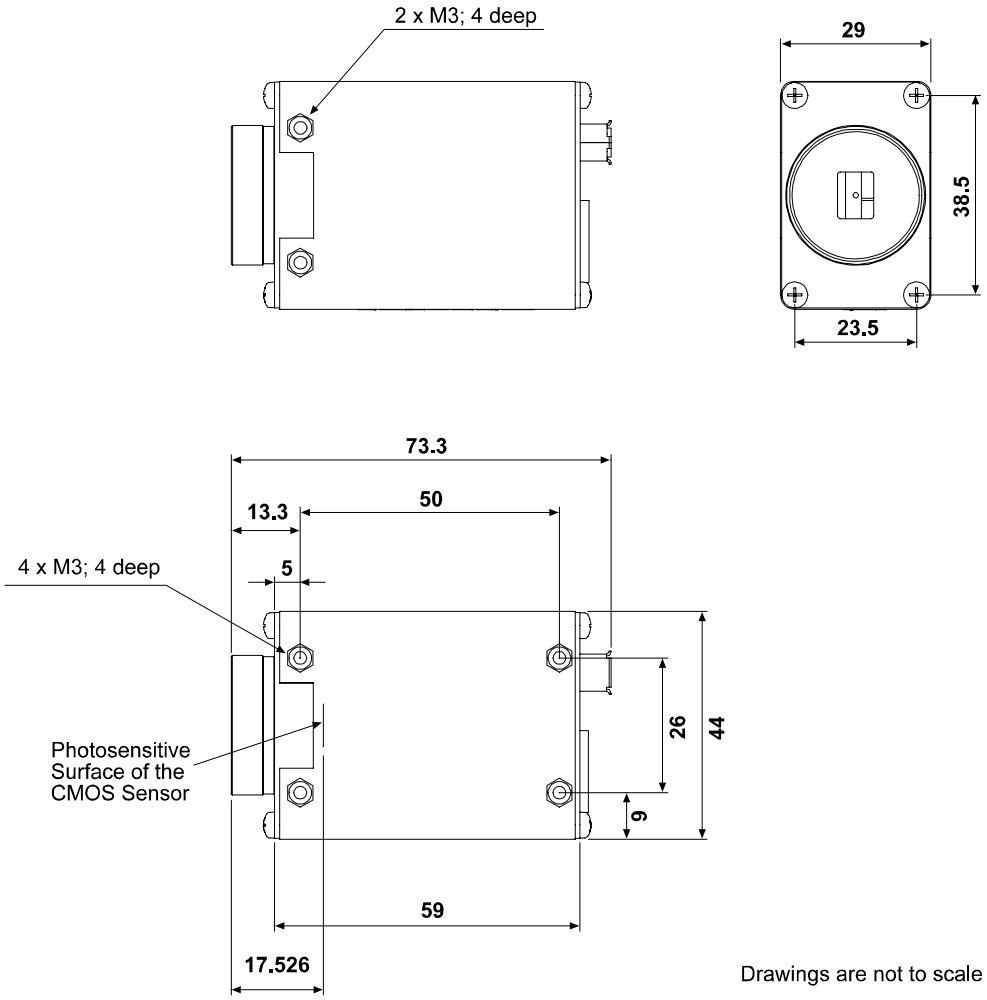


Figure 7-1: **A620f** Mechanical Dimensions (in mm)

7.2 Sensor Positioning Accuracy

The sensor positioning accuracy is as shown in Figure 7-2.

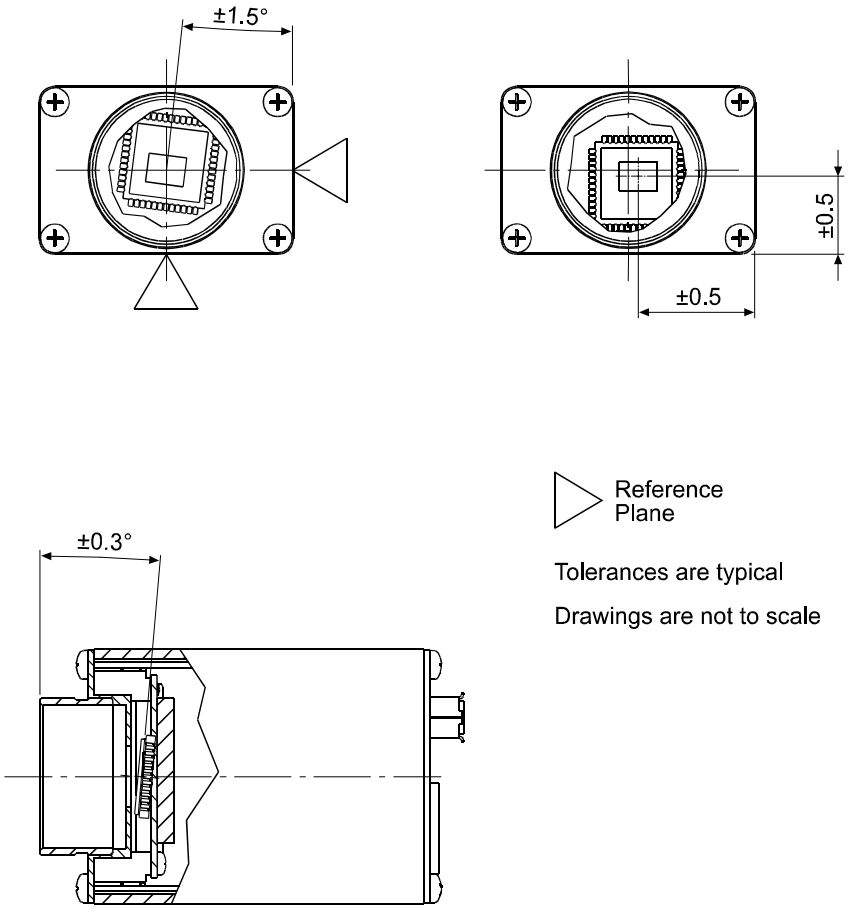


Figure 7-2: Sensor Positioning Accuracy (in mm or degrees)

Revision History

Doc. ID Number	Date	Changes
DA00069601	22 October 2004	Initial release of the A620f User's Manual
DA00069602	2 March 2005	Added Section 5 describing image data formats and structures. Moved image data format and structure information to a separate chapter. Added Section 3.3.7 to clarify the terminology used to describe frame readout, buffering and transmission. Updated the terminology and layout of Section 4 to match the other IEEE 1394 camera manuals. Corrected the CSR Guid for Output Port 3 configuration on page 6-30.

Feedback

Your feedback will help us improve our documentation. Please click the link below to access an online feedback form. Your input is greatly appreciated.

http://www.baslerweb.com/umfrage/survey.html

Index

R

S

T

V

W