SKA4 Server Board and Memory Module

Technical Product Specification

Revision 1.0

May 1, 2000

Enterprise Server Group

Revision History

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March 10, 2000	0.91	Pre-production release.
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1. SKA4 Server Board Architecture Overview

1.1 Feature Overview

The Intel® SKA4 server board set design features quad Intel® Pentium® III Xeon™ processor support and the ServerWorks Champion* 2HE chipset. The SKA4 server board combines the latest technology and integrated features to provide a high-performance platform at mid-range cost efficiency. The SKA4 server baseboard utilizes the ServerWorks Champion 2HE chipset to maximize system performance for 32-bit application software and operating systems (OSs).

The SKA4 server baseboard supports one to four Pentium III Xeon processors (conforming to the Slot 2 specification) contained on Single Edge Contact (SEC) cartridges. The baseboard provides four Slot 2 connectors, and connectors for three, VRM 8.3-compliant, plug-in voltage regulator modules. The SKA4 server board design will accommodate identified upgrades to future Intel® processing technology.

The SKA4 server board set provides the following features:

- Quad Intel Pentium III Xeon processor cartridge support.
  - Four SC330.1 Slot 2 Single Edge Contact cartridges for installation of one to four identical Intel Pentium III Xeon processors.
  - Four embedded VRMs and three VRM connectors to support four processor cartridges.
- ServerWorks Champion 2HE chipset.
  - Champion 2 HE North Bridge (CNB20HE).
  - Open South Bridge (OSB4).
  - Champion 2 I/O Bridge (CIOB).
  - Memory Address and Data Path (MADP).
- Support for 16 PC-100 compliant registered ECC SDRAM memory modules.
  - ECC single-bit correction, and multiple-bit error detection.
- 32-bit, 33-MHz 5V keyed PCI segment (P32-C) with two expansion connectors and three embedded devices.
  - PCI narrow/wide Ultra SCSI controller—Adaptec* AIC-7880 SCSI controller.
  - PCI network interface controller—Intel® 82559 Fast Ethernet controller.
  - 3D/2D Graphics Accelerator —ATI Rage* IIc video controller.
- 64-bit, 66-MHz, 3.3V keyed hot-plug PCI segment (P64-A) with two expansion connectors and one embedded device.
  - DesotoE2* PCI hot-plug controller.
- 64-bit, 33-MHz, 5V keyed PCI hot-plug segment (P64-B) with four expansion connectors and two embedded devices.
  - DesotoE2 PCI hot-plug controller.
  - Dual Channel Wide Ultra/Ultra II/Ultra 160/M SCSI controller—Adaptec 7899 SCSI controller.
- Compatibility bus segment with three embedded devices.

  - Super I/O controller chip providing all PC-compatible I/O (floppy, parallel, serial, keyboard, mouse).
  - Baseboard Management Controller (BMC) providing monitoring, alerting, and logging of critical system information obtained from embedded sensors on baseboard.
  - 8 Mbit Flash device for system BIOS.
- Two externally accessible Universal Serial Bus (USB) ports.
- One IDE connector, supporting up to two ATA33 compatible devices.

Figure 1-1 shows the functional blocks of the SKA4 server board and memory expansion card (MEC).

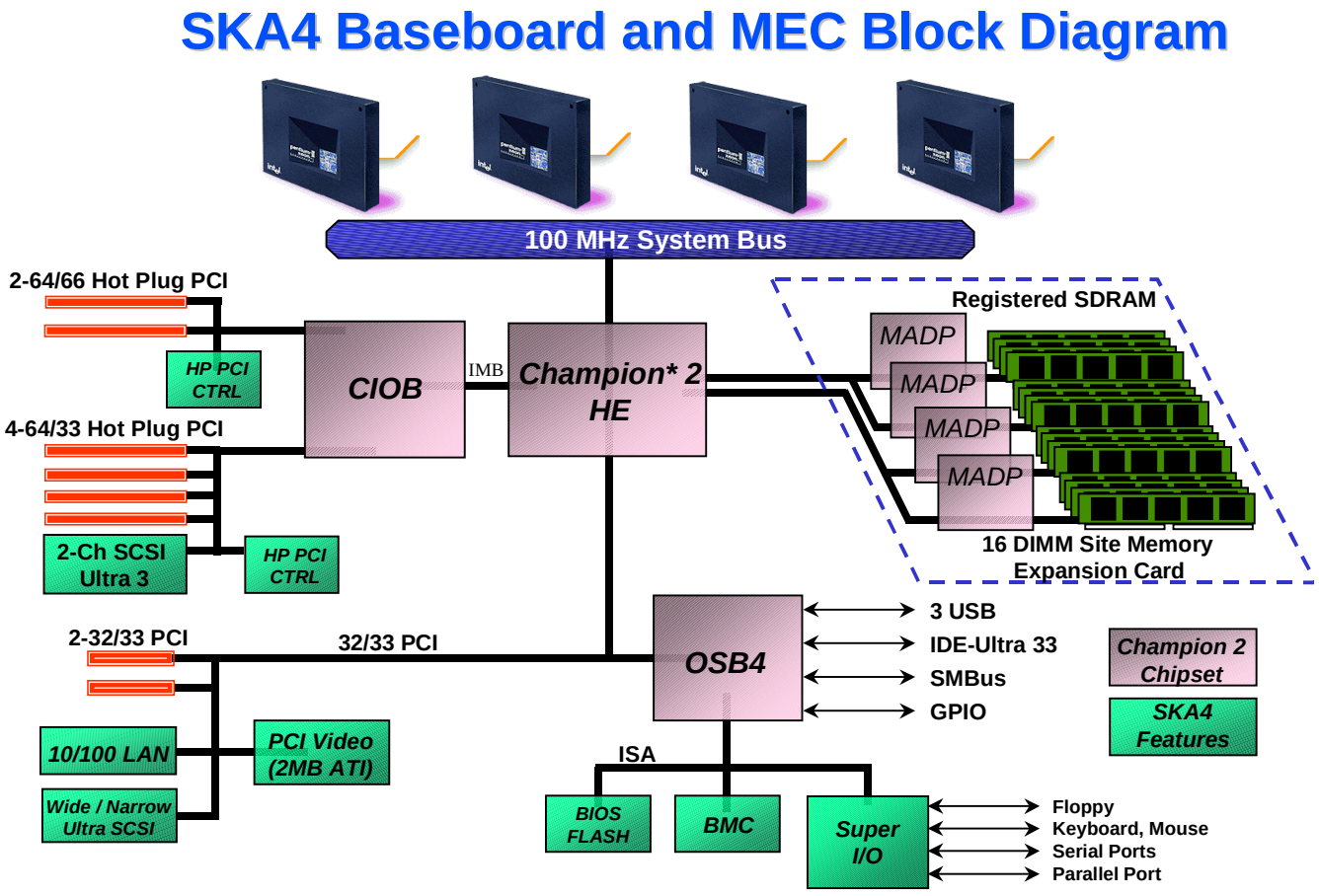

Figure 1-1: SKA4 MP Server Functional Block Architecture

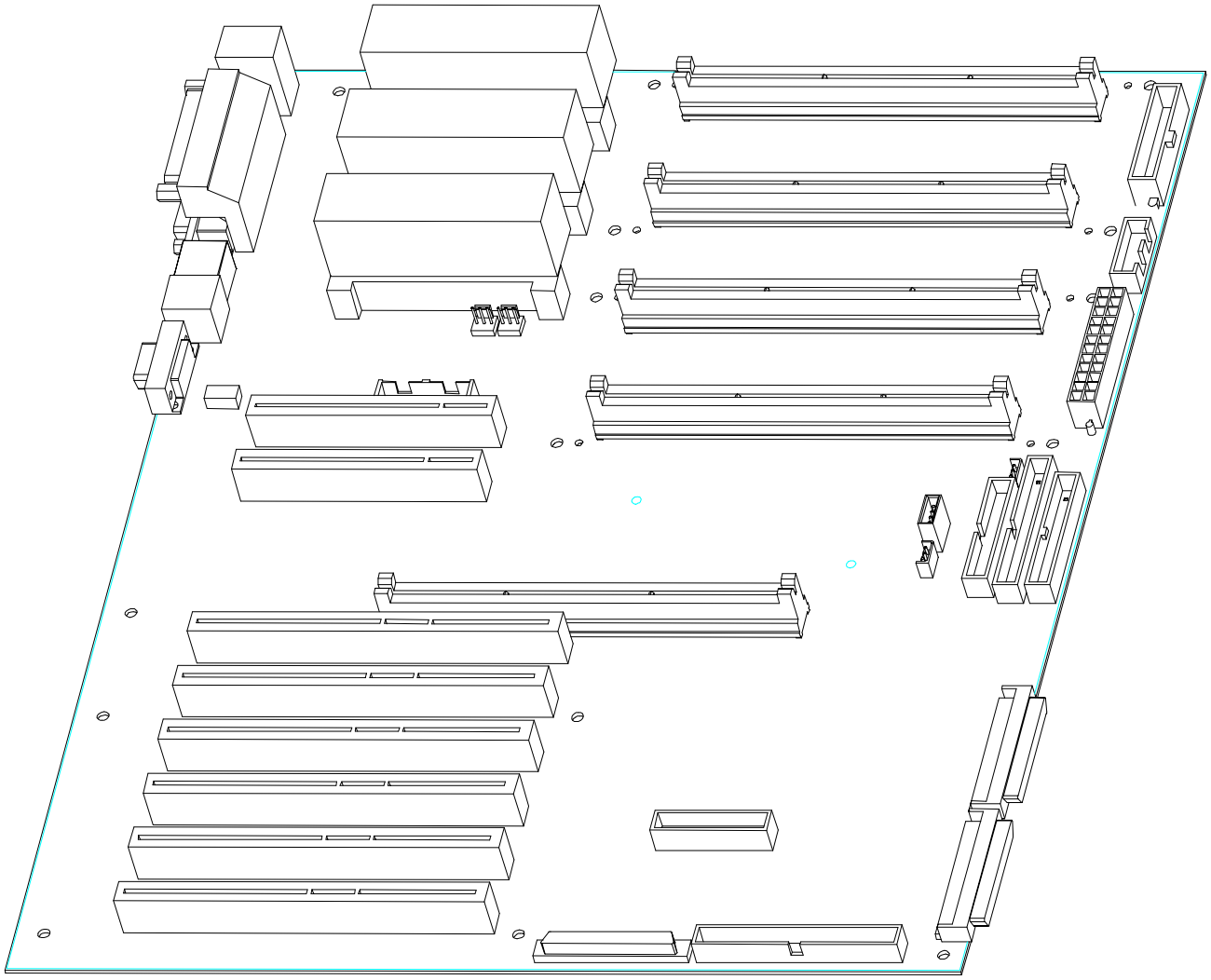

Figure 1-2: SKA4 MP Baseboard Layout Diagram

1.2 Processor/PCI Host Bridge

The SKA4 server board processor/PCI bridge/memory sub-system consists of one to four identical Pentium III Xeon processors, a plug-in memory board, and support circuitry on the baseboard consisting of the following:

- ServerWorks Champion 2HE chipset providing an integrated I/O bridge and memory controller and a flexible I/O subsystem core (PCI) optimized for multiprocessor systems and standard high-volume (SHV) servers.
- Quad SC330.1 compliant edge connectors that accept the Intel Pentium III Xeon processors.
- A 330-pin connector interface to the memory expansion board.
- Processor host bus AGTL+ support circuitry, including termination power supply.

- Four embedded VRMs providing Vtt power, cache power for all processor slots and Vcc core for the first processor. Three sockets for plug-in VRMs to provide Vcc core power for up to three additional processor cards.
- APIC bus support.
- Miscellaneous logic for reset configuration, processor card presence detection, ITP port, and server management.

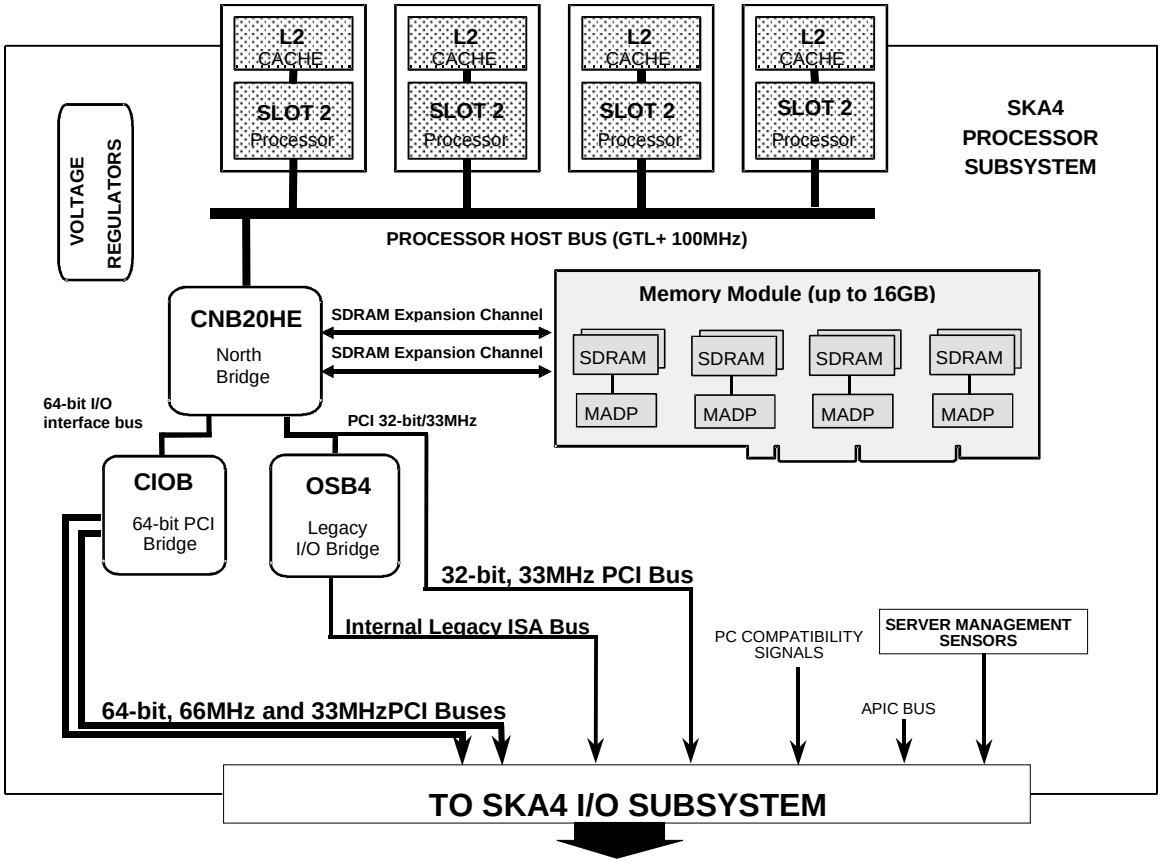

Figure 1-3: Processor/PCI Host Bridge/Memory Sub-system

1.3 Pentium® III Xeon™ Processor Cartridge

The SKA4 server board is designed to accommodate the Pentium III Xeon Slot 2 cartridges which run at frequencies at or above 500 MHz and interface with the front side bus at 100 MHz.

The Pentium III Xeon processor cartridge external interface is designed to be MP-ready. Each processor contains a local APIC section for interrupt handling. When four processor cartridges are installed, all processor cartridges must be of identical revision, core voltage, and bus/core speeds.

Note: All processor slots must be populated with either a processor or a termination card. The BMC will not allow DC power to be applied to the system unless all four SC330.1 slots contain a properly seated processor or termination card.

1.3.1 Processor Support

SKA4 specifically supports all Pentium III Xeon processors at 500 MHz and 550 MHz with 512k, 1M and 2M cache sizes. SKA4 also supports 700-MHz+ Pentium III Xeon processors, although not all versions. Specifically, SKA4 supports the 2.8V 700-MHz+ Pentium III Xeon processors with cache sizes of 1M and 2M. SKA4 will not support the 256k cache size versions or the 5/12V 600-MHz+ Pentium III Xeon processors. The table below summarizes this information.

Table 1-1: SKA4 Processor Support Matrix

Name	Frequency	Cache Size	Support (Yes/No)
Pentium® II Xeon™	400 MHz, 450 MHz	512k, 1M, 2M	No
Pentium III Xeon	**500 MHz 550 MHz**	**512k, 1M, 2M**	**Yes**
Pentium III Xeon	600 MHz +	256k	No
2.8V Pentium III Xeon	**700 MHz +**	**1M, 2M**	**Yes**
5/12V Pentium III Xeon	600 MHz +	1M, 2M	No

1.3.2 Retention Module

The Pentium III Xeon processor retention module is used to add stability to the processor cartridge connector and a way of providing attachment to the baseboard. The processor retention module is attached with screws. For details on retention module installation, please reference the *SKA4 Server Board Product Guide*.

1.3.3 Processor Cartridge Connector

The Pentium III Xeon processor cartridge edge connector conforms to the SC330.1 (“Slot 2”) specification. The baseboard provides 4 SC330.1 processor cartridge connectors. Slot 2 connectors are keyed to ensure proper orientation.

1.3.4 Processor Heat/Fan Sinks

The SKA4 server baseboard is not dependent on having fan sinks, nor are fan sinks supported by the SKA4 server board.

1.3.5 Processor Bus Termination/Regulation/Power

The termination circuitry required by the Intel Pentium III Xeon processor bus (AGTL+) signaling environment, and the circuitry to set the AGTL+ reference voltage, are implemented directly on the processor cards. The baseboard provides 1.5 V AGTL+ termination power (VTT), and VRM 8.3-compliant DC-to-DC converters to provide processor power (VCCP) at each connector. The baseboard provides four embedded and three VRM sockets to power the processors. The four embedded derive power from the 5V supply and provide power to AGTL/VTT (1 VRM), Core power for processor 1 (1 VRM), and cache power for processors 1 and 2 (1 VRM) and processors 3 and 4 (1 VRM). The three VRMs sockets derive power from the 12V supply and provide core power for processors 2, 3, and 4 (respectively). Note that 700+ MHz 2.8V processors get all their power from the core supply. For more information, see the *VRM 8.3 DC-DC Converter Specification*.

1.3.6 Termination Card

Logic is provided on the baseboard to detect the presence and identity of installed processor or termination cards. If any SEC processor cartridge is not installed in the system, a termination card must be installed in the vacant SEC processor cartridge slot to ensure reliable system operation. The termination card contains AGTL+ termination circuitry, clock signal termination, and Test Access Port (TAP) bypassing for the vacant connector. The system will not boot unless all slots are occupied with a processor or termination card.

1.3.7 APIC Bus

Interrupt notification and generation for the processors is done using an independent path between local APICs in each processor and the I/O APIC in the OSB4 located on the baseboard. This independent bus consists of two data signals and one clock line.

1.4 ServerWorks Champion* 2HE Chipset

The ServerWorks Champion 2HE chipset provides an integrated I/O bridge and memory controller and a flexible I/O subsystem core (PCI), targeted for multiprocessor systems and standard high-volume servers based on the Intel Pentium III Xeon processor. The ServerWorks Champion 2HE chipset consists of four components, as listed below:

- **CNB20HE—Champion North Bridge.** The CNB20HE is responsible for accepting access requests from the host (processor) bus and for directing those accesses to memory or to one of the PCI buses. The CNB20HE monitors the host bus, examining addresses for each request. Accesses may be directed to a memory request queue, for subsequent forwarding to the memory subsystem, or to an outbound request queue, for subsequent forwarding to one of the PCI buses. The CNB20HE also accepts inbound requests from the CIOB and the legacy PCI bus. The CNB20HE is also responsible for generating the appropriate controls to the MEC to control data transfer to and from the memory.
- **CIOB—Champion I/O Bridge.** The CIOB provides the interface for both the 64-bit/66-MHz Rev. 2.2-compliant PCI bus and the 64-bit/33-MHz Rev. 2.2-compliant PCI bus. The CIOB is both master and target on both PCI buses.
- **OSB4—Open South Bridge**. The OSB4 controller has several components. It provides the interface for a 32-bit/33-MHz Rev. 2.2-compliant PCI bus. The OSB4 can be both a master and a target on that PCI bus. The OSB4 also includes a USB controller and an IDE controller. The OSB4 is also responsible for much of the power management functions, with ACPI control registers built in. The OSB4 also provides a number of GPIO pins.
- **MADP—Memory Address and Data Path**. The SKA4 memory module has four MADP components. These devices are used to expand the SDRAM signaling environment to support up to 16 PC-100 Registered SDRAM DIMMs. These DIMMs can be up to 1 GB each.

1.4.1 ServerWorks Champion* 2HE Chipset Memory Architecture Overview

The CNB20HE provides the memory controller for the system. The main memory interface consists of two concurrent 100MHz SDRAM channels. These channels run to a connector called the Memory Expansion Card Connector (MECC).

The 100-MHz SDRAM channels to the MECC connect to four MADP repeater devices on the memory expansion card to interface to PC-100 Registered ECC SDRAM DIMMs. Main memory sizes from 256 MB to 16 GB are supported with 72-bit, four-way interleaved PC-100 Registered SDRAM DIMMs. The ECC algorithm used during main memory accesses is capable of correcting single-bit errors and detecting all double-bit errors.

The interface between the CNB20HE and the 4 MADP devices on the MEC is a proprietary interface. This interface provides 1.6 GB / second bandwidth to/from main memory.

For details on the Memory Expansion Card, see the SKA4 Server Board SDRAM Memory Module section.

1.4.2 I/O Architecture Overview

The CNB20HE, CIOB, and OSB4 chips provide the pathway between processor and I/O systems. The CNB20HE is responsible for accepting access requests from the host (processor) bus, and directing all I/O accesses to one of the PCI buses or legacy I/O locations. If the cycle is directed to one of the 64-bit PCI segments, the HE communicates with the CIOB through a private interface called the IMB. If the cycle is directed to the 32-bit PCI segment or to the OSB4, the cycle is output on the HE's 32-bit PCI bus. The CIOB translates the IMB bus operation to a 64-bit PCI Rev. 2.2-compliant signaling environment operating at either 66 MHz or 33 MHz.

The IMB bus consists of two data paths, one upstream (to the CNB20HE from the CIOB) and one downstream (from the CNB20HE to the CIOB). The interface is 16 bits wide and operates at 133 MHz with double pumped data, providing over 1GB per second of bandwidth or 533 MB per second in each direction concurrently.

All I/O for SKA4, including PCI- and PC-compatible, is directed through the CNB20HE and then through either the CIOB or the HE provided 32-bit/33-MHz PCI bus.

The HE provides a 32-bit/33-MHz PCI bus hereafter called P32-C.

The CIOB provides a 64-bit/66-MHz PCI bus hereafter called P64-A, and the 64-bit/33-MHz PCI bus hereafter called P64-B.

This independent bus structure allows all three PCI buses to operate concurrently and provides 1.2 GB per second of I/O bandwidth.

1.4.3 CNB20HE

The Champion North Bridge Rev 2.0 High End (CNB20HE) is the third generation product in ServerWorks's Champion North Bridge Technology. The CNB20HE uses the proven components of previous generations like the Pentium Pro bus interface unit, the PCI interface unit and the SDRAM memory interface unit. In addition to the above-mentioned units, the CNB20HE incorporates an Intra Module Bus (IMB) Interface. The IMB interface enables the

CNB20HE to directly interface with the CIOB20. The CNB20HE also increases the main memory interface bandwidth and maximum memory configuration with a 144-bit wide memory interface.

The CNB20HE integrates three main functions: 1) an integrated high performance main memory subsystem; 2) an IMB bus interface that provides a high-performance data flow path between the Pentium Pro bus and the I/O subsystem; and 3) a PCI interface which provides an interface to the compatibility PCI bus segment and the OSB4 (South Bridge).

Other features provided by the CNB20HE include the following:

- Full support of ECC on the processor bus.
- Full support of ECC on the memory interface.
- Eight deep in-order queue.
- Full support of registered PC-100 ECC SDRAM DIMMs.
- Support for 16 GB of 4-way interleaved SDRAM.

The CNB20HE also provides the legacy 32-bit PCI subsystem. The CNB20HE acts as the central resource on this PCI interface.

P32-C supports the following embedded devices and connectors:

- Two 120-pin, 32-bit PCI expansion connectors numbered P32-C1 and P32-C2.
- OSB4 – Open South Bridge.
- PCI network interface controller—Intel 82559 Fast Ethernet Controller.
- 3D/2D Graphics Accelerator —ATI Rage IIc Video Controller.
- PCI narrow/wide Ultra SCSI controller—Adaptec AIC-7880 SCSI Controller.

See the SKA4 Server Board PCI I/O Subsystem section for details on this I/O segment.

1.4.4 CIOB

The Champion I/O Bridge (CIOB) provides an integrated I/O bridge that provides a high-performance data flow path between the IMB and the 64-bit I/O subsystem. This subsystem supports peer 64-bit PCI segments. Having multiple PCI interfaces, the CIOB is able to provide large and efficient I/O configurations. The CIOB functions as the bridge between IMB and the multiple 64-bit PCI I/O segments.

The IMB interface is capable of supporting 512 MB/s of data bandwidth in both the upstream and downstream direction simultaneously.

1.4.4.1 P64-A I/O Subsystem

P64-A supports the following embedded devices and connectors:

- Two 184-pin, 3.3 V keyed, 64-bit PCI expansion slot connectors, numbered P64-A1 and P64-A2, supporting both 66-MHz and 33-MHz 3.3 V-compliant PCI adapters.
- One DesotoE2 hot-plug PCI controller.

All of the slots on segment P64-A support PCI hot-plug and conform to the *PCI Hot-Plug Specification, Revision 1.0.*

1.4.4.2 P64-B I/O Subsystem

P64-B supports the following embedded devices and connectors:

- One Adaptec 7899 dual channel SCSI-3 Ultra 160/m SCSI controller.
- Four 184-pin, 5 V keyed, 64-bit PCI expansion slot connectors, numbered P64-B1, P64-B2, P64-B3, and P64-B4, supporting 33-MHz 5V PCI compliant PCI adapters.
- One DesotoE2 hot-plug PCI controller.

All slots on segments P64-B support PCI hot-plug and conform to the *PCI Hot-plug Specification, Revision 1.0*.

1.4.5 OSB4

The OSB4 is a PCI device that provides multiple PCI functions in a single package: PCI-to-ISA bridge, PCI IDE interface, PCI USB controller, and power management controller. Each function within the OSB4 has its own set of configuration registers; once configured, each appears to the system as a distinct hardware controller sharing the same PCI bus interface.

On the SKA4 baseboard, the primary role of the OSB4 is to provide the gateway to all PC-compatible I/O devices and features. The SKA4 baseboard uses the following OSB4 features:

- PCI interface.
- IDE interface, with Ultra DMA 33 capability.
- USB interface.
- PC-compatible timer/counters and DMA controllers.
- Baseboard Plug and Play support.
- General purpose I/O.
- Power management.
- APIC and 8259 interrupt controller.
- Host interface for AT compatible signaling.
- Internal only ISA bus (no ISA expansion connectors) bridge for communication with Super I/O, BIOS flash and BMC.

The following sections describe each supported feature as used on the SKA4 baseboard.

1.4.5.1 PCI Interface

The OSB4 fully implements a 32-bit PCI master/slave interface, in accordance with the *PCI Local Bus Specification, Revision 2.2*. On the SKA4 baseboard, the PCI interface operates at 33 MHz, using the 5V-signaling environment.

1.4.5.2 PCI Bus Master IDE Interface

The OSB4 acts as a PCI-based Fast IDE controller that supports programmed I/O transfers (transfer rates up to 14 MBps) and bus master IDE transfers (transfer rates up to 33 MBps).

While the OSB4 supports two IDE channels, supporting two drives each (drives 0 and 1), the SKA4 baseboard uses only the primary IDE channel. A single IDE connector, featuring 40 pins (2 x 20), is provided on the baseboard.

The SKA4 IDE interface supports Ultra DMA/33 Synchronous DMA Mode Transfers.

1.4.5.3 USB Interface

The OSB4 contains a USB controller and USB hub. The USB controller moves data between main memory and the two USB connectors provided.

The SKA4 baseboard provides a dual external USB connector interface on the back. Both ports function identically and with the same bandwidth. The external connector is defined by the *USB Specification, Revision 1.0*.

1.4.5.4 Compatibility Interrupt Control

The OSB4 provides the functionality of two 82C59 PIC devices, for ISA-compatible interrupt handling.

1.4.5.5 APIC

The OSB4 integrates a 16-entry IO APIC that is used to distribute 16 PCI interrupts. It also includes an additional 16-entry IO APIC for distribution of legacy ISA interrupts.

1.4.5.6 Power Management

One of the embedded functions of OSB4 is a power management controller. The SKA4 baseboard uses this to implement ACPI-compliant power management features. SKA4 supports sleep states S0, S1, S4 and S5.

1.4.6 MADP

The SKA4 Memory Module utilizes four MADP components in the HE-Classic mode.

In this configuration the MADP provides signal buffering to expand the two memory interface channels on the CNB20HE to four independent channels, expanding the maximum memory configuration to 16GB and 16 DIMM sites.

1.5 Chipset Support Components

1.5.1 Legacy I/O (Super I/O) National* PC97317VUL

The National* PC97317VUL Super I/O Plug and Play Compatible with ACPI Compliant Controller/Extender is used on the SKA4 baseboard. This device provides the system RTC, two serial ports, one parallel port, floppy disk controller, PS/2-compatible keyboard and mouse controller, general purpose I/O pins, Plug and Play functions and a power management controller. The SKA4 baseboard provides the connector interface for the floppy, dual serial ports, parallel port, PS/2 mouse and the PS/2 keyboard. Upon reset, the SIO reads the values on strapping pins to determine its boot-up address configuration.

1.5.1.1 Serial Ports

Two 9-pin connectors in D-Sub housing are provided for serial port A and serial port B. Both ports are compatible with 16550A and 16450 modes, and both are re-locatable. Each serial port can be set to one of four different COM-x ports, and each can be enabled separately. When enabled, each port can be programmed to generate edge- or level-sensitive interrupts. When disabled, serial port interrupts are available to add-in cards. Pinout is shown below:

Table 1-2: Serial Port Connector Pinout

Pin	Name	Description
1	DCD	Data Carrier Detected
2	RXD	Receive Data
3	TXD	Transmit Data
4	DTR	Data Terminal Ready
5	GND	Ground
6	DSR	Data Set Ready
7	RTS	Request to Send
8	CTS	Clear to Send
9	RIA	Ring Indication Active

1.5.1.2 Parallel Port

The SKA4 baseboard provides a 25-pin parallel port connector. The SIO provides an IEEE 1284-compliant 25-pin bi-directional parallel port. BIOS programming of the SIO registers enables the parallel port and determines the port address and interrupt. When disabled, the interrupt is available to add-in cards. Pinout is shown below:

Table 1-3: Parallel Port Connector Pinout

Pin	Name	Pin	Name
1	STROBE_L	14	AUFDXT_L
2	D0	15	ERROR_L
3	D1	16	INIT_L
4	D2	17	SLCTIN_L
5	D3	18	GND
6	D4	19	GND
7	D5	20	GND
8	D6	21	GND
9	D7	22	GND
10	ACK_L	23	GND
11	BUSY	24	GND
12	PE	25	GND
13	SLCT		

1.5.1.3 Floppy Port

The FDC in the SIO is functionally compatible with floppy disk controllers CMOS 765B and 82077AA. The baseboard provides the 24-MHz clock, termination resistors, and chip selects. All

other FDC functions are integrated into the SIO, including analog data separator and 16-byte FIFO. Pinout is shown below:

Table 1-4: Floppy Port Connector Pinout

Pin	Name	Pin	Name
1	GND	18	FD_DIR_L
2	FD_DENSEL	19	GND
3	GND	20	FD_STEP_L
4	n/c	21	GND
5	Key	22	FD_WDATA_L
6	FD_DRATE0	23	GND
7	GND	24	FD_WGATE_L
8	FD_INDEX_L	25	GND
9	GND	26	FD_TRK0_L
10	FD_MTR0_L	27	FD_MSEN0
11	GND	28	FD_WPROT_L
12	FD_DR1_L	29	GND
13	GND	30	FD_RDATA_L
14	FD_DR0_L	31	GND
15	GND	32	FD_HDSEL_L
16	FD_MTR1_L	33	GND
17	FD_MSEN1	34	FD_DSKCHG_L

1.5.1.4 Keyboard and Mouse Connectors

The keyboard and mouse connectors are mounted within a single stacked housing. The mouse connector is stacked over the keyboard connector. External to the board they appear as two connectors. The keyboard controller is functionally compatible with the 8042A. The keyboard and mouse connectors are PS/2-compatible. Pinouts are shown below:

Table 1-5: Keyboard Connector Pinout

Pin	Signal	Description
1	KEYDAT	Keyboard Data
2	(NC)	
3	GND	Ground
4	FUSED_VCC	+5 V, fused
5	KEYCLK	Keyboard Clock
6	(NC)	

Table 1-6: Mouse Connector Pinout

Pin	Signal	Description
1	MSEDAT	Mouse Data
2	(NC)	
3	GND	Ground

4	FUSED_VCC	+5 V, fused
5	MSECLK	Mouse Clock
6	(NC)	

1.5.1.5 Real-time Clock

The PC97317VUL contains an MC146818-compatible real-time clock with external battery backup. The device also contains 242 bytes of general purpose battery-backed CMOS RAM.

1.5.1.6 Plug and Play Functions / ISA Data Transfers

The PC97317VUL contains all signals for ISA compatible interrupts and DMA channels. It also provides ISA control, data, and address signals to transfer data to/from the BMC and the BIOS flash device. This ISA subsystem transfers all SIO peripheral control data to the OSB4 south bridge as well.

1.5.1.7 Power Management Controller

The PC97317VUL contains functionality that allows various events to allow the power-on and power-off of the system. This can be from PCI Power Management Events or from the BMC or front panel. This circuitry is powered off stand-by voltage present anytime the system is plugged into the AC outlet.

1.5.2 BIOS Flash

The SKA4 baseboard incorporates an Intel® 5V FlashFile™ 28F008SA Flash Memory component. The 28F008SA is a high-performance 8-Mbit memory organized as 1 MB of 8 bits each. There are 16 64-KB blocks.

The 8-bit flash memory provides 1024K x 8 of BIOS and nonvolatile storage space. The flash device is directly addressed as 8-bit ISA memory. For more information, see the *5 Volt FlashFile™ Memory (28F008SA x8) Datasheet.*

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2. SKA4 Server Board PCI I/O Subsystem

2.1 Overview

The primary I/O bus for SKA4 is PCI, with three PCI bus segments. All the PCI buses comply with the *PCI Local Bus Specification, Revision 2.2*. All the 64-bit slots on SKA4 support PCI hot-plug and comply with the *PCI Hot-Plug Specification, Revision 1.0*. The table below lists the characteristics of the three PCI bus segments.

Table 2-1: PCI Bus Segment Characteristics

PCI Bus Segment	Width	Speed	Type	Add-in PCI Slot Support, Total Eight Slots
P64-A	64 bit	66/33 MHz	Peer bus	2 slots (64-bit 66/33-MHz) Full-length cards
P64-B	64 bit	33 MHz	Peer bus	4 slots (64-bit/33-MHz) Full-length cards
P32-C	32 bit	33 MHz	Peer bus	2 slots (32-bit/33-MHz) Cards from 5.6” to 6.3” in length

2.2 64-bit/66-MHz PCI Subsystem (P64-A)

P64-A supports these embedded devices and connectors:

- Two 184-pin, 3.3 V, 64-bit PCI expansion connectors, numbered P64-A1 and P64-A2.
- One DesotoE2 Hot-plug PCI Controller.

2.2.1 Device IDs (IDSEL)

All slots on segment A support PCI hot-plug and conform to the *PCI Hot-Plug Specification, Revision 1.0*. Each device under the PCI host bridge has its IDSEL signal connected to one bit of **AD[31::16]**, which acts as a chip select on the PCI bus segment. This determines a unique PCI device ID value for use in configuration cycles. The following table shows both the bit to which each IDSEL signal is attached for P64-A devices and the corresponding device number.

Table 2-2: P64-A Configuration IDs

IDSEL Value	Device
29	PCI Slot P64-A1
30	PCI Slot P64-A2
23	DesotoE2* PHPC

2.2.2 P64-A Arbitration

P64-A supports four PCI masters (slots P64-A1, P64-A2, DesotoE2 PHP Controller and the CIOB). All PCI masters must arbitrate for PCI access, using resources supplied by the CIOB. The host bridge PCI interface (CIOB) arbitration lines **REQx*** and **GNTx*** are a special case in that they are internal to the host bridge. The following table defines the arbitration connections.

Table 2-3: P64-A Arbitration Connections

Baseboard Signals	Device
PA_REQ0*/P_GNT0*	P64-A Slot P64-A1
PA_REQ1*/P_GNT1*	P64-A Slot P64-A2
PA_REQ2*/P_GNT2*	DesotoE2* PHPC

2.2.3 DesotoE2* Hot-plug Controller

The DesotoE2 is a PCI device located on P64-A PCI bus. The DesotoE2 is the PCI Hot-plug Controller (PHPC) for the PHP slots.

The PHPC contains the Compaq*-designed PHPC Megacell for compatibility with existing PHP drivers. The DesotoE2 contains the necessary memory index and access registers located in PCI configuration space to permit access to the PHPC functions.

2.2.4 P64-A Hot-plug Support

The two P64-A slots comply with the *PCI Hot-Plug Specification, Revision 1.0*. The slots support 3.3 V, 64-bit and 32-bit, 66- or 33-MHz PCI adapters.

The actual bus operating speed is determined during the system's Power-on Self-Test (POST). If any installed PCI adapters do not support 66-MHz operation, the bus speed will be adjusted to run at 33 MHz. If no adapters are installed, the bus segment can be selected to operate at either 66 MHz or 33 MHz based on the BIOS SETUP option.

Note: To comply with the published PCI specification, the PCI bus segment must be reset when the bus speed is changed. This may be done only when the system is reset. Therefore, once the speed of the P64-A bus segment is set during POST, it may not be changed while the system is running.

If a 33-MHz PCI adapter is hot-plugged into the P64-A bus segment while the bus is running at 66 MHz, the PCI hot-plug controller and operating system driver will not allow the newly added PCI adapter online.

2.3 64-bit/33-MHz PCI Subsystem

PCI segments A and B are peer buses. P64-B supports the following embedded devices and connectors:

- One Adaptec 7899 dual channel SCSI-3 Ultra 160/m SCSI Controller.
- Four 184-pin, 5 V, 64-bit PCI expansion connectors, numbered P64-B1, B2, B3, and B4.
- One DesotoE2 Hot-plug PCI Controller.

2.3.1 Device IDs (IDSEL)

All slots on segment B support PCI hot-plug and conform to the *PCI Hot-Plug Specification, Revision 1.0*. The PCI IDSEL signal connections to PCI AD[31::11] lines for P64-B devices are shown in the following table.

Table 2-4: P64-B Configuration IDs

IDSEL Value	Device
24	PCI Slot P64-B1
25	PCI Slot P64-B2
26	PCI Slot P64-B3
27	PCI Slot P64-B4
22	7899 SCSI Controller
21	DesotoE2* PHPC

2.3.2 P64-B Arbitration

P64-B supports six PCI masters: slots P64-B1 through P64-B4, wide SCSI controller and the DesotoE2 PHP Controller. All PCI masters must arbitrate for PCI access using resources supplied by the CIOB. The CIOB interface arbitration connections are internal to the device. The following table defines the external arbitration connections:

Table 2-5: P64-B Arbitration Connections

Baseboard Signals	Device
S_REQ0*/S_GNT0*	PCI Slot P64-B1
S_REQ1*/S_GNT1*	PCI Slot P64-B2
S_REQ2*/S_GNT2*	PCI Slot P64-B3
S_REQ3*/S_GNT3*	PCI Slot P64-B4
S_REQ4*/S_GNT4*	Wide SCSI Controller
S_REQ5*/S_GNT5*	DesotoE2* PHPC

2.3.3 DesotoE2* Hot-Plug Controller

The DesotoE2 is a PCI device located on P64-B PCI bus. The DesotoE2 is the PCI Hot-plug Controller for the PHP slots.

The PHPC contains the Compaq-designed PHPC Megacell for compatibility with existing PHP drivers. The DesotoE2 contains the necessary memory index and access registers located in PCI configuration space to permit access to the PHPC functions.

2.3.4 Ultra 160/m SCSI Controller (Adaptec* 7899)

SKA4 provides an embedded dual-function Adaptec AIC-7899 PCI SCSI host adapter on the P64-B segment. The AIC-7899 controller contains two independent SCSI controllers that share a single PCI bus master interface as a multifunction device. Internally, each controller is identical, capable of operations using either 16-bit SE or LVD SCSI providing 40 MBps (Ultra-wide SE), 80 MBps (Ultra 2), or 160 MBps (Ultra 160/m).

In the SKA4 MP implementation, both controller A and controller B attach to a 68-pin 16-bit differential SCSI connector LVD interface. Each controller has its own set of PCI configuration registers and SCSI I/O registers. As a PCI bus master, the AIC-7899 supports burst data transfers on PCI up to the maximum rate of 266 MBps using on-chip buffers. Refer to the *AIC-7899 PCI-Dual Channel SCSI Multi-Function Controller Data Manual* for more information on the internal operation of this device and for descriptions of SCSI I/O registers.

2.4 32-bit/33-MHz PCI Subsystem

All 32-bit/33-MHz PCI I/O for the SKA4 baseboard, including PCI- and PC-compatible, is directed through the CNB20HE. The 32-bit/33-MHz PCI segment created by the CNB20HE is called the P32-C segment. The P32-C segment supports the following embedded devices and connectors:

- Two 120-pin, 32-bit PCI expansion connectors, numbered P32-C1 and P32-C2.
- OSB4 I/O APIC, PCI-to-ISA bridge, IDE controller, USB controller, and power management.
- PCI Video Controller.
- PCI Network Interface Controller.
- PCI Legacy Ultra SCSI controller.

2.4.1 Device IDs (IDSEL)

Each device under the PCI hub bridge has its IDSEL signal connected to one bit of **AD[31::16]**, which acts as a chip select on the PCI bus segment in configuration cycles. This determines a unique PCI device ID value for use in configuration cycles. The following table shows the bit to which each IDSEL signal is attached for P32-C devices, and corresponding device number. For more information see “Chapter Six: Configuration Space” in the *PCI Local Bus Specification, Revision 2.2.*

Table 2-6: P32-C Configuration IDs

IDSEL Value	Device
18	PCI Slot P32-C1
19	PCI Slot P32-C2
17	PCI 7880 SCSI
20	PCI NIC 82559
28	ATI Rage* IIc Video Controller
31	OSB4; ISA Bridge, IDE, USB, SM Bus

2.4.2 P32-C Slot Specifics

The PCI slots support the PME# and 3.3VAUX signals as described in the *PCI Bus Power Management Interface Specification*.

The 3.3VAUX signal is a limited current 3.3 V supply maintained even when the system power is turned off.

WARNING: The SKA4 baseboard only supports one slot consuming 375mA of Standby current on the 3.3V AUX power line. This capability is only available to the 32bit/33MHz slots. The other slot can consume a maximum of 120mA. The system will not operate correctly if this limit is exceeded.

These two slots have length and height restrictions as follows.

Table 2-7: P32-C Slot Use Restrictions

Slot #	Maximum Length	Maximum Component Height	
P32-C1	5.3”	.570”	
P32-C2	6.3”	.400”	.300” component height restriction from 5.3” to 6.3” length and up 1” from the baseboard in the CNB20HE heat sink area.

2.4.3 Legacy SCSI (Adaptec* 7880)

The SKA4 provides an embedded SCSI host adapter on the P32-C bus: AIC-7880. The AIC-7880 contains a single SCSI controller with full-featured PCI bus master interface in a 160-pin PQFP. The 7880 supports either 8- or 16-bit Fast SCSI providing 10MBps or 20MBps (Fast-10) throughput, or Fast-20 SCSI that can burst data at 20 MBps or 40 MBps. As a PCI 2.2 bus master (complies with *PCI Local Bus Specification, Revision 2.2*), the AIC-7880 supports burst data transfers on PCI up to the maximum rate of 133 MBps using the on-chip 256-byte FIFO.

The SKA4 AIC-7880 implementation offers 8-bit or 16-bit SCSI connectors and operation at data transfer rates of 10, 20, or 40 MBps. The AIC-7880 also offers active negation outputs, controls for external differential transceivers, a disk activity output, and a SCSI terminator power-down control. Active negation outputs reduce the chance of data errors by actively driving both polarities of the SCSI bus, avoiding indeterminate voltage levels and common-mode noise on long cable runs. The SCSI output drivers can directly drive a 48-mA single-ended SCSI bus with no additional drivers (the SCSI segment can support up to 15 devices).

Because the AIC-7880 can be used as an 8-bit controller (via the narrow, 50-pin connector) and as a 16-bit controller (via the wide, 68-pin connector), the AIC-7880 is not always at one end of the SCSI bus, and termination is controlled through some simple circuitry. The circuitry senses when there is a device attached through the narrow, 50-pin connector or the wide, 68-pin connector. When there are devices off both connectors, the termination is on for the upper 8 bits of data and the parity bit associated with these data lines. All other signals are not terminated on board and are terminated by the devices attached through the connector. When there is a device on only one connector (either wide or narrow), all on-board termination is on.

2.4.4 Network Interface Controller (NIC)

SKA4 supports a 10BASE-T/100BASE-TX network subsystem based on the Intel 82559 Fast Ethernet Multifunction PCI/CardBus Controller. This device is similar in architecture to its predecessor (Intel® 82558 controller). The 82559 is a highly integrated PCI LAN controller in a 196-pin BGA supporting 10 or 100 Mbps Fast Ethernet networks. As a PCI bus master, the 82559 can burst data at up to 132 MBps.

2.4.4.1 Supported Network Features

The 82559 includes an IEEE MII-compliant interface to the components necessary to implement an IEEE 802.3 100BASE-TX network connection. SKA4 supports the following features of the 82559 controller:

- Glueless 32-bit PCI Bus Master Interface (Direct Drive of Bus), compatible with *PCI Local Bus Specification*, *Revision 2.2.*

- 82596-like chained memory structure, with improved dynamic transmit chaining for enhanced performance.
- Programmable transmit threshold for improved bus utilization.
- Early receive interrupt for concurrent processing of receive data.
- On-chip counters for network management.
- Autodetect and autoswitching for 10- or 100-Mbps network speeds.
- Support for both 10-Mbps and 100-Mbps networks, full or half duplex-capable, with back-to-back transmit at 100 Mbps.
- Integrated physical interface to TX magnetics.
- The magnetics component terminates the 100BASE-TX connector interface. A flash device stores the network ID.

2.4.4.2 NIC Connector and Status LEDs

The 82559 drives LEDs on the network interface connector that indicate transmit/receive activity on the LAN, a valid link to the LAN, and 10- or 100-Mbps operation. The green LED (left) indicates network connection when on and TX/RX activity when blinking. The yellow LED indicates 100-Mbps operation when lit.

2.4.5 Video Controller

The SKA4 MP server provides an ATI Rage IIc VGA Graphics Accelerator, along with video SGRAM and support circuitry for an embedded SVGA video subsystem. The ATI Rage IIc chip contains an SVGA video controller, clock generator, BitBLT engine, and RAMDAC in a 208-pin PQFP. One 256K x 32 SGRAM chip provides 2 MB of 10-ns video memory. The SVGA subsystem supports a variety of modes, up to 1600 x 1200 resolution, or up to 16.7 M colors. It also supports analog VGA monitors, single- and multifrequency, interlaced and noninterlaced, up to 100 Hz vertical retrace frequency. The SKA4 MP server provides a standard 15-pin VGA connector and video blanking logic for server management console redirection support.

2.4.5.1 Video Modes

The ATI Rage IIc chip supports all standard IBM VGA modes. The following tables show all the modes that this implementation supports, including the number of colors, resolution, and refresh rates.

Table 2-8: Standard VGA Modes

Resolution	Max Refresh Rate (Hz)	Colors
640x480	200	256
800x600	200	256
1024x768	150	256
1152x864	120	256
1280x1024	100	256
1600x1200	76	256
640x480	200	65K
800x600	200	65K
1024x768	150	65K

Resolution	Max Refresh Rate (Hz)	Colors
1152x864	120	65K
640x480	200	16.7M
800x600	160	16.7M

2.4.5.2 VGA Connector

The following table shows the pinout of the VGA connector. For more information, see the *ATI Rage IIc Technical Reference Manual*.

Table 2-9: Video Port Connector Pinout

Pin	Signal	Description
1	RED	Analog color signal R
2	GREEN	Analog color signal G
3	BLUE	Analog color signal B
4	nc	No connect
5	GROUND	Video ground (shield)
6	GROUND	Video ground (shield)
7	GROUND	Video ground (shield)
8	GROUND	Video ground (shield)
9	nc	No connect †
10	GROUND	Video ground
11	nc	No connect
12	DDCDAT	Monitor ID data
13	HSYNC	Horizontal Sync
14	VSYNC	Vertical Sync
15	DDCCLK	Monitor ID clock

Notes:
† This no-connect pin is used to reduce EMI.

2.5 Interrupt Routing

2.5.1 Overview

SKA4 interrupt architecture accommodates both PC-compatible PIC mode and APIC mode interrupts through use of the integrated I/O APICs in the OSB4.

2.5.2 Legacy Interrupt Routing, OSB4 Compatibility Interrupt Controller

For PC-compatible mode, the OSB4 provides two 82C59-compatible interrupt controllers embedded in the device. The two controllers are cascaded with interrupt levels 8-15 entering on level 2 of the primary interrupt controller (standard PC configuration). A single interrupt signal is presented to the processors, to which only one processor will respond for servicing. The OSB4 contains configuration registers that define which interrupt source logically maps to I/O APIC INTx pins.

Interrupts, both PCI and IRQ types, are handled by the OSB4. The OSB4 then translates these to the APIC bus. The number in the table below indicates the OSB4 PCI interrupt input pin to

which the associated device interrupt (INTA, INTB, INTC, INTD) is connected. The OSB4's I/O APIC exists on the I/O APIC bus with the processors.

Table 2-10: PCI Interrupt Routing/Sharing

Interrupt	INT A	INT B	INT C	INT D
P64A-Slot1	1	0	0	0
P64A-Slot2	3	2	2	2
DesotoE2-66*	14			
P64B-Slot1	5	4	4	4
P64B-Slot2	7	6	6	6
P64B-Slot3	9	8	8	8
P64B-Slot4	11	10	10	10
DesotoE2-33	14			
7899 Channel 1	8			
7899 Channel 2	8			
P32C-Slot1	12	12	12	12
P32C-Slot2	13	13	13	13
82559 NIC	15			
7880-SCSI	15			

2.5.3 APIC Interrupt Routing

For APIC mode, SKA4 interrupt architecture incorporates two Intel® I/O APIC devices to manage and broadcast interrupts to local APICs in each processor. The I/O APICs monitor each interrupt on each PCI device including PCI slots in addition to the ISA compatibility interrupts IRQ(0-15). When an interrupt occurs, a message corresponding to the interrupt is sent across a three-wire serial interface to the local APICs. The APIC bus minimizes interrupt latency time for compatibility interrupt sources. The I/O APICs can also supply greater than 16 interrupt levels to the processor(s). This APIC bus consists of an APIC clock and two bi-directional data lines.

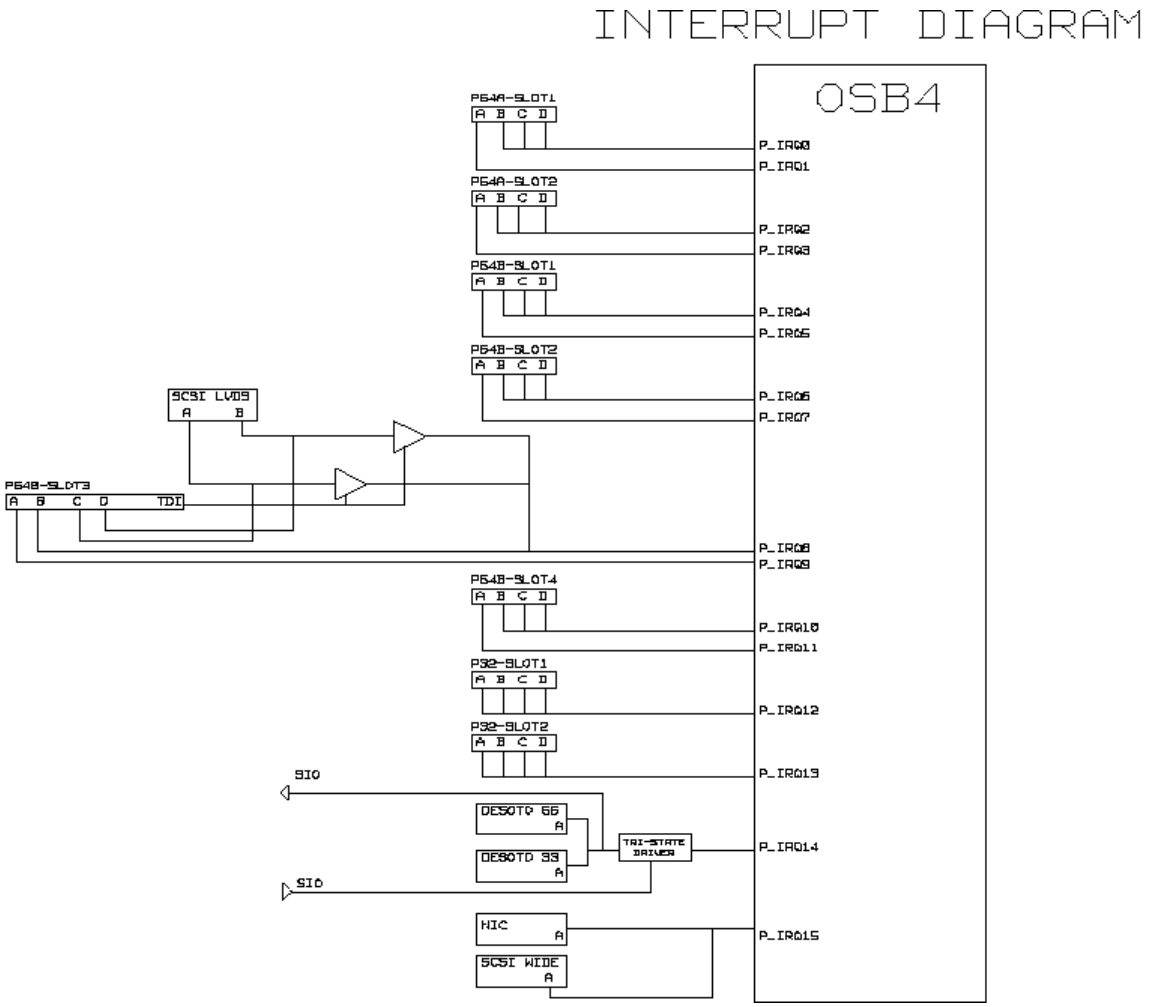

Figure 2-1: SKA4 Baseboard Interrupt Diagram

2.5.4 Legacy Interrupt Sources

The table below recommends the logical interrupt mapping of interrupt sources on the SKA4 baseboard. The actual interrupt map is defined using configuration registers in the OSB4.

Table 2-11: Interrupt Definitions

ISA Interrupt	Description
INTR	Processor interrupt.
NMI	NMI to processor.

ISA Interrupt	Description
IRQ1	Keyboard interrupt.
IRQ3	Serial port A or B interrupt from SIO device, user-configurable.
IRQ4	Serial port A or B interrupt from SIO device, user-configurable.
IRQ5	
IRQ6	Floppy disk.
IRQ7	Parallel port.
IRQ8_L	Active low RTC interrupt.
IRQ9	Reserved (SCI)
IRQ10	Reserved (USB)
IRQ11	
IRQ12	Mouse interrupt.
IRQ14	Compatibility IDE interrupt from primary channel IDE devices 0 and 1.
IRQ15	Reserved

3. PCI Hot-plug

This section discusses the PCI hot-plug (PHP) features implemented on the SKA4 server board and operating system related issues.

3.1 Overview

PCI hot-plug permits the user to add, remove, and replace PCI adapters installed in the PHP slots without interrupting normal operation or powering down the system. PHP technology improves Reliability, Availability, and Serviceability (RAS) for the system. The operating system must have the appropriate PHP driver and operating system installed to support PHP operation.

Hot plug support is provided on (all) six of the PCI slots on the 64-bit PCI bus segments (A and B). No hot plug support is provided on the 32-bit bus segment (C). Segment A can operate at either 66 MHz or 33 MHz; segment B only operates at 33 Mhz. The logic for powering-on and powering-off the slots is controlled by the DesotoE2 ASIC. Only the CBL (Connect Bus Last) power sequence is supported.

3.2 PHP Functionality

In order to support PCI hot-plug, systems require hot-plug hardware, a hot-plug operating system, and hot-plug capable adapter drivers. To insure backward compatibility, any combination of hot-plug and conventional versions of each of these components is permitted, including mixing both hot-plug and conventional adapter drivers. If a conventional driver is loaded under a hot-plug operating system, or a hot-plug driver is loaded under a conventional operating system, the driver will continue to have the same capability it always had in the conventional environment.

3.2.1 Power-up

At first power-up, BIOS is responsible for initializing the PHP Controller. The initial slot power-up sequence occurs after this device initialization. The following power-up sequence can typically be expected:

Power is applied to the slots one segment at a time, segment A followed by B. This can be observed on the HPIB: first the two Green LEDs for Segment A light-up (then turn-off), followed by the four LEDs for Segment B. During initialization BIOS determines the presence and speed of the cards in the slots. Power remains ON to slots containing a (valid) PCI card, and is turned OFF to empty slots.

Refer to the Bus Speed Control section for related information.

3.2.2 Operating System

The initial steps involved in booting to an OS do not change because of PHP support. But after the OS has booted, drivers are usually required to get PHP functionality. Drivers for supported operating systems can be downloaded from IBL (the Intel Business Link Web site).

Three terms that are commonly used to describe PCI hot-plug operations are Hot Replace, Hot Add, and Hot Upgrade. "Hot Removal" and "Hot Insertion" refers to the sequence of steps involved in removing and inserting, respectively, a PCI card from a hot plug-able PCI slot.

Hot Replace – To hot remove an adapter card and then Hot Insert an identical adapter into the same slot. The replacement adapter card will use the same PCI resources that were assigned to the previous card and its driver will not be updated. Hot Replace is also commonly referred to as "Like-for-Like Replacement."

Hot Add – To Hot Insert an adapter card to a previously unoccupied slot. This operation requires that a driver also be loaded for the hot-added adapter. This operation requires that PCI resources have been reserved by the system BIOS for the hot-added adapter card. Hot Add is also sometimes referred to as "Hot Expansion."

Hot Upgrade – To Hot Remove an adapter card and then Hot Insert an upgraded adapter (i.e., new revision) that requires different PCI resources than the original card. The adapter's driver may or may not use the same driver as the previous adapter.

Not all of these operations are supported by every hot-plug capable operating system. Furthermore, each operating system may implement these operations in a different manner. Under Microsoft* Windows NT* 4.0, for example, only the Hot Replace operation is supported. Typical functionality is outlined below:

The first step, after booting, is to load the needed drivers. After loading the drivers, a PHP graphical user interface (GUI) can be enabled by clicking on **Start** -> **Programs** -> **PCI Hot Plug** -> **PCI HP Utility**, on the Windows NT 4.0 menu bar. This GUI provides the adapter status to the hot-plug user interface, and also allows the user to control hot plug functionality. The initial screen lists: *LED Condition* (Green, Amber), *Location* (logical slot number), *Board* (description, driver support), and *Status* (Normal/Not Ready). Logical slot numbering starts from 3 and ends at 8, in increments of 1. Only slots containing a card with hot-plug capable drivers can be controlled from the GUI. Pressing the power button (HW or SW) for these slots powers them on/off; in response the Green LED either lights up or turns off. Pressing the power button for an empty slot toggles its power condition (no drivers required).

3.2.3 Bus Speed Control

Segment A can be operated at 33 MHz or 66 MHz. A PHP Hot Add (or Hot Upgrade) operation creates the possibility for the user to add a different speed capable card than the existing bus speed. Logic on the baseboard ensures proper operation in compliance with the *PCI Local Bus Specification*. The possible bus speed scenarios are summarized in the following table:

Table 3-1: Bus Speed Control

	Original Speed (MHz)	Hot Added Card	Final Speed (MHz)	Notes
Empty Bus	33 or 66	N/A	No change	Setup selectable
Loaded Bus	33	33 or 66	33	
Loaded Bus	66	33	66	Error Message
Loaded Bus	66	66	66	

Segment B is fixed at 33 MHz, regardless of the type of hot-added cards.

3.2.4 LED Control

Each slot has two LEDs. A green LED indicates the state of power on each slot. The amber LED is the slot attention indicator. The amber LED indicates an error condition with that slot. Table 6-2 summarizes typical LED states that may be encountered during operation:

Table 3-2: Slot State and Attention Indicators

LED States	Interpretation
Green On Amber Off	The slot is on and functioning normally
Green On Amber On	The slot is on and the card requires attention
Green Off Amber On	The slot is off and the card in it requires attention
Green Off Amber Off	The slot is off
Green Blinking Amber Off	Slot power transitioning (ON->OFF or OFF->ON)

3.2.5 HW Push Button

The HW push button is located on the Hot-plug Indicator Board. It duplicates the functionality of the GUI-based SW button. A single push button is provided for each slot. Pressing the button normally initiates a power-on or power-off cycle (green LED blinking). A populated slot, under Windows NT 4.0, must have drivers before the push button will properly function.

3.2.6 Power Fault

A power fault condition is generated when an overcurrent or undervolatge condition is detected. Power to the slot is automatically removed in this case.

3.2.7 Interlock Switch Support

SKA4 does not support a mechanical interlock switch. The switch input is permanently grounded (enabled) on the baseboard.

3.3 DesotoE2*

The DesotoE2 is a 32-bit, 33- or 66-MHz PCI bus agent that manages PCI hot-plug functionality on the PCI segment on which it resides. There is one DesotoE2 on each 64-bit PCI segment (A and B). The DesotoE2 PHPC is ACPI compliant and compatible with Compaq's PHPC design to permit reuse of existing drivers. The DeSotoE2 supports either 3.3 V or 5 V PCI bus implementations. It is responsible for the following functions:

- Manage power application/removal to individual PCI slots.
- Properly reset newly-added PCI cards prior to bringing the card online.

- Manage connection/disconnection of the PCI signals between the PCI bus and add-in card.
- Manage seamless addition/removal of individual PCI add-in cards without impacting bus functionality by generating dummy PCI cycles during transitions.

3.3.1 Configuration Registers

DesotoE2 contains 256 PCI configuration space registers for access to the standard PCI configuration space. These registers are accessible according to the mapping of the IDSEL pin: device 7 (on segment A) and device 5 (on segment B).

3.3.2 Memory Allocation

In order to enable the hot-add capability, PCI memory space is padded during startup. The amount of padding is determined by a BIOS setup option. The default option is "minimum" which allocates ~75MBs/empty slot. Other options are "maximum", which allocates ~186MBs/empty slot and "disabled" which allocates no memory/empty slot.

In a 4 to 16 GB configuration, the BIOS creates a "memory" hole just below 4 GB to accommodate system BIOS flash, APIC memory, and memory mapped I/O located on 32-bit PCI devices. The size of this hole depends upon the number of PCI cards and the memory mapped resources requested by them - this hole is typically under 128MB + the amount of memory reserved for PCI hot add operations.

If enabled in Setup, some amount of the system memory corresponding to this hole can be reclaimed for 2 specific memory configurations. If memory banks A, B, and C are filled with 256MB DIMMs (for a total of 3GB), the BIOS will map the memory found in bank D above 4GB leaving at least a 1GB hole below 4GB (this operation does not make sense for OSs that do not support over 4GB of memory). If memory bank A contains 512MB DIMMs (for a total of 2GB), the BIOS will map the memory found in banks B, C and D above 4GB leaving at least a 2GB hole below 4GB (this operation does not make sense for OSs that do not support over 8GB of memory) . Please note that the BIOS may be required to create a hole larger than that specified above to accommodate large PCI device configurations. In this case, additional memory may be lost and can not be reclaimed.

3.3.3 Troubleshooting Tips

- During boot-up, a populated slot powers up, then immediately powers off.
  - Verify that a valid PCI card is being used (supports PCI configuration space, for example). Some test cards (such as LAI adapters) will need a valid PCI card installed in their onboard connector before they can be recognized and powered on. Additionally, a power fault condition can also produce this behavior.
- The PHP push button functions under DOS, but is non-functional under an OS.
  - The OS-specific PHP drivers must be loaded for push button functionality.

4. SKA4 Server Board SDRAM Memory Module

4.1 Introduction

The SKA4 memory module plugs into the Memory Expansion Card Connector on the SKA4 baseboard. It contains four MADPs (Memory Address Data Path), three clock buffers to provides 100-MHz clocks to the MADPs, and the 16 DIMM sockets. The memory module comprises four banks of memory, each bank comprising four DIMMs. The banks are A,B,C and D. Bank A has A1, A2, A3 and A4 DIMMs, and so on. At least one bank of memory has to be populated for the system to work. Refer to the Supported Memory section for DIMM populating order.

The SKA4 memory module will support up to 16 GB of system memory using 1 GB PC-100 Registered DIMMs, although thermal and mechanical issues may exist in specific chassis that may limit this to less than 16 GB. Check your specific chassis.

Below is a preliminary drawing of a populated SKA4 memory module:

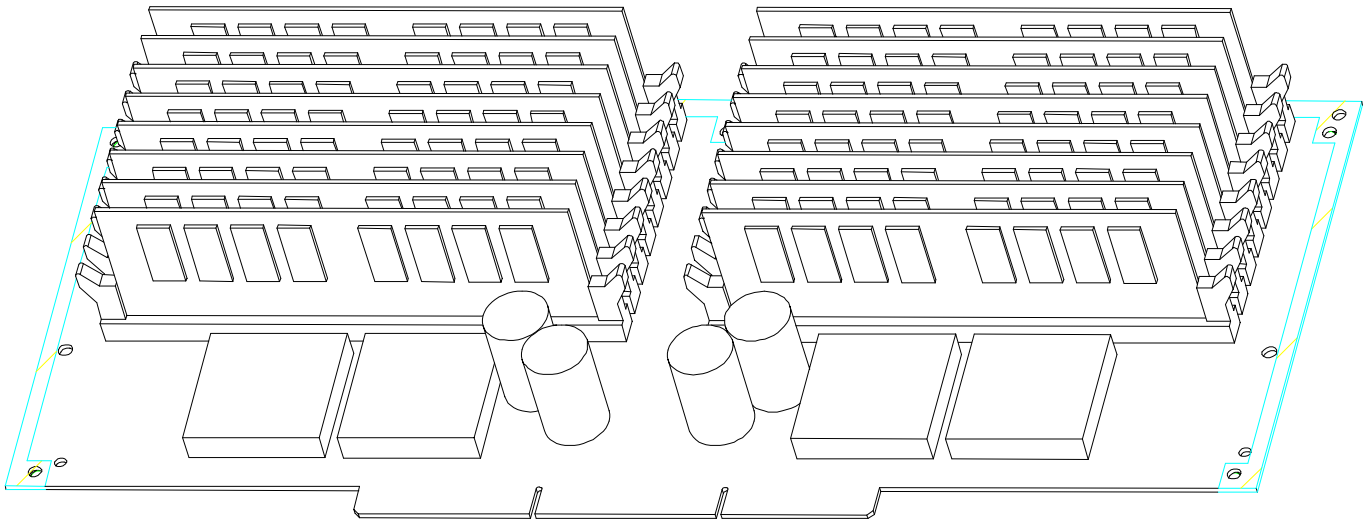

Figure 4-1: SKA4 Memory Module Mechanical Drawing

4.2 Supported Memory

The SKA4 board set supports only PC-100 compliant Registered DIMMs. Furthermore, the SKA4 board set is only qualified with ECC DIMMs.

The minimum supported DIMM size is 64 MB. Therefore the minimum main memory configuration is 4 x 64 MB or 256 MB. The largest size DIMM supported is a 1 GB stacked registered PC-100 ECC DIMM based on 256 Mbit technology.

Note: The board set will support both stacked and un-stacked PC100 compliant registered DIMMs, although thermal limitations of certain chassis may limit the configured system support. Thermal testing should be conducted to ensure the chassis provides adequate cooling to support the target memory configurations.

Note: The power dissiapation of some un-stacked DIMMs exceeds that of some stacked DIMMs. Thermal evaluations of all possible memory to be populated should be conducted.

4.3 SKA4 SDRAM Memory Module Components

4.3.1 MECC 330-pin Edge Connector

The memory module plugs into the MECC on the baseboard by the 330-pin edge connector. The 100-MHz interface between the CNB20HE and the four MADPs goes through this connector. The interface includes control signals (RAS, CAS, CS and Address), 144-bit of data and ECC, a 100-MHz clock to the clock buffer, and a 100-MHz Read Clock that goes back to the CNB20HE. There are also three separate IIC buses going from the baseboard up to the memory module.

There are sufficient ground and power pins on the connector and bulk and high frequency decoupling capacitors on the memory module to supply adequate voltages and currents to perform proper memory operations.

Note: On the baseboard, a Slot 2 connector is used for the MECC. To protect the system from damage when a Slot 2 processor or a Slot 2 processor termination card is mistakenly plugged in to the MECC, logic on the baseboard will prevent the system from powering up.

4.3.2 MADP

The MADPs receive control signals from the CNB20HE and buffer them to the DIMMs. Therefore all of the control and address lines are common to all the DIMMs except for the CS signals where MADPs decode them. The CS lines are to select one bank (four DIMMs) out of the four banks of memory, as only one bank of memory is accessed at any given time. All the control lines including the CS lines are series terminated to protect the DIMM registers from excessive over/undershoot.

The MADPs transfer 4x72 bit of data and ECCs at one clock to/from four DIMMs (of a bank) and transfer 2x72 bit of data and ECCs to/from CNB20HE.

MADP has two current strength settings: high or low configured by the CNB20HE. If there is minimum memory in the system—only one bank of non-stacked DIMM on the memory module—the strength is set to low for both the control and address lines and data lines. If more than one bank is populated, the CNB20HE will set the MADPs to high strength.

MADP also has internal PLL to synchronize the MADPs-CNB20HE bus and MADPs-DIMMs bus.

The memory data is ECC protected. SBCE (single bit correctable error) is detected and corrected by the CNB20HE. The CNB20HE also logs the syndrome bits along with the bank where the error was found. Based on that, the BIOS can correctly point to which DIMM has a bit

error. In case of MBE (multiple bit error), the BIOS can point to two out of the four DIMMs in a bank (one of the two DIMMs caused errors).

4.3.3 DIMM Sockets

Data transfers between MADPs and DIMMs in a four-way interleaved fashion. Therefore, four DIMMs in a bank must be populated. At least one bank has to be fully populated in order for the system to boot. If additional banks have less than four DIMMs, the memory for that bank(s) will not be available to the system.

There are four banks of DIMMs in the memory module; they are A, B, C and D. Bank A contains DIMM A1, A2, A3 and A4, bank B contains DIMM B1, B2, B3 and B4, and so on. These identifications are marked with silk screen on the module next to each DIMM to label its bank number. DIMMs should be installed from bank A through D in alphabetical order to best optimize the memory subsystem for signal integrity/temperature cooling.

4.3.4 IIC Buses

There are three IIC buses from the baseboard up to the memory module. Two of them connect 16 DIMM sites (one bus connects eight DIMMs each). The third bus connects to the FRU (field replaceable unit) EEPROM.

The DIMM's IIC buses are for the BIOS to retrieve information from each DIMM (such as type, size, etc.) to program the CNB20HE memory registers accordingly to boot system. The FRU EEPROM contains useful information for field services.

Below is the IIC address for all of the devices. The SKA4 baseboard implements a multiplexer that allows the two DIMM I2C busses to share the SMB bus from the OSB4. The two different memory module I2C busses are selected via GPIOs from the National* 87317. The I2C bus the FRU device resides on shares the baseboard's BMC Primary Private I2C Bus.

Table 4-1: I2C Address for Memory Module SMB

Device	Address	Selected Bus #
DIMM A3	A0	1
DIMM C3	A2	1
DIMM B3	A4	1
DIMM D3	A6	1
DIMM A1	A8	1
DIMM C1	AA	1
DIMM B1	AC	1
DIMM D1	AE	1
DIMM A4	AO	2
DIMM C4	A2	2
DIMM B4	A4	2
DIMM D4	A6	2
DIMM A2	A8	2
DIMM C2	AA	2

Device	Address	Selected Bus #
DIMM B2	AC	2
DIMM D2	AE	2
FRU EEPROM	0xACh	3

4.3.5 Clocks

Three clock buffers are on the memory module to generate zero delay, low skew and low jitter to the MADPs and DIMMs. The ICS2509 is a zero-delay buffer which takes the 100-MHz input clock from the baseboard and generates four 100-MHz clocks to the MADPs, and one Read Clock goes back to the CNB20HE.

The MADPs in turn generate 100-MHz clocks to drive the two ICS2510 low skew buffers. These two buffers drive 100-MHz clocks to the DIMMs and Read Clock back to the MADPs. Note that only two MADP output clocks are used to drive the two buffers. MADP has its own PLL and the design uses this PLL for zero-delay (instead of the PLL inside the ICS2510) between the MADP's outputs to the 100-MHz clocks to the DIMMs and the MADP's Read Clocks. Please refer to the Clock Generation and Distribution section for details.

4.4 SKA4 Memory Module Functional Block Diagram

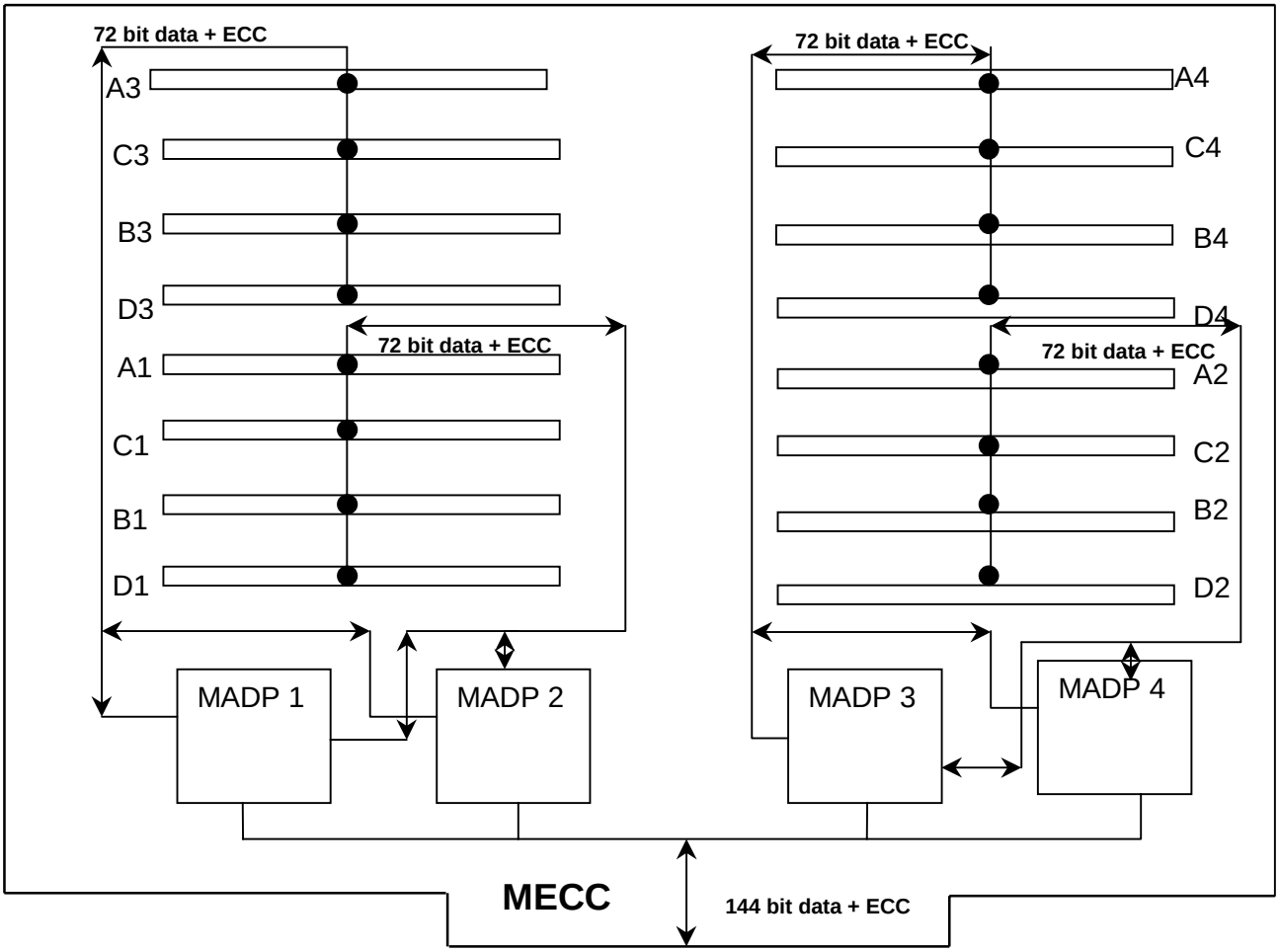

Figure 4-2: SKA4 Memory Module Functional Block Diagram

4.5 ECC Functionality

4.5.1 Single Bit Error (SBE)

Single-bit errors are correctable and the location of the bad DIMM and syndrome bits are logged in the System Error Log (SEL). On the SKA4 board, up to four data bits from four different "interleaves" can fail at the same time with the result being four SBEs - not a multiple bit error. If x4 DRAM are used, one DRAM can go bad without hanging the system. This functionality is achieved through the data routing on the memory board (through the MADP chips) such that each of the four bits from any x4 DRAM in any DIMM slot belongs to a different 36 bit interleave going back to the HE.

4.5.2 Double Bit Error (DBE)

Multi-bit errors are not correctable and only the bank where the error occurred can be isolated - as opposed to the location of the failed DIMM. In some cases, the bank location cannot be logged as MBEs continue to occur while executing the BIOS code that initiates the logging of the SEL message.

5. Clock Generation and Distribution

All buses on the SKA4 baseboard operate using synchronous clocks. Clock synthesizer/driver circuitry on the baseboard generates clock frequencies and voltage levels as required, including the following:

- 100 MHz at 2.5 V logic levels—For Slot 2 connectors, the CNB20HE, and the ITP port.
- 66 MHz at 3.3 V logic levels—For CNB20HE, CIOB and the CIOB PCI clock.
- 33.3 MHz at 3.3 V logic levels—Reference clock for the PCI bus clock driver.
- 16.67 MHz at 2.5 V logic levels—Processor and the OSB4 APIC bus clocks.
- 14.318 MHz at 3.3V logic levels—OSB4, Super I/O, and video clocks.

There are five main synchronous clock sources on the SKA4 baseboard:

- 100-MHz host clock generator for processors, the CNB20HE, and the ITP.
- 66-MHz clock for CNB20HE and the CIOB PCI clocks.
- 48-MHz clock for OSB4 USB.
- 33.3-MHz PCI reference clock.
- 16.67 MHz APIC.
- 14.318 MHz OSB4, Super I/O, and video clocks.

For information on processor clock generation, see the *CK133-WS Synthesizer/Driver Specification*.

The SKA4 baseboard also provides asynchronous clock generators:

- 40-MHz clock for the embedded SCSI controllers.
- 32-KHz clock for the OSB4 RTC.
- 22.1-MHz clock for the BMC.

The following figure illustrates clock generation and distribution on the SKA4 baseboard.

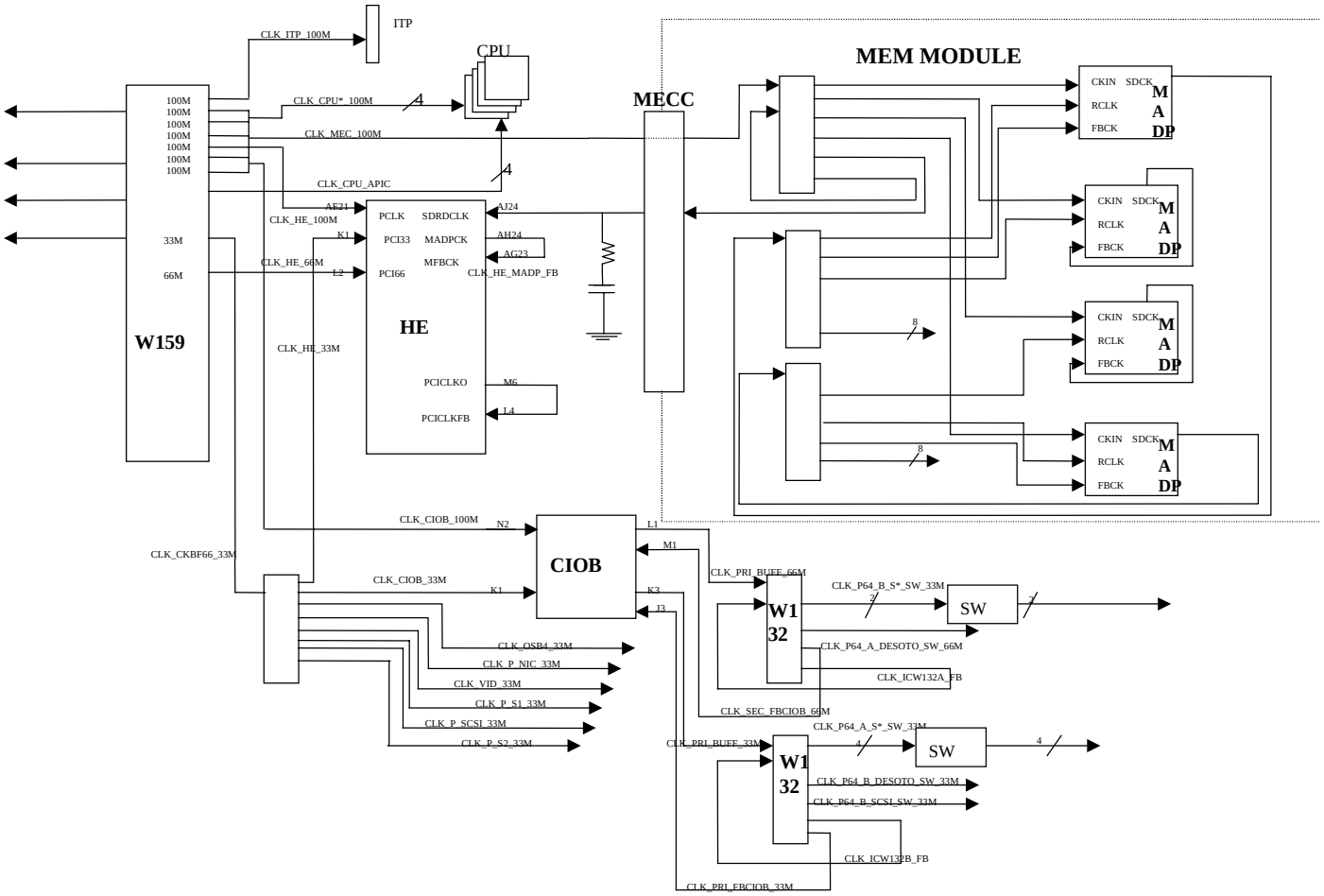

Figure 5-1: SKA4 Baseboard Clock Distribution

6. SKA4 Server Board ACPI Implementation

This section documents the SKA4 ACPI implementation.

6.1 ACPI

An ACPI aware OS generates an SMI to request that the system be switched into ACPI mode. The BIOS responds by sending the appropriate command to the BMC to enable ACPI mode. The system automatically returns to legacy mode upon hard reset or power-on reset.

The SKA4 platform supports S0, S1, S4, and S5 states. When the system is operating in ACPI mode, the OS retains control of the system and OS policy determines the entry methods and wake up sources for each sleep state – **sleep entry and wake up event capabilities are provided by the hardware but are enabled by the OS.**

6.1.1 Front Panel Switches

SKA4 supports up to four front panel buttons (via the front panel connector): the power button, the sleep button, the reset button, and a NMI button.

The power button input (FP_PWR_BTN*) in the SKA4 design is a request that is forwarded by the BMC to the power state machines in the National PC97317 Super I/O. It is monitored by the BMC and does not directly control power on the power supply.

The power button input and the sleep button input (FP_SLP_BTN*) behave differently depending on whether or not the operating system supports ACPI. The sleep switch has no effect unless an operating system with ACPI support is running. If the operating system supports ACPI and the system is running, pressing the sleep switch causes an event. The OS will cause the system to transition to the appropriate System State depending on the user settings.

Power Switch Off to On: The OSB4 and SIO may be configured to generate wake up events for several different system events: Wake-on-LAN*, PCI Power Management Interrupt, and Real Time Clock Alarm are examples of these events. The BMC monitors the power button and wake up event signals from the OSB4 and SIO. A transition from either source results in the BMC starting the power-up sequence. Since the processors are not executing, the BIOS does not participate in this sequence. The OSB4 and SIO receive power good and reset from the BMC and then transition to an ON state.

On to Off (Legacy): The SIO is configured to generate an SMI due to a power button event. The BIOS services this SMI and sets the state of the machine in the OSB4 and SIO to the OFF state. The BMC monitors power state signals from the SIO and de-asserts PS_PWR_ON to the power supply. As a safety mechanism, the BMC automatically powers off the system in 4-5 seconds, if the BIOS fails to service the SMI.

On to Off (ACPI): If an ACPI operating system is loaded, the power button switch generates a request (via SCI) to the OS to shutdown the system. The OS retains control of the system and OS policy determines what sleep state (if any) the system transitions into.

On to Sleep (ACPI): If an ACPI operating system is loaded, the sleep button switch generates a request (via SCI) to the OS to place the system in sleep mode. The OS retains control of the system and OS policy determines what sleep state (if any) the system transitions into.

Sleep to On (ACPI): If an ACPI operating system is loaded, the sleep button switch generates a wake event to the OSB4 and a request (via SCI) to the OS to place the system in the "On" state. The OS retains control of the system and OS policy determines what sleep state (if any) the system can wake from.

6.1.2 Wake Up Sources (ACPI and Legacy)

SKA4 hardware is capable of wake up from several sources under a non-ACPI configuration, e.g., when the operating system does not support ACPI. The wake up sources are defined in the table below. Under ACPI, the operating system programs the OSB4 and SIO to wake up on the desired event, but in legacy mode the BIOS enables/disables wake up sources based on a switch in Setup. It is required that the operating system or a driver clear any pending wake up status bits in the associated hardware (such as the Wake-on-LAN status bit in the LAN application specific integrated circuit (ASIC), or PCI power management event (PME) status bit in a PCI device). The legacy wake up feature is disabled by default.

Table 6-1: Supported Wake Events

Wake Event	Supported via ACPI (by sleep state)	Supported Via Legacy Wake
Power Button	Always wakes system	Always wakes system
Sleep Button	S1	No
Ring indicate from COMA	S1, S4, S5	Yes
Ring indicate from COMB	S1, S4, S5	Yes
PME from PCI 32/33	S1, S4, S5	Yes
PME from PCI 64/33	S1, S4, S5	No
PME from PCI 64/66	S1, S4, S5	No
BMC source (i.e. EMP)	Simulated as power button	Simulated as power button
RTC Alarm	S1, S4, S5	Yes
Mouse	S1	No
Keyboard	S1	No
USB	S1	Yes

7. SKA4 System Bus Error Monitoring

This section documents the types of system bus error conditions monitored by the SKA4 board set and how they propagate to SMI#.

7.1 Error Sources and Types

One of the major requirements of server management is to correctly and consistently handle system errors. System errors on the SKA4, which can be disabled and enabled individually or as a group, can be categorized as follows:

- PCI bus.
- Processor bus errors.
- Memory single and multi-bit errors.
- General Server Management sensors.

On the SKA4 platform, General Server Management sensors are managed by the BMC. See the Server Management section for specifics on these sensors.

7.1.1 PCI Bus Errors

The PCI bus defines two error pins, PERR# and SERR#, for reporting PCI parity errors and system errors, respectively. In the case of PERR#, the PCI bus master has the option to retry the offending transaction, or to report it using SERR#. All other PCI-related errors are reported by SERR#. SERR# is routed to NMI if enabled by BIOS.

7.1.2 Pentium® III Xeon™ Processor Bus Errors

The CNB20HE supports all the data integrity features supported by the Pentium Pro bus including Address, Request and Response parity. The CNB20HE always generates ECC data while it is driving the processor data bus although data bus ECC can be disabled or enabled by BIOS (enabled by default). The CNB20HE generates MIRQ# on single-bit errors (SBEs) and generates SALERT# on uncorrectable errors. In addition the CNB20HE can generate BERR# on unrecoverable ECC errors detected on the processor bus. Unrecoverable errors are routed to NMI by BIOS.

In the case of irrecoverable errors on the host processor bus, proper execution of SMI handler cannot be guaranteed and SMI handler cannot be relied upon to log such conditions. The BIOS SMI handler will record the error to the system event log only if the system has not experienced a catastrophic failure that compromises the integrity of the SMI handler. The BIOS always enables the error correction and detection capabilities of the processors by setting appropriate bits in processor model specific register (MSR).

7.1.3 Memory Bus Errors

The CNB20HE is programmed to generate an SMI on single-bit data errors in the memory array if ECC memory is installed. The CNB20HE performs the scrubbing. The SMI handler simply records the error and the DIMM location to the system event log. Double-bit errors in the memory array are mapped to SMI because the BMC cannot determine the location of the bad

DIMM. The double-bit errors may have corrupted the contents of SMRAM. The SMI handler will log the failing DIMM number to the BMC if the SMRAM contents are still valid. Unrecoverable errors are routed to NMI by BIOS.

If more than 10 single-bit errors occur in a time span less than 1 hour, the BIOS SMI handler will stop logging SBEs to avoid filling the event log. The BIOS would also prevent further single-bit errors from generating SMIs to avoid a condition known as SMI shock, a condition where the processors spend all their time servicing SMIs because of a stream of single-bit errors. Note that the chipset will continue to correct single-bit errors and the system will continue to work correctly even if one of the data lines on a DIMM gets stuck. The BIOS enables logging and SMIs the next time the system is rebooted.

7.1.4 Error Event Propagation to SMI#

The diagram below shows how specific error signals are propagated to SMI# on the SKA4 server board.

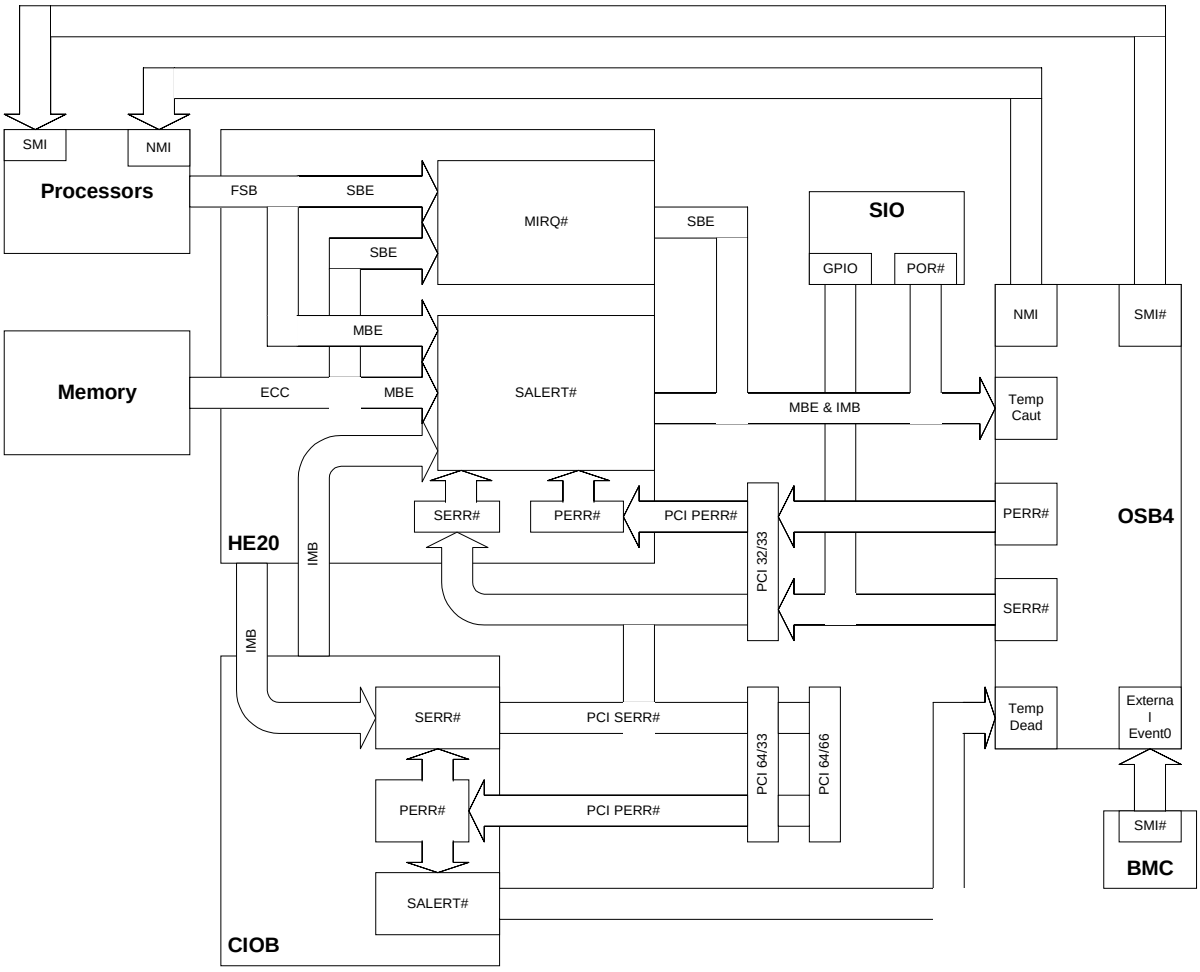

Figure 7-1: SKA4 Error Signal Propagation to SMI#

8. SKA4 Basic Input Output System (BIOS)

8.1 BIOS Overview

The term BIOS, as used in the context of this document, refers to the system BIOS, the BIOS Setup and option ROMs for onboard peripheral devices that are contained in the system flash. System BIOS controls basic system functionality using stored configuration values. The terms flash ROM, system flash, BIOS flash, and 28F008S5 may be used interchangeably in this document.

The term BIOS Setup refers to the flash ROM-resident Setup utility that provides the user with control of configuration values stored in battery-backed CMOS configuration RAM. The System Setup Utility (SSU) is covered in a separate document. BIOS Setup is closely tied with the system BIOS and is considered a part of BIOS.

The Flash Memory Update utility (iFlash) is used to load predefined areas of flash ROM with Setup, BIOS, and other code/data.

8.1.1 System BIOS

The system BIOS is the core of the flash ROM-resident portion of the BIOS. The system BIOS provides standard PC-BIOS services and support for some new industry standards, such as the *Advanced Configuration and Power Interface Specification, Revision 1.0*, Hot-plug PCI, and *Wired For Management Baseline Specification*, *Revision 2.0*. In addition, the system BIOS supports certain features that are common across all the Intel® servers. These include security, MPS support, server management and error handling, CMOS configuration RAM management, OEM customization, PCI and Plug and Play (PnP) BIOS interface, console redirection, and resource allocation support. BIOS setup is embedded in flash ROM and provides the means to configure onboard hardware devices and add-in cards.

8.1.2 Flash Update Utility

The system BIOS and the setup utility are resident in partitioned flash ROM. The device is in-circuit reprogrammable. On the SKA4 platform, 1 MB of flash ROM is provided by the 28F008S5. Recovery boot block protection is accomplished through the use of the 28F008S5 software locking mechanisms. The SKA4 BIOS does not support a SecureBIOS feature like some server products from Intel. Adding SecureBIOS increases boot time, and complexities, but does not provide compelling benefits for the SKA4 platform.

The iFlash Utility may be used to reprogram the BIOS operational code located in the flash ROM. A BIOS image is provided on a diskette in the form of several binary files that are read by the iFlash Utility. The utility compares the board ID against the ID in the load files to protect against reprogramming the flash ROM with the BIOS for a different, incompatible platform. Baseboard revisions may create hardware incompatibilities and may require different BIOS code.

8.1.2.1 System Flash ROM Layout

The flash ROM contains system initialization routines, BIOS strings, BIOS Setup, and run-time support routines. The exact layout is subject to change, as determined by Intel. A 16 KB user

block is available for user ROM code and another 16 KB block is available for custom logos. The flash ROM also contains compressed initialization code for onboard peripherals such as SCSI, NIC, and video controllers. The complete ROM is visible, starting at physical address 4 GB less 1 MB. The BIOS alone needs to know the exact map. The BIOS image contains all the BIOS components at appropriate locations. The Flash Memory Update Utility can be used to reprogram the BIOS operational code areas.

At run time, none of the flash blocks are visible at the aliased addresses below 1 MB due to shadowing. Intel reserves the right to change the flash map without notice.

A 32 KB parameter block in the flash ROM is dedicated to storing configuration data that controls extended system configuration data (ESCD), onboard SCSI configuration, OEM configuration areas, etc. The block is partitioned into separate areas for logically different data. Application software must use standard advanced programmable interrupts (APIs) to access these areas and may not access the data directly.

8.2 Revision History Format

The BIOS Revision Identification is used to track board, OEM, and build revision information for any given BIOS. This identifier can be a maximum of 32 characters. The first 28 characters have been defined using the following format:

The figure below illustrates a standard 32-byte BIOS ID.

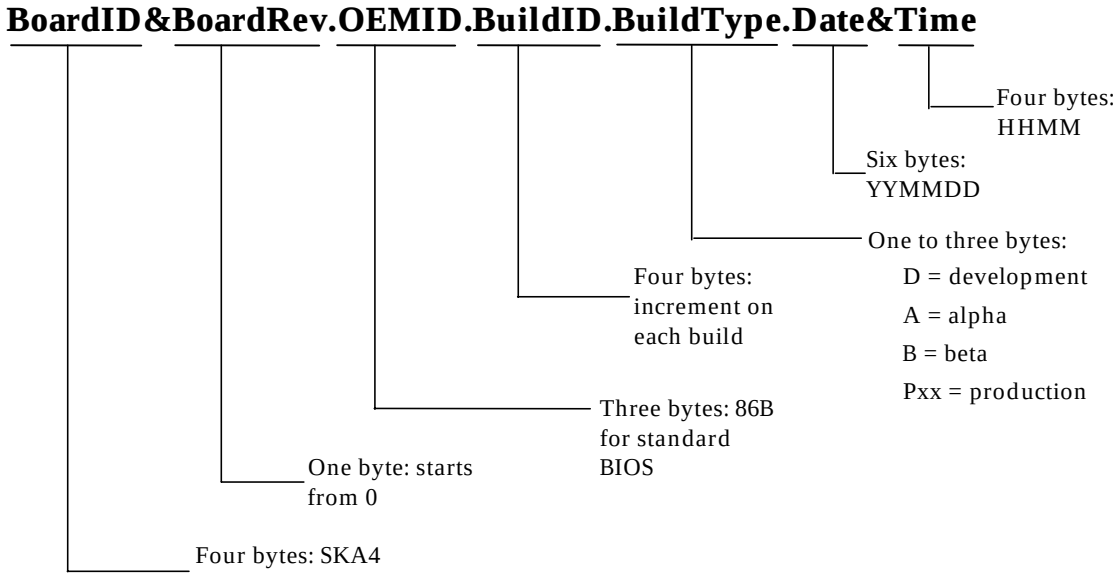

Figure 8-1: Standard 32-byte BIOS ID

8.3 Error Handling

This chapter defines how errors are handled by the system BIOS on the SKA4 platform. Also discussed is the role of BIOS in error handling, and the interaction between the BIOS, platform

hardware, and server management firmware with regard to error handling. In addition, error logging techniques are described and beep codes for errors are defined.

8.3.1 Error Sources and Types

One of the major requirements of server management is to correctly and consistently handle system errors. System errors on the SKA4, which can be disabled and enabled individually or as a group, can be categorized as follows:

- PCI bus.
- Memory single- and multi-bit errors.
- Sensors.
- Processor internal error, bus/address error, thermal trip error, temperatures and voltages, and GTL voltage levels.

On the SKA4 platform, sensors are managed by the BMC. The BMC is capable of receiving event messages from individual sensors and logging system events.

8.3.2 SMI Handler

The SMI handler is used to handle and log system level events that are not visible to the server management firmware. If the SMI handler control bit in Setup is disabled, no SMI signals are generated on system errors. If enabled, all system errors are preprocessed by the SMI handler, even those that are normally considered to generate an NMI. The SMI handler sends a command to the BMC to log the event and provides the data to be logged. For example, BIOS programs CNB20HE and OSB4 to generate SMI on a single-bit memory error and logs the location of the faulty DIMM in the system event log. System events that are handled by the BIOS generate SMI.

8.3.3 Handling and Logging System Errors

This section describes actions taken by the SMI handler with respect to the various categories of system errors. It covers the events logged by the BIOS and the format of data bytes associated with those events. The BIOS is responsible for monitoring and logging certain system events. BIOS sends a platform event message to BMC to log the event. Some of the errors, such as processor failure, are logged during early POST and not through SMI handler.

8.3.3.1 Logging Format Conventions

The BIOS complies with the *Intelligent Platform Management Interface Specification, Revision 1.0*. The BIOS always uses system software ID within the range 20h-27h to log errors. As a result, the generator ID byte will be an odd number in the range 41h-4fh. OEM user binary should use software IDs of 1 and SMM User Binary should use an ID of 11h. The Software ID allows external software to find the origin of the event message.

The BIOS uses the following format when logging events. Note that detection of some of the errors listed below may not be supported by hardware and will never get logged in a SKA4 platform. Note also that the event reading/type code has changed to 6F in accordance with *IPMI Specification Version 1.0*.

Table 8-1: System Event Logging Format

Event Types	Sensor Type	Sensor # [1]	Type Code	Data Bytes 1,2,3
Single-bit Memory Error	0Ch	xx	6Fh	A0h, card/DIMM#, Syndrome[2]
Multi-bit Memory Error	0Ch	xx	6Fh	A1h, card/DIMM#, Syndrome[3]
System Bus Correctable Error[4]	13h	xx	6Fh	07h, 0FFh, 0FFh
System Bus Uncorrectable Error[5]	13h	xx	6Fh	08h, 0FFh, 0FFh
PCI PERR	13h	xx	6Fh	24h, BUS#, 0FFh
PCI SERR[6]	13h	xx	6Fh	25h, BUS#, 0FFh
PCI DATA Parity Error	13h	xx	6Fh	26h, BUS#, 0FFh
ECC Logging Disabled	10h	xx	6Fh	00h, 0FFh, 0FFh
IMB Command Failure	13h	xx	6Fh	60h, IMB Command#, 0FFh

Notes:

1. Sensor # = 0xx (don't care). The system BIOS "sensors" are just logical entities that generate events. BIOS should make sure that each different combination of sensor type (e.g., memory) and event type (e.g., sensor-specific) has a different sensor number. Software should ignore these values.
2. The format of these data bytes was changed to allow consistency between multiple platforms. For the SKA4 platform, the memory card number field will always be 0 and the data byte 2 will be equal to the DIMM number.
3. The format of these data bytes was changed to allow consistency between multiple platforms. For the SKA4 platform, the memory card number field will always be 0 and the data byte 2 will be equal to the DIMM number.
4. Errors reported by this event include Processor Bus Correctable Error, IMB Bus Retry Error and IMB Bus Timeout Error.
5. Errors reported by this event include Processor Bus Uncorrectable Error, Processor Bus AERR#, Processor Bus BERR#, Processor Bus BINIT#, Processor Bus Protocol Error, IMB Bus Parity Error, IMB Bus Sequence Error, IMB Bus Generic Error, IMB Bus Command Error, and IMB Bus Data Error.
6. Errors reported by this event include PCI SERR#, Received Target Abort, and Address Parity Error.

8.3.3.2 PCI Bus Error

The PCI bus defines two error pins, PERR# and SERR#, for reporting PCI parity errors and system errors, respectively. The BIOS can be instructed to enable or disable reporting PERR# and SERR# through NMI.[1] In the case of PERR#, the PCI bus master has the option to retry the offending transaction, or to report it using SERR#. All other PCI-related errors are reported by SERR#. SERR# is routed to NMI if bit 2 of I/O register 61 is set to 0. In the SKA4 platform, all the PCI-to-PCI bridges are configured so that they generate SERR# on the primary interface whenever there is SERR# on the secondary side, if SERR# is enabled through Setup. The same is true for PERR#. Two OEM data bytes are present. The first OEM byte indicates the PCI bus number. The second OEM byte encodes the PCI device number and the PCI function number in a standard manner. The most significant five bits have the device number and the other three bits indicate the function number. The offset from the event trigger field determines whether it was a PERR or SERR.

8.3.3.3 Pentium® III Xeon™ Processor Bus Error

In the case of irrecoverable errors on the host processor bus, proper execution of SMI handler cannot be guaranteed and SMI handler cannot be relied upon to log such conditions. The BIOS SMI handler will record the error to the system event log only if the system has not experienced

[1] Disabling NMI for PERR# and/or SERR# also disables logging of the corresponding event.

a catastrophic failure that compromises the integrity of the SMI handler. The BIOS always enables the error correction and detection capabilities of the processors by setting appropriate bits in processor model specific register.

8.3.3.4 Memory Bus Error

The CNB10HE and OSB4 are programmed to generate an SMI on single-bit data errors in the memory array if ECC memory is installed. The CNB20HE performs the scrubbing. The SMI handler simply records the error and the DIMM location to the system event log. Double-bit errors in the memory array are mapped to SMI because the BMC cannot determine the location of the bad DIMM. The double-bit errors may have corrupted the contents of SMRAM. The SMI handler will log the failing DIMM number to the BMC if the SMRAM contents are still valid.

In both cases, the event message contains two OEM data bytes. The DIMM number (as indicated by the memory board silkscreen) and the syndrome byte is included in the OEM data byte in this record. The instrumentation software can use information provided in SM BIOS specification tables to get the DIMM slot label. The syndrome information can be used to determine the data bit in error. If the error is detected during the initial memory sizing (POST code 28) only the bank number of DIMM will be reported (4 DIMM granularity.) If a single-bit error is detected during the memory test at POST code 60, a single DIMM number will be identified. If a multiple-bit error is detected during the memory test at POST code 60, a pair of DIMMs will be identified.

If more than 10 single-bit errors occur in a time span less than 1 hour, the BIOS SMI handler will stop logging SBEs to avoid filling the event log. The BIOS would also prevent further single-bit errors from generating SMIs to avoid a condition known as SMI shock, a condition where the processors spend all their time servicing SMIs because of a stream of single-bit errors. Note that the chipset will continue to correct single-bit errors and the system will continue to work correctly even if one of the data lines on a DIMM gets stuck. The BIOS enables logging and SMIs the next time the system is rebooted.

8.3.3.5 System Limit Error

The BMC monitors system operational limits. It manages the A/D converter, defining voltage and temperature limits as well as fan senses and chassis intrusion. Any sensor values outside of specified limits are fully handled by BMC and there is no need to generate an SMI to the host processor.

Refer to the *SKA4 Server Management External Architecture Specification* for details on various sensors and how they are managed.

8.3.3.6 Processor Failure

The BIOS detects processor BIST failure and logs this event. The failed processor can be identified by the first OEM data byte field in the log. For example, if processor 0 fails, the first OEM data byte will be 0. The BIOS will depend upon BMC to log the watchdog timer reset event.

If an OS device driver is using the watchdog timer to detect software or hardware failures and that timer expires, an Asynchronous Reset (ASR) is generated, which is equivalent to a hard

reset. The POST portion of the BIOS can query BMC for watchdog reset event as the system reboots, and logs this event in the system event log (SEL).

8.3.3.7 Boot Event

The BIOS downloads the system date and time to the BMC during POST and logs a boot event. This does not indicate an error, and software that parses the event log should treat it as such.

8.4 Error Messages and Error Codes

The system BIOS displays error messages on the video screen. Prior to video initialization, beep codes inform the user of errors. POST error codes are logged in the event log.

The BIOS displays POST error codes on the video monitor. The error codes are defined by Intel and whenever possible are backward-compatible with error codes used in the MB440LX platform.

Following are definitions of POST error codes, POST beep codes, and system error messages.

8.4.1 POST Codes

The BIOS indicates the current testing phase during POST after the video adapter has been successfully initialized by writing a 2-digit hex code to I/O location 80h. If a Port-80h card (Postcard*) is installed, it displays this 2-digit code on a pair of hex display LEDs.

Table 8-2: Port-80h Code Definition

Code	Meaning
CP	Phoenix check point (port-80) code

The following table contains the port-80 codes displayed during the boot process. A beep code is a series of individual beeps on the PC speaker, each of equal length. The following table describes the error conditions associated with each beep code and the corresponding POST check point code as seen by a port 80h card. For example, if an error occurs at checkpoint 22h, a beep code of 1-3-1-1 is generated. The beep codes 1-1-1-1, 1-5-1-1, 1-5-2-1 and 1-5-3-1 are reserved for BMC usage.

Table 8-3: Standard BIOS Port-80 Codes

CP	Beeps	Reason
xx	1-1-1-1	There are no processors present in the system, or the processors are so incompatible that the system BIOS cannot be run (like mismatched cache voltages)
02		Verify Real Mode
04		Get processor type
06		Initialize system hardware
08		Initialize chipset registers with initial POST values
09		Set in POST flag
0A		Initialize processor registers

CP	Beeps	Reason
0B		Enable processor cache
0C		Initialize caches to initial POST values
0E		Initialize I/O
0F		Initialize the local bus IDE
10		Initialize Power Management
11		Load alternate registers with initial POST values
12		Restore processor control word during warm boot
14		Initialize keyboard controller
16	1-2-2-3	BIOS ROM checksum
18		8254 timer initialization
1A		8237 DMA controller initialization
1C		Reset Programmable Interrupt Controller
20	1-3-1-1	Test DRAM refresh
22	1-3-1-3	Test 8742 Keyboard Controller
24		Set ES segment register to 4GB
28	1-3-3-1	Autosize DRAM, system BIOS stops execution here if the BIOS does not detect any usable memory DIMMs
2A		Clear 8 MB base RAM
2C	1-3-4-1	Base RAM failure, BIOS stops execution here if entire memory is bad
32		Test processor bus-clock frequency
34		Test CMOS
35		RAM initialize alternate chipset registers
36		Warm start shut down
37		Reinitialize the chipset
38		Shadow system BIOS ROM
39		Reinitialize the cache
3A		Autosize cache
3C		Configure advanced chipset registers
3D		Load alternate registers with CMOS values
40		Set Initial Processor speed new
42		Initialize interrupt vectors
44		Initialize BIOS interrupts
46	2-1-2-3	Check ROM copyright notice
47		Initialize manager for PCI Option ROMs
48		Check video configuration against CMOS
49		Initialize PCI bus and devices
4A		Initialize all video adapters in system
4B		Display QuietBoot screen
4C		Shadow video BIOS ROM
4E		Display copyright notice
50		Display processor type and speed
52		Test keyboard
54		Set key click if enabled
55		USB initialization
56		Enable keyboard

CP	Beeps	Reason
58	2-2-3-1	Test for unexpected interrupts
5A		Display prompt "Press F2 to enter SETUP"
5C		Test RAM between 512 and 640k
60		Test extended memory
62		Test extended memory address lines
64		Jump to UserPatch1
66		Configure advanced cache registers
68		Enable external and processor caches
6A		Display external cache size
6B		Load custom defaults if required
6C		Display shadow message
6E		Display non-disposable segments
70		Display error messages
72		Check for configuration errors
74		Test real-time clock
76		Check for keyboard errors
7A		Test for key lock on
7C		Set up hardware interrupt vectors
7D		Intelligent system monitoring
7E		Test coprocessor if present
80		Detect and install external RS232 ports
82		Detect and install external parallel ports
85		Initialize PC-compatible PnP ISA devices
86		Re-initialize on board I/O ports
88		Initialize BIOS Data Area
8A		Initialize Extended BIOS Data Area
8C		Initialize floppy controller
90		Initialize hard disk controller
91		Initialize local bus hard disk controller
92		Jump to UserPatch2
93		Build MPTABLE for multi-processor boards
94		Disable A20 address line
95		Install CD-ROM for boot
96		Clear huge ES segment register
98	1-2	Search for option ROMs. One long, two short beeps on checksum failure
9A		Shadow option ROMs
9C		Set up Power Management
9E		Enable hardware interrupts
A0		Set time of day
A2		Check key lock
A4		Initialize typematic rate
A8		Erase F2 prompt
AA		Scan for F2 key stroke
AC		Enter SETUP
AE		Clear in-POST flag

CP	Beeps	Reason
B0		Check for errors
B2		POST done – prepare to boot operating system
B4	1	One short beep before boot
B5		Display MultiBoot menu
B6		Check password, password is checked before option ROM scan
B7		ACPI initialization
B8		Clear global descriptor table
BC		Clear parity checkers
BE		Clear screen (optional)
BF		Check virus and backup reminders
C0		Try to boot with INT 19
C8		Forced shutdown
C9		Flash recovery
DO		Interrupt handler error
D2		Unknown interrupt error
D4		Pending interrupt error
D6		Initialize option ROM error
D8		Shutdown error
DA		Extended Block Move
DC		Shutdown 10 error

Table 8-4: Recovery BIOS Port-80 Codes

CP	Beeps	Reason
xx	1-1-1-1	There are no processors present in the system, or the processors are so incompatible that the system BIOS cannot be run (like mismatched cache voltages).
E0		Initialize chipset
E1		Initialize bridge
E2		Initialize processor
E3		Initialize timer
E4		Initialize system I/O
E5		Check forced recovery boot
E9		Set 4 GB segment limits
E6		Validate checksum
E7		Go to BIOS
E8		Initialize processors
E9		Set 4 GB segment limits
EA		Perform platform initialization
EB		Initialize PIC and DMA
EC		Initialize memory type
ED		Initialize memory size
EE		Shadow boot block
EF		Test system memory
F0		Initialize interrupt services
F1		Initialize real time clock
F2		Initialize video

CP	Beeps	Reason
F3		Initialize beeper
F4		Initialize boot
F5		Restore segment limits to 64 KB
F6		Boot mini DOS
F7		Boot full DOS

8.4.2 POST Error Codes and Messages

The following table defines POST error codes and their associated messages. The BIOS will prompt the user to press a key in case of serious errors. Some of the error messages are preceded by the string "Error" to highlight the fact that these indicate a system that might be malfunctioning. All POST errors and warnings are logged in the system event log unless it is full.

Table 8-5: POST Error Messages and Codes

Code	Error Message	Pause on Error
0200	Failure Fixed Disk	No
0210	Stuck Key	No
0211	Keyboard Error	No
0212	Keyboard Controller Failed	Yes
0213	Keyboard Locked - Unlock key switch	Yes
0220	Monitor type does not match CMOS - Run SETUP	No
0230	System RAM Failed at offset:	No
0231	Shadow Ram Failed at offset:	No
0232	Extended RAM Failed at offset:	No
0233	Memory type mix	No
0234	Memory Ecc single	No
0235	Memory Ecc multiple	No
0250	System battery is dead - Replace and run SETUP	Yes
0251	System CMOS checksum bad - Default configuration used	No
0260	System timer error	No
0270	Real time clock error	No
0271	Check date and time settings	No
0297	Base (Extended) memory error: DIMM Jx	Yes
02B2	Incorrect Drive A type - run SETUP	No
02B3	Incorrect Drive B type - run SETUP	No
02D0	System cache error - Cache disabled	No
02F5	DMA Test Failed	Yes
02F6	Software NMI Failed	No
0401	Invalid System Configuration Data - run configuration utility	No
None	System Configuration Data Read Error	No
0403	Resource Conflict	No
0404	Resource Conflict	No
0405	Expansion ROM not initialized	No
0406	Warning: IRQ not configured	No
0504	Resource Conflict	No

Code	Error Message	Pause on Error
0505	Expansion ROM not initialized	No
0506	Warning: IRQ not configured	No
0601	Device configuration changed	No
0602	Configuration error - device disabled	No
8100	Processor 1 failed BIST	Yes
8101	Processor 2 failed BIST	Yes
8102	Processor 3 failed BIST	Yes
8103	Processor 4 failed BIST	Yes
8104	Processor 1 Internal Error (IERR) failure	Yes
8105	Processor 2 Internal Error (IERR) failure	Yes
8106	Processor 1 Thermal Trip failure	Yes
8107	Processor 2 Thermal Trip failure	Yes
8108	Watchdog Timer failed on last boot	No
810A	Processor 1 failed initialization on last boot	No
810B	Processor 1 failed initialization	No
810C	Processor 1 disabled	No
810D	Processor 2 disabled	No
810E	Processor 1 failed FRB-3 timer	Yes
810F	Processor 2 failed FRB-3 timer	Yes
8110	Server Management Interface failed to function	Yes
8112	BMC in update mode	No
8121	2:1 core to bus speed ratio: Processor cache disabled	No
8128	Processor 3 Internal error (IERR)	Yes
8129	Processor 4 Internal error (IERR)	Yes
8130	Processor 3 Thermal Trip error	Yes
8131	Processor 4 Thermal Trip error	Yes
8138	Processor 3 failed FRB-3 timer	Yes
8139	Processor 4 failed FRB-3 timer	Yes
8140	Processor 3 disabled	Yes
8141	Processor 4 disabled	Yes
8148	Processor 2 failed initialization on last boot	Yes
8149	Processor 3 failed initialization	Yes
814A	Processor 4 failed initialization	Yes
814B	BMC in Update Mode	Yes
8150	NVRAM Cleared by Jumper	Yes
8151	NVRAM CRC cleared	No
8152	ESCD Data cleared	No
8153	Password Cleared by Jumper	Yes
8160	Unable to apply BIOS Update for Processor 4	No
8161	Unable to apply BIOS Update for Processor 3	No
8162	Unable to apply BIOS Update for Processor 2	No
8163	Unable to apply BIOS Update for Processor 1	No
8168	Processor 4 L2 cache failed	Yes
8169	Processor 3 L2 cache failed	Yes
816A	Processor 2 L2 cache failed	Yes

Code	Error Message	Pause on Error
816B	Processor 1 L2 cache failed	Yes
8170	BIOS does not support current stepping for Processor 4	No
8171	BIOS does not support current stepping for Processor 3	No
8172	BIOS does not support current stepping for Processor 2	No
8173	BIOS does not support current stepping for Processor 1	No
8181	Mismatch among Processors detected	No
8182	L2 cache size mismatch	No
8187	Processor FSB speed mismatch	Yes
8250	All Memory modules failed memory test, system halted	Yes (system halted)
8400	Switch fault on PCI hot-plug	No

8.4.3 Additional Diagnostic Beep Codes

In addition to the POST codes and POST error codes and messages, the BMC generates beep codes upon detection of the failure conditions listed below.

Table 8-6: BMC Beep Codes

Code	Reason for Beep
1-5-2-1	Empty processor slot or wrong type of processor installed (12/5V vs. expected 2.8 V)
1-5-3-1	L2 cache voltage ID mismatch, modules 1&2
1-5-3-2	L2 cache voltage ID mismatch, modules 3&4
1-5-1-1	FRB failure
1-5-4-1	240VA failure
1-5-4-2	Power fault: DC power unexpectedly lost
1-5-4-3	PIIX4 control failure
1-5-4-4	Power control fault

8.5 OEM Customization

An OEM can customize the SKA4 BIOS for product differentiation. The extent of customization is limited to what is stated in this section. OEMs can change the BIOS look and feel by adding their own splash screen/logo. OEMs can manage OEM-specific hardware, if any, by executing their own code during POST by using the “User-supplied BIOS Code Support.”

8.5.1 User-supplied BIOS Code Support

A 16 KB region of flash ROM is available to store a user binary. The iFlash utility allows the OEM or end user to update the user binary region with OEM supplied code and/or data. At several points throughout POST, control is passed to this user binary. Intel provides tools and reference code to help OEMs create a user binary. The user binary must adhere to the following requirements:

- To allow detection by BIOS and protection from run time memory managers, the user binary must have an option ROM header (i.e., 55AAh, size).

- The system BIOS performs a scan of the user binary area at predefined points during POST. Mask bits must be set within the user binary to inform the BIOS which entry points exist.
- System state must be preserved by the user binary (all registers, including extended and MMX, stack contents, and nonuser binary data space, etc.).
- The user binary code must be relocatable. The user binary is located within the first 1 MB of memory. The user binary code must not make any assumptions about the value of the code segment.
- The user binary code is always executed from RAM and never from flash.
- The user binary must not hook critical interrupts, must not reprogram the chipset, and must not take any action that affects the correct functioning of the system BIOS.

The BIOS copies the user binary into system memory before the first scan point. If the user binary reports that it does not contain run time code, it is located in conventional memory (0-640K). Reporting that the user binary has no run time code has the advantage of not using limited option ROM space (therefore, more option ROMs may be executed in a large system configuration). If user binary code is required at run time, it is copied into and executed from option ROM space (0C8000H – 0E7fffH). At each scan point during POST, the system BIOS determines if the scan point has a corresponding user binary entry point to transfer control to the user binary. Presence of a valid entry point in the user binary is determined by examining the bitmap at byte 4 of the user binary header; each entry point has a corresponding “presence” bit in this bitmap. If the bitmap has the appropriate bit set, an entry point ID is placed in the “AL” register and execution is passed to the address computed by (ADR(Byte 5)+5*scan sequence #).

During execution, the user binary may access 11 bytes of extended BIOS data area RAM (EBDA). The segment of EBDA can be found at address 40:0e. Offset 18h through offset 22h is available for the user binary. The BIOS also reserves 16 CMOS bits for the user binary. These bits are in an unchecksummed region of CMOS with default values of zero, and will always be located in the first bank of CMOS. These bits are contiguous, but are not in a fixed location. Upon entry into the user binary, DX contains a ‘token’ that points to the reserved bits. This token is of the following format:

MSB LSB

15			12	11											0
# of bit available –1				Bit offset from start of CMOS of first bit											

The most significant four bits are equal to the number of CMOS bits available minus one. This field is equal to seven, since there are eight CMOS bits available. The 12 least significant bits define the position of the CMOS bit in the real-time clock. This is a bit address rather than a byte address. The CMOS byte location is 1/8th of the 12-bit number, and the remainder is the starting bit position within that byte. For example, if the 12-bit number is 0109h, user binary can use bit 1 of CMOS byte 0108h/8 or 021h. It should be noted that the bits available to the user binary may span more than one byte of CMOS (i.e., a value of 07084h indicates that the upper nibble of byte 10h and the lower nibble of byte 11h are reserved for the user binary).

The following code fragment shows the header and format for a user binary:

```
            db    55h, 0AAh, 20h   ; 16KB USER Area

MyCode      PROC  FAR              ; MUST be a FAR procedure
            db    CBh              ; Far return instruction
                                   ;
            db    04h              ; Bit map to define call points, a 1
                                   ; in any bit specifies
                                   ; that the BIOS is called at that
                                   ; scan point in POST
            db    CBh              ; First transfer address used to
                                   ; point to user binary extension
                                   ; structure
            dw    ?                ; Word Pointer to extension
                                   ; structure
            dw    0                ; Reserved

            JMP   ErrRet           ; This is a list of 7 transfer
                                   ; addresses, one for each
            JMP   ErrRet           ; bit in the bitmap.
                                   ; 5 Bytes must be used for each
            JMP   Start            ; JMP to maintain proper offset for
                                   ; each entry.  Unused entry JMP's
                                   ; should be filled with 5 byte
                                   ; filler or JMP to a RETF
            JMP   ErrRet           ;
            JMP   ErrRet
            JMP   ErrRet
            JMP   ErrRet
```

8.5.1.1 Scan Point Definitions

The table below defines the bitmap for each scan point, indicating when the scan point occurs and which resources are available (RAM, stack, binary data area, video, and keyboard).

Table 8-7: User Binary Area Scan Point Definitions

Scan Point	Mask	RAM/Stack/BDA	Video/Keyboard
Near pointer to the user binary extension structure, mask bit is 0 if this structure is not present. Instead of a jump instruction the scan address (offset 5) contains an 0CB followed by a near pointer.	01h	Not applicable	Not applicable
Obsolete. No action taken.	02h	NA	NA
This scan occurs immediately after video initialization.	04h	Yes	Yes
This scan occurs immediately before video initialization.	08h	Yes	No
This scan occurs on POST error. On entry, BX contains the number of the POST error.	10h	Yes	Yes

Scan Point	Mask	RAM/Stack/BDA	Video/Keyboard
This final scan occurs immediately prior to the INT 19 for normal boot and allows one to completely circumvent the normal INT 19 boot if desired.	20h	Yes	Yes
This scan occurs immediately before the normal option ROM scan.	40h	Yes	Yes
This scan occurs immediately following the option ROM area scan.	80h	Yes	Yes

Table 8-8: Format of the User Binary Information Structure

Offset	Bit definition
0	Bit 0 = 1 if mandatory user binary, 0 if not mandatory. If a user binary is mandatory, it will always be executed. If a platform supports a disabling of the user binary scan through Setup, this bit will override Setup setting. Bit 1 - 1 if runtime presence required (other than SMM user binary portion, SMM user binary will always be present in runtime irrespective of setting of this bit). 0, if not required in runtime, and can be discarded at boot time. Bit 7:2 – reserved for future expansion.
1 - 0fh	Reserved for future expansion.

If this structure is not present (bit 0 of the scan point structure is not set), the system BIOS assumes that the user binary is not mandatory (bit 0 in User Binary Information Structure assumed cleared), and it is required in run time (bit 1 in User Binary Information Structure assumed set).

8.5.2 OEM Splash Screen

A 16 KB region of Flash ROM is available to store the OEM logo in compressed format. The BIOS will contain the standard Intel logo. Using the iFlash utility, this region can be updated with OEM supplied logo image. The OEM logo must fit within 640 X 384 size to accommodate the progress meter at the top and hotkey messages at the bottom. If OEM logo is flashed into the system, it will override the built in Intel logo.

Intel supplies utilities that will compress and convert a 16 color bitmap file into a logo file suitable for iFlash. Intel also supplies a blank logo. If the logo area is updated with a blank logo, the system will behave as if there is no logo and it will always display the POST diagnostic screen.

8.6 Flash Update Utility

The Flash Memory Update Utility (iFlash) loads a fresh copy of the BIOS into flash ROM. The loaded code and data include the following:

- Onboard video BIOS, network controller BIOS, and SCSI BIOS.
- Setup utility.
- User-definable flash area (user binary area).
- OEM logo.

When running iFlash in interactive mode, the user may choose to update a particular flash area. Updating a flash area takes a file or series of files from a hard or floppy disk, and loads it in the

specified area of flash ROM. In interactive mode, iFlash can display the header information of the selected files.

Note: The iFlash utility must be run without the presence of a 386 protected mode control program, such as Windows* or EMM386. iFlash uses the processor's flat addressing mode to update the flash part.

Other platforms have shown interactions between system sensor event logging, and the iFlash. In the SKA4 platform, sensor event logging is not performed via SMI, thus there are no potential interactions to affect/corrupt flash.

8.6.1 Loading the System BIOS

A new SKA4 BIOS is contained in .bIx files. The number of .bIx files is determined by the size of the SKA4 BIOS area in the flash part. As of this writing, the system BIOS area contains 12 files (896 KB). The number of files is constrained by the fact that the image and the utilities fit in a single 1.44 MB DOS bootable floppy. The files are named as follows:

```
xxxxxxxx.BI0
xxxxxxxx.BI1
xxxxxxxx.BI2
```

The first eight letters of each filename on the release diskette can be any value, but cannot be renamed. Each file contains a link to the next file in the sequence. iFlash does a link check before updating to ensure that the process is successful. The first file in the list can be renamed, but all subsequent file names must remain unchanged.

Once an update of the system BIOS is complete, the user is prompted for a reboot. Language files are overwritten by updating the system BIOS. If a custom language file has been created, it must be flashed in after the system BIOS has been updated. The user binary area is also updated during a system BIOS update. User binary can be updated independently of the system BIOS. CMOS is not cleared when the system BIOS is updated in normal or recovery mode. Configuration information like ESCD is not overwritten during BIOS flash update.

8.6.2 User Binary Area

The SKA4 includes a 16 KB area in flash for implementation-specific OEM add-ons. The user binary area can be saved and updated exactly as described above. Only one file is needed. The valid extension for user files is .usr.

8.6.3 Language Area

The system BIOS language area can be updated only by updating the entire BIOS. The SKA4 platform supports English, Spanish, French, German, Italian, and Japanese. Intel provides translations for all the strings in six languages. These languages are selectable using Setup.

8.6.4 Recovery Mode

In the case of a corrupt .bIx image or an unsuccessful update of the system BIOS, the SKA4 platform can boot in recovery mode. To place the SKA4 platform into recovery mode, move the boot option jumper to recovery position. The jumper forces normal BIOS execution in default

position. Recovery mode may also be initiated automatically, if the checksum on the operational BIOS code is determined to be invalid.

Recovery mode requires at least 4 MB of RAM. Also, drive A: must be set up to support a 3.5” 1.44 MB floppy drive. This is the mode of last resort, used only when the main system BIOS will not come up. In recovery mode operation, iFlash (in noninteractive mode only) automatically updates the main system BIOS. iFlash senses that the SKA4 platform is in recovery mode and automatically attempts to update the system BIOS.

Before powering up the SKA4, obtain a bootable MS-DOS* diskette that contains a copy of the BIOS release. Boot the system from drive A: using this diskette, which executes a special AUTOEXEC.BAT file from the BIOS release. The batch file invokes iFlash, which updates the flash ROM with the BIOS found on the diskette.

Note: During recovery mode, video will not be initialized. One high-pitched beep announces the start of the recovery process. The entire process takes two to four minutes. A successful update ends with two high-pitched beeps. Failure is indicated by a long series of short beeps.

If a failure occurs, it is most likely that one or more of the system BIOS iFlash files is corrupt or missing.

After a successful update, power down the system and move the recovery jumper back to pins 1 and 2. Power up the system. Verify that the BIOS version number matches the version of the entire BIOS used in the original attempt to update.

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9. Server Management

9.1 Overview

The SKA4 server management features are implemented using a Dallas* 80CH11 controller. The following diagram illustrates the SKA4 server management architecture. A description of the hardware architecture follows.

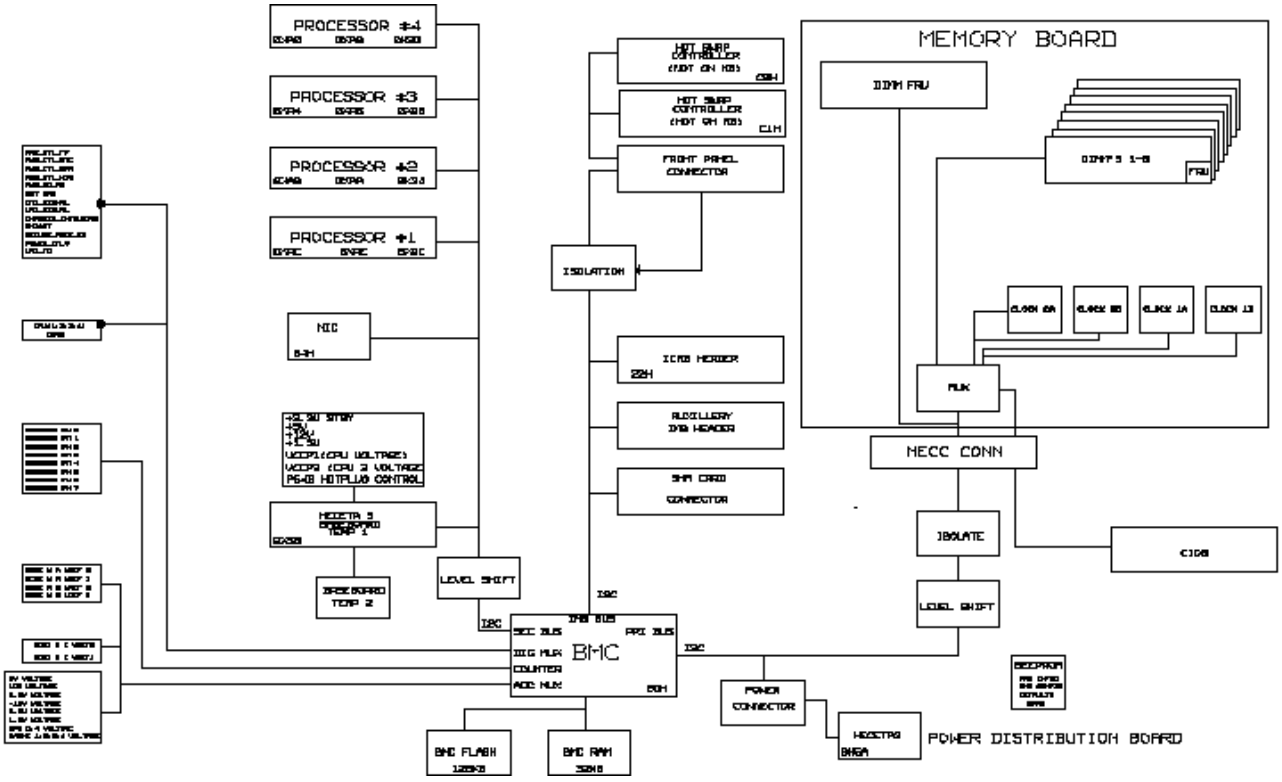


Figure 9-1: SKA4 Server Management Block Diagram

9.2 Baseboard Management Controller

The BMC is an 8051-compatible microcontroller used to monitor the system for critical events. The BMC monitors all power supplies, including those generated by the external power supplies and those regulated locally on the baseboard. The BMC also monitors SCSI termination voltages, fan tachometers for detecting a fan failure, and system temperature. Temperature is measured on each of the processors and at two locations on the baseboard farthest from the fans. When any monitored parameter is outside defined thresholds, the BMC logs an event in its system event log.

The BMC uses three types of memory: flash, SRAM, and serial EEPROM (SEEPROM). The flash and SRAM reside on the BMC external data bus, while the SEEPROM resides on the primary private I^2C* bus. The BMC supports 64 KB of addressable space only on the external data bus, so two GPIO bits were defined to allow more memory space to be used. The memory

address space is selected using the MEM_MODE<0.1> bits to swap between two 64-KB data segments of the flash, and/or swap the flash and SRAM between code and data spaces:

- Memory mode bit 0 selects whether the flash and SRAM are in code or data space. When bit M0 is logic 1, the flash is in the code space and the SRAM in the data space. Toggling bit M0 will swap the flash and SRAM between the two memory spaces.
- Memory mode bit 1 selects whether the upper or lower half of the 128-KB flash is being used.

The following table contains the memory map for the two devices on this bus (M0 and M1 are the memory mode bits).

Table 9-1: BMC Memory Map

128K Flash			32K SRAM	
Address	**Block**	**Memory Mode**	**Address**	**Block**
0x1FFFF 0x18000	BMC Operational Code	0	0x1FFFF 0x18000	Unused
0x17FFF 0x10000	BMC Operational Code	0	0x17FFF 0x10000	Mirrored SRAM blocks from below
0x0FFFF 0x0A000	System Event Log	1	0x0FFFF 0x08000	Unused
0x09FFF 0x04000	Sensor Data Record / Parameter Access Code	1	0x07FFF 0x02000	XBUS Variables, Parameter Access Code
0x03FFF 0x00000	Boot Block	1	0x01FFF 0x00000	Boot Loader, Flash Update, Mode Switching

An ADM1024* has been attached to the secondary I^2C bus for monitoring the two system temperatures (one internal and one external to the part) and additional analog voltages. The table below describes these added signals. The ADM1024 device also provides a digital-to-analog converter for use in fan speed control. The output is 0-2.5 V and is connected to the power subsystem for proper conversion of the fan voltage rails.

Table 9-2: BMC ADM1024 Input Definition

ADM1024* Pin	Type	Attached Signal
9	Analog Input	+3.3 V standby
16	Analog Input	+5 V
15	Analog Input	+12 V
6	Analog Input	+1.5 V
19	Analog Input	VCC Processor 1
5	Analog Input	VCC Processor 2
11	Analog Output	Fan speed control
17	Analog Input	Unused
18	Analog Input	Unused
13,14	Temperature In	Baseboard Temperature 2

ADM1024* Pin	Type	Attached Signal
20	Digital Input	PCI hot-plug power state 0
21	Digital Input	PCI hot-plug power state 1
22	Digital Input	PCI hot-plug power state 2
23	Digital Input	PCI hot-plug power state 3
24	Digital Input	PCI hot-plug power state 4
7	Digital Input	Chassis Intrusion

9.2.1 Fault Resilient Booting

The BMC implements Fault Resilient Booting (FRB) levels 1, 2, and 3. If the default bootstrap processor (BSP) fails to complete the boot process, FRB attempts to boot using an alternate processor.

- FRB level 1 is for recovery from a BIST failure detected during POST. This FRB recovery is fully handled by BIOS code.
- FRB level 2 is for recovery from a watchdog timeout during POST. The watchdog timer for FRB level 2 detection is implemented in the BMC.
- FRB level 3 is for recovery from a watchdog timeout on Hard Reset/Power-up. Hardware functionality for this level of FRB is provided by the BMC.

9.2.1.1 FRB-1

In a multiprocessor system, the BIOS registers the application processors in the MP table and the ACPI APIC tables. When started by the BSP, if an AP fails to complete initialization within a certain time, it is assumed to be nonfunctional. If the BIOS detects that an application processor has failed BIST or is nonfunctional, it requests the BMC to disable that processor. The BMC then generates a system reset while disabling the processor; the BIOS will not see the bad processor in the next boot cycle. The failing AP is not listed in the MP table (refer to the *Multi-Processor Specification, Rev. 1.4*), nor in the ACPI APIC tables, and is invisible to the OS. If the BIOS detects that the BSP has failed BIST, it sends a request to BMC to disable the present processor. If there is no alternate processor available, the BMC beeps the speaker and halts the system. If BMC can find another processor, it transfers BSP ownership to that processor via a system reset.

9.2.1.2 FRB-2

The second watchdog timer (FRB-2) in the BMC is set for approximately 6 minutes by BIOS and is designed to guarantee that the system completes BIOS POST. The FRB-2 timer is enabled before the FRB-3 timer is disabled to prevent any “unprotected” window of time. Near the end of POST, before the option ROMs are initialized, the BIOS disables the FRB-2 timer in the BMC. If the system contains more than 1 GB of memory and the user chooses to test every DWORD of memory, the watchdog timer is disabled before the extended memory test starts, because the memory test can take more than 6 minutes under this configuration. If the system hangs during POST, the BIOS does not disable the timer in the BMC, which generates an asynchronous system reset. For more details, refer to the *Baseboard Management Controller Interface Specification.*

9.2.1.3 FRB-3

The first timer (FRB-3) starts counting down whenever the system comes out of hard reset, which is usually about 5 seconds. If the BSP successfully resets and starts executing, the BIOS disables the FRB-3 timer in the BMC by de-asserting the FRB_TIMER_HLT* signal (GPIO) and the system continues on with the POST. If the timer expires because of the BSP's failure to fetch or execute BIOS code, the BMC resets the system and disables the failed processor. The system continues to change the bootstrap processor until the BIOS POST gets past disabling the FRB-3 timer in the BMC. The BMC sounds beep codes on the speaker, if it fails to find a good processor. The process of cycling through all the processors is repeated upon system reset or power cycle.

9.3 System Reset Control

Reset circuitry on the SKA4 baseboard looks at resets from the front panel, OSB4, ITP, and processor subsystem to determine proper reset sequencing for all types of reset. The reset logic is designed to accommodate a variety of ways to reset the system, which can be divided into the following categories:

- Power-up reset.
- Hard reset.
- Soft (programmed) reset.

The following subsections describe each category of reset.

9.3.1 Power-up Reset

When the system is disconnected from AC power, all logic on the baseboard is powered off. When a valid input (AC) voltage level is provided to the power supply, 5-volt standby power will be applied to the baseboard. A power monitor circuit on 5-volt standby will assert **RST_BMC,** causing the BMC to reset. The BMC is powered by 5-volt standby and monitors and controls key events in the system related to reset and power control.

After the system is turned on, the power supply will assert the **PWR_GD_PS** signal after all voltage levels in the system have reached valid levels. The BMC receives **PWR_GD_PS** and after 500 ms asserts **P6_PWR_GOOD,** which indicates to the processors and OSB4 that the power is stable. Upon **P6_PWR_GOOD** assertion, the OSB4 will toggle PCI reset.

P6_PWR_GOOD is also used for isolation control of the Intelligent Platform Management Bus (IPMB) via the front panel. For more details, see Section 9.4.

9.3.2 Hard Reset

Hard reset can be initiated by software, by the user resetting the system through the front panel switch, or through the Server Management Module (SMM). For Front Panel or SMM resets, the BMC de-asserts **P6_PWR_GOOD**. After 600 ms, it is reasserted, and the Power-up Reset sequence is done.

The BMC is not reset by a hard reset. It may be reset at power-up.

9.3.3 Soft Reset

Soft reset causes the processors to begin execution in a known state without flushing caches or internal buffers. Soft resets can be generated by the keyboard controller located in the SIO or by the OSB4. The output of the SIO (**RST_KB_L**) is input to the OSB4.

9.4 Intelligent Platform Management Buses

Management controllers (and sensors) communicate on the I^2C-based Intelligent Platform Management Bus. A bit protocol defined by the *I^2C Bus Specification*, and a byte-level protocol defined by the *Intelligent Platform Management Bus Communications Protocol Specification*, provide an independent interconnect for all devices operating on this I^2C bus. The IPMB extends throughout the baseboard and system chassis. An added layer in the protocol supports transactions between multiple servers on inter-chassis I^2C bus segments.

The IPMB connects to various devices external to the baseboard. The IPMB connectors outside of the baseboard (Auxiliary IPMB, SMM card, and ICMB) cannot load the bus without power, because this would prevent bus communication. For devices attached via the front panel connector, an isolation circuit was added that disconnects the bus from the BMC when power good is inactive. The table below lists all baseboard connections to the IPMB.

Table 9-3: IPMB Bus Devices

IPMB I^2C* Addresses				
Function	**Voltage**	**Supply**	**Address**	**Notes**
ICMB	5	standby	0x28	
BMC controller	5	standby	0x20	
SMM card connector	5	standby	not assigned	
Auxiliary IPMB connector	5	standby	not assigned	
SCSI hot swap controller	5	standby	TBD	
FDB FRU SEEPROM	5	standby	0xAA	AT24C02
FDB Fan Fail Indicator	5	standby	0x4E	PCF8574
FDB Fan Fail Indicator	5	standby	0x46	PCF8574
FDB Temp Sense	5	standby	0x9A	DS1621

Besides the “public” IPMB, the BMC also has two private I^2C buses. The BMC is the only master on the private bus. The table below lists all baseboard connections to the BMC private I^2C buses.

Table 9-4: BMC Primary Private I^2C* Bus Devices

Primary Private Bus				
Function	**Voltage**	**Supply**	**Address**	**Notes**
Power Distribution Board (PDB) - Heceta 3	5	standby	0x5A	Connects to SSI HS Power Supplies
PDB FRU SEEPROM	5	standard	0xA6	AT24C02
PS 1 FRU SEEPROM	5	standard	0xA0	AT24C02
PS 2 FRU SEEPROM	5	standard	0xA2	AT24C02

Primary Private Bus				
Function	**Voltage**	**Supply**	**Address**	**Notes**
PS 3 FRU SEEPROM	5	standard	0xA4	AT24C02
BMC SEEPROM	5	standby	0xAE	AT24C08
Memory Board FRU SEEPROM	3.3	standard	0xAC	AT24C02
CPU Speed Mux (Write)	3.3	standard	0x9C	PCF8550
CPU Speed Mux (Read)	3.3	standard	0x9D	PCF8550

Table 9-5: BMC Secondary Private I^2C* Bus Devices

Secondary Private Bus				
Function	**Voltage**	**Supply**	**Address**	**Notes**
Baseboard Heceta 3	3.3	standby	0x58	Placed near the PCI slots; monitors two baseboard temps, five analog voltages, and chassis intrusion.
CPU1 SEEPROM	3.3	standby	0xA0	VID information and OEM access.
CPU1 RO SEEPROM	3.3	standby	0xA2	
CPU1 temp	3.3	standby	0x30	Core temperature reading.
CPU2 SEEPROM	3.3	standby	0xA4	
CPU2 RO SEEPROM	3.3	standby	0xA6	
CPU2 temp	3.3	standby	0x98	
CPU3 SEEPROM	3.3	standby	0xA8	
CPU3 RO SEEPROM	3.3	standby	0xAA	
CPU3 temp	3.3	standby	0x34	
CPU4 SEEPROM	3.3	standby	0xAC	
CPU4 RO SEEPROM	3.3	standby	0xAE	
CPU4 temp	3.3	standby	0x9C	

10. Jumpers

10.1 Hardware Configuration (J9F2, J9F1, J9G1)

This section describes jumper options on the baseboard.

Two 11-pin, and one 3-pin single inline headers provide a total of eight 3-pin jumper blocks that control various configuration options, as shown in the figure below. The shaded areas show default jumper placement for each configurable option.

Note that J9F1 will not be stuffed for production. The functions on these jumpers are intended to be used during evaluation only and will not be populated during production.

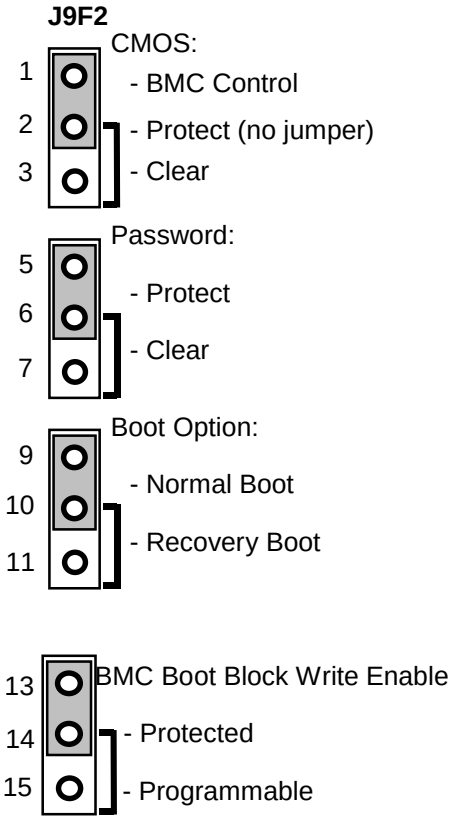


Figure 10-1: SKA4 Configuration Jumpers

The following table describes each jumper option.

Table 10-1: Configuration Jumper Options

Option	Description
CMOS	If pins 1 and 2 of J9F2 are jumpered (default), NVRAM contents are preserved through system reset unless the user clears them through the front panel (by pressing the Power and Reset buttons together for four seconds). If pins 2 and 3 of J9F2 are jumpered, NVRAM contents are set to manufacturing default during system reset. If the jumper is removed, NVRAM contents are preserved through system reset.
Password	If pins 5 and 6 of J9F2 are jumpered (default), the current system password is maintained during system reset. If pins 6 and 7 of J9F2 are jumpered, the password is cleared on reset.
Boot Option	If pins 9 and 10 of J9F2 are jumpered (default), BIOS will jump to a protected area of the flash part containing the "Recovery BIOS." If the normal BIOS gets corrupted, and you are unable to reload a fresh copy from the floppy disk, install the jumper between pins 10 and 11 of J9F2, which enables the system to boot from the Recovery BIOS. This code expects a fresh copy of the normal BIOS to be located on a floppy disk present in the floppy drive.
FRB Timer	If pins 1 and 2 of J9F1 are jumpered (default) FRB operation is enabled, which allows the system to boot from another processor if processor 1 fails. If pins 2 and 3 of J9F1 are jumpered, FRB is disabled. This header will not be stuffed in production, meaning the default cannot be overridden.
Chassis Intrusion Detection	If pins 5 and 6 of J9F1 are jumpered (default), a switch installed on the chassis will indicate when the cover has been removed. If pins 6 and 7 of J9F1 are jumpered, the chassis intrusion switch is bypassed. This header will not be stuffed in production, meaning the default cannot be overridden.
BMC FRC Update Mode	If pins 9 and 10 of J9F1 are jumpered (default), then BMC will go to operational mode upon the deassertion of its reset. If pins 10 and 11 of J9F1 are jumpered, then BMC will go to force update mode upon the deassertion of its reset. This header will not be stuffed in production, meaning the default cannot be overridden.
BMC Boot Block Write Enable	This jumper provides protection for the BMC flash boot block. If enabled, the jumper will allow writes to the BMC Flash boot block.

11. Connections

11.1 Connector Locations

The diagram below identifies all the connector locations.

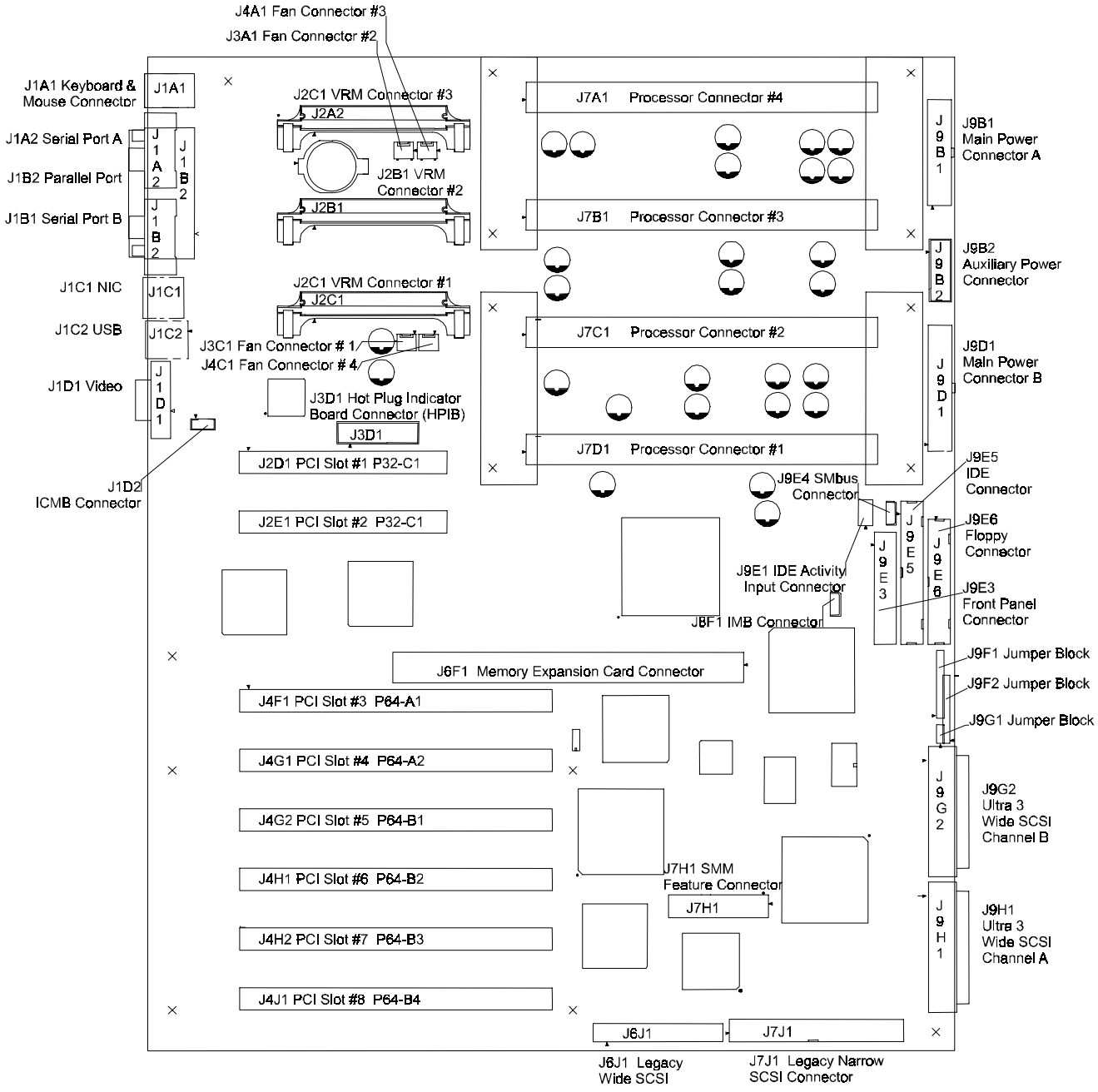


Figure 11-1: SKA4 Baseboard Connector Identification and Locations

11.2 Power Distribution Board Interface Connectors (J9B1, J9D1, J9B2)

The SKA4 baseboard and memory module receive their main power through two primary power connectors and one auxiliary power connector. The two main power connectors are identified as J9B1 and J9D1. The auxiliary power connector, identified as J9B2, provides a power subsystem communication path, control signals, power supply sense connections and other miscellaneous signals defined below.

Table 11-1: Main Power Connector A (J9B1)

Pin	Signal	Type †	Current Carrying Capability	Description
1	12V	power	6 Amps	Power supply 12V
2	Ground	ground	6 Amps	Ground return connection
3	Ground	ground	6 Amps	Ground return connection
4	Ground	ground	6 Amps	Ground return connection
5	Ground	ground	6 Amps	Ground return connection
6	VCC	power	6 Amps	Power supply 5V
7	VCC	power	6 Amps	Power supply 5V
8	VCC	power	6 Amps	Power supply 5V
9	VCC	power	6 Amps	Power supply 5V
10	VCC	power	6 Amps	Power supply 5V
11	SB5V	power	6 Amps	Power supply 5V standby
12	Ground	ground	6 Amps	Ground return connection
13	Ground	ground	6 Amps	Ground return connection
14	Ground	ground	6 Amps	Ground return connection
15	Ground	ground	6 Amps	Ground return connection
16	VCC	power	6 Amps	Power supply 5V
17	VCC	power	6 Amps	Power supply 5V
18	VCC	power	6 Amps	Power supply 5V
19	VCC	power	6 Amps	Power supply 5V
20	VCC	power	6 Amps	Power supply 5V

Notes:
† Type (in, out, in/out, power, ground) is from the perspective of the baseboard.

Table 11-2: Main Power Connector B (J9D1)

Pin	Signal	Type †	Current Carrying Capability	Description
1	VCC3	power	6 Amps	Power supply 3.3V
2	VCC3	power	6 Amps	Power supply 3.3V
3	VCC3	power	6 Amps	Power supply 3.3V
4	VCC3	power	6 Amps	Power supply 3.3V
5	VCC3	power	6 Amps	Power supply 3.3V
6	VCC3	power	6 Amps	Power supply 3.3V
7	Ground	ground	6 Amps	Ground return connection

Pin	Signal	Type †	Current Carrying Capability	Description
8	Ground	ground	6 Amps	Ground return connection
9	Ground	ground	6 Amps	Ground return connection
10	Ground	ground	6 Amps	Ground return connection
11	Ground	ground	6 Amps	Ground return connection
12	12V	power	6 Amps	Power supply 12V
13	VCC3	power	6 Amps	Power supply 3.3V
14	VCC3	power	6 Amps	Power supply 3.3V
15	VCC3	power	6 Amps	Power supply 3.3V
16	VCC3	power	6 Amps	Power supply 3.3V
17	VCC3	power	6 Amps	Power supply 3.3V
18	VCC3	power	6 Amps	Power supply 3.3V
19	Ground	ground	6 Amps	Ground return connection
20	Ground	ground	6 Amps	Ground return connection
21	Ground	ground	6 Amps	Ground return connection
22	Ground	ground	6 Amps	Ground return connection
23	Ground	ground	6 Amps	Ground return connection
24	12V	power	6 Amps	Power supply 12V

Notes:
† Type (in, out, in/out, power, ground) is from the perspective of the baseboard.

Table 11-3: Auxiliary Power Connector (J9B2)

Pin	Signal	Type †	Current Carrying Capability	Description
1	Ground	ground		Ground return connection
2	5V Sense	out	N/A	Sense line feedback to power supply
3	3.3V Sense	out	N/A	Sense line feedback to power supply
4	BMC FAN SPD CTL	out	N/A	
5	SM PRI 5VSB SCL	In/out	N/A	Server Management I2C bus - clock
6	SM PRI 5VSB SDA	In/out	N/A	Server Management I2C bus - data
7	Ground	ground		Ground return connection
8	PWRGD PS	In	N/A	Signal from power subsystem indicating power is stable
9	PS PWR ON_L	Out	N/A	Control signal from baseboard to power supply
10	Ground	ground		Ground return connection
11	-12V	power		Power supply negative 12V
12	Key		N/A	
13	12V	power		Power supply 12V
14	Ground	ground		Ground return connection

Notes:
† Type (in, out, in/out, power, ground) is from the perspective of the baseboard.

11.3 Front Panel Interface (J9E3)

A 30-pin header is provided that attaches to the system front panel. The header contains reset, NMI, sleep, and power control buttons, LED indicators, and an IPMB connection. The table below summarizes the front panel signal pins, including the signal mnemonic, name, and brief description.

Table 11-4: Front Panel Connector (J9E3)

Pin	Signal	Type †	Description
1	SPKR_FP	out	SPEAKER DATA for the front panel/chassis mounted speaker.
2	GROUND	ground	GROUND is the power supply ground.
3	CHASSIS_INTRUSION	in	CHASSIS INTRUSION is connected to the BMC and indicates that the chassis has been opened. CHASSIS_INTRUSION is pulled high to +5 V standby on the baseboard.
4	FP_HD_ACT*	out	HARD DRIVE ACTIVITY indicates there is activity on one of the hard disk controllers in the system.
5	+5V	power	+5 V is the 5 volt power supply.
6	FP_SLP_BTN*	in	FRONT PANEL SLEEP is connected to the BMC and causes the system to be put to sleep if supported by the operating system. FP_SLP_BTN* is pulled high to +5 V on the baseboard and is intended to be connected to a momentary-contact push button (connected to GROUND when pushed) on the system front.
7	COOL_FLT_LED*	out	COOLING FAULT LED indicates that either a fan failure has occurred or the system is approaching an over-temperature situation. COOL_FLT_LED* is an output of the BMC.
8	PWR_LED*	out	POWER PRESENT LED.
9	PWR_FLT_LED*	out	SYSTEM FAULT indicates that either a power fault or SCSI drive failure has occurred in the system.
10	GROUND	ground	GROUND is the power supply ground.
11	SM_IMB_SDA	in/out	I^2C DATA is the data signal for the Intelligent Platform Management Bus.
12	FP_NMI_BTN*	in	FRONT PANEL NMI is connected to a BMC input port, allowing the front panel to generate an NMI. FP_NMI_BTN* is pulled high to +5 V on the baseboard and is intended to be connected to a momentary-contact push button (connected to GROUND when pushed) on the system front panel.
13	SM_IMB_SCL	in/out	I^2C CLOCK is the clock signal for the Intelligent Platform Management Bus.
14	FP_RST_BTN*	in	FRONT PANEL RESET is connected to the BMC and causes a hard reset to occur, resetting all baseboard devices except for the BMC and BMC. FP_RST_BTN* is pulled high to +5V on the baseboard, and is intended to be connected to a momentary-contact push button (connected to GROUND when pushed) on the system front panel.
15	+5V standby	power	+5 V STANDBY is the standby 5 volt power supply.
16	FP_PWR_BTN*	in	FRONT PANEL POWER CONTROL is connected to the BMC and causes the power to toggle (on → off, or off → on). FP_PWR_BTN* is pulled high to +5 V standby on the baseboard and is intended to be connected to a momentary-contact push button (connected to GROUND when pushed) on the system front panel.
17	SM_FP_ISOL	in	SM_FP_ISOL, when asserted, isolates the front panel SM bus.
18	GROUND	ground	GROUND is the power supply ground.
19	FAN_TACH(0)	in	FAN_TACH signal is connected to the BMC to monitor the FAN speed.
20	FAN_TACH(1)	in	FAN_TACH signal is connected to the BMC to monitor the FAN speed.

Pin	Signal	Type †	Description
21	FAN_TACH(2)	in	FAN_TACH signal is connected to the BMC to monitor the FAN speed.
22	FAN_TACH(3)	in	FAN_TACH signal is connected to the BMC to monitor the FAN speed.
23	FAN_TACH(4)	in	FAN_TACH signal is connected to the BMC to monitor the FAN speed.
24	FAN_TACH(5)	in	FAN_TACH signal is connected to the BMC to monitor the FAN speed.
25	FAN_TACH(6)	in	FAN_TACH signal is connected to the BMC to monitor the FAN speed.
26	FAN_TACH(7)	in	FAN_TACH signal is connected to the BMC to monitor the FAN speed.
27	RJ45_ACTLED_R	in	NIC activity LED.
28	reserved	-	Reserved.
29	SM_PRI_SCL	in/out	I^2C CLOCK is the clock signal for the Primary Private Bus.
30	SM_PRI_SDA	in/out	I^2C DATA is the data signal for the Primary Private Bus.

Notes:
† Type (in, out, in/out, power, ground) is from the perspective of the baseboard.

11.4 Hot-plug PCI Indicator Board Interface (J3D1)

The Hot-plug PCI Indicator Board (HPIB) contains the necessary LEDs and push button switches to help the user run PCI hot-plug operations.

Each PHP slot contains a green LED and amber LED to indicate slot status. The actual interpretation of the LEDs depends on the operating system running on the system.

Each PHP slot also has a momentary push button switch used to notify the operating system that a PHP operation on the respective slot is requested. If PHP operation is supported by the operating system, the user momentarily presses the switch and then waits for the operating system to signal via the LEDs that the PHP slot has been disabled. The user can then perform the desired PHP operation on the slot, such as replacing, removing, or adding a PCI adapter. When the user wants the operating system to enable and initialize the PHP slot, the user momentarily presses the switch again.

This (Active Low) push button switch for the respective slot is routed to the PRSNT1# input to the PCI hot-plug controller. This switch should not be confused with slot-interlock switches, which are used in conjunction with mechanical lever designs to prevent access to an energized PHP slot. The slot interlock inputs into the PHPC are permanently pulled down to ground and are not accessible through the hot-plug PCI indicator board interface.

The hot-plug PCI indicator board interface contains the necessary signals to drive the LEDs and receive the push button signals.

A 20-pin connector is provided on the baseboard for connection to the external HPIB. The pinout for this connector is as follows:

Table 11-5: Hot-plug Indicator Board Connector Pinout (J3D1)

Connector Contact	Signal Name	Connector Contact	Signal Name
1	Vcc	2	GROUND
3	P64_A_SWITCH<0>	4	P64_A_GRN_LED<1>
5	P64_A_AMB_LED<0>	6	P64_A_SWITCH<1>

Connector Contact	Signal Name	Connector Contact	Signal Name
7	P64_A_GRN_LED<1>	8	P64_A_AMB_LED<1>
9	P64_B_SWITCH<0>	10	P64_A_GRN_LED<0>
11	P64_B_AMB_LED<0>	12	P64_B_SWITCH<1>
13	P64_B_GRN_LED<1>	14	P64_A_AMB_LED<1>
15	P64_B_SWITCH<2>	16	P64_A_GRN_LED<2>
17	P64_A_AMB_LED<2>	18	P64_B_SWITCH<3>
19	P64_A_GRN_LED<3>	20	P64_A_AMB_LED<3>

11.5 Memory Module Interface (J6F1)

Table 11-6: Memory Board Connector Pinout (J6F1)

Pin †	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A001	GND	B001	PIN_B1	A084	GND	B084	MAA9
A002	GND	B002	VCC3	A085	MAA10	B085	VCC3
A003	GND	B003	SYNTH_OUT_MADP CLK	A086	MAA11	B086	MAA12
A004	GND	B004	VCC3	A087	GND	B087	MAA13
A005	ASCLK	B005	VCC3	A088	MAA14	B088	VCC3
A006	CMD0	B006	ASDATA	A089	MCD_MUXSEL	B089	VCC3
A007	GND	B007	CMD16	A090	GND	B090	VCC3
A008	CMD1	B008	VCC3	A091	BSCLK	B091	VCC3
A009	CMD2	B009	CMD3	A092	MECC12	B092	BSDATA
A010	GND	B010	CMD19	A093	GND	B093	MECC14
A011	CMD17	B011	VCC3	A094	MECC13	B094	VCC3
A012	CMD4	B012	CMD20	A095	MECC15	B095	CMD97
A013	GND	B013	CMD6	A096	GND	B096	CMD96
A014	CMD18	B014	VCC3	A097	CMD112	B097	VCC3
A015	CMD5	B015	CMD21	A098	CMD113	B098	CMD98
A016	GND	B016	CMD23	A099	GND	B099	CMD99
A017	CMD8	B017	VCC3	A100	CMD114	B100	VCC3
A018	CMD7	B018	CMD22	A101	CMD100	B101	CMD116
A019	GND	B019	CMD9	A102	GND	B102	CMD115
A020	CMD25	B020	VCC3	A103	CMD101	B103	VCC3
A021	CMD26	B021	CMD24	A104	CMD117	B104	CMD102
A022	GND	B022	CMD10	A105	GND	B105	CMD103
A023	CMD12	B023	VCC3	A106	CMD118	B106	VCC3
A024	CMD28	B024	CMD11	A107	CMD119	B107	CMD104
A025	GND	B025	CMD27	A108	GND	B108	CMD120
A026	CMD29	B026	VCC3	A109	CMD105	B109	VCC3
A027	CMD14	B027	CMD30	A110	CMD121	B110	CMD106
A028	GND	B028	CMD13	A111	GND	B111	CMD107
A029	CMD15	B029	VCC3	A112	CMD122	B112	VCC3
A030	CMD31	B030	MECC0	A113	CMD123	B113	CMD108
A031	GND	B031	MECC1	A114	GND	B114	CMD124
A032	MECC2	B032	VCC3	A115	CMD109	B115	VCC3
A033	MECC3	B033	CKE_0	A116	CMD125	B116	CMD110
A034	GND	B034	0_RAS	A117	GND	B117	CMD126

Pin †	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A035	0_WE*	B035	VCC3	A118	GND	B118	VCC3
A036	0_CAS	B036	0_CS0	A119	GND	B119	VCC3
A037	GND	B037	0_CS1	A120	CMD111	B120	VCC3
A038	0_CS2	B038	VCC3	A121	CMD127	B121	CKE_1
A039	0_CS3	B039	0_MCDOE*	A122	GND	B122	1_RAS
A040	GND	B040	MEMPRSNT	A123	1_WE*	B123	VCC3
A041	0_MCDSEL*	B041	VCC3	A124	1_CAS	B124	1_CS0
A042	GND	B042	TMD0	A125	GND	B125	1_CS1
A043	GND	B043	VCC3	A126	1_CS2	B126	VCC3
A044	CMD34	B044	VCC3	A127	1_CS3	B127	1_MCDOE*
A045	CMD50	B045	CMD49	A128	GND	B128	1_MCDSEL*
A046	GND	B046	CMD54	A129	CMD80	B129	VCC3
A047	CMD52	B047	VCC3	A130	MECC8	B130	MECC10
A048	CMD51	B048	CMD33	A131	GND	B131	CMD64
A049	GND	B049	CMD32	A132	CMD81	B132	VCC3
A050	CMD40	B050	VCC3	A133	MECC9	B133	MECC11
A051	CMD38	B051	CMD53	A134	GND	B134	CMD65
A052	GND	B052	CMD36	A135	CMD66	B135	VCC3
A053	CMD35	B053	VCC3	A136	CMD82	B136	CMD85
A054	CMD42	B054	CMD58	A137	GND	B137	CMD67
A055	GND	B055	CMD39	A138	CMD83	B138	VCC3
A056	GND	B056	VCC3	A139	CMD84	B139	CMD68
A057	GND	B057	VCC3	A140	GND	B140	CMD71
A058	CMD55	B058	VCC3	A141	CMD87	B141	VCC3
A059	CMD37	B059	CMD43	A142	CMD70	B142	CMD86
A060	GND	B060	CMD57	A143	GND	B143	CMD69
A061	CMD56	B061	VCC3	A144	CMD73	B144	VCC3
A062	CMD62	B062	CMD63	A145	CMD89	B145	CMD72
A063	GND	B063	CMD61	A146	GND	B146	CMD88
A064	CMD44	B064	VCC3	A147	CMD76	B147	VCC3
A065	CMD60	B065	CMD41	A148	CMD92	B148	CMD75
A066	GND	B066	MECC6	A149	GND	B149	CMD91
A067	CMD47	B067	VCC3	A150	CMD74	B150	VCC3
A068	CMD48	B068	CMD59	A151	CMD90	B151	CMD78
A069	GND	B069	CMD45	A152	GND	B152	CMD77
A070	CMD46	B070	VCC3	A153	CMD94	B153	VCC3
A071	MECC7	B071	MECC4	A154	CMD93	B154	CMD79
A072	GND	B072	MECC5	A155	GND	B155	CMD95
A073	GND	B073	VCC3	A156	GND	B156	VCC3
A074	MADPCLK_FB_DLY	B074	VCC3	A157	GND	B157	VCC3
A075	GND	B075	BCLK_MADP_OUT	A158	GND	B158	VCC3
A076	MAA0	B076	VCC3	A159	GND	B159	VCC3
A077	MAA1	B077	VCC3	A160	GND	B160	VCC3
A078	GND	B078	SDRDCLK_HE_DLY	A161	GND	B161	VCC3
A079	MAA2	B079	VCC3	A162	GND	B162	RESERVED162
A080	MAA3	B080	MAA4	A163	GND	B163	VCC
A081	GND	B081	MAA5	A164	GND	B164	VCC

Pin †	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A082	MAA6	B082	VCC3	A165	PIN_A165	B165	VCC
A083	MAA7	B083	MAA8	A166	NC	B166	NC

11.6 Processor Module Support

11.6.1 Processor Module Connector (J7A1, J7B1, J7C1, J7D1)

Table 11-7: Processor Card Connector Pinout (J7A1, J7B1, J7C1, J7D1)

Pin †	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A001	RESERVED (nc)	B001	PWR_EN1	A084	GND	B084	RESERVED (nc)
A002	VCC_TAP	B002	VCCP	A085	D11*	B085	VCCP
A003	RESERVED (nc)	B003	OCVR_OK*	A086	D10*	B086	D17*
A004	GND	B004	TEST_VSS_B4	A087	GND	B087	D15*
A005	VTT	B005	VCCP	A088	D14*	B088	VCCP
A006	VTT	B006	VTT	A089	D9*	B089	D12*
A007	SELFSB1	B007	VTT	A090	GND	B090	D7*
A008	RESERVED_A8	B008	VCCP	A091	D8*	B091	VCCP
A009	RESERVED_A9	B009	RESERVED (nc)	A092	D5*	B092	D6*
A010	GND	B010	FLUSH*	A093	GND	B093	D4*
A011	TEST_GND (pd)	B011	VCCP	A094	D3*	B094	VCCP
A012	IERR*	B012	SMI*	A095	D1*	B095	D2*
A013	GND	B013	INIT*	A096	GND	B096	D0*
A014	A20M*	B014	VCCP	A097	BCLK	B097	VCCP
A015	FERR*	B015	STPCLK*	A098	TEST_VSS (pd)	B098	RESET*
A016	GND	B016	TCK	A099	GND	B099	FRCERR
A017	IGNNE*	B017	VCCP	A100	BERR*	B100	VCCP
A018	TDI	B018	SLP*	A101	A33*	B101	A35*
A019	GND	B019	TMS	A102	GND	B102	A32*
A020	TDO	B020	VCCP	A103	A34*	B103	VCCP
A021	PWRGOOD	B021	TRST*	A104	A30*	B104	A29*
A022	GND	B022	RESERVED (nc)	A105	GND	B105	A26*
A023	TEST_25 (pu)††	B023	VCCP	A106	A31*	B106	VCCL2
A024	THERMTRIP*	B024	RESERVED (nc)	A107	A27*	B107	A24*
A025	GND	B025	RESERVED (nc)	A108	GND	B108	A28*
A026	OCRV_EN	B026	VCCP	A109	A22*	B109	VCCL2
A027	INTR	B027	TEST_VCCP (pu)	A110	A23*	B110	A20*
A028	GND	B028	NMI	A111	GND	B111	A21*
A029	PICD0	B029	VCCP	A112	A19*	B112	VCCL2
A030	PREQ*	B030	PICCLK	A113	A18*	B113	A25*
A031	GND	B031	PICD1	A114	GND	B114	A15*
A032	BP3*	B032	VCCP	A115	A16*	B115	VCC_L2
A033	BMP0*	B033	BP2*	A116	A13*	B116	A17*
A034	GND	B034	RESERVED (nc)	A117	GND	B117	A11*
A035	BINIT*	B035	VCCP	A118	A14*	B118	VCC_L2
A036	DEP0*	B036	PRDY*	A119	GND	B119	A12*
A037	VSS	B037	BPM1*	A120	A10*	B120	VCCL2
A038	DEP1*	B038	VCCP	A121	A5*	B121	A8*
A039	DEP3*	B039	DEP2*	A122	GND	B122	A7*

Pin †	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A040	GND	B040	DEP4*	A123	A9*	B123	VCCL2
A041	DEP5*	B041	VCCP	A124	A4*	B124	A3*
A042	DEP6*	B042	DEP7*	A125	GND	B125	A6*
A043	GND	B043	D62*	A126	RESERVED (nc)	B126	VCCL2
A044	D61*	B044	VCCP	A127	BNR*	B127	AERR*
A045	D55*	B045	D58*	A128	GND	B128	REQ0*
A046	GND	B046	D63*	A129	BPRI*	B129	VCCL2
A047	D60*	B047	VCCP	A130	TRDY*	B130	REQ1*
A048	D53*	B048	D56*	A131	GND	B131	REQ4*
A049	GND	B049	D50*	A132	DEFER*	B132	VCCL2
A050	D57*	B050	VCCP	A133	REQ2*	B133	LOCK*
A051	D46*	B051	D54*	A134	GND	B134	DRDY*
A052	GND	B052	D59*	A135	REQ3*	B135	VCCL2
A053	D49*	B053	VCCP	A136	HITM*	B136	RS0*
A054	D51*	B054	D48*	A137	GND	B137	HIT*
A055	GND	B055	D52*	A138	DBSY*	B138	VCCL2
A056	CPU_SENSE	B056	VCCP	A139	RS1*	B139	RS2*
A057	GND	B057	L2_SENSE	A140	GND	B140	RP*
A058	D42*	B058	VCCP	A141	BR2*	B141	VCCL2
A059	D45*	B059	D41*	A142	BR0*	B142	BR3*
A060	GND	B060	D47*	A143	GND	B143	BR1*
A061	D39*	B061	VCCP	A144	ADS*	B144	VCCL2
A062	TEST_25 (pu)††	B062	D44*	A145	AP0*	B145	RSP*
A063	GND	B063	D36*	A146	GND	B146	AP1*
A064	D43*	B064	VCCP	A147	VID2_CORE	B147	VCCL2
A065	D37*	B065	D40*	A148	VID1_CORE	B148	RESERVED (nc)
A066	GND	B066	D34*	A149	GND	B149	VID3_CORE
A067	D33*	B067	VCCP	A150	VID4_CORE	B150	VCCL2
A068	D35*	B068	D38*	A151	RESERVED (nc)	B151	VID0_CORE
A069	GND	B069	D32*	A152	GND	B152	VID0_L2
A070	D31*	B070	VCCP	A153	VID2_L2	B153	VCCL2
A071	D30*	B071	D28*	A154	VID1_L2	B154	VID4_L2
A072	GND	B072	D29*	A155	GND	B155	VID3_L2
A073	D27*	B073	VCCP	A156	VTT	B156	VCCL2
A074	D24*	B074	D26*	A157	VTT	B157	VTT
A075	GND	B075	D25*	A158	GND	B158	VTT
A076	D23*	B076	VCCP	A159	SA2	B159	VCCL2
A077	D21*	B077	D22*	A160	VCC3.3	B160	SCLK
A078	GND	B078	D19*	A161	GND	B161	SDAT
A079	D16*	B079	VCCP	A162	SA1	B162	VCCL2
A080	D13*	B080	D18*	A163	SA0	B163	RESERVED (nc)
A081	GND	B081	D20*	A164	GND	B164	RESERVED (nc)
A082	TEST_VTT (pu)	B082	VCCP	A165	PWR_EN0	B165	RESERVED (nc)
A083	RESERVED (nc)	B083	RESERVED (nc)				

Notes:

† Pins are numbered with respect to the module edge connector. Axx signals appear on the front (processor side) of the processor card. For mechanical specifications, see Section 12.

†† Signals that have no connection except for a pullup resistor to 2.5 volts are labeled with the signal mnemonic followed by “(pu).”

* Signal is active low.

11.6.2 Processor Termination/Regulation/Power

The termination circuitry required by the Intel Pentium III Xeon processor bus (AGTL+) signaling environment, and the circuitry to set the AGTL+ reference voltage, are implemented directly on the processor cards. The baseboard provides 1.5 V AGTL+ termination power (VTT), and VRM 8.3-compliant DC-to-DC converters to provide processor power (VCCP) at each connector. The baseboard provides three embedded and three VRM sockets to power the processors, which derive power from the +5 V and 12 V supplies. Each processor has a separate VRM to power its core; however, two processors share a VRM to power their cache. For more information, see the *VRM 8.3 DC-DC Converter Specification.*

11.6.3 Processor Voltage Regulator Module Connectors (J2A2, J2B1, J2C1)

Table 11-8: Add-in VRM Connector Pin Listing

Pin	Signal	Type †	Description
A1	P5VIN1	POWER	
A2	P5VIN2	POWER	
A3	P5VIN3	POWER	
A4	P12VIN1	POWER	
A5	P12VIN3	POWER	
A6	P1SHARE		
A7	VID0	OUT	
A8	VID2	OUT	
A9	VID4	OUT	
A10	VCCP1	POWER	
A11	VSS1	POWER	
A12	VCCP2	POWER	
A13	VSS2	POWER	
A14	VCCP3	POWER	
A15	VSS3	POWER	
A16	VCCP4	POWER	
A17	VSS4	POWER	
A18	VCCP5	POWER	
A19	VSS5	POWER	
A20	VCCP6	POWER	
B1	P5VIN4	POWER	
B2	P5VIN5	POWER	
B3	P5VIN6	POWER	
B4	P12VIN2	POWER	
B5	RES		
B6	OUTEN	OUT	
B7	VID1	OUT	
B8	VID3	OUT	
B9	PWRGOOD		
B10	VSS6	POWER	

Pin	Signal	Type †	Description
B11	VCCP7	POWER	
B12	VSS7	POWER	
B13	VCCP8	POWER	
B14	VSS8	POWER	
B15	VCCP9	POWER	
B16	VSS9	POWER	
B17	VCCP10	POWER	
B18	VSS10	POWER	
B19	VCCP11	POWER	
B20	VSS11	POWER	

11.6.4 Termination Card

CAUTION: A termination card *must* be installed in any vacant processor card slot to ensure reliable system operation.

The termination card contains AGTL+ termination circuitry, clock signal termination, and Test Access Port (TAP) bypassing for the vacant connector. The system will not boot unless all slots are occupied with a processor or termination card.

For signal descriptions, see the specific processor Electrical and Mechanical Technical Specification (EMTS).

11.7 System Management Interfaces

11.7.1 Server Monitor Module Connector (J7H1)

The baseboard supports the Server Monitor Module feature connector. The table below shows the pinout of the 26-pin baseboard connector.

Note: On the SKA4 baseboard, pins 1, 9, 15, and 17 are connected to **SMI_L**, **NMI, SECURE_MODE**, and **CHASSIS_INTRUSION**, but these signals are not monitored on any existing or planned SM module.

Table 11-9: Server Monitor Module Connector Pinout

Pin	Signal	Type †	Description—SKA4 Implementation
1	SMI_L	out	System Management Interrupt: not supported on SMM
2	I2C_SCL	in	I^2C clock line
3	CONP_L	out	Connector Present: tied to ground on the baseboard
4	Reserved		Reserved pin: NC on baseboard
5	PWR_CNTL_L	in	Power supply on/off control: allows SMM to control system power
6	I2C_SDA	in/out	I^2C serial data line
7	5VSTNDBY	out	+5 V standby: monitored by SMM to determine if AC power is applied
8	Reserved		Pulled up to 5 V through 10k on baseboard
9	NMI	out	Non-maskable interrupt: not supported on SMM

Pin	Signal	Type †	Description—SKA4 Implementation
10	HOST_AUX	out	Baseboard voltage monitored by SMM card: connected to 3.3 V
11	RESET_L	in	Baseboard reset signal from Server Monitor Module
12	GROUND	ground	Ground
13	GROUND	ground	Ground
14	Key		No connect on baseboard
15	SECURE_MODE	out	Secure mode indication: not supported on SMM
16	GROUND	ground	Ground
17	CHASSIS_INTRUSION	out	Chassis intrusion indication: not supported on SMM
18	Reserved		Reserved pin: NC on baseboard
19	Reserved		Reserved pin: NC on baseboard
20	GROUND	ground	Ground
21	Reserved		Reserved pin: NC on baseboard
22	Reserved		Reserved pin: NC on baseboard
23	Reserved		Reserved pin: NC on baseboard
24	Reserved		Reserved pin: NC on baseboard
25	key		No connect on baseboard
26	Reserved		Reserved pin: NC on baseboard

Notes:
† Type (in/out) is from the perspective of the baseboard.

11.7.2 SM Bus Connector (J9E4)

This header allows connection to the memory module I^2C bus that the DIMMs EEPROMs reside on. See the SKA4 Server Board SDRAM Memory Module section for more details on this I^2C bus.

WARNING: A shorted I^2C connection at the SM bus I^2C connector will prevent the system BIOS from sizing and configuring main memory.

Table 11-10: SMB Connector (J9E4)

Pin	Signal	Description
1	Local I2C SDA	OSB4 SM Bus Data Line
2	GROUND	
3	Local I2C SCL	OSB4 SM Bus Clock Line

11.7.3 ICMB Connector (J1D2)

The external Intelligent Chassis Management Bus provides external access to ICMB devices that are within the chassis. This makes it possible to externally access chassis management functions, alert logs, post-mortem data, etc. It also provides a mechanism for chassis power control. As an option, the server can be configured with an ICMB adapter board to provide two SEMCONN 6-pin connectors to allow daisy chained cabling.

Table 11-11: ICMB Connector Pinout (J1D2)

Pin	Signal	Type	Description
1	SDA	Signal	IPMB I^2C* Data
2	Ground	Power	
3	SCL	Signal	IPMB I^2C Clock
4	5 V standby	Power	

11.7.4 Auxiliary I^2C* Connector (J9E4)

The baseboard provides a 3-pin auxiliary I^2C connector for OEM access to the IPMB. This connector is not isolated when power is off. Any devices connected must remain powered in this state or the BMC will not work properly.

WARNING: A shorted I^2C connection at the auxiliary I^2C connector will prevent restoration of main power because the BMC needs the bus to boot the server from standby power.

Table 11-12: IMB Connector Pinout (J8F1)

Pin	Signal	Description
1	Local I2C SDA	BMC IMB 5VSTNDBY Clock Line
2	GROUND	
3	Local I2C SCL	BMC IMB 5VSTNDBY Data Line

11.8 Baseboard Fan Connectors (J3C1, J3A1, J4A1, J4C1)

There are four fan connectors located on the baseboard. These connectors are to be used for additional processor cooling if needed.

Note: The SKA4 board set only supports monitoring a total of eight tachometer fan inputs. The front panel connector provides connections to all eight tachometer fan inputs. The tachometer signals from these four processor fan connectors are connected to the same tachometer fan signals FAN_TACH(4), FAN_TACH(5), FAN_TACH(6), FAN_TACH(7) provided on the front panel connector J9E3. Care should be taken to ensure only one connection is utilized at any given time.

Table 11-13: Processor Fan Connector #1 (J3C1)

Pin	Signal	Type	Description
1	Ground	power	GROUND is the power supply ground
2	12V	power	Power Supply 12V
3	Fan Tach	out	FAN_TACH signal is connected to the BMC to monitor the FAN speed

Table 11-14: Processor Fan Connector #2 (J3A1)

Pin	Signal	Type	Description
1	Ground	power	GROUND is the power supply ground
2	12V	power	Power Supply 12V
3	Fan Tach	out	FAN_TACH signal is connected to the BMC to monitor the FAN speed

Table 11-15: Processor Fan Connector #3 (J4A1)

Pin	Signal	Type	Description
1	Ground	power	GROUND is the power supply ground
2	12V	power	Power Supply 12V
3	Fan Tach	out	FAN_TACH signal is connected to the BMC to monitor the FAN speed

Table 11-16: Processor Fan Connector #4 (J4C1)

Pin	Signal	Type	Description
1	Ground	power	GROUND is the power supply ground.
2	12V	power	Power Supply 12V
3	Fan Tach	out	FAN_TACH signal is connected to the BMC to monitor the FAN speed

11.9 Internal I/O Bus Connections

11.9.1 Internal Disk Drive LED Connection

This connector allows external drive controllers the ability to blink the front panel disk drive activity LED.

Table 11-17: Internal Disk Drive LED Connector

Pin	Signal	Description
1	NC	No Connect
2	Activity Signal	5V, High True Activity Signal
3	Activity Signal	Same as Pin 2 (Shorted to pin 2)
4	NC	No Connect

11.10 Standard I/O Panel

The following diagram shows the locations of serial, parallel, video, keyboard, and mouse connector interfaces on the system I/O panel, as viewed from the rear of the system.

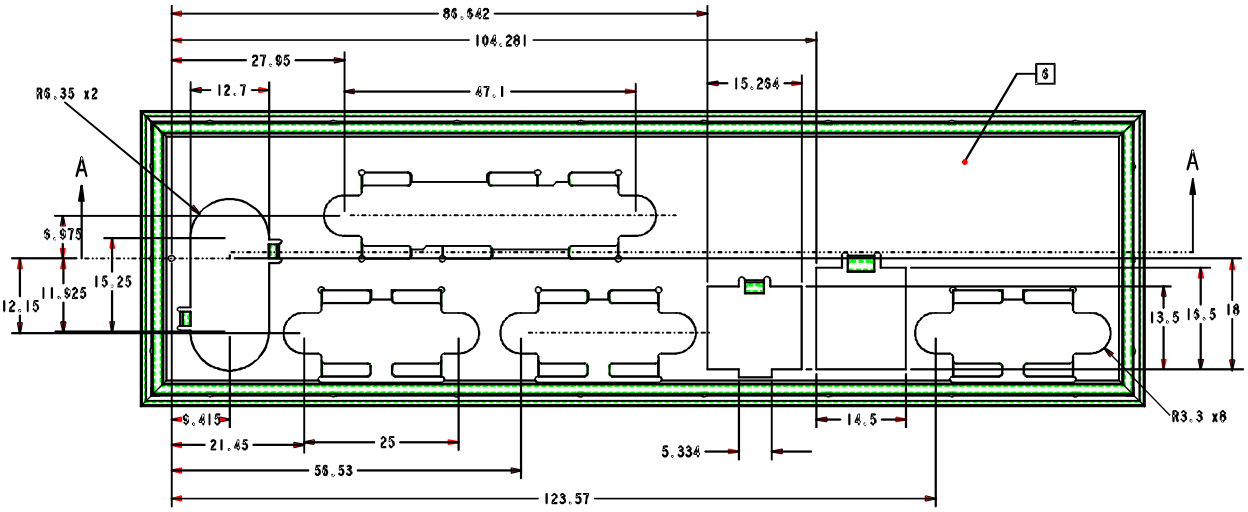


Figure 11-2: SKA4 I/O Panel Connector Location Dimensions

The next diagram shows a graphical representation with identification of the physical connections at the I/O panel.

Figure 11-3: SKA4 I/O Panel Connector Graphical Locations

11.10.1 Keyboard and Mouse Ports

These identical PS/2 compatible ports share a common housing. The top one is labeled mouse and the bottom one is labeled keyboard, although the board set supports swapping these connections.

Table 11-18: Keyboard and Mouse Ports

Mouse		Keyboard	
Pin	**Signal**	**Pin**	**Signal**
1	MSEDAT (mouse data)	1	KEYDAT (keyboard data)
2	No connection	2	No connection
3	GND (ground)	3	GND (ground)
4	Fused VCC (+5 V)	4	Fused VCC (+5 V)
5	MSECLK (mouse clock)	5	KEYCLK (keyboard clock)
6	No connection	6	No connection

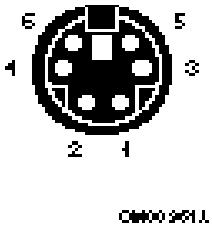


Figure 11-4: Keyboard or Mouse Connector

11.10.2 Serial Ports

The baseboard provides two RS-232C serial ports (COM1 is to the left, COM2 is to the right). They are D-subminiature 9-pin connectors. Each serial port can be enabled separately with the configuration control provided on the baseboard.

The COM2 serial port can be used either as an emergency management port (EMP) or as a normal serial port. As an emergency management port, COM2 is used as a communication path by the Server Management RS-232 connection to the baseboard management controller. This provides a level of emergency management through an external modem. The RS-232 connection can be monitored by the BMC when the system is in a powered down (standby) state.

Table 11-19: Serial Port Connector

Pin	Signal
1	DCD (carrier detect)
2	RXD (receive data)
3	TXD (transmit data)
4	DTR (data terminal ready)
5	GROUND
6	DSR (data set ready)
7	RTS (request to send)
8	CTS (clear to send)
9	RIA (ring indicator)

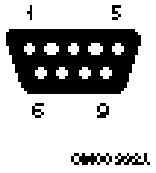


Figure 11-5: Serial Port Connector

11.10.3 Parallel Port

The IEEE 1284-compatible parallel port—used primarily for a printer—sends data in parallel format. The parallel port is accessed through a D-subminiature 25-pin connector.

Table 11-20: Parallel Port Connector

Pin	Signal	Pin	Signal
1	STROBE_L	14	AUFDXT_L (auto feed)
2	Data bit 0	15	ERROR_L
3	Data bit 1	16	INIT_L (initialize printer)
4	Data bit 2	17	SLCTIN_L (select input)
5	Data bit 3	18	GND (ground)
6	Data bit 4	19	GND
7	Data bit 5	20	GND
8	Data bit 6	21	GND
9	Data bit 7	22	GND
10	ACK_L (acknowledge)	23	GND
11	BUSY	24	GND
12	PE (paper end)	25	GND
13	SLCT (select)		

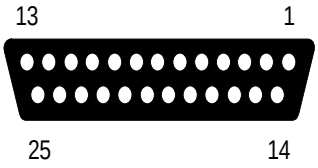


Figure 11-6: Parallel Port Connector

11.10.4 Video Port

The video port interface is a standard VGA compatible 15-pin connector. Onboard video is supplied by an ATI Rage2C_VT4 video controller with 2 MB of onboard video SGRAM.

Table 11-21: Video Connector

Pin	Signal
1	Red (analog color signal R)
2	Green (analog color signal G)
3	Blue (analog color signal B)
4	No connection
5	GND
6	GND
7	GND
8	GND
9	Fused VCC (+5V)
10	GND
11	No connection
12	DDCDAT
13	HSYNC (horizontal sync)

Pin	Signal
14	VSYNC (vertical sync)
15	DDCCLK

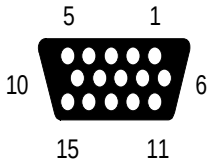


Figure 11-7: Video Connector

11.10.5 Universal Serial Bus Interface

The baseboard provides two stacked USB ports (Port 0 on top, Port 1 on bottom). The built-in USB ports permit the direct connection of two USB peripherals without an external hub. If more devices are required, an external hub can be connected to either of the built-in ports.

Table 11-22: Dual USB Connector

Pin	Signal
A1	Fused VCC (+5V /w over current monitor of both port 0 and 1)
A2	DATAL0 (Differential data line paired with DATAH0)
A3	DATAH0 (Differential data line paired with DATAL0)
A4	GND
B1	Fused VCC (+5V /w over current monitor of both port 0 and 1)
B2	DATAL1 (Differential data line paired with DATAH1)
B3	DATAH1 (Differential data line paired with DATAL1)
B4	GROUND

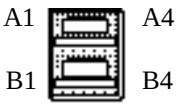


Figure 11-8: Dual USB Connector

11.10.6 Ethernet Connector

The system supports one 10/100Mbps TX based onboard Ethernet connection.

Table 11-23: Ethernet Connector

Pin	Signal
1	TXP
2	TXM
3	RXP
4	
5	
6	RXM
7	
8	

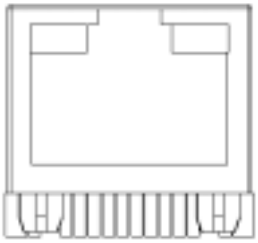


Figure 11-9: Ethernet Connector

The 82559 drives LEDs on the network interface connector that indicate transmit/receive activity on the LAN, a valid link to the LAN, and 10- or 100-Mbps operation. The green LED (left) indicates network connection when on and TX/RX activity when blinking. The yellow LED indicates 100-Mbps operation when lit.

11.11 Connector Manufacturers and Part Numbers

The following table shows the quantity and manufacturers' part numbers for connectors on the baseboard. Item numbers reference the circled numbers on the mechanical drawing. Refer to manufacturers' documentation for more information on connector mechanical specifications.

Table 11-24: Baseboard Connector Manufacturer Part Numbers

J #'s	Qty	Manufacturer and Part #	Description (Functional)
J9G1	1	AMP*; 146225-3	BMC FLASH BOOT BLOCK WRITE ENABLE (1X3 HEADER)
		FOXCONN/HON HAI*; HB1903G	
J9F2	1	TBD	PRODUCTION JUMPER BLOCK
J9F1	2	AMP; 1-146218-2	EVALUATION JUMPER BLOCK (NOT STUFFED)
J1B3	1	TBD	INTERNAL USB CONNECTOR
J2D1, J2E1	2	FOXCONN/HON HAI; EH06011-PC-W	32-BIT PCI CONNECTOR
J4G2, J4H1, J4H2, J4J1	4	AMP; 145034-1	64-BIT PCI CONNECTOR (5-VOLT)
J4F1, J4G1	2	AMP; 145168-4	64-BIT PCI CONNECTOR (3.3-VOLT)
J1A1	1	AMP; 84405-1	STACKED PS2 KEYBOARD & MOUSE
		FOXCONN/HON HAI; MH11067-D5	
J9E3	1	FOXCONN/HON HAI; HL17156	FRONT PANEL HEADER (2X15)
J7H1	1	AMP; 11970-6	SERVER MANAGEMENT FEATURE HEADER (2X13)
J7J1	1	FOXCONN/HON HAI; HL11256-D6	NARROW SCSI CONNECTOR (2X25)
J9E6	1	FOXCONN/HON HAI; HL16176-P4	FLOPPY DRIVE CONNECTOR (2X17)
		MOLEX*; 87256-3456	
		MOLEX; 0872563456	
J9E5	1	FOXCONN/HON HAI; HL16206-D2	IDE CONNECTOR (2X20)
		MOLEX; 87256-4056	
		MOLEX; 0872564056	
J3D1	1	FOXCONN/HON HAI; HL17106	HOT PLUG PCI STATUS INDICATOR HEADER (2X10)
J9E1	1	AMP; 640456-4	HARD DISK DRIVE ACTIVITY HEADER (1X4)
J3A1, J3C1, J4A1, J4C1	4	FOXCONN/HON HAI; HF08030-P1	AUX / CPU FAN HEADER (1X3)
J1B2	1	FOXCONN/HON HAI; DM11356-R1	PARALLEL PORT CONNECTOR (RIGHT ANGLE)
J4D1	1	AMP; 104864-4	ITP HEADER (2X15) (Not Stuffed in Production)
J1A2, J1B2	2	FOXCONN/HON HAI; DT10126-R9	SERIAL PORT (RIGHT ANGLE)
		AMP; 787650-4	
J1C1	1	AMP; 1116075-4	RJ45 (NIC) CONNECTOR (RIGHT ANGLE)
J9G2, J9H1	2	MOLEX; 71061-0003	WIDE SCSI CONNECTOR (RIGHT ANGLE)
J6J1	1	FOXCONN/HON HAI; QA01343-P4	WIDE SCSI CONNECTOR (STRAIGHT)
J8F1, J9E4	2	MOLEX; 22-44-7031	I2C HEADER (1X3)
		MOLEX; 0022447031	
J1C2	1	AMP; 787745-2	DUAL USB CONNECTOR (RIGHT ANGLE)
		FOXCONN/HON HAI; UB1112C-NO	
J1D1	1	FOXCONN/HON HAI; DZ11A36-R9	VIDEO CONNECTOR (RIGHT ANGLE)
J1D2	1	TBD	ICMB Connector
J2A2, J2B1, J2C1	3	BERG*; 95798-202	PLUG IN VOLTAGE REGULATOR CONNECTOR
J9B1	1	MOLEX; 39-29-9202	BOARD POWER CONNECTOR A (2X10)
		MOLEX; 0039299202	
J9D1	1	MOLEX; 44206-0001	BOARD POWER CONNECTOR B (2X12)
		MOLEX; 0442060001	
J9B2	1	AMP; 111950-2	AUX POWER CONNECTOR (2X7)
J6F1, J7A1, J7B1, J7C1, J7D1	5	MOLEX; 71109-5005	330 PIN SC330.1 PROCESSOR AND MECC CONNECTORS
		MOLEX; 0711095005	
XBH2A1	1	SONY ELECTRONICS*; HL32-E2R	BATTERY HOLDER
		RENATA BATTERIES U.S.*; HU2032-1	

12. Electrical, Thermal, and Mechanical Specifications

This chapter specifies the operational parameters and physical characteristics for the SKA4 server board. This is a board-level specification only. System specifications are beyond the scope of this document.

12.1 Absolute Maximum Electrical and Thermal Ratings

Operation of the SKA4 board set at conditions beyond those shown in the following table may cause permanent damage to the system (provided for stress testing only). Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 12-1: Absolute Maximum Electrical and Thermal Specifications

Operating Temperature	5°C to +50°C †
Storage Temperature	-55°C to +150°C
Voltage on any signal with respect to ground	-0.3V to V_{DD} + 0.3V ††
3.3V supply voltage with respect to ground	-0.3 to +3.63V
5V supply voltage with respect to ground	-0.3 to +5.5V

Notes:
† Chassis design must provide proper airflow to avoid exceeding Pentium III Xeon 100-MHZ FSB maximum case temperature.
†† V_{DD} means supply voltage for the device.

The table lists the maximum component case temperatures for baseboard components that could be sensitive to thermal changes. Case temperatures could be affected by the operating temperature, current load, or operating frequency. Maximum case temperatures are important when considering proper airflow to cool the motherboard.

CAUTION: An ambient temperature that exceeds the board's maximum operating temperature by 5°C to 10°C might cause components to exceed their maximum case temperature. When determining system compliance, consideration should be given for maximum rated ambient temperatures.

Table 12-2: Thermal Specification for Key Components

Component	Maximum Temperature
Pentium® III Xeon™ 1M and 2M Cache 100-MHz FSB processor	65°C (thermal plate)
CNB20HE	80°C (case)
CIOB	80°C (case)
MADP	90°C (case)
ROSB4	90°C (case)
Lithium battery	70°C (case)

12.2 Airflow Specification for CIOB and HE

HE Heat Sink:

- Maximum Operating Ambient: 40°C.
- Minimum Airflow Requirement: 1.5m/s.

CIOB Heat Sink:

- Maximum Operating Ambient: 44°C.
- Minimum Airflow Requirement: 1m/s.

12.3 Electrical Specifications

DC and AC specifications for SKA4 are summarized here.

12.3.1 Power Consumption

The following table shows the power consumed on each supply line for a combined SKA4 server baseboard and memory module. These numbers are for budgetary use and are calculated based on worst case use.

These numbers do not include any processors, memory or add-in peripherals or cards.

Note: The three onboard voltage regulators for the primary processor's VCCcore and all four processors' VCC cache are derived for the 5V rail. These regulators are budgeted at 85% efficiency. Therefore all power consumed on these pins (P1 VCCcore and P1, P2, P3 and P4 VCCcache) will result in a 15% power loss not reflected in the numbers below.

Table 12-3: SKA4 Baseboard and Memory Module Power Consumption

Voltage Rails	3.3V	+5V	+12V	-12V	5V Standby
Maximum Current (A)	12.2A	7A + VRM inefficiency (see note above)	1.5A	.1A	1.3A

For your system or configured calculations, add the power consumed by all devices plugged into the SKA4 server board set.

12.3.2 Power Supply Specifications

This section provides power supply design guidelines for an SKA4-based system, including voltage and current specifications, and power supply on/off sequencing characteristics.

Table 12-4: SKA4 Server Power Supply Voltage Specification

Item	Min	Nom	Max	Units	Tolerance
3.3 Volts	3.15	3.30	3.46	V	+/- 5%
5 Volts	4.75	5.00	5.25	V	+/- 5%
+12 Volts	11.40	12.00	12.60	V	+/- 5%
-12 Volts	-11.40	-12.00	-12.60	V	+/- 5%

Item	Min	Nom	Max	Units	Tolerance
-5 Volts	-4.75	-5.00	-5.25	V	+/- 5%
5 Volts Standby	+4.75	+5.00	+5.25	V	+/- 5%

12.3.3 Power Timing

These are the timing requirements for single power supply operation.

The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 5 to 200 ms. The +3.3V, +5V and +12V output voltages should start to rise approximately at the same time. All outputs must rise monotonically. The +5V output needs to be greater than the +3.3V output during any point of the voltage rise, however, never by more than 2.25V. Each output voltage shall reach regulation within 100 ms (T_{vout_on}) of each other and begin to turn off within 100 ms (T_{vout_on}) of each other. The table below shows the output voltage timing parameters.

The second table below shows the timing requirements for a single power supply being turned on and off via the AC input, with PSON held low and the PSON signal, with the AC input applied. The $ACOK^{\#}$ signal is not being used to enable the turn on timing of the power supply.

Table 12-5: Voltage Timing Parameters

Item	Description	Min	Max	Units
T_{vout_rise}	Output voltage rise time from each main output.	5	200	msec
T_{vout_on}	All main outputs must be within regulation of each other within this time.		100	msec

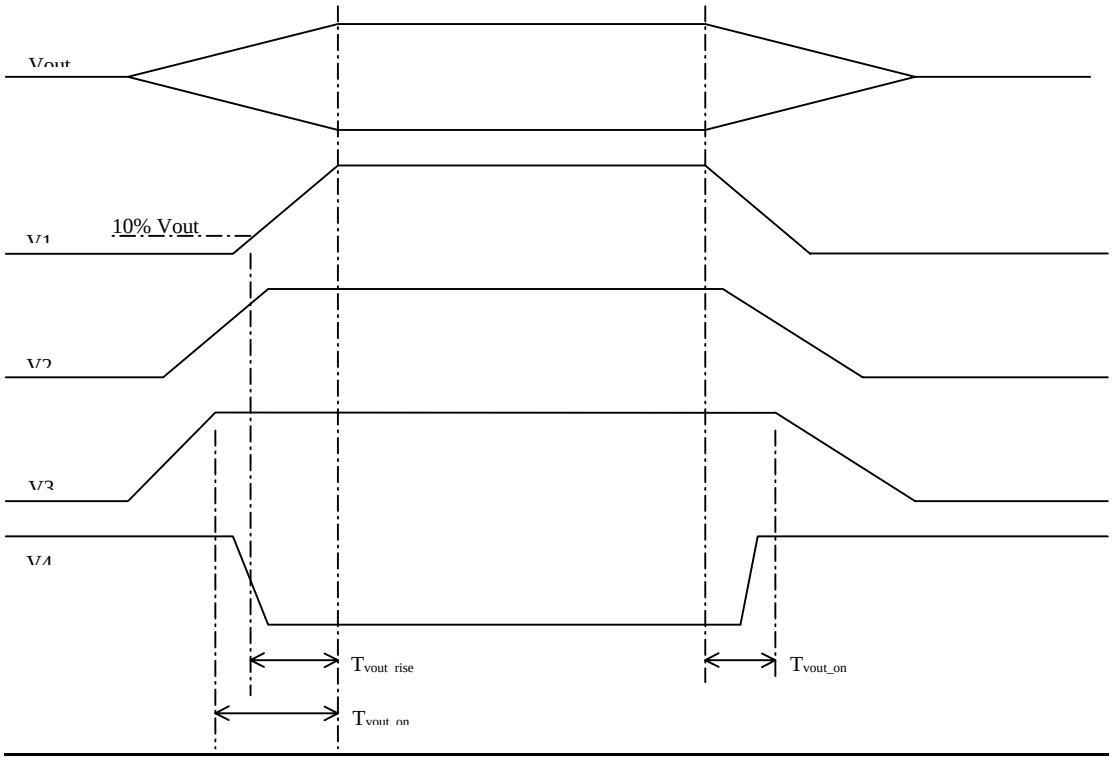


Figure 12-1: Output Voltage Timing

Table 12-6: Turn On/Off Timing

Item	Description	MIN	MAX	UNITS
$T_{sb\_on\_delay}$	Delay from AC being applied to 5VSB being within regulation.			msec
$T_{ac\_on\_delay}$	Delay from AC being applied to all output voltages being within regulation.		2500	msec
T_{vout_holdup}	Time all output voltages, including 5VSB, stay within regulation after loss of AC.	21		msec
T_{pwok_holdup}	Delay from loss of AC to deassertion of PWOK	20		msec
$T_{pson\_on\_delay}$	Delay from PSON# active to output voltages within regulation limits.	5	400	msec
T_{pson_pwok}	Delay from PSON# deactive to PWOK being deasserted.		50	msec
T_{acok_delay}	Delay from loss of AC input to deassertion of ACOK#.	20		msec
T_{pwok_on}	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	1000	msec
T_{pwok_off}	Delay from PWOK deasserted to output voltages (3.3V, 5V, 12V, -12V, 5VSB) dropping out of regulation limits.	1	200	msec

Item	Description	MIN	MAX	UNITS
T_{pwok_low}	Duration of PWOK being in the deasserted state during an off/on cycle using AC or the PSON signal.	100		msec

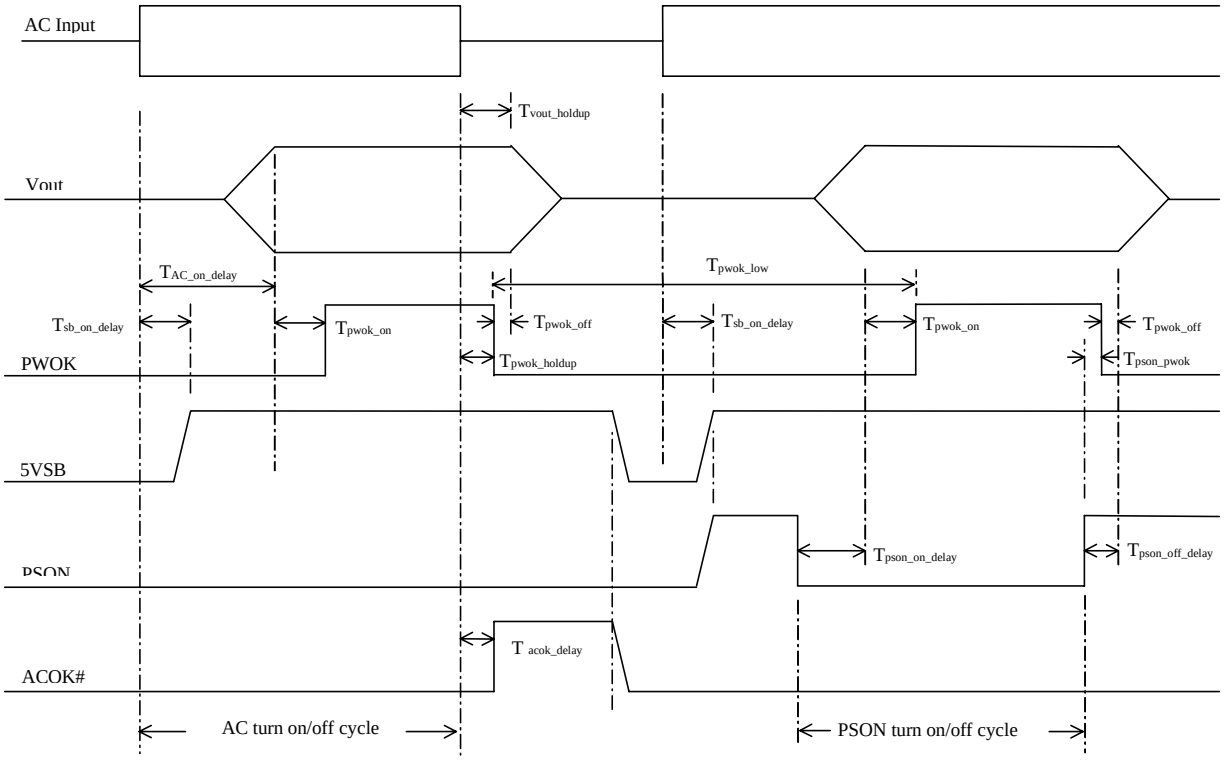


Figure 12-2: Turn On/Off Timing

12.3.4 Voltage Recovery Timing Specifications

The power supply must conform to the following specifications for voltage recovery timing under load changes:

1. Voltage shall remain within +/- 5% of the nominal set voltage on the +5V, +12V, 3.3V, -5V and -12V outputs, during instantaneous changes in load shown in the table below.

2. Voltage regulation limits shall be maintained over the entire AC input range and any steady state temperature and operating conditions specified.

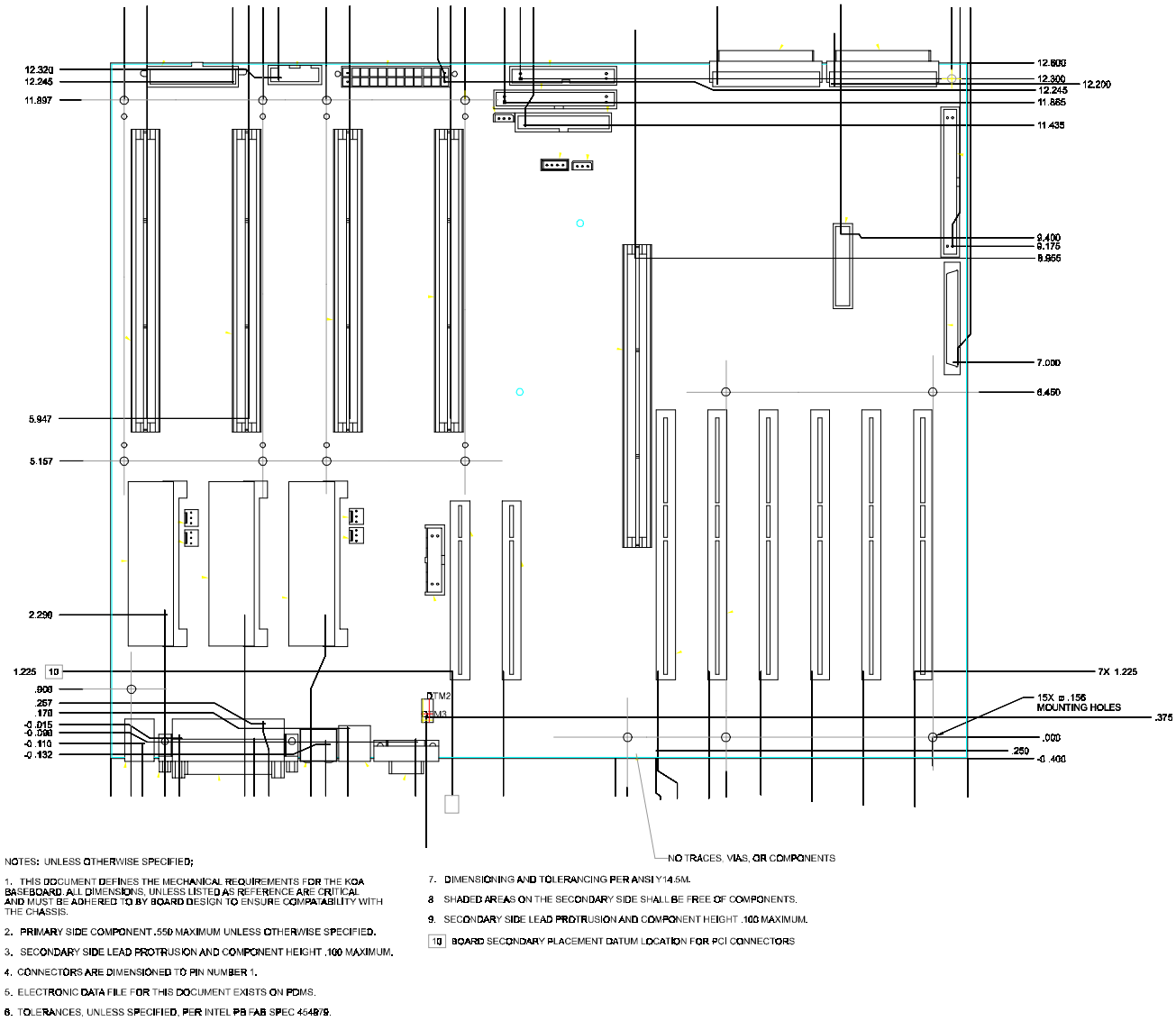
3. Voltages shall be stable as determined by bode plot and transient response. The combined error of peak overshoot, set point, regulation, and undershoot voltage shall be less than or equal to +/-5% of the output voltage setting. The transient response measurements shall be made with a load changing repetition rate of 50 Hz to 5 kHz. The load slew rate shall not be greater than 0.2A/µs.

Table 12-7: Transient Load Requirements

Output	Step Load Size	Starting Level	Finishing Level	Slew Rate
+3.3V	8.0 A	Min. Load	Min. load + 8.0A and step up to max. load	0.50A/µs
+5V	6.0 A	Min. Load	Min. load + 6.0A and step up to max. load	0.50 A/µs
+12V	7.0A	Min. Load Min. Load	Min. load + 7.0A and step up to max. load	0.50 A/µs
+5VSB	150mA	Min. Load	Min. load + 150mA and step up to max. load	0.1 A/us
-12V	250mA	Min. Load	Min load +250mA and step up to max. load	0.1 A/us

13. Mechanical Specifications

The following diagrams show the mechanical specifications of the SKA4 server baseboard. All dimensions are given in inches, and are dimensioned per ANSI Y15.4M. Connectors are dimensioned to pin 1.

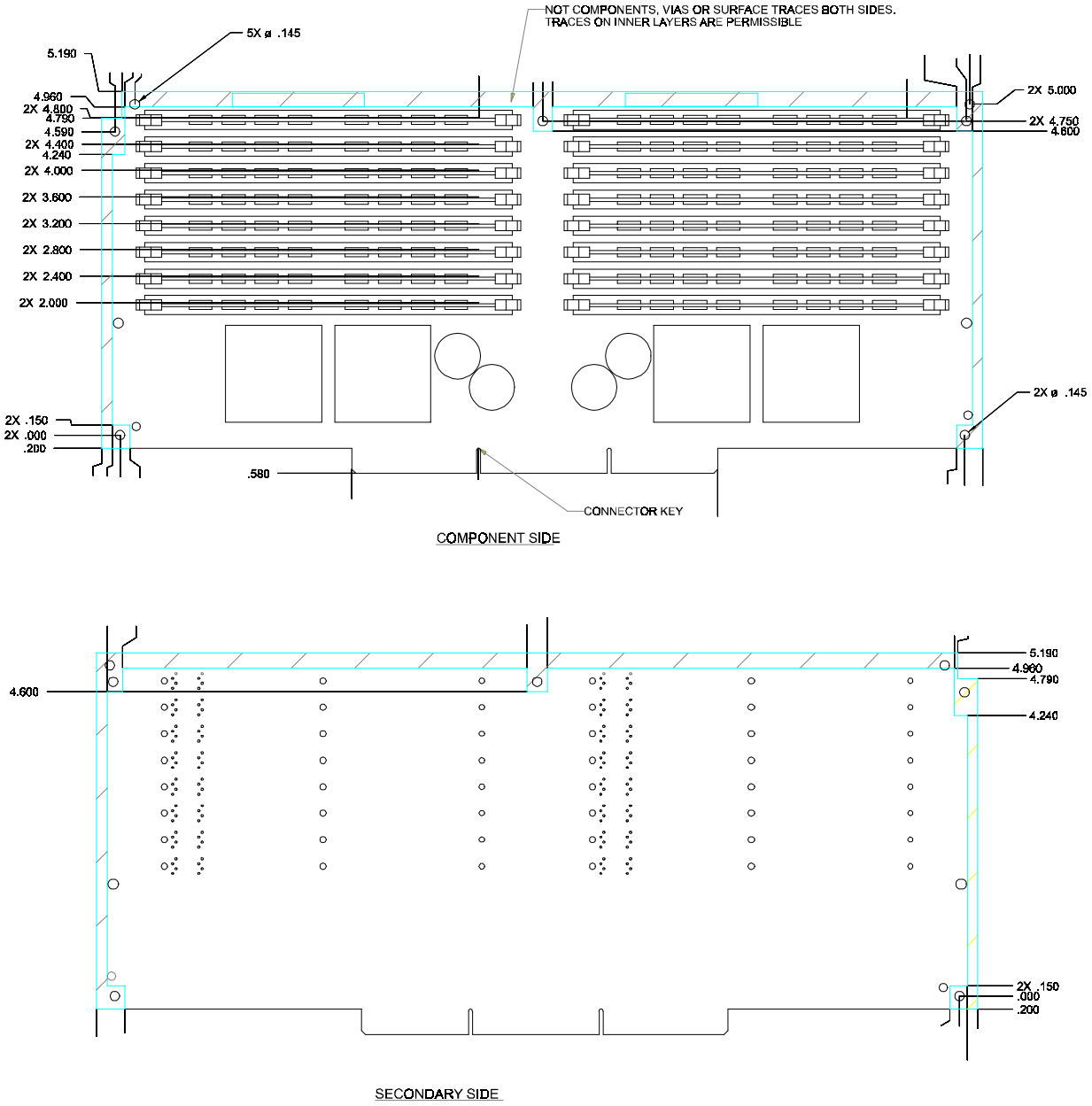


NOTES: UNLESS OTHERWISE SPECIFIED;

1. THIS DOCUMENT DEFINES THE MECHANICAL REQUIREMENTS FOR THE KOA BASEBOARD. ALL DIMENSIONS, UNLESS LISTED AS REFERENCE ARE CRITICAL AND MUST BE ADHERED TO BY BOARD DESIGN TO ENSURE COMPATABILITY WITH THE CHASSIS.
2. PRIMARY SIDE COMPONENT .550 MAXIMUM UNLESS OTHERWISE SPECIFIED.
3. SECONDARY SIDE LEAD PROTRUSION AND COMPONENT HEIGHT .100 MAXIMUM.
4. CONNECTORS ARE DIMENSIONED TO PIN NUMBER 1.
5. ELECTRONIC DATA FILE FOR THIS DOCUMENT EXISTS ON PDMS.
6. TOLERANCES, UNLESS SPECIFIED, PER INTEL PB FAB SPEC 454879.
7. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M.
8. SHADED AREAS ON THE SECONDARY SIDE SHALL BE FREE OF COMPONENTS.
9. SECONDARY SIDE LEAD PROTRUSION AND COMPONENT HEIGHT .100 MAXIMUM.

10 BOARD SECONDARY PLACEMENT DATUM LOCATION FOR PCI CONNECTORS

Figure 13-1: SKA4 Baseboard Mechanical Diagram



NOTES: UNLESS OTHERWISE SPECIFIED:

1. THIS DOCUMENT DEFINES THE MECHANICAL REQUIREMENTS OF THE KOA MEMORY BOARD. ALL DIMENSIONS, UNLESS LISTED AS REFERENCE ARE CRITICAL AND MUST BE ADHERED TO BY BOARD DESIGN TO ENSURE COMPATABILITY WITH CHASSIS.
2. PRIMARY SIDE COMPONENT 1.875 MAXIMUM UNLESS OTHERWISE SPECIFIED.
3. SECONDARY SIDE LEAD PROTRUSION AND COMPONENT HEIGHT .100 MAXIMUM.
5. ELECTRONIC DATE FILE FOR THIS DOCUMENT EXISTS IN PDMS.
4. COMPONENTS ARE DIMENSIONS TO PIN NUMBER 1.
6. TOLERANCE, UNLESS SPECIFIED, PER INTEL PB FAB SPEC 454979.
7. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M.
8. SHADED AREARS ON THE SECONDARY SIDE SHALL BE FREE OF COMPONENTS.
9 SEE INTEL DOCUMENT 695467 FOR BOARD EDGE DETAILS.

Figure 13-2: SKA4 Memory Module Mechanical Diagram

14. Regulatory and Integration Information

14.1 Regulatory Compliance

The SKA4 server board has been verified to comply with the following Safety and EMC regulations when correctly installed in a compatible Intel host system.

Table 14-1: Safety Regulations

Regulation	Title
UL 1950/CSA950	Bi-National Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA and Canada)
EN60950	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Community)
IEC60 950	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)
EMKO-TSE (74-SEC) 207/94	Summary of Nordic deviations to EN 60950. (Norway, Sweden, Denmark, and Finland)

Table 14-2: EMC Regulations

Regulation	Title
FCC Class A	Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, pertaining to unintentional radiators. (USA)
CISPR 22 (Class A)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (International)
VCCI Class A(ITE)	Implementation Regulations for Voluntary Control of Radio Interference by Data Processing Equipment and Electronic Office Machines. (Japan)
EN55022 (ClassA)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (Europe)
EN555024	ITE Generic Immunity Standard (Europe)
ICES-003	Interference-Causing Equipment Standard, Digital Apparatus, Class A (Including CRC c.1374) (Canada)

This printed circuit assembly has the following product certification markings:

- UL Joint Recognition Mark: Consists of small c followed by a stylized backward UR and followed by a small US (Component side).
- Manufacturer's recognition mark: Consists of a unique UL recognized manufacturer's logo, along with a flammability rating (94V-0) (Solder side).
- UL File Number for motherboards: E139761 (Component side).
- PB Part Number: Intel® bare circuit board part number XXXXXX-ZZZ (Solder side).
- Battery "+" marking: located on the component side of the board in close proximity to the battery holder.
- CE Mark: (Component side) The CE mark should also be on the shipping container.
- Australian C-Tick Mark: Consists of solid circle with white check mark and supplier code N232.

Installation Instructions

CAUTION: Follow these guidelines to meet safety and regulatory requirements when installing this board assembly.

Read and adhere to all of these instructions and the instructions supplied with the host computer and associated modules. If the instructions for the host computer are inconsistent with these instructions or the instructions for associated modules, contact the supplier's technical support to find out how you can ensure that your computer meets safety and regulatory requirements. If you do not follow these instructions and the instructions provided by host computer and module suppliers, you increase safety risk and the possibility of noncompliance with regional laws and regulations.

Ensure EMC

Before computer integration, make sure that the host chassis, power supply, and other modules have passed EMC certification testing.

In the installation instructions for the host chassis, power supply, and other modules, pay close attention to the following:

- Certifications.
- External I/O cable shielding and filtering.
- Mounting, grounding, and bonding requirements.
- Keying connectors when mismating of connectors could be hazardous.

If the host chassis, power supply, and other modules have not passed applicable EMC certification testing before integration, EMC testing must be conducted on a representative sample of the newly completed computer.

Ensure Host Computer and Accessory Module Certifications

Make sure that the host computer and any added subassembly (such as a board or drive assembly, including internal or external wiring) are certified for the region(s) where the end product will be used. Marks on the product are proof of certification. Certification marks are as follows:

In Europe

The CE marking signifies compliance with all relevant European requirements. If the host computer does not bear the CE marking, obtain a supplier's Declaration of Conformity to the appropriate standards required by the European EMC Directive and Low Voltage Directive. Other directives, such as the Machinery and Telecommunications Directives, may also apply depending on the type of product. No regulatory assessment is necessary for low voltage DC wiring used internally or wiring used externally when provided with appropriate overcurrent protection. Appropriate protection is provided by a maximum 8 Amp current limiting circuit or a maximum 5 Amp fuse or positive temperature coefficient (PTC) resistor. This Intel® server board has PTCs on all external ports that provide DC power externally.

In the United States

A certification mark by a Nationally Recognized Testing Laboratory (NRTL) such as UL, CSA,

or ETL signifies compliance with safety requirements. External wiring must be UL Listed and suitable for the intended use. Internal wiring must be UL Listed or Recognized and rated for applicable voltages and temperatures. The FCC mark (Class A for commercial or industrial only or Class B for residential) signifies compliance with electromagnetic interference requirements.

In Canada
A nationally recognized certification mark such as CSA or cUL signifies compliance with safety requirements. No regulatory assessment is necessary for low voltage DC wiring used internally or wiring used externally when provided with appropriate overcurrent protection. Appropriate protection is provided by a maximum 8 Amp current limiting circuit or a maximum approved 5 Amp fuse or positive temperature coefficient (PTC) resistor. This server board has PTCs on all external ports that provide DC power externally.

Prevent Power Supply Overload

Do not overload the power supply output. To avoid overloading the power supply, make sure that the calculated total current load of all the modules within the computer is less than the maximum output current rating of the power supply. If you do not do this, the power supply may overheat, catch fire, or damage the insulation that separates hazardous AC line circuitry from low voltage user accessible circuitry and result in a shock hazard. If the load drawn by a module cannot be determined by the markings and instructions supplied with the module, contact the module supplier's technical support.

Place Battery Marking on Computer

There is insufficient space on this server board to provide instructions for replacing and disposing of the battery. The following warning must be placed permanently and legibly on the host computer as near as possible to the battery.

> **⚠ WARNING**
> **Danger of explosion if battery is incorrectly replaced.**
>
> **Replace with only the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.**

Use Only for Intended Applications

This product was evaluated for use in ITE computers that will be installed in offices, schools, computer rooms and similar locations. The suitability of this product for other product categories other than ITE applications, (such as medical, industrial, alarm systems, and test equipment) may require further evaluation.

Installation Precautions

When you install and test the server board, observe all warnings and cautions in the installation instructions. To avoid injury, be aware of the following:

- Sharp pins on connectors.

- Sharp pins on printed circuit assemblies.
- Rough edges and sharp corners on the chassis.
- Hot components (like processors, voltage regulators, and heat sinks).
- Damage to wires that could cause a short circuit.
- Observe all warnings and cautions that instruct you to refer computer servicing to qualified technical personnel.

WARNING: Do not open the power supply. There is risk of electric shock and burns from high voltage and rapid overheating. Refer servicing of the power supply to qualified technical personnel.

14.2 Environmental Limits

14.2.1 System Office Environment

Table 14-3: Office System Environment Summary

Operating Temperature	+10°C to +35°C with the maximum rate of change not to exceed 10°C per hour
Non-Operating Temperature	-40°C to +70°C
Non-Operating Humidity	95%, non-condensing @ 30°C
Altitude De-rate	0.5° per 1000 feet
Acoustic noise	< 47 dBA with one power supply @ 28+-2°C < 50 dBA with two power supplies @ 28+-2°C < 55 dBA with three power supplies @ 28+-2°C
Operating Shock	No errors with a half sine wave shock of 2G (with 11 millisecond duration)
Package Shock	System operational after a 30" free fall, cosmetic damage may be present
ESD	20KV per Intel Environmental Test Specification

14.2.2 System Environmental Testing

The system environmental tests include the following:

- Temperature Operating and Non-Operating.
- Humidity Non-Operating.
- Shock Packaged and Unpackaged.
- Vibration Packaged and Unpackaged.
- AC Voltage, Freq. & Source Interrupt.
- AC Surge.
- Acoustics.
- ESD.

15. Reliability, Serviceability and Availability

The Intel® server system should be serviced only by a qualified technician. The desired Mean-Time-To-Repair (MTTR) of the system is 30 minutes including diagnosis of the system problem. To meet this goal, the system enclosure and hardware have been designed to minimize the MTTR. Following are the maximum times a trained field service technician should take to perform the listed system maintenance procedures, after diagnosis of the system.

Table 15-1: Serviceability Times

Remove cover	2 minutes
Remove and replace disk drive	1 minute
Remove and replace power supply	3 minutes
Remove and replace fan	5 minutes
Remove and replace expansion board	2 minutes
Remove and replace front panel board	10 minutes
Remove and replace baseboard (with no expansion boards)	15 minutes
Remove and replace power backplane	10 minutes
Remove and replace SCSI backplane	10 minutes
Replace memory module	3 minutes
Replace/add DIMMs	2 minutes
Replace/add processor	5 minutes
Replace/add ICMB	2 minutes
Overall MTTR	20 minutes

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Appendix A: Glossary

Term	Definition
ASIC	Application Specific Integrated Circuit
ASR	Asynchronous Reset
BMC	Baseboard Management Controller
BSP	Bootstrap Processor
EMP	Emergency Management Port
ESCD	Extended System Configuration Data
FRB	Fault Resilient Booting
FRU	Field Replaceable Unit
HPIB	Hot-plug Indicator Board
IMB	Intra Module Bus
IPMB	Intelligent Platform Management Bus
MADP	Memory Address and Data Path
MBE	Multiple Bit Error
MEC	Memory Expansion Card
MECC	Memory Expansion Card Connector
MP	Multiprocessor
MSR	Model Specific Register
MTTR	Mean Time To Repair
NIC	Network Interface Card
NMI	Non-maskable Interrupt
OS	Operating System
PHP	PCI Hot-plug
PHPC	PCI Hot-plug Controller
PME	Power Management Event
POST	Power On Self Test
RTC	Real Time Clock
SBE	Single Bit Error
SEC	Single Edge Contact
SEL	System Event Log
SGRAM	Synchronous Graphics RAM
SHV	Standard High Volume
SM	Server Management
SMM	Server Management Module
SSU	System Setup Utility
TAP	Test Access Port
TBD	To Be Determined
USB	Universal Serial Bus

Appendix B: Reference Documents

Refer to the following documents for additional information:

- *PCI Hot-plug Specification, Revision 1.0.*
- *RCC Champion 2.0 North Bridge (CNB20HE) Specification.*
- *RCC Champion 2.0 Open South Bridge (OSB4) Specification.*
- *RCC Champion 2.0 Memory Address and Data Path (MADP) Specification.*
- *RCC Champion 2.0 IO Bridge (CIOB) Specification.*
- *PCI Local Bus Specification, Revision 2.1.*
- *USB Specification, Revision 1.0.*
- *5 Volt Flash File (28F008SAx8) Datasheet.*
- *PCI Bus Power Management Interface Specification.*
- *AIC-7899 PCI-Dual Channel SCSI Multi-function Controller Data Manual.*
- *ATI Rage IIc Technical Reference Manual.*
- *I^2C Bus Specification.*
- *Intelligent Platform Management Bus Communications Protocol Specification.*
- *Compaq PCI Hot-Plug Megacell Specification, Draft Copy, Rev. AX.*
- *CK133-WS Synthesizer/Driver Specification.*
- *VRM 8.3 DC-DC Converter Specification.*
- *Adaptec AIC-7899 PCI Bus Master Dual-channel Ultra 160/M SCSI Host Adapter Chip Data Book.*
- *Adaptec AIC-7880 PCI Bus Master Single-chip SCSI Host Adapter Data Book.*
- *ATI-264 VT4 Graphics Controller Technical Reference Manual.*
- *Intel® 82559 Fast Ethernet Multifunction PCI/CardBus Controller Datasheet.*
- *Intelligent Platform Management Interface (IPMI) Specification.*
- *PCI Hot-Plug Application and Design,* Alan Goodrum, ISBN 0-929392-60-4, March 1998.
- *33-MHz PCI Hot-Plug Controller Application Guide, Rev A.*
- *66-MHz PCI Hot-Plug Controller Application Guide, Rev A.*
- *SSI Midrange Power Supply Specification.*